# MPQ3425-AEC1

## 3A, 55V Boost Converter with Programmable Switching Frequency, AEC-Q100 Qualified

## DESCRIPTION

The MPQ3425 is a current-mode, step-up converter with a 3.5A, 90mΩ internal switch that provides a highly efficient regulator with fast response. The MPQ3425 features a programmed frequency of up to 2MHz that provides easy filtering and low noise. An external compensation pin allows for flexibility in setting loop dynamics and operates with small, low ESR ceramic output capacitors. The soft-start feature provides a small inrush current and can be programmed with an external capacitor. The MPQ3425 operates with an input voltage as low as 3.1V and can generate 48V at up to 350mA from a 12V supply.

Full protection features include under-voltage lockout (UVLO), current limiting, and thermal overload protection. The MPQ3425 is available in a low-profile QFN-14 (3mmx4mm) package with an exposed pad.

## FEATURES

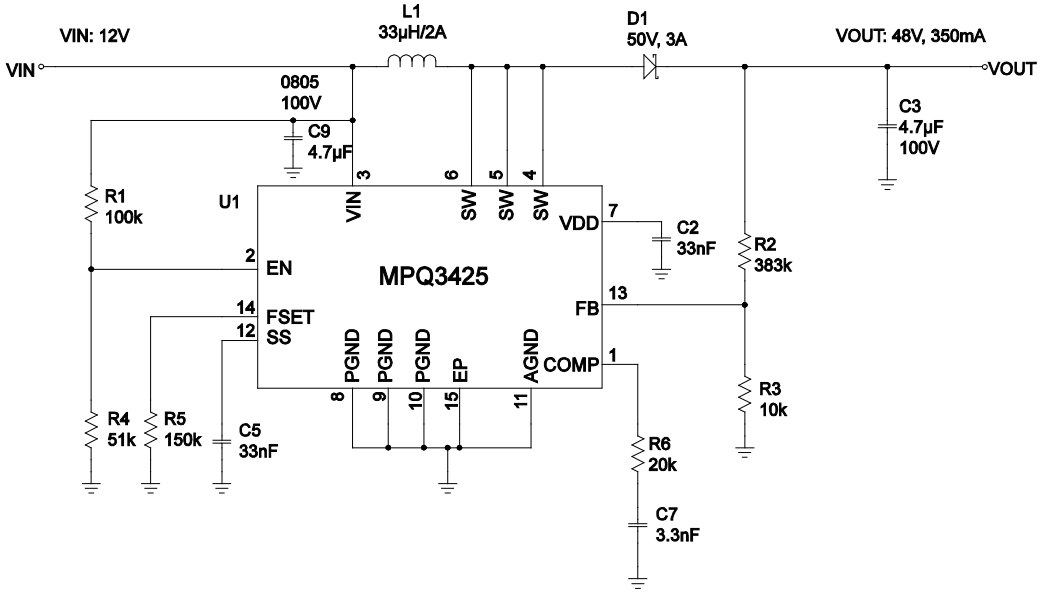
- Guaranteed Industrial and Automotive Temp Range Limits
- 3.5A, 90mΩ, 55V Power MOSFET
- Uses Small Capacitors and Inductors
- Wide Input Range: 3.1V to 22V
- Output Voltage up to 55V
- Programmable $F_{SW}$: 300kHz - 2MHz
- Programmable Under-Voltage Lockout (UVLO), Soft-Start, UVLO Hysteresis
- Micropower Shutdown <1μA
- Thermal Shutdown
- Available in a QFN-14 (3mmx4mm) Package
- AEC-Q100 Qualified Grade 1

## APPLICATIONS

- Telecom and Power Supplies
- Microphones and Tuner Bias
- Automotive



## TYPICAL APPLICATION

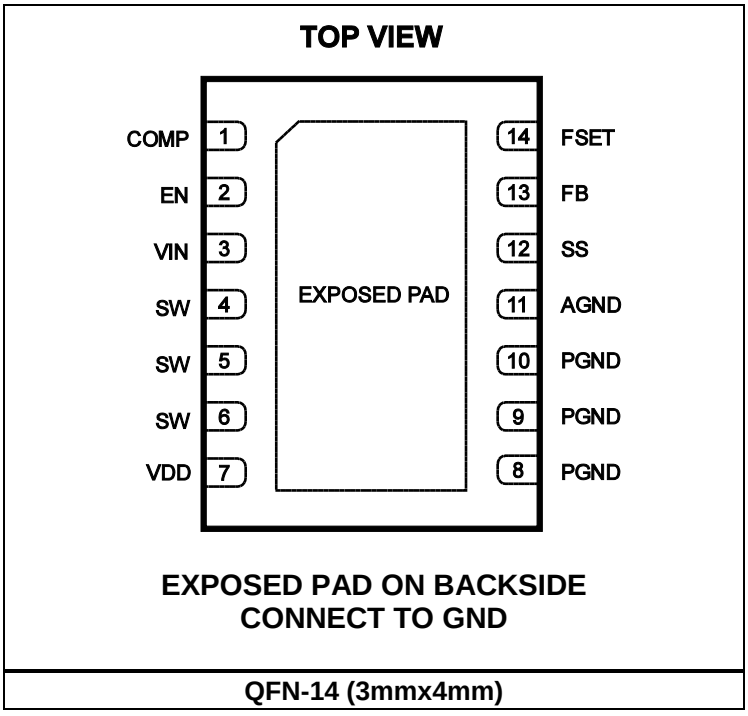


## ORDERING INFORMATION

| Part Number | Package | Top Marking |
|---|---|---|
| MPQ3425DL* | QFN-14 (3mmx4mm) | 3425 |
| MPQ3425DL-AEC1** | QFN-14 (3mmx4mm) | 3425 |

* For Tape & Reel, add suffix -Z (e.g. MPQ3425DL-Z)
For RoHS Compliant Packaging, add suffix -LF (e.g. MPQ3425DL-LF-Z)
** For Tape & Reel, add suffix -Z (e.g. MPQ3425DL-AEC1-Z)
For RoHS Compliant Packaging, add suffix -LF (e.g. MPQ3425DL-AEC1-LF-Z)

## PACKAGE REFERENCE




QFN-14 (3mmx4mm)

## ABSOLUTE MAXIMUM RATINGS (1)

SW ..... -0.5V to +55V
IN…… ..... -0.5V to +22V
All other pins..... -0.3V to +6.5V
Continuous power dissipation ($T_A$ = +25°C) (2)
QFN-14.....2.5W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

### *Recommended Operating Conditions* (3)

Supply voltage ($V_{IN}$) ..... 3.1V to 22V
Output voltage ($V_{OUT}$)..... 3.1V to 55V
Operating junct. temp ($T_J$)..... - 40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

QFN-14.....50 .....12 ...°C/W

**NOTES:**

1) Absolute maximum are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = $(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = $V_{EN}$ = 5V, $T_J$ = -40°C to +125°C. Typical values are $T_J$ = +25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Operating input voltage | $V_{IN}$ | | | 3.1 | | 22 | V |
| Under-voltage lockout | | $V_{IN}$ rising | $T_J$ = +25°C | 2.8 | | 3.1 | V |
| | | | $T_J$ = -40°C to +125°C | 2.75 | | 3.15 | |
| Under-voltage lockout hysteresis | | | | | 250 | | mV |
| VDD voltage gate driver voltage supply | $V_{VDD}$ | C = 10nF | | | | 6 | V |
| Supply current (shutdown) | $I_{IN-SD}$ | $V_{EN}$ = 0V | | | | 1 | µA |
| Supply current (quiescent) | $I_{IN}$ | $V_{FB}$ = 1.35V | $T_J$ = +25°C | | 650 | 900 | µA |
| | | | $T_J$ = -40°C to +125°C | | | 950 | |
| Switching frequency | $F_{SW}$ | FSET = 84.5kΩ | | 0.44 | 0.55 | 0.66 | MHz |
| Minimum off time | $T_{OFF}$ | $V_{FB}$ = 0V | | | 40 | | ns |
| Minimum on time (4) | $T_{ON}$ | $V_{FB}$ = 1.35V | | | 100 | | ns |
| EN high threshold | | $V_{EN}$ rising (switching) | $T_J$ = +25°C | 1.45 | 1.5 | 1.55 | V |
| | | | $T_J$ = -40°C to +125°C | 1.4 | | 1.6 | |
| EN high threshold | | $V_{EN}$ rising (micro power) | | | | 1.0 | V |
| EN low threshold | | | $T_J$ = +25°C | 0.5 | | | V |
| | | | $T_J$ = -40°C to +125°C | 0.45 | | | |
| EN input bias current | | $V_{EN}$ = 0V, 5V | | | 0.1 | 1 | µA |
| UVLO hysteresis current into EN | | 1.0 < EN < 1.4 | | | 4 | | µA |
| Soft-start current | $I_{SS}$ | | | | 6 | | µA |
| FB voltage | $V_{FB}$ | | $T_J$ = +25°C | 1.200 | 1.225 | 1.250 | V |
| | | | $T_J$ = -40°C to +125°C | 1.19 | | 1.26 | |
| FB input bias current | | | | -200 | -100 | | nA |
| Error amp voltage gain (4) | $A_{VEA}$ | | | | 300 | | V/V |
| Error amp transconductance $(\frac{\mu A}{V})$ (4) | $G_{EA}$ | | | | 160 | | µA/V |
| Error amp output current (4) | | | | | 20 | | µA |
| GCS: I(SW) / $V_{COMP}$ (4) | $G_{CS}$ | | | | 9 | | A/V |
| SW on resistance | $R_{ON}$ | | | | 90 | | mΩ |
| SW current limit | $I_{LIMIT}$ | Duty cycle = 0% | $T_J$ = +25°C | 3.5 | 5 | | A |
| | | | $T_J$ =-40°C to +125°C | 3 | | | |
| Thermal shutdown (4) | $T_{SD}$ | | | | 160 | | °C |

**NOTE:**

4) Guaranteed by design, not tested in production.

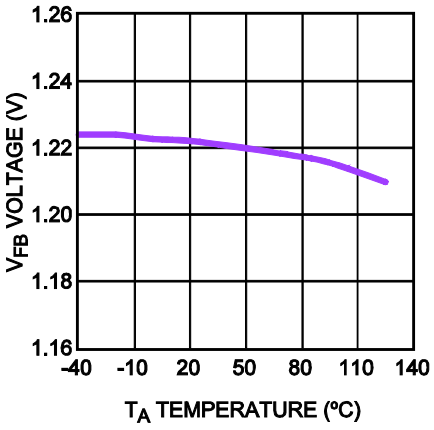
## PIN FUNCTIONS

| QFN-14 Pin # | Name | Description |
|---|---|---|
| 1 | COMP | **Compensation.** Connect a capacitor and resistor in series from COMP to AGND for loop stability. |
| 2 | EN | **Regulator on/off control input.** A high input at EN turns on the converter; a low input at EN turns off the converter. When not in use, connect EN to the input source through a 100kΩ pull-up resistor for automatic start-up if $V_{IN}$ > 6V. EN can also be used to program $V_{IN}$ UVLO. Do not leave EN floating. |
| 3 | VIN | **Input supply.** VIN must be bypassed locally. |
| 4, 5, 6 | SW | **Power switch output.** SW is the drain of the internal MOSFET switch. Connect the power inductor and output rectifier to SW. |
| 7 | VDD | **LDO output.** |
| 8, 9, 10, Exposed Pad | PGND | **Power ground.** The bottom exposed pad is the power ground. For best thermal resistance, solder the exposed pad to the underlying PCB. |
| 11 | AGND | **Analog ground.** Connect AGND to the ground plane through the exposed pad. |
| 12 | SS | **Soft-start control.** Connect a soft-start capacitor to SS. The soft-start capacitor is charged with a constant current of 5μA. Leave SS disconnected if the soft-start is not needed. |
| 13 | FB | **Feedback input.** Reference voltage is 1.25V. Connect a resistor divider to FB. |
| 14 | FSET | **Frequency programming.** Connect a resistor from FSET to AGND. The voltage on FSET is regulated internally to 0.5V. The current flowing out of FSET sets the operation frequency linearly. |
| | | **Exposed pad.** The bottom exposed pad is the power ground. For best thermal resistance, solder the exposed pad to the underlying PCB. |

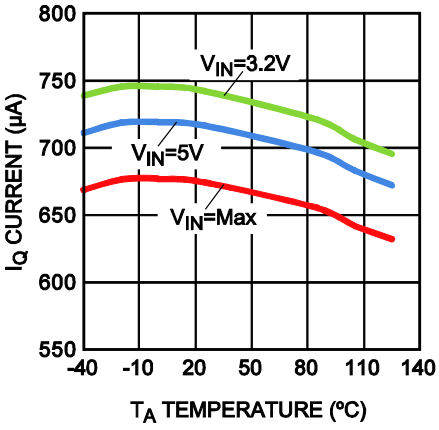
## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 48V, L = 33µH, $C_{OUT}$ = 4.7µF, $f_{SW}$ = 300kHz, $T_A$ = +25°C, unless otherwise noted.**

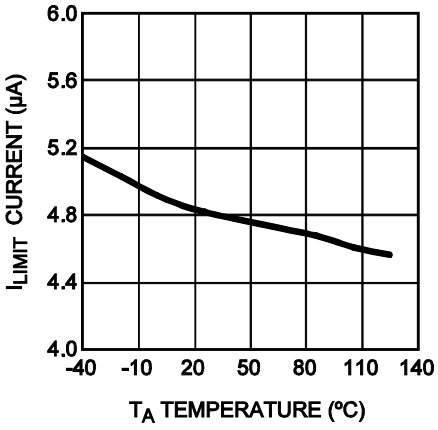
**$V_{FB}$ vs. Temperature**



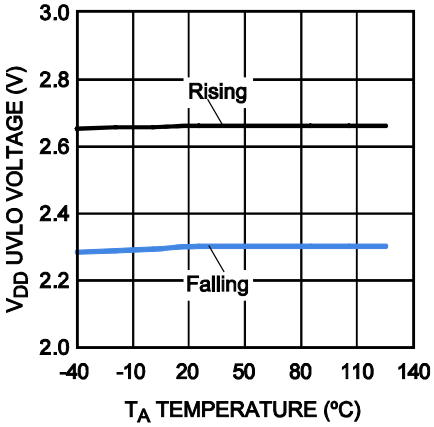

**$I_Q$ vs. Temperature**



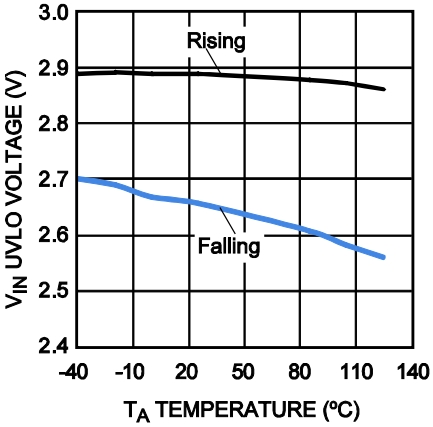

**$I_{LIMIT}$ vs. Temperature**



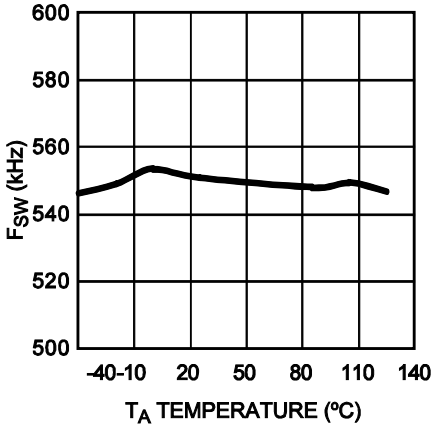

**$V_{DD}$ UVLO vs. Temperature**




**$V_{IN}$ UVLO vs. Temperature**



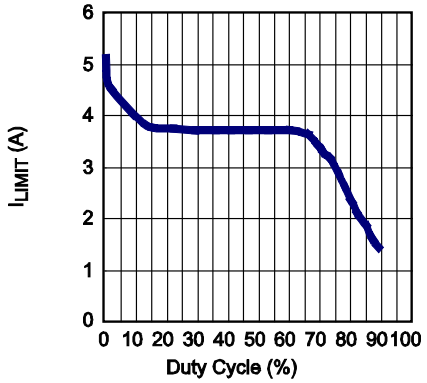

**$F_{SW}$ vs. Temperature**



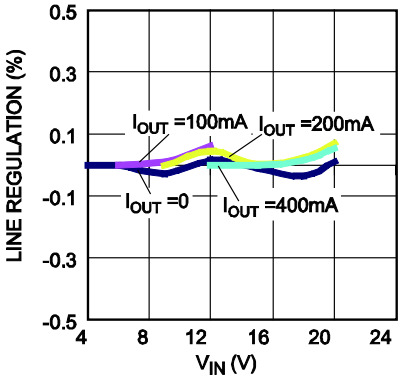
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 48V, L = 33µH, $C_{OUT}$ = 4.7µF, $f_{SW}$ = 300kHz, $T_A$ = +25°C, unless otherwise noted.**

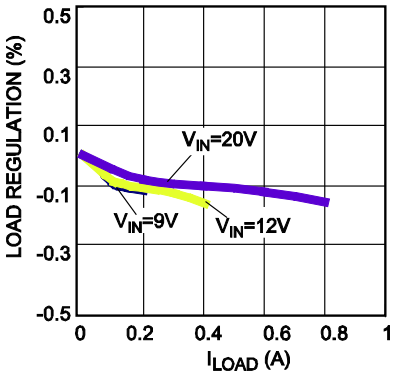
**$I_{LIMIT}$ vs. Duty Cycle**



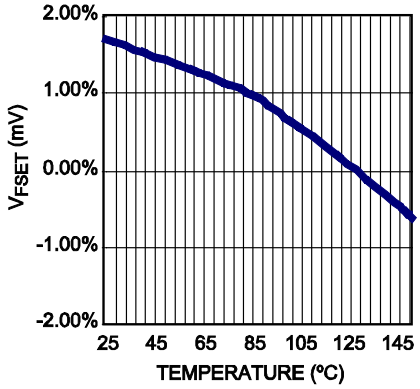

**Line Regulation**



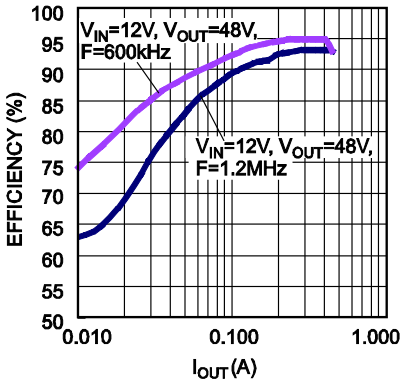

**Load Regulation**



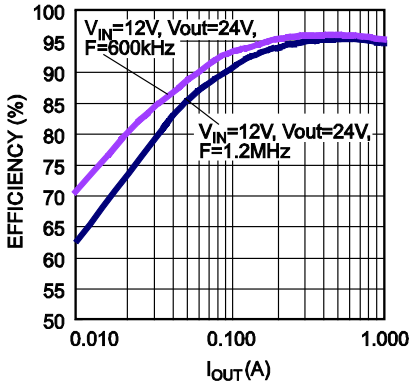

**$V_{FSET}$ vs. Temperature**



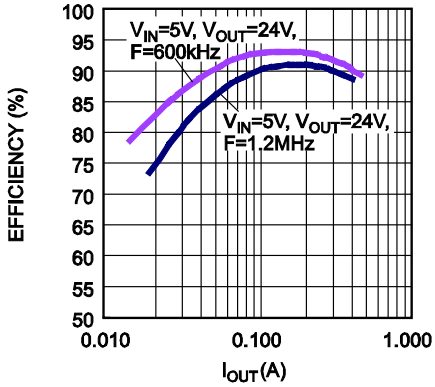

**Efficiency**



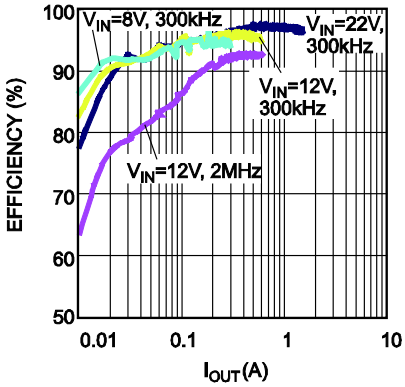

**Efficiency**




**Efficiency**



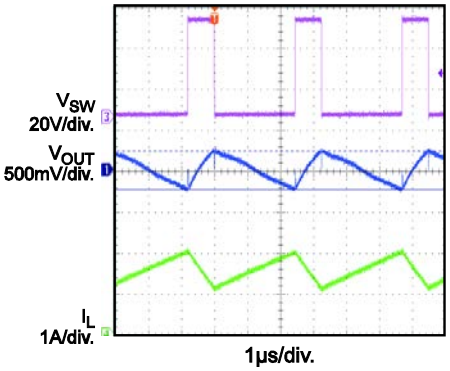

**Efficiency**



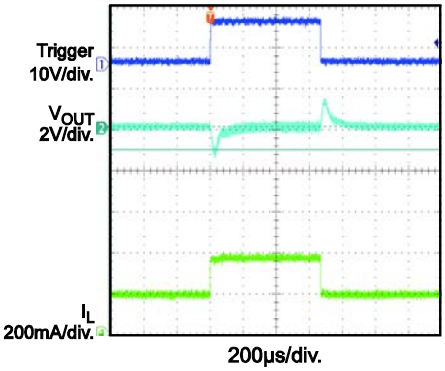
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 48V, L = 33µH, $C_{OUT}$ = 4.7µF, $f_{SW}$ = 300kHz, $T_A$ = +25°C, unless otherwise noted.**

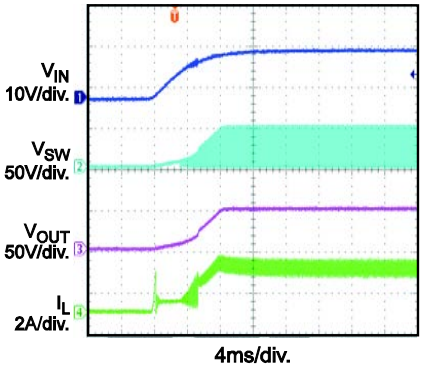
**$V_{OUT}$ Ripple**
$I_{OUT}$ = 0.4A



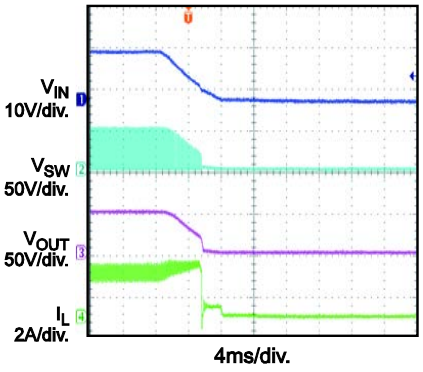

**Transient Response**
$I_{OUT}$ = 0.2A-0.4A step



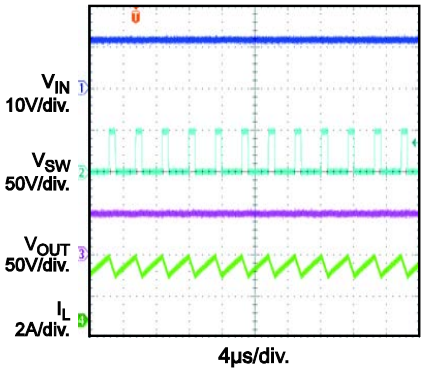

**Power Ramp Up**
$I_{OUT}$ = 0.5A



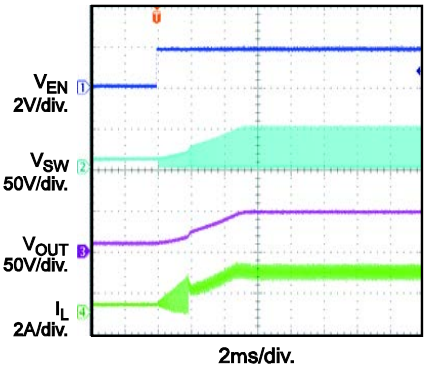

**Power Ramp Down**
$I_{OUT}$ = 0.5A



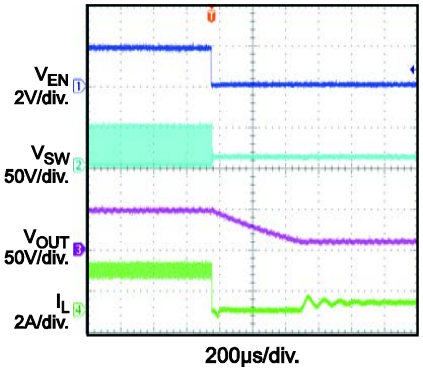

**Steady State**
$V_{IN}$ = 12V, $I_{OUT}$ = 0.6A



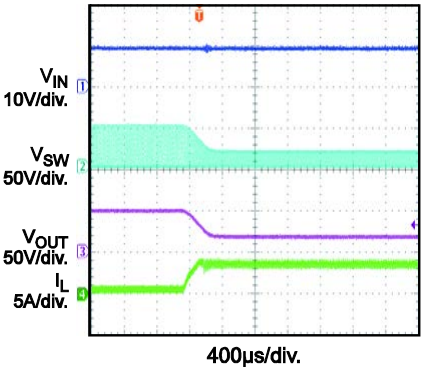

**EN Start-Up**
$V_{IN}$ = 10V, $I_{OUT}$ = 0.4A



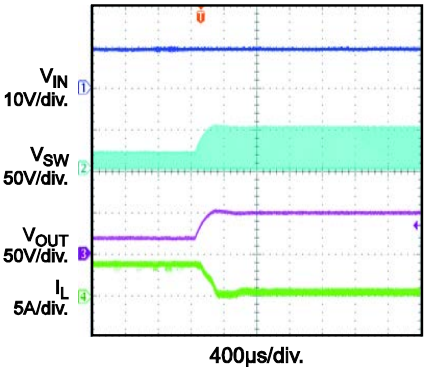

**EN Shutdown**
$V_{IN}$ = 10V, $I_{OUT}$ = 0.4A




**Over-Current Protection**
$V_{IN}$ = 10V, $I_{OUT}$ = 0.1A to 2A




**Over-Current Recovery**
$V_{IN}$ = 10V, $I_{OUT}$ = 0.1A to 2A



## BLOCK DIAGRAM

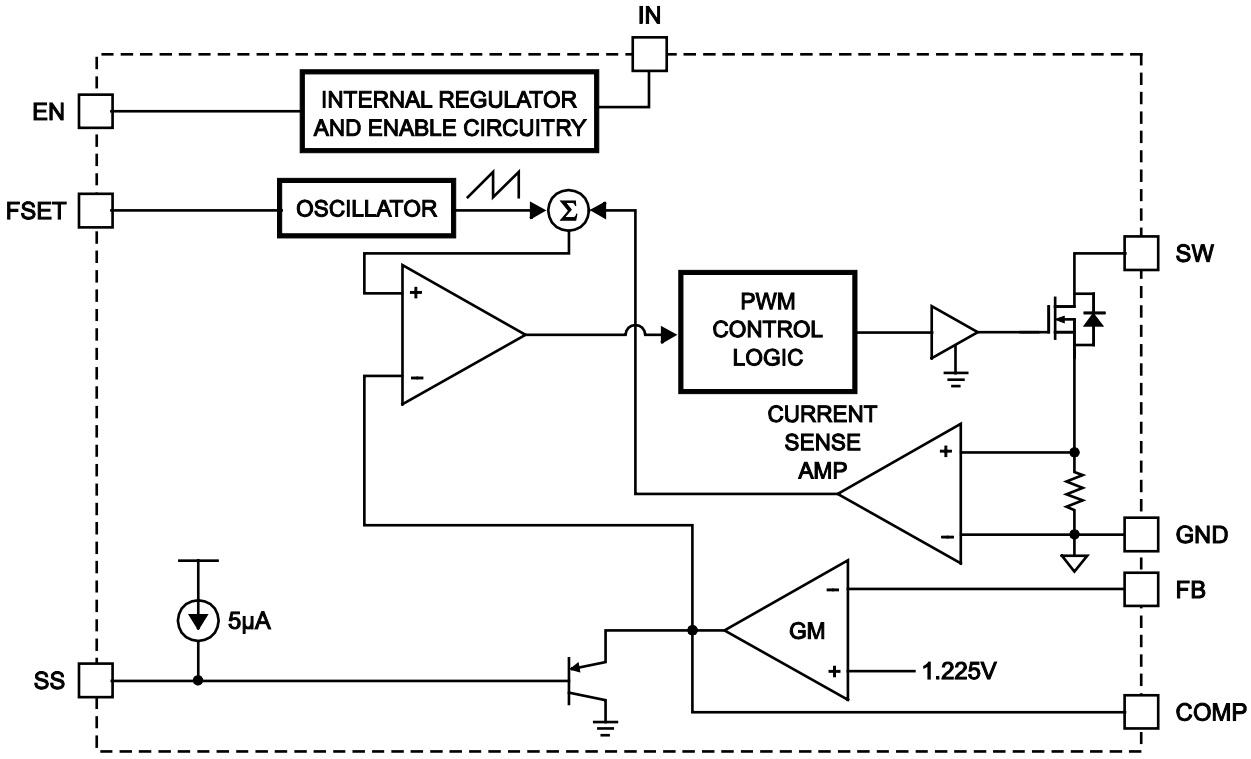



**Figure 1: Functional Block Diagram**

# APPLICATION INFORMATION

**Components referenced below apply to the "*Typical Application Circuit*".**

### Theory of Operation

The MPQ3425 uses a constant-frequency, peak-current-mode boost regulation architecture to regulate feedback voltage. For operation details of the MPQ3425, refer to the functional block diagram on page 8.

At the beginning of each cycle, the N-channel MOSFET switch is turned on, forcing the inductor current to rise. The current at the source of the switch is measured internally and converted to a voltage by the current sense amplifier. That voltage is compared to the error voltage at COMP. The voltage at the output of the error amplifier is an amplified version of the difference between the 1.225V reference voltage and the feedback voltage.

When theses two voltages are equal, the PWM comparator turns the switch off. The inductor current flows to the output capacitor through the external rectifier diode. This causes the inductor current to decrease. The peak inductor current is controlled by the COMP voltage, which is controlled by the output voltage. The output voltage is regulated by the inductor current to satisfy the load. Current mode regulation improves transient response and control loop stability.

### Selecting the Switching Frequency

The switching frequency is set by R5 and can be calculated with Equation (1):

$$F_{SET} = 23 \times \left(R5^{-0.86}\right) \quad (1)$$

Where R5 is in kΩ. See Table 1 for more frequency options

### UVLO Hysteresis

The MPQ3425 features a programmable UVLO hysteresis (see Figure 2). When VIN powers up, a 4μA current sink is applied to the resistor divider attached to EN. Therefore, VIN must increase by an extra amount to overcome the current sink. This extra amount is the current sink times the resistor from VIN to EN. Once EN reaches 1.5V, the current sink turns off to create the reverse hysteresis for VIN falling.

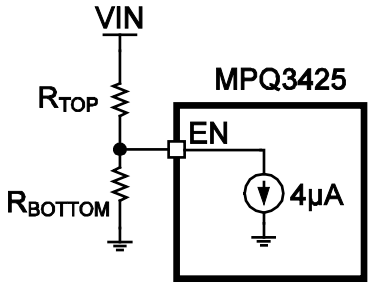



**Figure 2: UVLO Hysteresis**

UVLO hysteresis can be calculated with Equation (2):

$$UVLOHysteresis = 4\mu A \times R_{TOP} \quad (2)$$

**Table 1: Frequency Selection**

| R5 (kΩ) | Freq (MHz) |
|---|---|
| 180 | 0.26 |
| 160 | 0.29 |
| 150 | 0.31 |
| 143 | 0.32 |
| 66.5 | 0.62 |
| 35.7 | 1.06 |
| 25 | 1.44 |
| 18 | 1.91 |
| 16 | 2.12 |
| 14 | 2.37 |

### Selecting the Soft-Start Capacitor

The MPQ3425 uses a soft-start timer that limits the voltage at COMP during start-up to prevent excessive current at input. This prevents premature termination of the source voltage at start-up due to an input current overshoot.

When power is applied to the MPQ3425 and enable is asserted, a 5μA internal current source charges the external capacitor at SS. As the SS capacitor is charged, the SS voltage rises. When the SS voltage reaches 250mV, the MPQ3425 begins switching at a quarter of the programmed frequency. This is known as frequency foldback mode.

At 800mV, the switching frequency becomes the programmed value. The soft-start ends when the voltage at SS reaches 2.5V. This limits the inductor current at start-up, forcing the input current to rise slowly to the current required to regulate the output voltage.

The soft-start period is determined with Equation (3):

$$t_{SS} = \frac{C_{SS} \times 10^{-9} \times 2.5V}{6\mu A} \quad (3)$$

Where $C_{SS}$ (nF) is the soft-start capacitor from SS to GND.

### Setting the Output Voltage

The output voltage is sensed through two sensing resistors in series (R2 and R3). The feedback voltage is 1.225V, typically. The output voltage can be calculated with Equation (4):

$$V_{OUT} = V_{REF} \times (1 + \frac{R2}{R3}) \quad (4)$$

Where R2 is the top feedback resistor, R3 is the bottom feedback resistor, and $V_{REF}$ is the reference voltage (typically 1.225V).

Select feedback resistors in the 10k range or higher for optimum efficiency.

### Selecting the Input Capacitor

An input capacitor is required to supply AC ripple current to the inductor while limiting noise at the input source. A low ESR capacitor is required to keep the noise at the IC minimal. Ceramic capacitors are recommended, but tantalum or low ESR electrolytic capacitors are also sufficient.

Use an input capacitor with a value greater than 4.7µF. The capacitor can be electrolytic, tantalum, or ceramic. However, since the capacitor absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with an RMS current rating greater than the inductor ripple current. See the “Selecting the Inductor” section to determine the inductor ripple current.

To ensure stable operation, place the input capacitor as close to the IC as possible. Alternately, a smaller, high-quality, 0.1µF ceramic capacitor may be placed closer to the IC with the larger capacitor placed further away. If using this technique, it is recommended that the larger capacitor be tantalum or electrolytic. All ceramic capacitors should be placed close to the MPQ3425.

### Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Low ESR capacitors are recommended to keep the output voltage ripple low. The characteristics of the output capacitor also affect the stability of the regulation control system. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. With ceramic capacitors, the impedance of the capacitor at the switching frequency is dominated by the capacitance, so the output voltage ripple is independent of the ESR. The output voltage ripple can be estimated with Equation (5):

$$V_{RIPPLE} \cong \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times F_{SW}} \quad (5)$$

Where $V_{IN}$ and $V_{OUT}$ are the DC input and output voltages respectively, $I_{LOAD}$ is the load current, $F_{SW}$ is the switching frequency, and $C_{OUT}$ is the capacitance of the output capacitor.

With tantalum or low ESR electrolytic capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be estimated with Equation (6):

$$V_{RIPPLE} \cong \frac{(1 - \frac{V_{IN}}{V_{OUT}}) \times I_{LOAD}}{C_{OUT} \times F_{SW}} + \frac{I_{LOAD} \times R_{ESR} \times V_{OUT}}{V_{IN}} \quad (6)$$

Where $R_{ESR}$ is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the output ripple and load transient requirements of the design. A 4.7µF - 22µF ceramic capacitor is suitable for most applications.

### Selecting the Inductor

An inductor with a larger value results in less ripple current and a lower peak inductor current, reducing stress on the internal N-channel switch. However, the larger-value inductor has a larger physical size, higher series resistance, and lower saturation current.

Allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current. Ensure that the peak inductor current is below 75% of the current limit at the operating duty cycle to prevent regulation loss caused by the current limit. Also ensure that the inductor does not saturate under the worst-case load transient and start-up conditions. Calculate the required inductance value with Equation (7) and Equation (8):

$$L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times F_{SW} \times \Delta I} \quad (8)$$

$$I_{IN(max)} = \frac{V_{OUT} \times I_{LOAD(MAX)}}{V_{IN} \times \eta} \quad (9)$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, ΔI = (30% - 50%) x $I_{LOAD\ (MAX)}$, and η is the efficiency.

### Selecting the Diode

The output rectifier diode supplies current to the inductor when the internal MOSFET is off. Use a Schottky diode to reduce losses caused by the diode forward voltage and recovery time. The diode should be treated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current, and the peak current rating must be greater than the peak inductor current.

### Compensation

The output of the transconductance error amplifier (COMP) is used to compensate for the regulation control system. The system uses two poles ($F_{P1}$ and $F_{P2}$) and one zero ($F_{Z1}$) to stabilize the control loop. $F_{P1}$ is set by the output capacitor ($C_{OUT}$) and the load resistance ($R_{LOAD}$). $F_{P2}$ is set by the compensation capacitor ($C_{COMP}$). $F_{Z1}$ is set by the compensation resistor ($R_{COMP}$) and $C_{COMP}$.

These poles are determined by Equation (10), Equation (11), and Equation (12):

$$F_{P1} = \frac{1}{2 \times \Pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (10)$$

$$F_{P2} = \frac{G_{EA}}{2 \times \Pi \times A_{VEA} \times C_{COMP}} (Hz) \quad (11)$$

$$F_{Z1} = \frac{1}{2 \times \Pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (12)$$

Where $R_{LOAD}$ is the load resistance, $G_{EA}$ is the error amplifier transconductance, and $A_{VEA}$ is the error amplifier voltage gain.

The DC loop gain can be calculated with Equation (13):

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS}}{0.5 \times V_{OUT}^{2}} (V/V) \quad (13)$$

Where $G_{CS}$ is the compensation voltage to the inductor current gain, and the $V_{FB}$ is the feedback regulation threshold.

There is also a right-half-plane zero ($F_{RHPZ}$) that exists in continuous conduction mode in step-up converters, where the inductor current does not drop to zero in each cycle. The frequency of the right-half-plane zero can be calculated with Equation (14):

$$F_{RHP} = \frac{R_{LOAD}}{2 \times \Pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz) \quad (14)$$

Table 2 lists the recommended compensation components for different input voltages, output voltages, and capacitances of the most frequently used output ceramic capacitors. Ceramic capacitors have extremely low ESR values, so a second compensation capacitor from COMP to GND is not required.

**Table 2: Component Selection**

| $V_{IN}$ (V) | $V_{OUT}$ (V) | $C_{OUT}$ (µF) | Rcomp (kΩ) | $C_{COMP}$ (nF) | Switching Frequency (kHz) | Inductor (µH) |
|---|---|---|---|---|---|---|
| 3 | 12 | 4.7 | 10 | 6.8 | 600 | 8.2 |
| 3 | 12 | 10 | 15 | 6.8 | 600 | 8.2 |
| 3 | 12 | 22 | 30 | 6.8 | 600 | 8.2 |
| 5 | 12 | 10 | 12 | 4.9 | 600 | 6.8 |
| 5 | 12 | 22 | 25 | 4.9 | 600 | 6.8 |
| 5 | 18 | 4.7 | 12 | 4.9 | 600 | 10 |
| 5 | 18 | 10 | 25 | 4.9 | 600 | 10 |
| 5 | 18 | 22 | 50 | 4.9 | 600 | 10 |
| 12 | 24 | 4.7 | 10 | 6.8 | 600 | 10 |
| 12 | 24 | 10 | 20 | 6.8 | 600 | 10 |
| 12 | 24 | 22 | 40 | 6.8 | 600 | 10 |
| 12 | 48 | 4.7 | 30 | 4.7 | 600 | 33 |
| 12 | 48 | 10 | 60 | 4.7 | 600 | 33 |
| 12 | 48 | 22 | 60 | 10 | 600 | 33 |

For a faster control loop and better transient response, set the capacitor C7 to the recommended value in Table 2. Then, slowly increase the resistor (R6) and check the load step response on a bench to ensure that the ringing and overshoot on the output voltage at the edge of the load steps is minimal. Finally, the compensation needs to be checked by calculating the DC loop gain and the crossover frequency.

The crossover frequency where the loop gain drops to 0dB (a gain of 1) can be obtained visually by placing a -20dB/decade slope at each pole, and a +20dB/decade slope at each zero. The crossover frequency should be at least one decade below the frequency of the right-half-plane zero at the maximum output load current to obtain a high enough phase margin for stability.

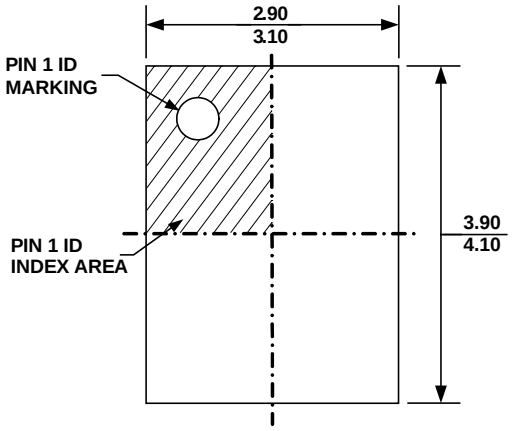
## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation and low noise. For best results, refer to the MPQ3425 demo board and follow the guidelines below.

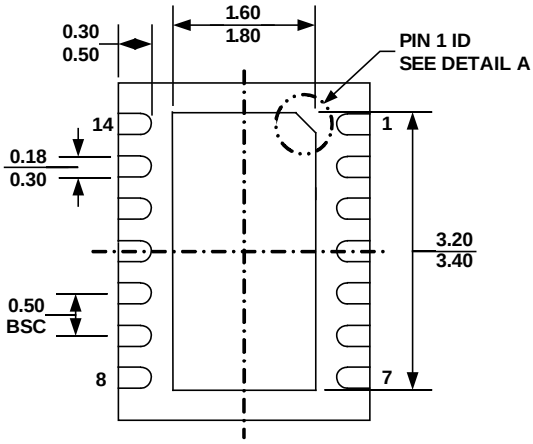
1. Place all components as close to the IC as possible.
2. Keep the path between L1, D1, and $C_{OUT}$ extremely short for minimal noise and ringing.
3. Place $C_{IN}$ close to IN for best decoupling results.
4. Keep all feedback components close to FB to prevent noise injections on the FB trace.
5. Tie the ground return of $C_{IN}$ and $C_{OUT}$ close to GND.

# PACKAGE INFORMATION

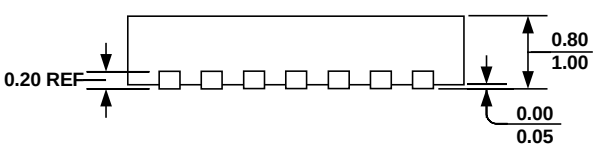
## QFN-14 (3mmx4mm)



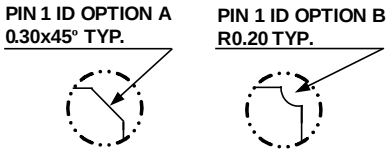

TOP VIEW



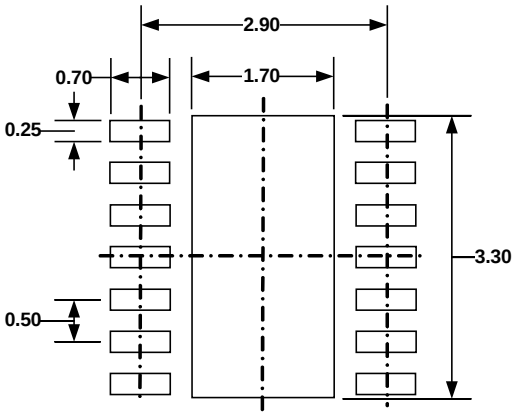

BOTTOM VIEW




SIDE VIEW




DETAIL A




RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE