

# Design Guidelines for Flyback Converter

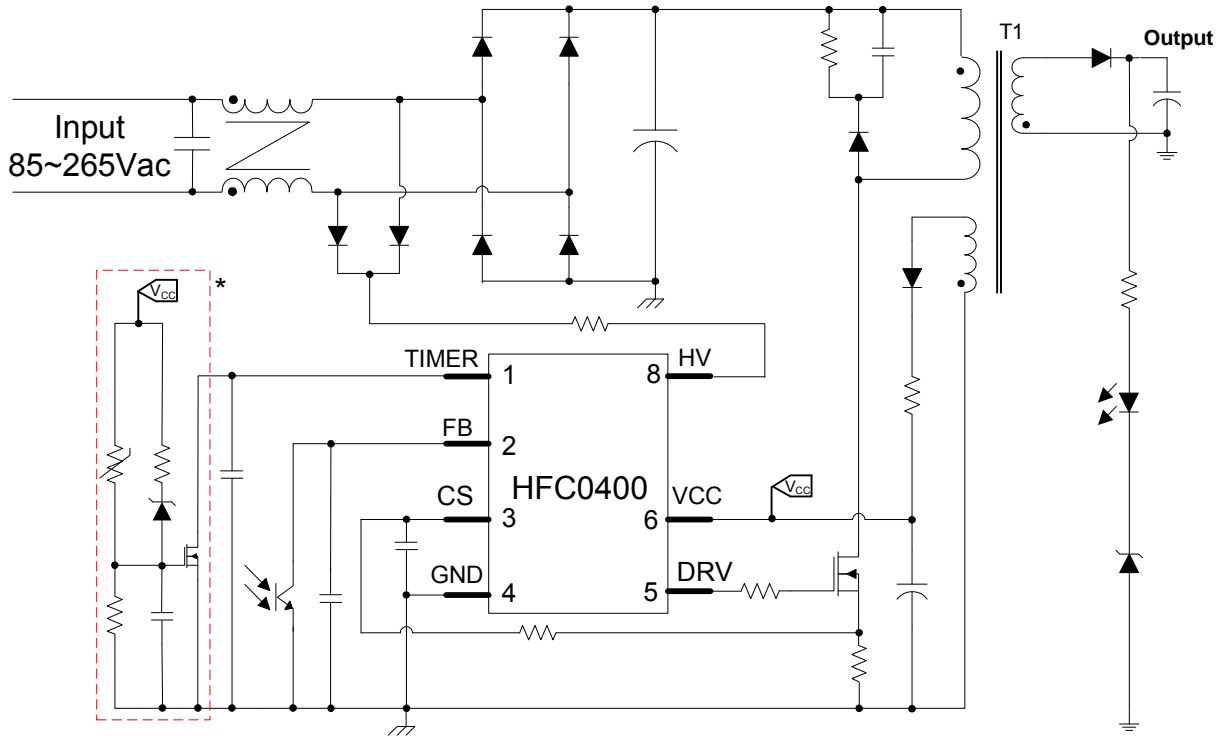
## Using HFC0400 Application Note

*Prepared by San Chen*

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**ABSTRACT**

This paper presents design guidelines for flyback power supply with HFC0400 of MPS as shown in Figure1. Design of a flyback converter with peak current control is quite simple and straightforward through the step-by-step design procedure described in this application note. Experimental results based on the design example are presented in the last part.



\* The circuit in red is optional. Implements external OVP and OTP function by pulling the TIMER pin down.

**Figure 1: Flyback converter using HFC0400**

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## 1. HFC0400 INTRODUCTION

HFC0400 is a current mode controller with full features. The controller supports continuous conduction mode (CCM) with a wide input voltage range as the built in slope compensation helps to avoid sub-harmonic oscillation when duty is larger than 0.5. The IC implements a frequency foldback down to 25 kHz at light load condition for excellent efficiency at all load range. HFC0400 offers frequency jittering for better EMI performance which helps to spread out energy in conducted noise. At very light load, the controller enters burst mode to achieve very low standby power consumption. HFC0400 also has the X-CAP discharge function, through the HV Pin signal motoring, it can discharge the X-CAP when the input is unplugged, and the power loss caused by the X-CAP discharge resistors can be eliminated. Variable protections like Vcc under Voltage Lockout (UVLO), Over Load Protection (OLP), Over Voltage Protection (OVP), Over Temperature Protection (OTP) and Brown-Out Protection are integrated in the IC to minimize the external component count. This paper presents practical design guidelines for an off-line flyback converter employing HFC0400. Step-by-step design procedure for flyback converter using HFC0400 is introduced in this application note, mainly including transformer design, output filter design and the key components selection.

## 2. FREQUENCY FOLDBACK

Figure 2 shows the switching frequency vs. FB and peak current vs. FB. At heavy load condition (FB>2V), the switching frequency is fixed with frequency jittering for EMI reduction. The FB voltage regulates the primary side peak current signal (sensed by sensing resistor) connected to CS pin with an internal 1/3 voltage gain. When the load decreases to a given level (1.33V<FB<2V), the controller freezes the peak current (0.67V) and reduces the switching frequency down to 25kHz which helps to reduce the switching loss. If the load continues to decrease, the switching frequency is fixed to 25kHz and the peak current decreases with decreasing of FB voltage to avoid audible noise. When the load continues to decrease to very light or no-load, HFC0400 enters burst-mode operation. The controller stops the gate switching signal when the FB voltage drops below the lower burst threshold  $V_{BRUL}$ —0.32V. And the output voltage starts to decrease which causes the FB voltage to increase again. Once the FB voltage exceeds the higher burst threshold  $V_{BRUH}$ —0.46V, the switching resumes. The FB voltage then falls and rises repeatedly. The burst mode operation alternately enables and disables the switching of the MOSFET thereby reducing switching loss at no load or light load conditions.

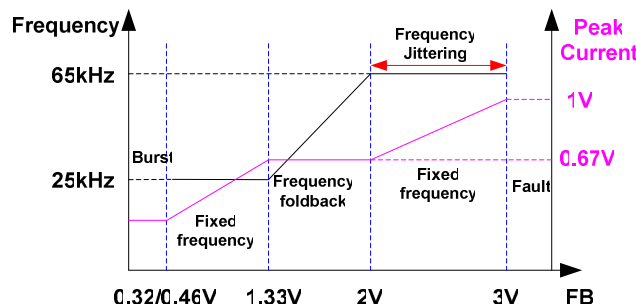


Figure 2: Frequency and Peak Current vs. FB

## 3. X-CAP DISCHARGE FUNCTION

X capacitors are usually connected across input terminals of AC-DC power supply to filter out differential mode EMI noise. These X capacitors may present a safety hazard because they can store unsafe levels of high-voltage energy for long period of time after the AC is disconnected. To meet safety standards, the traditional method is placing resistors in parallel with the X capacitor (if the X-cap is larger than 0.1 $\mu$ F) to discharge the X-cap in a specified time. The time constant of the X-cap and paralleled resistor should meet  $C_x \cdot R_{discharge} < 1sec$ . Considering the tolerance of X-cap ( $\pm 10\%$  or  $\pm 20\%$  typical) and discharge resistors ( $\pm 1\%$  or  $\pm 5\%$  typical) in application, there should be certain margin for

the time constant  $C_x \cdot R_{\text{discharge}} \leq 0.78\text{sec}$ . However, these bleeding resistors produce a power loss while the AC is connected, for example, if  $R_{\text{discharge}}=2\text{M}\Omega$ , there will be 35mW loss at 265V<sub>ac</sub> RMS input. The loss is a significant contributor to no-load and standby input power consumption. The following table shows power loss of bleeding resistor with different X-cap.

**Table 1: Power loss of bleeding resistor vs Cx**

Cx (Deviation ±20%)	0.22μF	0.33μF	0.47μF	1μF
Bleeding resistance (Deviation ±5%)	3.4MΩ	2.2MΩ	1.5MΩ	780kΩ
Power loss at 265V <sub>AC</sub> input	20.7 mW	31.9 mW	46.8 mW	90 mW

HFC0400 implements a novel X-cap discharge function without the bleeding resistors. When the AC voltage is applied, internal high voltage current source turns off to block current flow into the HV Pin and the IC will continuously monitor the HV voltage. When the AC voltage is unplugged, the IC will turn on high voltage current source after a delay time to discharge the X-cap. So the traditional bleeding resistors can be removed and the standby power loss of system is significantly reduced.

## 4. DESIGN PROCEDURE

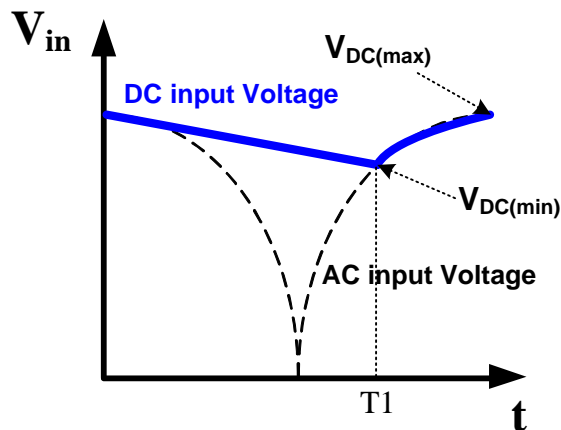
### A. Predetermine Input and Output Specifications

- Input AC voltage range:  $V_{\text{ac}(\text{min})}$ ,  $V_{\text{ac}(\text{max})}$ , for example 85V<sub>ac</sub>~265V<sub>ac</sub> RMS  
Note: due to the brown-out function in HFC0400, the minimum input should be larger than 82V<sub>ac</sub>RMS.
- DC bus voltage range:  $V_{\text{in}(\text{max})}$ ,  $V_{\text{in}(\text{min})}$ .
- Output:  $V_o$ ,  $I_o(\text{min})$ ,  $I_o(\text{max})$ ,  $P_{\text{out}}$ .
- Estimated efficiency:  $\eta$ , It is used to estimate the power conversion efficiency at lowest input voltage to calculate the maximum input power. Generally,  $\eta$  is set to be 0.75~0.85 according to different input range and output applications.

Then the maximum input power can be given as:

$$P_{\text{in}} = \frac{P_{\text{out}}}{\eta} \tag{1}$$

Figure 3 shows the typical waveform of DC bus voltage. The DC input capacitor  $C_{\text{in}}$  is usually set as 2μF/W of input power  $P_{\text{in}}$  for the universal input condition. For 230V<sub>ac</sub> single range application, the capacitance can be 1μF/W of input power.



**Figure 3: Input Voltage Waveform**

From the waveform above, the AC input Voltage  $V_{AC}$  and DC input Voltage  $V_{DC}$  can be got as:

$$V_{AC}(V_{ac}, t) = \sqrt{2} \cdot V_{ac} \cdot \cos(2 \cdot \pi \cdot f \cdot t) \quad (2)$$

$$V_{DC}(V_{ac}, t) = \sqrt{2 \cdot V_{ac}^2 - \frac{2 \cdot P_{in}}{C_{in}} \cdot t} \quad (3)$$

By setting  $|V_{AC}|=V_{DC}$ , T1 where DC input voltage had reached to its minimum  $V_{DC(min)}$  can be solved by (2) and (3).

$$V_{DC(min)} = V_{DC}(V_{ac(min)}, T1) \quad (4)$$

Then, the minimum average DC input voltage  $V_{in(min)}$  can be got as:

$$V_{in(min)} = \frac{\sqrt{2} \cdot V_{ac(min)} + V_{DC(min)}}{2} \quad (5)$$

The maximum average DC input voltage  $V_{in(max)}$  can be got as:

$$V_{in(max)} = \sqrt{2} \cdot V_{ac(max)} \quad (6)$$

## B. Determine the Startup Circuitry

Figure 4 shows the startup circuit, when power is on, the internal high voltage current source charges C1 from AC line by R1, D1 and D2. As soon as  $V_{CC}$  voltage reaches  $V_{CC(OFF)}$  (14.5V typically), the current source turns off and controller detects the voltage on HV pin. Once voltage on HV pin is higher than  $HV_{ON}$  before  $V_{CC}$  drops down to  $V_{CC(SS)}$  (11.5V typically), the controller starts switching, or brown-out is defaulted to lock driver output,  $V_{CC}$  will drop down to 5.3V and the current source turns on to recharge C1. The supply of the IC is taken over by the auxiliary winding of the transformer after the controller starts switching. If  $V_{CC}$  falls back below 8.0V, switching pulse is stopped and the current source turns on again (see Figure 5). The value of R1 and C1 determines the start up delay time of system, the larger R1 or C1, the larger start up delay. For example, if R1 is chosen as 20k $\Omega$ , C1 is chosen as 47 $\mu$ F, the start up delay time is about 700ms at 85V $_{AC}$  input. Furthermore, the time duration of  $V_{CC}$  drops from  $V_{CC(OFF)}$  to  $V_{CC(SS)}$  for brown-out detection should be larger than half of input period, the  $V_{CC}$  capacitance can be got as equation(7), where  $I_{CC(noswitch)}$  is the inner consumption close to  $I_{CC(latch)}$ ,  $T_{input}$  is period of AC input. As a result,  $V_{CC}$  capacitance is recommended to be larger than 10 $\mu$ F.

$$C_1 > \frac{I_{CC(noswitch)} \cdot 0.5 \cdot T_{input}}{V_{CC(OFF)} - V_{CC(SS)}} \quad (7)$$

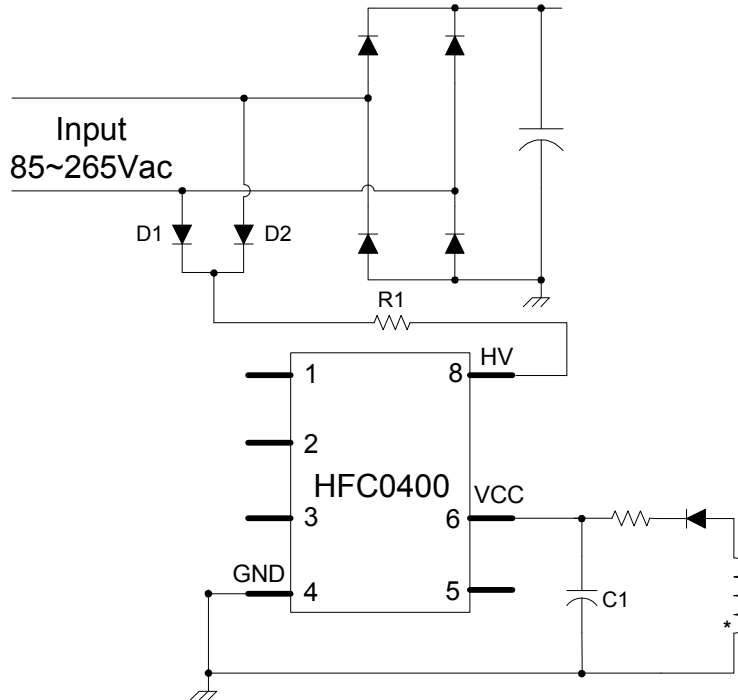


Figure 4: The Startup Circuit of HFC0400

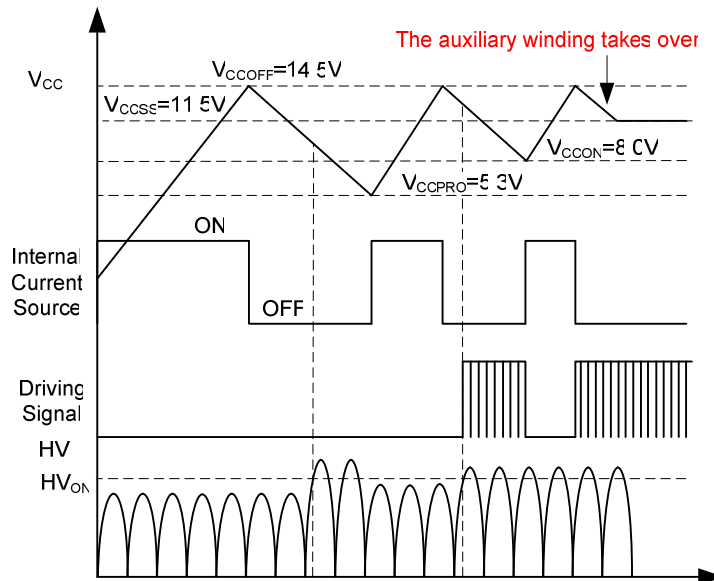


Figure 5: The Startup and VCC UVLO of HFC0400

### C. Reflected output voltage $V_{RO}$ , Turns Ratio-N, Primary MOSFET and Secondary Rectifier Diode Selection

$V_{RO}$  is the reflected output voltage to primary side during secondary diode conduction:  $V_{RO} = N \cdot (V_O + V_F)$ , where  $V_F$  is the forward voltage drop of secondary diode. Considering the efficiency and voltage stress on MOSFET and secondary diode, the optimal selection of  $V_{RO}$  depends on the output specification. For lower voltage output applications (such as 5V),  $V_{RO}$  is recommended at 80V~110V. For higher voltage output application (such as 19V),  $V_{RO}$  is recommended at 100V~135V. Once  $V_{RO}$  is set, the turns ratio N can be obtained.

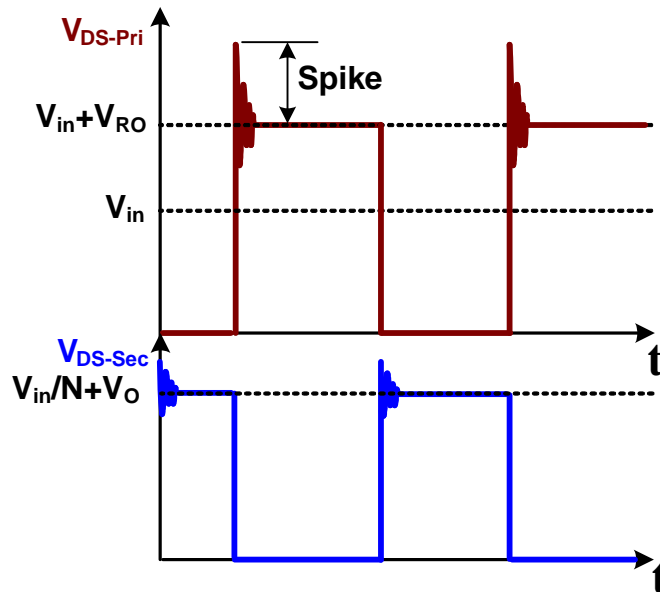
Figure 6 shows the typical Drain-Source voltage waveform of the primary MOSFET and secondary rectifier diode in a flyback converter. From the waveform, the primary MOSFET Drain-Source voltage rating  $V_{P-MOS}$  can be got as:

$$V_{P-MOS} = \frac{V_{in(max)} + V_{RO} + 60V}{k} \quad (8)$$

where  $k$  is the derating factor which is typically selected as 0.9, 60V spike voltage is assumed here. The secondary rectifier diode voltage rating  $V_{DIODE}$  can be got as:

$$V_{DIODE} = \frac{V_{in(max)} / N + V_O + 20V}{k} \quad (9)$$

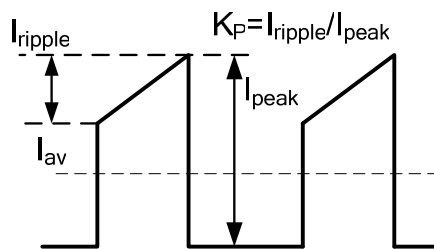
20V spike voltage is assumed here.



**Figure 6: Drain-Source voltage of Primary MOSFET and Secondary Rectifier Diode**

**D. Primary side Inductance  $L_m$**

At heavy load condition, the switching frequency is fixed with frequency jittering. With build-in slope compensation, HFC0400 can operate under CCM when duty cycle is larger than 0.5. Assume the ratio of primary side ripple current to peak current is  $K_P$  as shown in Figure 7 ( $0 < K_P \leq 1$ ,  $K_P = 1$  at DCM). Smaller  $K_P$  can reduce RMS current, but it needs larger inductance which may increase transformer size. For trade off consideration,  $K_P$  is recommended at 0.6~0.8 for universal input range and 0.8~1 for 230V<sub>ac</sub> single input range.



**Figure 7: Typical primary current waveform**



If the flyback converter is designed in CCM at minimum input, the duty cycle of converter is shown as equation (10).

$$D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \quad (10)$$

Turn-on time of MOSFET is given as

$$T_{on} = D \cdot T_s \quad (11)$$

Where  $T_s$  is the nominal switching period without considering the frequency jittering,  $\frac{1}{T_s} = f_s = 65kHz$ .

The average, peak, ripple and valley value of primary side current can be got as follows:

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \quad (12)$$

$$I_{peak} = \frac{I_{av}}{\left(1 - \frac{K_P}{2}\right) \cdot D} \quad (13)$$

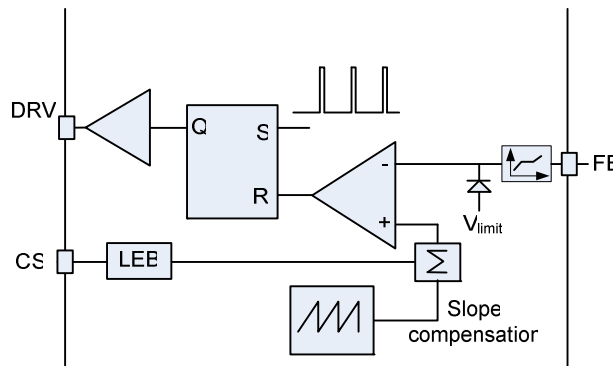
$$I_{ripple} = K_P \cdot I_{peak} \quad (14)$$

$$I_{valley} = (1 - K_P) \cdot I_{peak} \quad (15)$$

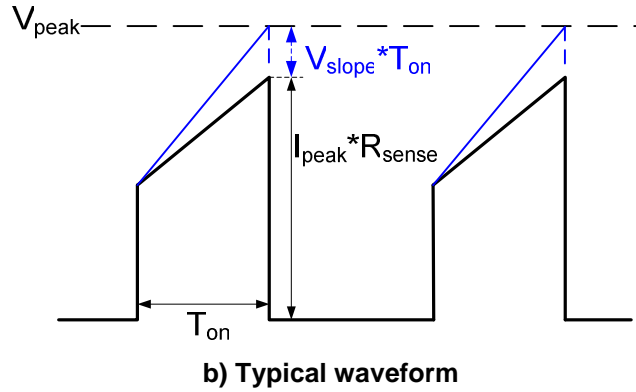
The primary inductance  $L_m$  can be obtained by equation (16).

$$L_m = \frac{V_{in(min)} \cdot T_{on}}{I_{ripples}} \quad (16)$$

### E. Current Sense Resistance



a) Peak current comparator circuit



**Figure 8: Peak current comparator circuit in HFC0400**

The circuit diagram of peak current mode control is shown in Figure 8. When voltage of sensing resistor plus the internal slope reaches  $V_{peak}$ , the comparator outputs high level to reset R-S flip flop. DRV pin is pulled down to turn off MOSFET. The maximum current limit point of HFC0400 is  $V_{limit} = 0.95V$ . The build-in slope compensation is  $V_{slope} = 25mV/\mu s$  typically. Considering the margin, take  $95\% \cdot V_{limit}$  as  $V_{peak}$  at full load. The voltage of sensing resistor can be got as follow:

$$V_{sense} = 95\% \cdot V_{limit} - V_{slope} \cdot T_{on} \quad (17)$$

So the sensing resistance is

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \quad (18)$$

The current sense resistor with the proper power rating should be chosen based on the power loss given

$$P_{sense} = \left[ \left( \frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} (I_{peak} - I_{valley})^2 \right] \cdot D \cdot R_{sense} \quad (19)$$

## F. Transformer Design

### F-1. Transformer Core Selection

Firstly, a proper core for certain output power should be selected. Ferrite is usually adopted in flyback transformer. The core area product ( $A_E A_W$ ) which is the product of core cross-sectional area and core window area for windings, is widely used for an initial estimate of core size for a specific application. A rough indication of the required area product is given by following:

$$A_E \cdot A_W = \left( \frac{L_m \cdot I_{peak} \cdot I_{pri-rms} \times 10^4}{B_{max} \cdot K_u \cdot K_j \cdot f_s} \right)^{4/3} \text{ cm}^4 \quad (20)$$

where  $K_u$  is window utilization factor. In application, AC-DC product is required to keep safety isolation between primary and secondary side, the transformer needs enough insulation, which reduce the available area for windings.  $K_u$  is usually set 0.2~0.3 for an off-line transformer with triple insulated wire, 0.05~0.15 for the transformer with 6mm margin tape.  $K_j$  is the current-density coefficient (typically 400~450 for ferrite core).  $B_{max}$  is the allowed maximum flux density which should be lower than the

saturation flux density of the core material within the operating temperature range, is usually preset to (0.3T~0.4T).  $I_{pri-rms}$  is the RMS current of primary inductance given as follow

$$I_{pri-rms} = \sqrt{\left[ \left( \frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} (I_{peak} - I_{valley})^2 \right] \cdot D} \quad (21)$$

### F-2. Primary and Secondary Winding Turns

With a given core size and  $B_{max}$ , the turns can be calculated. The normal saturation specification is E-T or volt-second rating. The E-T rating is the maximum voltage, E, which can be applied over a time of T seconds. (The E-T rating is identical to the product of inductance L and peak current) Equation (22) defines a minimum value of  $N_p$  for the transformer primary winding to avoid the core saturation:

$$N_p = \frac{L_m \cdot I_{peak}}{B_{max} \cdot A_E} \quad (22)$$

Where:

$L_m$  = the primary inductance of the transformer

$A_E$  = the effective cross sectional area of core

$I_{peak}$  = the peak current in the primary side of the transformer, which is given in (13).

Secondary turns count is a function of turn ratio N and primary turns  $N_p$ :

$$N_s = \frac{N_p}{N} \quad (23)$$

### F-3. Wire size

Once all the winding turns have been determined, wire size must be properly chosen to minimize the winding conduction loss and leakage inductance. The winding loss depends on the RMS current value, the length and the cross section of wire.

The wire size could be determined by the RMS current of the winding. For a flyback converter, the RMS current on secondary side is:

$$I_{sec-rms} = N \cdot \sqrt{\left[ \left( \frac{I_{peak} + I_{valley}}{2} \right)^2 + \frac{1}{12} (I_{peak} - I_{valley})^2 \right] \cdot (1-D)} \quad (24)$$

Then, the wire size required on primary and secondary side is got by equation (25) and equation (26)

$$S_{pri} = \frac{I_{pri-rms}}{J} \quad (25)$$

$$S_{sec} = \frac{I_{sec-rms}}{J} \quad (26)$$

Here J is the current density of the wire which is 500-700A/cm<sup>2</sup> typically.

Due to the skin effect and proximity effect of the conductor, the diameter of the wire selected is usually less than  $2 \cdot \Delta d$  ( $\Delta d$ : skin effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_s \cdot \mu \cdot \sigma}} \quad (27)$$

where  $\mu$  is the magnetic permeability of the conductor, which is usually equals to the permeability of vacuum for most conductor, i.e.  $4\pi \times 10^{-7}$  H/m,  $\sigma$  is the conductivity of the wire (for copper,  $\sigma$  is typically  $6 \times 10^7$  S/m at 0 °C,  $\sigma$  will be larger as temperature increases, which means the  $\Delta d$  will get smaller).

Sometimes the size of selected wire is less than required; it needs to add parallel windings. The number of primary and secondary windings can be got as follows:

$$n_{pri} = \frac{S_{pri}}{\frac{1}{4} \pi d_{pri}^2} \quad (28)$$

$$n_{sec} = \frac{S_{sec}}{\frac{1}{4} \pi d_{sec}^2} \quad (29)$$

where  $d_{pri}$  and  $d_{sec}$  are the wire diameter of primary and secondary winding respectively.

After the wire sizes have been determined, it is necessary to check whether the window area with selected core can accommodate the windings calculated in the previous steps. The window area required by each winding should be calculated respectively and added together, the area for inter-winding insulation, spaces existing between the turns and area of margin tape (if margin tape is placed) should also be taken into consideration. The fill factor, means the winding area to the whole window area of the core, should be well below 1 due to these inter-winding insulation and spaces between turns. It is recommended that a fill factor no greater than about 30% be used. For transformers with multiple outputs this factor may need to be reduced further.

Based on these considerations, the total required window area is then compared to the available window area of a selected core. If the required window area is larger than the selected one, either wire size must be reduced, or a larger core must be chosen. Of course, a reduction in wire size leads to more copper loss of the transformer.

#### F-4. Air gap

With the selected core and winding turns, the air gap of the core is given as:

$$l_a = \mu_0 \cdot A_E \cdot \frac{N_p^2}{L_m} - \frac{l_c}{\mu_r} \quad (30)$$

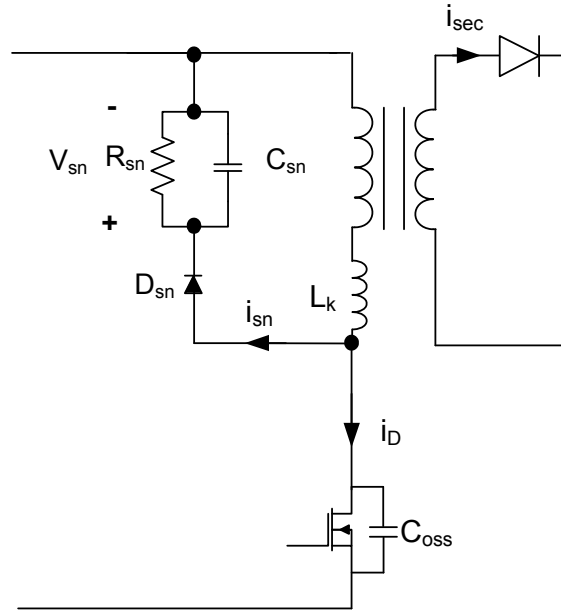
where  $A_E$  is the cross sectional area of the selected core,  $\mu_0$  is the permeability of vacuum which equals  $4\pi \times 10^{-7}$  H/m.  $L_m$  and  $N_p$  is the primary winding inductance and turns respectively,  $l_c$  is the core magnetic path length and  $\mu_r$  is the relative magnetic permeability of the core material. For Ferrite core,  $\mu_r$  is very large, so  $l_a$  can be approximately calculated as equation (31).

$$l_a = \mu_0 \cdot A_E \cdot \frac{N_p^2}{L_m} \quad (31)$$

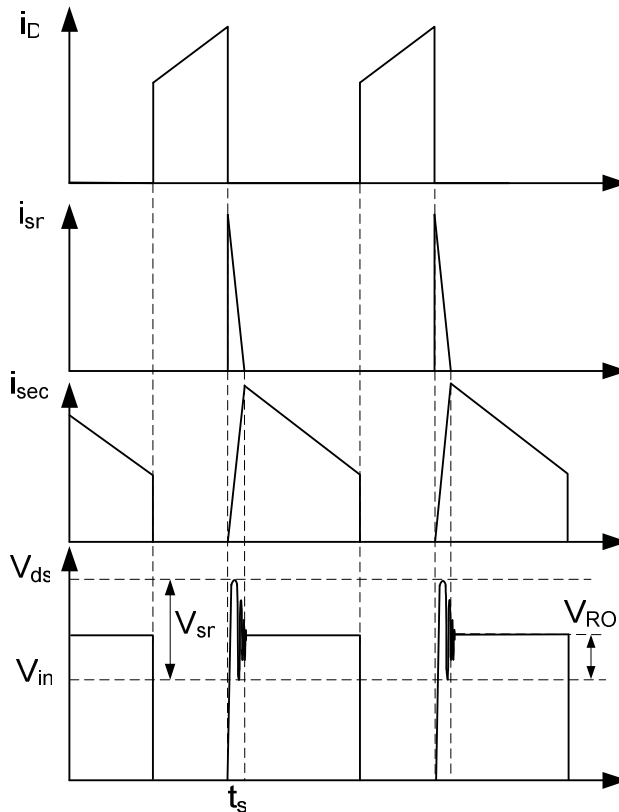
#### G. Design the RCD snubber

In application, a small amount of energy is stored in the leakage inductor of the transformer, which cannot be transferred to the output side in flyback converter. This amount of energy may result in a high voltage spike on the drain-source of the MOSFET when it turns off, which should be well clamped to protect the MOSFET from breakdown.

The RCD snubber is usually adopted to clamp the drain-source voltage as shown in Figure 9. The value of the capacitor,  $C_{sn}$ , and resistor,  $R_{sn}$ , depend on the energy stored in the parasitic inductor, as the energy must be dissipated by the RC network during each cycle. Figure 10 shows the typical waveform of snubber during turn-off phase.



**Figure 9: RCD snubber on primary side**



**Figure 10: Waveform of MOSFET and RCD snubber**

When the MOSFET turns off and  $V_{ds}$  is charged to  $V_{in}+N*(V_o+V_F)$ , the secondary diode turns on, and the current of secondary winding increases from 0. The primary current continues to flow through the snubber diode ( $D_{sn}$ ) to  $C_{sn}$ . The voltage stress of MOSFET is clamped to  $V_{in}+V_{sn}$ . Therefore, the voltage across  $L_k$  is  $V_{sn}-N*(V_o+V_F)$ . The slope of  $i_{sn}$  is given by equation (32).

$$\frac{di_{sn}}{dt} = -\frac{V_{sn} - N \cdot (V_o + V_F)}{L_k} \quad (32)$$

Where  $i_{sn}$  is the current that flows through  $D_{sn}$ ,  $V_{sn}$  is the voltage across the snubber capacitor  $C_{sn}$ ,  $L_k$  is the leakage inductance of the transformer. The time  $t_s$  is obtained by equation (33).

$$t_s = \frac{L_k \cdot I_{peak}}{V_{sn} - N \cdot (V_o + V_F)} \quad (33)$$

$V_{sn}$  is usually set as 1.5~2 times of  $N*(V_o+V_F)$ , the power dissipated in the snubber circuit is obtained by equation (34).

$$P_{sn} = V_{sn} \frac{I_{peak} \cdot t_s}{2} f_s = \frac{1}{2} L_k I_{peak}^2 \frac{V_{sn}}{V_{sn} - N \cdot (V_o + V_F)} f_s \quad (34)$$

Since the power consumed in the snubber resistor ( $R_{sn}$ ) is  $V_{sn}^2/R_{sn}$ , the resistance is obtained by:

$$R_{sn} = \frac{V_{sn}^2}{\frac{1}{2} L_k I_{peak}^2 \frac{V_{sn}}{V_{sn} - N \cdot (V_o + V_F)} f_s} \quad (35)$$

The snubber resistor with the proper rated power should be chosen based on the power loss. The maximum ripple of the snubber capacitor voltage is obtained equation (36).

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} \cdot R_{sn} \cdot f_s} \quad (36)$$

Generally, a 5~10% ripple voltage is reasonable. Therefore, the snubber capacitance can be calculated.

## H. Design the Output Filters

The RMS current of the output capacitor can be obtained as:

$$I_{cap-out} = \sqrt{I_{sec-rms}^2 - I_{out}^2} \quad (37)$$

where  $I_{out}$  is the output current and  $I_{rms-sec}$  is the secondary RMS current in (24).

The RMS current should be smaller than the RMS current specification of the selected capacitor.

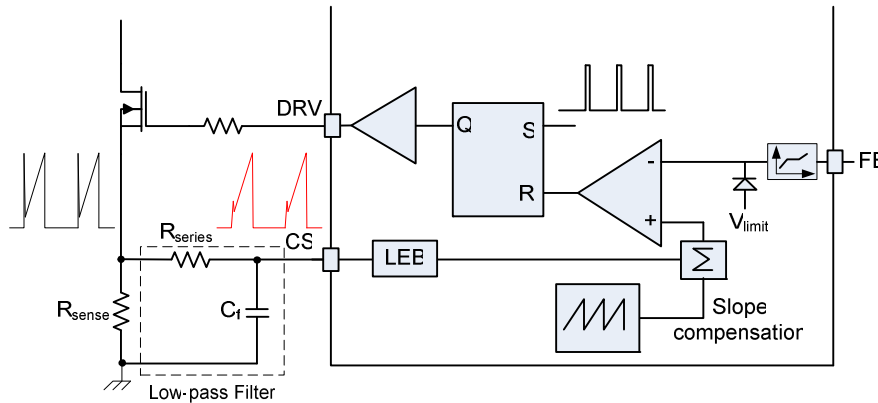
The voltage ripple on the output can be estimated by:

$$\Delta V_{out} = \frac{I_{out} \cdot (T_s - T_{secon})}{C_{out}} + ESR \cdot (N \cdot I_{peak} - I_{out}) \quad (38)$$

where  $T_{secon}$  is the conduction time of secondary diode, ESR is the equivalent series resistance of output cap. By setting a voltage ripple, the value of output capacitor is derived by the upper equation. The output capacitor can be electrolytic capacitor. If the electrolytic capacitor is used, due to its high ESR and ESL, a film capacitor or ceramic capacitor is usually paralleled to the electrolytic capacitor to

provide a low impedance current path for high frequency current ripple. To further reduce the output voltage ripple, a small LC filter can be inserted between the output capacitor and output terminal.

**I. Low-pass Filter on CS Pin**



**Figure 11: Low-pass Filter on CS Pin**

A small capacitor is usually connected to CS pin to form a low-pass filter with  $R_{series}$  for noise filtering at MOSFET turn-on and turn-off, as shown in Figure 11. The resistance in series to CS pin  $R_{series}$  is recommended to be less than  $1k\Omega$ . The  $R_{series} \cdot C_f$  of low-pass filter on CS pin should be no larger than  $1/3$  of leading edge blanking for SCP (LEB2, 250ns), or else the real sense voltage is filtered so can't touch SCP point (1.5V) to trigger SCP when short circuit at output occurs.

**J. Jittering Period**

Frequency jittering is an effective method to reduce EMI by spreading energy over a wide frequency range. The bandwidth of  $n$  order harmonic of noise is  $B_{Tn} = n \cdot (2 \cdot \Delta f + f_{jitter})$ , where  $\Delta f$  is the amplitude of frequency jittering,  $f_{jitter}$  is the jitter frequency. If  $B_{Tn}$  is larger than resolution bandwidth (RBW) of spectrum analyzer (200Hz for noise frequency less than 150 kHz, 9 kHz for noise frequency between 150k~30MHz), the energy of noise received by spectrum analyzer reduces.

The period of frequency jittering is determined the capacitor connected to TIMER pin. A 10uA current source charges the capacitor, when the TIMER voltage reaches 3.2V, it is discharged to 2.8V with another 10uA current source, then charged and discharged repeatedly.

The jittering period can be got as follow:

$$T_{jitter} = \frac{1}{f_{jitter}} = \frac{2 \cdot C_{TIMER} \cdot (3.2V - 2.8V)}{10\mu A} \tag{39}$$

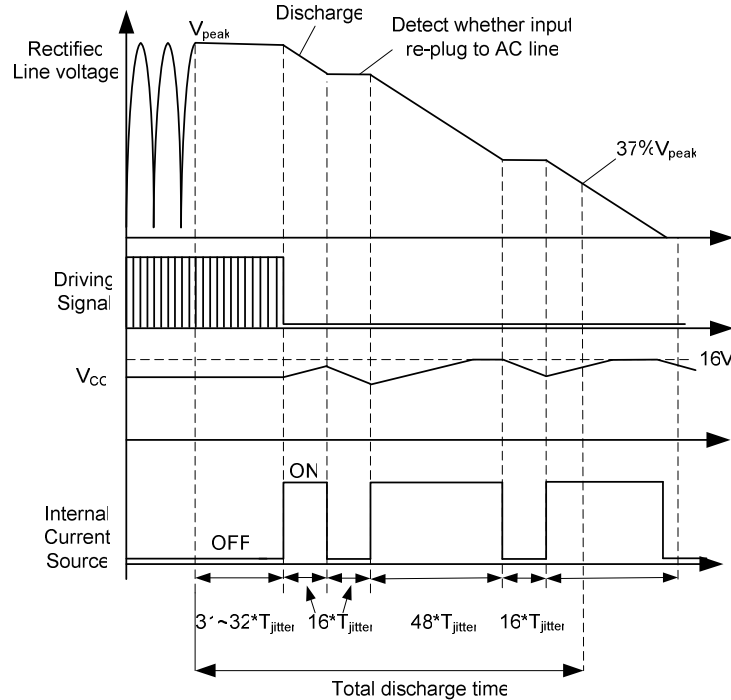
Where  $C_{TIMER}$  is the capacitor connected to TIMER pin.

In theory, the smaller  $f_{jitter}$ , the better harmonic suppression effect. However, due to measurement bandwidth requirements,  $f_{jitter}$  should be large compared to spectrum analyzer RBW for effective EMI reduction [2]. Also,  $f_{jitter}$  should be less than the control loop gain crossover frequency to avoid disturbing the regulation of output voltage. As a result,  $f_{jitter}$  is recommended between 200Hz~400Hz.

**K. X-cap Discharge Time Estimate**

When the AC voltage is unplugged, the IC turns on high voltage current source after 31~32 TIMER cycles to discharge the energy of X-cap. The first discharge duration is 16 TIMER cycles, then IC turns off current source for 16 TIMER cycles to detect whether the input is re-plugged to AC line. If AC input is still disconnected, the IC will turn on current source for 48 TIMER cycles and then re-detect for 16

TIMER cycles repeatedly until the voltage on X-cap drops to  $V_{cc}$ . Once the reconnected AC input is detected, high voltage current source won't turn on until  $V_{cc}$  drops to 5.3V then recharge  $V_{cc}$  for restart of system. Figure 14 shows the waveforms of discharge function. The max time of discharge occurs at high-line input and no-load condition because the energy on X-cap is only released but can't be delivered to bulk capacitor.



**Figure 14: X-cap discharge function**

The max delay time of discharge action is

$$T_{\text{delay}} = 32 \cdot T_{\text{jitter}} \quad (40)$$

When high voltage current source turns on, a constant supply current  $I_{\text{HV}}$  (1.6mA minimum) flows into HV pin. On time of the current source discharging the X-cap to 37% of peak voltage can be estimated by:

$$T_{\text{discharge}} = \frac{C_X \cdot 63\% \cdot \sqrt{2} \cdot V_{\text{ac(max)}}}{I_{\text{HV}}} \quad (41)$$

Where  $C_X$  is capacitance of the X-cap,  $V_{\text{ac(max)}}$  is RMS value of the max AC input. The first discharging section is  $16 \cdot T_{\text{jitter}}$ , others are  $48 \cdot T_{\text{jitter}}$  since the second. The times of section can be calculated:

$$n = \frac{T_{\text{discharge}} - 16 \cdot T_{\text{jitter}}}{48 \cdot T_{\text{jitter}}} + 1 \quad (42)$$

Rounded  $n$  is the times of detecting section, as every section is  $16 \cdot T_{\text{jitter}}$ , the detecting time is shown as follow:

$$T_{\text{detect}} = 16 \cdot T_{\text{jitter}} \cdot n \quad (43)$$



As a result, the total discharge time can be got as equation (44).

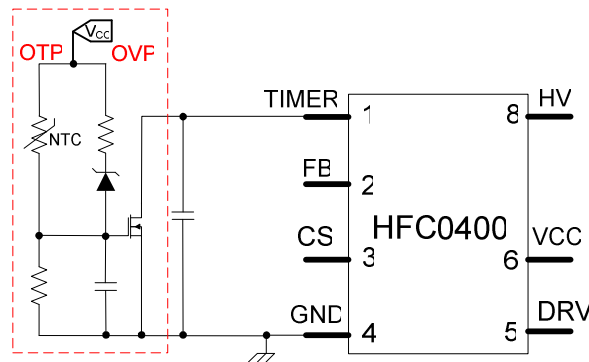
$$T_{total} = T_{delay} + T_{discharge} + T_{detect} \tag{44}$$

The total discharge time is relative to  $T_{jitter}$ . For example, if  $C_{TIMER}$  is 47nF,  $T_{jitter}=3.7ms$ , in order to discharge the X-cap in 1 second due to the value deviation of X-cap, the X-cap should be less than 3.3 $\mu$ F.

Though the X-cap is discharged, high voltage may be maintained on the bulk capacitor. For safety, make sure it is released before the board is debugged.

**L. External OTP or OVP Circuit by TIMER Pin Latch-off (Optional)**

If voltage on TIMER pin gets less than 1V for 12 $\mu$ s, the controller enters latch-off mode. OTP or OVP also can be realized by adding external circuit shown in Figure 15 on TIMER pin. Take OVP for an example, when output loop is open, Vcc voltage rises as well as output. If the voltage on gate of MOSFET dividing Vcc by zener and resistors exceeds gate threshold VGS(th), MOSFET turns on so TIMER voltage is pulled down to latch the controller.



**Figure 15: External OTP or OVP circuit**

## 5. DESIGN SUMMARY

- A detailed reference design of flyback converter with HFC0400 controller is shown in Figure 16 and 17. The input voltage is 85Vac to 265Vac and the outputs are 5V/3A and 16V/1.5A.
- The transformer used in this design has a turn ratio of 57:9:3:9 (Np:Naux:Ns1:Ns2) with 870μH primary inductance. The transformer size selected is ER28. The winding structure is shown as Figure 18, 19 and Table 2.

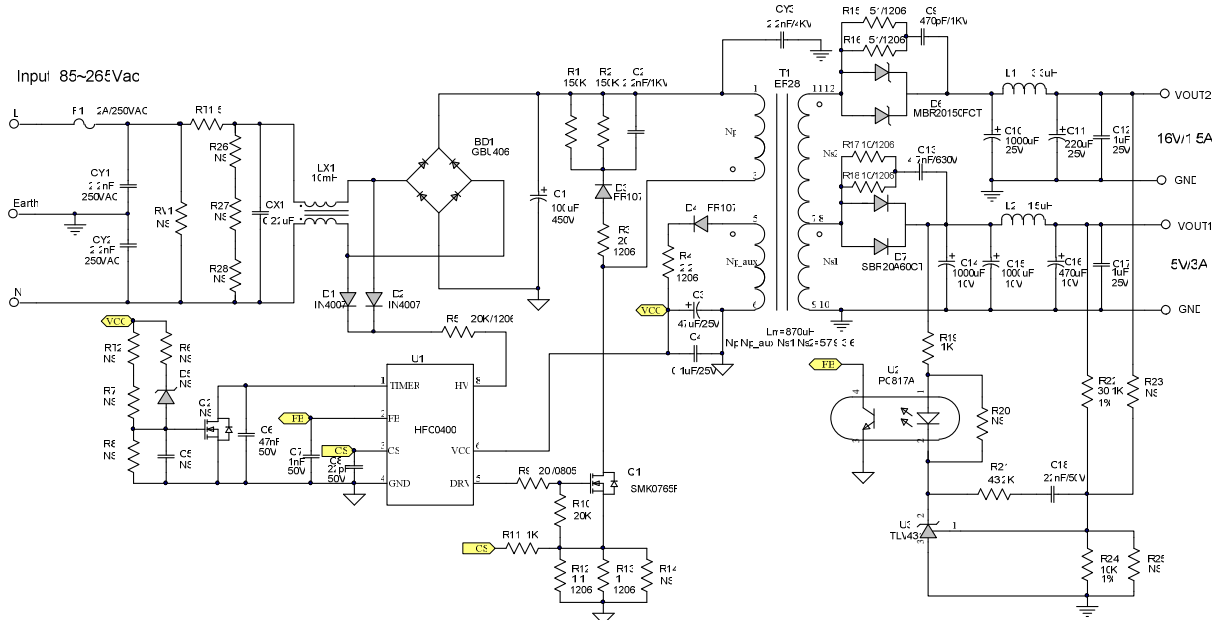
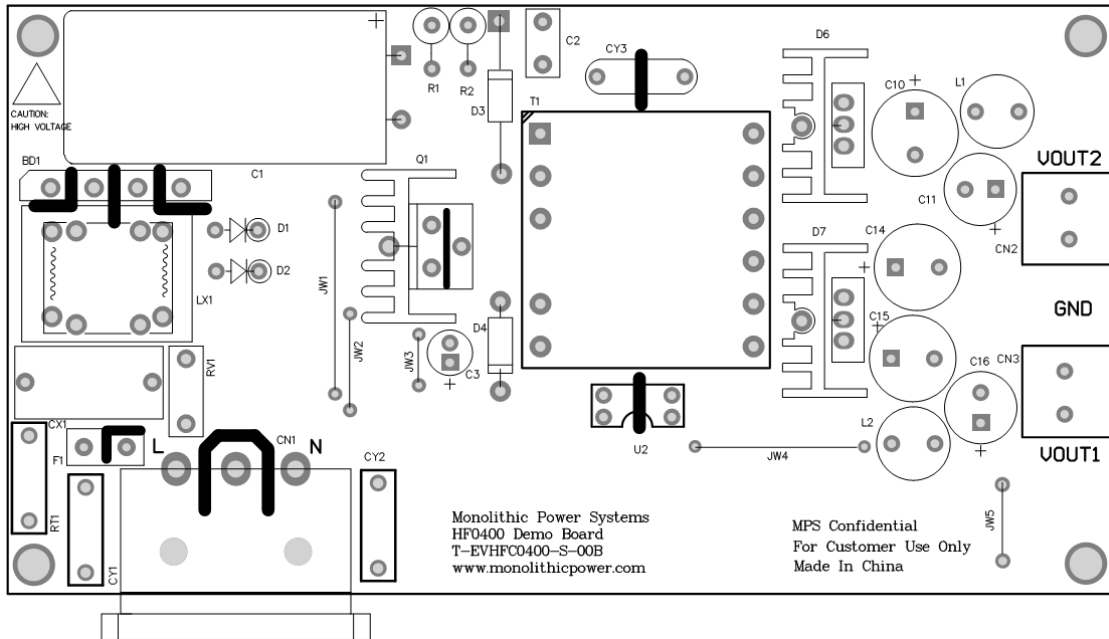
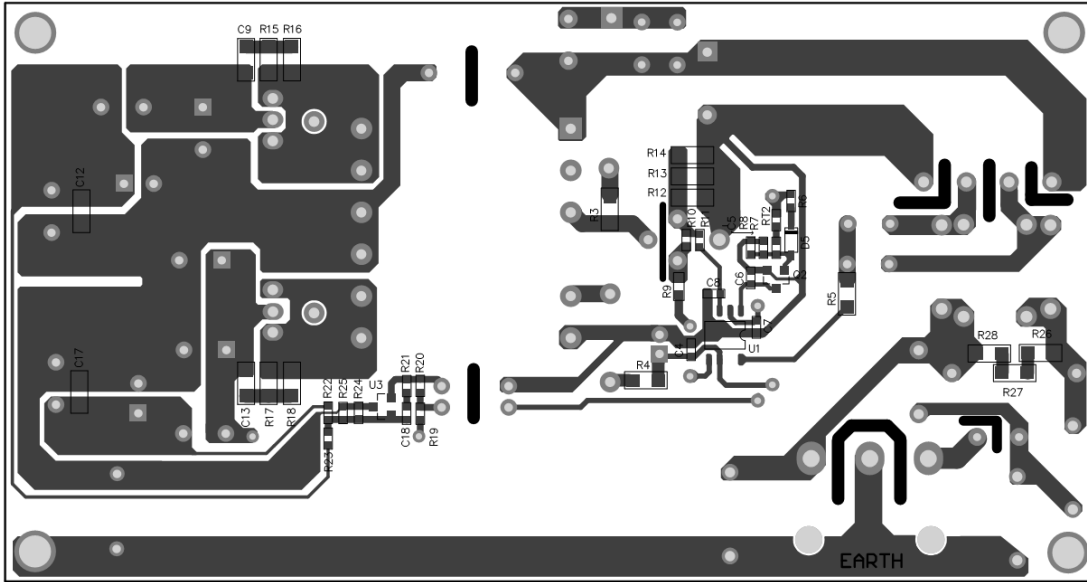


Figure 16: Schematic of HFC0400 Application for Multiple output



a) Top View



b) Bottom View

Figure 17: PCB Layout

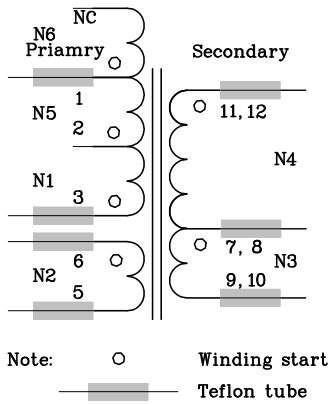
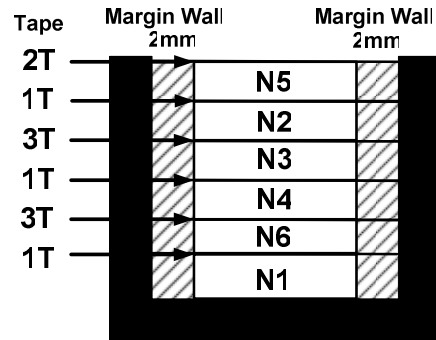


Figure 18: Connection Diagram



Bobbin

Figure 19: Winding Diagram

Table 2: Winding order

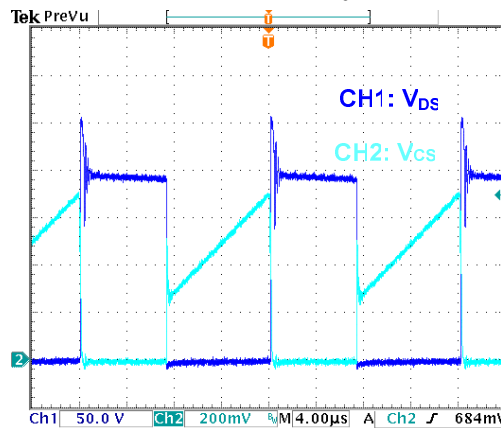
Tape(T)	Winding	Margin Wall PRI side	Terminal Start→End	Margin Wall SEC side	Wire Size (φ)	Turns ( T )
1	N1	2mm	3→2	2mm	0.27mm*2	28
1	N6	2mm	1→NC	2mm	0.3mm*1	20
3	N4	2mm	7,8→9,10	2mm	0.33mm*12	3
1	N3	2mm	11,12→7,8	2mm	0.33mm*5	6
3	N3	2mm	11,12→7,8	2mm	0.33mm*5	6
1	N2	2mm	5→6	2mm	0.27mm*1	9
2	N5	2mm	2→1	2mm	0.27mm*2	29

## 6. EXPERIMENTAL VERIFICATION

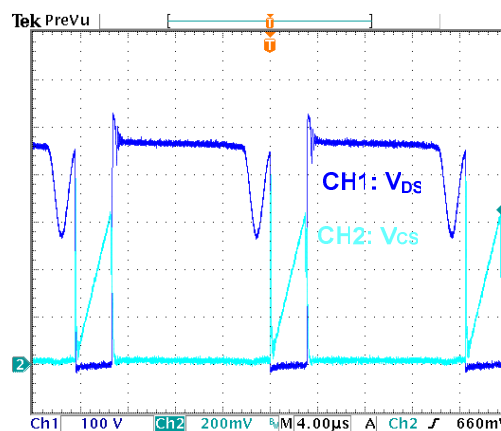
To verify design procedure presented in this application note and the performance, a prototype based in Figure 16 is built and tested with specified input/output condition (Input: 85Vac~265Vac; Output: 5V/3A, 16V/1.5A). The converter is designed to operate at CCM at 85Vac input and full load. Figure 20 and 21 show the current and drain-source voltage waveform of primary MOSFET. With built-in slope compensation, there is no sub-harmonic oscillation when duty is larger than 0.5.

Figure 22 shows the conducted EMI of the prototype, Figure 23 to Figure 27 shows the protections of converter with HFC0400 at different fault condition. With various integrated protections, the converter is more reliable under fault conditions.

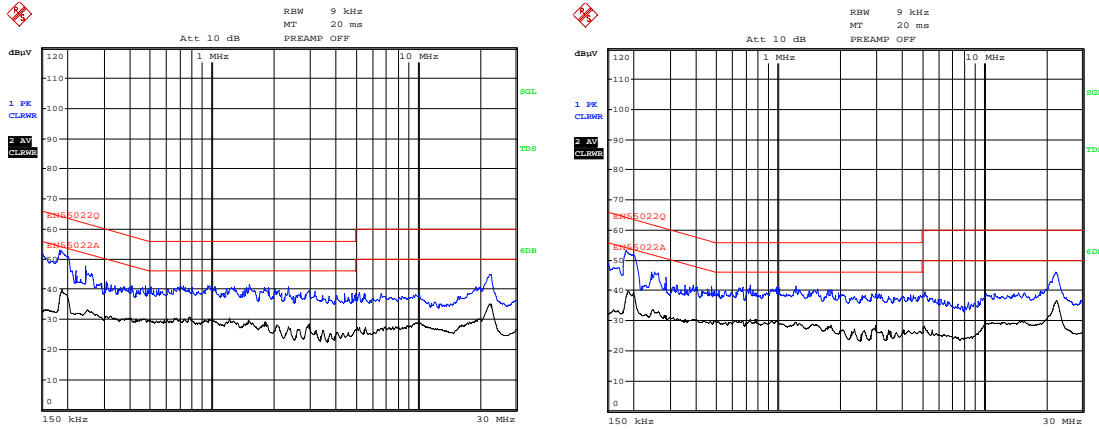
Figure 28 shows the measured efficiency. From the efficiency curve, the efficiency is still high at light load condition due to decreased switching frequency. Figure 29 shows waveform of the x-cap discharge when input is plugged. Figure 30 shows the burst mode operation at no-load condition. The power consumption at standby mode is given in Table 3. Due to the x-cap discharge function and burst mode operation, the power loss at no load condition is very small, even at high line input.



**Figure 20: Drain Voltage and Current of MOSFET at 85VAC Input**



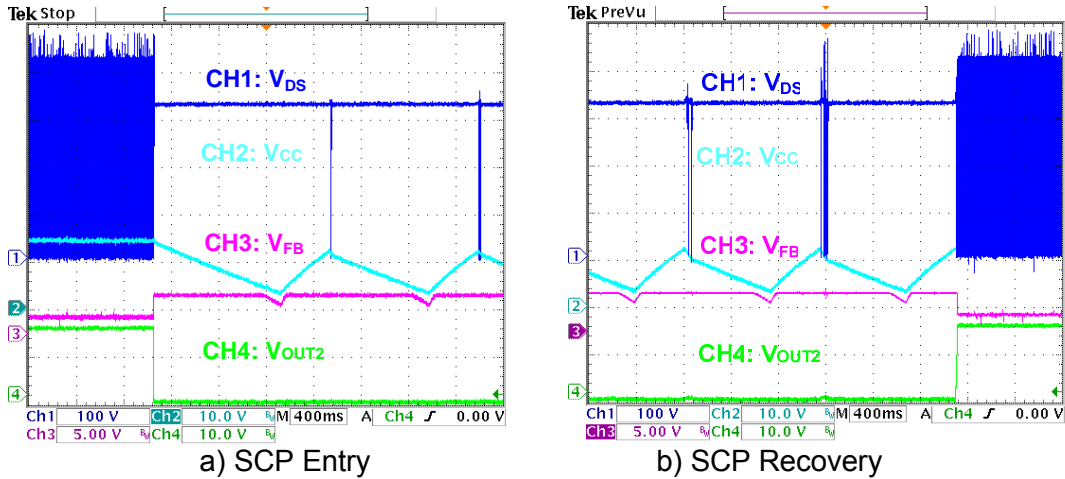
**Figure 21: Drain Voltage and Current of MOSFET at 265VAC Input**



EMI, L-Wire

EMI, N-Wire

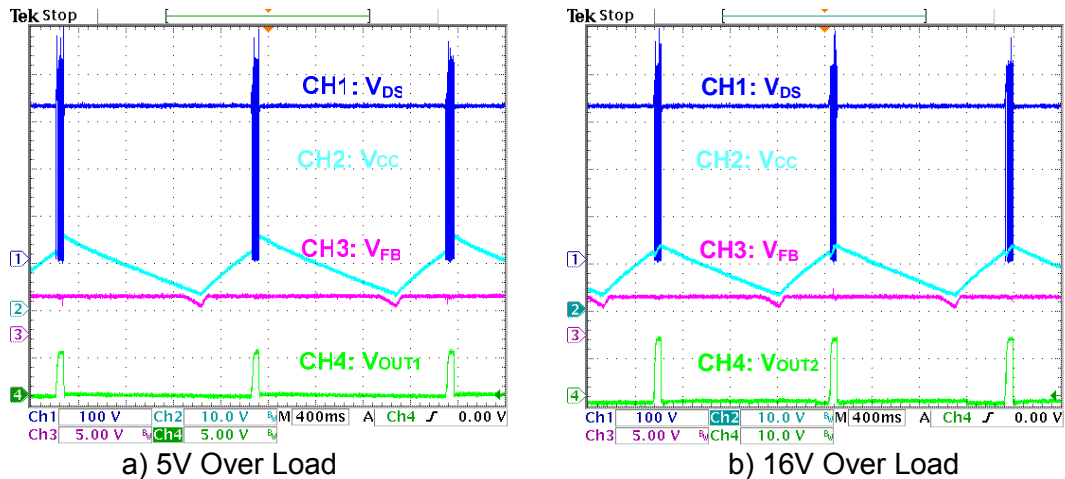
**Figure 22: Conducted EMI Test Result (230VAC Input)**



a) SCP Entry

b) SCP Recovery

**Figure 23: Output Short Circuit Protection (230VAC Input, 16V Shorted)**



a) 5V Over Load

b) 16V Over Load

**Figure 24: Over Load Protection (230VAC Input)**

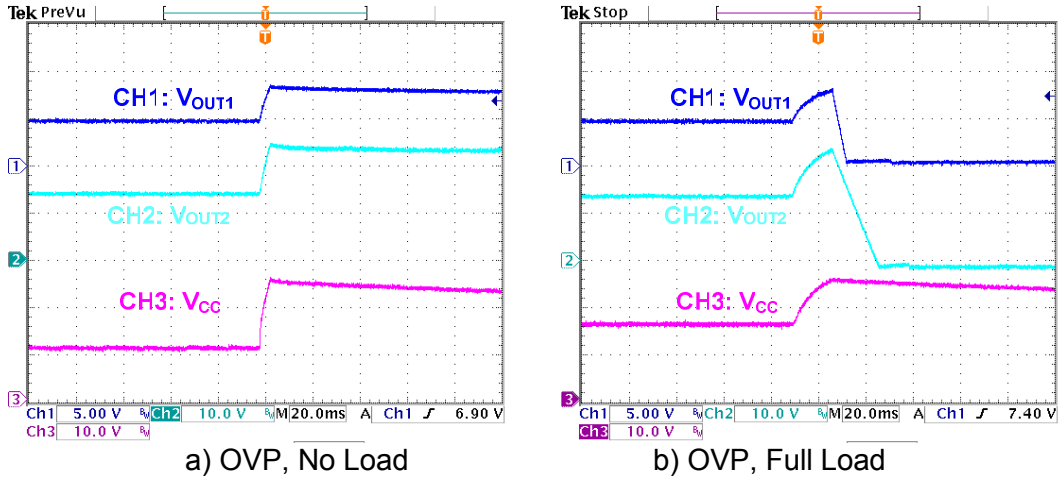


Figure 25: Output Over Voltage Protection (230VAC Input)

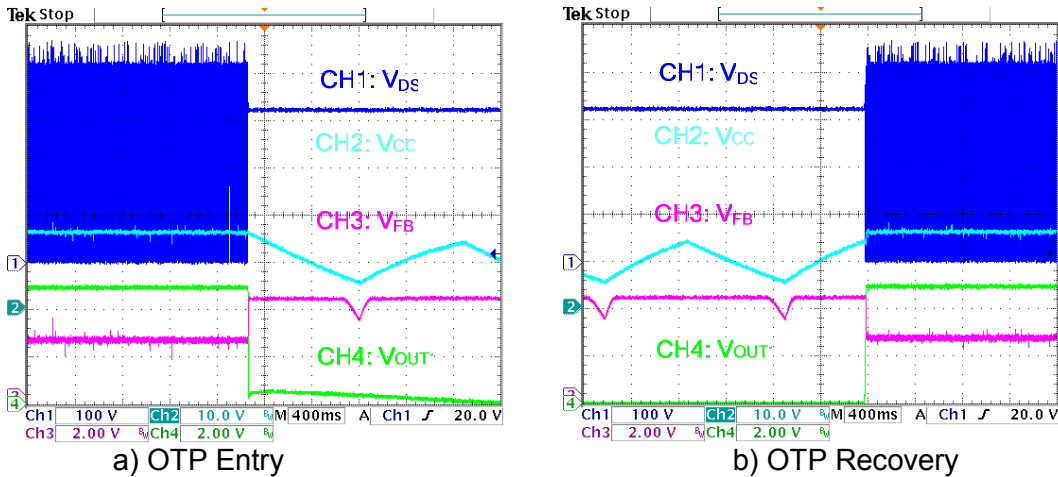


Figure 26: Over Temperature Protection (230VAC Input)

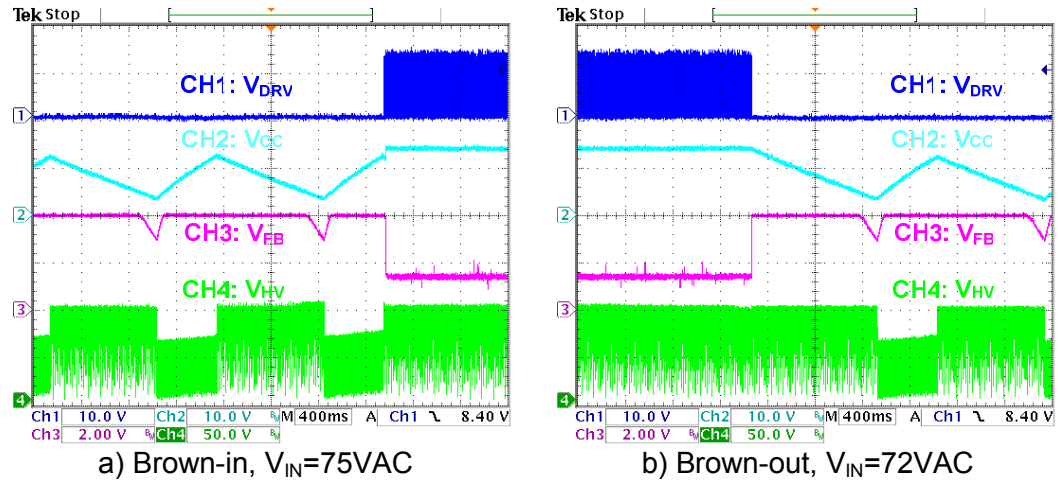


Figure 27: Brown-out Protection

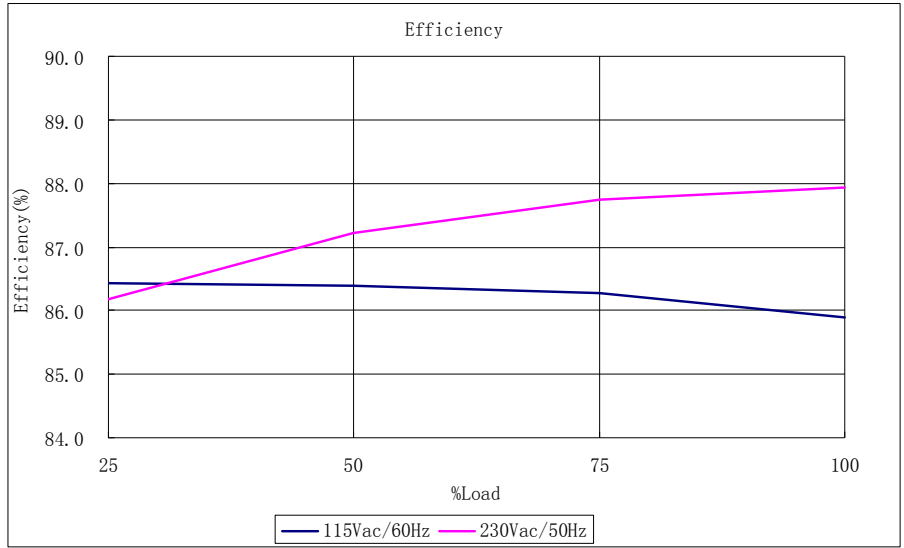
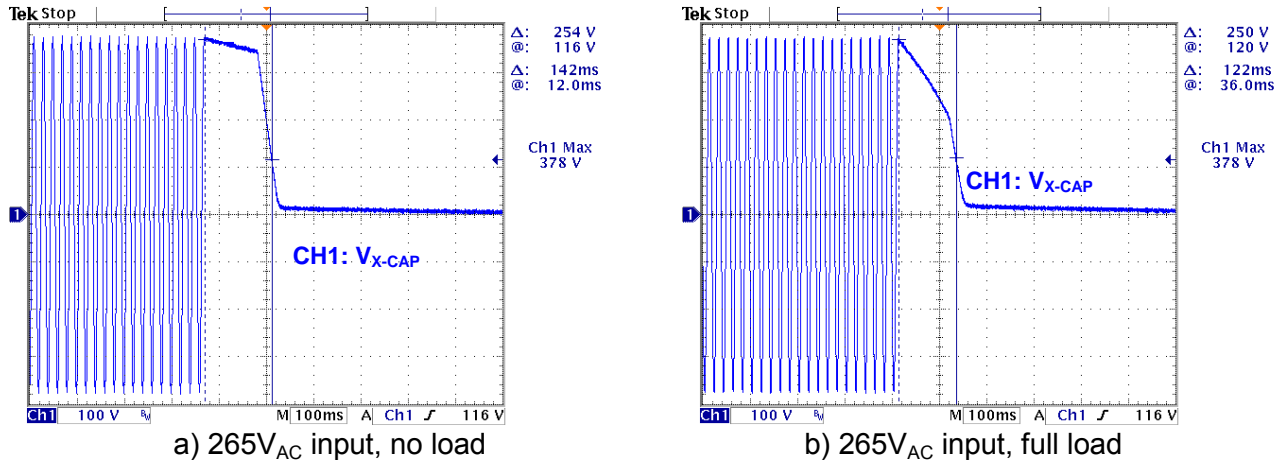


Figure 28: Efficiency of Prototype



a) 265V<sub>AC</sub> input, no load

b) 265V<sub>AC</sub> input, full load

Figure 29: X-cap Discharge of HFC0400

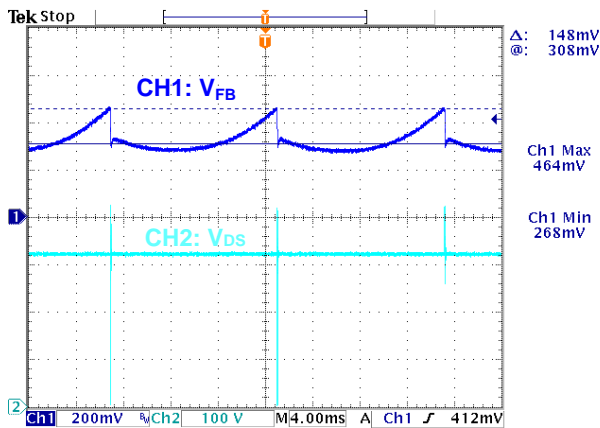


Figure 30: Burst Mode Operation of HFC0400 (230VAC Input, no load)

**Table 3: No Load Consumption at Different Input**

$V_{in}$ (V <sub>AC</sub> /Hz)		85/60	115/60	230/50	265/50
Pin (mW)	5V/0A, 16V/0A	26.35	27.59	32.40	35.26
	5V/6mA, 16V/0A	71.92	72.72	80.70	84.83

## 7. REFERENCES

- [1]. Lloyd H. Dixon, "Magnetics Design for Switching Power Supplies," in *Unitrode Magnetics Design Handbook*, 1990.
- [2]. F.Lin, D.Y. Chen, "Reduction of Power Supply EMI Emission by Switching Frequency Modulation," IEEE Trans. Power Electronic., vol.9, pp 132-137, Jan 1994.

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