Application Note for Flyback Converter

Using the Primary-Side Regulator MP020-5

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ABSTRACT

This paper mainly presents design guidelines for flyback converter using the primary-side regulator-MP020-5. Typical application schematic is shown in Figure 1. Design of a flyback converter with primary-side regulator of MP020-5 is quite simple and straightforward through the step-by-step design procedure described in this application note. Some importance aspects we need to pay attention during the design procedure are also clearly stated. Experimental results based on the design example are presented in the last part.

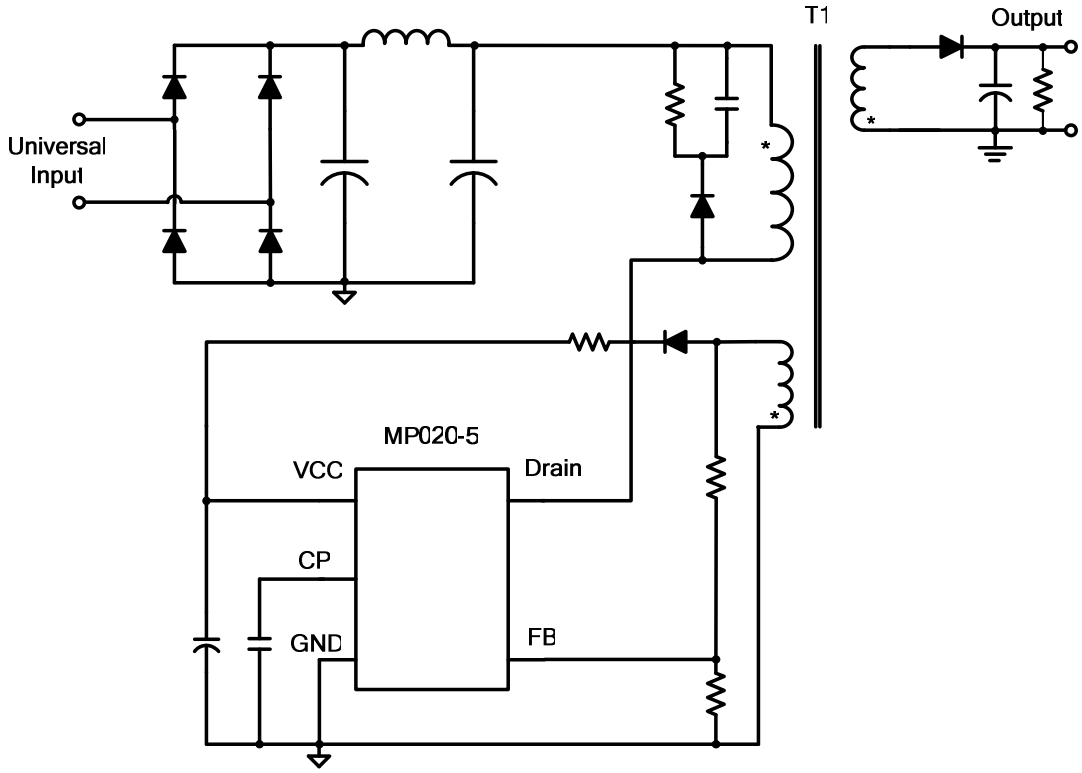

Figure 1-Flyback Converter with the Primary-Side Regulator-MP020-5

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1. INTRODUCTION

The MP020-5 is a high performance AC/DC power supply regulator adopting primary-side control technique which can provides accurate constant output voltage and tight constant output current regulation without opto-coupler and a secondary feedback circuit. MP020-5 has an integrated 700V MOSFET designed for offline supplies within 5W output power. Typical applications include cell phone charges, adapters for handheld electronics, stand-by and auxiliary power supplies and LED driver and so on.

The IC uses a variable off-time control method and it always operates in discontinuous conduction mode (DCM). The regulator decreases its frequency as the load becomes lighter. As a result, it offers excellent light load efficiency and the switching frequency will decrease to the minimum frequency when converter run at no load conditon.

The MP020-5 also features complete protection functions such as VCC under-voltage lockout, over-current protection, over temperature protection, open loop protection and over voltage protection. Its internal high-voltage start-up current source and power-saving technologies limit the no-load power consumption to less than 30mW.

Table 1: Output power table

Part Num.				Maximum Output Power(W) (85-265Vac)
	Ron(Ω)	I_limit(A)	Package	Adapter
MP020-5GS	10	0.38	SOIC8-7A	**5**

This application note presents detailed step-by-step design guidelines for an off-line flyback converter employing MP020-5, mainly including transformer design, component selection and other key points.

2. PRIMARY-SIDE REGULATOR OPERATION INTRODUCTION

The MP020-5 is a high performance AC/DC power supply regulator for the cost effective low power charger and adapter applications. It can achieve accurate constant voltage (CV) and tight constant current (CC) regulation without opto-coupler and secondary control circuitry. Meanwhile, it also eliminates the need of loop compensation circuitry while maintaining system stability. In addition, its internal high-voltage start-up current source and power-saving technologies limit the no-load power consumption to less than 30mW.

The MP020-5 uses a variable off-time control method (PFM) and it always operates in discontinuous conduction mode. So, the switching frequency presents a linear characteristic with the change of load. The CV and CC regulation are all realized by modulating switching frequency.

Constant Voltage Operation (CV)

The MP020-5 detects the auxiliary winding voltage from the FB pin and operates in constant voltage (CV) mode to regulate the output voltage.

Assuming the secondary winding and the auxiliary winding are well coupled, the FB pin voltage can be got as follow:

$$V_{FB} = \frac{N_{aux}}{N_s} \times (V_O + V_f) \times \frac{R_{down}}{R_{up} + R_{down}} \quad (1)$$

Where V_f is the secondary diode forward drop voltage. Rup and Rdown are the divided resistors.

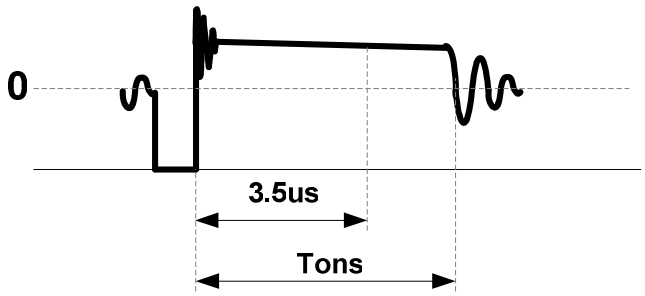


Figure 2- Auxiliary Winding Waveform

The output voltage is different from the secondary voltage because of a current-dependant diode forward voltage drop. If the secondary voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary voltage will be a fixed V_f. The MP020-5 samples the auxiliary winding voltage at 3.5μs after the primary switch turns off. The CV loop control function of MP020-5 then generates the secondary side diode OFF time to regulate the output voltage.

Constant Current Operation (CC)

Figure-3 shows the illustration of the constant current operation.

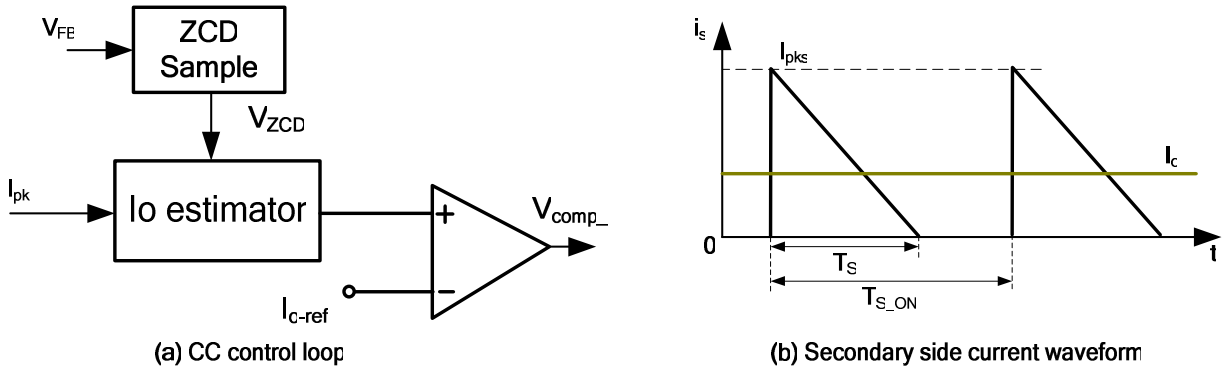


Figure 3- CC Operation

The flyback always works in DCM using the MP020-5 and in constant current (CC) operation, the ZCD sample block can detect the duty cycle of the secondary side diode. The calculated output current from the Io estimator block compares with I_{o_ref} and the error signal V_{comp_i} controls the turn on signal of the integral MOSFET. So the output current Io can be got as follow from the Figure 3.

$$I_o = \frac{1}{2} \times \frac{N_p}{N_S} \times I_{pk} \times D_s \quad (2)$$

Where:

D_s: the duty cycle of the secondary diode;

I_{pk}: the peak current of the primary side MOSFET;

N_p: the turns of the transformer primary side

N_s: the turns of the transformer secondary side.

3. DESIGN PROCEDURE

There is quite few external component need to choose so it makes the application simple and cost down. The key parameter is the primary-secondary turns ratio of the transformer for tight CC characteristic and the Design flow about the transformer can be referred to Figure 4.

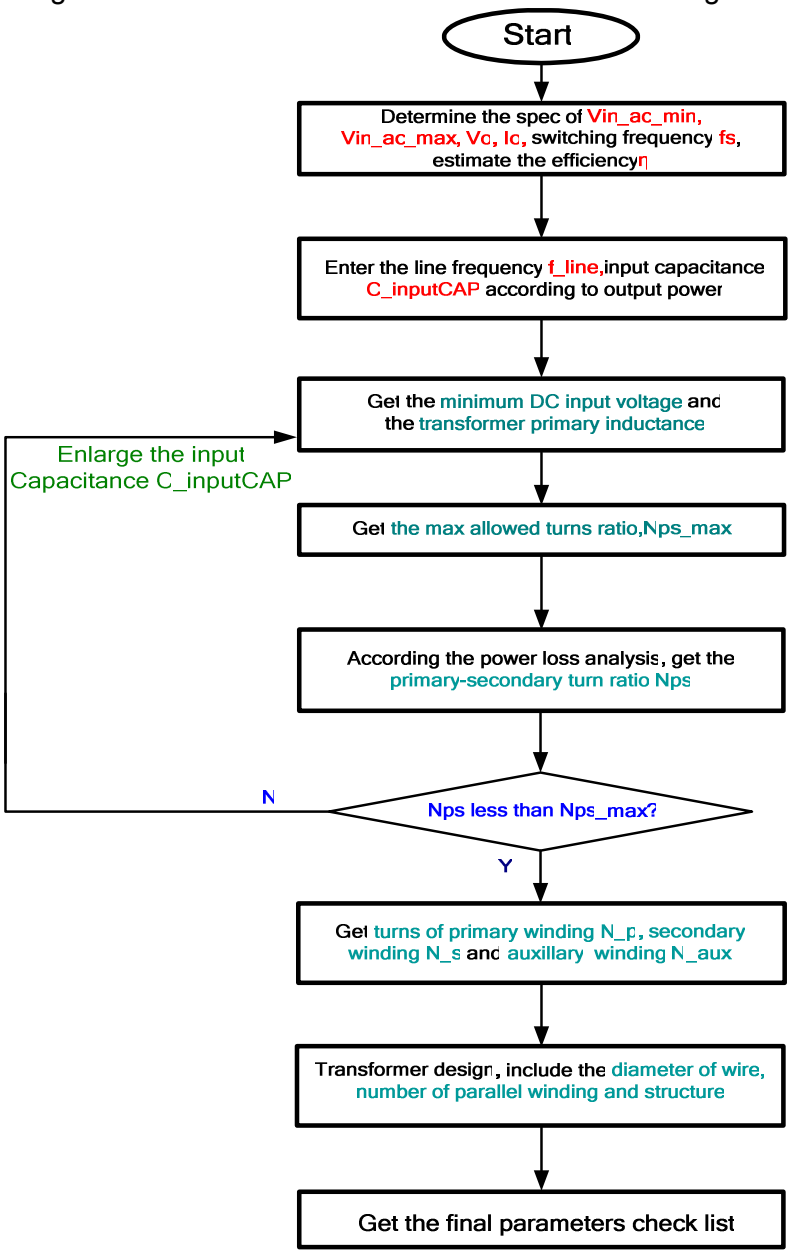


Figure 4- Transformer Design Flow Chart

A. Predetermined Input and Output Specifications

- Input AC voltage range: $V_{AC(min)}$, $V_{AC(max)}$, for example 85Vac~265Vac RMS universal input;
- Output: V_o, $I_{o(min)}$,$I_{o(max)}$,P_{out};
- Estimated efficiency: η, it is used to estimate the power converter efficiency to calculate the maximum input power. Generally, η is set to be 0.65~0.8 according to different output applications. For example, η can be estimated about 0.7 in the 5W cell phone application.

Then the maximum input power can be given as:

$$P_{in} = \frac{V_o \times I_o}{\eta} \quad (3)$$

Figure-5 illustrates the typical DC bus voltage waveform. The DC input capacitor $\mathbf{C_{in}}$ is usually set as 2uF/W for the universal input condition and full bridge rectifier for 230Vac single range application, the capacitance can be half the value.

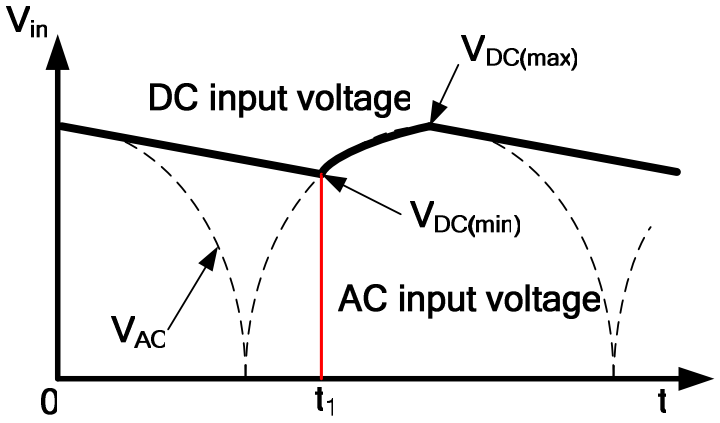


Figure 5- Input Voltage Waveform

From Figure-5, the AC input voltage Vac and DC input voltage V_{DC} can be got as follow:

$$V_{DC}(V_{ac}, t) = \sqrt{2 \times V_{ac}{}^2 - \frac{2 \times P_{in}}{C_{in}} \times t} \quad (4)$$

At t1, the DC bus voltage equals to the AC input again, and the DC bus capacitor will be charged up again. Then, the DC bus voltage at t1 is its minimum value $V_{DC(min)}$, which can be calculated as:

$$V_{DC(min)} = V_{DC}(V_{AC(MIN)}, t_1) \quad (5)$$

Then, the minimum average DC input voltage $V_{in(min)}$ is given as:

$$V_{IN(min)} = \frac{\sqrt{2} \cdot V_{ac(min)} + V_{DC(min)}}{2} \quad (6)$$

The maximum average DC input voltage Vin(max) can be got as :

$$V_{IN(max)} = \sqrt{2} \cdot V_{ac(max)} \quad (7)$$

In application, the minmum DC input voltage should be not too low which can not supply the full load. It's recommend that the minmum DC input voltage is not less than 2/3 Nps(Vo+Vf). If the minmum DC input voltage is too low, the input line ripple and output ripple will be bigger than normal operation.

B. Determine the Startup Circuitry

Initially, the IC is self supplied by the internal high voltage current source, which is drawn from the Drain pin. The internal high voltage current source will turn off for better efficiency as soon as the voltage of Vcc pin reaches the Vcc ON threshold. Afterward, it will be taken by the auxiliary winding of the transformer. When Vcc falls below the Vcc OFF threshold, the IC stops the switching and the internal high voltage current source turns on again. The theoretical startup waveforms are shown as Figure6.

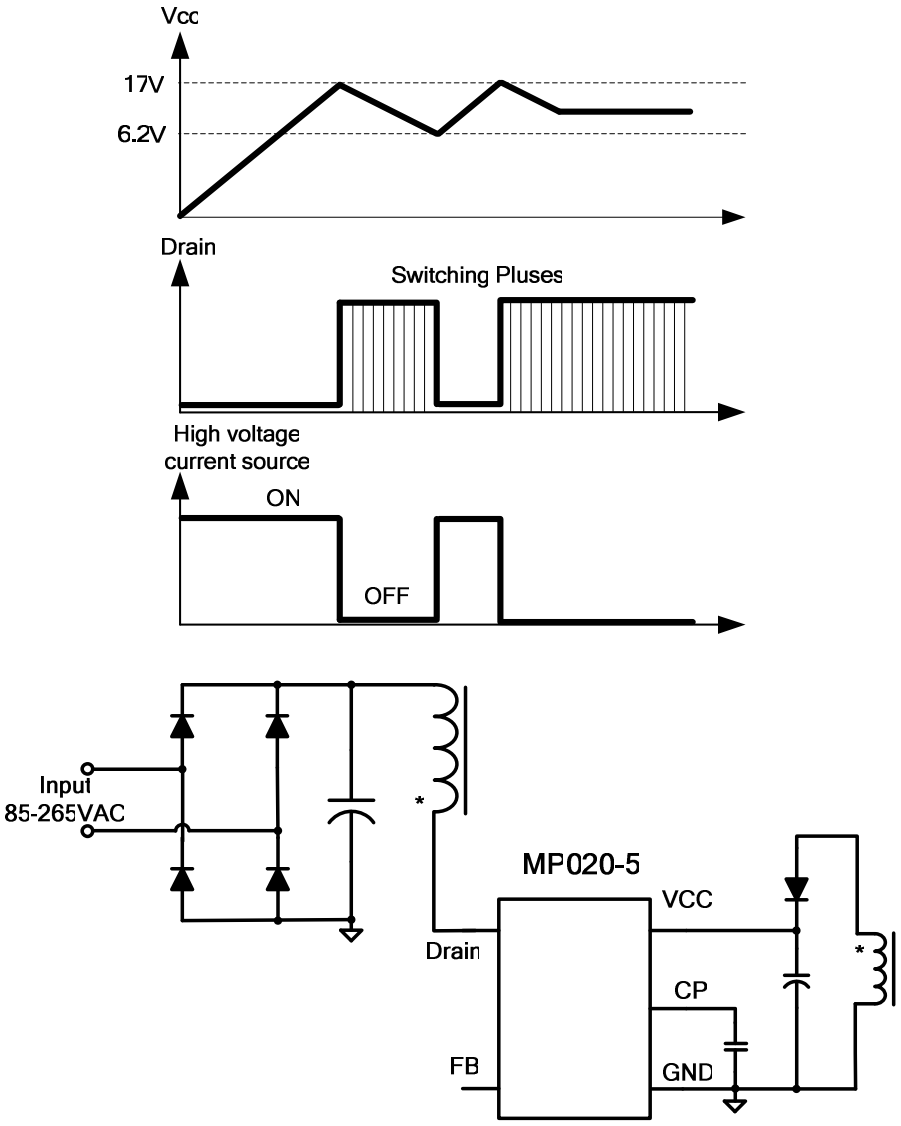


Figure 6- Vcc UVLO

To satisfy the requirement of the startup time, the cap of the VCC should be chose as follow:

$$C_{vcc} \leq \frac{I_{charge} \cdot T_{startup}}{V_{CCH}} \quad (8)$$

Where:

C_{vcc}:the cap of Vcc for IC power supply;

I_{charge}: the charge current of internal high voltage current;

$T_{startup}$: the startup time of the IC start to work normally;

V_{CCH}: the Vcc on threshold or the threshold of the internal high voltage current source turn off;

For example, if the $T_{startup}$ is 0.5s, I_{charge} is 550μA typically, V_{CCH} is 17.3V typically, so the Vcc can be calculated about 16μF.

C. Primary Side Inductance Lp

For a flyback converter with MP020-5, due to the DCM operation, the output power is given as:

$$P_o = \frac{1}{2} \cdot L_m \cdot I_{pk}^{\ 2} \cdot f_s \cdot \eta_s \quad (9)$$

Where L_m is the inductance of the transformer, I_{pk} is the peak current of the primary-side(I_{pk} is constant about 0.38A in MP020-5), f_s is the switching frequency of the converter at full load and the η_s is the efficiency of the power transferred to secondary side by transformer, as usually,. η_s can be estimated about 0.95 in 5W application.

The output power Po increases linearly with the switching frequency f_s increase because the Ipk keeps constant. So, we can calculate the Lm with equation (10).

$$L_m = \frac{2 \cdot P_o}{I_{pk}^{\ 2} \cdot f_s \cdot \eta_s} \quad (10)$$

D. Turns Ratio-Nps

The system should work in DCM under all conditions, especially with minimum input voltage and full load. Therefore equation (11) must be satisfied to guarantee the converter in DCM operation with minimum input voltage and full load condition. According to (11), we can derive the maximum turn ratio Nps limitation.

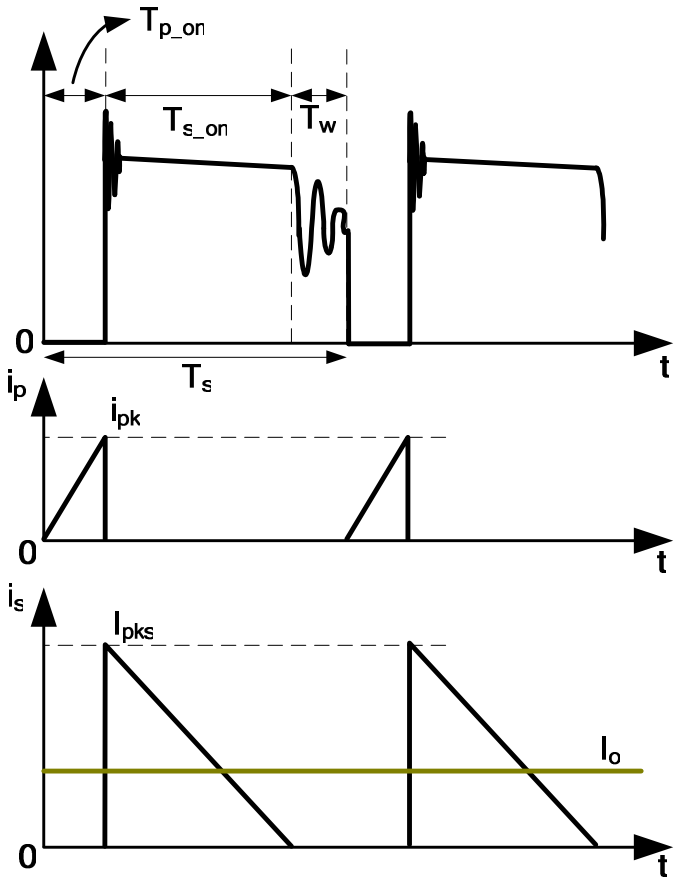


Figure 7- V_{DS}, Primary Side Current and Secondary Side Current

$$T_s \geq T_{p\_on} + T_{s\_on} \quad (11)$$

Where:
T_{p_on}: the time of switch turn on;
T_{s_on}: the time of secondary side diode turn on;
T_s: the working cycle;
T_w: the resonant time of inductance and capacitor of the switch;
I_{pk}: the peak current of the primary side;
I_{pks}: the peak current of the secondary side;

D-1. Maximum N_{ps}

Figure-7 shows the primary side MOSFET Drain-Source voltage, primary side current and secondary side current waveform. Since the converter operates in DCM mode, the magnetizing current increases from zero to its peak value and then drops to zero linearly in each switching cycle. The primary side switch on time and secondary diode on time can be calculated as follow:

$$T_{p\_on} = I_{pk} \frac{L_m}{V_{in}} \quad (12)$$

$$T_{s\_on} = I_{pk} \frac{L_m}{N_{ps}(V_o + V_f)} \quad (13)$$

Where:
V_f: the forward voltage of secondary diode;
N_{ps}:the transformer turns ratio (primary to secondary)

From the equation (11),(12),(13), we can get the (14).

$$I_{pk} \frac{L_m}{N_{ps}(V_o + V_f)} + I_{pk} \frac{L_m}{V_{in}} \leq T_s \quad (14)$$

As described in the operation principle of MP020-5 under CC mode, the CC loop control function of MP020-5 will keep the calculated Io by I_o estimator block about the I_{o_ref}, so the Ds is kept constant indirectly and the Ds is about 0.4 in CC mode.

$$T_s = T_{s\_on} \times \frac{1}{D_s} \quad (15)$$

So, from the equation (12), (13), (14) and (15), the following expression will be got:

$$V_{in} \geq N_{ps} \cdot (V_o + V_f) \cdot \frac{D_s}{1 - D_s} \quad (16)$$

The input DC voltage should satisfy the in equation (16) to ensure the converter can supply the power for load in DCM operation. It's easy to satisfy the in equation with high input voltage, but it should also be satisfied with low input voltage. The equation (16) can be rewritten as,

$$N_{ps} \leq \frac{V_{in}}{(V_o + V_f)} \cdot \frac{1 - D_s}{D_s} \quad (17)$$

When the Vin is the minimum value, the maximum N_{ps} can be got as following:

$$N_{ps} \leq N_{psmax} = \frac{V_{inmin}}{(V_o + V_f)} \cdot \frac{1 - D_s}{D_s} \quad (18)$$

Ineqation (18) sets the up limit for the transformer turns ratio with a given minimum DC voltage. If the calculated N_{ps} described below doesn't satisfy the in equation (18), we should recalculate the N_{ps} by increasing the value of the input cap to increase the $V_{inmin.}$

D-2. N_{ps} calculation

Figure-8 shows the ideal current waveform at secondary side, the output current can be easily calculated as:

$$I_o = \frac{1}{2} \times I_{pks} \times \frac{T_{s\_on}}{T_s} = \frac{1}{2} \times I_{pks} \times D_s \quad (19)$$

I_{pks} is the peak current of the secondary side.

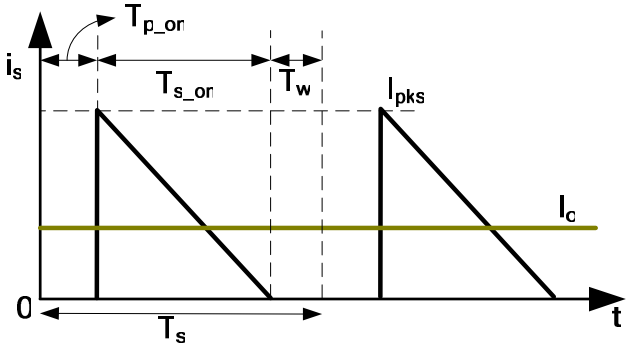


Figure 8- Secondary Side Current Waveform

And,

$$I_{pks} = N_{ps} \cdot I_{pk} \quad (20)$$

Assume there is no power loss during the period when the magnetizing currnt transfers from primary side to secondary side after the primary siwtch turns off and the transition time can be neglected, so we can take (20) into equation (19),

$$I_o = \frac{1}{2} \times N_{ps} \times I_{pk} \times D_s \quad (21)$$

Baed on the equation(21), the Nps can be determined based on the desired output current under this ideal assumption.

$$N_{ps} = \frac{2 \times I_o}{I_{pk} \times D_s} \quad (22)$$

In practice applicaiton, there is always leakage inductance and core loss,so the acutual I_{s_pk} will be slightly less than $N_{ps} \cdot I_{pk}$. And the practical waveform is illustrated as Figure-9.

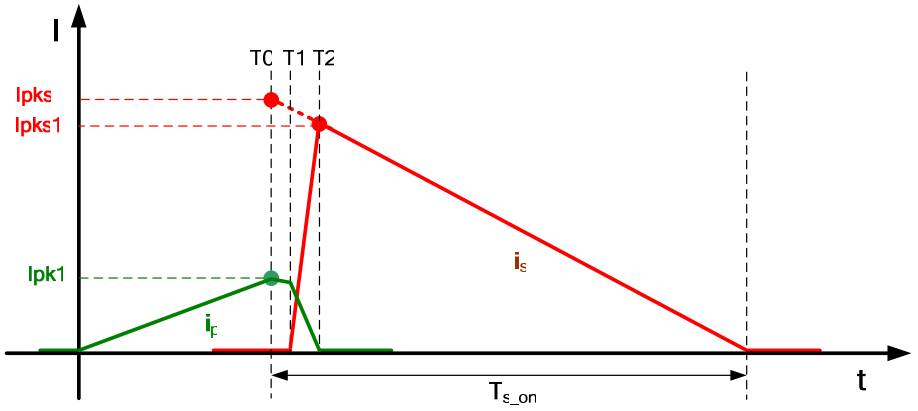


Figure 9- The Transition of the Primary Side Current and Secondary Side Current

Considering the leakage inductance and core loss, the energy transferred to output should exclude the energy stored in the leakage inductor and the core loss. The power stored in the leakage inductor is given in equation(23).

$$P_{lk} = \frac{1}{2} \cdot L_k \cdot I_{pk}^{\ 2} \cdot f_s \tag{23}$$

Assume the coupling coefficient of the transformer is K and K is determined by transformer structure.

$$K = 1 - \frac{L_k}{L_m} \tag{24}$$

So the equation(23) also can be expression as follow:

$$P_{lk} = \frac{1}{2} \cdot (1-K) L_m \cdot I_{pk}^{\ 2} \cdot f_s \tag{25}$$

On the other side ,the core loss can be got as follow:

$$P_{trans} = C_m \cdot f_s^{\ x} B_{ac}^{\ y} \cdot (C_{to} - C_{t1} \cdot T_{core} + C_{t2} \cdot T_{core}^{\ 2}) \cdot V_e \tag{26}$$

Where:

C_m, x, y, C_{t0}, C_{t1}, C_{t2} are coefficients related to core of PC40, C_m=2.65901, x=1.37276, y=2.51937, C_{t0}=4.2061, C_{t1}=0.065, C_{t2}=0.00032938483. The coefficients should be adjusted according different materials.

T_{core}: the working temperature of the core;

V_e: the volume of the core;

Considering these effect, the practical power transferred to secondary side can be got :

$$P_{lm} = P_m - P_{lk} - P_{trans} \tag{27}$$

According the equation(23), (24), (25), (26), (27), the equivalent peak current of primary side can be got as follow:

$$I_{pk1}=\sqrt{\frac{2\cdot(P_m-P_{lk}-P_{trans})}{L_m\cdot f_s}}=\sqrt{\frac{K\cdot L_m\cdot {I_{pk}}^2\cdot f_s-2\cdot P_{trans}}{L_m\cdot f_s}} \quad (28)$$

If the transition time can not be ignored, the practical secondary side peak current can be got as equation (29):

$$I_{pks}=N_{ps}\cdot\sqrt{\frac{K\cdot L_m\cdot {I_{pk}}^2\cdot f_s-2\cdot P_{trans}}{L_m\cdot f_s}} \quad (29)$$

Due to the exisiting of leakage inductance, there is certain currnt transition time when the magnetizing current transfers from primary side to secondary side as shown as figure-9.

This transition interval includes two sub-intervals, one is charging cource of paristic capacitor of the primary side mosfet (T1) and the second sub-interval is current commuation period, secondary side current rise to peak current(T2).

$$T_1=\frac{C_p\cdot[N_{ps}\cdot(V_o+V_f)+Vin]}{I_{pk}} \quad (30)$$

Where C_p is the parasitic capacitor of the primary MOSFET and T1 is just the time for voltage across the MOSFET rises from zero to $N_{ps}\cdot(V_o+V_f)+V_{in}$.

$$T_2=\frac{L_k\cdot I_{pk}}{V_{clamp}}=\frac{K\cdot L_m\cdot I_{pk}}{V_{clamp}} \quad (31)$$

Where Vclamp is the calmp voltae of RCD clamp circuit and T2 is the time of secondary side current rise from zero to peak current.

The calculation of Vclamp can be refered to RCD design and usually, the Vclamp is about 50%~100% $N_{ps}\cdot(V_o+V_f)$.

The ideal secondary side diode conduction time Ts_on and the T1,T2 can be calculated from equation (13), (30) and (31), so the secondary side peak current considering these non-ideal characteritic can be calculated as follow:

$$I_{pks1}=I_{pks}\cdot(1-\frac{T_1+T_2}{T_{s\_on}}) \quad (32)$$

So, the output current can be got:

$$I_o=\frac{1}{2}\times I_{pks1}\times D_s \quad (33)$$

According the equation(29), (30), (31), (32), (33), the relationship between output current Io and Nps is given in (34). And we can resolve it to get the desired Nps.

$$\frac{2\times I_o}{D_s}=N_{ps}\times\sqrt{\frac{K\cdot L_m\cdot {I_{pk}}^2\cdot f_s-2\cdot P_{trans}}{L_m\cdot f_s}}\times\left[1-\frac{\frac{C_p\cdot[N_{ps}\cdot(V_o+V_f)+Vin]}{I_{pk}}+\frac{K\cdot L_m\cdot I_{pk}}{V_{clamp}}}{\frac{N_{ps}\times\sqrt{\frac{K\cdot L_m\cdot {I_{pk}}^2\cdot f_s-2\cdot P_{trans}}{L_m\cdot f_s}}}{N_{ps}\cdot(V_o+V_f)}}\right] \quad (34)$$

If the N_{ps} calculated from (34) satisfies the inequation (18), the result is ok. If not, we should modify the minimum input voltage and recalculate the N_{ps} Until it satisfies inequation (20) at the same time.

E. Transformer Design

E-1. Transformer Core Selection

A core appropriate for certain output power at the operating frequency needs to be selected fristly. Ferrite is usually preferred for flyback transformer. The core area product (AeAw) which is the core magnetic cross-section area multiplied by its window area available for winding, is widely used for an initial estimate of core size for a given application. A rough indication of the required area product is given by following:

$$A_e\cdot A_w=\left(\frac{L_m\cdot I_{pk}\cdot I_{p\_rms}\times 10^4}{B_{max}\cdot K_u\cdot K_j\cdot f_{smin}}\right)^{4/3}\ cm^4 \quad (35)$$

Where:

K_u :winding factor which is usually 0.25 - 0.3 for an off-line transformer;.

K_j : the current density coefficient which is typically 400 - 600 for ferrite core;

I_{pk}: the maximum peak current of primary inductance;

I_{p_rms}: the RMS current of the primary inductance;

B_{max} : the allowed maximum flux density which is usually preset to be the saturation flux density of the core material (0.3T - 0.4T). It can be minished properly for good audible noise;

fs: the switching frequency at low line and full load condition.

MP020-5 works in DCM, so the RMS current can be given by following:

$$I_{p\_rms}=\sqrt{\frac{L_m\cdot {I_{pk}}^3}{3\times V_{inmin}}\cdot f_s} \quad (36)$$

Refer to the ferrite core manufacture's datasheet to select a proper core.

E-2. Primary and Secondary Winding Turns

With a given core size, of the primary side winding turns N_p is given as follows to prevent the core from saturation and to achieve desired inductance:

$$N_p=\frac{L_m\cdot I_{pk}}{A_e\times B_{max}} \quad (37)$$

B_{max} should be smaller than saturation density B_{sat} at high operation temperature because the B_{sat} will decrease as the temperature increases.

Secondary winding turns N_s can be easily calculated with transformer turns ratio N_{ps} and N_p, which is given as:

$$N_s = \frac{N_p}{N_{ps}} \tag{38}$$

E-3. Wire Size

Once all the winding turns are determined, the wire size should be properly chosen to minimize the winding conduction loss and leakage inductance. The winding loss depends on the its RMS current, the length and the cross section area of the wire, also the transformer winding structure.

The wire size could be determined by the RMS current of the winding. For a flyback converter, the RMS current on primary side is given by equation (39), and the RMS current on secondary side is given by following:

$$I_{s\_rms} = \sqrt{\frac{L_m \cdot I_{pk}^{\ 3}}{3 \times V_o} \cdot f_s \cdot N_{ps}} \tag{39}$$

Then, the wire cross section area required for secondary side is:

$$S_s = \frac{I_{s\_rms}}{J}(mm^2) \tag{40}$$

$$S_p = \frac{I_{p\_rms}}{J}(mm^2) \tag{41}$$

Here J is the current density of the wire which is 500A/cm^2 typically.
Due to the skin effect and proximity effect of the conductor ,the diameter of the wire should be less than $2\Delta d$ (Δd : the skin effect depth):

$$\Delta d = \sqrt{\frac{1}{\pi \cdot f_s \cdot \mu \cdot \sigma}}(mm) \tag{42}$$

Where:
σ: the conductivity of the wire, typically about $6 \times 10^7 S/m$ at 0 deg for copper, and it will increases as the temperature increases, which means the Δd will get smaller.
μ: the magnetic permeability of the conductor, which usually equals to the permeability of vacuum for most conductor, $4\pi \times 10^{-7} H/m$; If the required size of the winding is larger than Δd, multiple strands of thinner wire or Litz wire is usually adopted to minimize the AC resistance. The effective cross section area of multi-strands wire or Litz wire should be large enough to meet the requirement set by the current density.
After the wire size have been determined, it is necessary to check whether the window area with selected core can accommodate the windings calculated in the previous steps. The window area required by each winding should be calculated respectively and add together, the area for inter-winding insulation, bobbin and spaces existing between the turns should also be taken into consideration. The fill factor, means the winding area to the whole window area of the core, should be well below 1 due to these inter-winding insulation and spaces between turns. It is recommended that a fill factor no greater than about 0.3. For transformers with multiple outputs this factor may need to be reduced further.
Based on these considerations the total required window area is then compared to the available window area of a selected core. If the required window area is larger than the selected one, either wire size must be reduced, or the larger core must be chose. Of course, a reduction in wire size increases the copper loss of the transformer.

E-4. Air Gap

With the selected core and winding turns, the air gap of the core can be calculated by following expression:

$$L_{gap} = \mu_0 \cdot A_e \cdot \frac{N_p^2}{L_m} - \frac{l_c}{\mu_r} \quad (43)$$

Where:

μ_0 : the permeability of vacuum which equals $4\pi \times 10^{-7} H/m$;

μ_r : the relative magnetic permeability of the core material;

A_e: the cross sectional area of the selected core;

l_c: the core magnetic path length;

L_m: the primary inductance ;

N_p: the primary winding turns.

Usually, the μ_r is very large, so the L_{gap} can be approximately calculated as equation(44).

$$L_{gap} \approx \mu_0 \cdot A_e \cdot \frac{N_p^2}{L_m} \quad (44)$$

F. Cable Compensation

The MP020-5 has an internal output cable compensation circuit as shown in Figure-10. The internal ZCD sample can can detect the duty of the secondary side diode. The duty signal can be converted to a DC voltage through a low-pass filter. The filter voltage V_{CP} changes as the load current variety.

V_{CP} can be converted to a current signal sinks current from the FB pin. The voltage drop on the upper resistor of the divider will change the output voltage and realizes the output cable compensation..

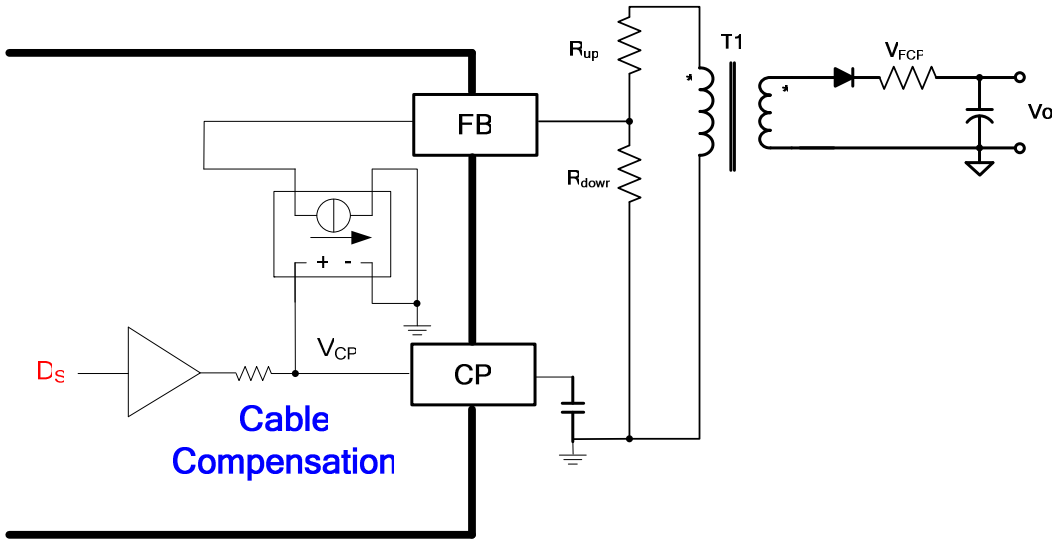


Figure 10- Output Cable Compensation

The formula of the compensation voltage of full load as follow:

$$V_{FCP} = \frac{5.6 \times D_S}{360 \times 10^3} \times 2 \times R_{UP} \times \frac{N_S}{N_{AUX}} \quad (45)$$

V_{FCP}: the compensation voltage drop on the secondary side diode and the cable resistor when full load;

D_S: the duty cycle of secondary side diode, it's about 0.4 in CC mode;

R_{up}: upper resistor of divided voltage resistor;

N_S: the secondary side winding turns of transformer;

N_{aux}: the auxiliary winding turns of transformer;

So, we can choose the R_{up} to design the cable compensation voltage.

It should be noted that the Rup is also the key component as the divider resistor to decide the output voltage. From equation (1), we can get the following equation.

$$V_{ref} = \frac{N_{aux}}{N_s} \times (V_O + V_f) \times \frac{R_{down}}{R_{up} + R_{down}} \quad (46)$$

Where the V_{ref} is the reference voltage of the IC for CV, R_{down} is the down resistor of the voltage divided resistors.

So, when the R_{up} is determined by the equation (45), then the R_{down} should be designed based on (46). To achieve more accurate CV regulation, the accuracy of these feedback resistors should be at least 1%. Besides, the divided resistors is recommended to select from 10k Ω to 100k Ω for better performance to avoid the noise disturb the internal logic.
Another key point for the good CV characteristic is the output filter capacitor. A low ESR capacitor is preferred to reduce the output voltage ripple caused by the pulsing current, which will make the sampling point more precise.

G. Design the RCD Snubber

The energy stored in the leakage inductor can not be transferred to the secondary side in the Flyback converter when switch turns off. And the energy may result in a high voltage spike across the primary side switch, which may destroy the MOSFET if the spike is not damped. So, the voltage spikes should be suppressed to an acceptable level to protect the switch.
The RCD snubber is usually adopted to clamp the drain voltage. The RCD clamp circuit and its key steady state waveforms are shown in the Figure-11 and Figure-12 respectively. The energy stored in the parasitic inductor must be dissipated by the RC network during each cycle and the value of the capacitor C_{sn} and resistor R_{sn} sets the clamp voltage V_{sn}.

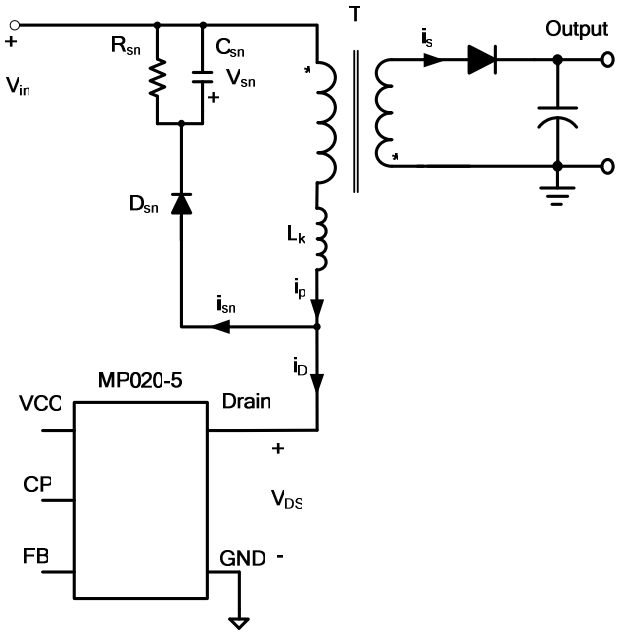


Figure 11- The RCD Clamp Circuit

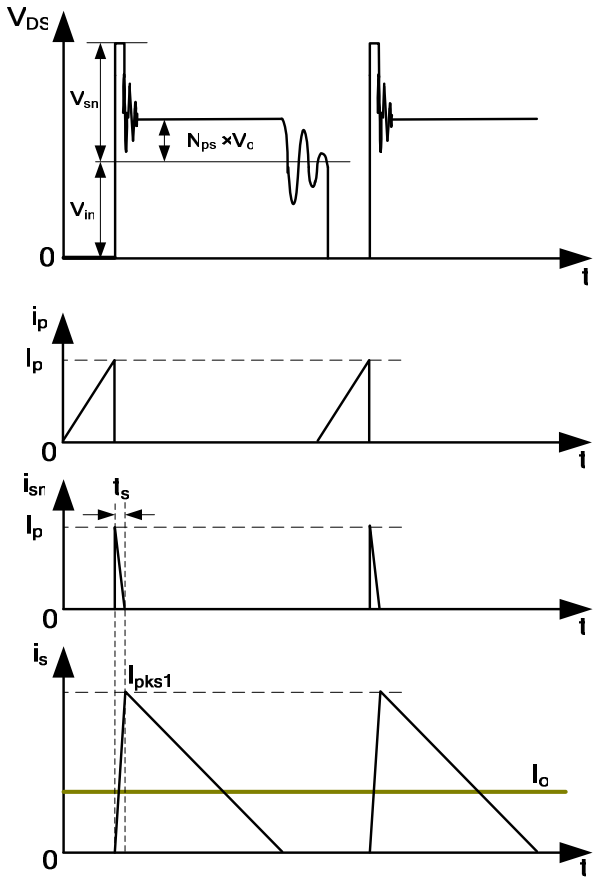


Figure 12- Waveforms

The energy stored in the leak indcutor is expressed as follow:

$$P_{sn} = \frac{1}{2} \cdot L_k \cdot I_{pk}^{\ 2} \cdot f_s \tag{47}$$

Where L_k is the primary side referred leakage inductance and the I_{pk} is the peak current in the primary side.

The RCD snubber circuit absorbs the energy in the leakage inductor when the V_{ds} exceeds $V_{in}+V_{sn}$. It is assumed that the snubber capacitor is large enough thus its voltage keeps constant during a switching period.

When the MOSFET turns off and V_{ds} is charged to $V_{in}+N_{ps}\times V_o$, the secondary diode turns on at the same time. The primary current continues to flow through the snubber diode (D_{sn}) to C_{sn}. The voltage stress of MOSFET is clamped to Vin+Vsn. Therefore, the voltage across L_k is V_{sn}- $N_{ps}\times V_o$. The slope of i_{sn} is given by equation (48).

$$\frac{di_{sn}}{dt} = -\left(\frac{V_{sn} - N_{ps} \times V_o}{L_k}\right) \tag{48}$$

Where i_{sn} is the current flows into the snubber circuit, V_{sn} is the voltage across the snubber capacitor C_{sn}. The transition time ts is obtained by following equation:

$$t_s = \frac{L_k}{V_{sn} - N_{ps} \times V_o} \times I_{pk} \tag{49}$$

Typically, we can assume an acceptable clamp voltage V_{sn} which is usually 50%~100% higher than the reflected output voltage $N_{ps} \times V_o$. So, the power dissipated in the snubber circuit is obtained by equation (50)

$$P_{sn} = V_{sn} \cdot \frac{I_{pk} \cdot t_s}{2} \cdot f_s = \frac{1}{2} \cdot L_k \cdot I_{pk}^2 \cdot \frac{V_{sn}}{V_{sn} - N_{ps} \times V_o} \times f_s \quad (50)$$

On the other hand, since the power consumed in the snubber resistor is V_{sn}^2 / R_{sn} , the resistance is calculated as:

$$R_{sn} = \frac{V_{sn}^2}{\frac{1}{2} \cdot L_k \cdot I_{pk}^2 \cdot \frac{V_{sn}}{V_{sn} - N_{ps} \times V_o} \cdot f_s} \quad (51)$$

The maximum ripple of the snubber capacitor voltage is obtained as follow:

$$\Delta V_{sn} = \frac{V_{sn}}{C_{sn} \cdot R_{sn} \cdot f_s} \quad (52)$$

Generally, 15% ripple is reasonable.
Normally, it's recommended the time constant $\tau = R_{sn} \times C_{sn}$ is less than 0.1ms for better CV sampling So, the resistor can be adjusted based on the power loss and the acceptable clamp voltage in practical application.

H. Design the Output Filters

The RMS current of the output capacitor can be obtained as:

$$I_{cap} = \sqrt{I_{s\_rms}^2 - I_o^2} \quad (53)$$

Where I_{s_rms} is the secondary RMS current.
The RMS current should be smaller than the RMS current specification of the capacitor.
The voltage ripple on the output cap can be estimate by:

$$\Delta V_{ripple} = \frac{I_o \cdot (T_{p\_on} + T_w)}{C_{out}} + (I_{pks} - I_o) \cdot R_{ESR} \quad (54)$$

Where I_{pks} is the secondary side peak current; R_{ESR} is the ESR of the output capacitor; C_{out} is the output filter capacitor.
In practical application, we should choose the output filter capacitor with sufficiently low ESR to meet the output voltage ripple requirement without adding an extra LC post filter. Another advantage by using the low ESR capacitor is more precise for the output voltage sampling at auxiliary winding.

Sometimes it is impossible to meet the ripple specification with a single electrolytic capacitor due to the high ESR and the parasitic inductance. Then, additional extra ceramic capacitor paralleled with the electrolytic capacitor or LCL filter can be used to provide a low impendence current path for high frequency current ripple.

I. Key points for system operation

In order to better performance and system operation, several key points need to be attention.

(1), Output capacitor

It's better to use the low ESR or very low ESR output capacitor for better precision of output voltage. The ripple will be lower and the efficiency will be little higher than non-low ESR output capacitor adoption. The ESR of output capacitor lower than 100mΩ is recommended.

(2), Secondary side diode

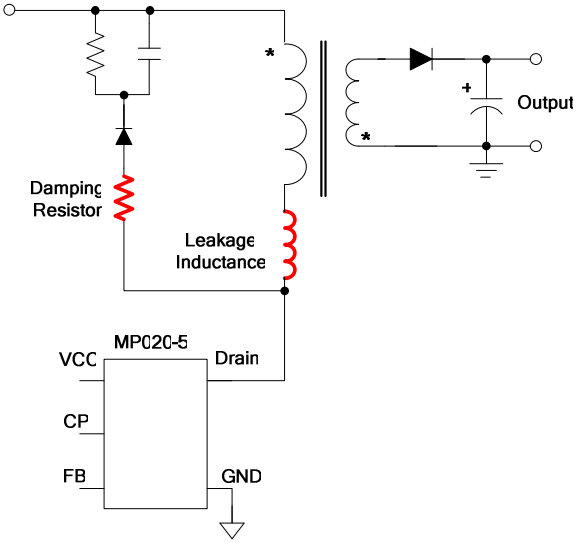
The Schottky diode will be recommended because of the fast switch rate and low forward drop for better high/low temperature CV regulation and efficiency.

(3), Leakage inductance of transformer

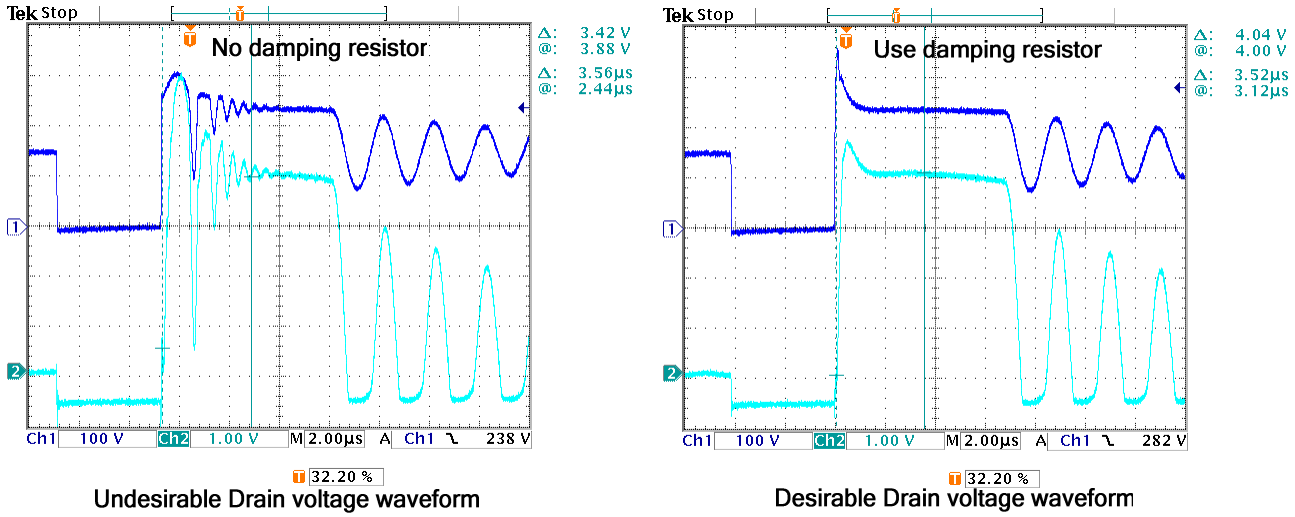
The leakage inductance of transformer should be as smaller as possible. Leakage inductance will affect the sampling point, decrease the efficiency and reduce the output current constant precision. So, optimize the transformer structure to improve the coupling of primary side and secondary side. It is better that the leakage inductance is less than 5% inductance.

(4), RCD snubber

Because of the leakage inductance of transformer always exists which will induce the drain voltage ringing, the damping resistor around 200Ω to 500Ω in series with the clamp diode is suggested to restrain the drain voltage ringing which will affect the sampling point, reduce the output voltage regulation and worsen the ripple. Figure 13 shows the compare result with the damping resistor.



(a) Schematic with Damping Resistor



(b) Waveforms Compare with the Damping Resistor
(CH1: V_{DS}; CH2: V_{FB})

Figure 13-Damping Resistor

(5), Divided resistor

The divided resistor is recommended to select from 10kΩ to 100kΩ to avoid the FB pin disturbed by noise. About 1kΩ to 2kΩ resistor can be added between the divided resistor and the FB pin usually to restrain the noise disturbance caused by layout or component usually which is shown as Figure 14.

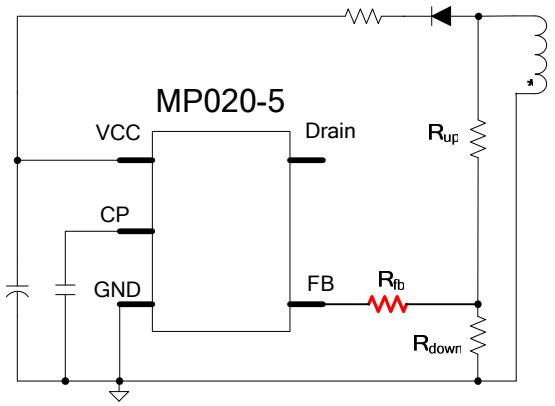


Figure 14-FB Pin in series with one resistor

(6), Maximum switching frequency

The maximum switching frequency is recommended lower than 75kHz because of the 3.5us sampling time tolerance and inductance tolerance. So considering the parameter tolerance of the chip and application in high or low temperature operation, the secondary side diode conduction time should be longer than 5.4μs normally which function can be expressed as follow.

$$T_{ons} = I_{pk} \cdot \frac{N_s \cdot L_m}{N_p \cdot (V_o + V_d)} > 5.4us \quad (54)$$

(7), Dummy load

When system operates in no load and no dummy load is used in circuit, the output voltage will rise higher than normal operation because of the minimum switching frequency limitation. One dummy load is required to use in application for good load regulation. Increasing the dummy load will deteriorate the efficiency and no load consumption, so the dummy load is tradeoff with the efficiency and load regulation. Normally, around 10mW dummy load is enough for good load regulation and it also satisfies the 30mW requirement.

4. DESIGN SUMMARY

- A detailed reference design of primary side regulator with MP020-5 and BOM are shown in Figure-15 and Table 2. The input voltage is 85Vac to265Vac and the output is 5V/1A.
- By sensing the voltage on auxiliary winding to achieve protection function. When output voltage is too high which make the voltage on auxiliary winding trigger the OVP threshold of FB pin. The auxiliary winding is used for powering the regulator and detecting the V_{ds} to ensure DCM and OCkP.
- The transformer's turns ratio is 127:18:4:4(Np:Np_au:Nsec1:Nsec2) and the primary inductance is 1.6mH. The transformer specification is shown as Figure-16.

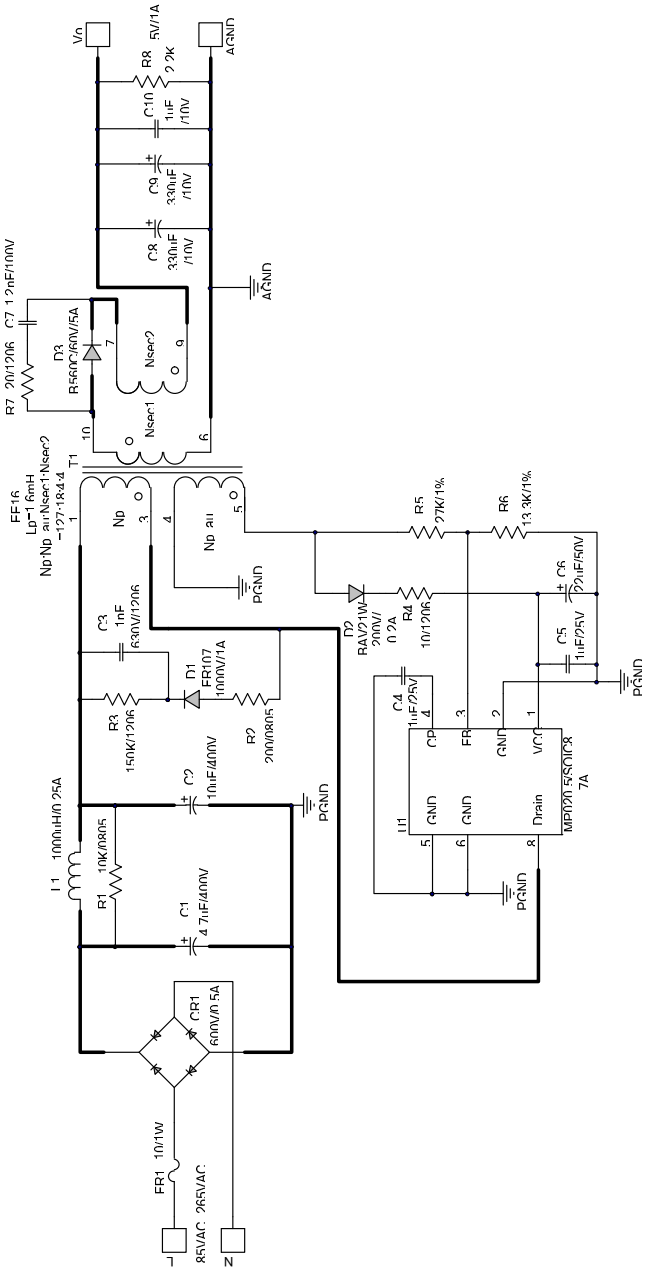
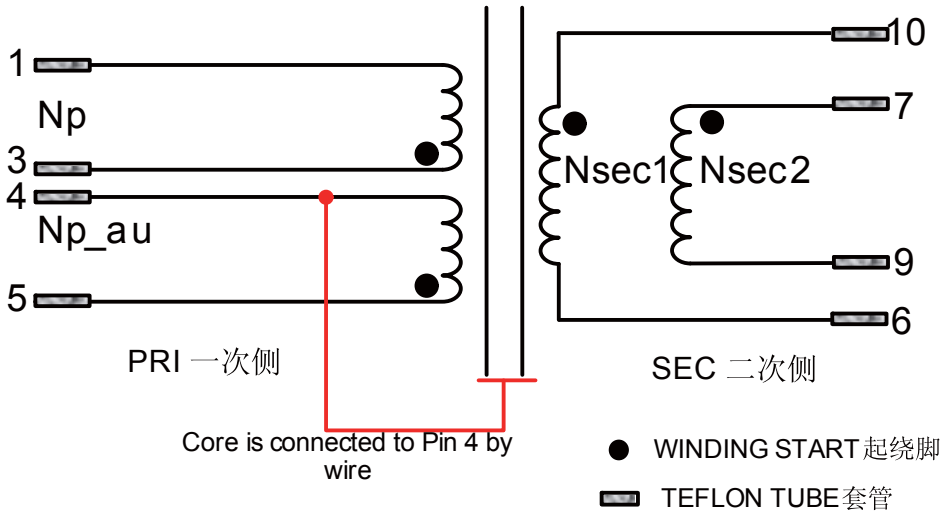


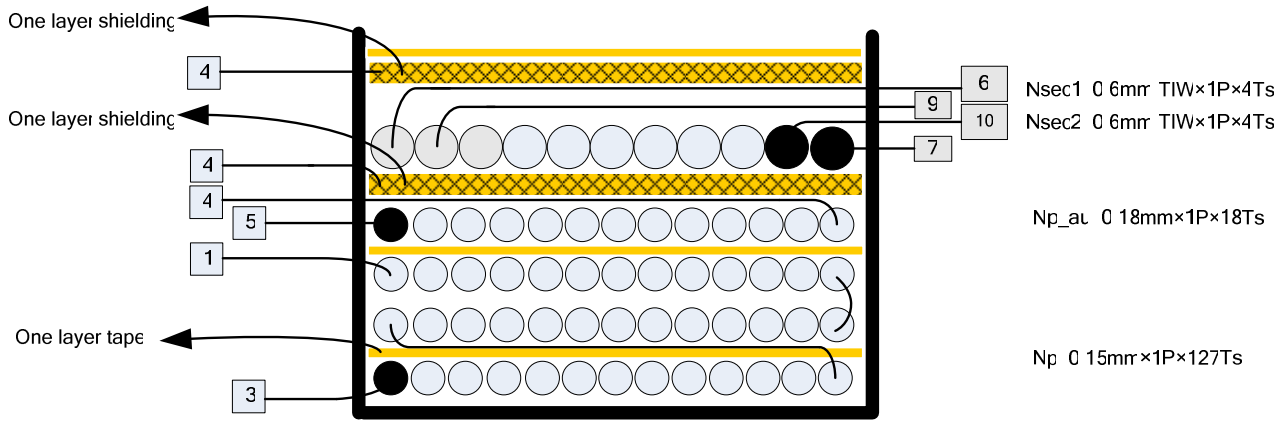
Figure15- Schematic with MP020-5

Table 2: Bill of materials

Qty	Ref	Value	Description	Manufacture	Package	Part Number
1	C1	4.7μF	Capacitor; 400V; 20%	Nichicon	DIP	UVY2G4R7MPD 10*12.5
1	C2	10μF	Capacitor; 400V; 20%	Ltec	DIP	TY Series 10*12.5
1	C3	1nF	Ceramic Capacitor; 630V; X7R	Murata	1206	GRM31A7U2J102JW31D
2	C4,C5	1μF	Ceramic Capacitor; 25V; X5R	TDK	0603	C1608X5R1E105K
1	C6	22μF	Electrolytic Capacitor; 50V;	Jianghai	DIP	CD281L-50V22
1	C7	1.2nF	Ceramic Capacitor; 100V; X7R	muRata	0603	GRM188R72A122KA01D
2	C8,C9	330μF	Electrolytic Capacitor; 10V;	Jianghai	DIP	HCN-10V330
1	C10	1μF	Ceramic Capacitor; 10V; X7R	Murata	0603	GRM188R71A105KA61D
1	CR1	MB6F	Diode; 600V; 0.5A	Diodes	SOP-4	MB6F
1	D1	FR107	Diode; 1000V; 1A	Diodes	DO-41	FR107
1	D2	BAV21W	Diode; 200V; 0.2A;	Diodes	SOD-123	BAV21W-7-F
1	D3	B560C	Schottky Diode; 60V; 5A;	Diodes	SMC	B560C
1	FR1	10Ω	Fusible Resistor,1W, 1%	Yageo	DIP	FKN1WSJT-52-10R
1	L1	1000uH	Inductor;1mH,6Ω,0.25A	Wurth	DIP	7447462102
1	R1	10kΩ	Film Resistor; 5%	Yageo	0805	RC0805JR-0710KL
1	R2	200Ω	Film Resistor; 5%;	Yageo	0805	RC0805JR-07200RL
1	R3	150kΩ	Film Resistor; 5%;	Yageo	1206	RC1206JR-07150KL
1	R4	10Ω	Film Resistor; 5%;	Yageo	1206	RC1206JR-0710RL
1	R5	27kΩ	Film Resistor; 1%;	Yageo	0603	RC0603FR-0727KL
1	R6	13.3kΩ	Film Resistor; 1%	Yageo	0603	RC0603FR-0713K3L
1	R7	20Ω	Film Resistor; 5%;	Yageo	1206	RC1206JR-0720RL
1	R8	2.2kΩ	Film Resistor; 5%;	Yageo	0603	RC0603JR-072K2L
1	T1		Transformer;1.6mH; Np:Np_au:Nsec1:Nsec2 =127:18:4:4		EE16	
1	U1		Primary side regulator	MPS	SOIC8-7A	MP020-5



(a) Electrical Diagram



(b) Winding Diagram

Figure 16- Transformer Specification

5. EXPERIMENTAL VERIFICATION

A prototype of primary side control adopting MP020-5 with the parameters given above has been built and tested (Input:85Vac~265Vac; Output:5V/1A). All the components in the circuit are as the same as that shown in Figure-15.

The operation waveforms are described as follows.

Figure 17 shows the startup waveform. When the V_{CC} is charged to about 17.3V by internal high voltage current source, the converter starts to work.

Figure 18 shows the output voltage sampling signal. The sampling point is about 4V during sampling time after the switch turns off.

Figure 19 shows the OVP function of MP020-5. When the FB pin senses the voltage higher than 6.35V, the MP020-5 will immediately shuts off the internal driving signals logic block and enter hiccup mode and it returns to normal operation when the fault has been removed.

Figure 20 shows the dynamic response with V_{OUT} is monitored at the end of board and it can meet the requirement of “USB Battery Charging 1.2 Compliance Plan”.

Figure 21 shows the CV/CC characteristic. From the curve, it can achieve accurate voltage regulation with error about +/- 5%. And it also has tight output current regulation with error +/-5%.

Figure 22 shows the measured efficiency. The average efficiency is about 76.56% with 230Vac input, 75.16% with 115Vac input.

Table 3 shows the no load power consumption and it is less than 30mW.

Figure 23 shows the test result of audible noise with the board enclosed into case and the noise probe keep 5cm distance to the case. Normally, human ear is insensitive with audible noise below 25dB.

Figure 24 shows the conducted EMI with the output connected to ground.

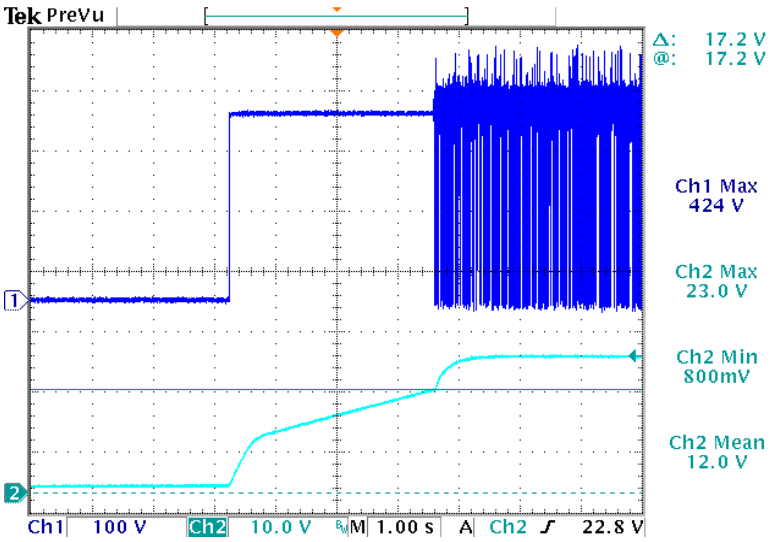


Figure 17- Startup Waveform (220Vac)

(CH1: V_{DS}; CH2: V_{CC})

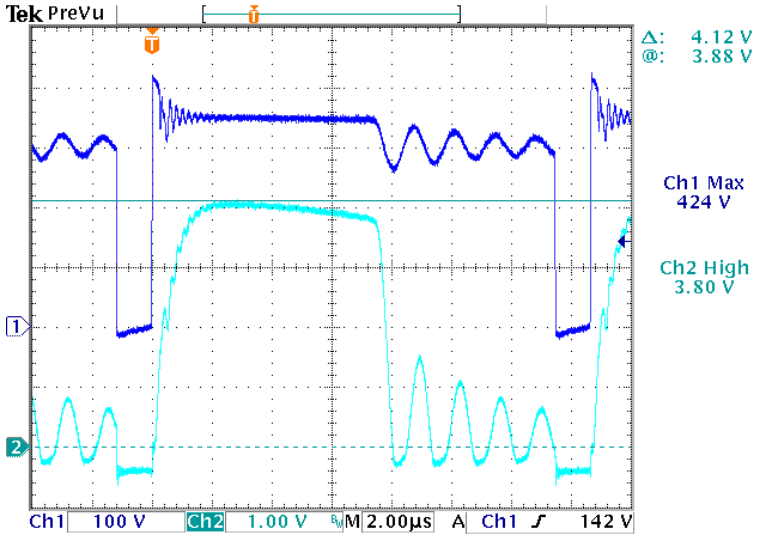


Figure 18- Switch Drain-Source Voltage and FB pin Sampling Signal (220Vac)

(CH1:V_{DS}; CH2:V_{FB})

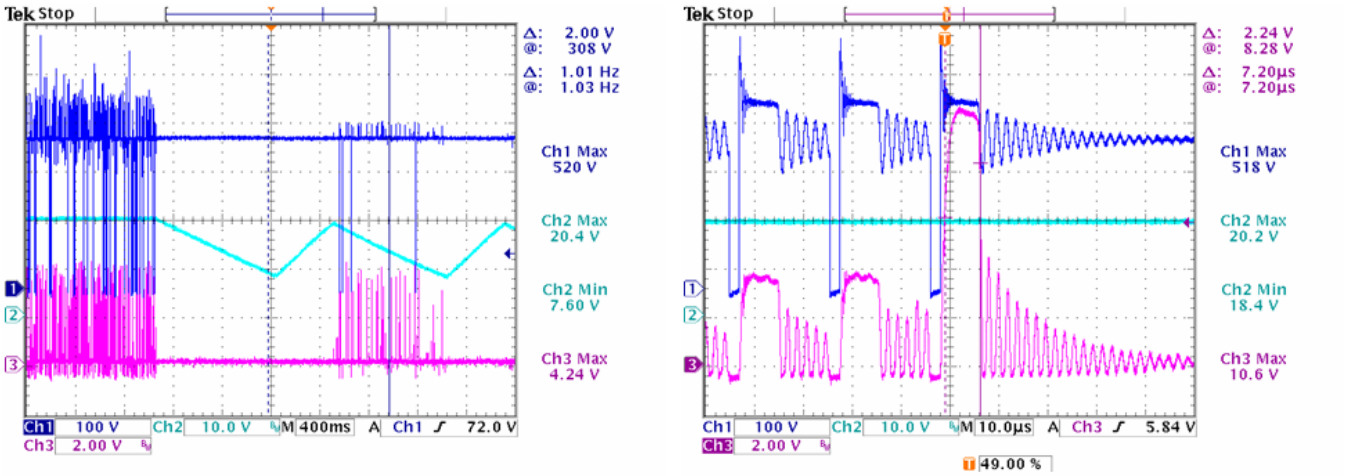
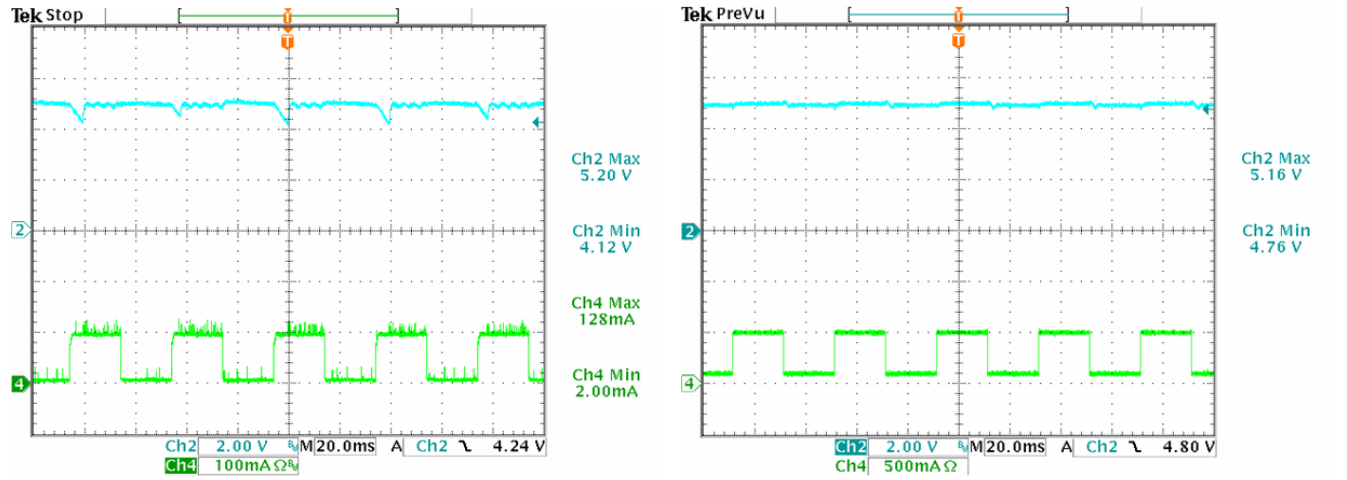


Figure 19- OVP Function (220Vac)

(CH1: V_{DS}; CH2: V_{CC}; CH3: V_{FB})



(a) I_{OUT}: 0A~0.1A **(b) I_{OUT}: 0.1A~0.5A**

Figure 20- Load Response

Frequency: 25Hz; Duty-cycle: 50%; Slew rate: 0.1A/µs

(CH2: V_{OUT}; CH4: I_{OUT})

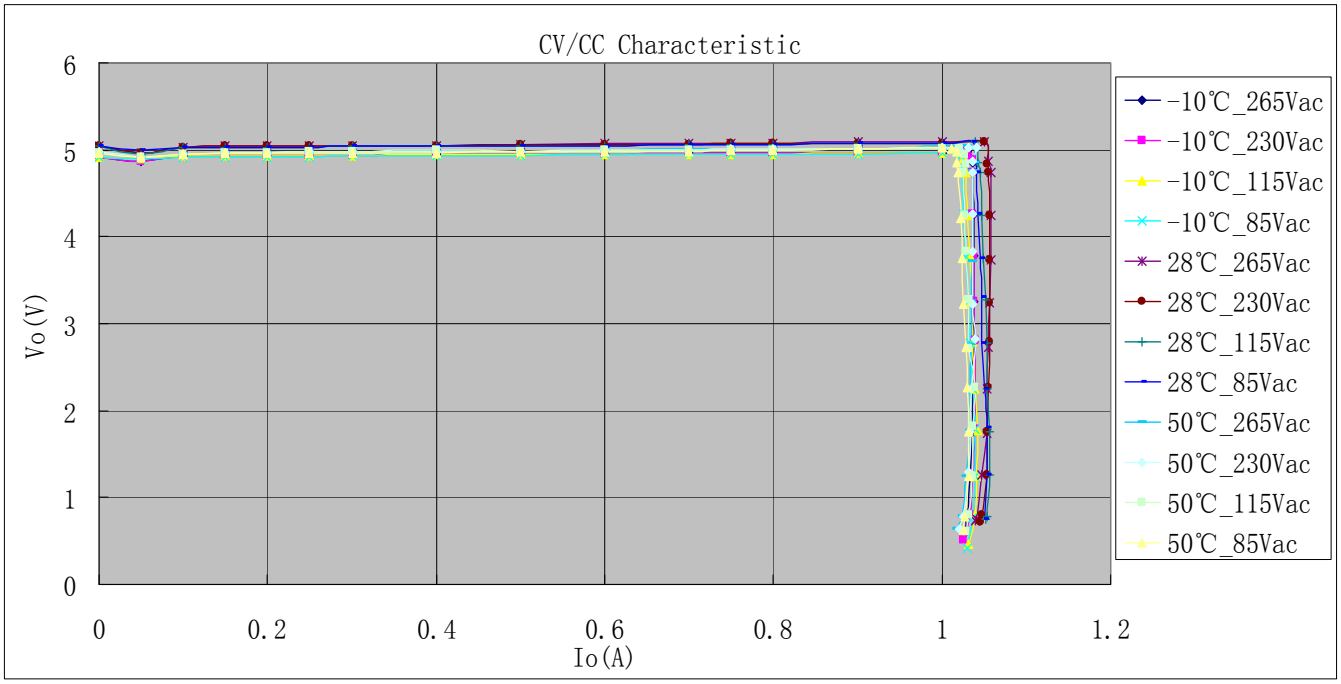


Figure 21- CV/CC Characteristic

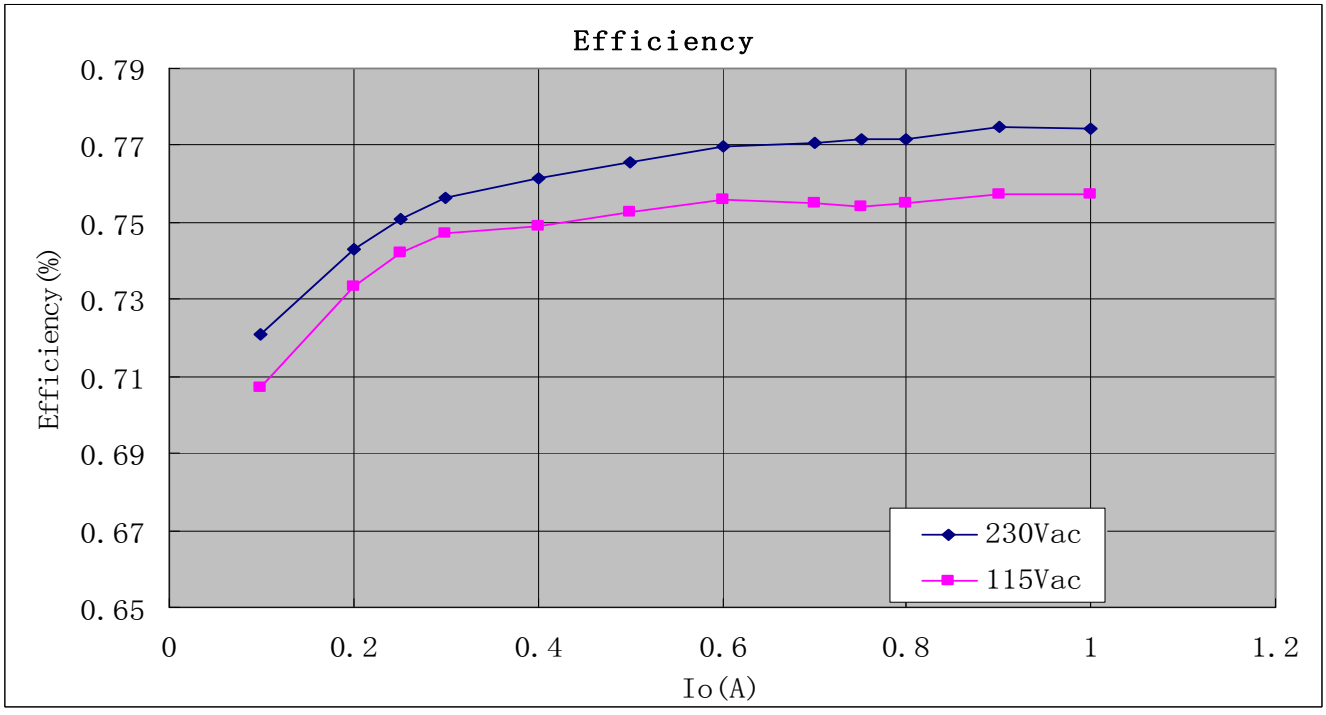


Figure 22- Efficiency of the system

Table 3: No Load Power Consumption

Input Voltage (Vac)	85	115	220	265
Input Power (mW)	21.53	22.4	23.81	26.51

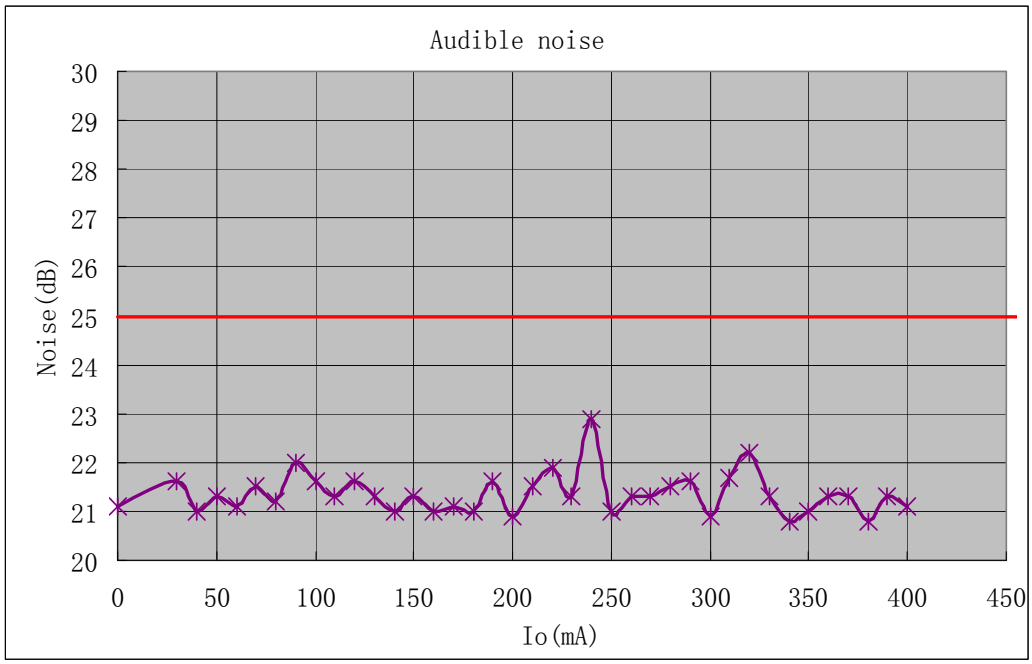
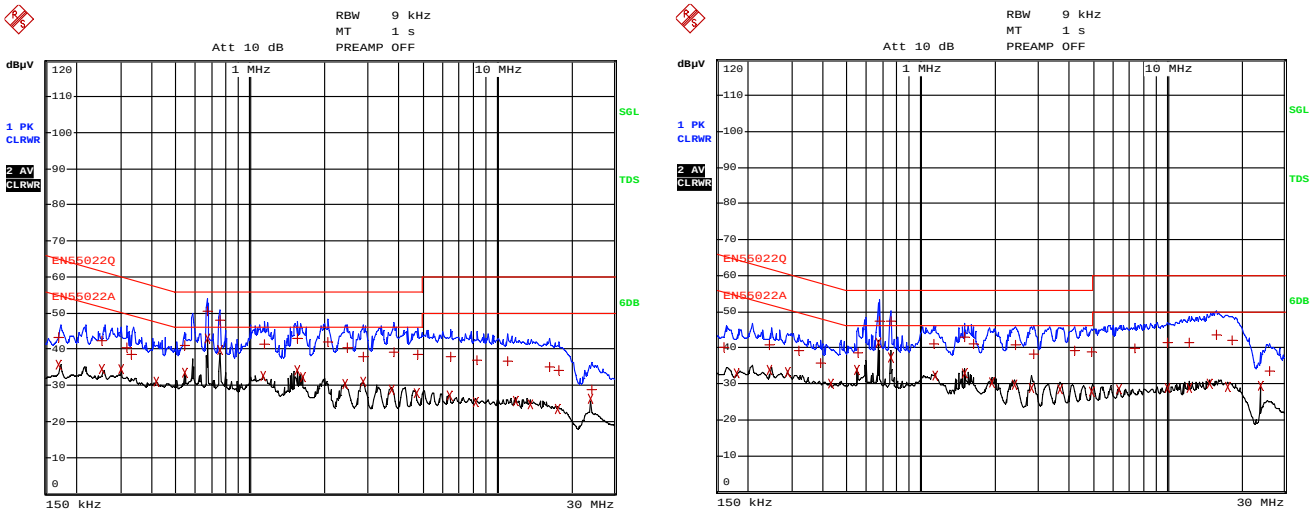


Figure 23- Audible Noise

(5cm distance and enclosed into case)



(a) Live wire **(b) Neutral wire**

Figure 24- Conducted EMI

(output connected to ground)

6. REFERENCES:

[1],Lloyd H. Dixon, “Magnetics Design for Switching Power Supplies”, in Unitrode Magnetics Design Handbook, 1990.