COT Buck Loop Bandwidth and Load Step Response Comparison

Application Note

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INTRODUCTION

Oftentimes, some design engineers request a Bode plot of a constant-on-time (COT) buck converter to gauge its loop response and stability. This is because Bode plots are readily available for peak current mode (PCM) controlled buck converters, typically. Bode plots can be taken on COT buck converters using the same measurement technique and equipment as with the PCM buck. The question is, does the COT buck bode plot truly represent the loop response of the converter?

The purpose of this application note is to determine if the Bode plot of the COT buck converter can be used to determine the loop response of the converter or whether a load step response is a better way to estimate it.

Before we look into this, it is beneficial to review the differences among the voltage mode, peak current mode, and COT mode controlled buck converters.

1. VOLTAGE MODE, PEAK CURRENT MODE, AND COT CONTROL COMPARISON

The control circuit of a DC/DC converter monitors the output/input voltages and FET/inductor current to regulate the output voltage against load and input voltage changes. There are three main types of control schemes for DC/DC converters: voltage mode, current mode, and constant-on-time (COT).

1.1 Voltage Mode Control

Figure 1 shows the diagram of a buck converter using voltage mode control where the output voltage feedback is compared to the reference voltage.

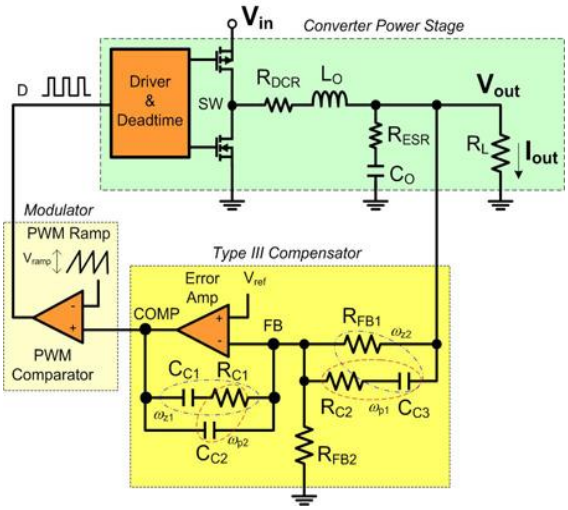


Figure 1: Voltage Mode Control

The error or difference between the two input voltages to the error amplifier (EA) is amplified at the output. This output is then compared to a ramp voltage by the PWM comparator. The higher the EA output voltage, the higher the duty cycle (D) of the high-side switch. The higher the duty cycle of the high-side switch, the higher the output voltage, and vice versa. The main drawback of voltage mode control is its slow transient response due to delays added by the Type III compensation around the EA. There can also be a zero formed by the ESR and the capacitance of the output capacitor (C_O). Type III compensation is required to counteract the second order pole formed by the output LC filter and the

zero. Another drawback with voltage mode control is that the converter must wait until the next clock cycle before it can react to changes on the feedback voltage.

1.2 Peak Current Mode Control (PCM)

Figure 2 shows the diagram of a buck converter using current mode control where the feedback voltage is also compared to the reference voltage.

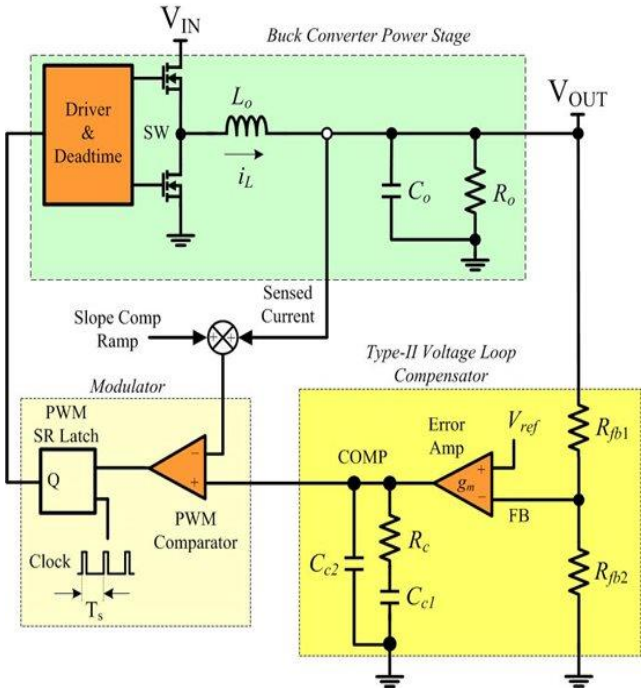


Figure 2: Peak current Mode Control

The error or difference between the two input voltages to the EA is also amplified at the EA output, whose output is used as the reference for the PWM comparator. The on cycle of the high-side switch is initiated by the clock and is terminated when the sensed inductor current reaches the EA output. Essentially, the EA output sets the peak current level for the inductor current. The higher the EA output voltage, the higher the duty cycle (D), and therefore, the higher the peak current of the high-side switch. The higher the duty cycle, the higher the output voltage and vice versa.

Since the peak current through the inductor is now set by the EA output, one can assume the inductor as a current source. Since the inductor acts as a current source, the output stage is now a single-order system formed by the output capacitor (C_O) and the load (R_O). There can also be a zero formed by the ESR and the capacitance of the output capacitor (C_O). Only Type II compensation is required to counteract the first order pole formed by the output capacitor (C_O), load (R_O), and the ESR zero. This single-order power stage and Type II compensation can push the PCM loop bandwidth higher than that in voltage mode, which makes its transient response faster than the voltage mode converter.

1.3 Constant On-Time Control (COT)

Figure 3 shows a diagram of a buck converter using COT control where the feedback voltage is compared to the reference voltage at the PWM comparator directly.

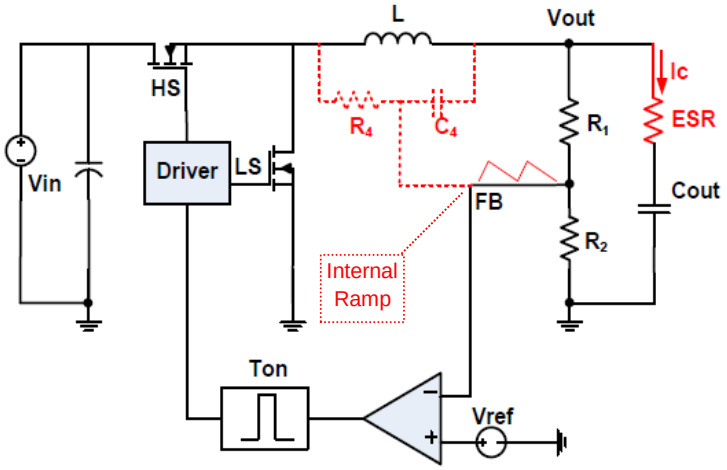


Figure 3: COT Control

COT requires a small ramp injected into its feedback node to work. This ramp signal has the same shape and phase as the inductor current ripple. There are three ways to add this ramp:

1. Using the ESR of the output filter.
2. Using the R-C network across the inductor.
3. Creating and feeding an internal ramp into the FB node.

The on-time of the high side switch is fixed at a given input and output voltage. Once the on-time expires, the high-side switch is turned off, and the low-side switch is turned on. There is a small dead time between the on cycles of the switches to prevent a shoot-through current. When the low-side switch is on, the inductor current free-wheels through the output and the low-side switch, causing the inductor current to ramp down. The AC component of the inductor current (ΔI_L) is shunted to ground by the output capacitor. If the capacitor has an equivalent series resistance (ESR), the output voltage ripple is the composite of Equation (1):

$$\Delta IL * ESR + \Delta IL/(2 * \pi * Fsw * Co) \quad (1)$$

Where ΔI_L is the inductor ripple current, Fsw is the switching frequency, and C_O is the output capacitor (See Figure 4).

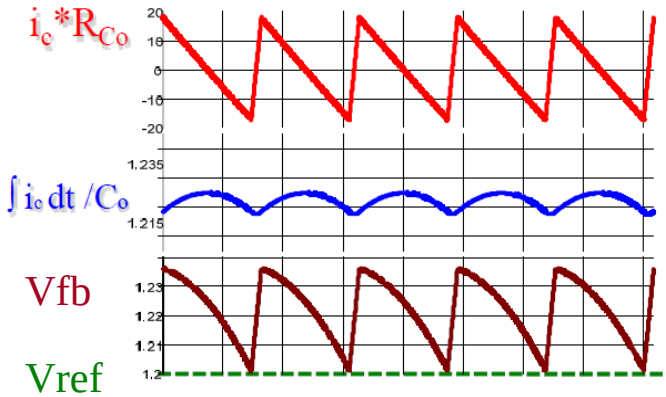


Figure 4: Buck Output Voltage Ripple

When the feedback voltage crosses the reference voltage, the low-side switch is turned off, the high-side switch is turned on again, and the cycle repeats.

Whenever the feedback voltage crosses the reference voltage, the converter initiates another on (constant) cycle. Therefore, when there is a step load, the rising edge of the load current is drawn from the output capacitor, causing the output voltage to dip. The feedback voltage immediately dips as well, initiating one or more on cycles until the valley of the feedback voltage is equal to the reference voltage. This makes the COT transient response faster than that in voltage mode or peak current mode control since the delays imposed by the compensators around the EA and clock are eliminated. The effective loop bandwidth of a COT converter is higher than can be achieved with either voltage mode or current mode control (see Table 1).

Table 1: Summary of Voltage Mode, Peak Current Mode, and COT control Advantages and Disadvantages

	Voltage Mode	Peak Current Mode	COT Control
Advantages	• Works with a wide range of duty cycles. • Stable PWM modulation – less sensitive to noise.	• Power stage is a single pole and single zero within the frequencies of interest. The other pole exists at a much higher frequency. • Simpler EA compensation and faster transient response. • Line rejection. • Cycle-by-cycle current limiting.	• No EA compensation. • Very fast load transient response – faster than current mode. • Fixed switching frequency with input feed-forward on on-time at constant load. The switching frequency varies a little – not fixed like voltage mode. • High efficiency at light load efficiency with pulse-skip mode.
Disadvantages	• Complex EA compensation due to LC double pole. • Slow response to input voltage changes. • Current limiting must be done separately. • Slow transient response.	• Sensitive to noise. • Minimum on-time limitation. • Sub-harmonic oscillation without current slope compensation.	• On-time jitter with inadequate ramp compensation. • Ramp compensation required with very low ESR output caps, such as ceramic. • Ramp compensation amplitude affects DC regulation. • Vfb and Vref are sensitive to noise.

2. PEAK-CURRENT MODE AND COT BODE PLOTS

2.1 Peak-Current Mode Control Bode Plot

Bode plots show loop bandwidth, gain, and phase responses of a system over a frequency range. To measure the Bode plot of voltage mode and current mode buck converters, a floating AC source with a small amplitude is injected in the loop often at the top feedback resistor. The network analyzer sweeps the frequency of the floating AC source, and the ratio of the output and input of the AC source is plotted in terms of its gain (dB) and phase (degrees). As an example, Figure 5 shows an application circuit of

the MP1497S, a 16V, 3A, peak-current mode control synchronous buck converter in a TSOT23 package.

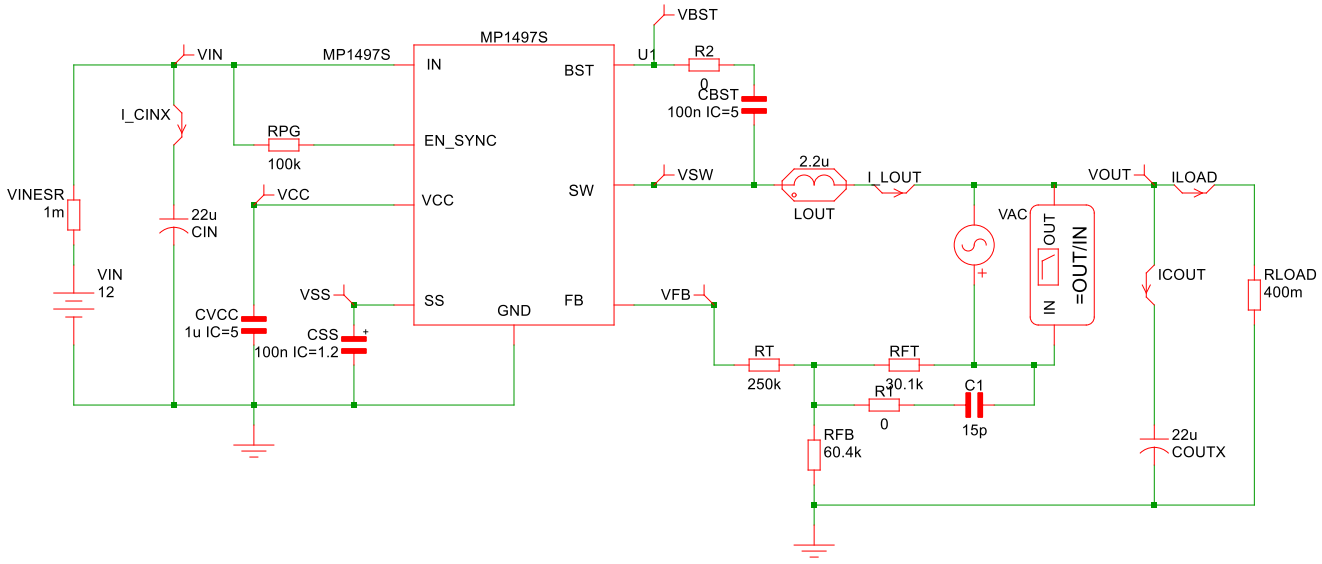


Figure 5: MP1497S Application Circuit for AC Analysis

The Bode plot shown in Figure 6 was taken from an evaluation board for the MP1497S with the same circuit. The test conditions were Vin = 12V, Vout = 1.2V, Iout = 3A, Fsw = 500kHz, L = 2.2µH, and Cout = 22µF.

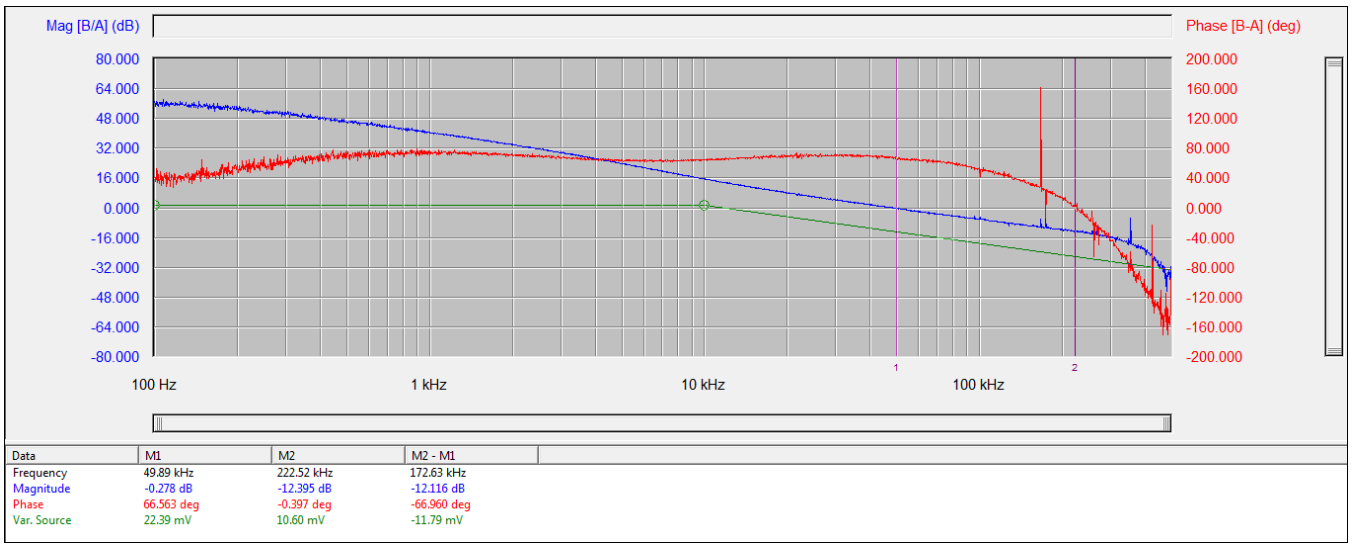


Figure 6: MP1497S Bode Plot with Adequate Gain and Phase Margins

The phase margin here is 66.5 degrees, the gain margin is -12.4dB, and the loop bandwidth is 49.9kHz. This is a stable system.

Phase margin is the phase of the system when the gain = 0dB. A typical phase margin required for a stable system is higher than 45 degrees. Gain margin is the gain of the system when the phase = 0 degrees. A typical gain margin for a stable system is lower than -10dB. Loop bandwidth is the frequency when the system gain = 0dB. The higher the bandwidth, the faster the system transient response.

To confirm stability, we can apply a step load on the output of the MP1497S and see how it responds (see Figure 7). The test conditions were Vin = 12V, Vout = 1.2V, Iout_DC = 1A, Istep = 1.5A @ 1.2A/µs, Fsw = 500kHz, L = 2.2µH, Cout = 22µF.

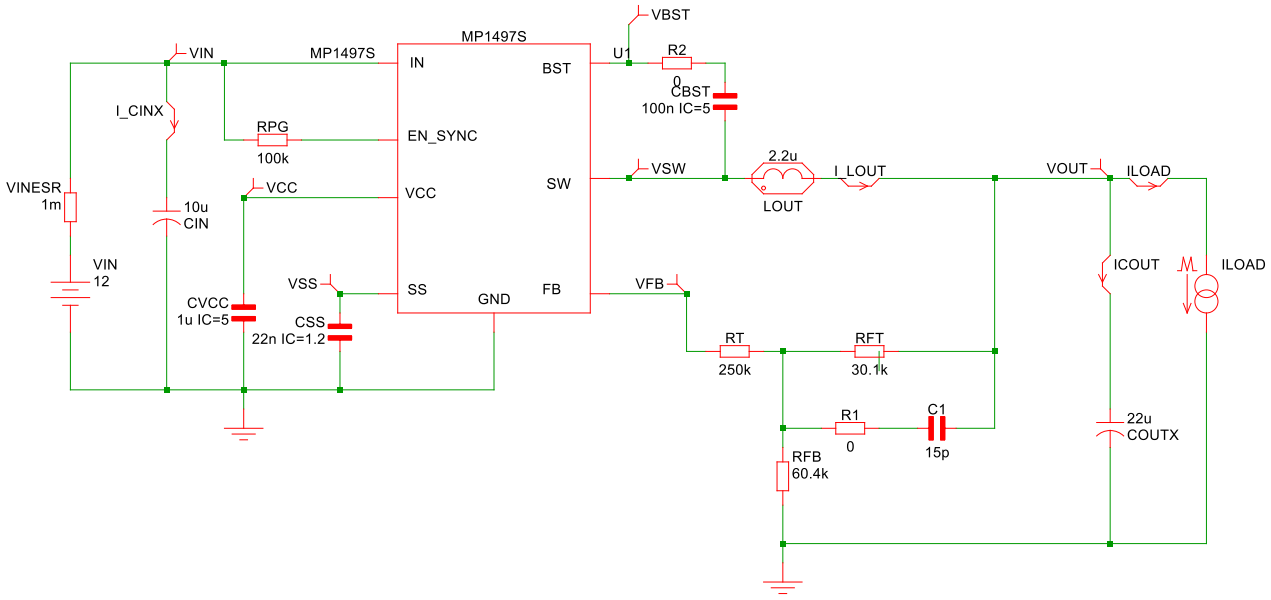


Figure 7: MP1497S Application Circuit for Transient Analysis

Figure 8 shows the measured transient response of the MP1497S.

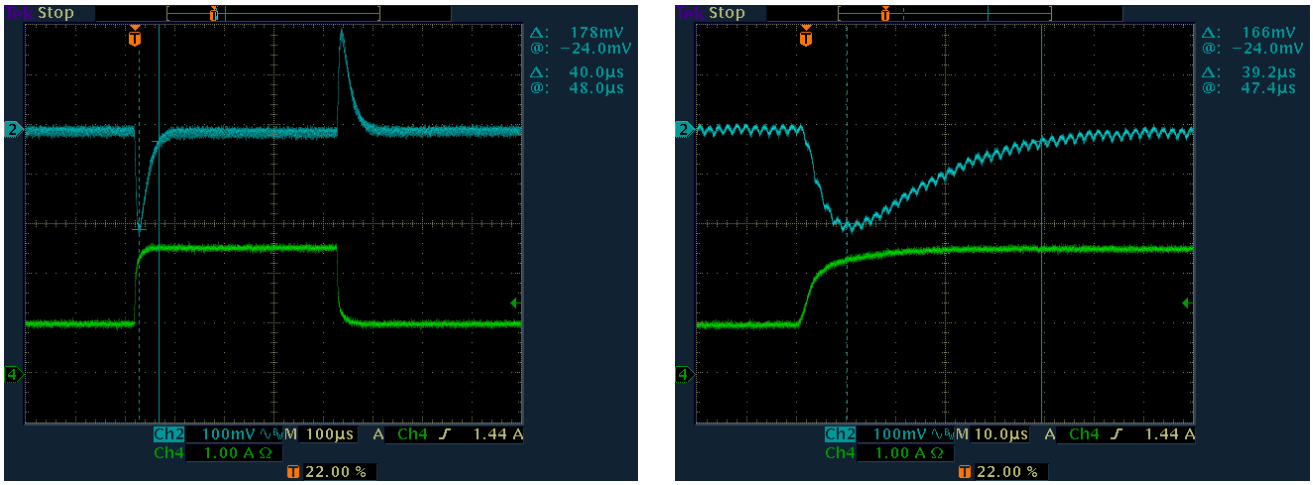


Figure 8: MP1497S Load Step Output Waveform, Ch2 = Vout, Ch4 = Iout

The MP1497S output undershoots to around 200mV below 1.2V during the low-to-high load transition (1 – 2.5A) and overshoots to around 200mV above 1.2V during the load high-to-low transition (2.5 – 1A). The converter output recovers after the undershoot and overshoot conditions within 40µs.

2.2 Comparing the MP1497S Bode Plot with Transient Response with Lower Phase Margin System

The MP1497S application circuit was slightly modified to reduce its phase margin. Reducing the phase margin causes ringing to appear on the output voltage as a response to a load step. Phase margin can be reduced by reducing resistor RT from 250kΩ to 30kΩ. Reducing RT increases the DC gain of the EA, which extends the loop bandwidth further out where the phase margin is lower. When RT is reduced, the Zi factor of the –Zf/Zi gain term of the internal EA decreases, causing its DC gain to go up. Zf is the feedback impedance of the EA, and Zi is the input impedance. Figure 9 shows a modified MP1497S circuit.

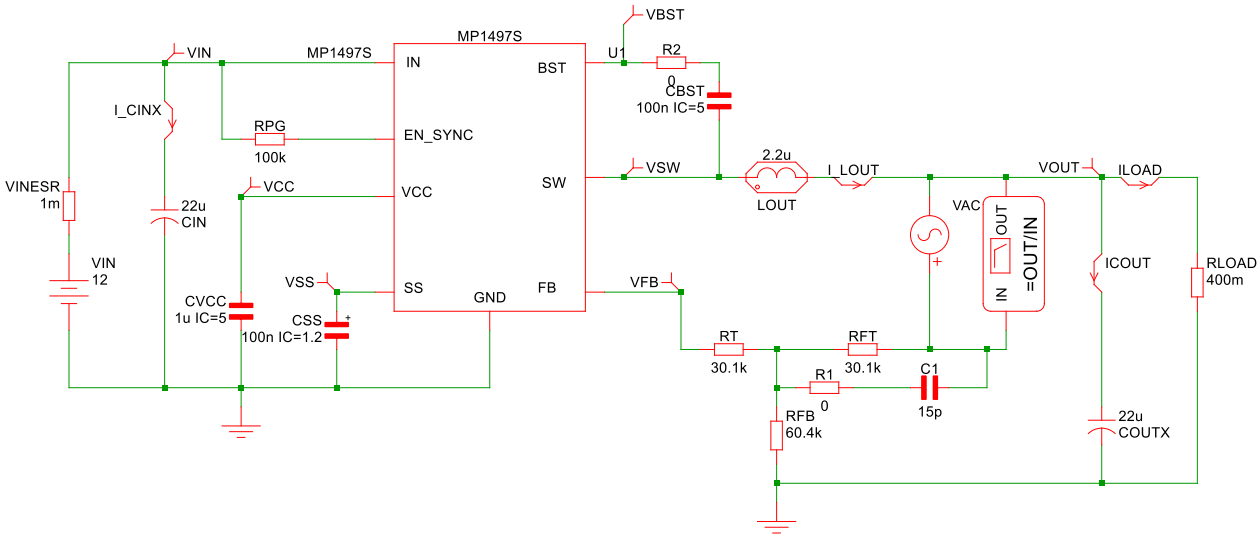


Figure 9: MP1497S Circuit with Lower Phase Margin

A Bode plot was performed with the following test conditions: Vin = 12V, Vout = 1.2V, Iout = 3A, Fsw = 500kHz, L = 2.2µH, Cout = 22µF. Figure 10 shows the MP1497S gain/phase plot with a phase margin of 27.3 degrees (previously 66.5 degrees), gain margin of -3.9dB (previously -12.4dB), and loop bandwidth of 164.7kHz (previously 49.9kHz).

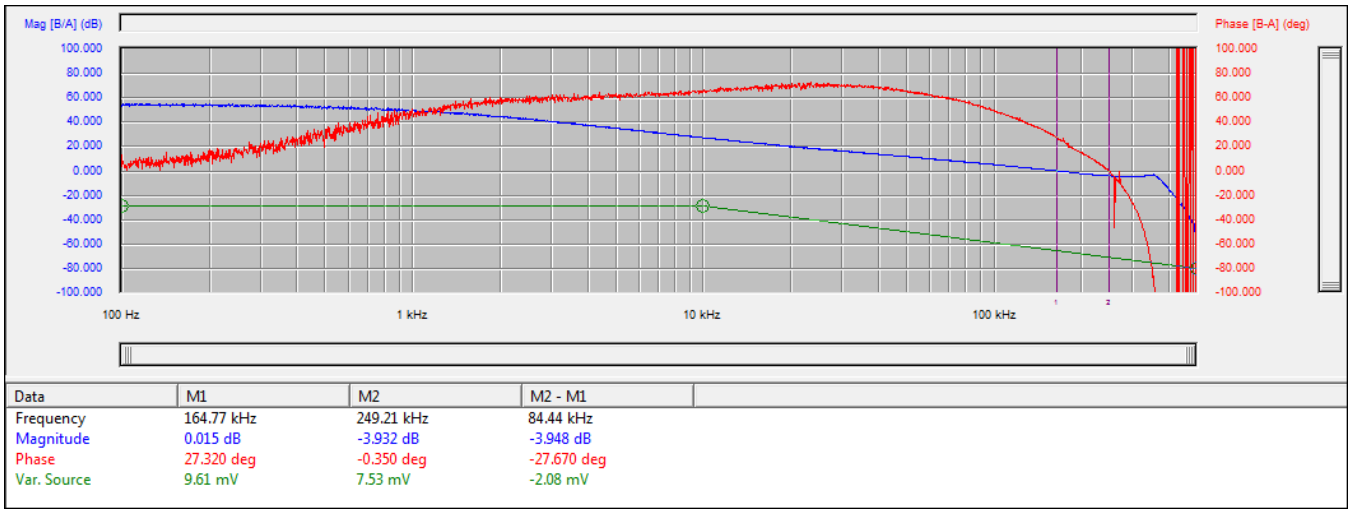


Figure 10: MP1497S Bode Plot with Low Gain and Phase Margins

Using the modified MP1497S circuit shown in Figure 11, a 1.5A step load was applied to the MP1497S output and its output response was measured. The test conditions were Vin = 12V, Vout = 1.2V, Iout_DC = 1A, Istep = 1.5A @ 1.2A/µs, Fsw = 500kHz, L = 2.2µH, Cout = 22µF.

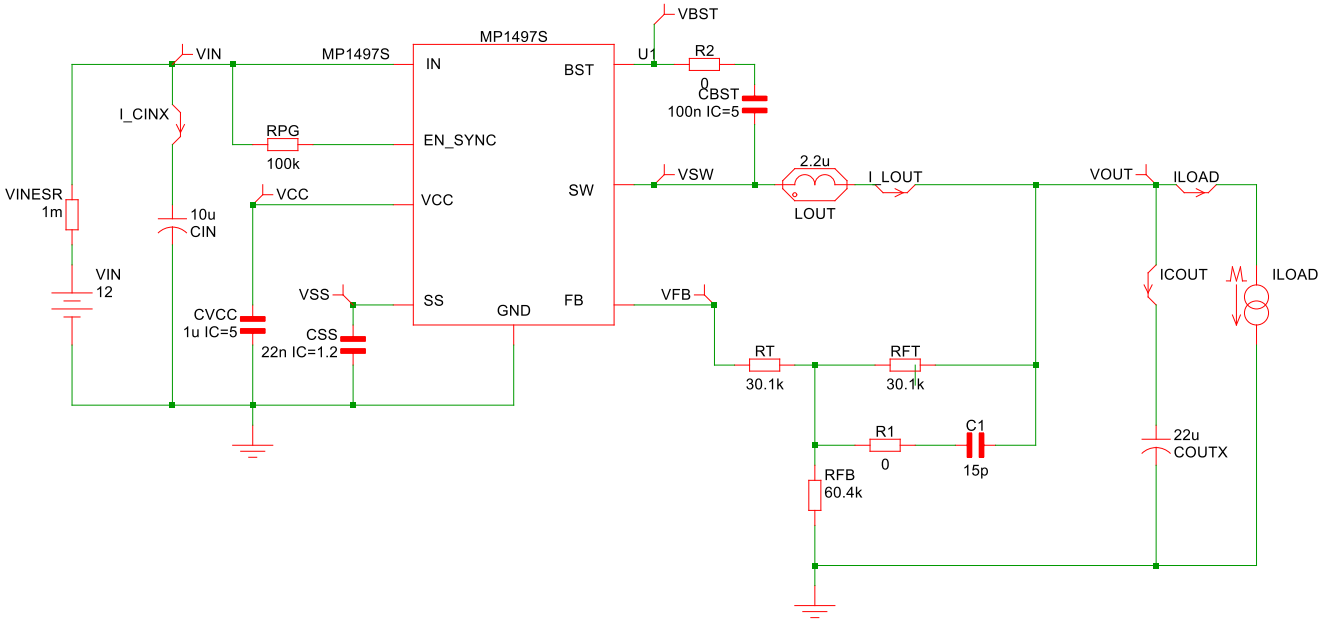


Figure 11: MP1497S Circuit for Transient Analysis with Lower Phase Margin

Figure 12 shows the measured output transient response. The ringing shows an under-damped response due to the phase margin being less than 45 degrees. The ringing period is the inverse of the loop bandwidth. For this example, the loop bandwidth was 164.7kHz (6.06µs period). The output waveform shows a ringing period of 6.0us. This is very close to the inverse of the loop bandwidth of 6.06µs, which confirms that the loop bandwidth corresponds to the output voltage transient ringing frequency.

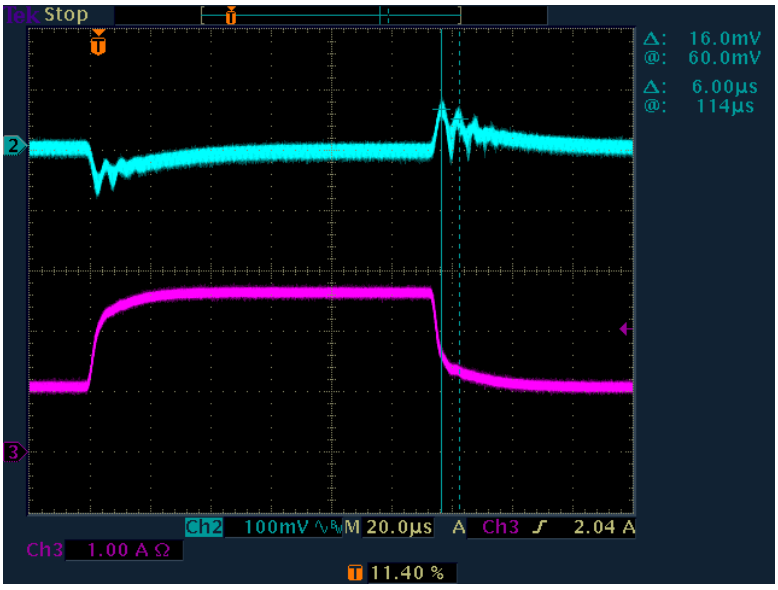


Figure 12: MP1497S Transient Response with Lower Phase Margin

2.3 COT Bode Plot

The same loop measurement technique can be used for COT buck converters where a floating AC source, with a small amplitude, is injected in series with the top feedback resistor. The network analyzer sweeps the frequency of the floating AC source, and the ratio of the output and input of the AC source is plotted in terms of its gain (dB) and phase (degrees).

Figure 13 shows a schematic diagram of the MP2316 (19V, 3A, COT, synchronous buck converter in a QFN 2x3mm package) used to measure the Bode plot.

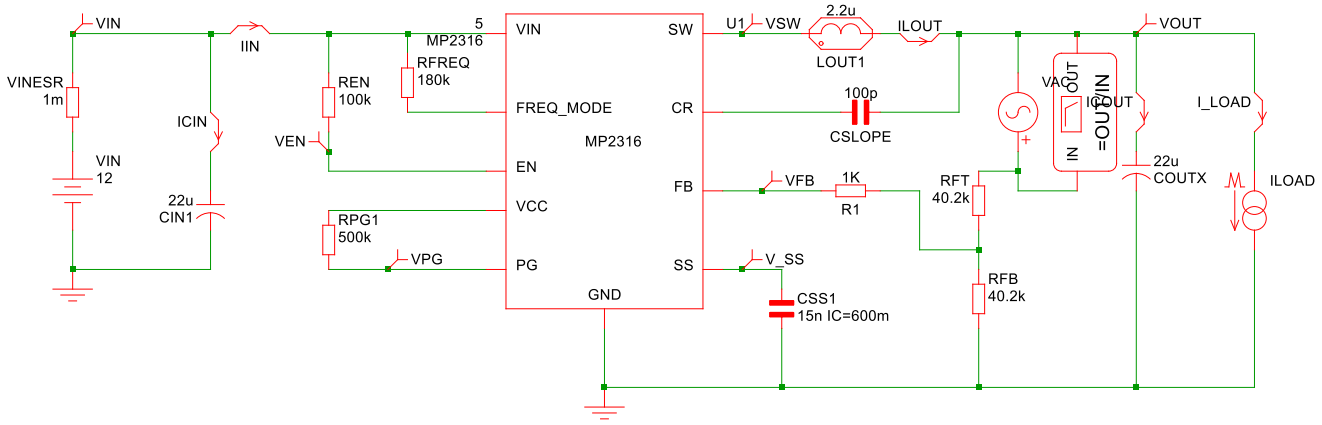


Figure 13: MP2316 Application Circuit for Measuring Bode Plot

An AC analysis was performed. Figure 14 shows the measured loop response with a phase margin of 61.5 degrees, loop bandwidth of 44.1 kHz, and gain margin of -11.7dB. The test conditions were Vin = 12V, Vout = 1.2V, Iout = 3A, Fsw = 500kHz, L = 2.2µH, Cout = 22µF.

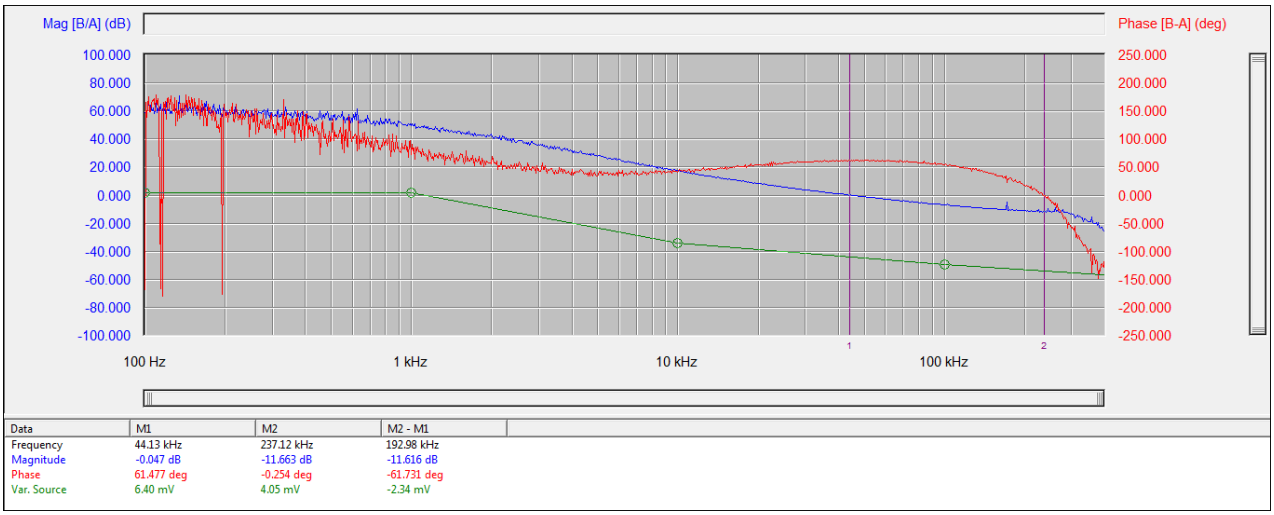


Figure 14: MP2316 Bode Plot

Figure 14 shows a stable system. However, the loop bandwidth is similar to that of the MP1497S, which is a peak current mode-controlled part. The MP2316 should have a higher loop bandwidth than the MP1497S since it is a COT-controlled part. We would expect that its phase margin information is valid since the loop response of the MP2316 is running at a nearly constant switching frequency, while the frequency of the injected AC signal is less than the converter switching frequency. For example, the

MP2316 switching frequency at continuous conduction mode (CCM) is 500kHz, and the frequency of the injected AC frequency is 44.1kHz when the loop gain is at 0dB.

One way to estimate the loop bandwidth of the MP2316 is to measure its output load step response. Refer to section 3.3 on page 18.

3. COT LOOP BANDWIDTH ESTIMATION USING LOAD STEP TEST

This section estimates the loop bandwidth of the COT buck converter using the settling time and voltage undershoot of the converter output. We will first review the relationship of quality factor and phase margin.

3.1 Explanation of Quality Factor vs. Phase Margin

This section describes the relationship of the proximity of the two poles in an open-loop system with the quality factor (Q) of the loop gain. Later sections will show the relationship of Q with the loop phase margin[1]. A typical open-loop gain of a system has a pole at the origin and another pole after the cross-over frequency, as shown in Equation (2):

$$T(s) = \frac{1}{\left(\frac{s}{w_0}\right)\left(1+\frac{s}{w_2}\right)} \quad (2)$$

The pole at the origin gives a -20dB slope as it crosses the 0dB gain. F_0 is the frequency when the gain crosses 0dB (see Figure 15).

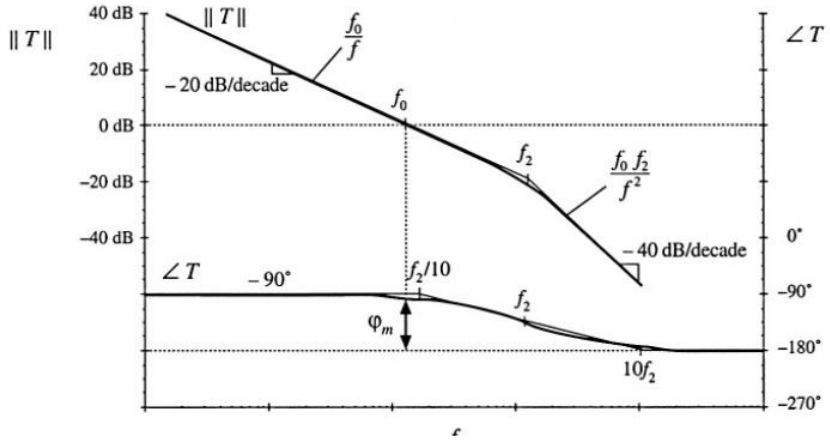


Figure 15: Gain/Phase Plot of Equation (2)

f_2 is the corner frequency of the second pole ($\omega_2/2\pi$). As f_2 approaches infinity, the phase margin approaches 90 degrees. As f_2 approaches f_0, the phase margin approaches 0 degrees. Therefore, the closer f_2 is to f_0, the smaller the phase margin.

The closed loop gain of T/(1+T) is shown in Equation (3):

[1] Erickson, Robert W. and Maksimovic Dragan, Fundamentals of Power Electronics, Second Edition, Kluwer Academic Publishers, 2001. Pages 343-345.

$$\frac{T(s)}{1+T(s)} = \frac{1}{1+\frac{1}{T(s)}} = \frac{1}{1+\frac{s}{w_0}+\frac{s^2}{w_0 w_2}} \quad (3)$$

Equation (3) can be put into the standard quadratic form shown in Equation (4):

$$\frac{T(S)}{1+T(s)} = \frac{1}{1+\frac{s}{Qw_c}+\left(\frac{s}{w_c}\right)^2} \quad (4)$$

Where Wc and Q are as shown in Equation (5) and Equation (6):

$$w_c = \sqrt{w_0 w_2} = 2\pi f_c \quad (5)$$

$$Q = \frac{w_0}{w_c} = \sqrt{\frac{w_0}{w_2}} \quad (6)$$

Q is the quality factor of a loop gain, which shows how under-damped the system is. The higher Q is, the more under-damped the system is. The lower the Q is, the more over-damped the system is.

The corner frequency (f_c) is the geometric mean of f_0 and f_2. Figure 16a shows a low Q case. Figure 16b shows a high Q case[1].

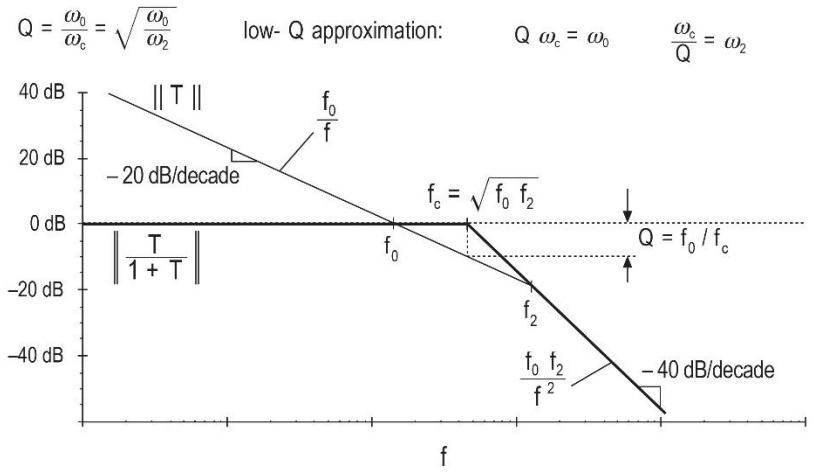


Figure 16a: Gain/Phase Plot of Equation (4) with Low Q

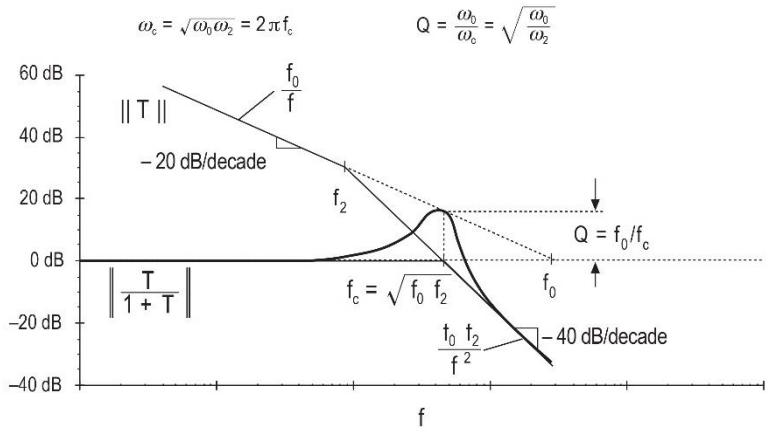


Figure 16b: Gain/Phase Plot of Equation (4) with High Q

The value of Q at $f_c = f_0/f_2$. This is true whether f_2 occurs before f_0 or much further away from f_0.

The Q factor and phase margin (ϕ_m) relationship is shown in Equation (7) and Equation (8)[1]:

$$Q = \frac{\sqrt{cos}\,\varphi_m}{\sin\varphi_m} \tag{7}$$

$$\varphi_m = tan^{-1}\sqrt{\frac{1+\sqrt{1+4Q^4}}{2Q^4}} \tag{8}$$

This relationship is plotted in Figure 17.

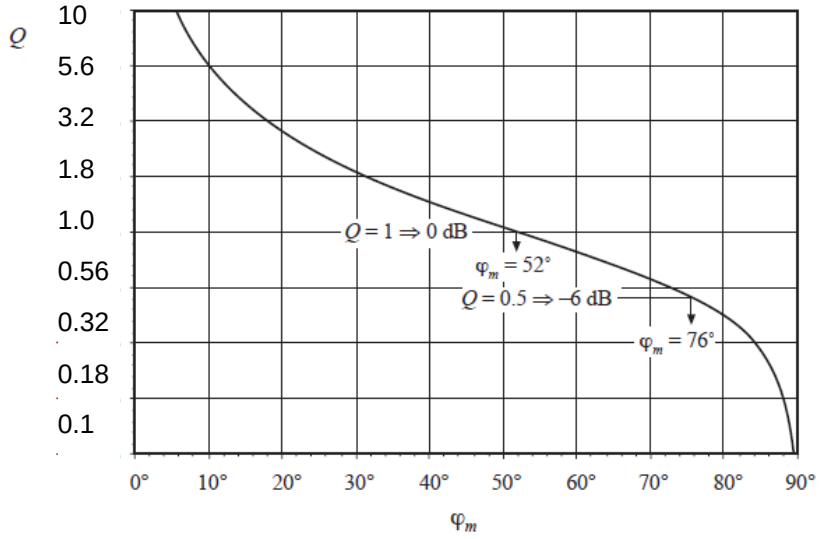


Figure 17: Phase Margin and Q Relationship

As shown in Figure 17, the higher Q is, the lower the phase margin is, and vice versa. In other words, the closer f_2 is to f_0, the higher the Q is, the lower the phase margin is, and vice versa.

3.2 Estimation of COT Loop Bandwidth Based on Measured Output Settling Time and Loop Phase Margin

We can estimate the COT buck loop bandwidth based on the settling time of the output voltage by applying a current load step.

Settling time is defined as the time required for the transient's damped oscillations to reach and stay within ±2% of the steady state output value[2]. The settling time is shown in Equation (9):

$$T_S = \frac{4}{Z\omega_a} \quad (9)$$

Where Ts is the settling time, z is the damping ratio, and ω_a is the ringing frequency or loop bandwidth. Z can be determined by Q = 1/(2z).

Figure 18 shows the plot of a second order system similar to Equation (4) with a damping ratio of 0.215.

Equation (9) can be expressed in terms of Q and f_0 by substituting z with 1/(2Q) and ω_a with $2\pi f_0$. The updated formula is shown in Equation (10):

$$Ts = 4Q/(\pi * f_0) \quad (10)$$

Substituting Q with the expression that is a function of phase margin as per Equation (11):

$$Q = \frac{\sqrt{\cos\varphi_m}}{\sin\varphi_m} \quad (11)$$

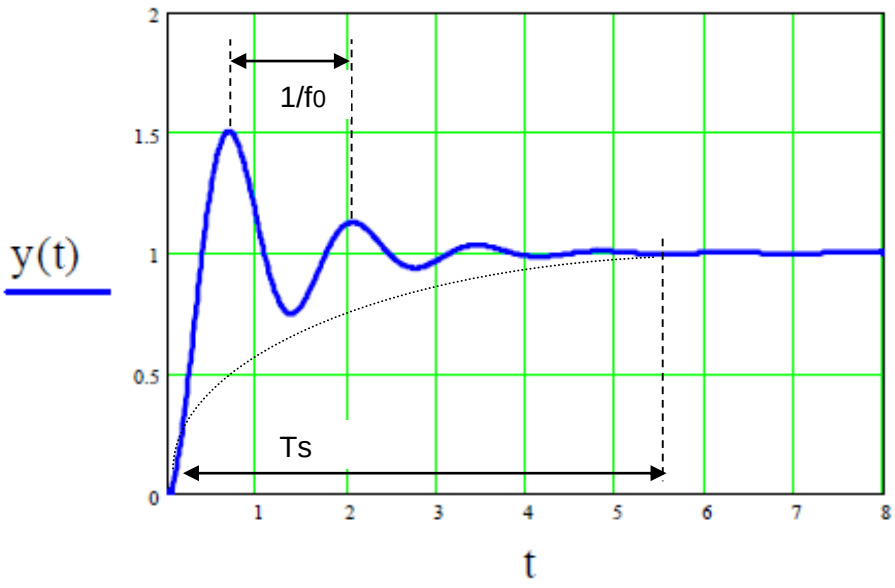


Figure 18: Plot of Second Order System Similar to Equation (4)

Ts becomes the formula shown in Equation (12):

[2] Redilla, Jack Andrew, Thesis on "A Frequency Based Approach To DC-DC Control Loop Design", Cleveland State University, 1989

$$4 * \frac{\sqrt{\cos(PM)}}{(\pi * f_0 * \sin(PM))} \tag{12}$$

Solving for f_0 yields Equation (13):

$$f_0 = 4 * \frac{\sqrt{\cos(PM)}}{(\pi * Ts * \sin(PM))} \tag{13}$$

Where f_0 is the loop bandwidth, PM is the phase margin, and Ts is the settling time. The loop bandwidth f_0 can now be estimated by using Equation (13) because both the phase margin and settling time can be measured.

The MP2316 circuit shown in Figure 19 was used to measure its transient response. A 1.5A @ 1.2A/µs load step was applied on top of the 1A DC load.

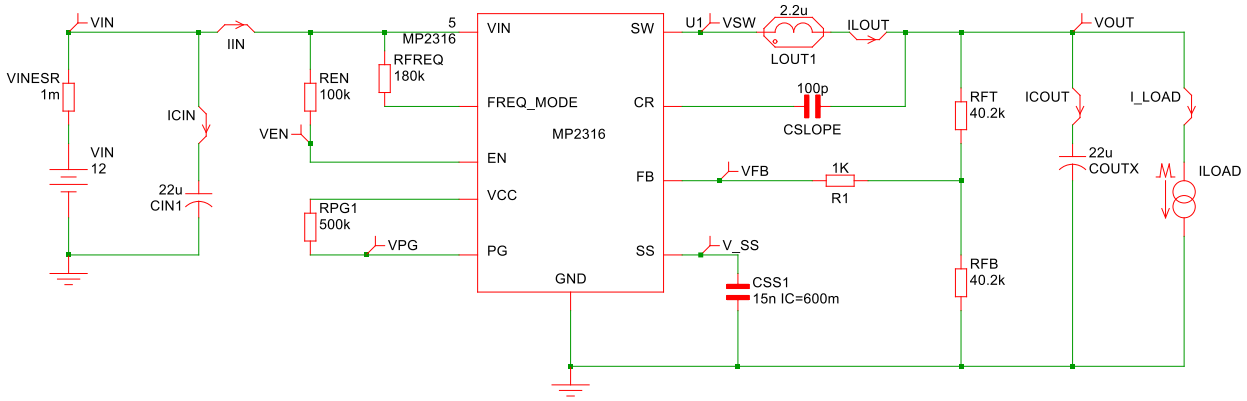


Figure 19: MP2316 Circuit for Transient Response Test

Figure 20 shows the MP2316 output waveform during a load step test with the following test conditions: Vin = 12V, Vout = 1.2V, Iout_DC = 1A, I_step = 1.5A @ 1.2A/µs, Fsw = 500kHz, L = 2.2µH, Cout = 22µF/25V.

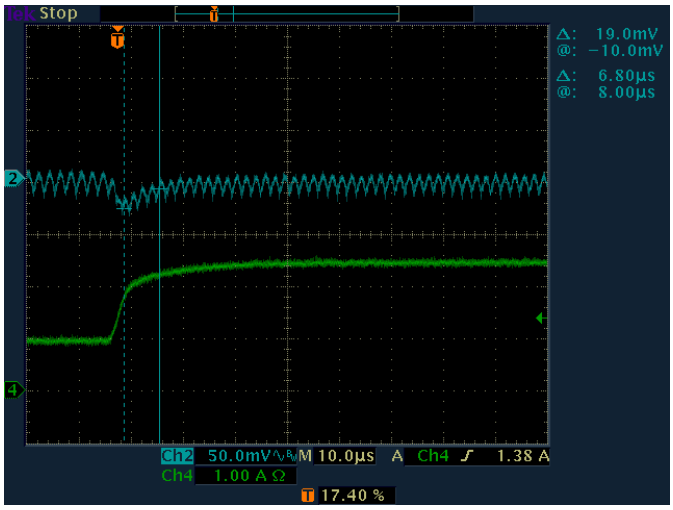


Figure 20: MP2316 Output Waveform during 1.5A Load Step Test

The settling time is around 6.8µs with an undershoot of around 30mV. The output shows a damped response, which indicates a phase margin of >45 degrees and therefore a stable loop. Refer to section 4 on page 19.

Using this settling time data and the phase margin data from section 2.3 on page 11 (61.5 degrees), we can now estimate the MP2316 closed loop bandwidth with Equation (14):

$$MP2316\ bandwidth = 4 * \frac{\sqrt{\cos(61.5°)}}{(\pi * 6.8\mu s * \sin(61.5°))} = 147.2kHz \quad (14)$$

Using the settling time data of 39.2µs and the phase margin data of 66.5 degrees from section 2.1 on page 6, we can now estimate the MP1497S's closed loop bandwidth using Equation (15):

$$MP1497S\ bandwidth = 4 * \frac{\sqrt{\cos(66.5°)}}{(\pi * 39.2\mu s * \sin(66.5°))} = 22.4kHz \quad (15)$$

The result of 22.4kHz is nearly half of the measured bandwidth of 49.9kHz.

Using the settling time method to estimate loop bandwidth does not appear to correlate with the measured data. However, the settling time method shows the MP2316 (COT) bandwidth to be much higher than that of the MP1497S (PCM).

As a side-by-side comparison, Figures 21a and 21b are the transient responses of the MP2316 COT buck versus the MP1497S PCM buck, respectively, using the same test conditions as above.

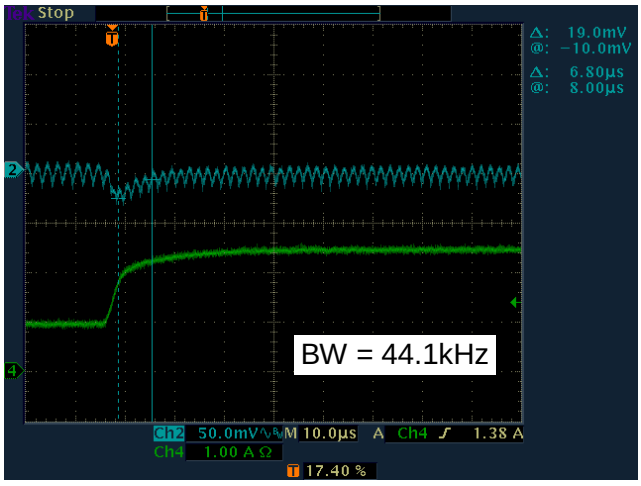


Figure 21a: MP2316 (COT) Load Transient Response

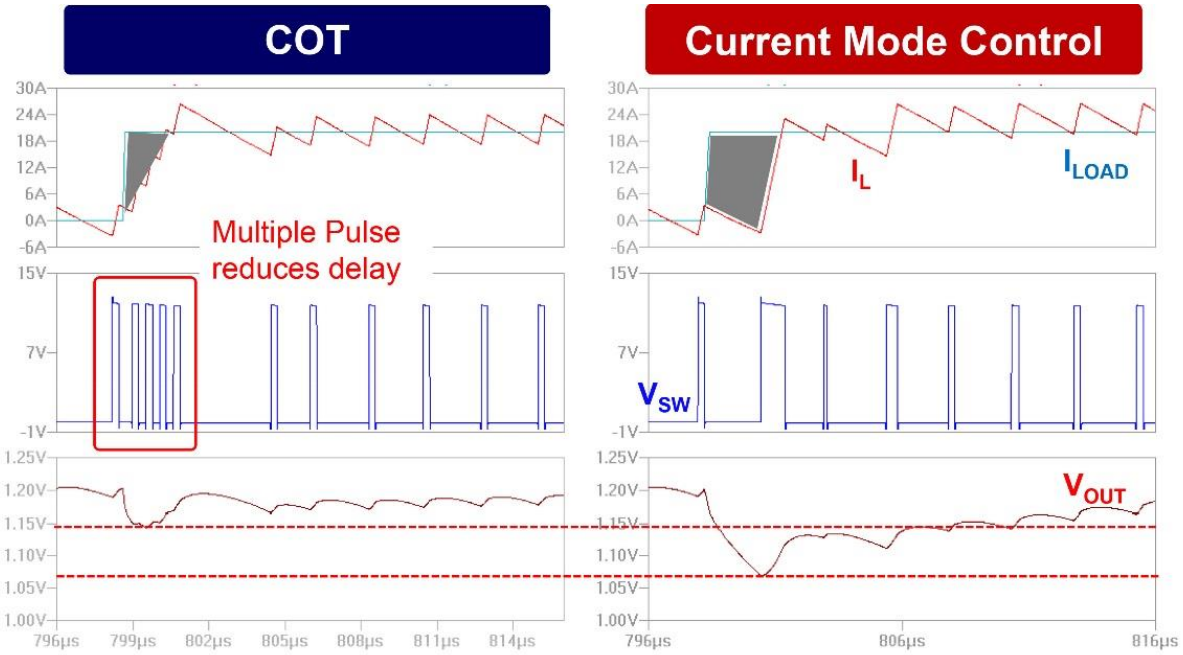
Figure 21b: MP1497S (PCM) Load Transient Response

The MP2316 (COT) has a much faster transient response compared to the MP1497S (PCM). This is because the COT-controlled buck converter switches to a much higher frequency with a fixed on-time and minimum off-time immediately whenever the feedback voltage drops below the reference voltage. During this condition, the COT converter delivers more current into the output capacitor and the load to support the front end of the load step, minimizing the undershoot and the settling time of the output.

Conversely, the MP1497S PCM converter relies mostly on the output capacitor to supply the front end of the load step current. This is because the MP1497S operates with a fixed frequency, so the inductor current must wait for the next switching cycle before it can increase to a higher peak level. Additionally,

the peak of the inductor current is set by the EA output, and the EA has internal Type II compensators. These internal compensators introduce delay to the loop that further slows down the reaction of the power stage during load step.

Figure 22 shows a comparison of the PCM- and COT-controlled buck converters during load step for further visual comparison. The shaded area is the front end of the step load current. The shaded area is the amount of charge drawn from the output capacitor. Since the shaded area on the PCM is larger, its output undershoot is larger than that in COT. Another benefit of COT is, for a given undershoot specification, a smaller output capacitance can be used compared to the PCM controlled converter.



***12VIN->1.2V/20A 400kHz 0.4uH Inductor 2x330uF+1x100uF**

Figure 22: COT vs. PCM Load Transient Response

3.3 Estimation of COT Loop Bandwidth Based on Measured Output Undershoot and Output Capacitance

Another way to estimate the COT loop bandwidth is to measure the output voltage undershoot and use Equation (16) or Equation (17) [3,4]:

$$\Delta V_{OUT} \approx \frac{\Delta I_{OUT}}{(2*\pi f_0 * C_{OUT})} \quad (16)$$

$$f_0 \approx \frac{\Delta I_{OUT}}{(\Delta V_{OUT} * C_{OUT} * 2 * \pi)} \quad (17)$$

Where ΔV_{OUT} is the output undershoot, ΔI_{OUT} is the load step current, f_0 is the loop bandwidth, and C_{OUT} is the output capacitance.

The output undershoot can be measured by applying a load step at the output of the converter.

[3] Tutorial on “DC-DC Converters Feedback and Control”, On Semiconductor, 2008
[4] Basso, Christophe, Designing Control Loops for Linear and Switching Power Supplies, Artech House, 2012

Figures 23a and 23b show the transient responses of the MP2316 COT buck versus the MP1497S PCM buck, respectively, from section 3.2 on page 14. The test conditions for both parts were Vin = 12V, Vout = 1.2V, Iout_DC = 1A, I_step = 1.5A @ 1.2A/µs, Fsw = 500kHz, L = 2.2µH, Cout = 22µF/25V.

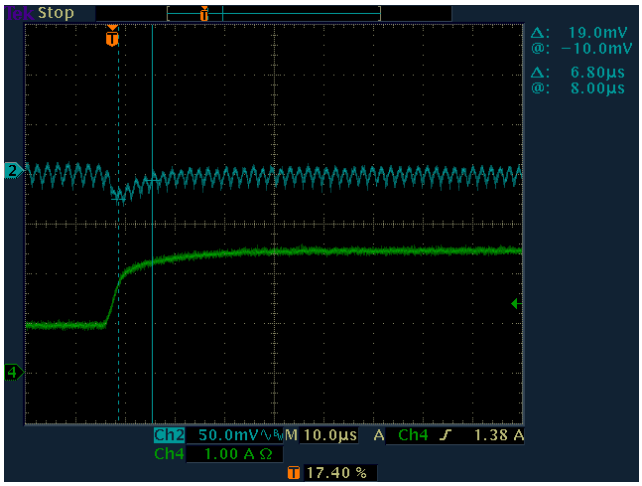


Figure 23a: MP2316 (COT) Load Transient Response

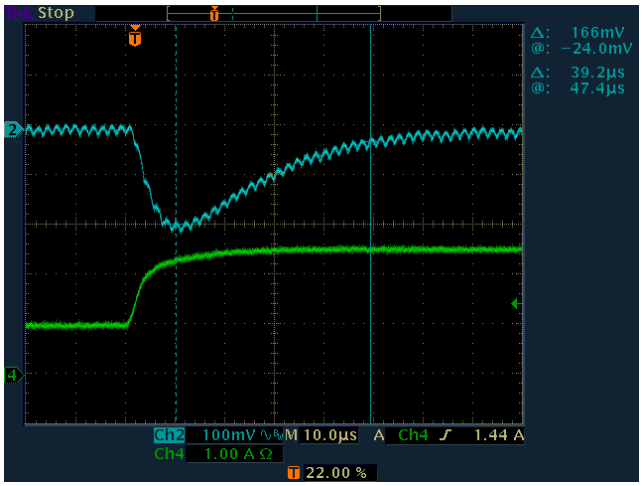


Figure 23b: MP1497S (PCM) Load Transient Response

The output undershoot for the MP2316 is ~30mV and ~200mV for the MP1497S when a 1.5A load step with a 1.2A/µs slew rate is applied.

The estimated loop bandwidth for the MP2316 (COT) and MP1497S (PCM) can be calculated with Equation (18) and Equation (19):

$$MP2316\ bandwidth = \frac{1.5A}{(30mV*22\mu F*2*\pi)} = 361.7kHz \quad (18)$$

$$MP1497S\ bandwidth = \frac{1.5A}{(200mV*22\mu F*2*\pi)} = 54.3kHz \quad (19)$$

The result of 54.3kHz is close to the measured bandwidth of 49.9kHz from section 2.1 on page 6.

This loop bandwidth estimation, which is based on the output undershoot, appears to be closer to the measured bandwidth of the MP1497S. If we base the MP2316 (COT) loop bandwidth on this approach, then it is around 6x wider than that of the MP1497S (PCM).

Whether both COT loop bandwidth estimation techniques are accurate or not, it is evident from the load transient response test data that the MP2316 (COT) has a much faster transient response compared to the MP1497S (PCM).

4. COT LOOP RESPONSE AND STABILITY USING LOAD STEP TEST

In section 3, we estimated the loop bandwidth of the COT buck using the output settling time and undershoot of the converter during load transient test. We have not yet addressed the stability of the COT buck converter after a load transient test. This section discusses the COT buck loop response and stability based on how its output voltage behaves upon the application of a load step.

4.1 Explanation of Load Step Response vs. Phase Margin

Figure 24 shows a plot of various step responses against the phase margin. This data was based on a peak current mode buck with a 4.3kHz loop bandwidth[3,4].

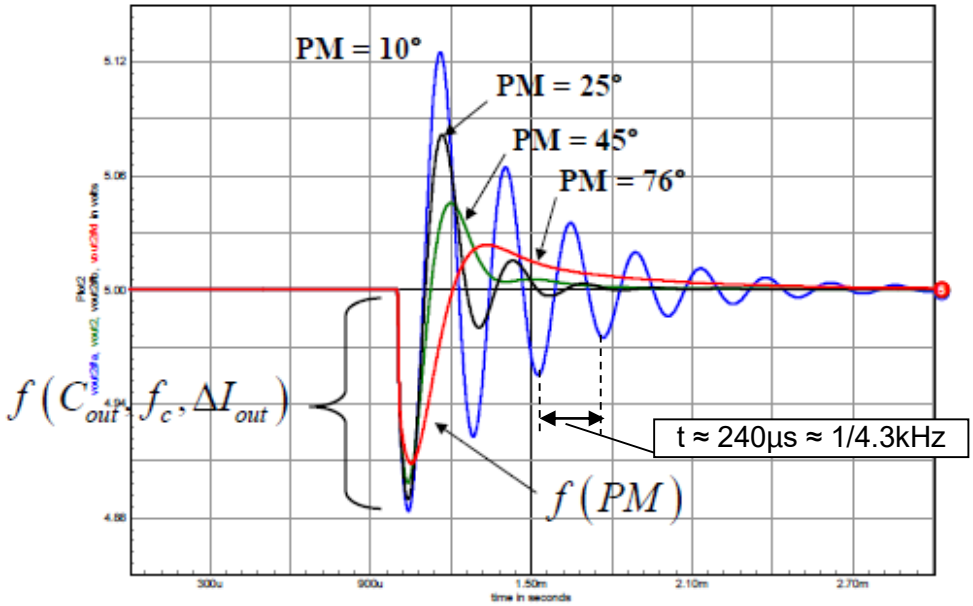


Figure 24: PCM Buck Transient Response

The ringing frequency is the inverse of the loop bandwidth. The lower the phase margin is, the more under-damped the transient response is. The higher the phase margin is, the more over-damped the transient response is. In other words, the lower the phase margin is, the more ringing on the converter load step response there is, and vice versa.

4.2 Estimating COT Buck Loop Response and Stability based on its Load Step Response

Bode plots show the loop bandwidth, gain, and phase of a system over a frequency range. Phase margin is the phase of the system when the gain = 0dB. A typical phase margin required for a stable system is higher than 45 degrees when the gain is 0dB. Gain margin is the gain of the system when the phase = 0 degrees. A typical gain margin for a stable system is lower than -10dB when the phase crosses 0 degrees. Loop bandwidth is the frequency when the system gain = 0dB. The higher the bandwidth is, the faster the system transient response is.

In time domain, the load step response of a system indicates how fast the system reacts to the load step and whether it has a damped or oscillatory response. Table 2 shows a quick comparison between the bode plot and load step response on a system.

Table 2: Comparison of Bode Plot and Positive Load Step Response

Bode Plot	Loop Bandwidth (kHz)	Phase Margin (Degrees)	Gain Margin (dB)
Positive Load Step Response	Magnitude of output voltage undershoot (mV)	Output voltage behavior after load step (magnitude of overshoot, duration of settling time, and whether it has damped or oscillatory response)	Does not show up in the load transient response

Since the bode plot of a COT buck does not reflect how fast it responds to a load step, we can use its load transient or load step response to measure how fast it reacts to a load step and how well it recovers after the load step application.

We can use the load transient response plot in Figure 25[3.4] as our template.

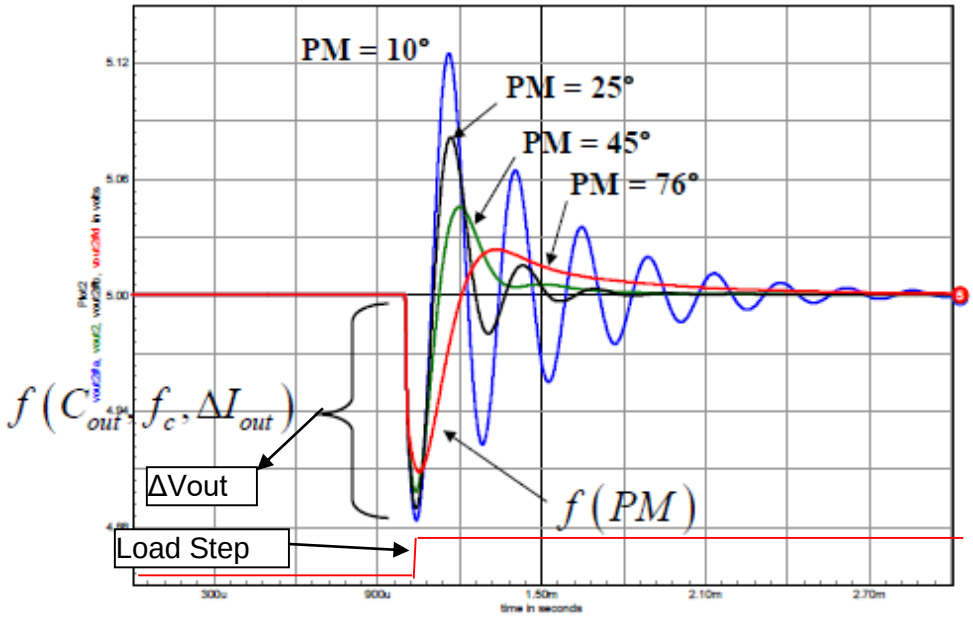


Figure 25: PCM Buck Transient Response

The undershoot magnitude (ΔV_{OUT}) roughly equals $\Delta I_{OUT}/(2*\pi*f_0*C_{OUT})$, per Equation (16), if we exclude the output capacitor's ESR and equivalent series inductance (ESL). The smaller the output undershoot, the faster the loop response is.

This is evident when comparing the transient responses of the MP1497S PCM buck versus the MP2316 COT buck, where the output undershoot for the MP2316 is ~30mV and ~200mV for the MP1497S when a 1.5A load step with a 1.2A/µs slew rate is applied (see Figure 21a and Figure 21b).

The output behavior after the load step application shows how fast the converter settles back to regulation, how high the output overshoot is, and whether it has a damped or oscillatory response. In this application note, we use the number of rings as an indication of the COT converter phase margin. As shown in Figure 25, the lower the phase margin is, the more ringing there is on the output after the load step application, and vice versa. The lower the phase margin, the longer the settling time and output overshoot are, and vice versa. Using the different transient responses from Figure 25, we can make the summary shown in Table 3.

Table 3: Comparison of Phase Margin and Number of Output Rings after Load Step

Phase Margin	10°	25°	45°	76°
No. of Output Rings after Load Step Application	7	3	1	0

This table can be used as a rough guide when estimating the phase margin of the COT converter by counting the number of oscillatory rings on the output after the load step application. The lower the number of output rings there are after the load step application, the higher the phase margin is, and therefore, the more stable the converter is.

In Figure 21a, the MP2316 COT buck output response to the load step shows no ring, which indicates that its phase margin is greater than 45 degrees. In section 2.3, the bode plot for the MP2316 shows 61.5 degrees of phase margin, which should show no rings after the load step application. In Figure 8, the MP1497S PCM buck output response to the load step shows no ringing, which indicates that its phase margin is greater than 45 degrees. In section 2.1, the bode plot for the MP1497S shows 66.5 degrees of phase margin, which should show no rings after the load step application.

SUMMARY

The bode plot of a constant-on-time (COT) buck converter can be measured using a loop analyzer and the same measurement method used on the peak-current mode (PCM) converter. The PCM bode plot information (loop bandwidth and phase margin) correlates well with its transient response. However, on the measured COT bode plot, only the phase margin and gain margin information can be used, since these are the loop response when operating at a constant switching frequency. The frequency of the injected AC signal is less than the converter's switching frequency. The loop bandwidth information cannot be used, since the COT converter switches to its maximum frequency at fixed on time and minimum off time during transient loading when the feedback voltage falls below the reference voltage.

Since the loop bandwidth estimation using a measured settling time, phase margin data, and Equation (13) does not correlate to the measured MP1497S data, we cannot use this approach to estimate the COT loop bandwidth.

Estimating the loop bandwidth using the output voltage undershoot and Equation (17) nearly correlates to the measured MP1497S bandwidth. If we use the same method to estimate the loop bandwidth of the MP2316 (COT), it is evident that its bandwidth is indeed much higher than the MP1497S (PCM). This is evident also on their respective measured transient responses.

A better way to estimate the loop response of a COT converter is to measure its load step or load transient response.

The smaller the output undershoot is, the faster the loop response is. This is evident when comparing the transient responses of the MP1497S PCM buck versus the MP2316 COT buck as shown in Figure 21a and Figure 21b, where the output undershoot for the MP2316 is ~30mV and ~200mV for the MP1497S when a 1.5A load step with a 1.2A/µs slew rate is applied.

The lower the number of output rings is after the load step application, the higher the phase margin is, and therefore, the more stable the converter is. Both the MP2316 COT buck and MP1497S PCM buck show no ringing on their respective output after the load step application, which indicates that the phase margin that is greater than 45 degrees. In fact, their measured phase margins are 61.5 degrees and 66.5degrees, respectively (see Table 4).

Table 4: Summary of PCM vs. COT Methods/Results

	Measured BW	Measured PM	Measured GM	Settling Time	Estimated BW using Settling Time and Equation (15)	Undershoot during Load Step	Estimated BW using Undershoot and Equation (16) or (17)
MP1497S (PCM)	49.9kHz	66.5°	-12.4dB	39.2µs	22.4kHz	200mV	54.3kHz
MP2316 (COT)	44.1kHz	61.5°	-11.7dB	6.8µs	147.2kHz	30mV	361.7kHz