DIY8883

High-Efficiency, 45V, 3A, Digitally Calibrated Synchronous Step-Down Converter

DESCRIPTION

The DIY8883 is a high frequency, synchronous, rectified, step-down converter with an I²C control interface and a multipage one-time programmable memory. It can achieve up to 3A continuous output current with excellent load and line regulation over a wide input supply range.

The DIY8883 integrates internal high-side and low-side power MOSFETs for high efficiency without an external Schottky diode and is available in a 16-pin QFN3x3 package. With internal compensation and a feedback divider, the DIY8883 can offer a very compact solution with a minimal number of readily available, standard, external components.

The DIY8883 is designed to be very versatile. The output voltage level can be adjusted from 0.6V to 12V on-the-fly through an I²C serial interface. Voltage slew rate, switching frequency, enable, and power savings mode are also programmable via the I²C interface. This allows users to optimize each output for their particular requirements.

During bench evaluations, different configurations can be easily obtained through the I²C interface instead of reworking external components. Once the desired optimal setting has been reached, a multipage, one-time programmable memory is available, allowing the settings to be stored permanently .

Current-mode operation provides fast transient response and eases loop stabilization. Full protection features include under-voltage lockout (UVLO), over-voltage protection (OVP), over-current protection (OCP), and over-temperature protection (OTP).

FEATURES

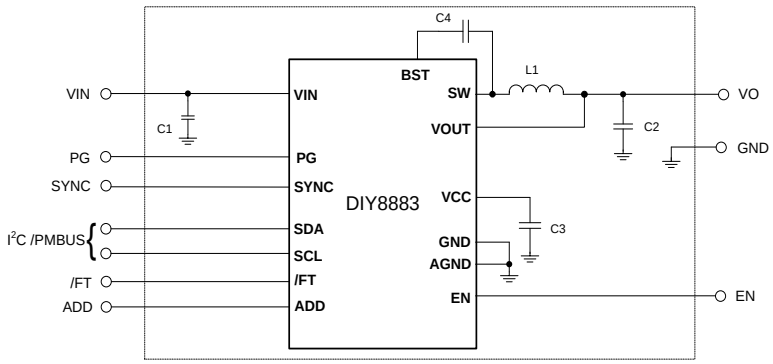
- Wide 3.5V to 45V Operation Input Range
- 3A Continuous Output Current
- High Efficiency Synchronous Mode Control
- Internal 90mΩ/50mΩ Low $R_{DS(ON)}$ MOSFETs
- Power Good and Fault Indications
- OVP, OCP, and OTP
- Internal Soft Start
- Programmable Address by Resistor
- Programmability via I²C Interface
  - Output Range from 0.6V to 12V
  - Switching Frequency
  - Compensation Network
  - Slope Compensation
  - EN Threshold
  - Input UVLO Threshold
  - PG Threshold
  - AAM, CCM Selection
  - Light-Load Mode Threshold
  - SCP Mode Selection
  - Current Limit Threshold
  - OVP Mode Selection
  - Input /Output OVP Threshold
  - OTP Threshold
  - Switching Slew Rate
  - Output Slew Rate (SS Time)
  - Phase Shift
  - Frequency Dithering for Low EMI Operation
- Multipage One-Time Programmable Memory for Permanent Storage
- Available in 16-pin QFN3x3 Package

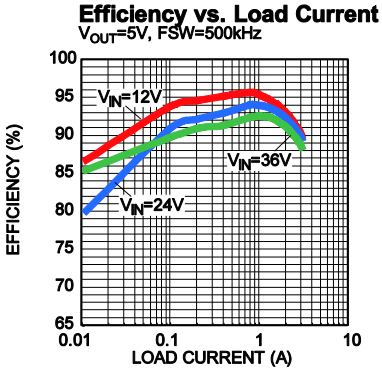
APPLICATIONS

- Industrial Power Systems
- Automotive Power Systems

Telecommunication Systems All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Products, Quality Assurance page.

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
DIY8883GQ-xxxx	QFN16 (3mmx3mm)	*See Below*

*For Tape & Reel, add suffix –Z (e.g. DIY8883GQ-xxxx–Z);

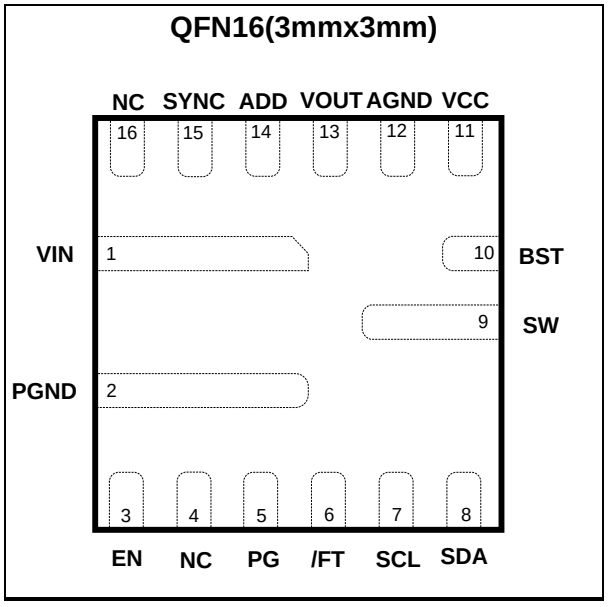
Note: The 4-digit suffix code “xxxx” is the configuration identifier for the register settings stored in the one-time programmable memory. For default configuration, the code is “0001”. For customized configurations, please contact the factory to get a 4-digit suffix code.

TOP MARKING

AQUY
LLL

AQU: Product code
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to 48V
V_{SW}.....-0.3V to V_{IN}+0.3V
V_{EN} .....-0.3V to 48V
V_{BST} ..... V_{SW}+5.5V
V_{CC} .....-0.3V to 5.5V
All Other Pins.....-0.3V to 5V
Continuous Power Dissipation(T_A = +25°C) **(2)**
QFN-16 (3mmx3mm)..... 2.27W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage (V_{IN}).....3.5V to 45V
Output Voltage (V_{OUT}) .....0.6V to 12V
Operating Junction Temp.(T_J).. -40°C to +150°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN16(3mmx3mm)……..55..... 13... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

DC/DC ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J =-40°C to +125°C(5), unless otherwise noted. Typical values are at T_J =+25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	$INUV_{Vth}$	I²C default set	2.9	3.2	3.4	V
V_{IN} UVLO threshold hysteresis	$INUV_{HYS}$	I²C default set		122		mV
VIN UVLO threshold DAC range	INUVVth	I²C set range	3.2		7.4	V
V_{IN} quiescent current	I_Q	V_{OUT}=5V V_{FB}>V_{REF} without BIAS power, no load, T_J =25°C		600	1000	μA
		V_{OUT}=5V V_{FB}>V_{REF} with BIAS power, no load(6)		11		μA
V_{IN} shutdown current	I_{SD}	V_{EN}=0V, T_J =25°C			1	μA
Default output voltage	V_{OUT}	I²C default set, T_J =25°C	4.95	5	5.05	V
	V_{OUT}	I²C default set, T_J =40~125°C	4.925	5	5.075	V
Operation output range	V_{OUT}	I²C set range	0.6		12	V
Default switching frequency	f_{SW}	I²C default set, T_J =25°C	450	500	550	kHz
Frequency programmable range	FPROG	I²C set range	250		2500	kHz
Sync frequency range	FSYNC	SNYC clock set range	250		2500	kHz
Sync voltage high threshold	VSYNC-HIGH			1.4	2	V
Sync voltage low threshold	VSYNC-LOW		0.4	1.1		V
Minimum on time(7)	T_{ON-MIN}	With emulated peak current mode		40		ns
		With peak current mode		80		ns
Minimum off time(7)	$T_{OFF-MIN}$			380		ns
HS switch on resistance	R_{DSON-H}	V_{BST}-V_{SW}=5V		95	180	mΩ
LS switch on resistance	R_{DSON-L}			50	100	mΩ
BST-SW refresh UVLO					2.8	V
BST-SW refresh UVLO hysteresis				0.2		V
Default soft-start time	T_{SS}	I²C default set		1		ms
Soft-start time range	T_{SS}	I²C set range	0.5		4	ms
Default EN voltage threshold	V_{EN}	I²C default set	1	1.2	1.4	V
EN voltage threshold range	V_{EN}	I²C default set	1.2		2	V
Default EN voltage hysteresis	V_{EN-HYS}	I²C default set		220		mV
EN voltage hysteresis range	V_{EN-HYS}	I²C default set	220		420	mV
Default PG upper trip threshold		As percentage of V_{OUT} set		110		%
PG upper trip threshold range		I²C set value	110		115	%
Default PG lower trip threshold		As percentage of V_{OUT} set		89		%
PG lower trip threshold range		I²C set value	84		89	%
PG trip threshold hysteresis		As percentage of V_{OUT} set		5.5		%
PG trip threshold hysteresis range		I²C set value	3		5.5	%

DC/DC ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J =-40ºC to +125ºC(5), unless otherwise noted. Typical values are at T_J =+25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG output voltage low	$V_{PG-SINK}$	I_{SINK} = 1mA		0.1	0.3	V
PG deglitch timer	$T_{PG-DELAY}$	Rising		30		µs
PG deglitch timer	$T_{PG-DELAY}$	Falling		30		µs
VCC regulator	V_{CC}	I_{CC}=0mA	4.8	5	5.2	V
Default peak current limit(7)	$I_{PEAK-LIMIT}$	I²C default set	4	5	6	A
Peak current limit range(7)	$I_{PEAK-LIMIT}$	I²C default set	2		8	A
Default valley current limit(7)	$I_{VALLEY-LIMIT}$	I²C default set	2.8	3.5	4.8	A
Valley current limit range(7)	$I_{VALLEY-LIMIT}$	I²C default set	1.5		4.5	A
Default output OVP threshold		As percentage of V_{OUT} set	115	120	125	%
Output OVP threshold range		I²C set range	110		130	%
Default output OVP hysteresis		As percentage of VOUT set		5.7		%
Output OVP hysteresis range		I²C set range	3.2		5.7	%
Input OVP threshold range		I²C set range	28		40	V
Input OVP threshold accuracy		I²C set 34V	32	34	36	V
Default input OVP hysteresis		As percentage of input OVP threshold set		5.5		%
Input OVP hysteresis range		I²C set range	3.5		5.5	%
Default thermal shutdown(7)	T_{SD}	I²C default set	150	175		°C
Thermal shutdown range (7)	T_{SD}	I²C set range	125		175	°C
Default thermal shutdown hysteresis(7)	T_{SD-SYS}	I²C default set		25		°C
Thermal shutdown hysteresis range(7)	T_{SD-SYS}	I²C set range	25		50	°C

Notes:

5) Not tested in production and guaranteed by over-temperature correlation.
6) This current is measured from Vin, Vcc external bias current does not include.
7) Not tested in production and guaranteed by design and characterization.

I²C PORT SIGNAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J =-40°C to +125°C(5), unless otherwise noted. Typical values are at T_J =+25°C.

Parameters	Symbol	Condition	Min	Typ	Max	Units
I²C Interface Specifications						
Input logic low	V_{IL}		0		0.4	V
Input logic high	V_{IH}		1.3			V
Output logic low	V_{OL}	I_{LOAD}=3mA			0.4	V
SCL clock frequency	f_{SCL}				400	kHz
SCL high time	t_{HIGH}		0.6			µs
SCL low time	t_{LOW}		1.3			µs
Data setup time	$t_{SU,DAT}$		100			ns
Data hold time	$t_{HD,DAT}$		0		0.9	µs
Setup time for repeated start	$t_{SU,STA}$		0.6			µs
Hold time for start	$t_{HD,STA}$		0.6			µs
Bus free time between a start and a stop condition	t_{BUF}		1.3			µs
Setup time for stop condition	$t_{SU,STO}$		0.6			µs
Rise time of SCL and SDA	t_R		20+0.1 ×C_B		120	ns
Fall time of SCL and SDA	t_F		20+0.1 ×C_B		120	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

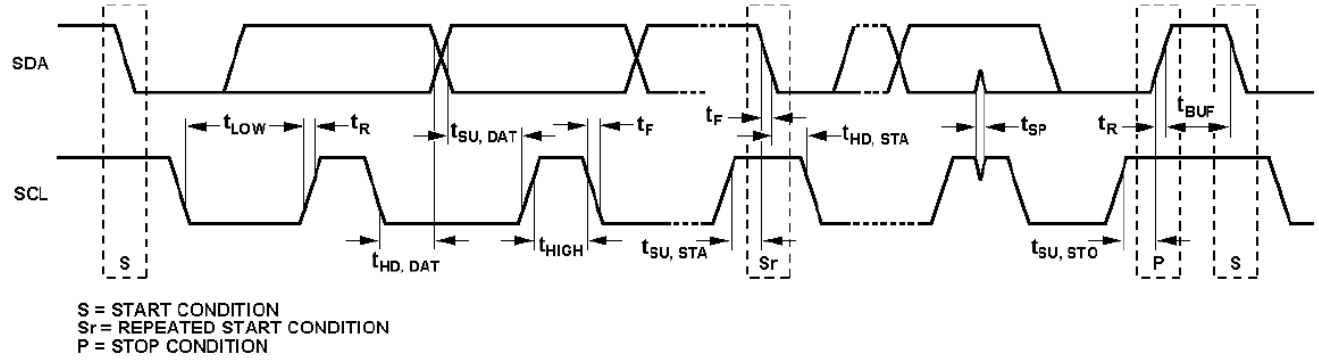


Figure 1: I²C Compatible Interface Timing Diagram

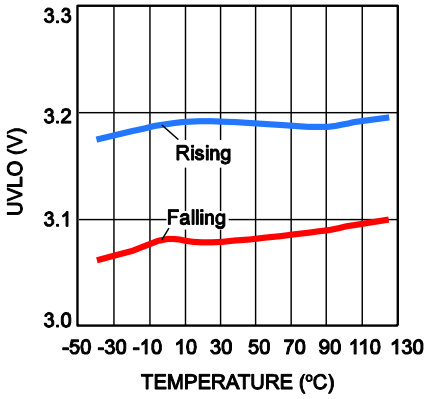
PIN FUNCTIONS

Pin #	Name	Description
1	VIN	**Supply voltage.** VIN supplies all power to the converter. Place a decoupling capacitor to ground as close as possible to the IC to reduce switching spikes. Connect using a wide PCB trace.
2	PGND	**Power ground.** Reference ground of the regulated output voltage. Connect PGND to larger copper areas for the best thermal results.
3	EN	**Enable.** Drive EN high to turn on the device, and drive it low or float it to turn off the device. It has an internal 1MΩ pull-down resistor to ground.
4	NC	**No connection.** No inside circuit is connected to NC.
5	PG	**Power good indicator.** The output of PG is an open drain. Please connect a resistor to a pull-up power source if used.
6	/FT	**Fault indicator.** Any Fault or Warning will pull /FT down.
7	SCL	**I²C serial clock.**
8	SDA	**I²C serial data.**
9	SW	**Switch output.** Internally connect to the high-side and low-side power switches. Externally connect to the output inductor. Please connect using a wide PCB trace.
10	BST	**Bootstrap.** Requires a capacitor connected between SW and BST to form a floating supply across the high-side switch driver.
11	VCC	**Internal 5V LDO regulator output.** Decouple with 0.22µF capacitor.
12	AGND	**Signal ground.** Ground for the internal logic and signal circuit. AGND is not connected to power ground internally. Ensure AGND is connected to power ground in the PCB layout.
13	VOUT	**Sense input of output voltage**.
14	ADD	**Address setting for I²C.**
15	SYNC	**Synchronized to external clock signal.** SYNC can be programmed by I²C to sync the input or output.
16	NC	**No connection.** No inside circuit is connected to NC. Keep floating.

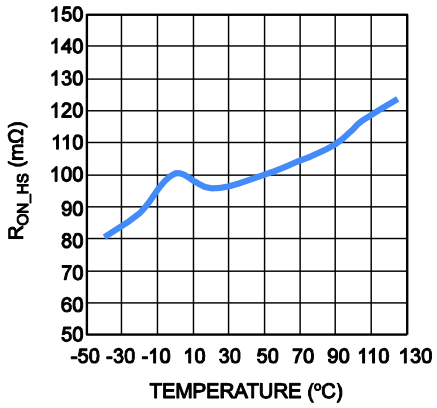
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J =-40°C to +125°C(5), unless otherwise noted. Typical values are at T_J =+25°C.

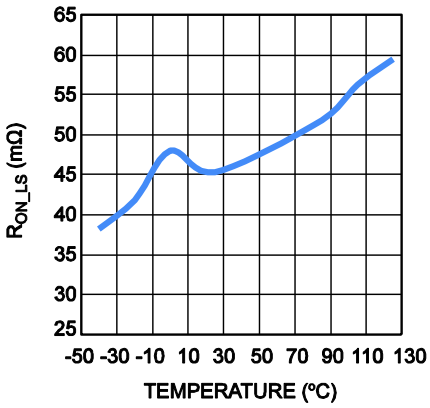
VIN UVLO Threshold vs. Temperature



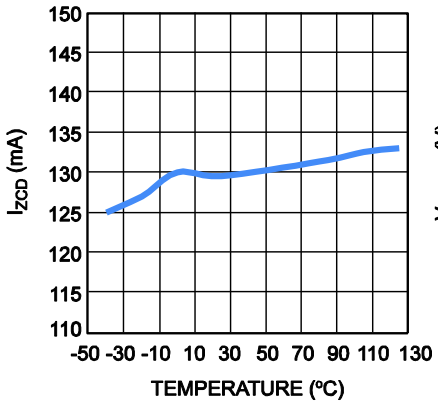
HS-FET On Resistance vs. Temperature



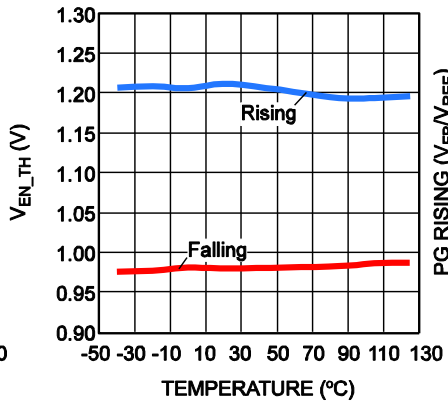
LS-FET On Resistance vs. Temperature



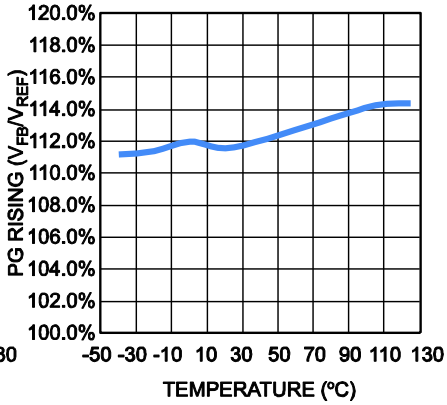
ZCD Current vs. Temperature



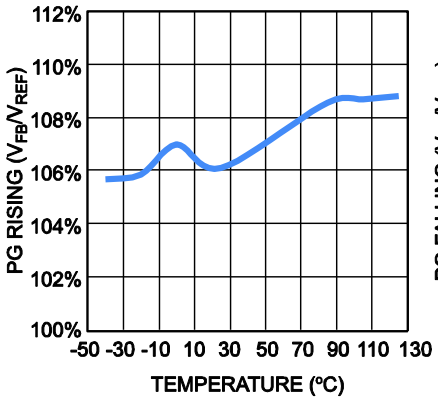
EN Threshold vs. Temperature



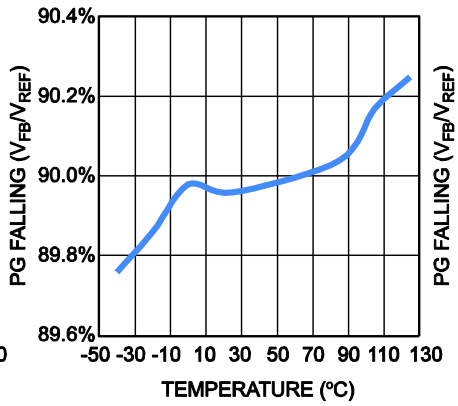
PG Rising Threshold (V_{FB} Rising) vs. Temperature



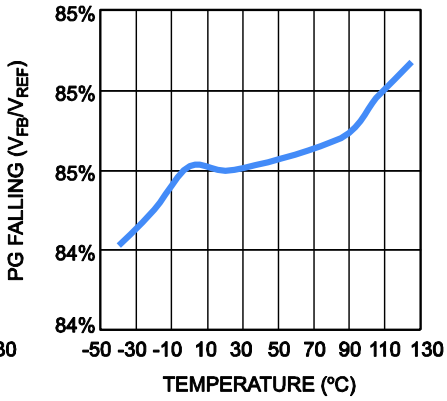
PG Rising Threshold (V_{FB} Falling) vs. Temperature



PG Falling Threshold (V_{FB} Falling) vs. Temperature



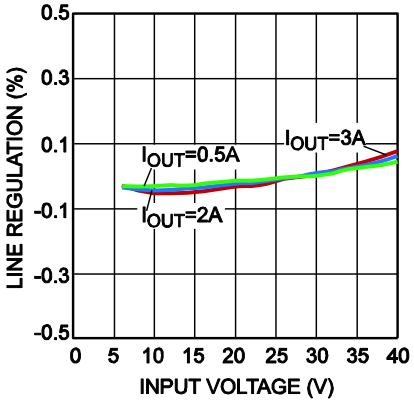
PG Falling Threshold (V_{FB} Rising) vs. Temperature



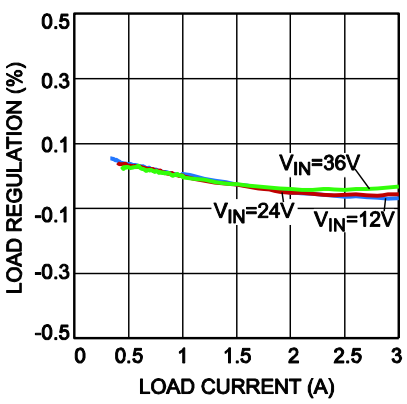
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT}= 3.3V,L= 10µH, F_{SW}=500kHz, AAM mode, T_A = +25°C, unless otherwise noted.

Line Regulation

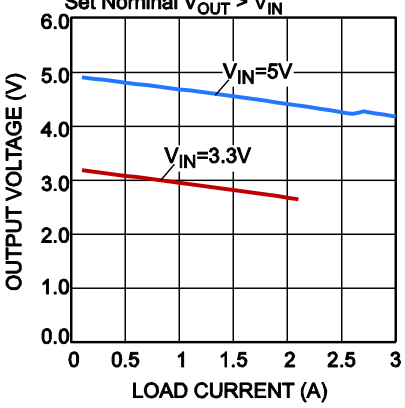


Load Regulation



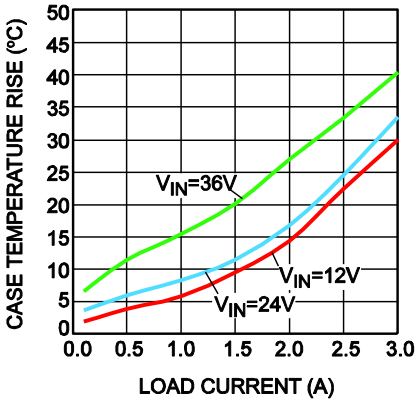
Output Voltage vs. Load Current

Dropout Performance
Set Norminal V_{OUT} > V_{IN}



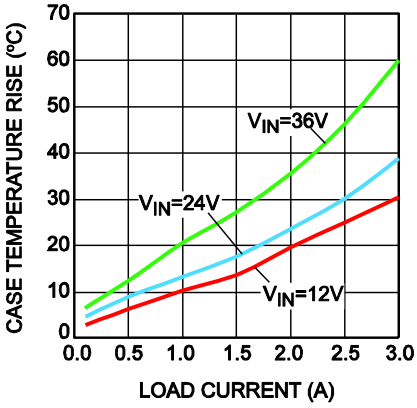
Case Temperature Rise vs. Load Current

V_{OUT}=3.3V, F_{SW}=500kHz



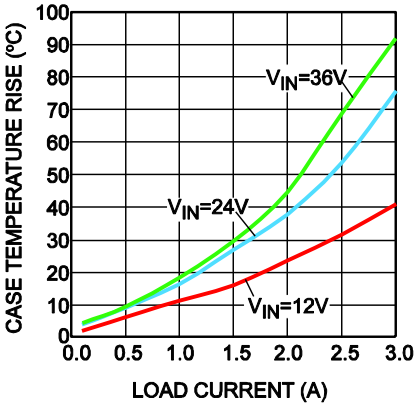
Case Temperature Rise vs. Load Current

V_{OUT}=3.3V, F_{SW}=1MHz



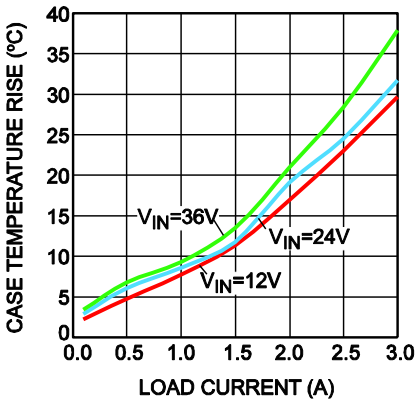
Case Temperature Rise vs. Load Current

V_{OUT}=3.3V, F_{SW}=2MHz



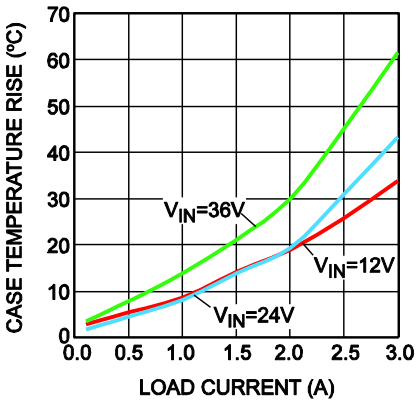
Case Temperature Rise vs. Load Current

V_{OUT}=5V, F_{SW}=500kHz



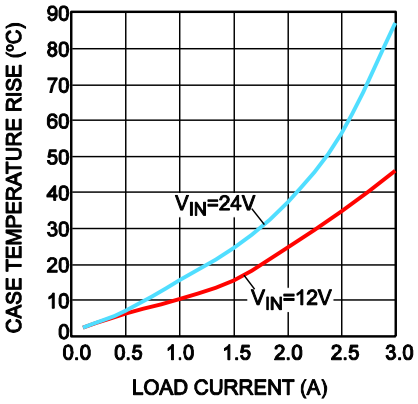
Case Temperature Rise vs. Load Current

V_{OUT}=5V, F_{SW}=1MHz



Case Temperature Rise vs. Load Current

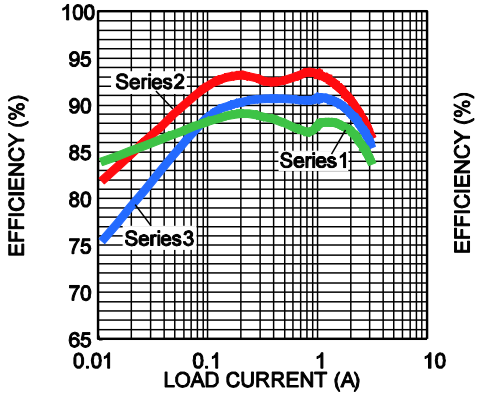
V_{OUT}=5V, F_{SW}=2MHz



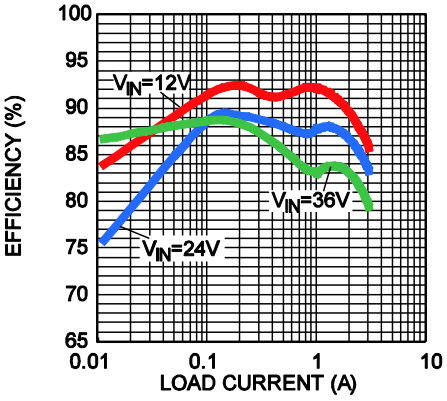
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT}=3.3V, L=10µH, F_{SW}=500kHz, AAM mode, T_A = +25°C, unless otherwise noted.

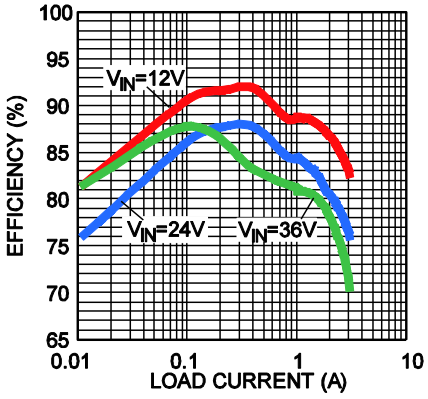
Efficiency vs. Load Current
V_{OUT}=3.3V, FSW=500kHz



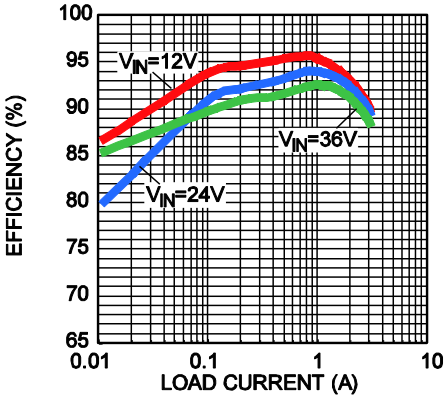
Efficiency vs. Load Current
V_{OUT}=3.3V, FSW=1MHz



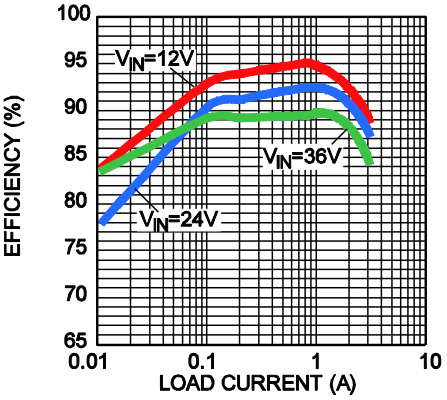
Efficiency vs. Load Current
V_{OUT}=3.3V, FSW=2.2MHz



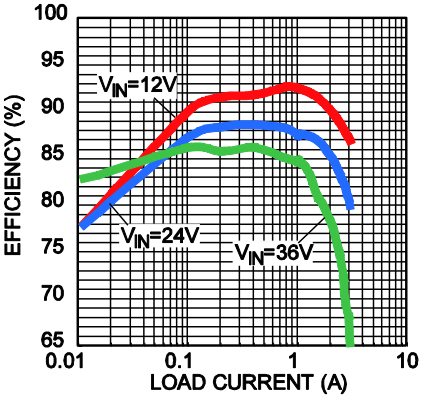
Efficiency vs. Load Current
V_{OUT}=5V, FSW=500kHz



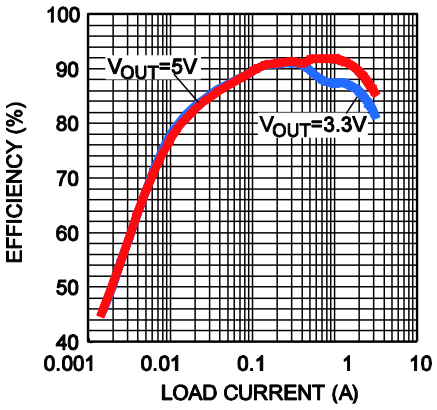
Efficiency vs. Load Current
V_{OUT}=5V, FSW=1MHz



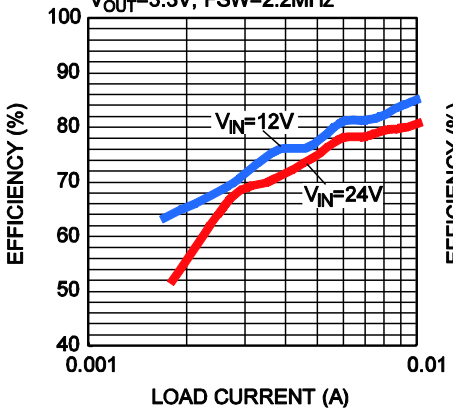
Efficiency vs. Load Current
V_{OUT}=5V, FSW=2.2MHz



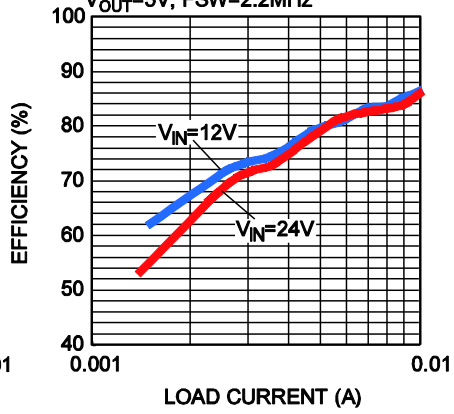
Efficiency vs. Load Current
V_{IN}=14V, FSW=2.2MHz



Efficiency vs. Load Current (Extreme Light Load)
V_{OUT}=3.3V, FSW=2.2MHz



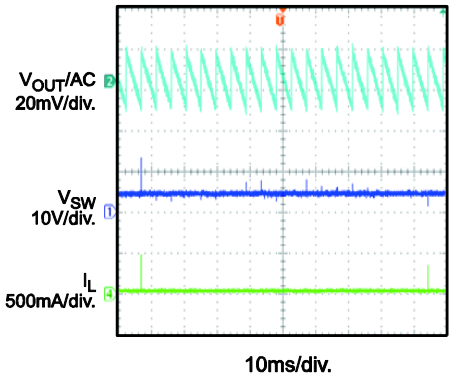
Efficiency vs. Load Current (Extreme Light Load)
V_{OUT}=5V, FSW=2.2MHz



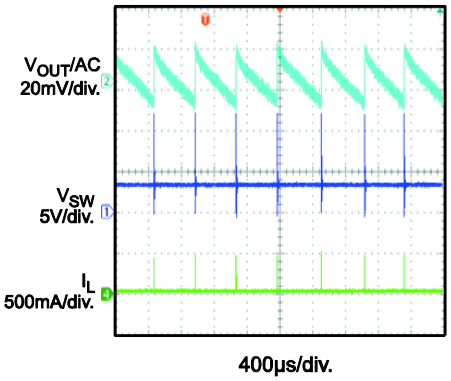
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT}=3.3V, L=10µH, F_{SW}=500kHz, AAM mode, T_A = +25°C, unless otherwise noted.

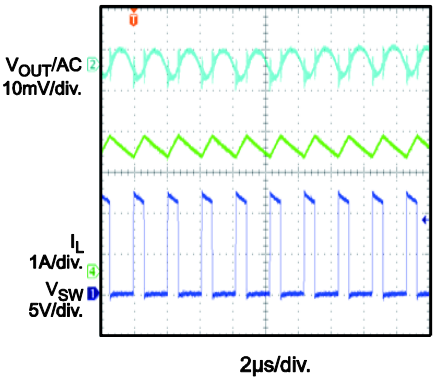
Steady State
I_{OUT}=0A, AAM mode



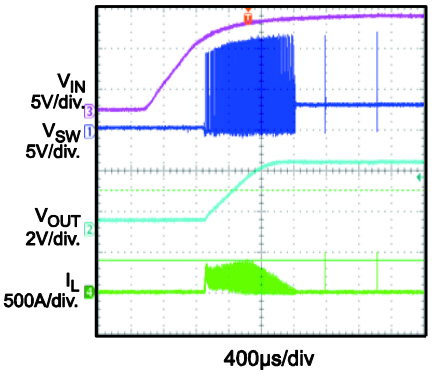
Steady State
I_{OUT}=1mA, AAM mode



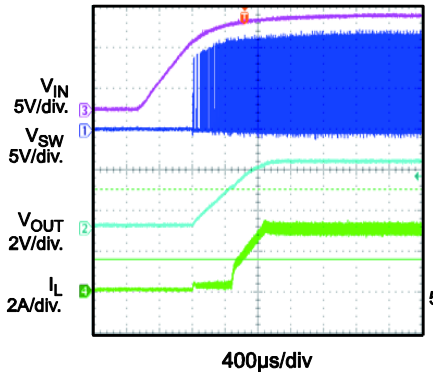
Steady State
I_{OUT}=3A



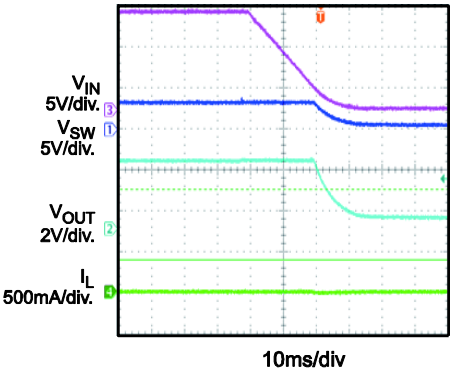
Start-up through VIN
I_{OUT}=0A



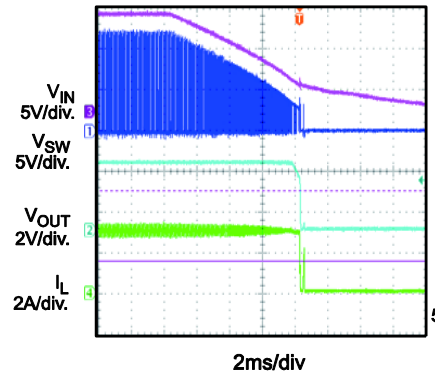
Start-up through VIN
I_{OUT}=3A



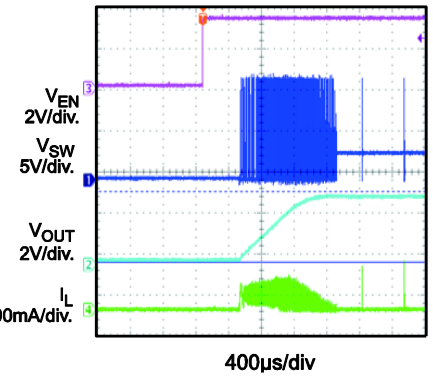
Shutdown through VIN
I_{OUT}=0A



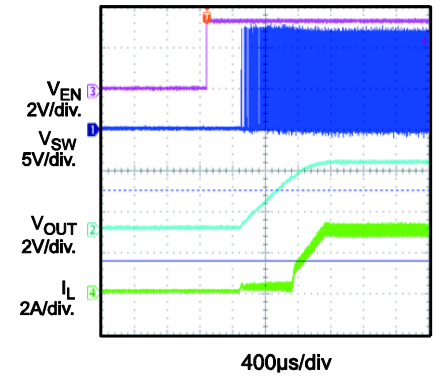
Shutdown through VIN
I_{OUT}=3A



VIN Power Off
Start-up through EN



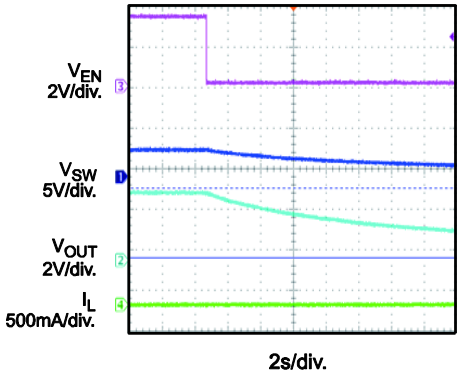
Start-up through EN
I_{OUT}=3A



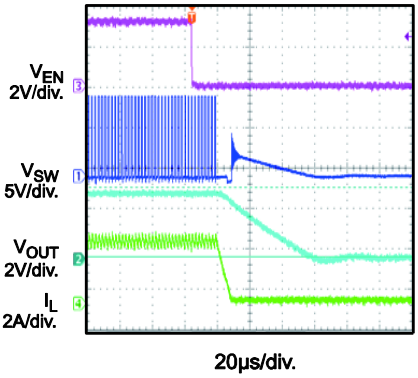
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT}=3.3V, L=10µH, F_{SW}=500kHz, AAM mode, T_A = +25°C, unless otherwise noted.

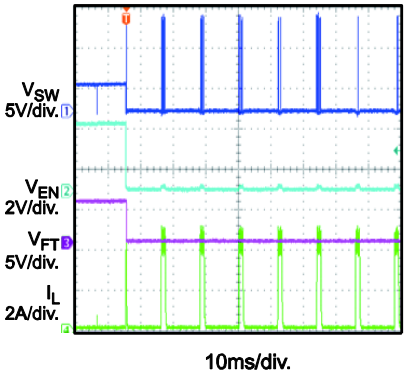
Shutdown through EN
I_{OUT}=0A



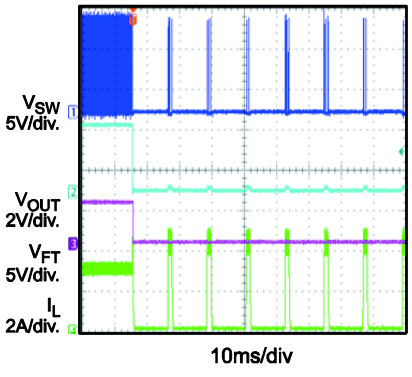
Shutdown through EN
I_{OUT}=3A



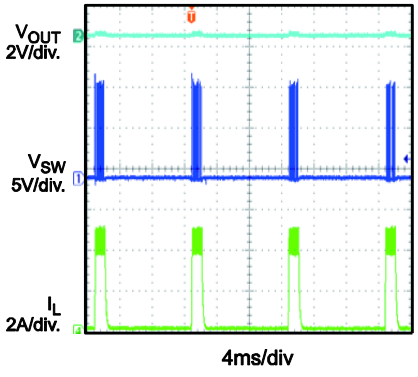
SCP Entry
I_{OUT}=0A to short circuit



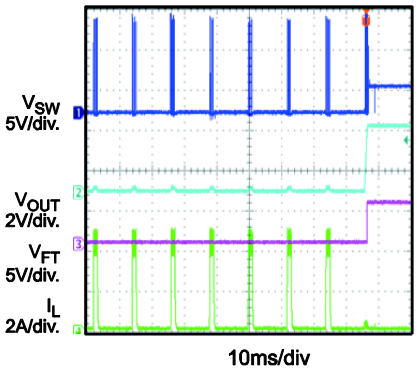
SCP Entry
I_{OUT}=3A to short circuit



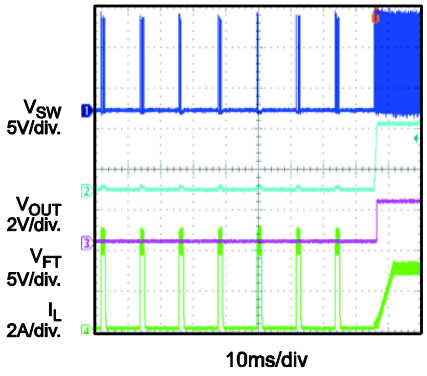
SCP Steady State



SCP Recovery
short circuit to I_{OUT}=0A



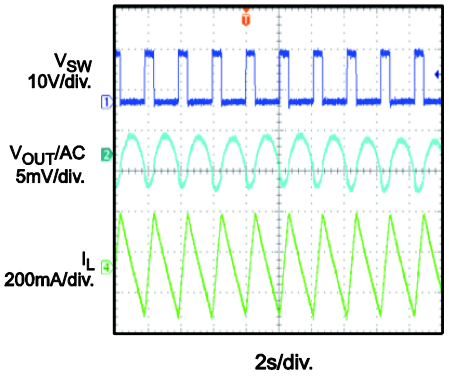
SCP Recovery
short circuit to I_{OUT}=3A



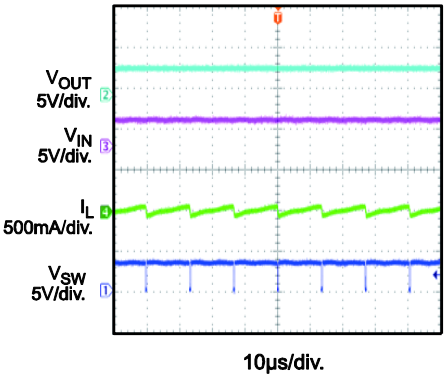
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT}=3.3V, L=10µH, F_{SW}=500kHz, AAM mode, T_A = +25°C, unless otherwise noted.

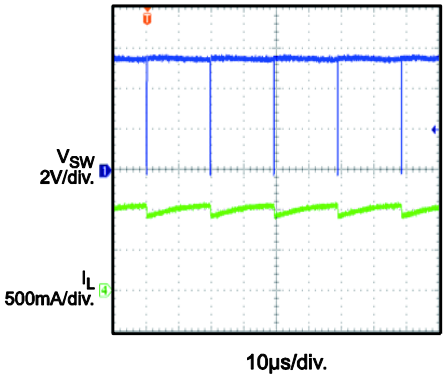
Forced CCM Operation
I_{OUT}=0A, forced CCM mode



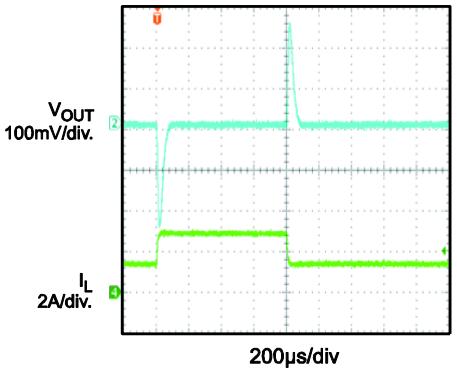
Dropout Operation
V_{IN}=3.3V, V_{OUT} set to 3.3V, I_{OUT}=0A



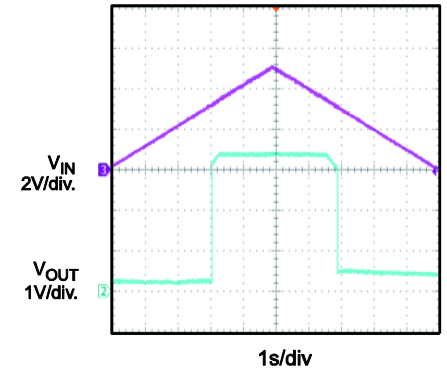
Dropout Operation
V_{IN}=6V, V_{OUT} set to 7V, I_{OUT}=3A



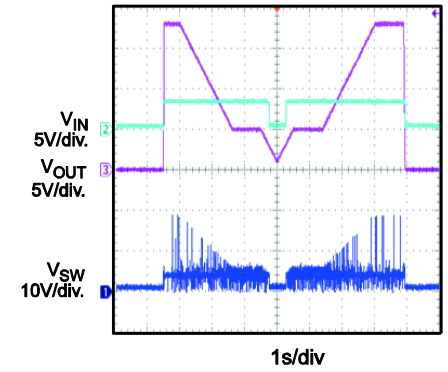
Load Transient
I_{OUT}=1.5A<->3A, 1.6A/µs



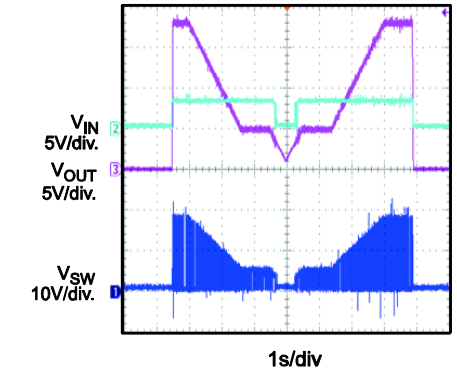
VIN Ramp Up and Down
I_{OUT}=0.1A



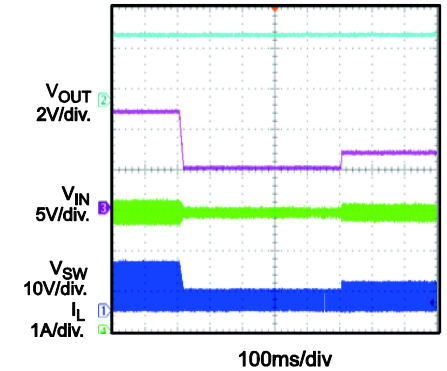
VIN Ramp Down and Up
I_{OUT}=10mA



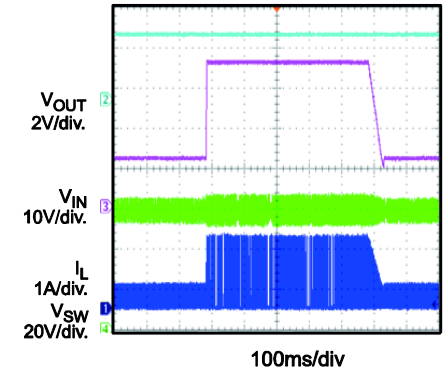
VIN Ramp Down and Up
I_{OUT}=3A



Cold-Crank
V_{IN}=12V->5V->7V, I_{OUT}=3A

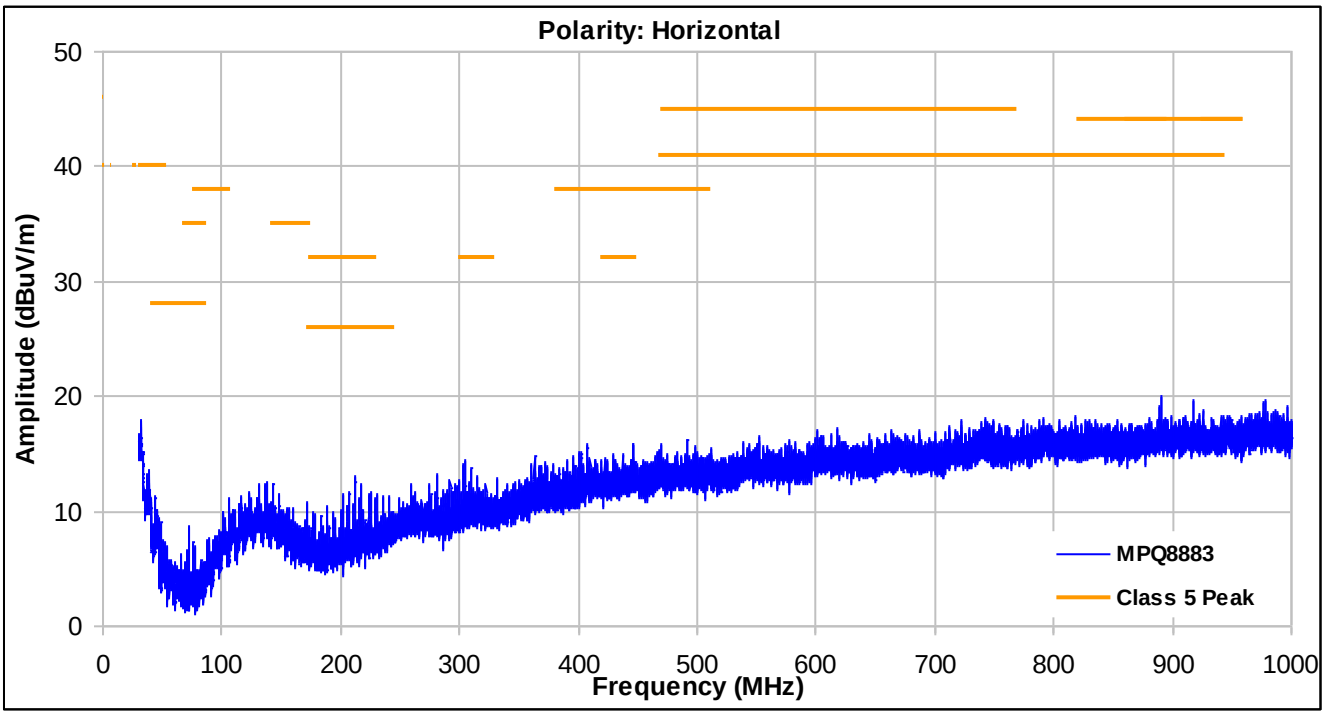


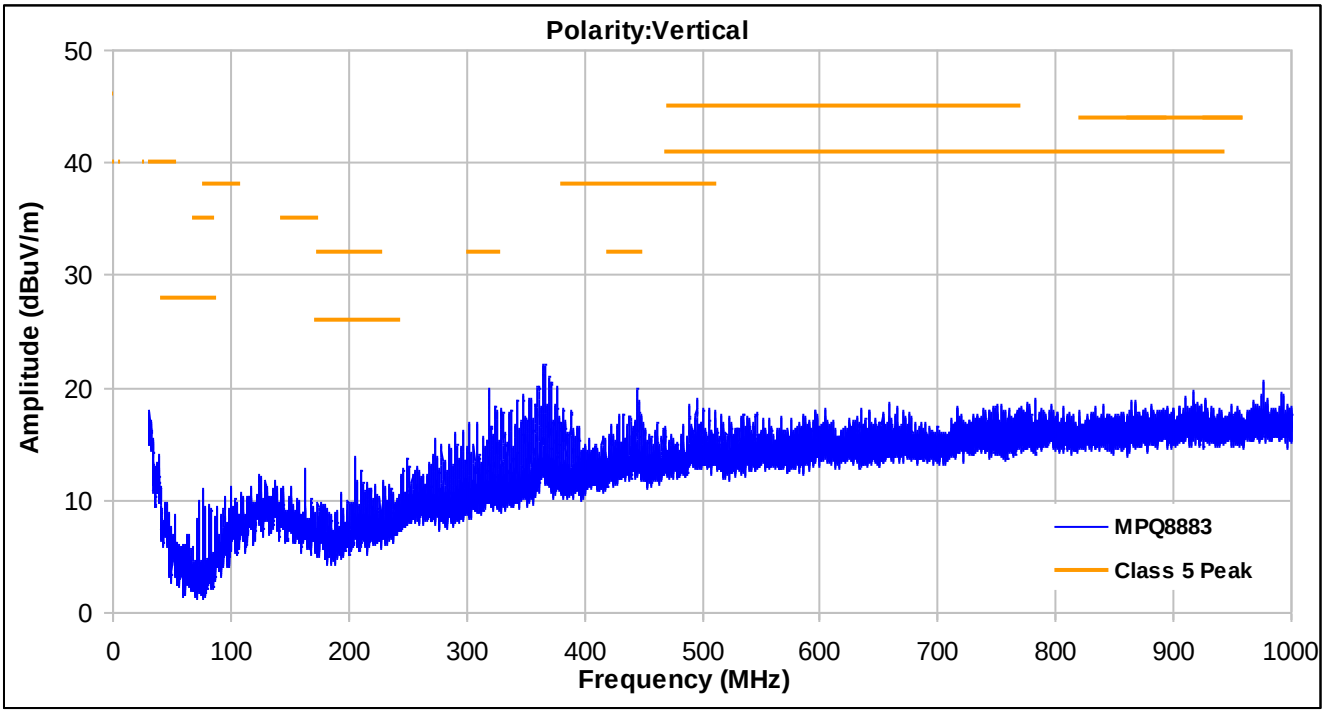
Load Dump
V_{IN}=12V<->36V, I_{OUT}=3A



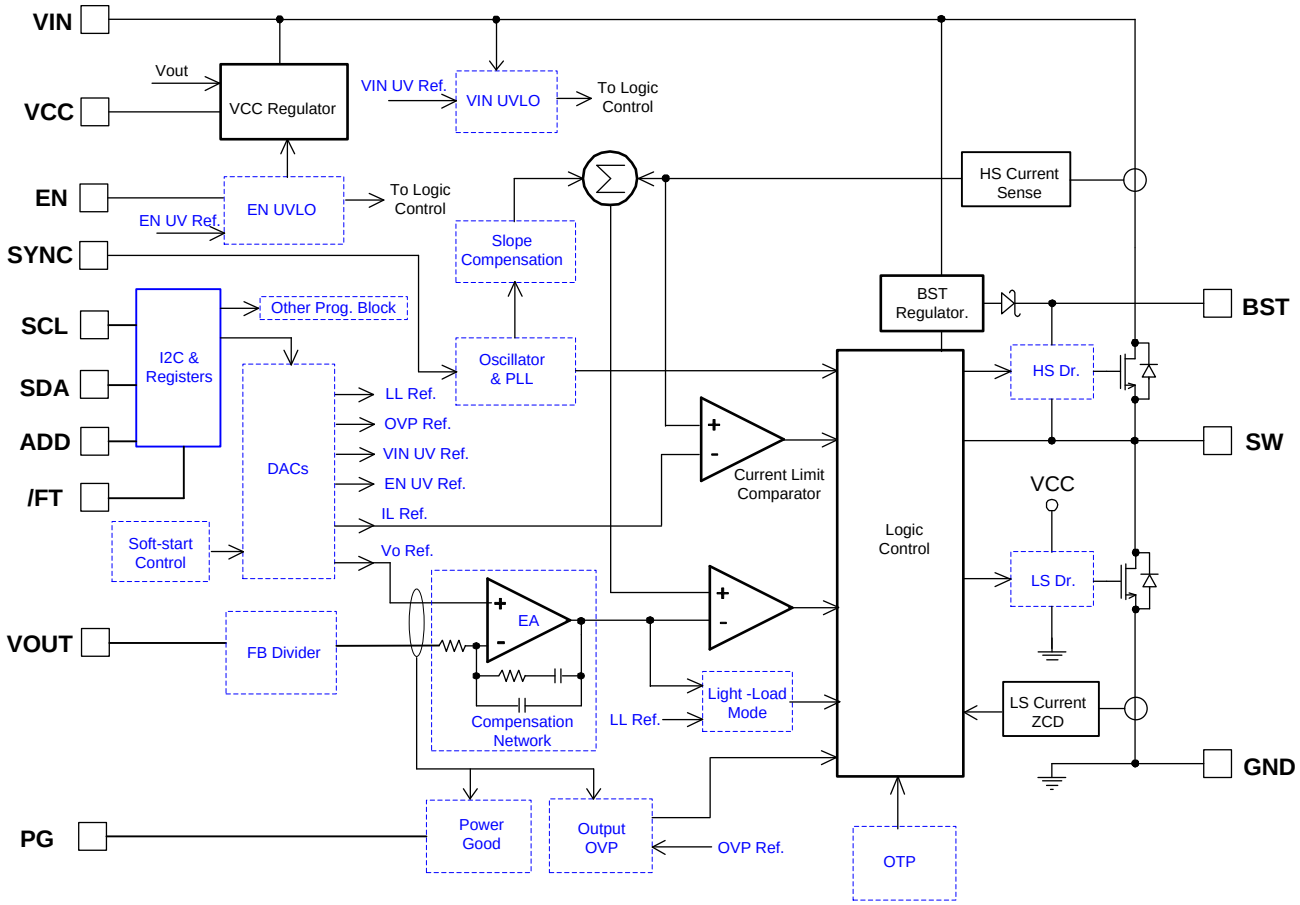
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT}=5V, L=10µH, I_{OUT}=2.5A, F_{SW}=2MHz, with the EMI filters, unless otherwise noted. (CISPR25 Radiated Emission Test with Class 5 Peak Limites)





FUNCTIONAL BLOCK DIAGRAM



The blocks with dashed boundary lines are programmable

Figure 2: Functional Block Diagram

OPERATION

The DIY8883 is a high frequency, synchronous step-down converter with built-in power MOSFETs. A block diagram of the device is shown in Figure 2. It is available with a wide 3.5V to 45V input supply range and can achieve up to 3A continuous output current with excellent load and line regulation over an ambient temperature range of -40°C to +125°C.

PWM Control

At moderate to high output current, the DIY8883 operates in a fixed frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. At the rising edge of the clock, the high-side switch (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until its current hits the COMP voltage, which is the output of the internal error amplifier. The output voltage of the error amplifier depends on the difference between the output feedback voltage and the internal high precision reference; it will decide how much energy should be transferred to the load. The higher the load current, the higher the COMP voltage. Both the feedback divider ratio and reference can be adjusted by the I^2C, which makes it easy to adjust different output voltages.

When the HS-FET is off, the low-side switch (LS-FET) will be turned on immediately and remains on until the next clock starts. During this time, the inductor current will flow through the LS-FET. In order to avoid a shoot-through issue, a dead time is inserted to avoid the HS-FET and LS-FET turning on at the same time.

If in one PWM period, the current in the HS-FET does not reach the COMP set current value, the HS-FET will remain on, saving a turn-off operation.

Mode Selection (AAM and Forced CCM)

The DIY8883 can work at light load AAM or forced CCM mode by the I^2C (see Figure 3). Advanced asynchronous modulation (AAM) mode is employed to optimize the efficiency during light-load or no-load conditions, while forced CCM can keep the switching frequency constant with a smaller output ripple. However, it has low efficiency at light load.

If AAM mode is enabled with the load decreasing, the DIY8883 will enter discontinuous conduction operation (DCM) first with a fixed frequency as long as the inductor current approaches zero. If the load decreases further, or there is no load, it will drive the inductor peak current lower than the AAM peak current threshold set by the I^2C. The DIY8883 will enter sleep mode consuming very low quiescent current to further improve the light-load efficiency. In sleep mode, the internal clock is blocked, thus the DIY8883 skips some pulses. The feedback voltage will be less than the reference, so V_{COMP} ramps up until the inductor peak current exceeds the AAM threshold. Then the internal clock will be reset, and the crossover time is taken as a benchmark for the next clock. This control scheme helps achieve high efficiency by scaling down the frequency to reduce the switching and gate driver losses.
As the output current increases from the light-load condition, V_{COMP} becomes larger, and the switching frequency increases. If the output current exceeds the critical level set by V_{COMP}, the DIY8883 resumes fixed frequency PWM control.

When forced CCM is enabled, the DIY8883 will operate in a fixed frequency peak-current-control mode to regulate the output voltage, regardless of the output current.

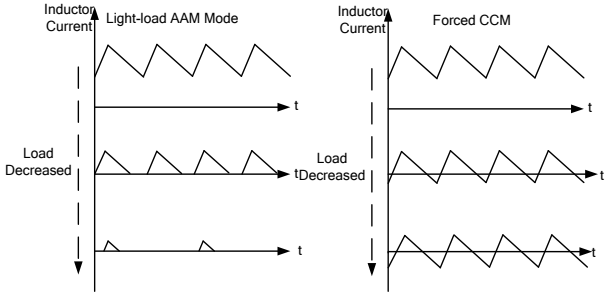


Figure 3: AAM and Forced CCM

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 5.0V, the output of the regulator is in full regulation. Lower values of V_{IN} result in lower output voltages. The regulator is enabled when V_{IN} exceeds its UVLO threshold and EN is

high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

For better thermal performance, BIAS mode can be chosen by the I²C if V_{OUT} is higher than 5V. Then VCC and the internal circuit will be powered by V_{OUT}.

Enable Control

EN is a digital control pin that turns the regulator, including the I²C block, on and off. Drive EN high to turn on the regulator; drive it low to turn it off. The EN threshold can be programmed by the I²C. An internal 5MΩ resistor from EN to GND allows EN to be floated to shut down the chip.

Oscillator Frequency

The default frequency of the DIY8883 is 500kHz, and it can be programmed from 300kHz to 2.5MHz by the I²C. Also, the frequency can be set by a logic level synchronal signal.

SYNC IN and SYNC OUT

SYNC can be programmed by the I²C to SYNC IN or SYNC OUT. When operating as SYNC IN, the internal oscillator frequency can be synchronized by an external clock via the SYNC pin. At start up, the DIY8883 will first operate at the internally set frequency, and quickly synchronize to the external clock once the soft start is ready. Ensure the high amplitude of the SYNC clock is higher than 1.8V, and the low amplitude is lower than 0.4V to drive the internal logic. The recommended external SYNC frequency is in the range of 250kHz and 2.5MHz.

The DIY8883 will operate in forced CCM mode with fixed frequency when there is a SYNC clock, regardless of the output current. A pulse longer than 200ns is recommended.

When SYNC is set to SYNC OUT, the DIY8883 can output the internal clock with a 0° or 180° phase shift. Using this function, the two devices can operate in the same frequency, but 180°out of phase, to reduce the total input current ripple, allowing a smaller input bypass capacitor.

Under-Voltage Lockout (UVLO)

The DIY8883 has input under-voltage lockout protection (UVLO) to ensure reliable output power. Assuming EN is active, the DIY8883 is powered on when the input voltage is higher than the UVLO rising threshold, and it is powered off when the input voltage drops below the UVLO falling threshold. The UVLO threshold can be set from 3.3V to 5.7V by the I²C. This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Soft Start

The DIY8883 has a built-in soft start (SS), which ramps up the output voltage in a controlled slew rate when EN goes high, avoiding overshoot during start-up. When the chip starts, the internal circuitry generates a soft-start voltage that ramps up slowly. When the SS voltage (V_{SS}) is lower than the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. At this point, the soft start finishes, and the DIY8883 enters steady state.

The SS time is set to a default 1ms internally. It can also be set to 0.5ms, 2ms, or 4ms by the I²C. When the output voltage is shorted to GND, the feedback voltage is pulled low, then V_{SS} is discharged. The part will soft start again when it returns to a normal state.

Pre-Bias Start-Up

At start-up, if the output feedback voltage is higher than V_{SS}, which means the output has pre-bias voltage, neither the high-side or low-side MOSFET will turn on until V_{SS} is higher than the feedback voltage.

Power Good Indicator

The DIY8883 has power good (PG) indication. The PG pin is the open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled to GND before the soft start is ready. When the output voltage is within a default ±10% window of the rated voltage, PG will be pulled high after a delay, typically 30μs. If V_{OUT} moves outside the default ±10% range with a hysteresis, the device pulls PG low to indicate a failure output status. Both the PG threshold and hysteresis can be programmed by the I²C.

FAULT Indicator

The /FT pin is also an open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). /FT will be pulled high during normal operation, and any fault or

warning will pull it down to indicate a fault status, including input OVP, output OVP, SCP, and thermal shutdown.

Over-Current Protection (OCP)

The DIY8883 has cycle-by-cycle over current limit control. The inductor current is monitored during the HS-FET on state. Once the inductor peak current exceeds the set current limit threshold, the HS-FET will be turned off immediately. Then the LS-FET will be turned on to discharge the energy, and the inductor current will decrease. The HS-FET will not be on again until the inductor current is lower than a certain current threshold, which is the valley current limit. Aim to prevent the inductor current from running away and possibly damaging the components. Both the peak current and valley current threshold can be programmed by the I^2C.

When the peak current limit is triggered, the OCP timer will start immediately. The OCP timer can be set to 32, 64, 128, or 256 cycles by the I^2C. Hitting the current limit during each cycle during this OCP timer will trigger SCP operation (hiccup as default).

Short-Circuit Protection (SCP)

When a short circuit occurs, the DIY8883 will hit its current limit immediately. Meanwhile, the output voltage will drop quickly to the under-voltage threshold—default 50% of the set output. Then the device will consider this an output dead short and will trigger SCP operation immediately. There are 3 modes which can be selected by the I^2C for SCP operation: hiccup as default, switching with non-hiccup, and latch off.

In default hiccup mode, the DIY8883 disables its output power stage first and resets the soft-start voltage. Then it initiates a soft-start procedure. The off time is decided by the soft-start time and the hiccup duty, which both can be set by the I^2C. If the short-circuit condition still holds after the soft start ends, the device will repeat this operation until the short circuit disappears, and the output returns to the regulation level. This protection mode greatly reduces the average short-circuit current by periodically restarting the part to alleviate thermal issues and protect the regulator.

Output Over-Voltage Protection (VOUT OVP)

The DIY8883 monitors the output voltage through the VOUT pin to detect output over-voltage conditions. When the output voltage exceeds the OVP threshold—default 120% of the set voltage, the OVP mode is triggered. There are 3 modes which can be selected by the I^2C for OVP operation: disable as default, discharge, and latch off.

Input Over-Voltage Protection (VIN OVP)

The DIY8883 also has optional input OVP. The threshold can be set to 28V, 34V, or 40V. If VIN exceeds the threshold, the DIY8883 will stop switching. This is a non-latch protection, and there is a hysteresis of either 2.5% or 5% of the input OVP threshold voltage. The device will return to normal operation when the input OVP is removed. Both the input OVP threshold and the hysteresis can be set by the I^2C interface.

Thermal Shutdown

The DIY8883 has over-temperature protection (OTP) by monitoring the IC temperature internally. This function prevents the chip from operating at an exceedingly high temperature. If the junction temperature exceeds the threshold—default 175°C, it shuts down the whole chip. This is a non-latch protection, and there is a default 25°C hysteresis. Once the junction temperature drops to about 150°C, the device resumes operation by initiating a soft start. Both the OTP threshold and hysteresis can be set by the I^2C interface.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. The floating driver has its own UVLO protection with a rising threshold of 2.5V and a hysteresis of 200mV.

The bootstrap capacitor voltage is charged to ~5V from VCC through a PMOS pass transistor when the LS-FET is on.

At high duty cycle operation or a sleep mode condition, the time period available to the bootstrap charging is shorter, so the bootstrap capacitor may not be charged sufficiently. If the external circuit does not have sufficient voltage and not enough time to charge the bootstrap capacitor, extra external circuitry can be used to

ensure the bootstrap voltage is in a normal operation range.

Low Dropout Operation (BST Refresh)

To improve drop out, the DIY8883 is designed to operate at close to 100% duty cycle as long as the BST to SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the high-side MOSFET is turned off using an UVLO circuit, which allows the low-side MOSFET to conduct and refresh the charge on the BST capacitor.

In cases where the input voltage drops, the HS-FET remains on and close to 100% duty cycle to maintain the output regulation until the BST to SW voltage falls below 2.5V. Since the supply current sourced from the BST capacitor is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is influenced mainly by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and printed circuit board resistance.

I²C Control and Default Output Voltage

When the DIY8883 is enabled, which means EN=high and VIN>UVLO, the chip starts up to a default 5V output voltage. After that, the I²C bus can communicate with the master. Once the I²C receives valid output voltage setting instructions, the output voltage will be determined by the I²C control.

The output voltage setting is achieved by adjusting the internal reference voltage and the output feedback divider ratio. After the DIY8883 receives a valid data byte of the output voltage setting, it searches the corresponding value from the truth table and then sends the command to adjust the reference and divider ratio to the correct voltage.

Frequency Dithering for Low EMI

Frequency dithering is used to reduce EMI, especially for EMI-sensitive applications. This spread-spectrum modulation technique spreads the frequency spectrum of the converter, which in turn will spread the energy of the switching harmonics over a wider band while reducing their amplitudes, helping to meet stringent EMI goals.

The programmable frequency dithering feature of the DIY8883 allows either a 3/48 or 3/28 variation range in the switching frequency, with a 120µs or 150µs dithering cycle. Both the frequency dithering range and the cycle can be set by the I²C interface.

Multipage One-Time Programmable Memory

The DIY8883 features 3 pages of one-time programmable memory to store desired settings permanently.

A differential one-time programmable cell, instead of a single ended cell, is used for long-term reliability. Data is stored on two floating gate avalanche injection metal oxide semiconductors (FAMOS), and output comparators are used for the differential reading.

The first page of the multipage one-time programmable memory has been programmed with manufacturer default values.

Once the device is enabled, the default values on the first page are used to set the control parameters in the registers. If there is data on other pages of the one-time programmable memory, the newest setting is identified by an internal indicator to the write registers. Refer to the Register Map and Register Description sections for details.

I²C INTERFACE

I²C Serial Interface Description

I²C is a 2-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are “idle.” Connecting to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The DIY8883 interface is an I²C slave, which will support both fast mode (400kHz), and typically, high speed mode (3.4MHz), adding flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters, can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 4).

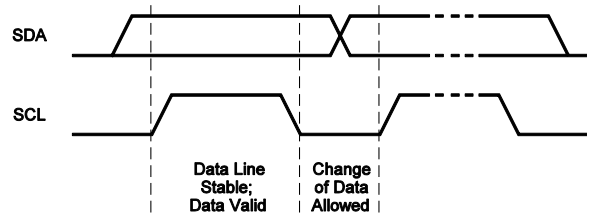


Figure 4: Bit Transfer on the I²C Bus

Start and Stop Conditions

The Start and Stop conditions are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The Start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The Stop condition is defined as the SDA signal transitioning from low to high while the SCL is high as shown in Figure 5.

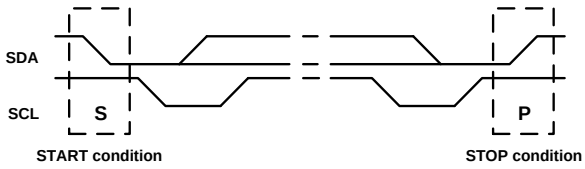


Figure 5: Start and Stop Conditions

Start and Stop conditions are always generated by the master. The bus is considered busy after the Start condition. The bus is considered free after a minimum of 4.7µs after the Stop condition. The bus stays busy if a repeated Start (Sr) is generated instead of a Stop condition. The Start (S) and repeated Start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Data transfers follow the format shown in Figure 6. After the Start condition (S), a slave address is sent. This address is 7-bits long followed by an eighth bit, which is a data direction bit (R/W). A ‘0’ indicates a transmission (write), and a ‘1’ indicates a request for data (read). A data transfer is always terminated by a Stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated Start condition (Sr) and address another slave without first generating a stop condition.

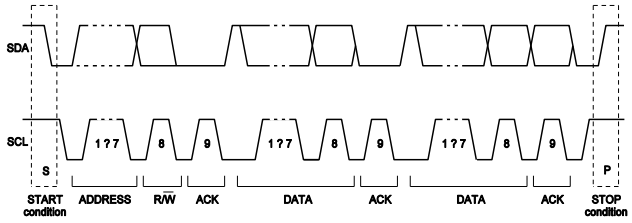


Figure 6: A Complete Data Transfer

I²C Update Sequence

The DIY8883 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receipt of each byte, the DIY8883 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the DIY8883. The DIY8883 performs an update on the falling edge of the LSB byte.

DIY8883 I²C Chip Address

The ADD pin can be used to program the I²C address. The DIY8883 supports 7 addresses for up to 7 voltage rails through configuring the resistor value connected between ADD and ground. When the master sends the address as an 8-bit value, the 7-bit address should be followed by “0/1” to indicate write/read operation.

Table 1 shows the resistor values for different I²C addresses.

Table 1: I²C Address

Resistor (kΩ) 1%	Address
0	21h
12.5+25	22h
12.5+50	23h
12.5+75	24h
12.5+100	25h
12.5+125	26h
12.5+150	27h

REGISTER DESCRIPTION

Register Map

ADD	R/W	D7	D6	D5	D4	D3	D2	D1	D0
D0	R/W	Reference Voltage (DAC)							
D1	R/W	Frequency Dithering (EN/disable)	Frequency Dithering (Dithering range)	Frequency Dithering (Dithering cycle)	Input OVP Hysteresis	Input OVP Threshold		FB Divider Ratio	
D2	R/W	NA	Phase Shift	Switching Frequency					
D3	R/W	Compensation, Ccomp2		Compensation, Rt			Compensation, Rcomp		
D4	R/W	Soft-Start Time		Slope Compensation			Compensation, Ccomp1		
D5	R/W	NA	EN Rising Threshold		EN Rising Hysteresis	VIN UVLO Rising Threshold			VIN UVLO Hysteresis
D6	R/W	SCP Mode		Peak Current Limit Threshold			Valley Current Limit Threshold		NA
D7	R/W	OTP Rising Threshold		OTP Hysteresis	Output OVP Mode		Output OVP Rising Threshold		Output OVP Hysteresis
D8	R/W	PG Lower Hysteresis	PG Lower Rising Threshold	PG Upper Hysteresis	PG Upper Rising Threshold	SCP Detecting Time		SCP Triggered FB Voltage	NA
D9	R/W	/FT Setting	NA	Hiccup Duty	Switching Slew Rate (falling)		Switching Slew Rate (rising)		NA
DA	R/W	NA							AAM/CCM
DB	R/W	AAM Threshold				PKC	VOUT BIAS		NA

Register Description

Register Description	Addr	Bits	Default Code	Default Value	Range/Values	Min Value	Max Value	Resolution /LSB	Units
Reference Voltage (DAC)	**D0**	D[7:0]	01100100	1	0.6V to 2.55V	0.60	2.55	0.01	V
FB Divider Ratio	**D1**	D[1:0]	01	1/5	1/5, 1/2, 1	1/5	1		
Input OVP Threshold	**D1**	D[3:2]	00	No OVP	No OVP, 28V, 34V, 40V	28	40		V
Input OVP Hysteresis	**D1**	D[4]	1	5%	2.5%, 5%	2.5%	5%		VIN
Frequency Dithering(cycle)	**D1**	D[5]	1	150	120, 150	120	150		µs
Frequency Dithering(range)	**D1**	D[6]	1	3/28	3/48, 3/28	3/48	3/28		f_{SW}
Frequency Dithering	**D1**	D[7]	0	Disable	Enable, Disable				
Switching Frequency	**D2**	D[5:0]	001010	500	250 to 2500	250	2500	50	kHz
Phase shift	**D2**	D[6]	0	0	0, 180 degree	0	180		°
Reserved	**D2**	D[7]	0	NA					
Compensation, Rcomp	**D3**	D[2:0]	011	700	400, 500, 600, 700, 800, 900, 1000, 1100	400	1100		kΩ
Compensation, Rt	**D3**	D[5:3]	011	60	0, 20, 40, 60, 80, 100, 120, 140	0	140		kΩ
Compensation, Ccomp2	**D3**	D[7:6]	00	0.5	0.5				pF
Compensation, Ccomp1	**D4**	D[2:0]	000	40	40, 45	40	45		pF

Register Description *(continued)*

Register Description	Addr	Bits	Default Code	Default Value	Range/Values	Min Value	Max Value	Resolution /LSB	Units
Slope Compensation	**D4**	D[5:3]	000	750	300, 450, 600, 750, 900, 1050, 1200	300	1200		mV
Soft-Start Time	**D4**	D[7:6]	01	1	0.5, 1, 2, 4	0.5	4		ms
VIN UVLO Hysteresis	**D5**	D[0]	1	4%	2%, 4%	2%	4%		V_{UVLO_TH}
VIN UVLO Rising Threshold	**D5**	D[3:1]	000	3.3	3.3, 3.9, 4.5, 5.1, 5.7, 6.3, 6.9, 7.5	3.3	7.5		V
EN Rising Hysteresis	**D5**	D[4]	0	200	200, 400	200	400		mV
EN Rising Threshold	**D5**	D[6:5]	01	1.2	1.2, 1.4,1.6, 2	1.2	2		V
Reserved	**D5**	D[7]	0	NA					
Reserved	**D6**	D[0]	0	NA					
Valley Current Limit Threshold	**D6**	D[2:1]	10	3.5	1.5, 2.5, 3.5, 4.5	1.5	4.5		A
Peak Current Limit Threshold	**D6**	D[5:3]	000	5	2, 3, 4, 5, 6, 7, 8	2	8		A
SCP Mode	**D6**	D[7:6]	00	Hiccup	Hiccup, Switching with Non-hiccup, Latch				
Output OVP Hysteresis	**D7**	D[0]	0	5%	2.5%, 5%	2.5%	5%		V_{OUT_SET}
Output OVP Rising Threshold	**D7**	D[2:1]	01	120%	110%, 120%, 130%	110%	130%		V_{OUT_SET}
Output OVP Mode	**D7**	D[4:3]	01	Stopping switching	Latch, Discharge, Stopping switching				
OTP Hysteresis	**D7**	D[5]	0	25	25, 50	25	50		°C
OTP Rising Threshold	**D7**	D[7:6]	10	175	125, 150, 175	125	175		°C
Reserved	**D8**	D[0]	0	NA					
SCP Triggered FB Voltage	**D8**	D[1]	0	50%	50%, 75%	50%	75%		V_{REF}
SCP Detecting Time	**D8**	D[3:2]	01	128	32, 64, 128, 256	32	256		T_{SW}
PG Upper Rising Threshold	**D8**	D[4]	0	110%	110%, 115%	110%	115%		V_{OUT_SET}
PG Upper Hysteresis	**D8**	D[5]	0	5%	2.5%, 5%	2.5%	5%		V_{OUT_SET}
PG Lower Rising Threshold	**D8**	D[6]	0	90%	85%, 90%	85%	90%		V_{OUT_SET}
PG Lower Hysteresis	**D8**	D[7]	0	5%	2.5%, 5%	2.5%	5%		V_{OUT_SET}
Reserved	**D9**	D[0]	0	NA					
Switching Slew Rate (rising)	**D9**	D[2:1]	01	2	1, 2, 3, 4	1	4		V/ns
Switching Slew Rate (falling)	**D9**	D[4:3]	01	2	1, 2, 3, 4	1	4		V/ns
Hiccup Duty (On time)	**D9**	D[5]	0	10%	10%, 20%	10%	20%		
/FT setting	**D9**	D[7]	1	Auto Reset	Auto reset when Fault removed, need EN restart				

					to reset the Fault status				
AAM/CCM control	**DA**	D[0]	0	AAM	AAM, CCM				
Reserved	**DA**	D[7:1]	0101000	NA					
Reserved	**DB**	D[0]	0	NA					
VOUT BIAS	**DB**	D[2:1]	01	BIAS	No BIAS, BIAS, BIAS in sleep only				
PKC	**DB**	D[3]	1	PKC	PKC				
AAM Threshold (PKC)	**DB**	D[7:4]	1000	530	Disable, 0, 75, 150, 225, 305, 380, 455, 530, 605, 680, 755, 830, 905, 980, 1055	0	1055		mA

APPLICATION INFORMATION

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, use a 4.7µF to 10µF capacitor. It is strongly recommended to use another lower value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high frequency switching noise. Make sure to place the small sized capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (1):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (1)$$

The worst case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (2):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (2)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (3):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (4):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \cdot (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (4)$$

Where L is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (5):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (6)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The DIY8883 can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A DC current rating at least 25% higher than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with lower DC resistance. A larger value inductor results in less ripple current and a lower output ripple voltage. However, the larger value inductor also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance value can be calculated with Equation (7):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

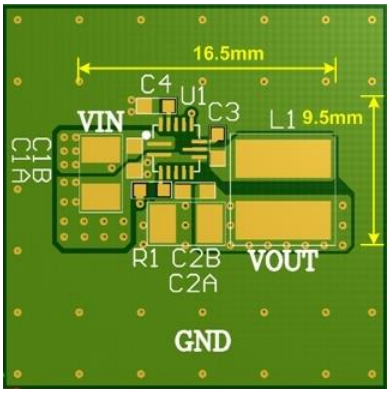
Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (8):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

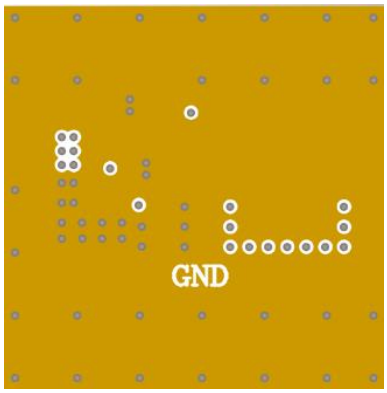
PCB Layout Guidelines

PCB layout is critical for stable operation. For best results, refer to Figure 7 and follow the guidelines below: (7) (8)

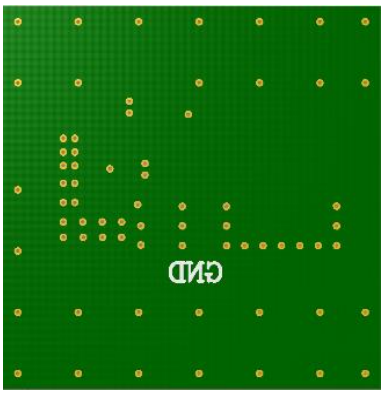
1. Keep the power loop of the input capacitors (HS switch and LS switch) as small as possible.
2. Use a large ground plane to connect directly to PGND. If the bottom layer is a ground plane, add vias near PGND.
3. Ensure the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor (especially the small package size (0603) input bypass capacitor) as close to VIN and PGND as possible to minimize high frequency noise. Keep the input capacitor and IN as short and wide as possible.
5. Place the VCC capacitor as close as possible to VCC and GND.
6. Route SW and BST away from sensitive analog areas.
7. Connect VIN, SW, VOUT, and GND to a large copper area to cool the chip and improve thermal performance and long-term reliability.
8. Separate the input GND from other GND areas on the top layer, and connect them at internal layers and the bottom layer through multiple vias.
9. Ensure an integrated GND is on the internal layer or bottom layer.
10. A four-layer layout is recommended to achieve better thermal performance. Use multiple vias to connect the power planes to the internal layers.



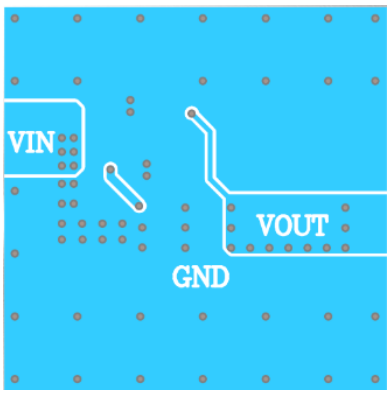
Top Layer



Inner2 Layer



Inner1 Layer



Bottom Layer

Figure 7: Recommended PCB Layout

Notes:

8) This layout covers a full range of specs. A much smaller layout size can be achieved for specific cases, like higher switching frequency, lower input voltage, or output current by selecting smaller packages of inductors and capacitors.
9) Please refer to Figure 8 as a corresponding schematic

TYPICAL APPLICATION CIRCUITS

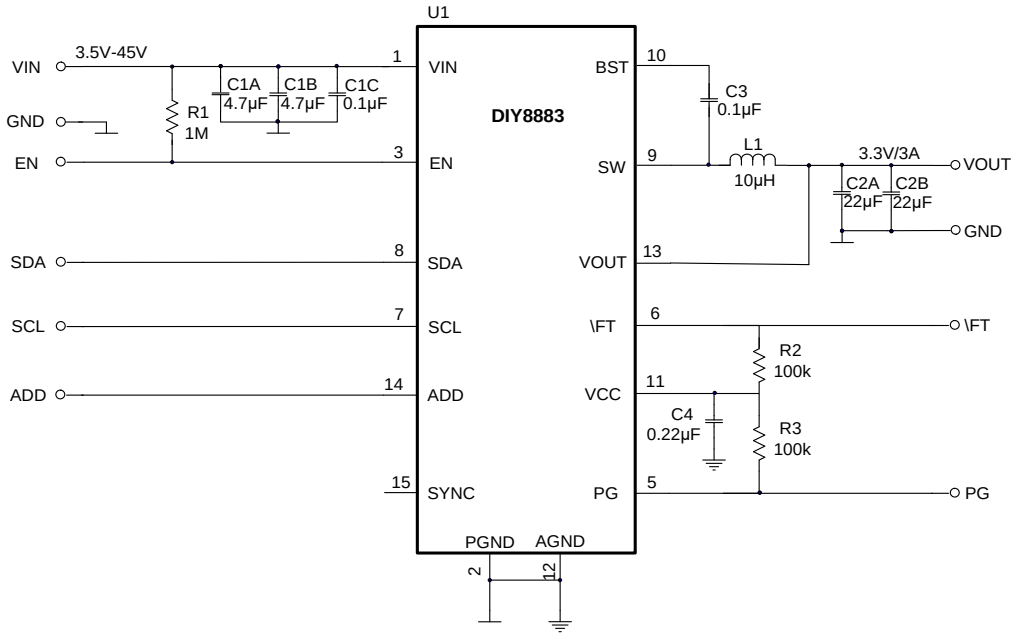
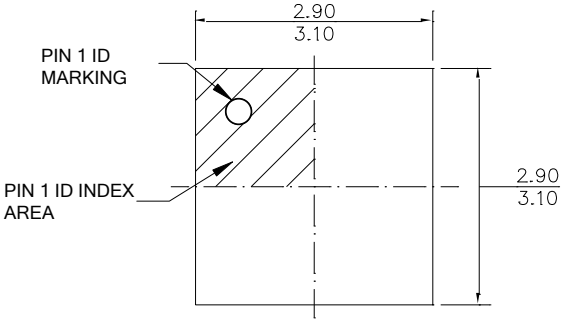


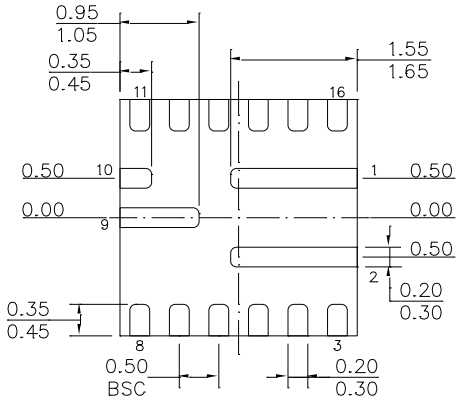
Figure 8:Application Circuit for V_{OUT} = 3.3V, I_{OUT} = 3A

PACKAGE INFORMATION

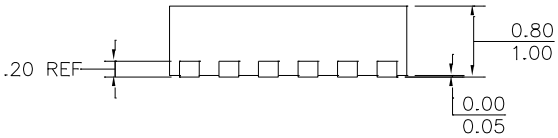
QFN16 (3mmx3mm)



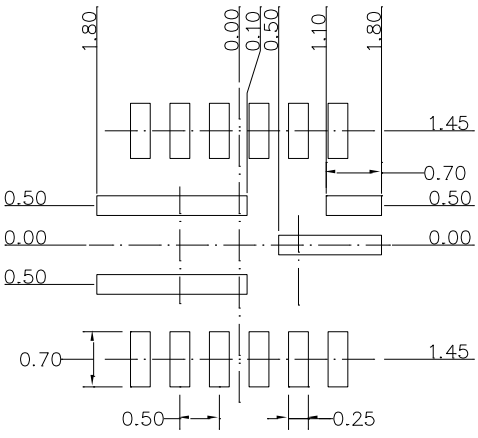
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.