

DESCRIPTION

The EV020-5-S-00C Evaluation Board is designed to demonstrate the capabilities of MP020-5. The MP020-5 is a primary-side-control regulator which can eliminates secondary feedback components.

The EV020-5-S-00C is typically designed for small appliances which output 12V/0.3A and 5V/0.1A load from 85VAC to 265VAC, 50HZ/60HZ.

The EV020-5-S-00C has an excellent efficiency and meets IEC61000-4-5 surge immunity and EN55022 conducted EMI requirements. It has multi-protection function as open circuit protection, short-circuit protection, cycle by cycle current limit and over-temperature protection, etc.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	85 to 265	VAC
Output Voltage 1	V_{OUT1}	12	V
Output Current 1	I_{OUT1}	0.3	A
Output Voltage 2	V_{OUT2}	5	V
Output Current 2	I_{OUT2}	0.1	A
Output Power	P_{OUT}	4.1	W
Efficiency (full load)	η	>70	%

FEATURES

- Primary-Side—Control without Opto-Coupler or Secondary Feedback Circuit
- Precise Constant Voltage Control (CV)
- Integrated 700V MOSFET with Minimal External Components
- Variable, Off-Time, Peak-Current Control
- 550 μ A High-Voltage Current Source
- Programmable Cable Compensation (By adding 1 μ F/25V ceramic cap at CP pin)
- Multiple Protections: OVP, OCP, OCKP, OTP, and VCC UVLO
- Natural Spectrum Shaping for Improved EMI Signature
- Low Cost and Simple External circuit

APPLICATIONS

- Small Appliances

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology", are Registered Trademarks of Monolithic Power Systems, Inc.



Warning: Although this board is designed to satisfy safety requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Board Number	MPS IC Number
EV020-5-S-00C	MP020-5GS

EVALUATION BOARD SCHEMATIC

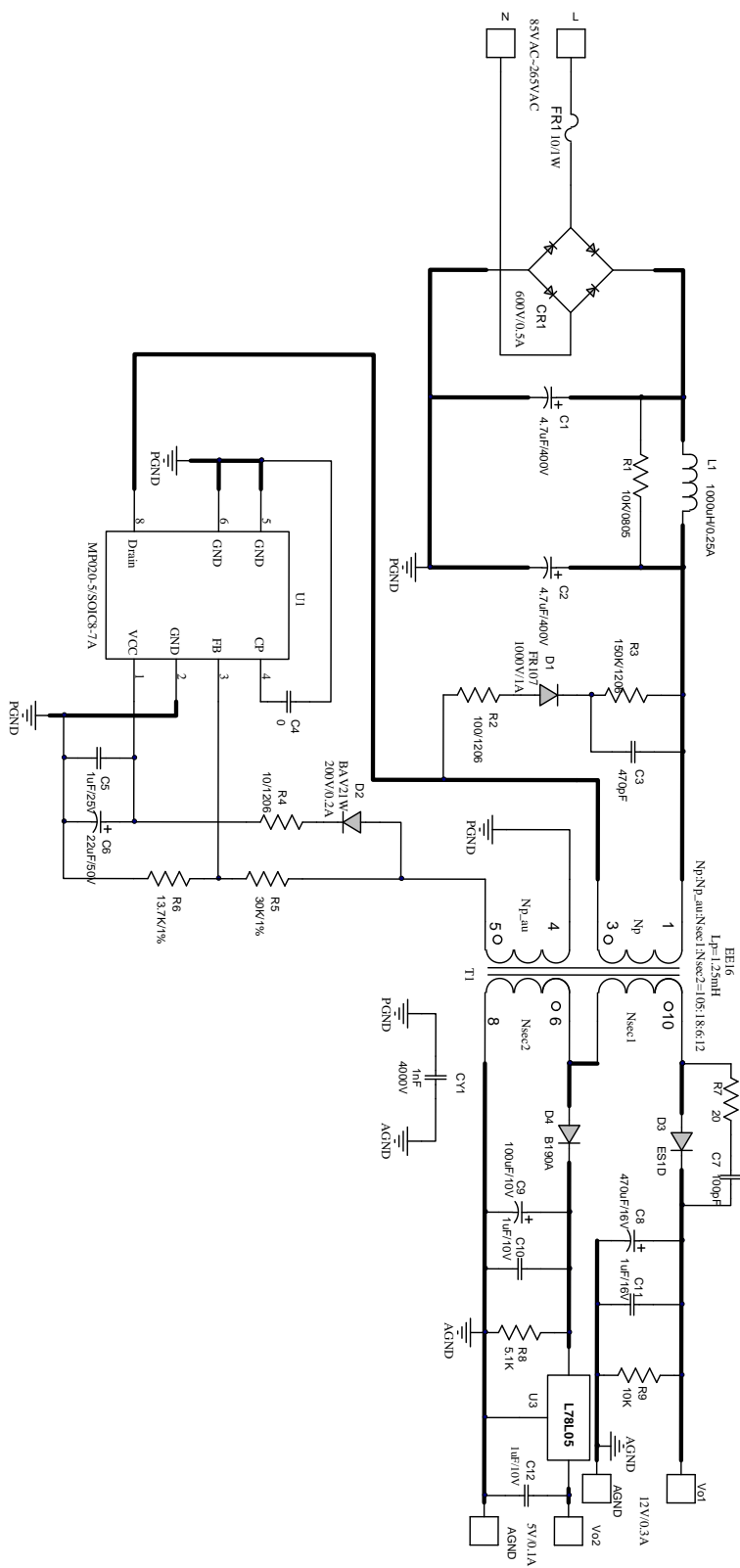


Figure 1—Schematic

PCB LAYOUT (SINGLE-SIDED)

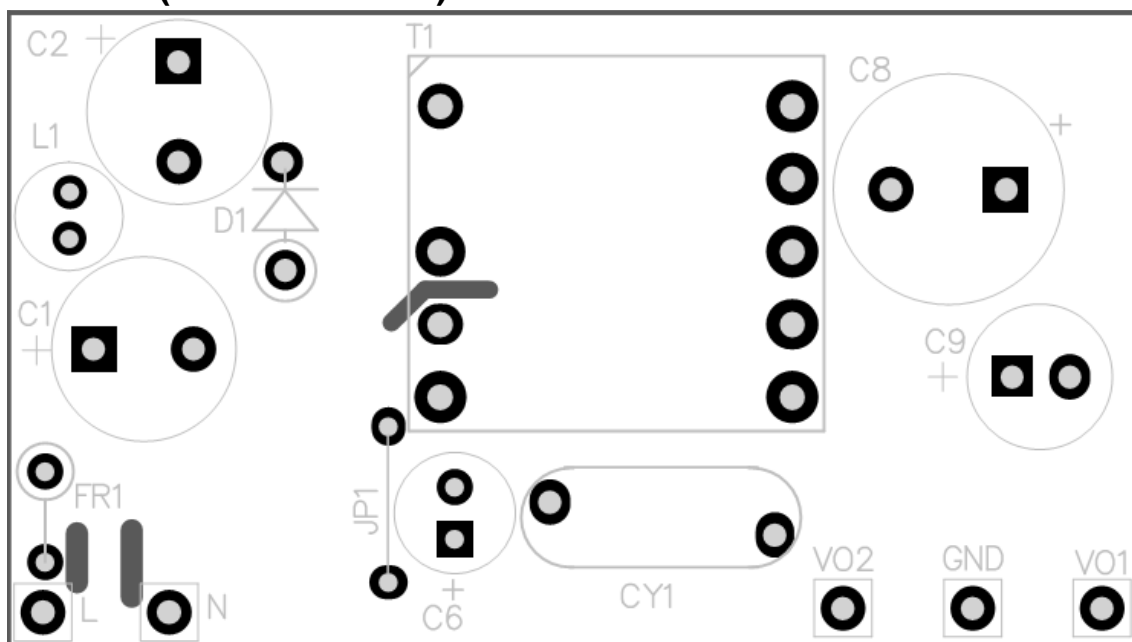
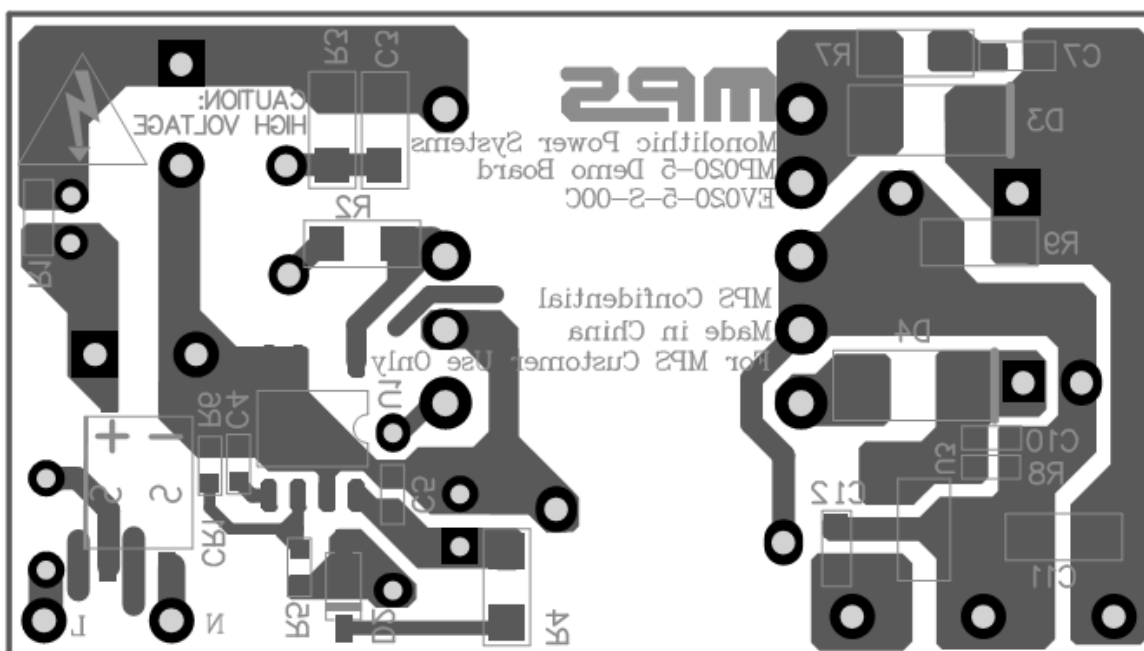


Figure 2—Top Layer



CIRCUIT DESCRIPTION

The EV020-5-S-00C is configured in a single-stage Flyback topology, it uses primary-side-control which can mostly simplify the schematic and get a cost effective BOM. It can also achieve accurate constant voltage and acceptable cross regulation.

FR1 and CR1 compose the input stage. FR1 is used to protect for the component failure or some excessive short events, also it can restrain the inrush current.

C1, L1 and C2 compose π filter to guarantee the conducted EMI meet standard EN55022. R1 paralleled with L1 is used to damp resonant between L1 and C1, C2. R2, R3, D1 and C3 compose the snubber circuit to reduce drain-source voltage spike.

R4, C5, C6 and D2 are used as Vcc power supply. C5 is high frequency decoupling capacitor and should be placed with Vcc pin as near as possible.

R5 and R6 are resistor divider for detecting output voltage by sampling voltage on primary auxiliary winding.

CY1 is Y capacitor lowering common mode noise to make sure there is enough EMI margin. T1 is power transformer, the structure of which is also very important to pass EMI test.

D3 is rectifier for 12V output. Schottky diode is recommended for better efficiency and regulation. C7 and R7 are composed snubber for D3, which is to restrain the voltage spike between D3.

C8 and C11 are output capacitors for 12V output. C8 should be low ESR electrolytic capacitor for better load regulation. C11 is ceramic capacitor to reduce high frequency voltage ripple. R9 is dummy load to lower the output voltage of 12V rail at no load condition.

D4 is rectifier for 5V output. Schottky diode is recommended for better efficiency and regulation. Due to the output current is low at this rail and there is no obvious spike on D4, so no RC snubber is needed.

C9 and C10 are output capacitors for 5V output. C9 should be low ESR electrolytic capacitor for better load regulation. C10 is ceramic capacitor to reduce high frequency voltage ripple. R8 is dummy load to lower the output voltage of 5V rail at no load condition.

U3 is three terminals voltage regulator for precise 5V output. C12 is output capacitor for U3.

EV020-5-S-00C BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer_P/N
2	C1, C2	4.7μF	Capacitor;400V;20%	DIP	Beryl	4.7μF/400V
1	C3	470pF	Ceramic Capacitor; 1000V;U2J;	1206	muRata	GRM31B7U3A471JW31L
1	C4	0Ω	Shorted with 0Ω resistor	0603	Yageo	RC0603JR-070RL
1	C5	1μF	Ceramic Capacitor; 25V;X7R;	0603	muRata	GRM188R71E105KA12D
1	C6	22μF	Electrolytic Capacitor; 50V;Electrolytic;	DIP	Jianghai	CD281L-50V22
1	C7	100pF	Ceramic Capacitor; 250V;COG	0805	Murata	GRM21A5C2E101JW01D
1	C8	470μF	Electrolytic Capacitor; 16V;Electrolytic;	DIP	Lelon	RXW471M1CBK-1012P
1	C9	100μF	Electrolytic Capacitor; 10V;Electrolytic;	DIP	Lelon	RXW101M1ABK-0511P
2	C10, C12	1μF	Ceramic Capacitor; 10V;X7R	0603	Murata	GRM188R71A105KA61D
1	C11	1μF	Ceramic Capacitor; 25V;X7R;	1206	TDK	C3216X7R1E105K
1	CR1	MB6F	Diode;600V;0.5A	SOP-4	Taiwan Semiconductor	MB6F
1	CY1	1nF	Y Capacitor;4000V;20%	DIP	Hongke	JN09E102MY02N
1	D1	FR107	Diode;1000V;1A	DO-41	Diodes	FR107
1	D2	BAV21W	Diode;200V;0.2A;	SOD-123	Diodes	BAV21W-7-F
1	D3	ES1D	Diode;200V;1A;	SMA	Taiwan Semiconductor	ES1D
1	D4	B190A	Schottky Diode;90V;1A;	SMA	Diodes	B190A
1	FR1	FKN1WSJT -52-10R	Fusible Resistor ;10Ω/1W	DIP	Yageo	FKN1WSJT-52-10R
1	L1	1000μH/ 0.25A	Inductor;1000μH;6 Ohm;0.25A	DIP	Wurth	7447462102
1	R1	10kΩ	Film Resistor;5%;	0805	Yageo	RC0805JR-0710KL
1	R2	100Ω	Film Resistor;5%;1/4W	1206	Yageo	RC1206JR-07100RL
1	R3	150kΩ	Film Resistor;1%;	1206	Panasonic	ERJ8ENF1503V
1	R4	10Ω	Film Resistor;5%	1206	Yageo	RC1206JR-0710R
1	R5	30kΩ	Film Resistor;1%;	0603	Yageo	RC0603FR-0730KL
1	R6	13.7kΩ	Film Resistor;1%	0603	Yageo	RC0603FR-0713K7L
1	R7	20Ω	Film Resistor;5%;1/4W	1206		1206J0200T5E
1	R8	5.1kΩ	Film Resistor;5%;	0603	Yageo	RC0603JR-075K1L
1	R9	10kΩ	Resistor;5%;	1206	Yageo	RM12JTN103
1	T1		EE16 Transformer, Lp=1.25mH Np:Np_au:Nsec1:Nsec2= 105:18:6:12	EE16		FX0295
1	U1	MP020-5	Primary Side Regulator	SOIC8-7A	MPS	MP020-5GS R3
1	U3	L78L05	Three-Terminal Voltage Regulator	SOT-89	STMicroelectronics	L78L05ACUTR

TRANSFORMER SPECIFICATION

Electrical Diagram

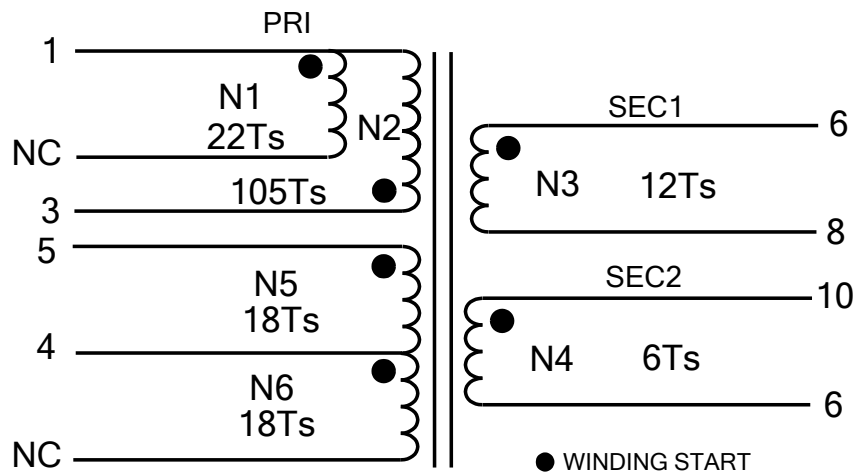


Figure 4—Transformer Electrical Diagram

Notes:

1. N1 is with 2 wires which are paralleled together.
2. N3 and N4 are both triple insulation wires.
3. One layer tape is between each layer winding. 3 layers tape is at the outside of last winding

Winding Diagram

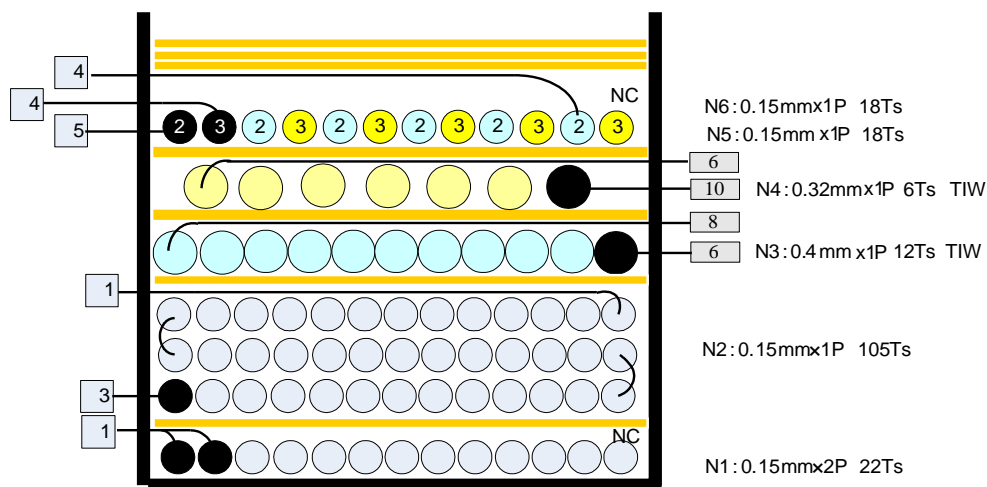


Figure 5—Winding Diagram

Winding Order

Tapes (T)	Winding	Start-End	Wire Diameter (Ø)	Turns (T)	Tube
0	N1	1—> NC	0.15mm*2	22	None
1		3—> 1	0.15mm*1	105	None
1	N2	6—> 8	0.4mm*1 TIW	12	None
1	N3	10—> 6	0.32mm*1 TIW	6	None
3	N4	5—> 4	0.15mm*1	18	None
	N5, N6	4—> NC	0.15mm*1	18	

Electrical Specifications

Electrical Strength	60 second, 60Hz, from PRI. to SEC.	3000VAC
	60 second, 60Hz, from PRI. to CORE.	500VAC
	60 second, 60Hz, from SEC. to CORE.	3000VAC
Primary Inductance	Pins 1 - 3, all other windings open, measured at 60kHz, 0.1 VRMS	1.25mH±10%
Primary Leakage Inductance	Pins 1 - 3 with all other pins shorted, measured at 60kHz. 0.1 VRMS	50µH±10%

Materials

Item	Description
1	Core: EE16, UI=2300±25%, AL=73.2nH/N ² ±3% GAPPED, or equivalent
2	Bobbin: EE16, 5+5PIN 1 SECT TH, UL94V-0
3	Wire:Φ0.15mm,, 2UEW, Class B
4	Triple Insulation Wire: Φ0.40mm, TIW
5	Triple Insulation Wire: Φ0.32mm TIW
6	Tape: 8.0mm(W)×0.06mm(TH)
7	Varnish: JOHN C. DOLPH CO, BC-346A or equivalent
8	Solder Bar: CHEN NAN: SN99.5/Cu0.5 or equivalent

EVB TEST RESULTS

Performance Data

Ta=25°C, unless otherwise noted.

Efficiency and Load/Line Regulation (Test at the end of board)

	Pin (W)	V _{OUT1} (V)	I _{OUT1} (A)	V _{OUT2} (V)	I _{OUT2} (A)	Efficiency	V _{OUT1} Regulation	V _{OUT2} Regulation
Vin=85Vac/60Hz	0.06293	11.9	0	5	0	0.00%	-0.83%	0.00%
	5.5626	11.75	0.3	5	0.1	72.36%	-2.08%	0.00%
	1.4909	11.89	0.03	5	0.1	57.46%	-0.92%	0.00%
	0.56577	11.72	0.03	5	0.005	66.56%	-2.33% Δ	0.00%
	4.5994	11.79	0.3	5	0.005	77.44%	-1.75%	0.00%

	Pin (W)	V _{OUT1} (V)	I _{OUT1} (A)	V _{OUT2} (V)	I _{OUT2} (A)	Efficiency	V _{OUT1} Regulation	V _{OUT2} Regulation
Vin=115Vac/60Hz	0.06221	11.89	0	5	0	0.00%	-0.92%	0.00%
	5.4373	11.76	0.3	5	0.1	74.08%	-2.00%	0.00%
	1.4935	11.89	0.03	5	0.1	57.36%	-0.92%	0.00%
	0.5646	11.72	0.03	5	0.005	66.70%	-2.33% Δ	0.00%
	4.5104	11.72	0.3	5	0.005	78.51%	-2.33% Δ	0.00%

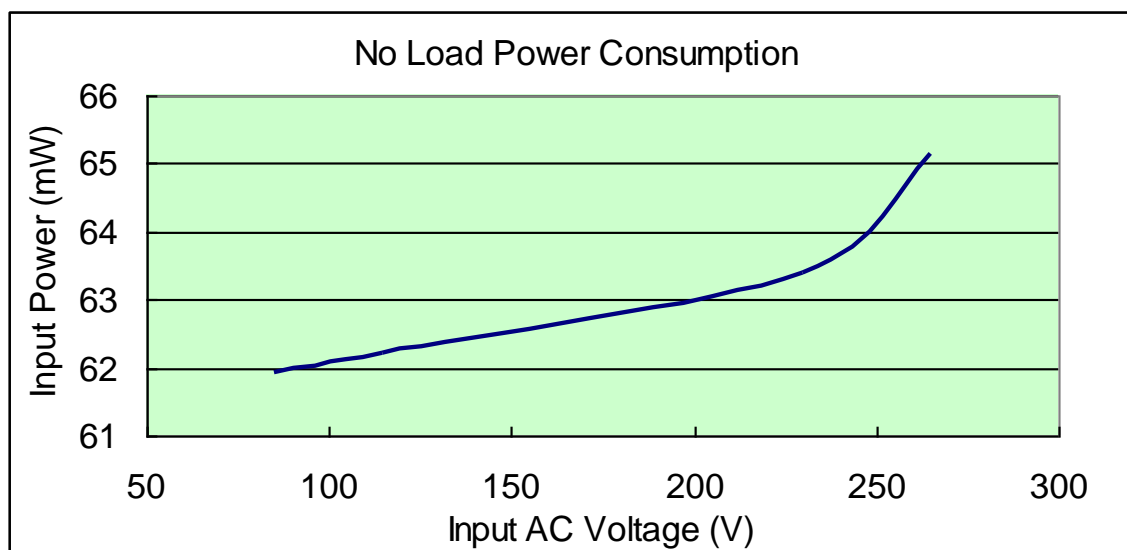
	Pin (W)	V _{OUT1} (V)	I _{OUT1} (A)	V _{OUT2} (V)	I _{OUT2} (A)	Efficiency	V _{OUT1} Regulation	V _{OUT2} Regulation
Vin=230Vac/50Hz	0.06338	11.94	0	5	0	0.00%	-0.50%	0.00%
	5.475	11.77	0.3	5	0.1	73.63%	-1.92%	0.00%
	1.5214	11.89	0.03	5	0.1	56.31%	-0.92%	0.00%
	0.57955	11.74	0.03	5	0.005	65.08%	-2.17%	0.00%
	4.5556	11.74	0.3	5	0.005	77.86%	-2.17%	0.00%

	Pin (W)	V _{OUT1} (V)	I _{OUT1} (A)	V _{OUT2} (V)	I _{OUT2} (A)	Efficiency	V _{OUT1} Regulation	V _{OUT2} Regulation
Vin=265Vac/50Hz	0.06514	11.98	0	5	0	0.00%	-0.17%	0.00%
	5.5176	11.77	0.3	5	0.1	73.06%	-1.92%	0.00%
	1.5205	11.9	0.03	5	0.1	56.36%	-0.83%	0.00%
	0.58397	11.75	0.03	5	0.005	64.64%	-2.08%	0.00%
	4.5994	11.75	0.3	5	0.005	77.18%	-2.08%	0.00%

Notes:

1. The red triangle means the worst case in table.

No Load Consumption



Electric Strength Test

Primary circuit to secondary circuit electric strength testing was completed according to IEC61000-4-2.

Input and output was shorted respectively. 3000VAC/50Hz sine wave applied between input and output for 1min, and operation was verified.

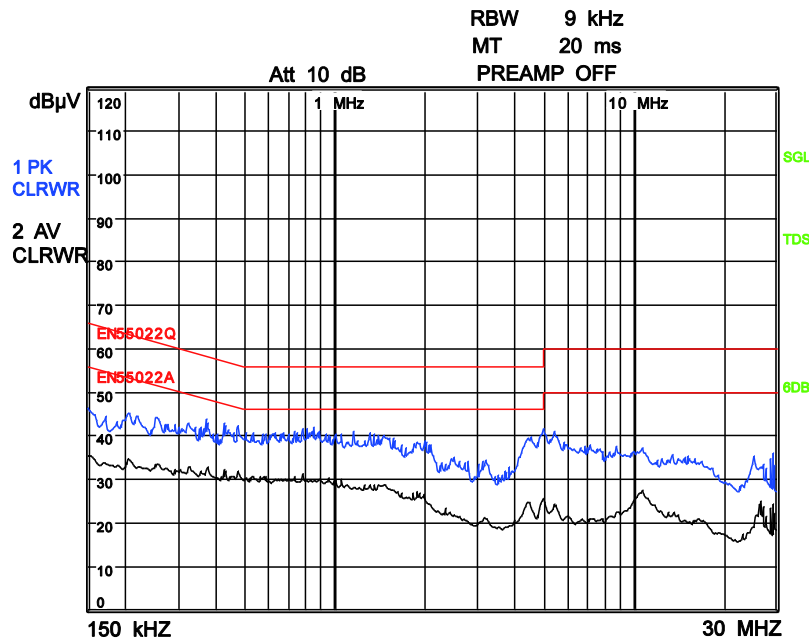
Surge Test

Line to Line 1kV and Line to Power Earth 1kV surge testing was completed according to IEC61000-4-5. Input voltage was set at 230VAC/50Hz. Output was loaded at full load and operation was verified following each surge event.

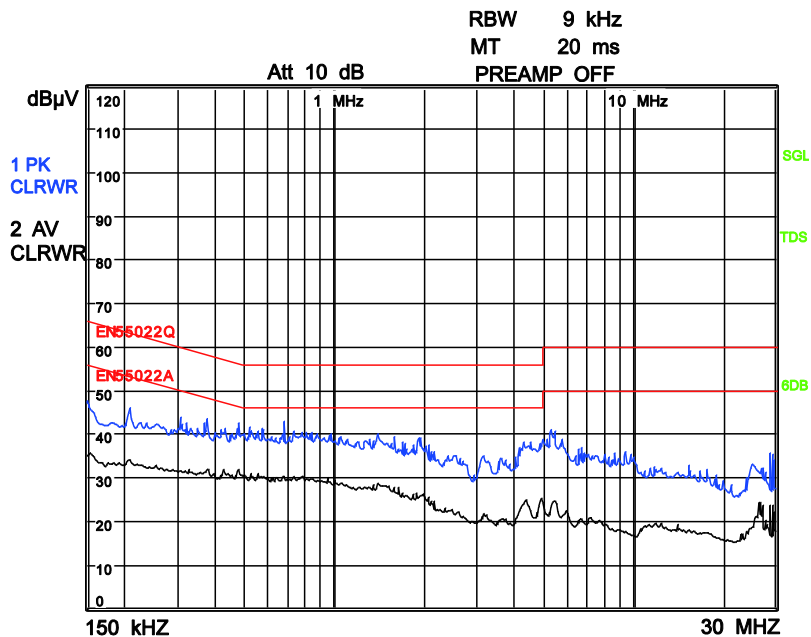
Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/Fail)
1000	230	L to N	90	Pass
-1000	230	L to N	270	Pass
1000	230	L to PE	90	Pass
-1000	230	L to PE	270	Pass
1000	230	N to PE	90	Pass
-1000	230	N to PE	270	Pass

Conducted EMI Test

Test with 230Vac input and full load condition



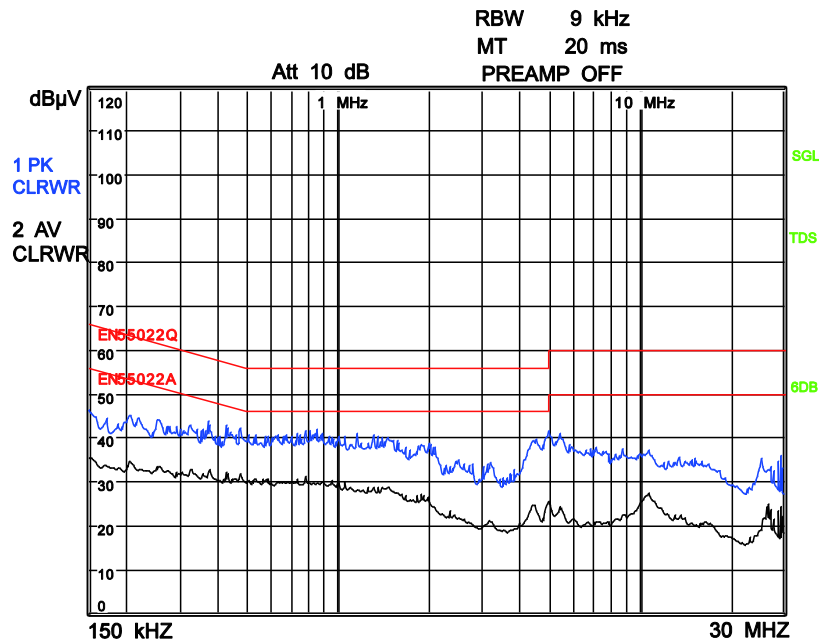
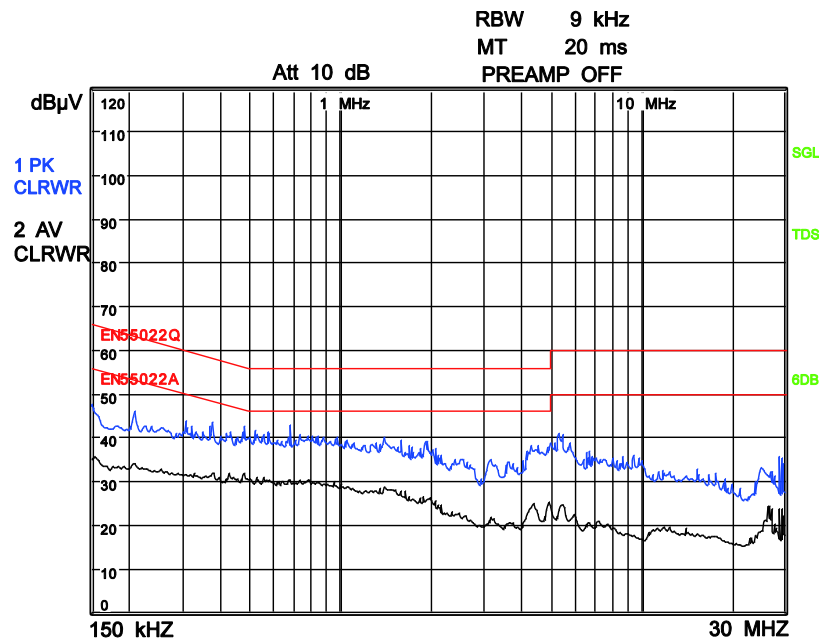
230Vac, 50Hz, Maximum Load, L Line, Output GND floats, EN55022 Limits



230Vac, 50Hz, Maximum Load, N Line, Output GND floats, EN55022 Limits

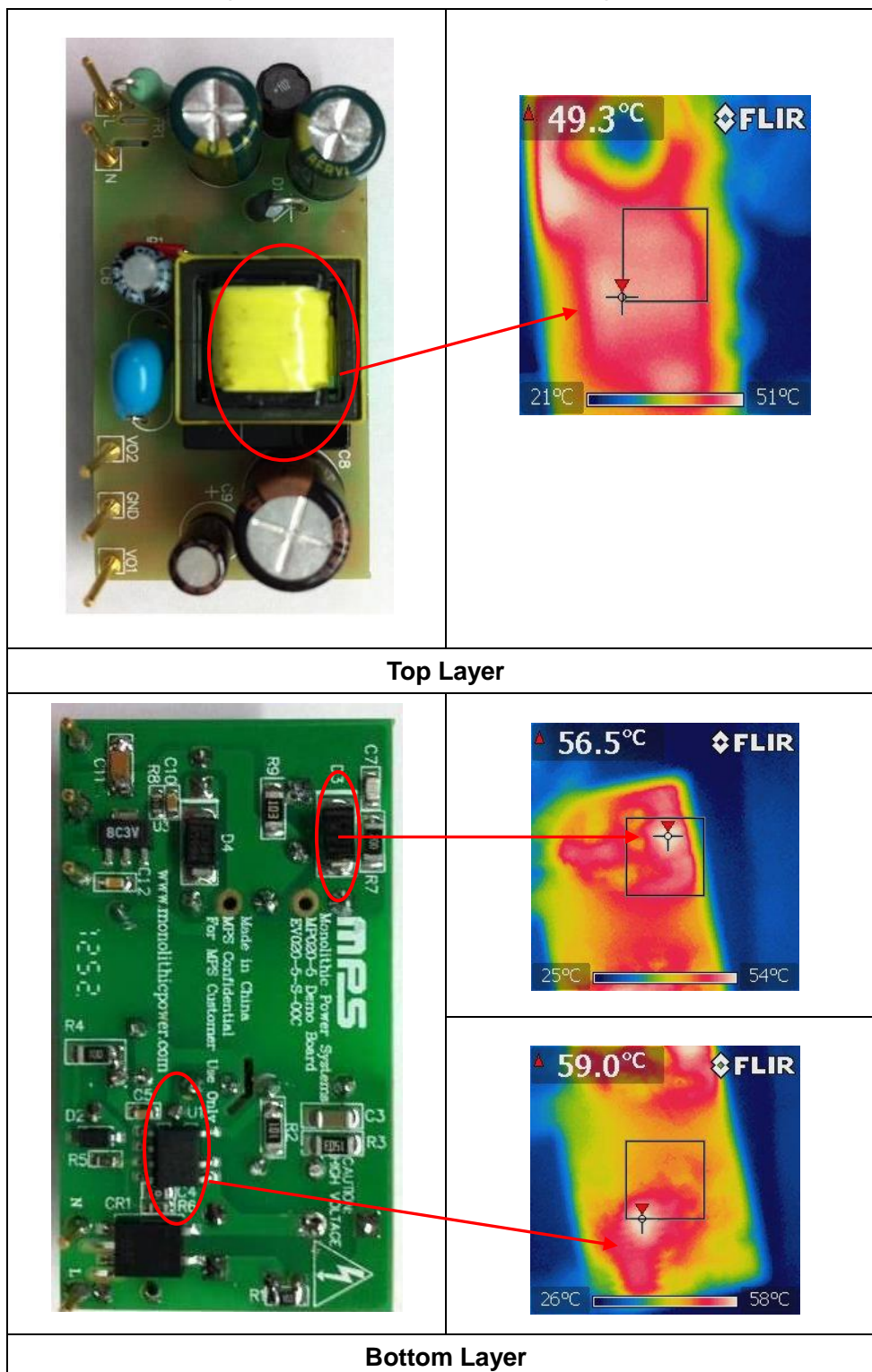
Conducted EMI Test (*continued*)

Test with 115Vac input and full load condition


115Vac, 60Hz, Maximum Load, L Line, Output GND floats, EN55022 Limits

115Vac, 60Hz, Maximum Load, N Line, Output GND floats, EN55022 Limits

Thermal Test

Test is conducted at ambient temperature of 25°C, 85Vac/60Hz input.

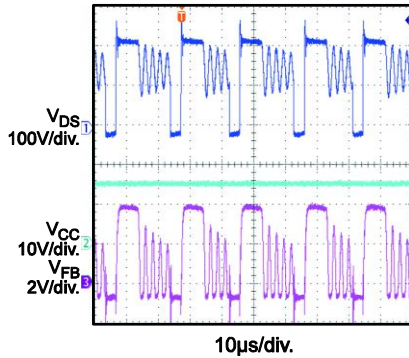


EVB TEST RESULTS

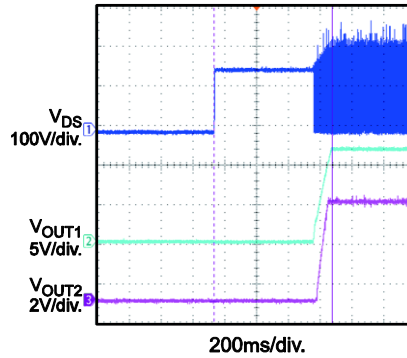
Performance waveforms are tested on the evaluation board.

$V_{IN}=115VAC/60Hz$, $V_{OUT1}=12V$, $I_{OUT1}=0.3A$, $V_{OUT2}=5V$, $I_{OUT2}=0.1A$, CC Mode Load, $T_a=25^{\circ}C$

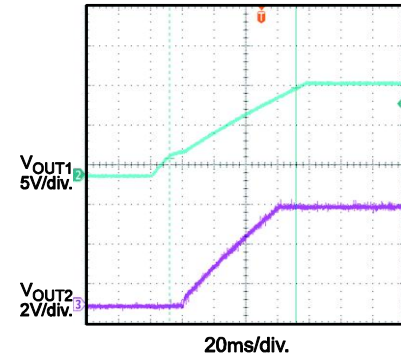
Steady State



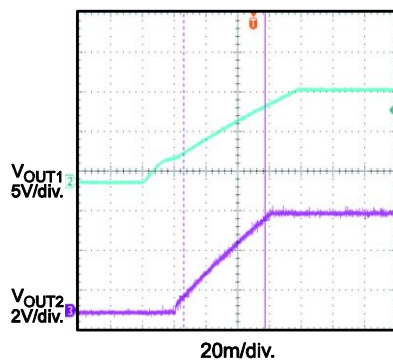
Turn On Delay



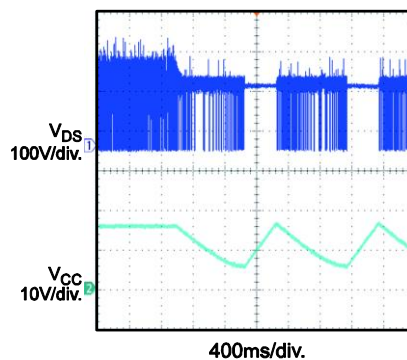
Output1 Rise Time



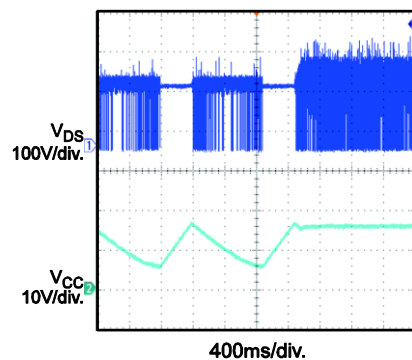
Output2 Rise Time



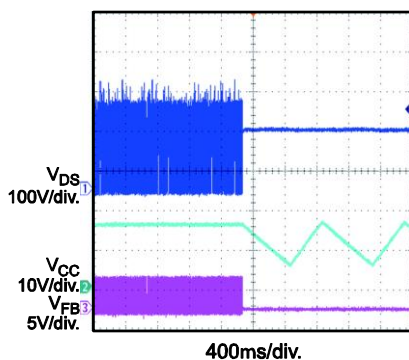
OCP Entry



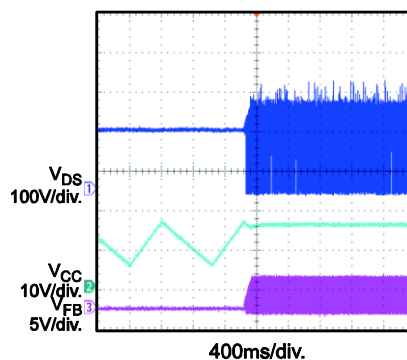
OCP Recovery



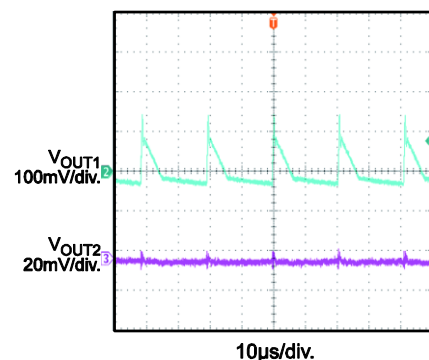
OCP Entry



OCP Recovery



Output Voltage Ripple

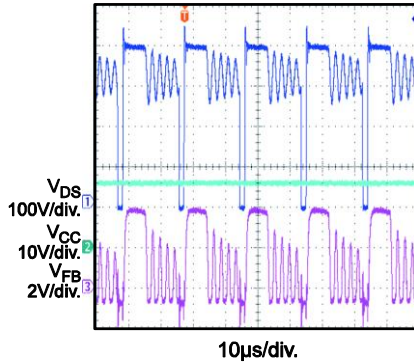


EVB TEST RESULTS *(continued)*

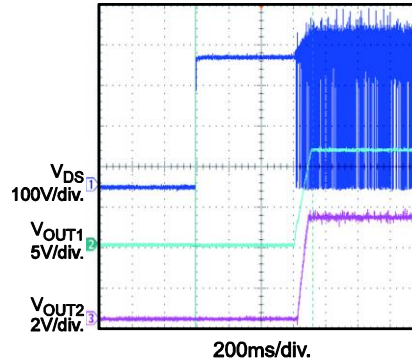
Performance waveforms are tested on the evaluation board.

$V_{IN}=230VAC/50Hz$, $V_{OUT1}=12V$, $I_{OUT1}=0.3A$, $V_{OUT2}=5V$, $I_{OUT2}=0.1A$, CC Mode Load, $T_a=25^{\circ}C$

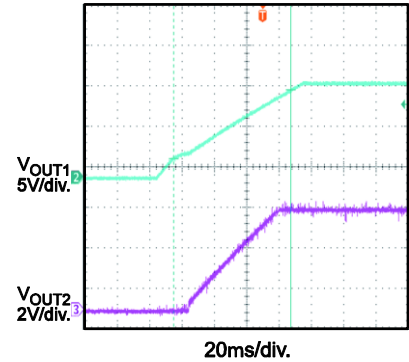
Steady State



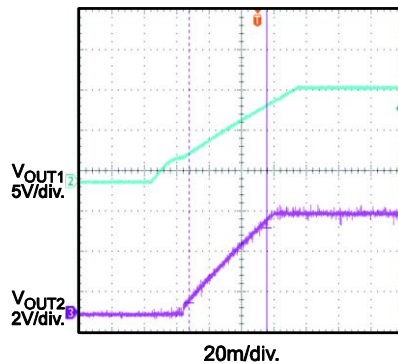
Turn On Delay



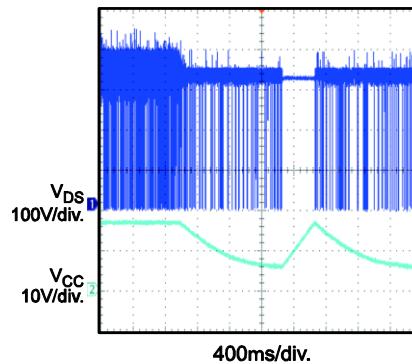
Output1 Rise Time



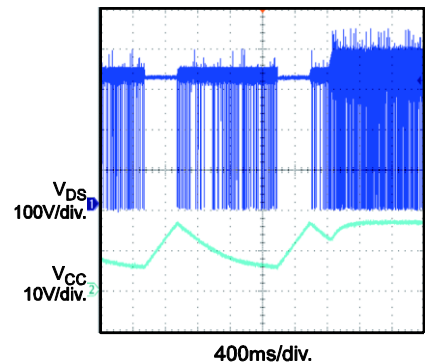
Output2 Rise Time



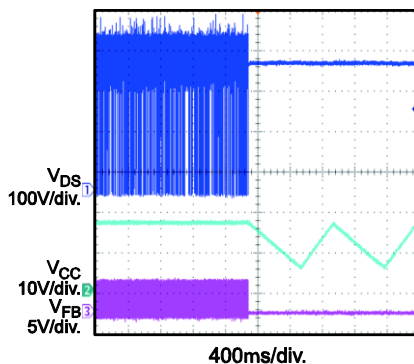
OCP Entry



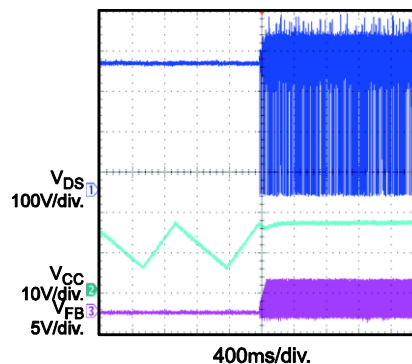
OCP Recovery



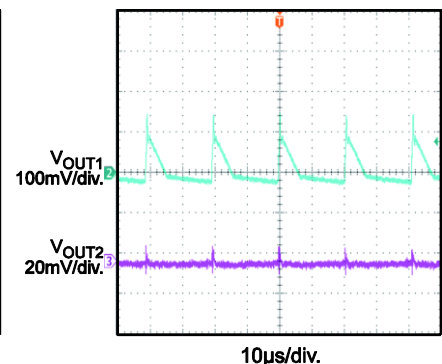
OCP Entry



OCP Recovery



Output Voltage Ripple



QUICK START GUIDE

1. Preset Power Supply to $85\text{VAC} \leq V_{\text{IN}} \leq 265\text{VAC}$.
2. Turn Power Supply off.
3. Connect the Line and Neutral terminals of the power supply output to L and N port. For three-wire input application, make OUTPUT GND connected to Earth.
4. Connect Different Load to Corresponding Outputs :
 - a. Positive 1 (+): 12V OUT
 - b. Positive 2 (+): 5V OUT
 - c. Negative (-): GND
5. Turn Power Supply on after making connections.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.