EV20075DH-00A

3A, 1.30V – 3.6V
DDR Memory VTT Termination Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP20075 integrates the DDR memory termination regulator with the output voltage (VTT) and a buffered VTTREF whose output is half of VREF.

The VTT-LDO is a 3A sink/source tracking termination regulator. It is specifically designed for low-cost/low-external component count systems, where space is a premium.

The MP20075 maintains a fast transient response only requiring 20uF (2x10µF) of ceramic output capacitance. The MP20075 supports Kelvin sensing functions.

The MP20075 is available in the 8-pin MSOP with Exposed PAD, package and is specified from −40°C to 85°C.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Bias Voltage	V_{DRV}	3.3	V
Input Voltage	V_{DDQ}	1.3 - 1.8	V
Reference Input Voltage	V_{REF}	V_{DDQ}	V
Output Voltage	V_{TT}	1/2 V_{DDQ}	V
Output Current	I_{TT}	±3	A

FEATURES

- VDDQ Voltage Range: 1.3V to 3.6V
- Up to 3A Integrated Sink/Source Linear Regulator with Accurate VDDQ/2 Divider Reference for DDR Termination
- Requires Only 20µF Ceramic Output Capacitance
- Drive Voltage 3.3V
- 1.3V Input (VDDQ) Helps Reduce Total Power Dissipation
- Integrated Divider Tracks VREF for VTT and VTTREF
- Kelvin Sensing (VTTSEN)
- ±30mV Accuracy for VTT and VTTREF
- Built-In Soft-Start, UVLO and OCL
- Thermal Shutdown

APPLICATIONS

- Notebook DDR2/3 Memory Supply and Termination Voltage in ACPI Compliant
- Active Termination Busses

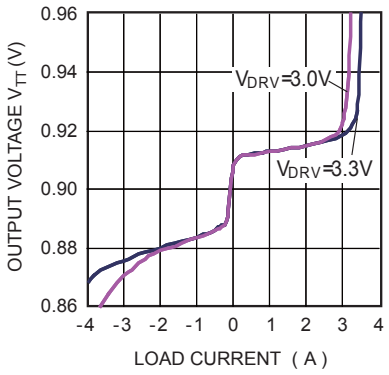
EV20075DH-00A EVALUATION BOARD

(L x W x H) 2.5” x 2.5” x 0.5”
(6.5cm x 6.5cm x 1.2cm)

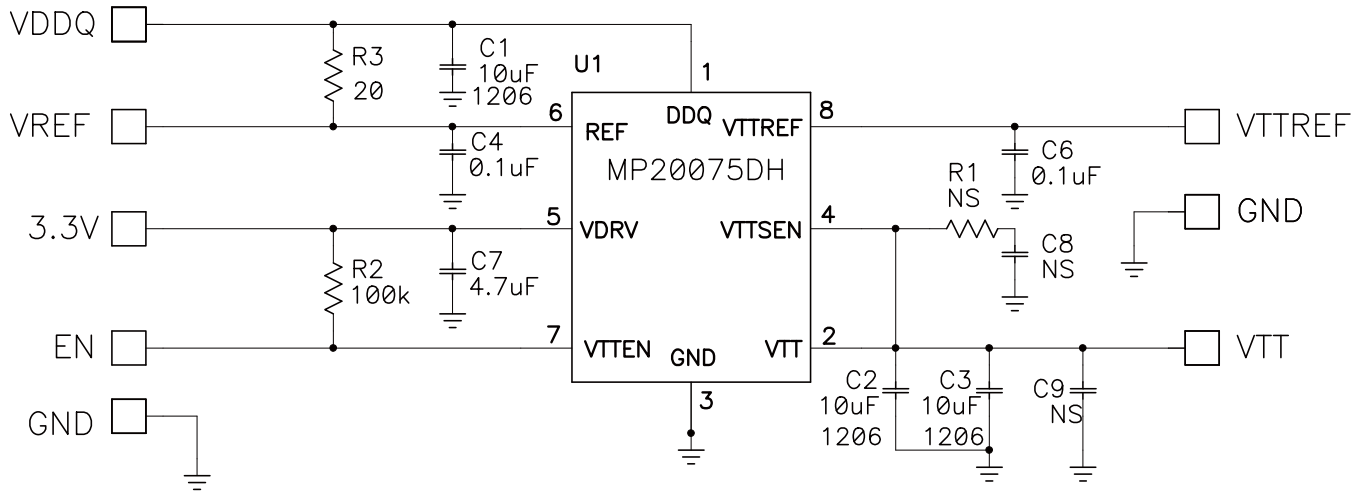
Board Number	MPS IC Number
EV20075DH-00A	MP20075DH

Load Regulation

$V_{REF}=V_{DDQ}=1.8V$



EVALUATION BOARD SCHEMATIC



EV20075DH-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer P/N
3	C1, C2, C3	10μF	Ceramic Cap., 16V, X7R	1206	muRata	GRM31CR71C106KAC7L
2	C4,C6	0.1μF	Ceramic Cap., 16V, X7R	0603	muRata	GRM188R71C104KA01D
3	C5,C8, C9	NS		0603		
1	C7	4.7μF	Ceramic Cap., 16V, X7R	0805	muRata	GRM21BR71C475KA73L
1	R1	NS		0603		
1	R2	100kΩ	Film Res., 5%	0603	Yageo	RC0603JR-07100KL
1	R3	20Ω	Film Res., 5%	0603	Yageo	9C06031A20R0JLHFT
1	U1		LDO	MSOP8	MPS	MP20075DH

PRINTED CIRCUIT BOARD LAYOUT

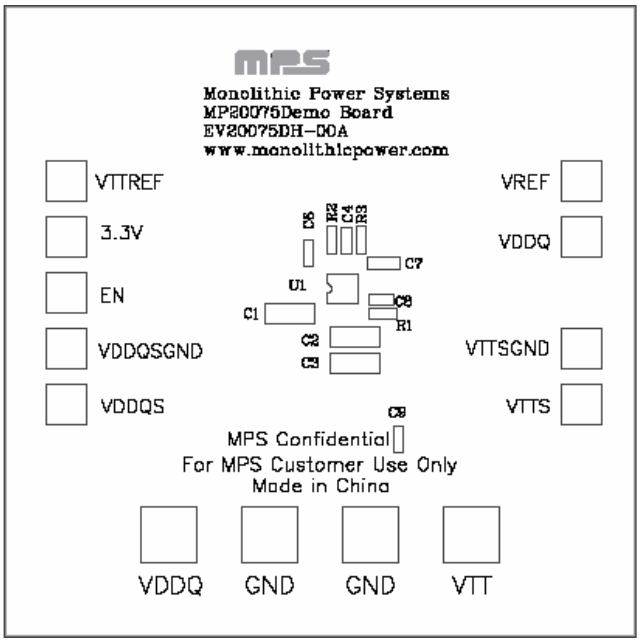


Figure 1—Top Silk Layer

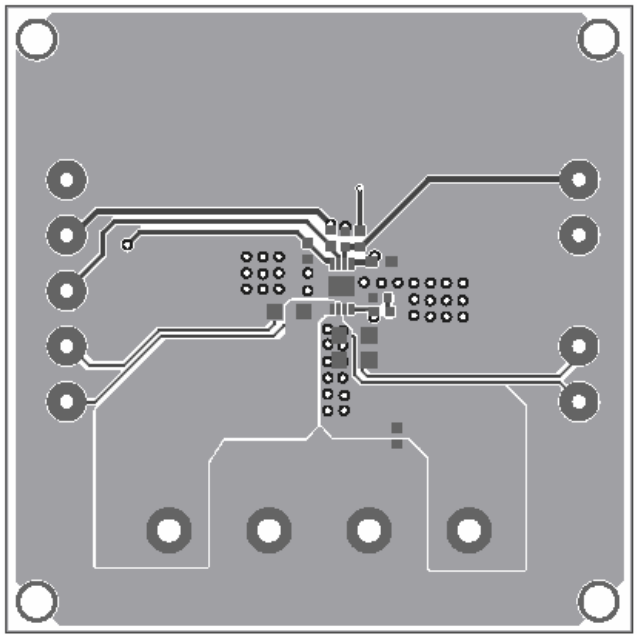


Figure 2—Top Layer

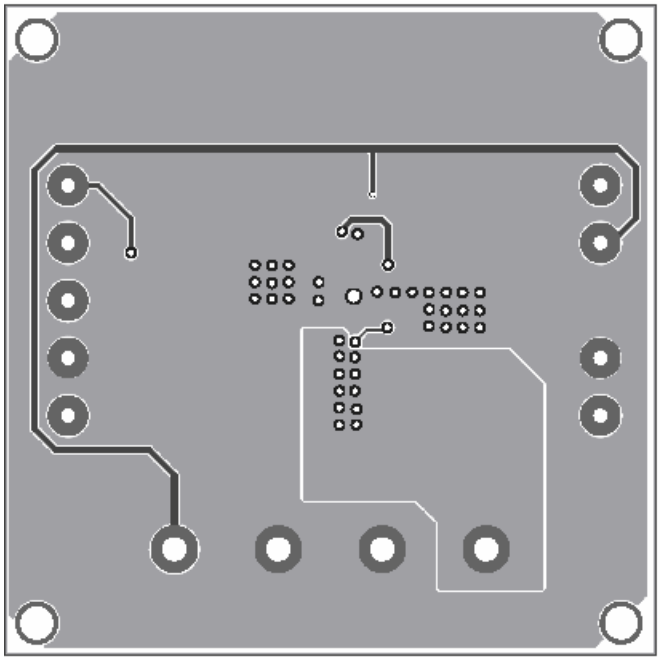


Figure 3—Bottom Layer

QUICK START GUIDE

The output voltage of this board is set by VREF voltage. The EN pin is connected to VDRV with a 100kΩ resistor for automatic startup. You can connect EN to GND to disable the MP20075.

1. Attach the positive and negative ends of the load to the VTT and GND pins, respectively.
2. Attach the input voltage (1.3V ≤ VDDQ ≤ 3.6V) and input ground to the VDDQ and GND pins, respectively. (the VREF and VDDQ is directly connected together by R3)
3. Attach the VDRV voltage 3.3V and ground to the VDRV and GND pins, respectively.
4. The VTT output voltage is 1/2 of VREF/VDDQ.