HR1200

High-Performance Digital PFC+LLC Combo Controller

NOT RECOMMENDED FOR NEW DESIGNS. REFER TO HR1203

DESCRIPTION

The HR1200 is a high-performance controller that integrates an advanced digital PFC controller and a half-bridge LLC resonant controller. It requires quite low input power at no load or ultra-light load, making it compliant with Energy using Product Directive (EuP) Lot 6 and Code of Conduct Version 5 Tier 2 specifications.

The PFC of the HR1200 employs a patented average current control scheme, which can operate both in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) according to the instantaneous condition of the input voltage and output load. The IC exhibits excellent efficiency and high power factor (PF) at light load. In CCM, the HR1200 can be used in applications up to 500W with minimal board size limitations. The performance of the PFC can be optimized by programming multiple parameters through an I^2C GUI. Programming can be completed either by the factory or by the customer referring to a detailed user guide.

The half-bridge LLC resonant converter achieves high efficiency with zero-voltage switching (ZVS). The HR1200 implements an adaptive dead-time adjustment (ADTA) function to guarantee ZVS in different load conditions. Additionally, the HR1200 can prevent the LLC converter from operating in capacitive mode, making it more robust and easier to design.

The HR1200 integrates a high-voltage (HV) current source internally for start-up. When the AC input is removed, the HV current source also functions as an X-cap discharger. Such features are helpful to reduce related devices, thus reduce power consumption at no load.

The HR1200 has multiple protection features including thermal shutdown (TSD), open-loop protection (OLP), over-current protection (OCP), over-voltage protection (OVP), and brown-in/brown-out protection.

FEATURES

General System Features

- Meets EuP Lot 6 and COC Version 5 Tier 2 Specifications
- HV Current Source for Start-Up
- Smart X-Cap Discharger
- Standard I^2C Interface
- 1k EEPROM to Store Parameters
- User-Friendly GUI for Digital PFC

PFC Controller

- High Efficiency from Light Load to Full Load by CCM/DCM Multi-Mode Control
- High PF Due to Patented Input Capacitor Current Compensation
- Programmable Frequency Jittering
- Programmable Brown-In and Brown-Out
- Programmable Soft Start
- Cycle-by-Cycle Current Limit
- Open-Loop Protection

LLC Controller

- 600V High-Side Gate Driver with Integrated Bootstrap Diode and High dv/dt Immunity
- Adaptive Dead-Time Adjustment of HB LLC with Minimum and Maximum Limit
- Burst Mode Switching
- Safe Start-Up in Case of System Fault
- Two-Level Over-Current Protection (OCP)
- Latch Shutdown Protection
- Over-Temperature Protection (OTP)
- Capacitive Mode Protection

APPLICATIONS

- Notebook Adapters
- All-in-One or Gaming Power Supply
- Desktop PC and ATX Power
- General AC/DC Power Supply up to 600W
- LCD TV and Plasma TV Power Supply

NOT RECOMMENDED FOR NEW DESIGNS. REFER TO HR1203

TYPICAL APPLICATION

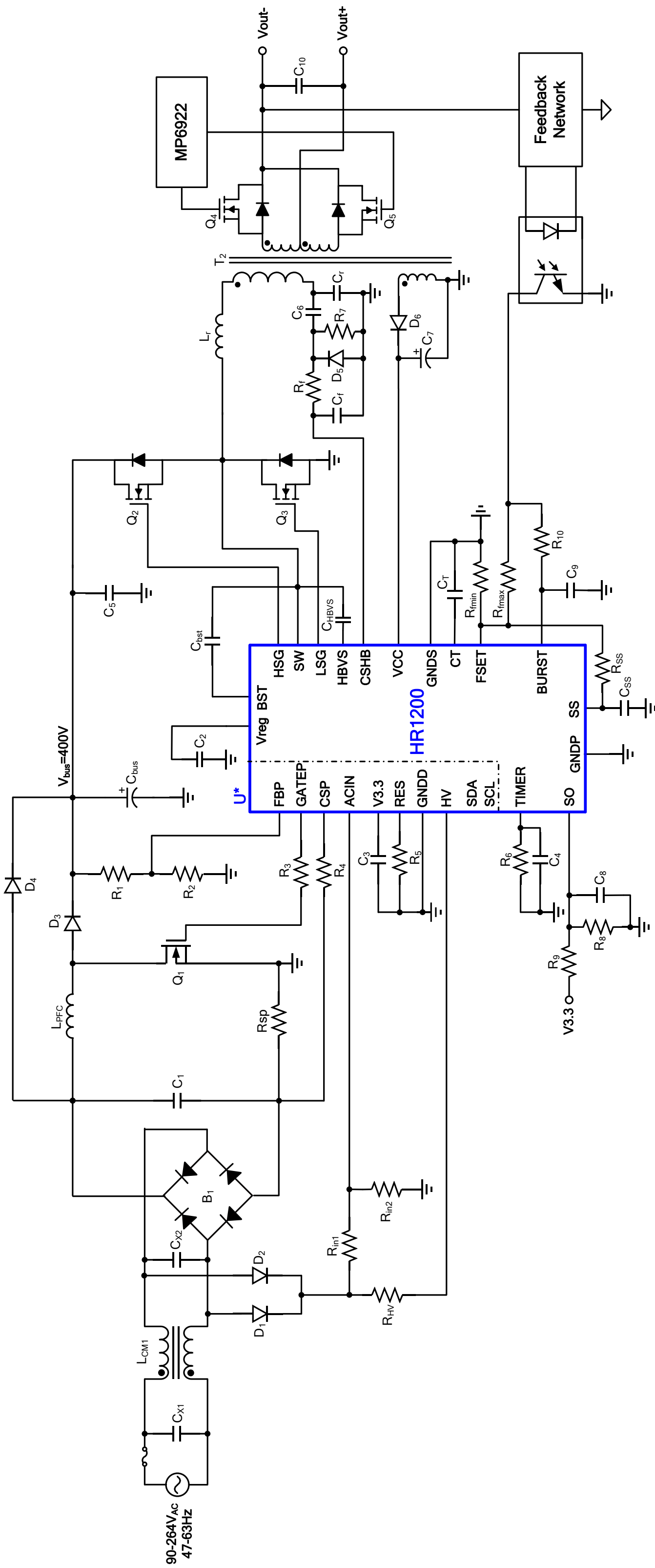


Figure 1: Typical Application

ORDERING INFORMATION

Part Number*	Package	Top Marking
HR1200GM−XXXX*	TSSOP-28	*See Below*
HR1200GY−XXXX*	SOIC-28	

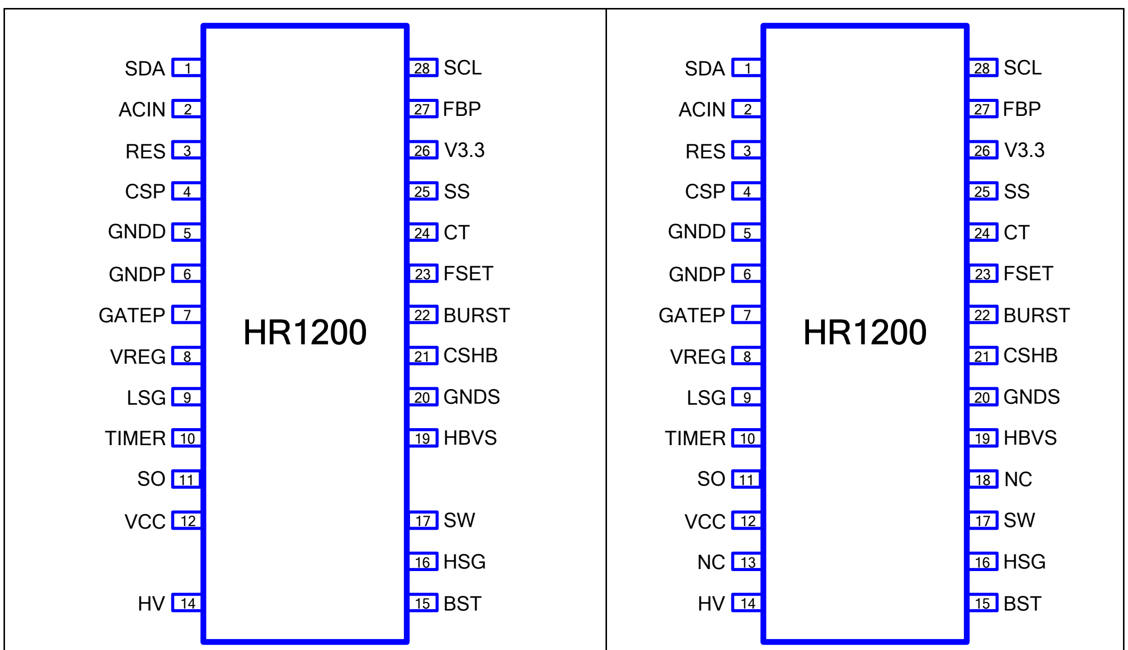
*−XXXX: internal code version control.
For customer-specific projects, MPS will assign a special 4-digit number.
For Tape & Reel, add suffix −Z (e.g. HR1200GM−XXXX−Z)
For Tape & Reel, add suffix −Z (e.g. HR1200GY−XXXX−Z)

TOP MARKING

MPSYYWW
HR1200
LLLLLLLLL

MPS: MPS prefix
YY: year code
WW: week code
HR1200: first six digits of the part number
LLLLLLLLL: lot number

PACKAGE REFERENCE



TSSOP-28	SOIC-28

Recommended Operating Conditions (1)

HV_{pk} .... ≤500V
Supply voltage (V_{CC}) .... 14V to 30V
Operating junction temp........... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSSOP-28	82	20	°C/W
SOIC-28	60	30	°C/W

ABSOLUTE MAXIMUM RATINGS (2)

Parameter	Symbol	Condition	Min	Max	Units
General					
Total power dissipation (3)	P_{total}	T_{amb} = 125°C		1.56	W
Storage temperature	T_{stg}		-55	+150	°C
Junction temperature	T_J		-40	+150	°C
Lead temperature	T_{LEAD}			260	°C
Voltage					
Voltage on HV	V_{HV}	Continuous	-0.5	+700	V
Floating supply voltage	V_{BST}		-1	+618	V
Floating ground voltage	V_{SW}		-3	+618	V
Voltage on high-side gate driver	V_{HSG}			+618	V
Floating ground max. slew rate	dV_{SW}/dt			50	V/ns
Voltage on VCC	V_{CC}		-0.5	+38	V
Voltage on VREG	V_{reg}		-0.5	+14	V
VREG Supply Current	I_{reg}			50	mA
V3.3 Supply Current	I_{3V3}			20	mA
Voltage on low-side gate driver	V_{LSG}		-0.5	+14	V
Voltage on PFC gate driver	V_{PFCG}		-0.5	+14	V
Voltage on CS	V_{CS}		-6.5	+6.5	V
Voltage on HBVS	V_{HBVS}		-0.3	Self-limited	V
Other analog pins			-0.5	6.5	V
Other digital pins			-0.5	2	V
Analog ground to digital ground	GNDP/GNDS to GNDD		-0.3	+0.3	V
Current					
Current on HBVS	I_{HBVS}		-65	+65	mA
Source current of FSET	I_{FSET}			2	mA
ESD (4)					
	All pins	Human body model		2000	V
	All pins	Machine model		200	V
	All pins	Charged device model		500	V

NOTES:
1) The device is not guaranteed to function outside of its operating conditions.
2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 25V, T_J = -40°C to 125°C, currents entering the IC are positive, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Voltage Start-Up Current Source (HV)						
Breakdown voltage	V_{HVBR}		700			V
Normal charge current	I_{HVNOR}	V_{HV} = 100V, V_{CC} = 15V, T_J = 25°C	5.5	7	8.5	mA
Normal charge current	I_{HVNOR}	V_{HV} = 100V, V_{CC} = 15V	4.5	7	8.9	mA
Supply current when fault occurs	$I_{HVLimit}$	V_{HV} = 100V, V_{CC} = 0V	0.8	1.4	2.1	mA
Leakage current when turned off	I_{HVoff}	V_{HV} = 400V, V_{CC} = 24V		7	10	µA
IC Power Supply (VCC)						
IC turn-on threshold voltage when HV is detected	$V_{CCON(HV)}$	V_{HV} > V_{HVON}	20	21.5	23.1	V
UV protection threshold 1	V_{CCUVP1}	LLC operation	10.5	11.3	12.1	V
UV protection threshold 2(5)	V_{CCUVP2}	LLC disabled	13.9	15	16.2	V
IC release threshold	V_{CCRST}		8.4	9	9.9	V
Operation current at normal	$I_{CC(nor)}$	R_{RES} =20kΩ f_{PFC} = 120kHz f_{LLC} = 200kHz		14		mA
Start-up current	$I_{CC\text{-}start1}$	V_{CC} = 20V		0.55	0.7	mA
Current at fault (LLC fault, PFC operation)(5)	$I_{CC\text{-}Disable1}$	TIMER = 4V PFC burst		2		mA
Current at fault (LLC fault, PFC fault)(5)	$I_{CC\text{-}Disable2}$	TIMER = 4V		0.5		mA
Regulated Power Supply (VREG)						
Regulated output voltage	V_{reg}	I_{reg} = 0mA	11.3	12	12.8	V
		I_{reg} = 30mA	10.8	11.8	12.6	V
IC enable threshold	V_{regON}		10.2	10.8	11.5	V
UVP	V_{regUVP}		7.7	8.2	8.8	V
Power Supply for Digital Core (V3.3)						
Voltage regulation range	V_{3V3}	I_{3V3} = 0mA	2.95	3.15	3.45	V
		I_{3V3} = 15mA	2.85	3.1	3.35	V
X-Cap Discharger (HV)						
X-cap discharger current(5)	$I_{X\text{-}d}$			5.5		mA
X-cap discharger clock time	$T_{X\text{-}d}$		0.9	1.5	2.4	ms
PFC Gate Driver						
Sourcing capacity(5)	I_{gate_sr}	C_{Gate} = 1nF		750		mA
Sinking capacity(5)	I_{gate_sk}	C_{Gate} = 1nF		-800		mA
Gate-on resistor	Ron(H)	Sourcing 20mA		4.5		Ω
	Ron(L)	Sinking 20mA		2.5		Ω
Voltage fall time	T_f	C_{Gate} = 1nF		10		ns
Voltage rise time	T_r	C_{Gate} = 1nF		15		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 25V, T_J = -40°C to 125°C, currents entering the IC are positive, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Reference Current (RES)						
Voltage regulation range	V_{RT}	T_J = 25°C	1.245	1.25	1.255	V
System Clock						
Clock frequency	f_{osc_nor}	At normal		19		MHz
	f_{osc_nopwm}	At fault or burst off		1		MHz
AC Input Sensing (ACIN)						
Voltage range		K_{ACIN} = 0.0032	0		1.6	V
PFC Feedback (FBP)						
Voltage range		K_{ACIN} = 0.0032	0		1.6	V
Current Sense (CSP)						
Voltage range		K_{ACIN} = 0.0032	0		1.6	V
Bias current in CSP	$I_{csp\text{-}bias}$	R_{RES} = 20kΩ	61	62.5	64	μA
ADC for ACIN, FB, and CSP						
ADC voltage reference		T_J = 25°C	1.593	1.600	1.607	V
ADC resolution(6)				10		bits
Acquisition time(6)					350	ns
Integral non-linearity (INL)(6)				±7.0		LSB
Differential non-linearity (DNL)(6)				±4.5		LSB
Offset error(6)				±0.5		LSB
Gain error(6)				±1.5		LSB
DAC for OVP and OCL						
Reference voltage		T_J = 25°C	1.593	1.600	1.607	V
Resolution(6)				7		bits
Integral non-linearity (INL)(6)				±1.5		LSB
Differential non-linearity (DNL)(6)				±0.3		LSB
Offset error(6)				±0.2		LSB
Gain error(6)				±1.5		LSB
Output setting time(5)				5		μs
DAC for Set Comparator						
Reference voltage		T_J = 25°C	1.593	1.600	1.607	V
Resolution(6)				10		bits
Integral non-linearity (INL)(6)				±4.5		LSB
Differential non-linearity (DNL)(6)				±2.0		LSB
Offset error(6)				±0.5		LSB
Gain error(6)				±1.5		LSB

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 25V, T_J = -40°C to 125°C, currents entering the IC are positive, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Comparator for Set Signal, OVP, and OCL						
Offset voltage				60	360	mV
I²C Characteristics (SCL/SDA)[5]						
Input high voltage (VIH)			2.1			V
Input low voltage (VIL)					0.8	V
Output low voltage (VOL)					0.4	V
I²C Timing Characteristics[5]						
Operating frequency range				100	400	kHz
Bus free time		Between stop and start	4.7			µs
Holding time			4.0			µs
Repeated start condition setup time			4.7			µs
Stop condition setup time			4.0			µs
Data hold time			0			ns
Data setup time			250			ns
Clock low time out			25		35	ms
Clock low period			4.7			µs
Clock high period			4.0		50	µs
Clock/Data fall time					300	ns
Clock/Data rise time					1000	ns
High-Side Floating Gate Driver Supply (BST, SW)						
BST leakage current	I_{LKBST}	V_{BST} = 600V			10	µA
SW leakage current	I_{LKSW}	V_{SW} = 582V			10	µA
Current Sensing of the Half-Bridge (CSHB)						
Frequency shift threshold	V_{CS-OCR}	OCR	0.7	0.77	0.83	V
OCP threshold	V_{CS-OCP}	OCP	1.41	1.48	1.55	V
Current polarity comparator reference when HSG is on	V_{CSPR}			80		mV
Current polarity comparator reference when LSG is on	V_{CSNR}			-80		mV
Output Voltage Sense (SO)						
Latch protection on SO	$V_{SO-Latch}$		3.22	3.42	3.6	V
Start-up failure protection on SO	V_{SO-SFP}		1.85	1.96	2.08	V
Pull-up current on SO	I_{SO-PU}			100		nA
Oscillator (FSET, CT)						
Output duty cycle	D	T_J = 25°C	48	50	52	%
		T_J = -40°C to 125°C	47	50	53	%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{CC} = 25V, T_J = -40°C to 125°C, currents entering the IC are positive, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillation frequency	f_{osc}				600	kHz
CT peak value	V_{CTP}		3.54	3.74	3.94	V
CT valley value	V_{CTV}		0.79	0.87	0.95	V
Voltage reference at FSET	V_{REF}		1.88	1.97	2.06	V
Dead time	t_{DMIN}	C_{HBVS} = 5pF		240		ns
	t_{DMAX}		0.82	1.1	1.38	µs
Timer for CMP	t_{D_float}	HBVS floating	230	300	390	ns
	t_{D_CMP}			50		µs
Half-Bridge Voltage Sensing (HBVS)						
Voltage clamp	V_{HBVS-C}			7.5		V
Minimum voltage for the change rate to be detected	dv_{min}/dt	C_{HBVS} = 5pF, typically			190	V/µs
Turn-on delay	T_d	Slope finish to turn-on delay		130		ns
Soft-Start Function (SS)						
Discharge resistance	R_d	V_{CS} > V_{CS-OCR}		120		Ω
Threshold for OCP	V_{SS-OCP}	V_{CS} > V_{CS-OCP}	1.61	1.72	1.82	V
Standby Function (BURST)						
Disable threshold	V_{th}		1.18	1.23	1.28	V
Hysteresis	V_{hys}			40		mV
Delayed Shutdown (TIMER)						
Charge current	I_{CHARGE}	V_{TIMER} = 1V, V_{CS} = 0.85V, SO = 3V	90	140	180	µA
Charge current for SFP	I_{CHARGE_SFP}	SO < 2.5V		25		µA
Threshold for forced operation at maximum frequency	V_{th1}		1.87	1.97	2.07	V
Shutdown threshold	V_{th2}		3.25	3.45	3.65	V
Restart threshold	V_{th3}		0.23	0.29	0.35	V
Low-Side Gate Driver (LSG)						
Peak source current(5)	$I_{sourcepk}$			0.75		A
Peak sink current(5)	I_{sinkpk}			0.87		A
Sourcing resistor	R_{source}			4		Ω
Sinking resistor	R_{sink}			2		Ω
Fall time	t_f			20		ns
Rise time	t_r			20		ns

ELECTRICAL CHARACTERISTICS *(continued)*

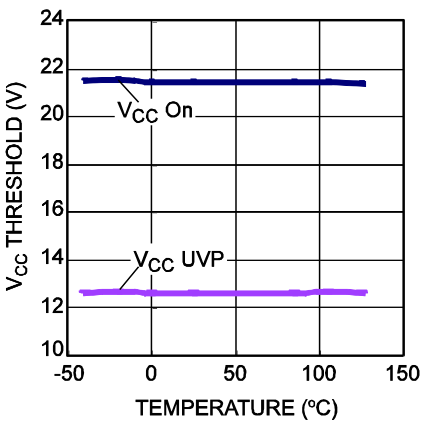
V_{CC} = 25V, T_J = -40°C to 125°C, currents entering the IC are positive, min and max are guaranteed by characterization, typical is tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Side Gate Driver (HSG, Referenced to SW)						
Peak source current(5)	$I_{sourcepk}$			0.74		A
Peak sink current(5)	I_{sinkpk}			0.87		A
Sourcing resistor	R_{source}			4		Ω
Sinking resistor	R_{sink}			2		Ω
Fall time	t_f			20		ns
Rise time	t_r			20		ns
Thermal Shutdown						
Thermal shutdown threshold				145		°C
Thermal shutdown recovery threshold				100		°C

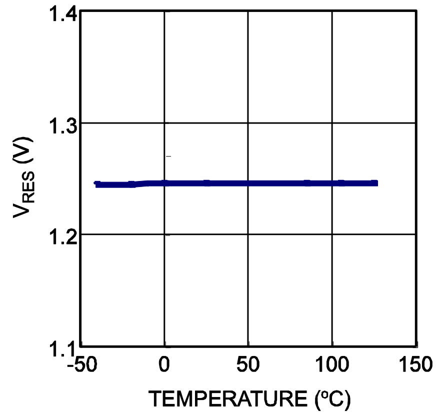
NOTE:
5) Guaranteed by design.
6) Guaranteed by characterization.

TYPICAL CHARACTERISTICS

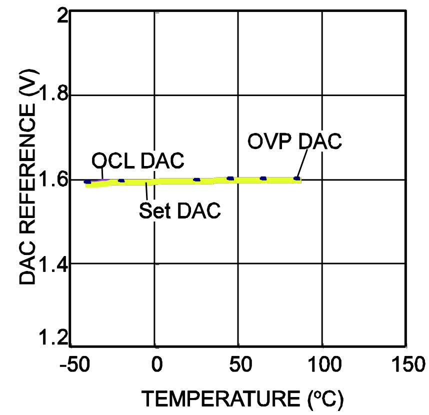
V_{CC} On & UVLO vs. T_J



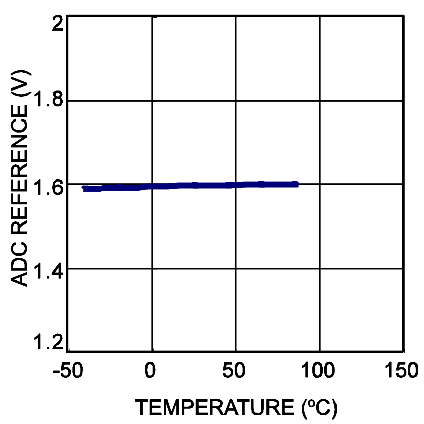
V_{RES} vs. T_J



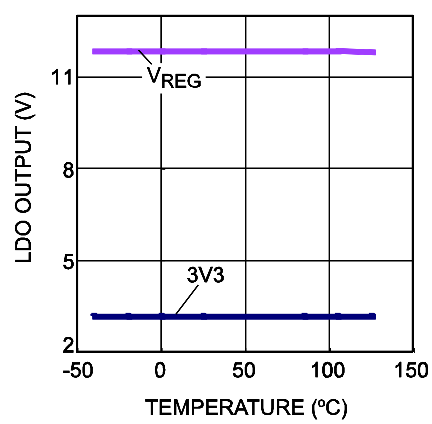
DAC Reference vs. T_J



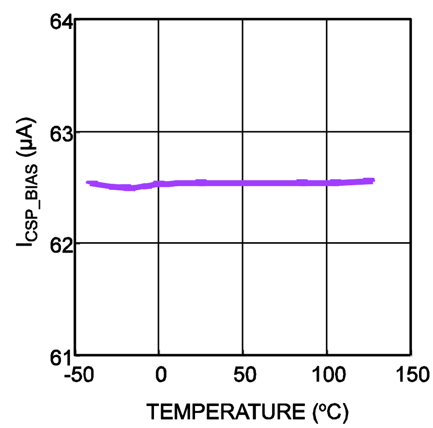
ADC Reference vs. T_J



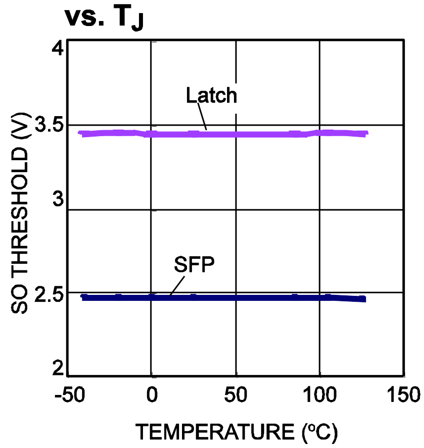
LDO Output vs. T_J



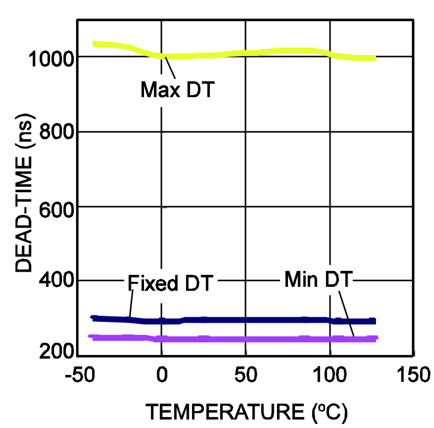
I_{CSP_Bias} vs. T_J



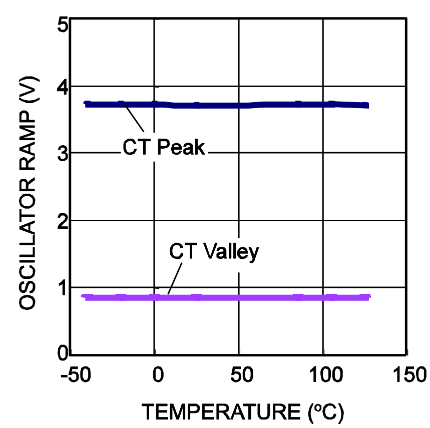
SO Threshold vs. T_J



Dead Time vs. T_J

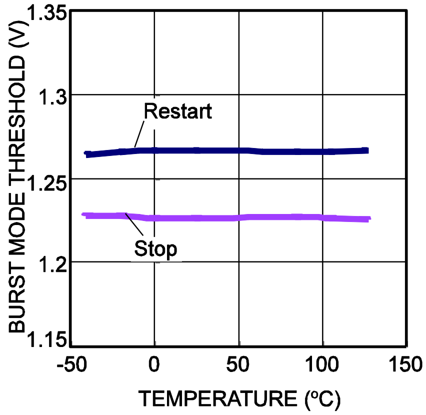


Oscillator Ramp vs. T_J

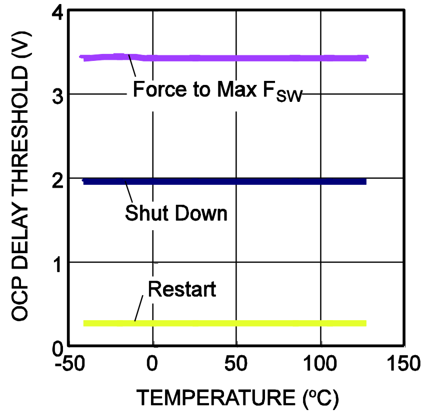


TYPICAL CHARACTERISTICS *(continued)*

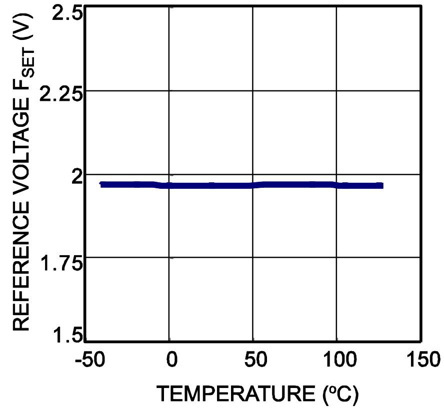
Burst Mode Threshold vs. T_J



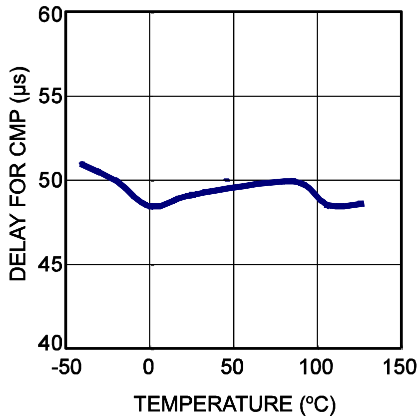
OCP Delay Threshold vs. T_J



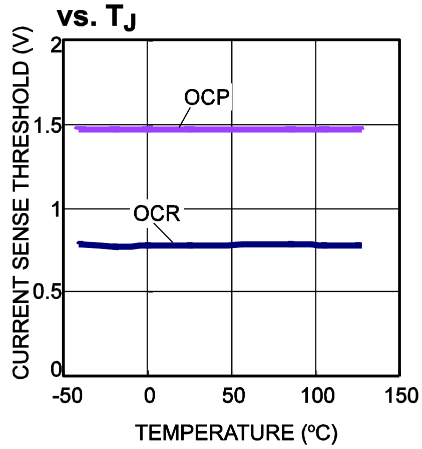
Reference Voltage F_{SET} vs. T_J



Delay for CMP vs. T_J



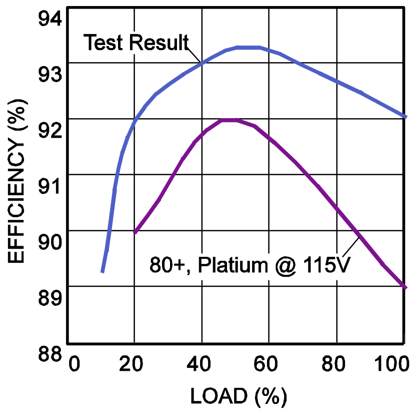
Current Sense Threshold vs. T_J



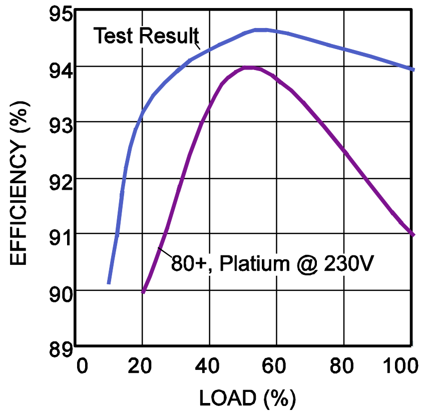
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 85V to 265V, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

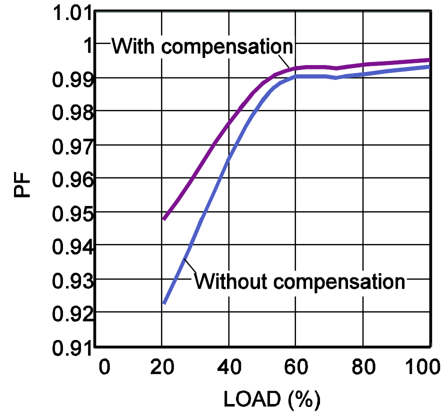
Efficiency
V_{IN}=115V, V_{OUT}=12V, P_{OMAX}=240W



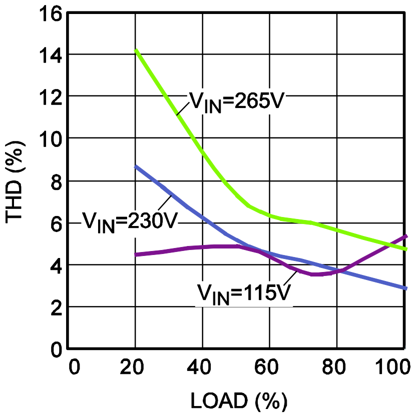
Efficiency
V_{IN}=230V, V_{OUT}=12V, P_{OMAX}=240W



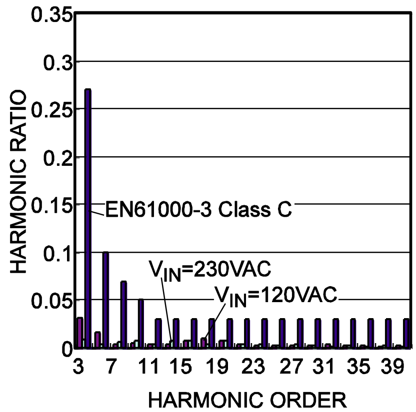
PF
V_{IN}=230V, V_{OUT}=12V, P_{OMAX}=240W



THD (%)
V_{OUT}=12V, P_{OMAX}=240W



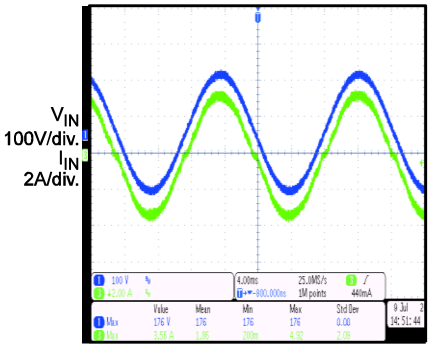
Harmonic
V_{IN}=120VAC/60Hz & 230VAC/50Hz, Full Load



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

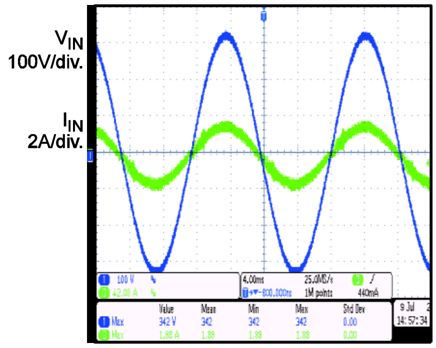
V_{IN} = 85V to 265V, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

Steady State @ Input
V_{IN} = 115VAC @ P_{OUT} = 240W



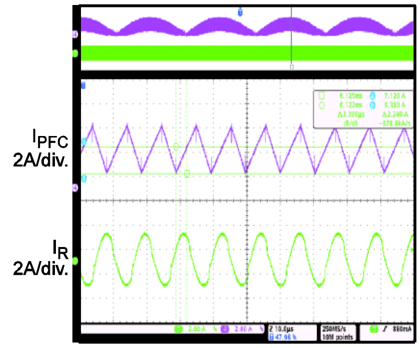
4ms/div.

Steady State @ Input
V_{IN} = 230VAC @ P_{OUT} = 240W



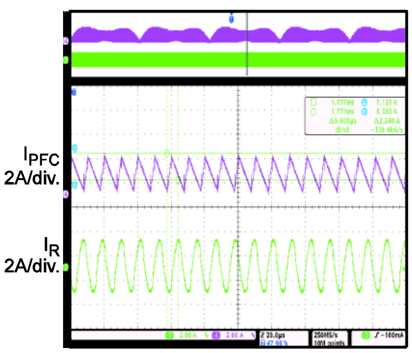
4ms/div.

Steady State @ I_{PFC} & I_R
V_{IN} = 120VAC @ P_{OUT} = 240W



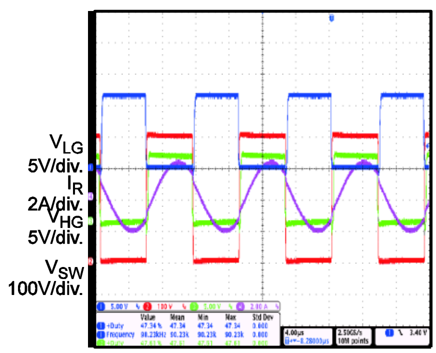
10μs/div.

Steady State @ I_{PFC} & I_R
V_{IN} = 230VAC @ P_{OUT} = 240W



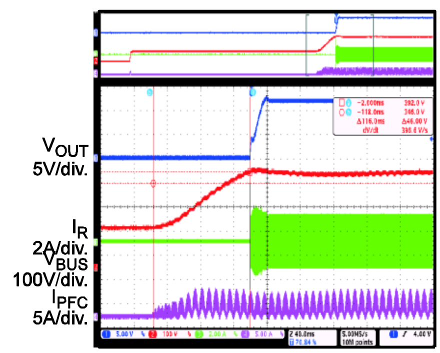
20μs/div.

Steady State @ LLC
P_{OUT} = 240W



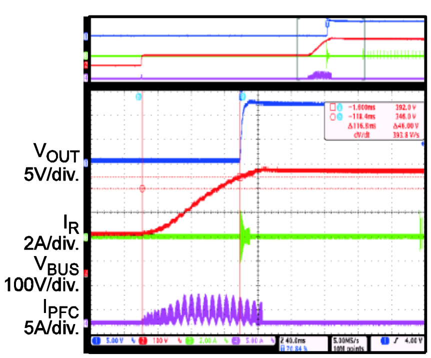
4μs/div.

Start-Up
V_{IN} = 115VAC @ P_{OUT} = 240W



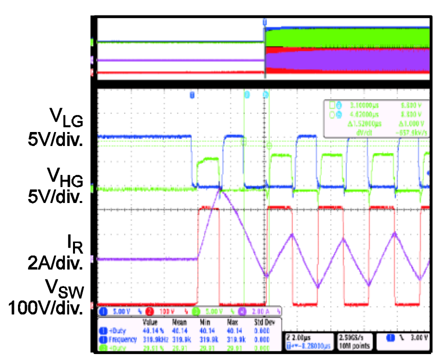
40ms/div.

Start-Up
V_{IN} = 115VAC @ P_{OUT} = 0W



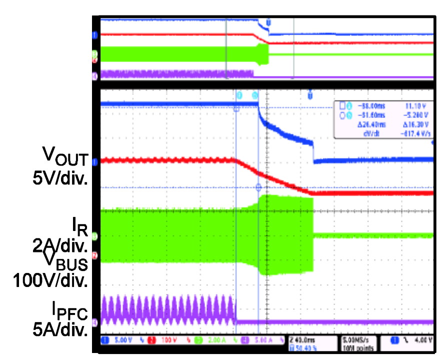
40ms/div.

Start-Up @ LLC
P_{OUT} = 240W



2μs/div.

Shutdown
V_{IN} = 115VAC @ P_{OUT} = 240W



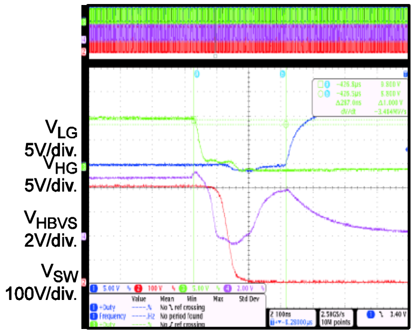
40ms/div.

NOT RECOMMENDED FOR NEW DESIGNS. REFER TO HR1203

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

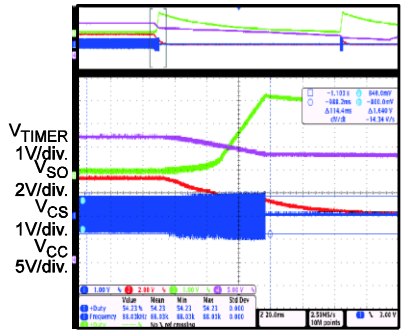
V_{IN} = 85V to 265V, V_{OUT} = 12V, I_{OUT} = 20A, T_A = 25°C, unless otherwise noted.

ADTA



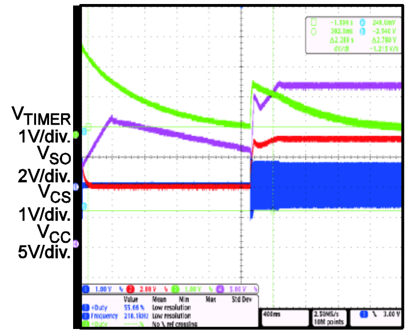
100ns/div.

Over-Current Protection



20ms/div.

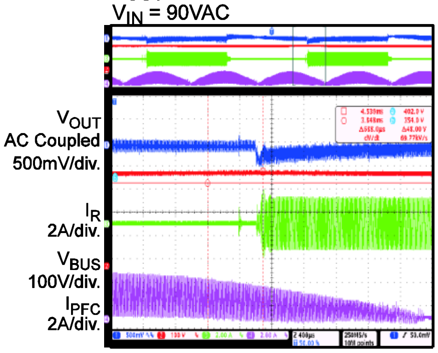
Over-Current Protection Recovery



400ms/div.

Load Transient

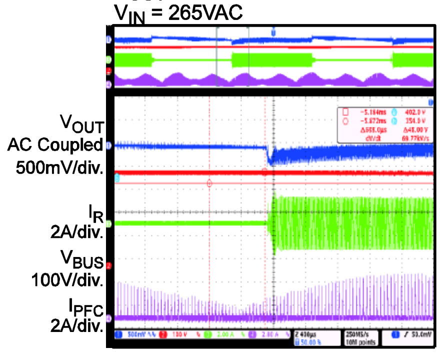
P_{OUT} = 0W to 240W, 1A/μs,
V_{IN} = 90VAC



400μs/div.

Load Transient

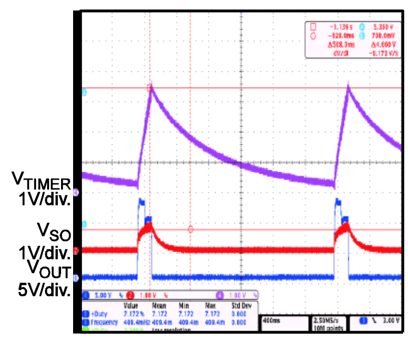
P_{OUT} = 0W to 240W, 1A/μs,
V_{IN} = 265VAC



400μs/div.

Start-Up Failure Protection

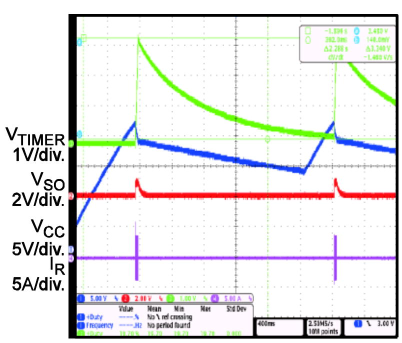
SO Pin Open



400ms/div.

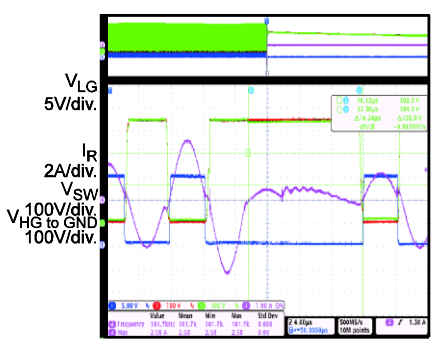
Start-Up Failure Protection

Output is Short



400ms/div.

Capacitive Mode Protection



4μs/div.

PIN FUNCTIONS

Package Pin #	Name	Description
1	SDA	**I²C data bus.** Connect a suitable pull-up resistor from SDA to V3.3.
2	ACIN	**Input voltage sensing.** ACIN is connected to ADC internally. The voltage is used for on-time calculation and brown-in/brown-out protection. The ratio of the external resistor divider should be 0.0032. It is recommended to connect a 680pF capacitor from ACIN to GNDD.
3	RES	**Reference current for producing system clock and bias voltage on CSP.** RES connects to a precise reference voltage of 1.25V internally. The reference current is produced by connecting a 20kΩ, 0.5% resistor externally from RES to GNDD.
4	CSP	**Sensing of the PFC inductor current.** Connect a 20kΩ, 0.5% resistor to CS to produce a bias voltage of 1.25V.
5	GNDD	**Ground reference for the digital core of the PFC.**
6	GNDP	**Ground reference of the PFC gate driver and the LLC low-side gate driver.**
7	GATEP	**Gate driver output of the PFC MOSFET.**
8	VREG	**Regulated power supply.** VREG provides a regulated power supply for the PFC and LLC gate drivers or external circuits.
9	LSG	**Low-side gate driver of HB.** The driver is capable of a minimum 0.7A sourcing current and a minimum 0.8A peak sinking current to drive the lower MOSFET of the half-bridge leg. LSG is actively tied to GND during UVLO.
10	TIMER	**Setting of protection and recovery time.** Connect a capacitor and a resistor from TIMER to GNDS to set both over-current protection delay and recovery delay.
11	SO	**Latch function for OVP and OTP.** If the SO voltage exceeds $V_{SO\text{-}Latch}$, the IC stops switching immediately and remains latched off until VCC drops below V_{CCRST}. When the LLC is enabled during start-up, if the SO voltage is still below $V_{SO\text{-}SFP}$ after the TIMER voltage reaches V_{th2}, the IC stops operating. Connect SO and GNDS with a noise-decoupling capacitor more than 100nF placed as close to the IC as possible.
12	VCC	**IC supply power.** When the power is on, VCC is charged up by HVCS internally at first and then by the auxiliary power supply.
13, 18	NC	**Not connected.** NC is not connected in SOIC28 package and removed in TSSOP28 package to increase creepage distance.
14	HV	**High-voltage current source for the IC start-up.** HV also acts as an X-cap discharger when the input voltage drops out.
15	BST	**Voltage bootstrap.** BST is connected externally to a capacitor to build a power supply to drive the high-side MOSFET of the HB LLC.
16	HSG	**High-side gate driver of HB.** HSG is the gate driver output for the high-side MOSFET of the HB LLC.
17	SW	**Reference of the high-side gate driver and bootstrap capacitor.**
19	HBVS	**Slope sensing to achieve adaptive dead-time adjustment.** Detect the dv/dt of the half-bridge mid-point. A 5pF high-voltage capacitor is recommended between SW and HBVS. LLC works with fixed dead-time (about 300ns) when HBVS is floating. Connecting HBVS to GNDS disables the LLC switching.
20	GNDS	**Ground reference of LLC and power management circuits.**

PIN FUNCTIONS *(continued)*

Package Pin #	Name	Description
21	CSHB	**Current sense of half-bridge.** The LLC current can be sensed by a sense resistor or a capacitive divider. CSHB has the following functions: **1. Over-current regulation:** As the voltage exceeds the V_{CS-OCR} threshold, the soft-start capacitor on SS discharges internally. The frequency increases, limiting the output power. An output short circuit results in a nearly constant peak primary current. A timer set on ACIN limits the duration of this condition. **2. Over-current protection:** If the current continues to build up (despite the frequency increase) when the CSHB voltage reaches V_{CS-OCP}, C_{SS} is discharged continuously, and OCP is not triggered immediately until $V_{SS} < V_{SS-OCP}$. If the condition for $V_{CS} > V_{CS-OCP}$ remains once V_{SS} drops below V_{SS-OCP}, the IC shuts down. C_{TIMER} continues to be charged by an internal 140µA current source until the TIMER voltage reaches V_{th2}. The IC resumes operation when the TIMER voltage falls below V_{th3}. **3. Capacitive mode protection:** The moment LSG is turned off, the CSHB voltage level is compared with a -80mV CMP threshold. If CSHB > -80mV, it blocks the HSG gate output until the slope comes down or the CMP timer runs out. Once HSG is turned off, CSHB is compared with a +80mV CMP threshold. If CSHB < +80mV, it blocks the LSG gate output until the slope comes up or the CMP timer runs out. As soon as capacitive mode is detected, the soft-start capacitor on SS discharges internally and the frequency increases. All functions are disabled when CSHB is connected to GND.
22	BURST	**Burst mode control.** If the voltage on BURST is lower than V_{th} (1.23V), the IC is disabled and resumes when the voltage exceeds 1.23V with a hysteresis of about 40mV. During burst mode, soft-start is not activated. This function helps reduce power loss at a lighter load.
23	FSET	**Switching frequency set.** Provide a precise and stable V_{REF} (1.97V) reference voltage. Current flowing out of FSET regulates the LLC switching frequency and output voltage. The minimum frequency is set via a resistor connected to GND. The resistor connecting the optocoupler and FSET sets the maximum frequency. An RC series connected from FSET to GND determines the specific operating frequency.
24	CT	**Time set.** Current flowing out of FSET is mirrored to charge and discharge the capacitor connected from CT to GNDS, which determines LLC switching frequency.
25	SS	**Soft-start for LLC.** Connect an external capacitor from SS to GND and a resistor to FSET to set both the maximum oscillator frequency and the time constant for the frequency shift during start-up. An internal switch discharges the capacitor when the chip is turned off to guarantee soft-start (all protections are listed except CMP).
26	V3.3	**A stable 3.3V voltage for digital PFC core or external circuit.** A 10µF decoupling ceramic capacitor is recommended to connect V3.3 and GNDS.
27	FBP	**Voltage sensing of PFC output.** The voltage of FBP is sampled by ADC. FBP is also used in on-time calculation, OVP, OLP, and digital PI. A 3.3MΩ pull-down resistor is connected internally. It is recommended to connect a 680pF capacitor from FBP to GNDD.
28	SCL	**I^2C serial clock input.** Connect a suitable pull-up resistor from SCL to V3.3.

BLOCK DIAGRAM

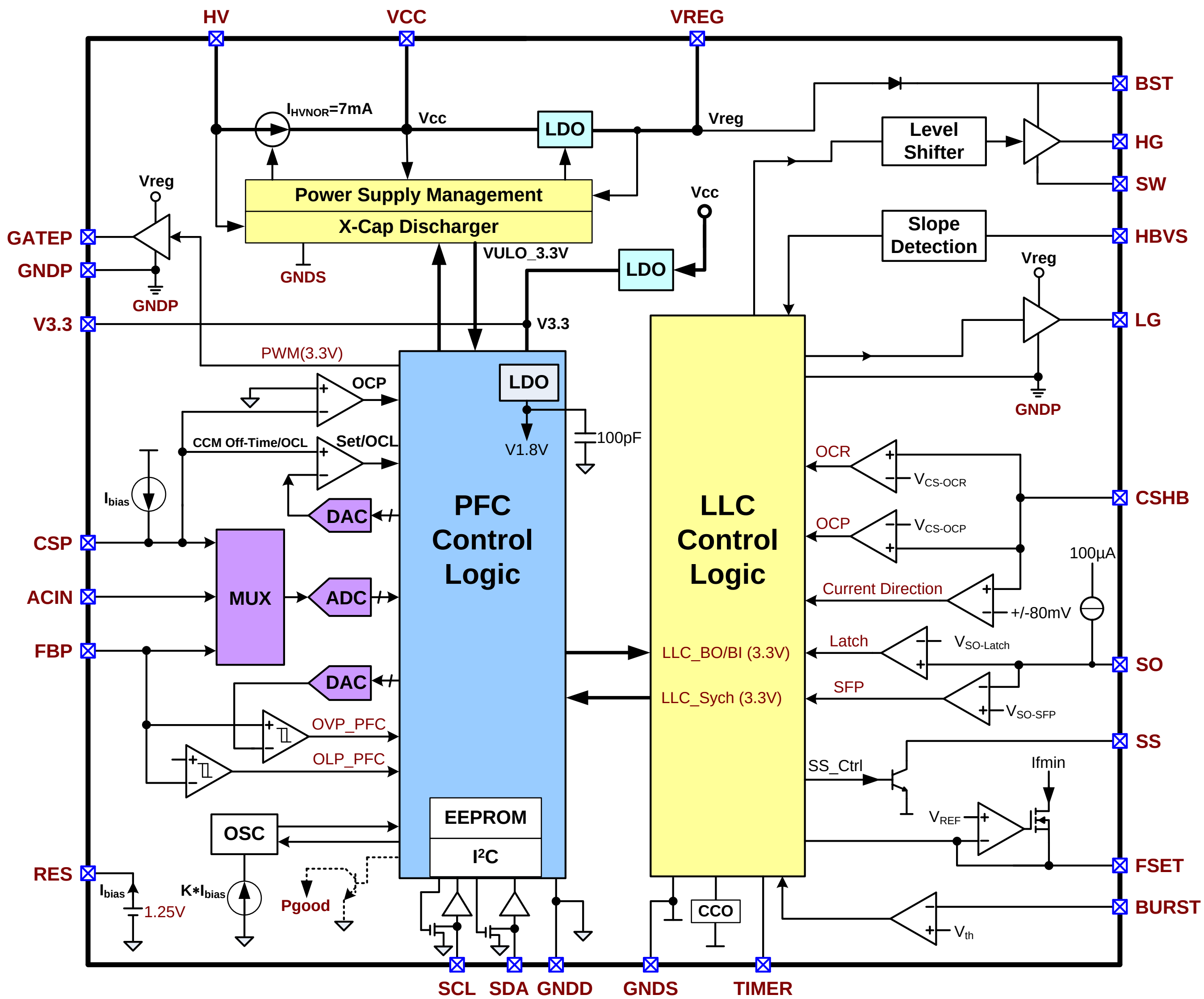


Figure 2: Functional Block Diagram

FUNCTION DESCRIPTION

The HR1200 is a high-performance combo controller that integrates digital PFC and HB LLC controllers.

EEPROM

The HR1200 applies EEPROM as the NVM. It has 1k bytes of data memory and 16 bytes of security memory.

There are only two commands used to operate the EEPROM:

1. Read all the data from EEPROM to the memory map. This process operates automatically before the controller runs or receives a RESTORE_USER_ALL command (51h) from the I²C.
2. Write all the data from the memory map to EEPROM. This process operates when it receives a STORE_USER_ALL command (50h) from the I2C.

I²C Communication and GUI

The HR1200 has a standard I²C interface. It is recommended to select an I²C tool with 100kHz clock frequency. The I²C can read and write the memory map. It can also send a command to load the data from EEPROM to memory map or reload the data from memory map to EEPROM with the graphic user interface (GUI) (see Figure 3). For details, please refer to the “User Guideline_HR1200 I²C Kit and GUI” and “User Guideline_HR1200 Layout” files available on the MPS website.

Power Supply Management

This section describes how the HR1200 produces and optimizes the power supply for circuits inside the IC. Optimized power source can reduce no-load consumption and provide robust operation with sufficient fault protection. A high-voltage current source is also integrated in the IC for start-up and X-cap discharge when the AC input drops out.

System Functions

This section describes functions that HR1200 integrates to improve system performance, including X-cap discharge, IC on/off control, a power good signal, and an interface between the PFC stage and LLC stage for synchronous operation.

Digital PFC Controller

The HR1200 uses a digital PFC controller integrating digital logic, ADC, DAC, and comparators to achieve PFC functionality. To acquire programmable design parameters, I²C communication functions and EEPROM are also included.

HB LLC Controller

The HB LLC converter can generate an isolated and regulated output voltage from the high voltage DC bus. With an adaptive dead-time control method, the HB LLC controller helps the converter operate in ZVS in a wider load range, improving the efficiency of the converter at light load. The IC implements anti-capacitive mode operation protection, allowing for robust product design.

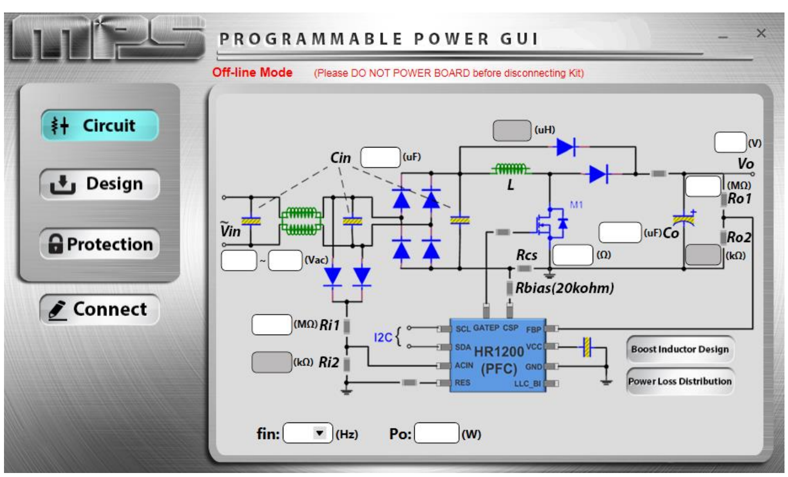


Figure 3: HR1200 I²C GUI

Part 1: Power Supply Management

The power supply management function is implemented via four output pins: HV, VCC, VREG, and V3.3. Figure 4 and Figure 5 show the block diagram and operation waveforms of the power management circuit.

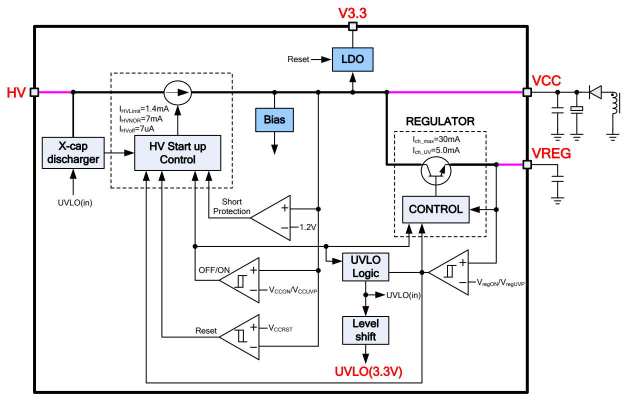


Figure 4: Block Diagram of Power Supply

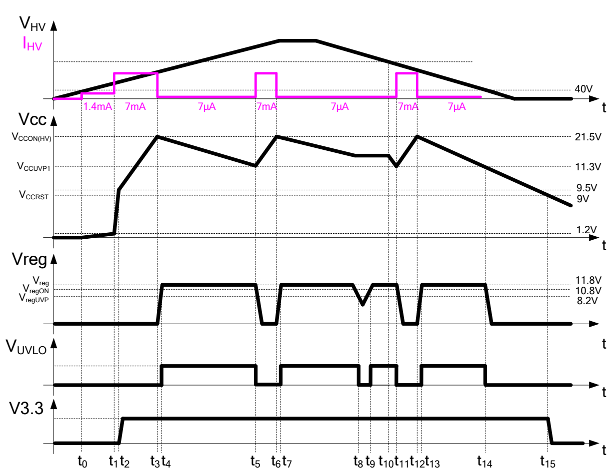


Figure 5: Operation Waveforms of Power Supply

High-Voltage Start-Up Input (HV)

A 7mA current source charges VCC internally when a voltage larger than 40V is applied to HV. If VCC is lower than 1.2V, the charge current from HV is limited to $I_{HVLimit}$ (1.4mA typically), to prevent excessive power loss caused by VCC short circuit during start-up.

During normal operation, the voltage on VCC rises quickly after start-up, and the HV current source switches to the nominal current I_{HVNOR} (7mA typically). I_{HVNOR} charges the capacitor connected to VCC externally, and VCC voltage ramps up. The HV current source is switched off when VCC voltage exceeds the start-up level $V_{CCON(HV)}$ (21.5V typically). The HV current source turns on again when VCC drops below V_{CCUVP1} (11.3V typically). Once the HV current source is turned off, the leakage current into HV should be below I_{HVoff} (7µA typically).

IC Supply Input (VCC)

VCC provides operational power for most of the internal circuits. Then the IC can start up with the HV start-up current source.

If the start-up current comes from HV when VCC reaches $V_{CCON(HV)}$, the internal LDO is powered on. VREG begins building up, and the IC starts operating if no fault condition occurs. Then VCC is powered by the auxiliary winding of the HBC transformer. Once VCC drops below V_{CCUVP1}, following actions occur:

- The IC stops operating, and the PFC controller stops switching immediately. But the HB LLC controller continues to operate until the low-side MOSFET becomes active.
- The VREG LDO is disabled.

The HV current source charges VCC until VCC reaches $V_{CCON(HV)}$, then VREG LDO is turned on again. If the IC enters latch mode, the latch status will remain until VCC falls below V_{CCRST}.

If VCC supplied by an external DC power source instead of HV current source, please refer to the HR1201 as an alternative.

Regulated Output (VREG)

An internal LDO is added to stabilize voltage in order to:

- Supply the internal PFC driver.
- Supply the internal low-side driver of HB LLC.
- Supply the internal high-side driver of HB LLC via a bootstrap diode.
- Supply a reference voltage.

The LDO is enabled only when VCC is higher than $V_{CCON(HV)}$. This ensures that any optional external circuitry connected to VREG does not dissipate any of the start-up current.

The IC starts switching only when VREG is higher than V_{regON} (10.8V typically). If VREG falls below V_{regUVP} (8.2V typically), the IC and the PFC controller stop switching immediately.

The HB LLC controller continues operating until the low-side MOSFET becomes active.

V3.3 for Digital Logic

V3.3 is a stabilized power supply for the internal digital logic. It is the output of an LDO with its input connected to VCC internally. The output of V3.3 is connected to a digital section with an internal bonding wire. When VCC is larger than V_{CCRST} plus a hysteresis of about 0.5V, the V3.3 LDO is enabled. It can be disabled only when VCC is lower than V_{CCRST}.

The capacitor on V3.3 should be in the range of 4.7µF to 10µF to guarantee that V3.3 is stable.

Out from the 3.3V LDO, there is another LDO with 1.8V output downstream for powering the internal digital circuits.

UVLO (3.3V signal)

The UVLO (3.3V signal) is an enable signal for both the digital PFC and LLC controller. When VCC is larger than V_{CCUVP1}, and VREG is larger than V_{regON}, UVLO (3.3V signal) goes high.

Part 2: System Functions

X-Cap Discharger

X-caps are critical components placed at the input terminals of the power supply to filter out differential mode EMI noise. If the AC line voltage is removed, the redundant voltage on X-caps may cause harm to the user. Safety standards require the voltage to be discharged to a safe level within a certain time frame.

Commonly, resistors are placed in parallel with X-caps across the AC line to provide a discharge path. However, extra resistors bring continuous power consumption as long as the AC input is connected, which is the significant contributor to power consumption at no-load or standby conditions.

The HV current source in the HR1200 acts as a smart X-cap discharger when the AC input is removed. So, traditional discharge resistors can be eliminated. Operating waveforms are shown in Figure 6.

In a normal stage, the HV current source is off. The leakage current in HV is small, so power consumption is reduced significantly. Once the AC voltage is disconnected, after a detection time window (Timer 1, 96ms typically), the IC controls the internal 7mA current source automatically to discharge energy from the X-cap to VCC within the Timer 3 period (48ms typically). The IC stops for an additional Timer 3 period to detect the AC. If no AC is re-applied during this last time period, the IC continues discharging during the Timer 2 period (144ms typically) until V_{HV} is below 35V. Once V_{HV} drops below 35V, VCC is discharged quickly by the internal current source, which speeds up recovery when the IC is in latch mode.

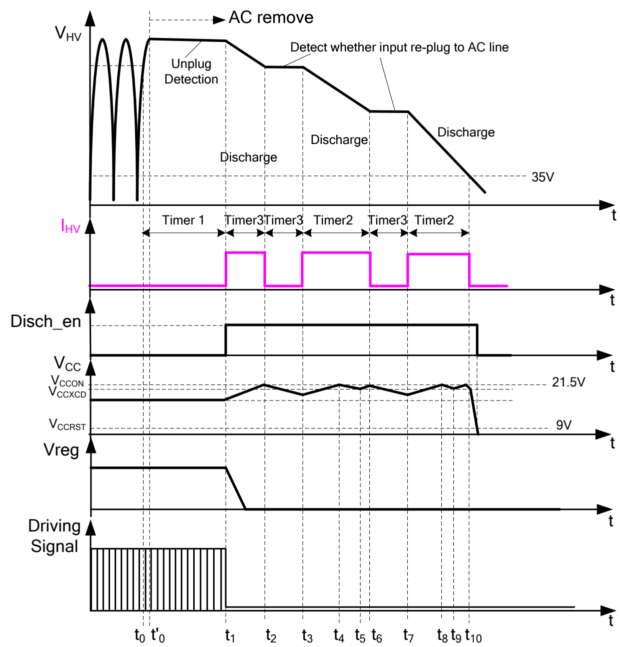


Figure 6: Operating Waveforms of X-Cap Discharger when AC Removed

If the AC recovers in HV again during the Timer 3 period, a new start-up procedure begins (see Figure 7).

If the X-cap discharge function is enabled, VCC should be regulated between V_{CCON} and V_{CCXCD} to avoid over-stressing VCC.

The X-cap discharge function is very flexible, and allows users to choose an X-cap value to optimize differential mode EMI filtering without worrying about the effect of the required bleed resistors on the standby power budget and system no-load.

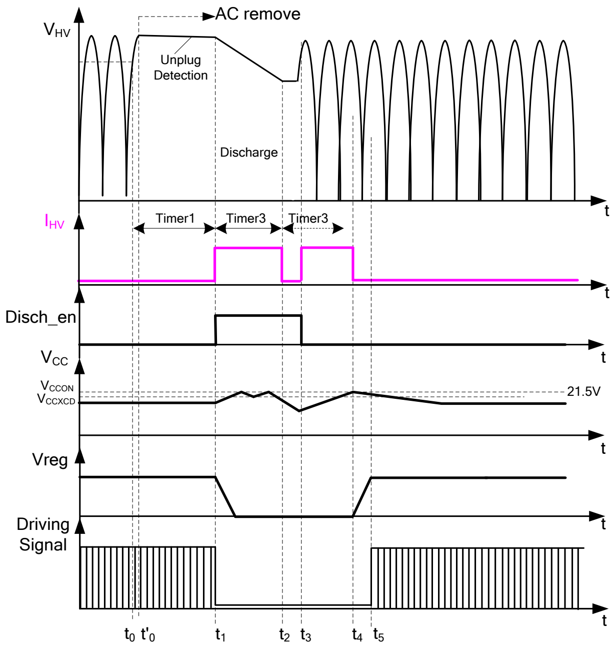


Figure 7: Operating Waveform of X-Cap Discharger when AC Recovered

Over-Temperature Protection (OTP)

Once the internal thermal sensor senses the IC temperature is over 145°C, the IC stops switching immediately. Both the LDO for VREG and V3.3 are disabled. If the IC temperature rises above 100°C, the high-voltage current source is disabled. The IC is enabled again when VCC drops below V_{CCRST}. If the IC temperature drops below 100°C, the IC starts up again.

IC On/Off Control

The IC is turned off by pulling FBP down to GND with an external MOSFET (see Figure 8). If the FB voltage is less than 0.2V, both the PFC and LLC disable the PWM switching during startup or operation. When the FBP voltage is higher than 0.3V, the IC is turned on again. Besides, the IC can be turned off from the secondary side through an optocoupler.

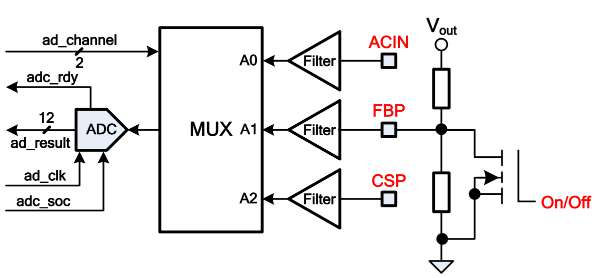


Figure 8: IC On/Off Control

The IC can be disabled by programming the EEPROM through the I²C GUI (see Table 1).

Table 1: IC Disabled through I²C and MPS' GUI

Resister address	56h							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function			IC enable: "1", enable IC "0", disable IC	LLC enable: "1", enable LLC "0", disable LLC				

PFC and LLC Interface

There are two signals between the PFC and the LLC part:

1. D2D brown-in/out signal (see Figure 9)

If the output voltage is higher than V_{D2D_BI}, the D2D_BI/BO signal is set high, enabling the LLC stage. The LLC stage is disabled when the output voltage drops below V_{D2D_BO}. This function guarantees the LLC operates within a proper input voltage range, preventing the LLC from running in capacitive mode.

V_{D2D_BI} and V_{D2D_BO} are programmable through I²C. The register address for V_{D2D_BI} is one word (16h, 17h). The register address for V_{D2D_BO} is one word (18h, 19h). The value in the register can be calculated with Equation (1):

$$\text{DEC2HEX}\left(V_{D2D\_BI/BO} \times 0.0032 \times \frac{1023}{1.6}\right) \quad (1)$$

2. LLC burst synchronize signal

When the LLC operates in burst mode, the PFC burst mode can be synchronized with the LLC burst mode. This is achieved by setting bit 7 of register 56h high. When bit 7 is low, the LLC and PFC burst independently.

Part 3: PFC Controller

The state-of-the-art CCM/DCM control scheme can reduce the RMS current drawn from the AC mains by ensuring good shape of the input current both in CCM and DCM. The control scheme reduces the switching frequency when the load is reduced, therefore achieving higher efficiency and higher power factor at light load.

Digital PFC Timing

Figure 9 shows the timing of the digital PFC block.

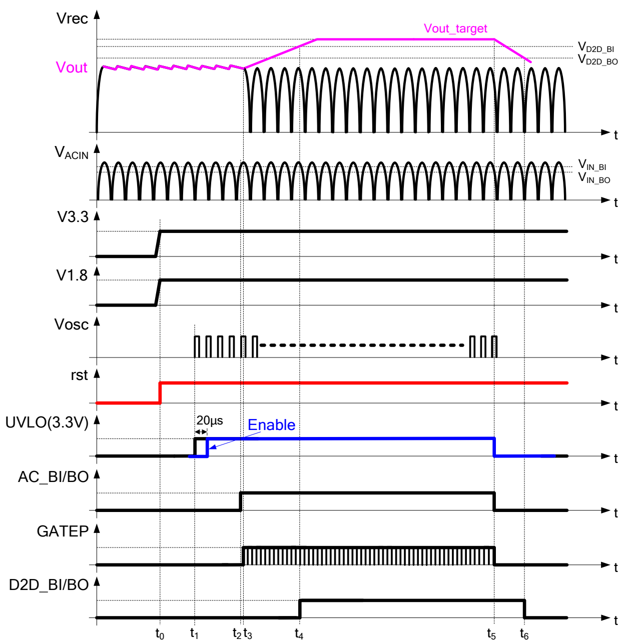


Figure 9: Power Supply Sequence of Digital Controller

Timing of the Power Supply

Once VCC rises above V_{CCRST} plus a hysteresis of about 0.5V, the V3.3 LDO is enabled and an internal LDO downstream produces a stable 1.8V power supply for the internal digital logic and system clocks. The rst signal is set high when both 3.3V and 1.8V are stable. When UVLO (3.3V signal) is validated, the IC enables OSC, ADC, DAC, and relative comparators. The enable signal is set high after a delay of 20µs, which indicates the digital core is ready to begin operation.

Timing of the Digital Core

If the enable signal is high, ADC begins sampling V_{ACIN} and V_{FBP}. If the AC input meets the brown-in condition and no open-loop fault is found on FBP, the AC_BI/BO signal is set high. The PFC soft starts until the output reaches the target value. While the PFC output voltage ramps up above $V_{D2D\text{-}BI}$, D2D_BI/BO is set high. the downstream LLC starts operating.

Reference Current (RES)

RES is connected internally to a precise reference voltage of 1.25V (see Figure 10). RES should be connected to a 20kΩ, 0.5% resistor externally. Reference current about 62.5µA is then generated. The current is mirrored and flows out of CSP. If CSP is also connected externally to a 20kΩ resistor, a bias voltage of 1.25V on CSP is produced, which keeps the CSP voltage positive (see Figure 11).

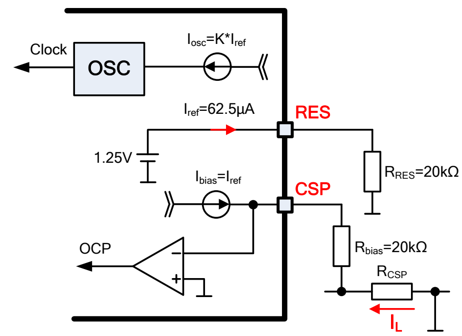


Figure 10: Reference Current

Moreover, the reference current is mirrored to produce a system clock (see Figure 11).

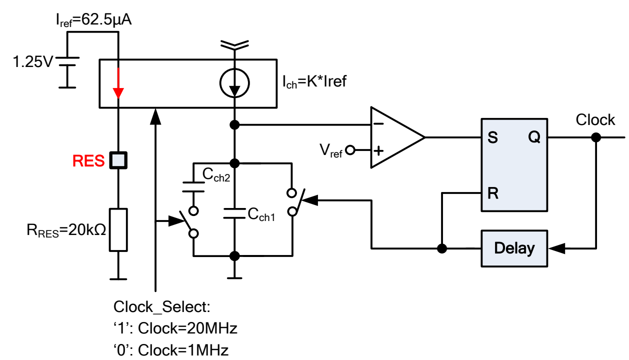


Figure 11: System Clock Generator

The system clock switches from 20MHz to 1MHz when PWM is disabled (i.e. burst off, OVP, OCP, etc.) in order to reduce IC power consumption.

Input Voltage Sensing

The input voltage is rectified and attenuated by a resistor divider with a fixed ratio (0.0032) before provided to the ACIN input. Then, the ADC samples the voltage on ACIN including the instantaneous value, the peak value, and the frequency of the input voltage. The data are used for on-time calculation, AC brown-in/out protection, capacitor current compensation and X-cap discharge.

Figure 12 shows the input voltage level defined for different functions. All parameters can be programmed through the I^2C Kit and MPS' GUI.

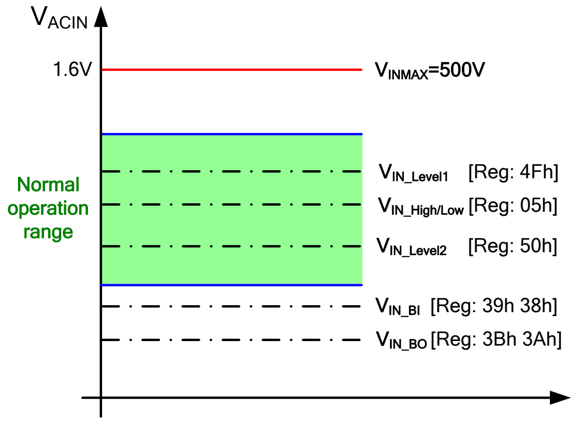


Figure 12: Input Voltage Level for Different Functions

Input Brown-In/Brown-Out

If V_{ACIN} is larger than the brown-in threshold (V_{IN_BI}), it means the IC is ready to switch. If V_{ACIN} is less than the brown-out threshold (V_{IN_BO}) for the length of one timer period, the IC stops switching. V_{IN_BI} and V_{IN_BO} are 10-bit values that are stored in the registers from 38h to 3Bh. The values can be calculated with Equation (2):

$$\mathrm{DEC2HEX}\left(V_{IN\_BI/BO} \times 0.0032 \times \frac{1023}{1.6}\right) \quad (2)$$

The brown-in and brown-out timer is set in register 3Ch (see Table 2).

Table 2: Brown-In/Out Timer in Register 3Ch

Bit	Item	Description
7:4	VIN_BI_TIME	Brown-in time
3:0	VIN_BO_TIME	Brown-out time

High/Low Line

The low line is determined when the input voltage is lower than $V_{IN\_High/Low}$. The high line is determined when the input voltage is larger than $V_{IN\_High/Low}$ plus a hysteresis of about 10V. The high/low-line signal sets the soft-start time and the resonant time for valley turn-on. It also regulates the output voltage at different levels to optimize the efficiency of the PFC stage.

V_{IN_Level1}, $V_{IN\_High/Low}$ and V_{IN_Level2} separate the input voltage into four ranges to achieve different compensation values to improve PF at different input voltage ranges.

The thresholds are 8-bit data. The value can be set according to Equation (3):

$$\mathrm{DEC2HEX}\left(V_{IN\_High/Low} \times 0.0032 \times \frac{256}{1.6}\right) \quad (3)$$

Output Voltage Sensing

Similar to input voltage sensing, the output voltage is attenuated by a resistor divider before connected to FBP. Then the voltage on FBP is sampled by ADC. The results are used for on-time calculation and a series of protections.

The internal pull down resistor of 3.3MΩ should be considered when designing the external resistors. Make the total divided ratio to 0.0032 according to Equation (4):

$$\frac{R_{FBL-L} // 3.3M\Omega}{R_{FBL-H} + (R_{FBL-L} // 3.3M\Omega)} = 0.0032 \quad (4)$$

Where RFBL-H is the divider resistor connected on high-side and RFBL-L is the divider resistor connect on low-side.

Figure 13 shows the output voltage level that is defined for different functions. All parameters can be programmed through the I^{2}C GUI.

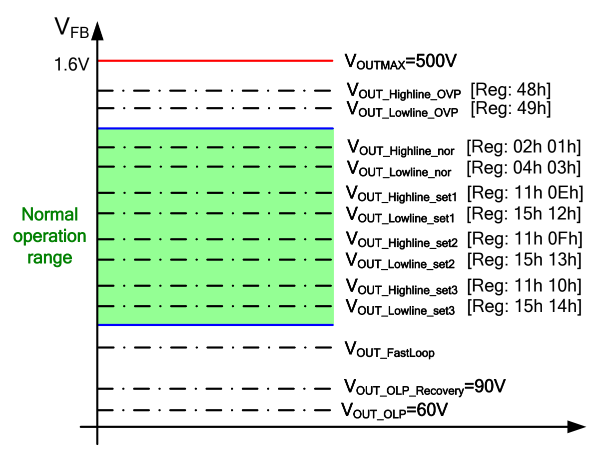


Figure 13: Output Voltage Level for Different Functions

Output Regulation

To optimize efficiency, the output voltage can be auto-regulated according to the input voltage and output power. The output voltage is divided into two ranges by $V_{IN\_High/Low}$ and is divided into four ranges according to the output power level, which can be programmed by registers from 06h to 0Bh. Therefore, the IC can auto-regulate eight output voltages accordingly.

Output Fast OVP

$V_{OUT\_Highline\_OVP}$ and $V_{OUT\_Lowline\_OVP}$ are 7-bit values stored in register 48h and 49h. They are programmable through the I²C GUI (430V typically). A 7-bit DAC converts V_{OUT_OVP} to an analog signal and compares the result with FBP voltage. If output voltage is larger than V_{OUT_OVP}, the PFC stops switching. Once output voltage decreases to regulation voltage, the PFC resumes switching. Figure 14 shows the OVP circuit.

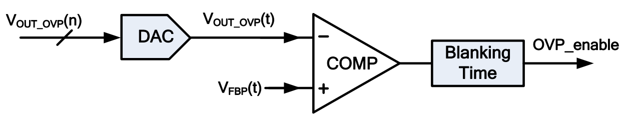


Figure 14: OVP Circuit

A blanking time is inserted in OVP, keeping the IC immune to switching noise interference (see Figure 15). Both of T_{OVP_T} and T_{OVP_R} are programmable in register 60h.

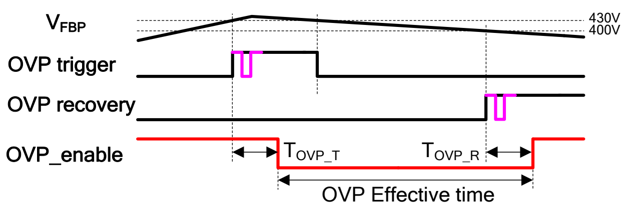


Figure 15: Output Fast OVP

Fast Loop

In a dynamic load event, the PFC output voltage decreases due to the low bandwidth of the voltage control loop, which may cause the output voltage to fall out of the regulated range. Fast loop is activated when the output voltage is lower than $V_{OUT\_FastLoop}$. Then Ki and Kp of the digital PI are changed with X times the normal value, depending on the GUI setting. In this way, the output voltage of the PFC is regulated faster in the dynamic load event.

Open Loop or IC Disable Condition

If the FBP voltage is less then V_{OUT_OLP} (60V typically), it is considered to be an open-loop or IC disable condition. The IC does not work and PWM switching is disabled during operation. The IC restarts only when the FBP voltage is larger than $V_{OUT\_OLP\_Recovery}$ (90V typically). The open loop is achieved by software and the value is fixed.

Peak Current Sensing

The PFC inductor current is sensed by R_{CSP} and produces a negative voltage. A precise current source (I_{bias}) exits CSP and produces a positive bias voltage on R_{bias} (see Figure 16).

The CSP voltage is calculated with Equation (5):

$$V_{CSP}(t) = V_{CSP\_Bias}(t) - V_{CS}(t) \quad (5)$$

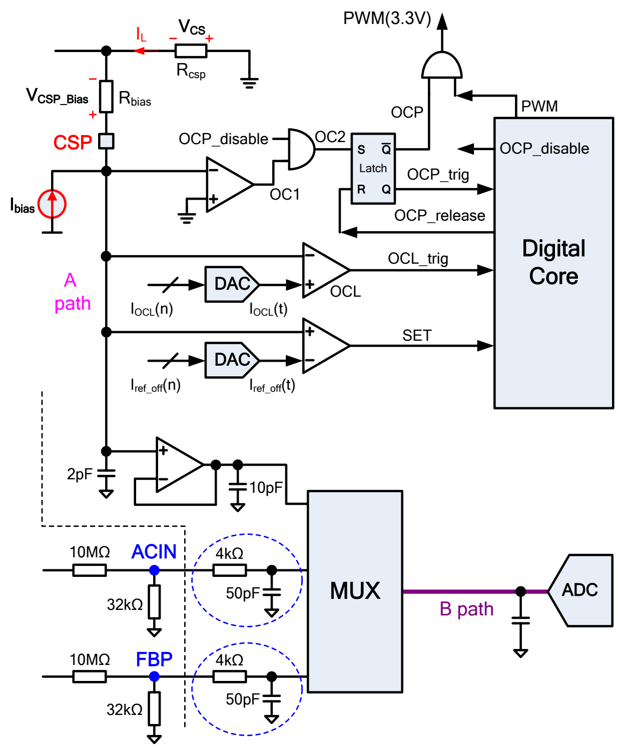


Figure 16: Current Sense Circuit in CSP

Overall, the CSP voltage is positive (see Figure 17). The ADC samples V_{CSP_Bias} (1.25V typically) regularly.

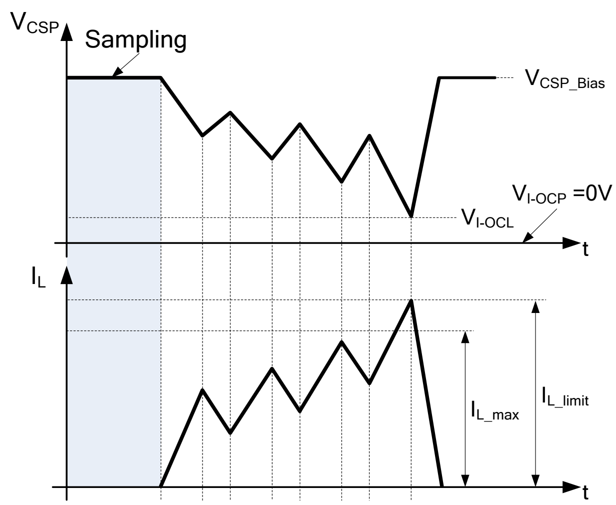


Figure 17: Voltage Waveform in CSP

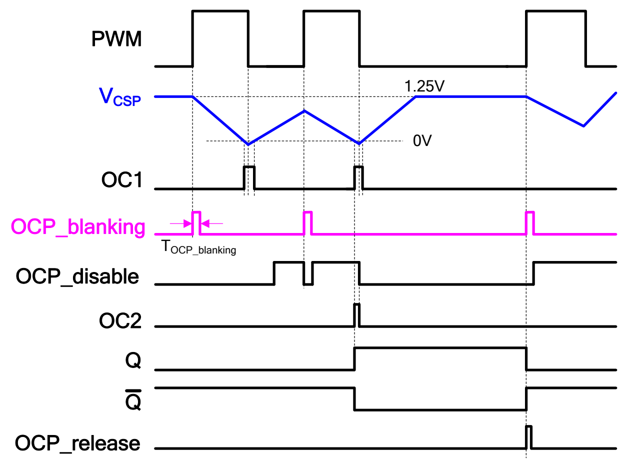


Figure 18: OCP Operation Waveform

Over-Current Protection (OCP)

If the CSP voltage is less than zero, over-current protection is enabled. The PFC stops switching immediately, and OCP_trig is set high simultaneously. The digital core detects this status and disables the PWM. OCP can be released by the OCP_release signal.

The OCP function is disabled by setting bit 3 of register 45h to logic low. The OCP behavior mode can be programmed by setting bit 2 to bit 0 of register 45h. It can be hiccup, latch or auto-restart with a delay time. The default setting is hiccup. The delay time is set in register 46h.

A programmable LEB1 ($T_{OCP\_blanking}$) of about 200ns is implemented to avoid error sensing due to switching noise.

The OCP function can avoid over-stressing when the inductor is shorted, or when the current is too large.

Figure 18 shows the operating waveforms of the OCP function.

Over-Current Limit (OCL)

The inductor current exists a cycle-by-cycle limit by setting the appropriate R_{CSP} and $V_{I\text{-}OCL}$. $V_{I\text{-}OCL}$ can be programmed in register 44h, and it can be converted to an analog signal by a 7-bit DAC. A programmable LEB1 ($T_{OCL\_blanking}$) of about 200ns is inserted to avoid switching noise if the digital core is turned on (similar to $T_{OCP\_blanking}$).

Digital PFC Control Scheme

Figure 19 shows the flowchart of the digital PFC control scheme.

Digital Current Reference

The digital PI compensates for the voltage loop. Its output $V_{comp}(n)$ is sent to the multiplier for current reference calculation (see Figure 20).

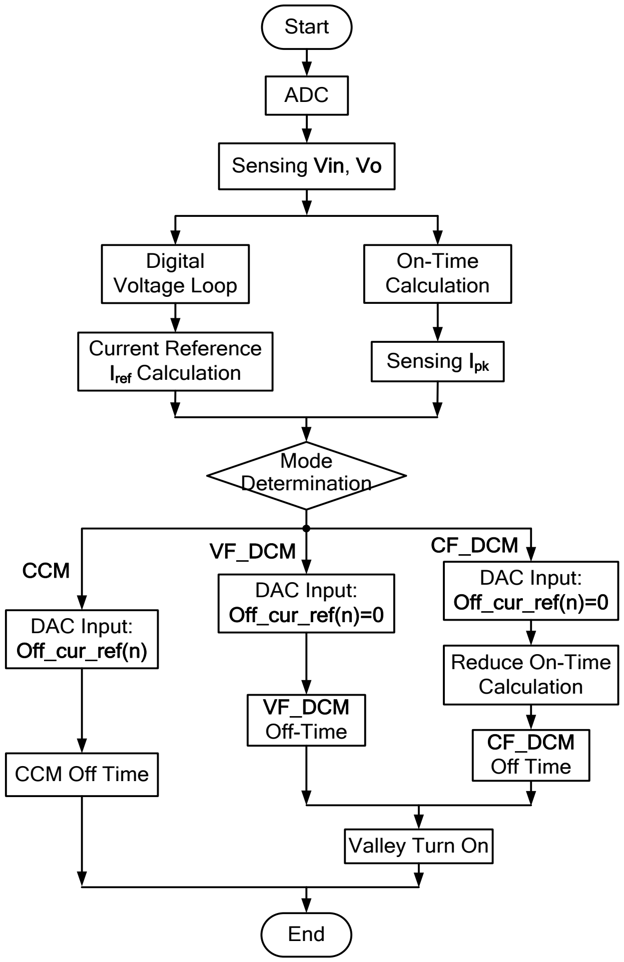


Figure 19: Flowchart of PFC Control Scheme

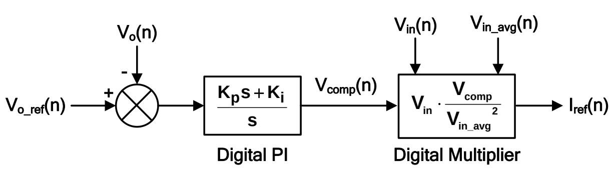


Figure 20: Current Reference

The digital current reference can be calculated with Equation (6):

$$I_{ref}(n) = V_{in}(n) \cdot \frac{V_{comp}(n)}{(0.5 \cdot V_{in\_pk}(n))^2} \qquad (6)$$

On-Time Calculation

The on-time can be calculated with Equation (7):

$$T_{on}(n) = \frac{V_{o\_ref} - V_{in}(n)}{V_{o\_ref}} \cdot T_s \qquad (7)$$

where T_S is the switching period, programmable in registers from 1Eh to 22h.

Mode Decision

The HR1200 has three operation modes: continuous conduction mode (CCM), variable frequency discontinuous conduction mode (VF-DCM), and constant frequency discontinuous conduction mode (CF-DCM).

The peak value of the inductor current in CCM should satisfy Inequality (8):

$$I_{pk}(n) < 2\, I_{ref}(n) \qquad (8)$$

The peak value of the inductor current in VF-DCM should satisfy Inequality (9):

$$2\, I_{ref}(n) < I_{pk}(n) < 2\, I_{ref}(n) \cdot \frac{T_{s\_max}}{T_s} \qquad (9)$$

The peak value of the inductor current in CF-DCM should satisfy Inequality (10):

$$I_{pk}(n) > 2\, I_{ref}(n) \cdot \frac{T_{s\_max}}{T_s} \qquad (10)$$

where T_{s_max} is the maximum switching period, programmable in registers from 23h to 27h.

1. CCM Operation

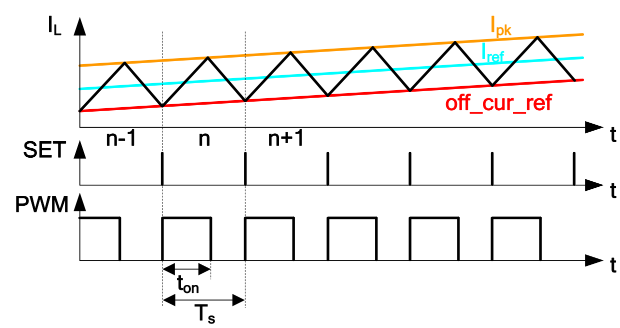


Figure 21: CCM Control Signals

When the converter operates in CCM, the off_cur_ref(n) is calculated and sent to DAC. The output of the DAC is an analog signal off_cur_ref(t) and is compared with $V_{CS}(t)$. If $V_{CS}(t)$ is lower than off_cur_ref(t), the signal will be set high. The PWM signal is set high accordingly (see Figure 21).

The off current reference at CCM can be calculated with Equation (11):

$$off\_cur\_ref(n) = 2\, I_{ref}(n) - I_{pk}(n) \qquad (11)$$

2. VF-DCM Operation

When the converter operates in VF-DCM, the off current reference is set to zero. In this case, the set signal represents the boundary of DCM (see Figure 22).

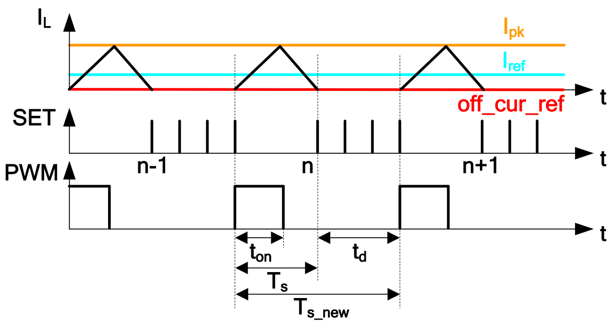


Figure 22: VF-DCM Control Signals

The new switching period is calculated with Equation (12):

$$T_{s\_new}(n) = \frac{I_{pk}(n)}{2I_{ref}(n)} T_s \quad (12)$$

The delay time is calculated with Equation (13):

$$t_d(n) = T_{s\_new}(n) - T_s = \left(\frac{I_{pk}(n)}{2I_{ref}(n)} - 1\right) \cdot T_s \quad (13)$$

3. CF-DCM Operation

When the converter operates in CF-DCM, the off current reference is set to zero. In this mode, the switching frequency is limited to the minimum switching frequency (see Figure 23).

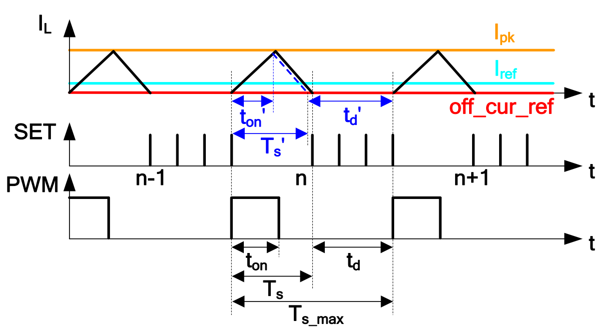


Figure 23: CF-DCM Control Signals

The PWM duty is modulated to achieve average current control. The new switching period is calculated with Equation (14):

$$T_s'(n) = \frac{2I_{ref}(n)}{I_{pk}'(n)} \cdot T_{s\_max} \quad (14)$$

As t_{on} changes minimally, the peak value of inductor current can be seen as unchanged. See Equation (15):

$$I_{pk}'(n) = I_{pk}(n) \quad (15)$$

The new turn-on time can be calculated with Equation (16):

$$t_{on}'(n) = \frac{V_{o\_ref} - V_{in}(n)}{V_{o\_ref}} \cdot T_s'(n) \quad (16)$$

The delay time is calculated with Equation (17):

$$t_d'(n) = T_{s\_max} - T_s'(n) = \left(1 - \frac{2I_{ref}(n)}{I_{pk}(n)}\right) \cdot T_{s\_max} \quad (17)$$

Soft Start (SS)

Once the AC input voltage is larger than V_{IN_BI}, the Vin_ok signal pulls high, and the HR1200 initiates a soft-start sequence (see Figure 24).

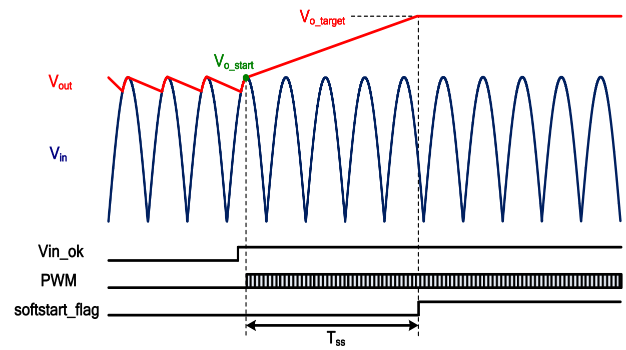


Figure 24: Soft-Start Sequence

The output voltage rises from the rectified output voltage to the target value. When softstart_flag is set high, the soft-start sequence is completed.

The soft-start time can be calculated with Equation (18):

$$T_{ss} = (V_{o\_target} - V_{o\_start}) \cdot \frac{2^{bit\_num} - 1}{V_{adc\_ref}} \cdot slewrate \quad (18)$$

where V_{o_target} is the target value of the output voltage, V_{o_start} is the soft-start value of the output voltage, bit_num is the ADC data bit (12 typically), V_{adc_ref} is the reference voltage of ADC (1.6V typically).

The slew rate is different at high line and low line. The slew rate at high line is programmable in register 1Ch; the slew rate at the low line is programmable in register 1Dh.

Burst-Mode Operation

At light load, the IC is always designed to run in burst mode for better efficiency or less no-load power consumption. Once the output load is lower than the threshold (e.g. 3% rated load), the PFC enters burst mode. The threshold can be programmed in register 2Dh for high line and register 2Fh for low line. In burst mode, the switching duty is calculated based on the 3% rated load. The output is regulated to V_{o_target} with a 5V hysteresis. The PFC keeps switching when the output voltage is below $V_{o\_target}-5V$. The PFC stops switching when the output voltage ramps up to V_{o_target}.

Burst-mode operation is synchronized with the LLC_sync signal. If the LLC_sync signal is high, the PFC PWM switching is turned off. Once the output voltage is lower than $V_{o\_target}-5V$, the PFC is turned on again even if the LLC_sync signal is high. This status continues until the output voltage ramps up to V_{o_target}.

When the PFC recovers from burst mode, it operates in critical conduction mode (CRM) for the first five switching cycles.

Capacitor Current Compensation

Traditional PFC control schemes only regulate the inductor current to match the shape of the input voltage. However, the input capacitor current is not controlled which may cause PF deterioration and undesired delay. With a larger capacitor or a higher input voltage, the PF even worsens.

To improve the PF, the HR1200 implements a patented method to compensate for PF deterioration. Relevant data are stored in registers from 4Bh to 4Eh, corresponding to different input voltage levels. With this function, the PF is improved at all input voltage levels.

Frequency Jittering

In order to reduce the EMI noise, the switching frequency is designed to be modulated by a triangular waveform with the frequency of f_m. The switching frequency is modulated to the maximum value at the peak of the triangle and to the minimum value at its valley. Figure 25 shows the algorithm modulating the switching frequency.

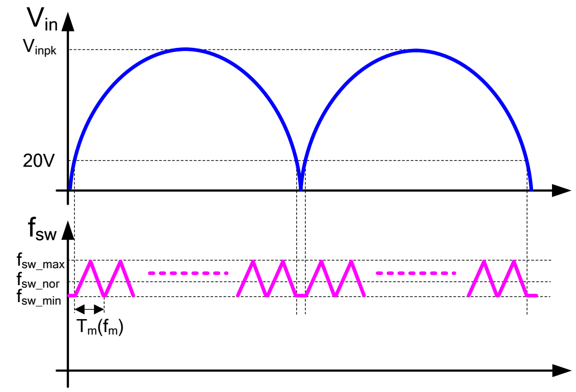


Figure 25: Frequency Jittering

The parameters of f_{sw_max}, f_{sw_min}, and f_m can be programmed by the I²C GUI for the best EMI performance.

Part 4: LLC Controller

Oscillator (FSET)

Figure 26 shows the block diagram of the oscillator. A modulated current charges and discharges the capacitor on CT. The voltage on the capacitor swings between the peak threshold and the valley threshold to determine the oscillator frequency.

The source current of FSET controls the current source I_{S-1} to charge the CT capacitor. Here, the current mirror ratio inside the HR1200 is 1A/A. When an oscillating cycle starts, I_{S-1} charges the CT capacitor until the voltage triggers the peak threshold voltage. The discharge current source I_{S-2} which is twice the source current of FSET is then turned on. Therefore, the CT capacitor is discharged with the source current of FSET. When the voltage on the CT capacitor drops to the valley threshold voltage, the I_{S-2} is turned off, and a new oscillating cycle repeats.

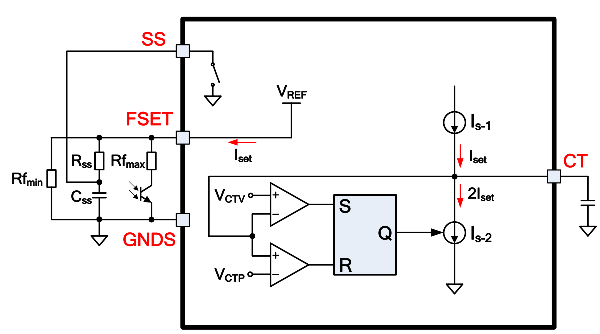


Figure 26: Oscillator Block Diagram

When VCC reaches the turn-on threshold, VREG starts to ramp up. As soon as VREG exceeds V_{regON}, CT begins to be charged and LSG switches on first. When CT ramps up to V_{CTP}, LSG switches off and CT holds for a period of dead time. Once the dead time expires, CT drops down and HSG switches on. HSG keeps working until CT drops down below V_{CTV}, HSG is turned off. A full switching cycle repeats unless VCC is lower than V_{CCUVP}. Figure 27 shows the detailed CT waveform from start-up to steady state.

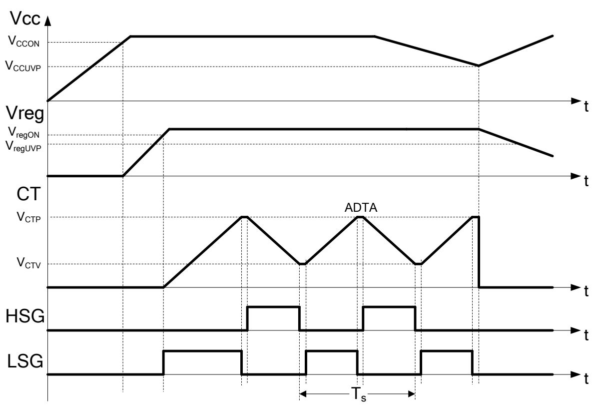


Figure 27: CT Waveform from Start-Up to Steady State

The RC network connected externally to FSET determines the switching frequency and the soft-start switching frequency.

Rf_{min} connected from FSET to GND contributes to the maximum resistance of the external RC network when the phototransistor is blocked. Therefore, it sets the minimum source current from FSET, which determines the minimum switching frequency.

Under normal operation, the phototransistor controls the current through Rf_{max} to modulate the frequency for output voltage regulation. When the phototransistor is saturated, the current through Rf_{max} is at its maximum, thus setting the maximum switching frequency.

An RC tank connected in series between FSET and GND is used to shift the frequency during start-up (see the “Soft Start” section for details).

The operation period can be expressed with Equation (19):

$$f_s = \frac{1}{3 \cdot CT \cdot R_{FSET}} \quad (19)$$

where R_{FSET} represents the total equivalent resistor on FSET.

The minimum and maximum frequency can be calculated with Equation (20) and Equation (21):

$$f_{min} = \frac{1}{3 \cdot CT \cdot Rf_{min}} \quad (20)$$

$$f_{max} = \frac{1}{3 \cdot CT \cdot (Rf_{min} \parallel Rf_{max})} \quad (21)$$

The values of Rf_{min} and Rf_{max} can be extracted:

$$Rf_{min} = \frac{1}{3 \cdot CT \cdot f_{min}} \quad (22)$$

$$Rf_{max} = \frac{Rf_{min}}{f_{max}/f_{min} - 1} \quad (23)$$

Soft Start (SS)

For the resonant half-bridge converter, the power delivered is inversely proportional to the switching frequency. To ensure the converter starts or restarts safely, the soft-start function sets the switching frequency at a high value until the value is controlled by the closed loop. The soft-start can be easily achieved using an external RC series circuit.

At the beginning of the start-up sequence, the SS voltage is 0V. The soft-start resistor R_{SS} is in parallel with Rf_{min}. So Rf_{min} and R_{SS} determine the initial frequency:

$$f_{start} = \frac{1}{3 \cdot CT \cdot (Rf_{min} \parallel R_{ss})} \quad (24)$$

During start-up, C_{SS} is charged until its voltage reaches the reference V_{REF}, and the current flowing through R_{SS} drops to zero. This period takes about $5R_{SS}C_{SS}$. During this period, the switching frequency changes following an exponential curve. Initially, the C_{SS} charging process decays relatively quickly, but the rate slows progressively. After this period, the output voltage is still not close to the setting value, so the feedback loop takes over after start-up. With a soft-start function, the input current increases gradually until the output voltage reaches the setting point with little overshoot.

The parameters of the soft-start RC network can be chosen according to Equation (25) and Equation (26):

$$R_{ss} = \frac{Rf_{min}}{\frac{f_{start}}{f_{min}} - 1} \quad (25)$$

$$C_{ss} = \frac{3 \times 10^{-3}}{R_{ss}} \quad (26)$$

Select the initial frequency f_{start} at least four times the minimum value f_{min}. When selecting C_{SS}, there is a trade-off between the desired soft-start operation and the OCP speed.

Adaptive Dead-Time Adjustment (HBVS)

The dead-time period between HSG and LSG drivers is always needed in half-bridge topologies in order to prevent any cross-conduction through the power stage MOSFETs, which may result in excessive current, high EMI noise and destructions in practical applications. Traditional fixed dead-time control scheme is often used in resonant converters as it is simple to implement. However, this method can cause hard switching in light load or large L_m design condition which eventually leads to thermal and reliability issues.

The HR1200 incorporates an intelligent ADTA logic circuit, which is capable of detecting the dv/dt of SW and automatically inserting a proper dead-time with respect to the actual operating conditions of the converter. To achieve this, a 5pF high-voltage capacitor is recommended between SW and HBVS. With ADTA, the MOSFET body diode conduction time can be minimized which enables the LLC converter to achieve high efficiency from light load to full load due to ZVS. Moreover, the design of thermal management and L_m of the transformer can be easier. Figure 28 shows the simplified block diagram of ADTA.

Once HSG switches off, SW begins swinging from a high voltage to a low voltage due to the resonant tank current I_r. A negative dv/dt draws a current from HBVS via C_{HBVS}. HBVS is pulled down depending on dv/dt and C_{HBVS}. If the differential current is higher than the internal comparator current, HBVS will be pulled down to zero and clamped. When SW stops slewing, the differential current elapses accordingly. HBVS starts to ramp up. LSG switches on after a minimum dead-time.

The duration from the time HSG switches off to the time LSG switches on is defined as the dead time. It relies on the completion of SW's transition.

When LSG switches off, SW swings from zero to high, creating a positive differential current via C_{HBVS}. The dead time adjusts automatically to current information.

To avoid damaging HBVS, the differential current should not be higher than 65mA. Otherwise, a smaller value for C_{HBVS} must be selected to meet Inequality (27):

$$i_d = \left| C_{HBVS} \cdot \frac{dV}{dt} \right| < 65mA \quad (27)$$

However, if the value for C_{HBVS} is too small to detect dv/dt, the minimum voltage change rate dv_{min}/dt is taken into account to choose an appropriate C_{HBVS}.

First, calculate the peak magnetizing current I_m according to Equation (28):

$$I_m = \frac{V_{in}}{8 \cdot L_m \cdot f_{max}} \quad (28)$$

Then C_{HBVS} can be designed:

$$C_{HBVS} > \frac{950\,\mu A}{I_m} \cdot \frac{C_{oss}}{2} \quad (29)$$

where C_{oss} is the output capacitance of the power stage MOSFET when V_{ds} equals zero. For a typical design, L_m=870µH, V_{in}=450Vdc, and f_{max}=140kHz. Based on calculation results, C_{HBVS} should be larger than 4.5pF. So 5pF is selected, typically fit for most MOSFETs.

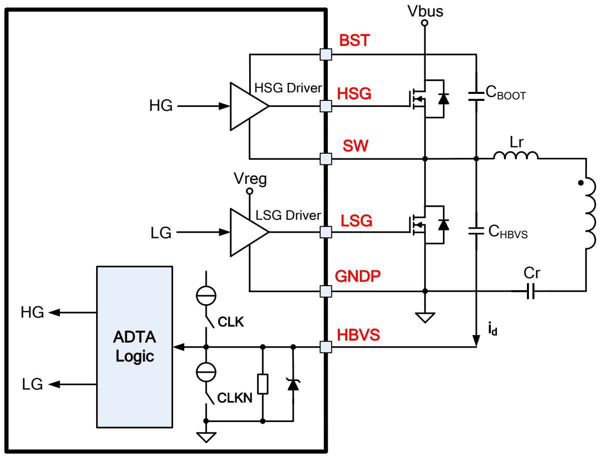


Figure 28: Block Diagram of ADTA

Figure 29 shows the operation waveform of ADTA. Figure 30 illustrates the possible dead time with ADTA logic. There are three kinds of possible dead time: minimum dead time t_{DMIN} (240ns typically), maximum dead time t_{DMAX} (1.1µs typically), and adjusted dead time (between t_{DMIN} and t_{DMAX}). When the transition time of SW is smaller than t_{DMIN}, the logic prevents the gate from providing output until t_{DMIN} is reached. This can avoid any shoot-through of the high-side and low-side MOSFET. If the dead time is too long, it may lead to duty cycle loss and loss of soft switching. So a maximum dead time t_{DMAX} is set forcing the gate to switch on.

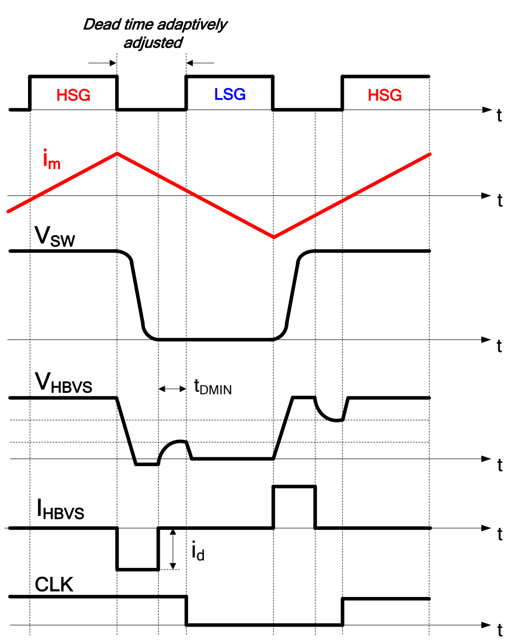


Figure 29: Operation Waveform of ADTA

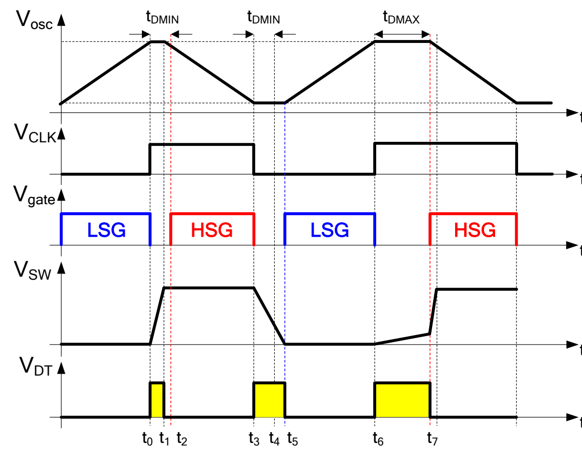


Figure 30: Dead Time in ADTA

If HBVS is shorted to GND, LLC stops switching. If HBVS is floating, the internal circuit cannot detect the differential current in HBVS, and the fixed dead time (300ns) takes effect.

Capacitive Mode Protection (CMP, CSHB)

In fault conditions such as over-load or short-circuit condition, the converter may run into the capacitive region. In capacitive mode, the voltage applied to the resonant tank is lagging off the current. The body diode of one of the MOSFETs switches on. So, to avoid device damage, the switching of the other MOSFET should be blocked. The functional block diagram of CMP is shown in Figure 31.

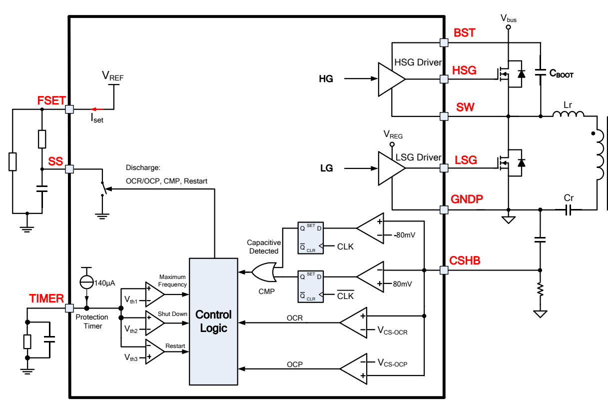


Figure 31: CMP and OCP Block Diagram

Figure 32 shows the operating principle of capacitive mode protection. CSPOS and CSNEG stand for the current polarity, which is generated by comparing the voltage of CS with internal +80mV and -80mV voltage reference.

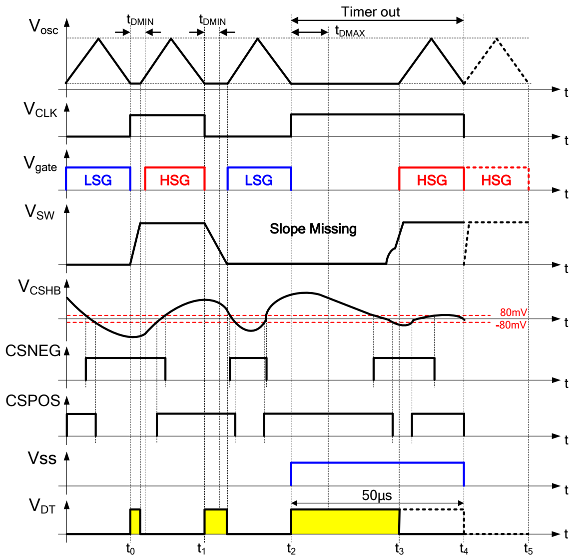


Figure 32: Operating Principle of CMP

At t_0, the low-side gate driver switches off for the first time. CSNEG is high, which means the current is at the right polarity, so the converter is operating in inductive mode. The capacitive mode protection circuit is not active.

At t_1, the high-side gate driver switches off for the first time. CSPOS is high, so the current is at the right polarity, and the converter operates in inductive mode. The capacitive mode protection circuit is still not active.

At t_2, the low-side gate driver turns off for a second time. CSNEG is zero and CSPOS is high, which means the converter is operating in capacitive mode. The body diode of the low-side MOSFET takes over the current after the low-side MOSFET is turned off. SW does not turn high, so HBVS cannot catch the dv/dt until the current returns to the correct polarity. The dead time remains high, and VCO is held. Another MOSFET does not switch on. So, capacitive switching is effectively avoided.

At t_3, the current returns to the correct polarity, then another MOSFET is turned on due to dv/dt being captured.

If the correct current polarity cannot be detected from t_2 to t_4, or the current is very small and is not capable of pulling SW up or down, eventually another MOSFET will be forced to switch on when the timer for CMP (50µs) expires (as shown in Figure 32 in dashed lines).

The V_{SS} control signal controls the soft start. When capacitive mode operation is detected, V_{SS} is high. An internal MOSFET is turned on to pull the voltage of C_{SS} low. Therefore, the switching frequency increases quickly to limit the power delivered to the output. V_{SS} is reset when the first gate driver is turned off (after CMP). The switching frequency decreases smoothly until the control loop takes over.

Over-Current Regulation and Over-Current Protection (CSHB, TIMER)

The HR1200 provides two levels of over-current protection (see Figure 33).

1. Over-Current Regulation

The first level of protection occurs when the voltage on CSHB exceeds $V_{CS\text{-}OCR}$ (0.77V). Following actions will take place:

a. The transistor connected internally between SS and GND is turned on for at least 10µs, which causes the C_{SS} voltage dropping down, resulting in a sharp increase in the oscillator frequency. Hence, the energy transferred to the output is reduced.

b. An internal 140µA current source is turned on to charge C_{TIMER} and raises the voltage of TIMER pin. If the CSHB voltage drops below $V_{CS\text{-}OCR}$ (10mV hysteresis) before the TIMER voltage reaches V_{th1} (1.97V), the discharging of C_{SS} and the charging of C_{TIMER} stop. Then the converter resumes normal operation.

t_{OC} represents the time for the C_{TIMER} voltage to rise from 0V to V_{th1}. It is actually a delay time for over-current regulation. There is no simple relationship between t_{OC} and C_{TIMER}. C_{TIMER} is selected based on experimental results.

If the CSHB voltage remains larger than $V_{CS\text{-}OCR}$ after the TIMER voltage reaches V_{th1}, C_{SS} is discharged completely. Simultaneously, internal 140µA current source continues charging C_{TIMER} until the TIMER voltage reaches V_{th2} (3.45V). At this time, the IC turns off all gate driver outputs.

The period for the TIMER voltage to rise from V_{th1} to V_{th2} can be calculated approximately by using Equation (30):

$$t_{OP} = 10^4 \cdot C_{TIMER} \quad (30)$$

The above status remains until V_{TIMER} drops to V_{th3} (0.29V) as C_{TIMER} is slowly discharged by

R_{TIMER}. The IC then restarts. The time period can be calculated using Equation (31):

$$t_{OFF} = \ln\frac{V_{th2}}{V_{th3}} \cdot R_{TIMER}C_{TIMER} \approx 2.5 \cdot R_{TIMER}C_{TIMER} \quad (31)$$

The OCR limits the energy transferred from the primary to the secondary winding during over-load or short-circuit period. However, excessive power consumption due to high continuous currents can damage the secondary-side windings and rectifiers. By incorporating the TIMER function, the IC provides additional protection to reduce the average power consumption. When OCR is triggered, the converter enters a hiccup-like protection mode that operates intermittently. Figure 33 shows the timing procedure.

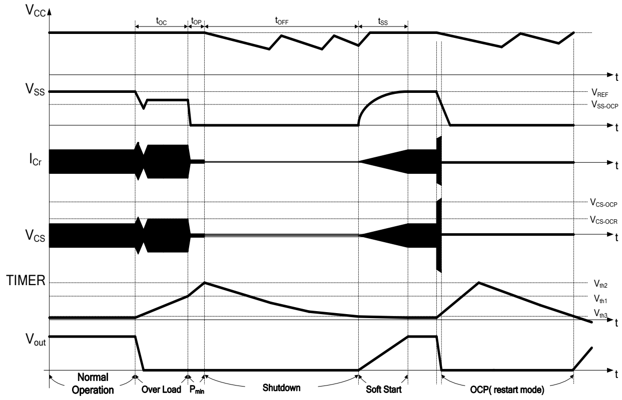


Figure 33: OCR Timing Sequence

2. Over-Current Protection

The second level of protection triggers when $V_{CS} > V_{CS\text{-}OCP}$ (1.48V). Normally, this condition occurs when the CSHB voltage continues rising during short–circuit period. Once V_{CS} rises to $V_{CS\text{-}OCP}$, the IC does not stop switching immediately until $V_{SS} < V_{SS\text{-}OCP}$, and C_{SS} is discharged by an internal transistor continuously. If V_{CS} remains above $V_{CS\text{-}OCP}$ until V_{SS} drops below $V_{SS\text{-}OCP}$, the IC shuts down. C_{TIMER} is charged by an internal 140µA current source until the TIMER voltage reaches V_{th2}. The IC resumes operation if the TIMER voltage falls below V_{th3}.

The OCP provides a high-speed over-current limitation. The IC works in auto-recovery mode when OCP triggers.

Current Sensing

The HR1200 uses two methods for sensing current: lossless current sensing and sense resistor current sensing. Generally, lossless current sensing is used in high-power applications (see Figure 34).

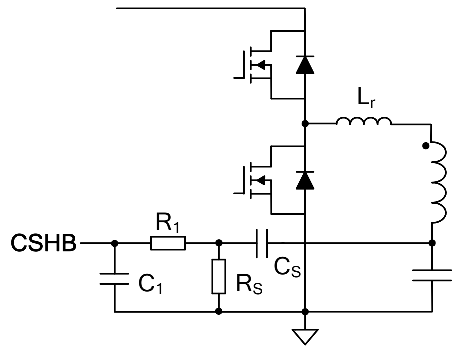


Figure 34: Current Sensing with Lossless Network

To design a lossless current sensing network, Inequality (32) should be satisfied:

$$C_S \leq \frac{C_r}{100} \quad (32)$$

R_S should meet Inequality (33):

$$R_S < \frac{V_{CS\text{-}OCR}}{I_{Crpk}} \cdot \left(1 + \frac{C_r}{C_S}\right) \quad (33)$$

where I_{Crpk} is the peak current of the resonant tank at low input voltage and full load. I_{Crpk} can be expressed in Equation (34):

$$I_{Crpk} = \sqrt{\left(\frac{NV_o}{4L_m f_s}\right)^2 + \left(\frac{I_o \pi}{2N}\right)^2} \quad (34)$$

where N is the turn ratio of the transformer, I_o and V_o are the output current and voltage respectively, f_s is the switching frequency, and L_m is the magnetizing inductance.

For capacitive mode detection in no load or tiny load condition, R_S should meet Inequality (35) as well:

$$R_S > \frac{80\text{ mV}}{I_m} \cdot \left(1 + \frac{C_r}{C_S}\right) \quad (35)$$

In some conditions especially when large L_m is used, it's difficult to meet Inequality (33) and Inequality (35) simultaneously. The system will operate without CMP function at light load if Inequality (35) is not satisfied.

The R_1 and C_1 network is used to attenuate the switching noise on CSHB. The time constant should be no larger than 100ns.

An alternative solution is to use a sense resistor in series with the resonant tank (see Figure 35). This method is quite simple, but may cause undesired power consumption on the sense resistor.

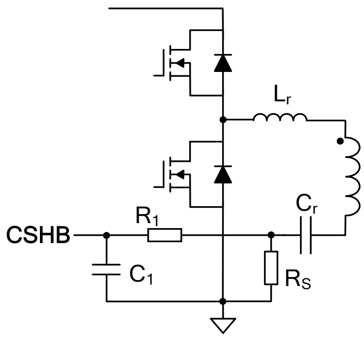


Figure 35: Current Sensing with A Sense Resistor

The sense resistor can be designed using Inequality (36):

$$R_S < \frac{V_{CS\text{-}OCR}}{I_{Crpk}} \quad (36)$$

LLC Brown-In/Brown-Out (D2D_BI/BO)

The LLC controller stops when the D2D_BI/BO signal is low and recovers once the D2D_BI/BO signal goes high.

Burst-Mode Operation (BURST)

Under light-load or no-load condition, the resonant half-bridge switching frequency is limited by the system maximum frequency. To control the output voltage and limit the power consumption, the HR1200 enables the converter to operate in burst mode to reduce the average switching frequency, thus reducing the average residual magnetizing current and related power losses.

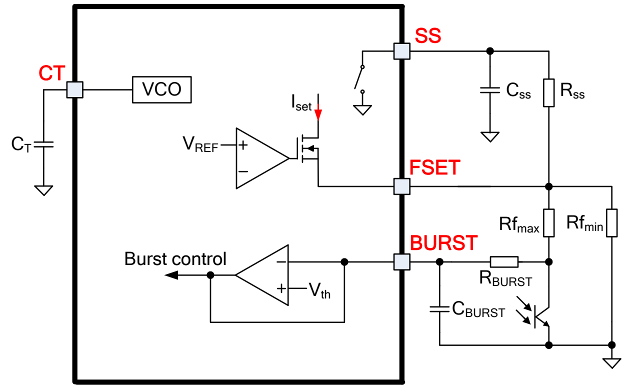


Figure 36: Burst-Mode Operation Set-Up

Figure 36 shows a typical circuit connecting BURST to the feedback signal. R_{BURST} and C_{BURST} must be optimized to adjust the number of switching cycles during burst-on period, which can reduce no-load power consumption. Rf_{max} can determine the maximum switching frequency which is needed for the IC to operate in burst mode. It also determines the level of output load needed to run into burst mode.

Figure 37 illustrates the burst-mode operation waveforms. When the output load decreases, the BURST voltage also decreases. If the BURST voltage drops below V_{th} (1.23V), the HR1200 stops switching both the HSG and LSG and connects CT to GNDS internally. Meanwhile, the SYN signal is set high. It is used to synchronize the burst of PFC and LLC. Once the voltage on BURST exceeds V_{th} by a hysteresis of 40mV, the HR1200 resumes normal operation and the SYN signal is set low. During burst-mode operation, VREG normally holds above V_{regUVP}, and the soft-start function is not activated.

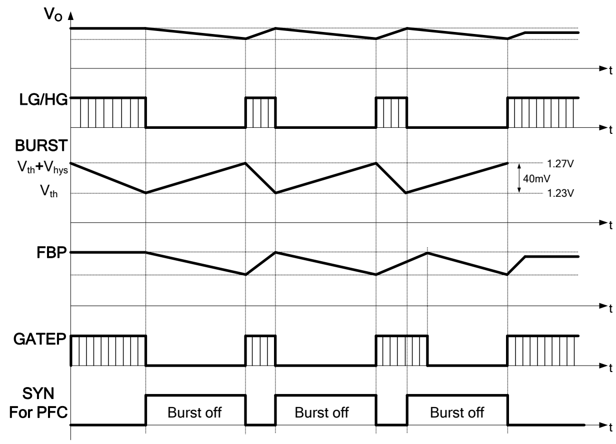


Figure 37: Burst-Mode Operation

Latch Protection (SO)

If the SO voltage exceeds the threshold $V_{SO\text{-}Latch}$ (3.42V), the IC latches off. This status can only be released when VCC drops below V_{CCRST}. This function can be used for OVP or OTP.

Start-Up Failure Protection (SFP, SO)

The HR1200 provides a one-shot start-up failure protection by sampling the SO voltage. Figure 38 shows the detailed SFP timing.

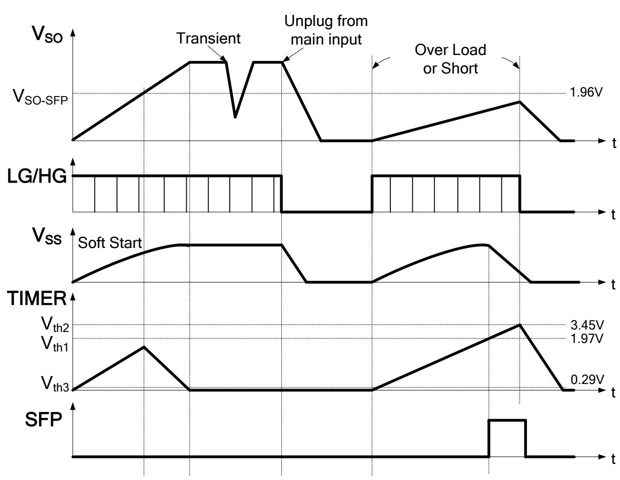


Figure 38: SFP Timing

During start-up, the TIMER capacitor begins to be charged up by an internal 25μA current source. If the SO voltage is less than $V_{SO\text{-}SFP}$ (1.96V) when the TIMER voltage rises up to V_{th1}, then the IC treats it as a fault condition. The HR1200 begins discharging the SS capacitor, and TIMER continues ramping up irreversibly. As soon as the TIMER voltage reaches V_{th2}, the HR1200 stops charging TIMER, both PFC and LLC stop switching. As a resistor is in parallel with the TIMER capacitor, the TIMER voltage is pulled down gradually. Until the TIMER voltage falls below V_{th3}, the IC attempts another restart sequence.

Connect SO to the resistor divider from V3.3 if the SO functions are not needed.

High-Side Gate Driver (HSG)

The external BST capacitor provides energy to the high-side gate driver. An integrated bootstrap diode charges this capacitor through VCC. This diode simplifies the external driving circuit for the high-side switch, allowing the BST capacitor to be charged when the low-side MOSFET is on.

Considering the BST capacitor charging time, in order to provide enough gate driver energy, a BST capacitor of 100nF to 1μF is recommender (see Figure 39).

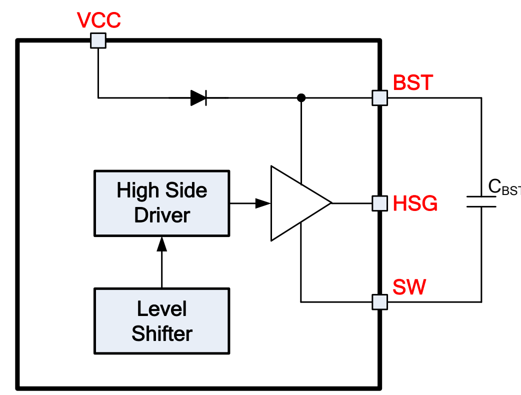


Figure 39: High-Side Gate Driver

Low-Side Gate Driver (LSG)

LSG provides the gate driver signal for the low-side MOSFET. The maximum absolute rating table shows the maximum LSG voltage is 14V. Under certain conditions (e.g. surge rating is too high), a large voltage spike may occur on LSG due to oscillations from the long gate-driver wire, the MOSFET parasitic capacitance, and the small gate-driver resistor. The voltage spike may cause damage to LSG. Although there is suppression internally in the chip, it is better to add a 13V Zener diode close to LSG and GND to prevent damage to the chip pins (see Figure 40).

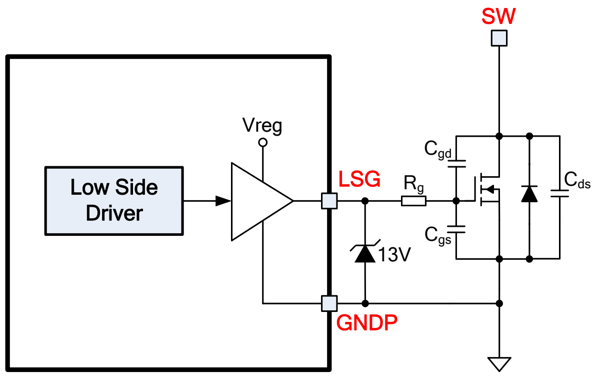


Figure 40: Low-Side Gate Driver

PROTECTION SUMMARY

Pin	Symbol	Description	Affected	Action
VCC	V_{CC_UVP}	Under-voltage protection for VCC	System	Disable
VCC	V_{CC_SCP}	Short-circuit protection for VCC	System	Disable and limit I_{HV}
VREG	V_{reg_UVP}	Under-voltage protection for VREG	System	Disable and limit I_{ch} (V_{reg})
SO	V_{SO_Latch}	Latch protection	System	Shutdown and latch
SO	V_{SO_SFP}	Start-up failure protection	System	Restart with timer out
	OTP	Over-temperature protection	System	Disable
ACIN	Brown-out	Line input under-voltage protection	System	Suspend switching
CSP	OCP_PFC	Current limit of PFC	PFC	Program with restart or latch off
FBP	OVP_PFC	Over voltage of PFC	PFC	Suspend switching
FBP	OLP_PFC	Open-loop protection	System	Restart with recovery
FBP	UVP_PFC	Under-voltage protection for PFC out	HBC	Suspend switching
	LLC brown-in/-out	LLC stage under-voltage protection	HBC	Suspend switching
CSHB	OCR_HBC	Over-current regulation of HBC	HBC	Restart with timer out
CSHB	OCP_HBC	Over-current protection HBC	HBC	Shutdown, restart with timer out
CSHB	CMR	Capacitive mode regulation	HBC	Increasing switching frequency
CSHB	ADT	Adaptive dead time	HBC	Prevent hard switching

TYPICAL APPLICATION CIRCUIT

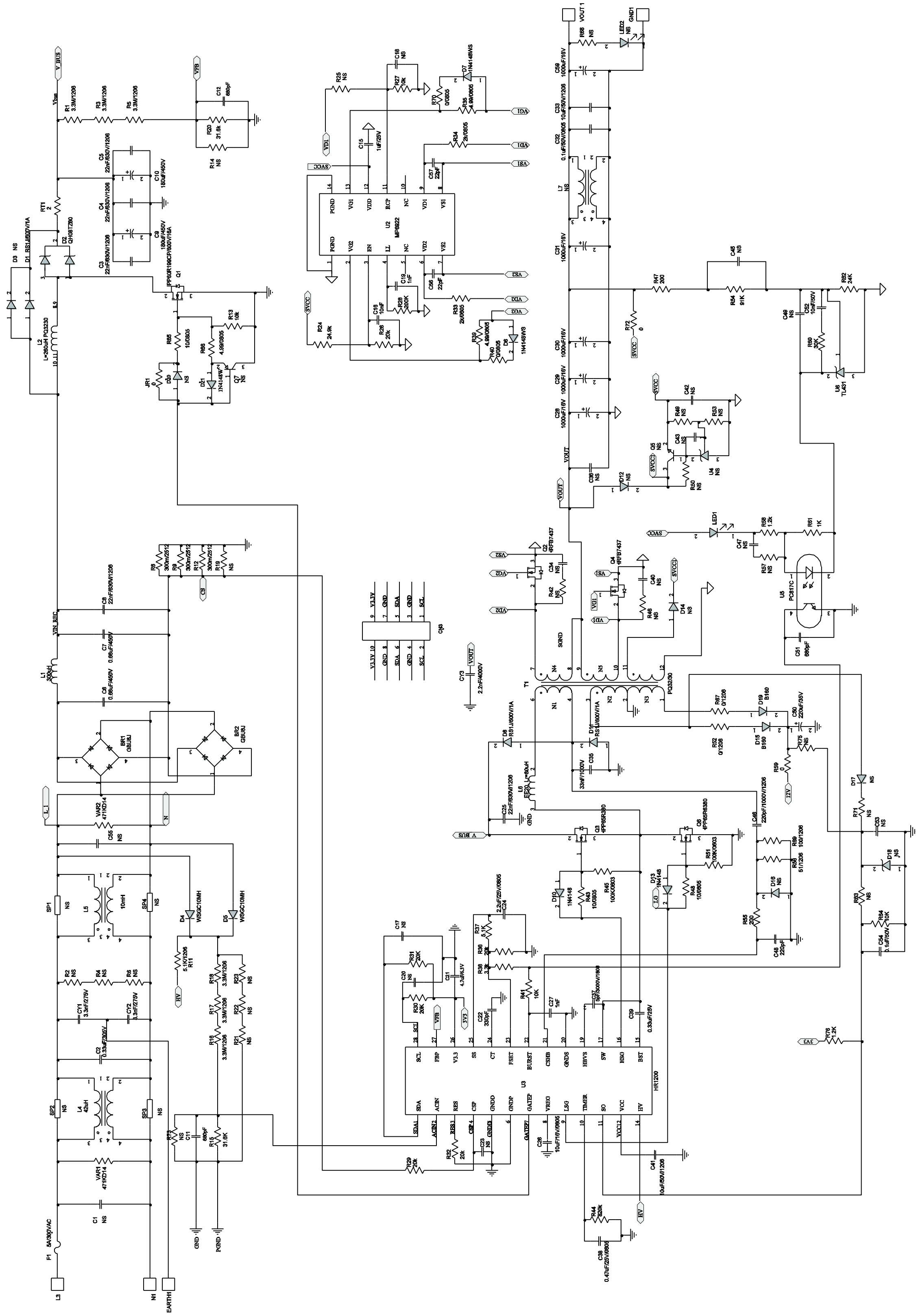
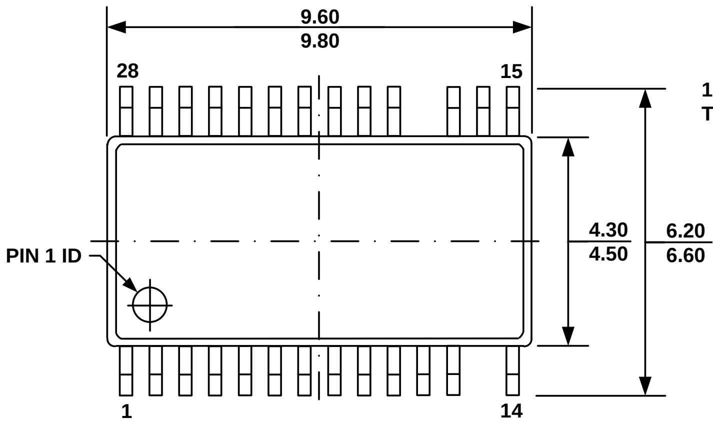


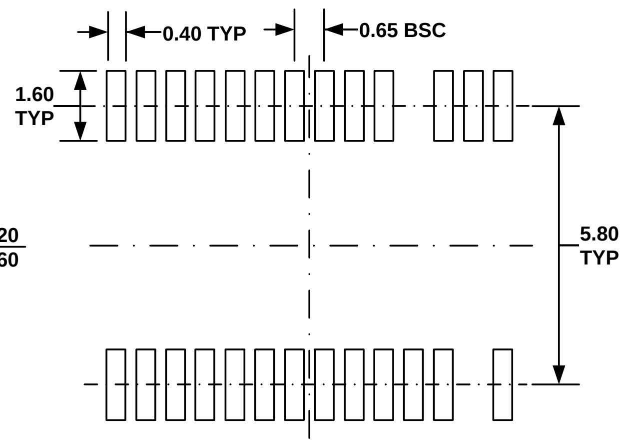
Figure 41: Application Circuit

PACKAGE INFORMATION

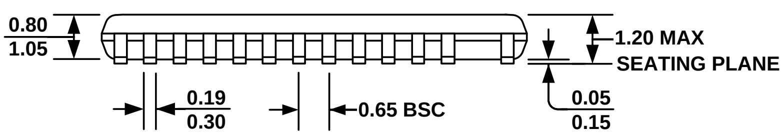
TSSOP-28



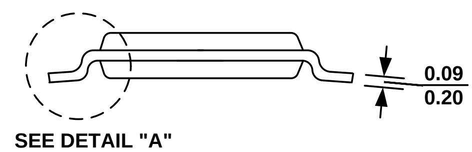
TOP VIEW



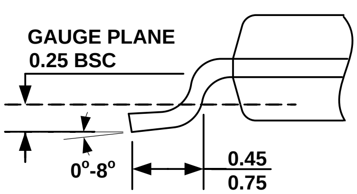
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



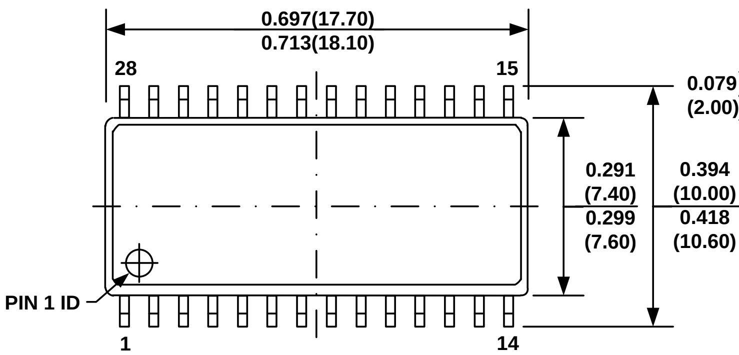
DETAIL "A"

NOTE:

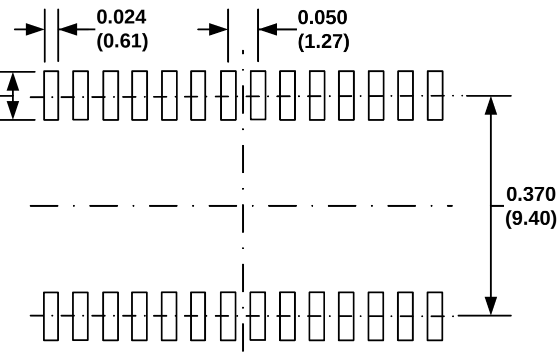
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

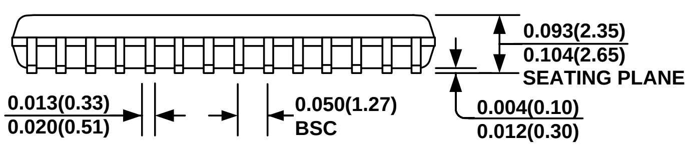
SOIC-28



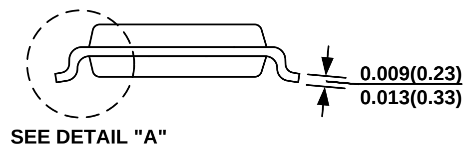
TOP VIEW



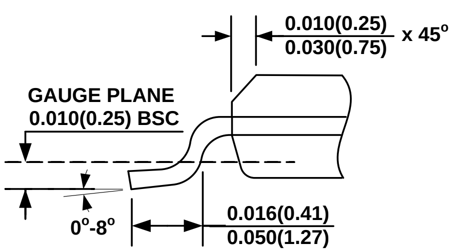
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

APPENDIX A: I²C COMMANDS AND REGISTERS

VOUT_CMD_H (02/01h, 10bits)

Set the normal value of the output voltage target at high line. The default setting for the -0001 version is 1100011110.

Command	VOUT_CMD_H															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VOUT_CMD_L (04/03h, 10bits)

Set the normal value of the output voltage target at low line. The default setting for the -0001 version is 1100011110.

Command	VOUT_CMD_L															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_HL_LINE (05h, 8bits)

Set the threshold of high line and low line. The default setting for the -0001 version is 01110001.

Command	VIN_HL_LINE							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUT_VCOMP1 (07/06h, 14bits)

Set the Load Level1 of the auto-output voltage. The default setting for the -0001 version is 011111111100.

Command	AUTO_VOUT_VCOMP1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUT_VCOMP2 (09/08h, 14bits)

Set the Load Level2 of the auto-output voltage. The default setting for the -0001 version is 001100110010.

Command	AUTO_VOUT_VCOMP2															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUT_VCOMP3 (0B/0Ah, 14bits)

Set the Load Level3 of the auto-output voltage. The default setting for the -0001 version is 000110011001.

Command	AUTO_VOUT_VCOMP3															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUT_CMPHYS (0D/0Ch, 14bits)

Set the load hysteresis of the auto-output voltage. The default setting for the -0001 version is 000011110101.

Command	AUTO_VOUT_CMPHYS															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTH_CMD1_L (0Eh, 8bits)

Set the low byte of the output voltage level one at high line. The default setting for the -0001 version is 00011110.

Command	AUTO_VOUTH_CMD1_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTH_CMD2_L (0Fh, 8bits)

Set the low byte of the output voltage level two at high line. The default setting for the -0001 version is 00011110.

Command	AUTO_VOUTH_CMD2_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTH_CMD3_L (10h, 8bits)

Set the low byte of the output voltage level three at high line. The default setting for the -0001 version is 00011110.

Command	AUTO_VOUTH_CMD3_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTH_CMD_H (11h, 6bits)

Set the high byte of the output voltage at high line. The default setting for the -0001 version is 111111.

Bit	Item	Description
5:4	AUTO_VOUTH_CMD3_H	High bits of output voltage level three at high line.
3:2	AUTO_VOUTH_CMD2_H	High bits of output voltage level two at high line.
1:0	AUTO_VOUTH_CMD1_H	High bits of output voltage level one at high line.

Command	AUTO_VOUTH_CMD_H							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTL_CMD1_L (12h, 8bits)

Set the low byte of the output voltage level one at low line. The default setting for the -0001 version is 00011110.

Command	AUTO_VOUTL_CMD1_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTL_CMD2_L (13h, 8bits)

Set the low byte of the output voltage level two at low line. The default setting for the -0001 version is 00011110.

Command	AUTO_VOUTL_CMD2_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTL_CMD3_L (14h, 8bits)

Set the low byte of the output voltage level three at low line. The default setting for the -0001 version is 00011110.

Command	AUTO_VOUTL_CMD3_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AUTO_VOUTL_CMD_H (15h, 6bits)

Set the high byte of the output voltage at low line. The default setting for the -0001 version is 111111.

Bit	Item	Description
5:4	AUTO_VOUTL_CMD3_H	High bits of output voltage level three at low line.
3:2	AUTO_VOUTL_CMD2_H	High bits of output voltage level two at low line.
1:0	AUTO_VOUTL_CMD1_H	High bits of output voltage level one at low line.

Command	AUTO_VOUTL_CMD_H							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w

LLC_ENABLE_HIGH (17/16h, 10bits)

Set the enable threshold voltage of the LLC. The default setting for the -0001 version is 1100101010.

Command	LLC_ENABLE_HIGH															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

LLC_ENABLE_LOW (19/18h, 10bits)

Set the disable threshold voltage of the LLC. The default setting for the -0001 version is 1001010001.

Command	LLC_ENABLE_LOW															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

ZCD_PERIOD_H (1Ah, 7bits)

Set the oscillation period of the turn-off current at high line. The default setting for the -0001 version is 0010100.

Command	ZCD_PERIOD_H							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

ZCD_PERIOD_L (1Bh, 7bits)

Set the oscillation period of the turn-off current at low line. The default setting for the -0001 version is 0101000.

Command	ZCD_PERIOD_L							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

SLEWRATE_HIGH (1Ch, 8bits)

Set the soft-start slew rate at high line. The default setting for -0001 version is 00000110.

Command	SLEWRATE_HIGH							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

SLEWRATE_LOW (1Dh, 8bits)

Set the soft-start slew rate at low line. The default setting for the -0001 version is 00001101.

Command	SLEWRATE_LOW							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS1_L (1Eh, 8bits)

Set the low byte of the switching period at level one of the input voltage. The default setting for the -0001 version is 11001000.

Command	TS1_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS2_L (1Fh, 8bits)

Set the low byte of the switching period at level two of the input voltage. The default setting for the -0001 version is 11001000.

Command	TS2_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS3_L (20h, 8bits)

Set the low byte of the switching period at level three of the input voltage. The default setting for the -0001 version is 11001000.

Command	TS3_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS4_L (21h, 8bits)

Set the low byte of the switching period at level four of the input voltage. The default setting for the -0001 version is 10100111.

Command	TS4_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS_H (22h, 4bits)

Set the high byte of the switching period. The default setting for the -0001 version is 0000.

Bit	Item	Description
3	TS4_H	High bit of switching period at level four of the input voltage.
2	TS3_H	High bit of switching period at level three of the input voltage.
1	TS2_H	High bit of switching period at level two of the input voltage.
0	TS1_H	High bit of switching period at level one of the input voltage.

Command	TS_H							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w

TS_MIN1_L (23h, 8bits)

Set the low byte of the maximum switching period at level one of the input voltage. The default setting for the -0001 version is 00100000.

Command	TS_MIN1_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS_MIN2_L (24h, 8bits)

Set the low byte of the maximum switching period at level two of the input voltage. The default setting for the -0001 version is 00100000.

Command	TS_MIN2_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS_MIN3_L (25h, 8bits)

Set the low byte of the maximum switching period at level three of the input voltage. The default setting for the -0001 version is 00100000.

Command	TS_MIN3_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS_MIN4_L (26h, 8bits)

Set the low byte of the maximum switching period at level four of the input voltage. The default setting for the -0001 version is 11110100.

Command	TS_MIN4_L							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TS_MIN_H (27h, 8bits)

Set the high byte of the maximum switching period. The default setting for the -0001 version is 01111111.

Bit	Item	Description
7:6	TS_MIM4_H	High bit of the maximum switching period at level four.
5:4	TS_MIN3_H	High bit of the maximum switching period at level three.
3:2	TS_MIN2_H	High bit of the maximum switching period at level two.
1:0	TS_MIN1_H	High bit of the maximum switching period at level one.

Command	TS_MIN_H							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

JITTER_AMPLITUDE (28h, 8bits)

Set the peak-to-peak amplitude of the switching frequency jitter. The default setting for the -0001 version is 00000010.

Command	JITTER_AMPLITUDE							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

JITTER_FS (30/29h, 13bits)

Set the step value and the period of step of the switching frequency jitter. The default setting for -0001 version is 0100000011110.

Bit	Item	Description
12:11	JITTER_STEP	Step value.
10:0	STEP_PERIOD	Step period.

Command	JITTER_FS															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TON_MIN (2Bh, 5bits)

Set the minimum turn-on time. The default setting for the -0001 version is 01100.

Command	TON_MIN							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w

MIN_OFF_TIME (2Ch, 5bits)

Set the minimum turn-off time. The default setting for the -0001 version is 01100.

Command	MIN_OFF_TIME							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w

BURST_POINT_H (2E/2Dh, 13bits)

Set the PFC burst load at high line. The default setting for the -0001 version is 0000111101011.

Command	BURST_POINT_H															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

BURST_POINT_L (30/2Fh, 13bits)

Set the PFC burst load at low line. The default setting for the -0001 version is 0000111101011.

Command	BURST_POINT_L															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

NORMAL_KI (31h, 8bits)

Set the Ki value at normal operation mode. The default setting for the -0001 version is 00010010.

Command	NORMAL_KI							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

NORMAL_KP (32h, 8bits)

Set the Kp value at normal operation mode. The default setting for the -0001 version is 01111000.

Command	NORMAL_KP							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

FAST_KI (34/33h, 10bits)

Set the Ki value at fast-loop operation mode. The default setting for the -0001 version is 0001001000.

Command	FAST_KI															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

FAST_KP (36/35h, 10bits)

Set the Kp value at fast-loop operation mode. The default setting for the -0001 version is 0100100000.

Command	FAST_KP															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

FASTLOOP_VOLTAGE (37h, 7bits)

Set the fast-loop level below the output voltage target. The default setting for the -0001 version is 0011111.

Command	FASTLOOP_VOLTAGE							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_BI_LEVEL (39/38h, 10bits)

Set the brown-in voltage of the input voltage. The default setting for the -0001 version is 0011101101.

Command	VIN_BI_LEVEL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_BO_LEVEL (3B/3Ah, 10bits)

Set the brown-out voltage of the input voltage. The default setting for the -0001 version is 0011011001.

Command	VIN_BO_LEVEL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_BIBO_TIME (3Ch, 8bits)

Set the brown-in and brown-out time of the input voltage. The default setting for the -0001 version is 00000101.

Bit	Item	Description
7:4	VIN_BI_TIME	Brown-in time.
3:0	VIN_BO_TIME	Brown-out time.

Command	VIN_BIBO_TIME							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_LEVEL1 (3E/3Dh, 9bits)

Level one of the input current reference. The default setting for the -0001 version is 010001001.

Command	IREF_LEVEL1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_LEVEL2 (40/3Fh, 9bits)

Level two of the input current reference. The default setting for the -0001 version is 001000101.

Command	IREF_LEVEL2															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_HYS (41h, 8bits)

Set the hysteresis of the level of the input current reference. The default setting for the -0001 version is 00010111.

Command	IREF_HYS							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_BO_TRIM1 (42h, 6bits)

Set the trim value of the brown-out level of the input voltage at level one. The default setting for the -0001 version is 000000.

Command	VIN_BO_TRIM1							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w

VIN_BO_TRIM2 (43h, 6bits)

Set the trim value of the brown-out level of the input voltage at level two. The default setting for the -0001 version is 000000.

Command	VIN_BO_TRIM2							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w

OCP_LIMIT (44h, 7bits)

Set the over-current limit of the inductor current. The default setting for the -0001 version is 0000100.

Command	OCP_LIMIT							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

OCP_MODE (45h, 4bits)

Set the over-current protection mode. The default setting for the -0001 version is 0000.

Bit	Item	Description
3	OCP_MODE_EN	1: enable 0: disable
2:0	OCP_MODE	000: latch 111: hiccup other: retry number

Command	OCP_MODE							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w

OCP_RETRY_DELAY (47/46h, 10bits)

Set the delay time of the system recovery after the OCP event is cleared. The default setting for the -0001 version is 0111110100.

Command	OCP_RETRY_DELAY															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

OVP_LIMIT_H (48h, 7bits)

Set the over-voltage limit of the output voltage at high line. The default setting for the -0001 version is 1101101.

Command	OVP_LIMIT_H							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

OVP_LIMIT_L (49h, 7bits)

Set the over-voltage limit of the output voltage at low line. The default setting for the -0001 version is 1101101.

Command	OVP_LIMIT_L							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

CODE ID (4Ah, 8bits)

Store customer code ID. The default setting for the -0001 version is 00000001.

Bit	Item	Description
7:2	CUSTOMER_ID	Customer number
1:0	PROGRAMMED CODE_ID	Programmed code number

Command	CODE ID							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_COMP_VALUE1 (4Bh, 7bits)

Set the first compensation amplitude of the input current reference. The default setting for the -0001 version is 0000001.

Command	IREF_COMP_VALUE1							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_COMP_VALUE2 (4Ch, 7bits)

Set the second compensation amplitude of the input current reference. The default setting for the -0001 version is 0000011.

Command	IREF_COMP_VALUE2							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_COMP_VALUE3 (4Dh, 7bits)

Set the third compensation amplitude of the input current reference. The default setting for the -0001 version is 0001101.

Command	IREF_COMP_VALUE3							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_COMP_VALUE4 (4Eh, 7bits)

Set the fourth compensation amplitude of the input current reference. The default setting for the -0001 version is 0001100.

Command	IREF_COMP_VALUE4							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_LEVEL_SEL1 (4Fh, 8bits)

Set the first voltage level of the input voltage. The default setting for the -0001 version is 10011001.

Command	VIN_LEVEL_SEL1							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_LEVEL_SEL2 (50h, 8bits)

Set the second voltage level of the input voltage. The default setting for the -0001 version is 01001000.

Command	VIN_LEVEL_SEL2							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VCOMP_MAX_L (52/51h, 16bits)

Set the maximum load. The default setting for the -0001 version is 0110110011010010.

Command	VCOMP_MAX_L															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VCOMP_MAX_H (53h, 8bits)

Set the maximum load. The default setting for the -0001 version is 01011001.

Command	VCOMP_MAX_H							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IREF_MAX (55/54h, 9bits)

Set the maximum value of the input current reference. The default setting for the -0001 version is 111100100.

Command	IREF_MAX															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

SYS_CONFIG (56h, 8bits)

Configure the system. The default setting for the -0001 version is 00110100.

Bit	Item	Description
7	BURST_LLC_SYNC_EN	Synchronize PFC with LLC in burst mode. 1: enable 0: disable
6	------	Reserved
5	POWER_ON	Power on the system. 1: enable 0: disable
4	LLC_EN	Enable LLC part. 1: enable 0: disable
3	AUTO_VOUT_EN	Output voltage target is determined by the load. 1: enable 0: disable
2	IREF_COMP_EN	Compensate the current of the input capacitance. 1: enable 0: disable
1	JITTER_EN	Switching frequency jitter. 1: enable 0: disable
0	ZCD_EN	Valley turn on. 1: enable 0: disable

Command	SYS_CONFIG							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

AD_SLEEP_FS (58/57h, 10bits)

Set the ADC sample rate when PWM is off. The default setting for the -0001 version is 1100100000.

Command	AD_SLEEP_FS															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

TON_AHEAD (59h, 4bits)

Set the peak-current sample point. The default setting for the -0001 version is 0010.

Command	TON_AHEAD							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w

OLP_HIGH (5Ah, 7bits)

Set the open-loop protection at high level. The default setting for the -0001 version is 1011100.

Command	OLP_HIGH							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

OLP_LOW (5Bh, 7bits)

Set the open-loop protection at low level. The default setting for the -0001 version is 0111101.

Command	OLP_LOW							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

SOFT_TON (5Ch, 7bits)

Set the soft turn-on time when the system recovers from OVP. The default setting for the -0001 version is 0101000.

Command	SOFT_TON							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

SOFT_SWITCH_CNT (5Dh, 4bits)

Set the number of switching events during soft turn on. The default setting for the -0001 version is 0111.

Command	SOFT_SWITCH_CNT							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r/w	r/w	r/w	r/w

MFR_MERGE_REG (5Eh, 8bits)

The default setting for the -0001 version is 00100001.

Bit	Item	Description
7:3	SWITCH_BLANK_TIME1	PWM off blanking time
2:1	CURRENT_MIRROR_GAIN	Set the current mirror gain. The reference current is 62.5µA. 00: GAIN =1 01: GAIN = 1.4 10: GAIN = 1.6 11: GAIN = 2
0	I2C_FILTER_EN	I^2C filter. 1: enable 0: disable

Command	MFR_MERGE_REG							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

SWITCH_BLANK_TIME (5Fh, 8bits)

Set the PWM on blanking time. The default setting for the -0001 version is 00110101.

Bit	Item	Description
7:4	SWITCH_BLANK_TIME2	PWM off blanking time for OCP.
3:0	SWITCH_BLANK_TIME3	PWM off blanking time for OCL.

Command	SWITCH_BLANK_TIME							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

OVP_DELAYTIME (60h, 6bits)

Set the blanking time of OVP. The default setting for the -0001 version is 110010.

Command	OVP_DELAYTIME							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w

BURST_MODE_HYS (61h, 6bits)

Set the hysteresis of the output voltage in burst mode. The default setting for the -0001 version is 001010.

Command	BURST_MODE_HYS							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w

ERROR_ZERO_REGION (62h, 5bits)

Set the non-regulation region of the output voltage. The default setting for the -0001 version is 00000.

Command	ERROR_ZERO_REGION							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w

VIN_ZERO_POINT (63h, 7bits)

Set the period detection point of the input voltage. The default setting for the -0001 version is 1010010.

Command	VIN_ZERO_POINT							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_PEAK_VALUE (64h, 7bits)

Set the value to detect the top of the input voltage. The default setting for the -0001 version is 0010100.

Command	VIN_PEAK_VALUE							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_VALLEY_VALUE (65h, 7bits)

Set the value to detect the valley of the input voltage. The default setting for the -0001 version is 0111101.

Command	VIN_VALLEY_VALUE							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

IPK_BIAS_TRIM (66h, 8bits)

Trim the bias voltage at CSP. The default setting for the -0001 version is 00000000.

Bit	Item	Description
7	CSP_FAULT_MODE	Determine the control mode when CSP is open or shorted. 1: hiccup 0: latch
6	IPK_BIAS_SAMPLE_EN	Enable sampling of the CSP bias voltage when power is on. 1: enable 0: disable
5:0	IPK_BISA_TRIM	Trim the bias voltage at CSP.

Command	IPK_BIAS_TRIM							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

ADC_OFFSET_TRIM (67h, 5bits)

Trim the ADC offset. The default setting for the -0001 version is 00000.

Command	ADC_OFFSET_TRIM							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r/w	r/w	r/w	r/w	r/w

DELTA_VOLTAGE (68h, 7bits)

Set the minimum delta voltage between the input voltage and output voltage for CSP bias voltage sampling. The default setting for the -0001 version is 0101001.

Command	DELTA_VOLTAGE							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_LEVEL1 (69h, 7bits)

Input voltage level one for the CSP bias voltage sample. The default setting for the -0001 version is 0010100.

Command	VIN_LEVEL1							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_LEVEL2 (6Ah, 7bits)

Input voltage level two for the CSP bias voltage sample. The default setting for the -0001 version is 0101001.

Command	VIN_LEVEL2							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_LEVEL3 (6Bh, 7bits)

Input voltage level three for the CSP bias voltage sample. The default setting for the -0001 version is 0111101.

Command	VIN_LEVEL3							
Bit	7	6	5	4	3	2	1	0
Access	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_LEVEL4 (6D/6Ch, 10bits)

Input voltage level four for the CSP bias voltage sample. The default setting for the -0001 version is 0100110011.

Command	VIN_LEVEL4															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

VIN_HL_HYS (6Eh, 8bits)

Set the hysteresis of the input voltage for adaptive control. The default setting for the -0001 version is 00000101.

Command	VIN_HL_HYS							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

ZCD_VIN_HYS (6Fh, 6bits)

Set the hysteresis of the input voltage for valley turn on. The default setting for the -0001 version is 010100.

Command	ZCD_VIN_HYS							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r/w	r/w	r/w	r/w	r/w	r/w