MP1494

High-Efficiency, 2A, 16V, 500kHz Synchronous, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP1494 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current with excellent load and line regulation over a wide input supply range. The MP1494 has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection and thermal shut down.

The MP1494 requires a minimal number of readily-available standard external components, and is available in a space-saving 8-pin TSOT23 package.

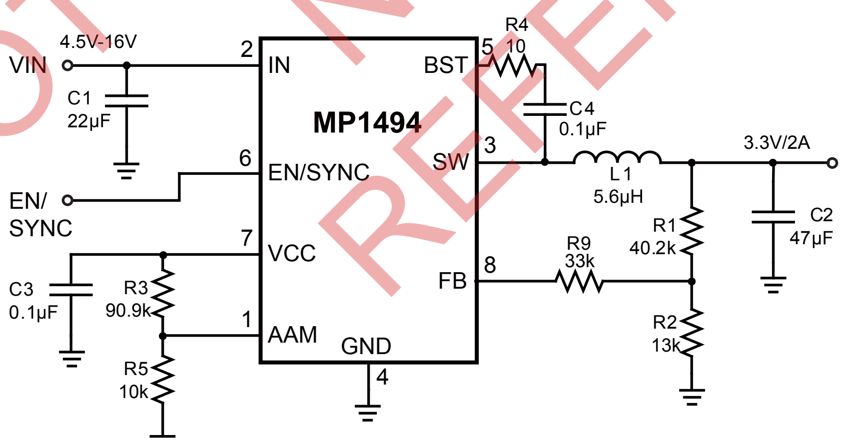
FEATURES

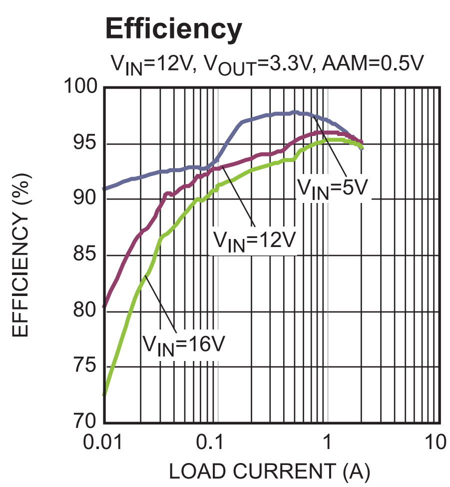
- Wide 4.5V-to-16V Operating Input Range
- 100mΩ/40mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Fixed 500kHz Switching Frequency
- Synchronizes from a 200kHz-to-2MHz External Clock
- AAM Power-Save Mode
- Internal Soft-Start
- OCP Protection and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in an 8-pin TSOT-23 Package

APPLICATIONS

- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



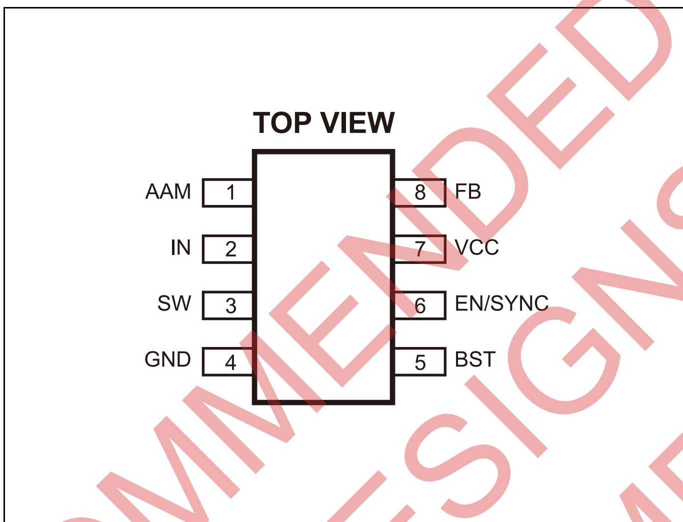


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP1494DJ	TSOT-23-8	ABZ

For Tape & Reel, add suffix –Z (e.g. MP1494DJ–Z);
For RoHS, compliant packaging, add suffix –LF (e.g. MP1494DJ–LF–Z).

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS [1]

V_{IN} ....-0.3V to 17V
V_{SW} ....
-0.3V (-5V for <10ns) to 17V (19V for <10ns)
V_{BS} .... V_{SW}+6V
All Other Pins.............................. -0.3V to 6V [2]
Continuous Power Dissipation (T_A = +25°C) [3]
.... 1.25W
Junction Temperature ....150°C
Lead Temperature ....260°C
Storage Temperature................. -65°C to 150°C

Recommended Operating Conditions [4]

Supply Voltage V_{IN} ....4.5V to 16V
Output Voltage V_{OUT}......................0.8V to V_{IN}-3V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance [5]	θ_{JA}	θ_{JC}	
TSOT-23-8............................	100	55...	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to Page 9, Enable/SYNC control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

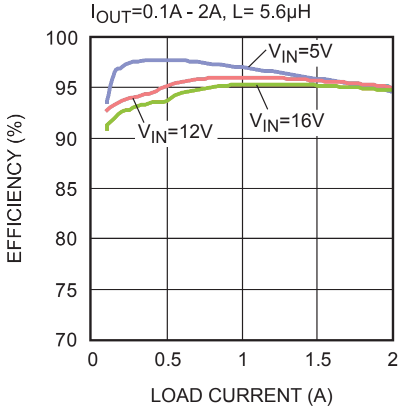
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			1	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, V_{FB} = 1V, AAM=0.5V		0.5	1	mA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		100		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V		40		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit (6)	I_{LIMIT}	Under 40% Duty Cycle	3			A
Oscillator Frequency	f_{SW}	V_{FB}=0.75V	440	500	580	kHz
Fold-Back Frequency	f_{FB}	V_{FB}<400mV		0.25		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=700mV	90	95		%
Minimum On Time(6)	t_{ON_MIN}			60		ns
Sync Frequency Range	f_{SYNC}		0.2		2	MHz
Feedback Voltage	V_{FB}	T_A =25°C	791	807	823	mV
		-40°C<T_A<85°C (7)	787	807	827	
Feedback Current	I_{FB}	V_{FB}=820mV		10	50	nA
EN Rising Threshold	V_{EN_RISING}		1.2	1.4	1.6	V
EN Falling Threshold	$V_{EN\_FALLING}$		1.1	1.25	1.4	V
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
		V_{EN}=0		0		μA
EN Turn-Off Delay	EN_{td-off}			8		μs
VIN Under-Voltage Lockout Threshold-Rising	$INUV_{Vth}$		3.7	3.9	4.1	V
VIN Under-Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$			650		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		3		%
Soft-Start Period	t_{SS}			1.5		ms
Thermal Shutdown (6)				150		°C
Thermal Hysteresis (6)				20		°C

Notes:
6) Guaranteed by design.
7) Not tested in production and guaranteed by over-temperature correlation.

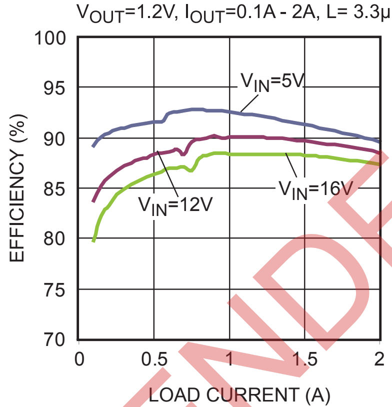
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, AAM=0.5V, T_A = 25°C, unless otherwise noted.

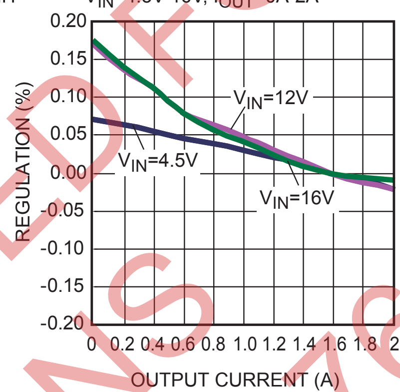
Efficiency
I_{OUT}=0.1A - 2A, L= 5.6µH



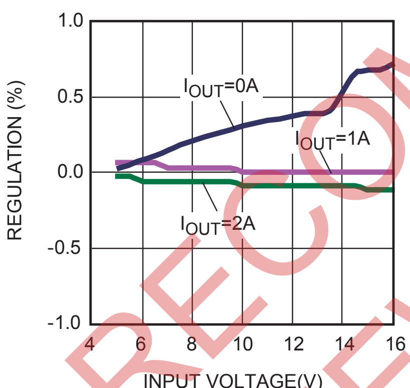
Efficiency
V_{OUT}=1.2V, I_{OUT}=0.1A - 2A, L= 3.3µH



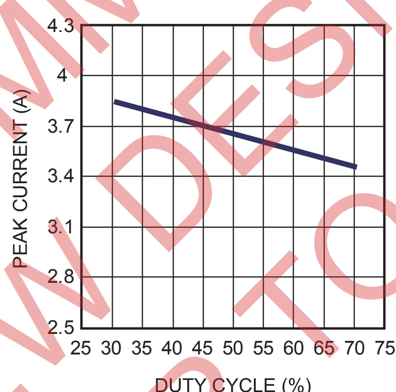
Load Regulation
V_{IN}=4.5V-16V, I_{OUT}=0A-2A



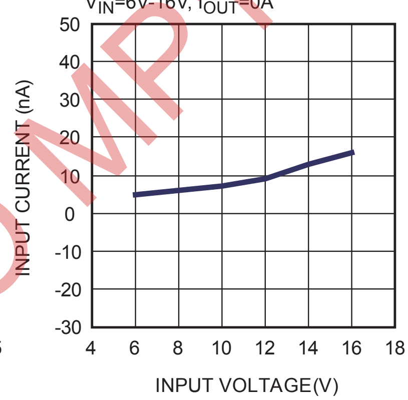
Line Regulation
V_{IN}=5V-16V



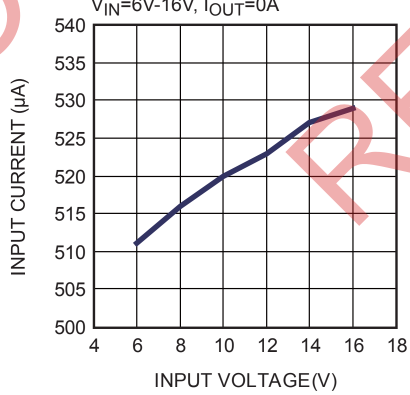
Peak Current vs. Duty Cycle



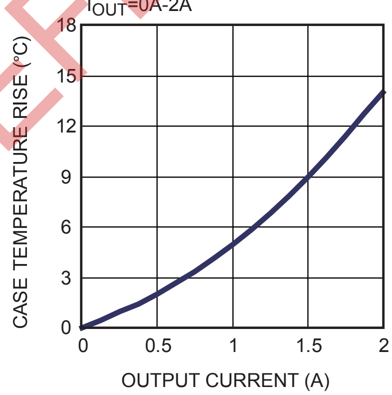
Disabled Supply Current vs. Input Voltage
V_{IN}=6V-16V, I_{OUT}=0A



Enabled Supply Current vs. Input Voltage
V_{IN}=6V-16V, I_{OUT}=0A



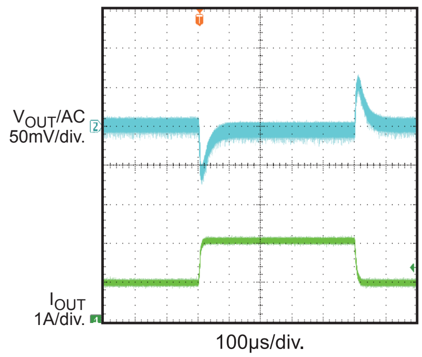
Case Temperature Rise vs. Output Current
I_{OUT}=0A-2A



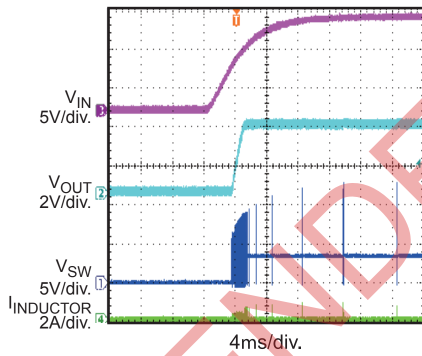
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, AAM=0.5V, T_A = 25°C, unless otherwise noted.

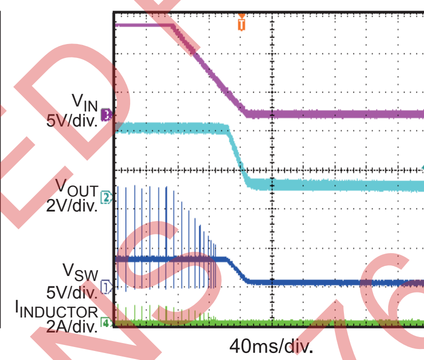
Transient Response
I_{OUT} = 1.2A, 1A/μs



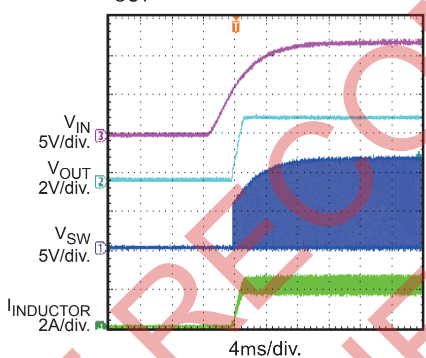
Startup through Input Voltage
I_{OUT} = 0A



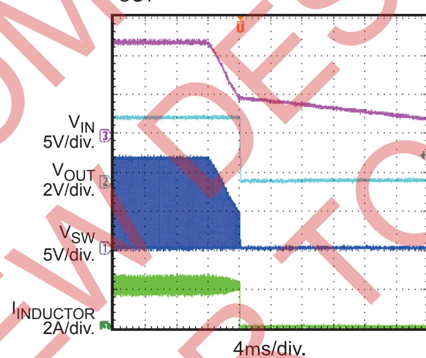
Shutdown through Input Voltage
I_{OUT} =0A



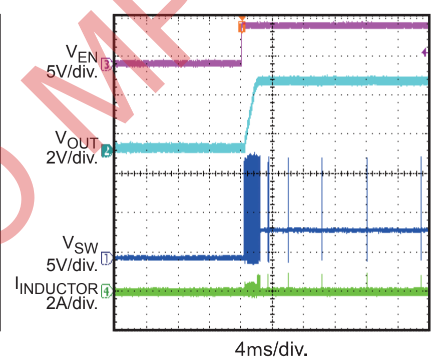
Startup through Input Voltage
I_{OUT} = 2A



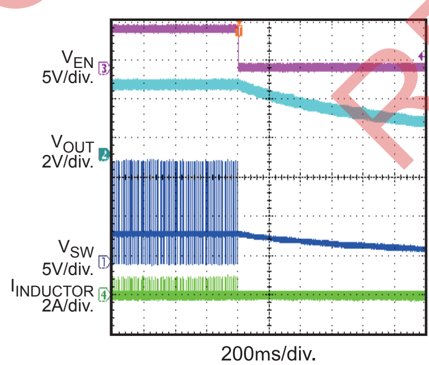
Shutdown through Input Voltage
I_{OUT} = 2A



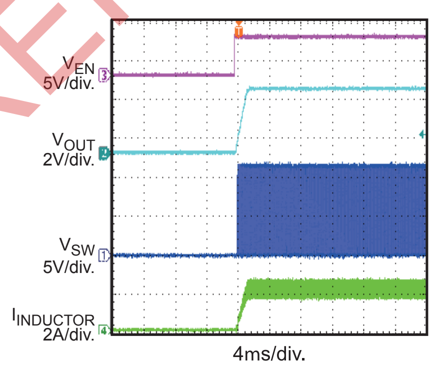
Startup through Enable
I_{OUT} = 0A



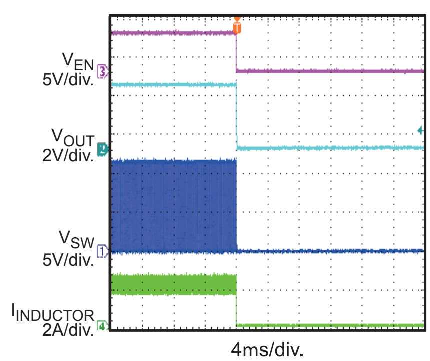
Shuthdown through Enable
I_{OUT} = 0A



Startup through Enable
I_{OUT} = 2A



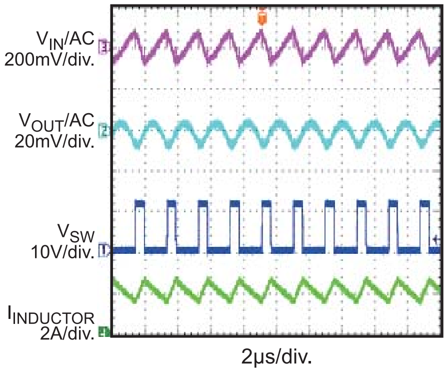
Shutdown through Enable
I_{OUT} = 2A



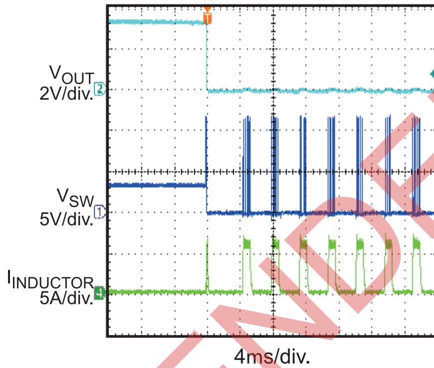
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, AAM=0.5V, T_A = 25°C, unless otherwise noted.

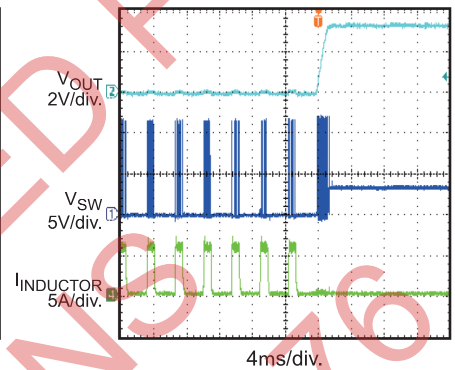
Input/Output Ripple
I_{OUT} = 2A



Short Circuit Entry
I_{OUT} = 0A



Short Circuit Recovery
I_{OUT} =0A



PIN FUNCTIONS

Package Pin #	Name	Description
1	AAM	Advanced Asynchronous Modulation. Connect to a voltage supply through 2 resistor dividers to force the MP1494 into non-synchronous mode under light loads. Drive AAM pin high (V_{CC}) to force the MP1494 into CCM.
2	IN	Supply Voltage. The MP1494 operates from a 4.5V-to-16V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
3	SW	Switch Output. Connect using a wide PCB trace.
4	GND	System Ground. Reference ground of the regulated output voltage. Requires special consideration during PCB layout. Connect to GND with copper traces and vias.
5	BST	Bootstrap. Requires a capacitor between SW and BST pins to form a floating supply across the high-side switch driver. A 10Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.
6	EN/SYNC	EN high to enable the MP1494. Apply an external clock can to the EN pin to change the switching frequency.
7	VCC	Bias Supply. Decouple with a 0.1μF-to-0.22μF capacitor. The capacitance should not exceed 0.22μF. VCC capacitor should be put closely to VCC pin and GND pin.
8	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 400mV to prevent current-limit run-away during a short-circuit fault condition.

FUNCTIONAL BLOCK DIAGRAM

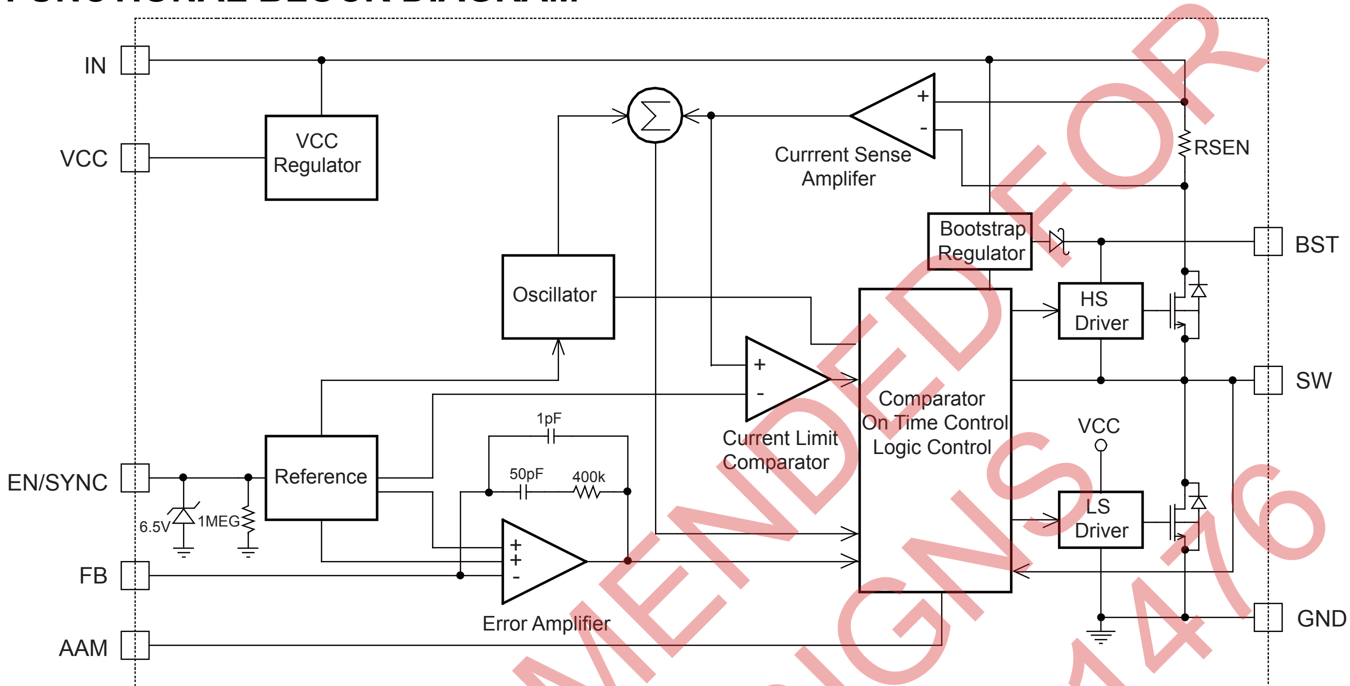


Figure 1: Functional Block Diagram

OPERATION

The MP1494 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves a 2A continuous output current with excellent load and line regulation over a wide input supply range.

The MP1494 operates in a fixed-frequency, peak-current–control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until the current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in within 95% of one PWM period, the current in the power MOSFET does not reach the value set by the COMP value, the power MOSFET is forced to turn off.

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. When V_{IN} is lower than 5.0V, the output decreases, and the part requires a 0.1µF ceramic decoupling capacitor.

Error Amplifier

The error amplifier compares the FB pin voltage against the internal 0.8V reference (REF) and outputs the COMP voltage—COMP controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Enable/SYNC control

EN/SYNC is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive it low to turn it off. An internal 1MΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

The EN pin is clamped internally using a 6.7V series-Zener-diode as shown in Figure 2. Connecting the EN input pin through a pullup resistor to the voltage on the V_{IN} pin limits the EN input current to less than 100µA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V – 6.5V) \div 100µA = 55kΩ$.

Connecting the EN pin is directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to ≤6V to prevent damage to the Zener diode.

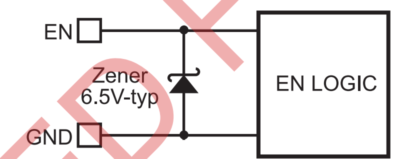


Figure 2: 6.5V Zener Diode Connection

For external clock synchronization, connect a clock with a frequency range between 200kHz and 2MHz 2ms after the output voltage is set: The internal clock rising edge will synchronize with the external clock rising edge. Select an external clock signal with a pulse width less than 1.7µs.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. The MP1494 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 3.9V while its falling threshold is 3.25V.

Internal Soft-Start

The soft-start prevents the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to 1.2V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is internally set to 1.5ms.

Over-Current-Protection and Hiccup

The MP1494 has a cycle-by-cycle over-current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, the output voltage drops until FB is below the Under-Voltage (UV) threshold—typically 50% below the reference. Once UV is triggered, the MP1494 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. The average short circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The MP1494 exits the hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 150°C, it shuts down the whole chip. When the temperature is less than its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1 and C2 (Figure 3). If (V_{IN}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4. A 10Ω resistor placed between SW and BST cap is strongly recommended to reduce SW spike voltage.

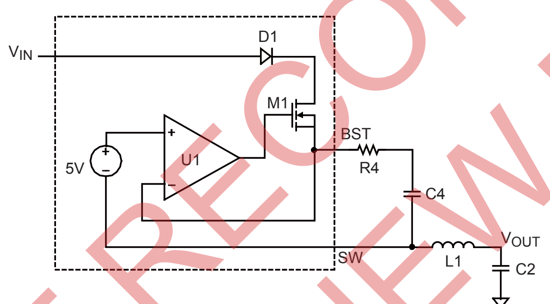


Figure 3: Internal Bootstrap Charging Circuit,
Startup and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Typical Application on page 1). Choose R1 around 40kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.807V} - 1}$$

The T-type network—as shown in Figure 4—is highly recommended when V_{OUT} is low.

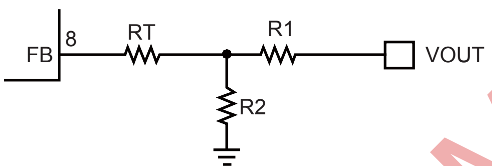


Figure 4: T-Type Network

Table 1 lists the recommended T-type resistors value for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Rt (kΩ)
1.0	20.5(1%)	82(1%)	82(1%)
1.2	30.1(1%)	60.4(1%)	82(1%)
1.8	40.2(1%)	32.4(1%)	56(1%)
2.5	40.2(1%)	19.1(1%)	33(1%)
3.3	40.2(1%)	13(1%)	33(1%)
5	40.2(1%)	7.68(1%)	33(1%)

Selecting the Inductor

Use a1µH-to-10µH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

Setting the AAM Voltage

The AAM voltage sets the transition point from AAM to CCM. Select a voltage to balance efficiency, stability, ripple, and transient.

A low AAM voltage improves stability and ripple, but degrades transient and efficiency during AAM. Likewise, a high AAM voltage improves the transient and efficiency during AAM, but degrades stability and ripple.

The AAM voltage comes from the tap of a resistor divider from V_{CC} (5V) to GND, as shown in Figure 5.

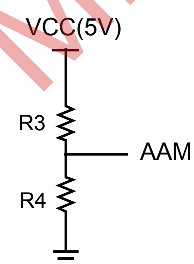


Figure 5: AAM Network

Generally, choose R4 to be around 10kΩ, then R3 is:

$$R3 = R4\left(\frac{VCC}{AAM} - 1\right)$$

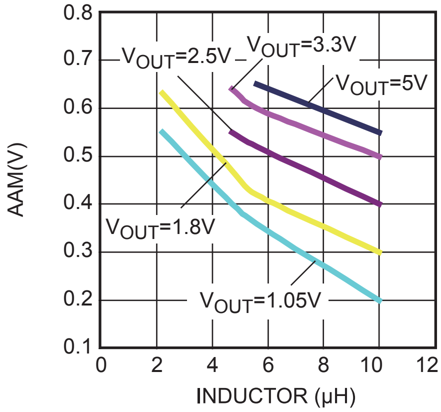


Figure 6: AAM Values for Common Output Voltages (V_{IN} = 4.5V to 16V)

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor is to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\ 2} \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP1494 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An external bootstrap diode can enhance the efficiency of the regulator given the following conditions:

- V_{OUT} is 5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In these cases, add an external BST diode from the VCC pin to BST pin, as shown in Figure 7.

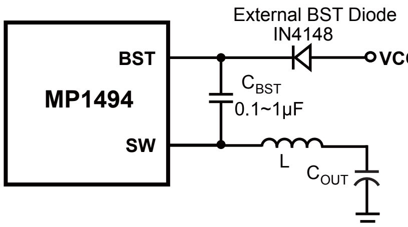


Figure 7: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1μF to 1μF.

PC Board Layout [8]

PCB layout is very important to achieve stable operation especially for VCC capacitor and input capacitor placement. For best results, follow these guidelines:

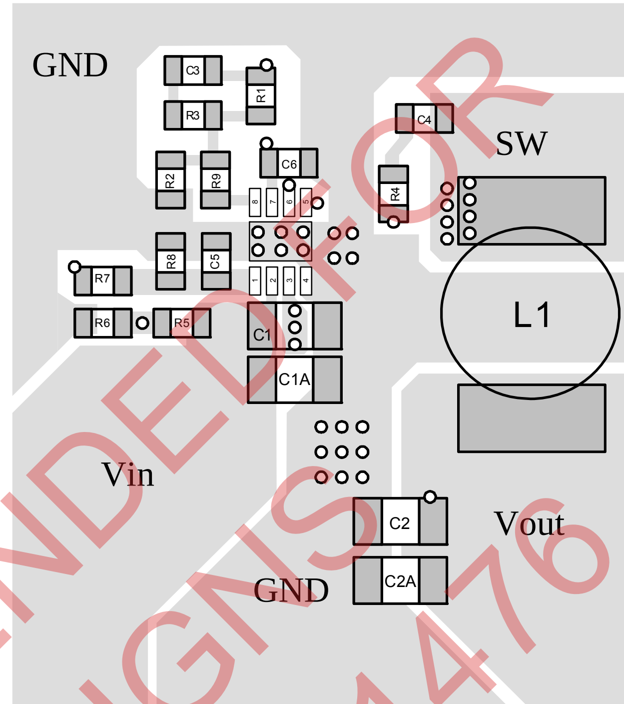
1) Use large ground plane directly connect to GND pin. Add vias near the GND pin if bottom layer is ground plane.

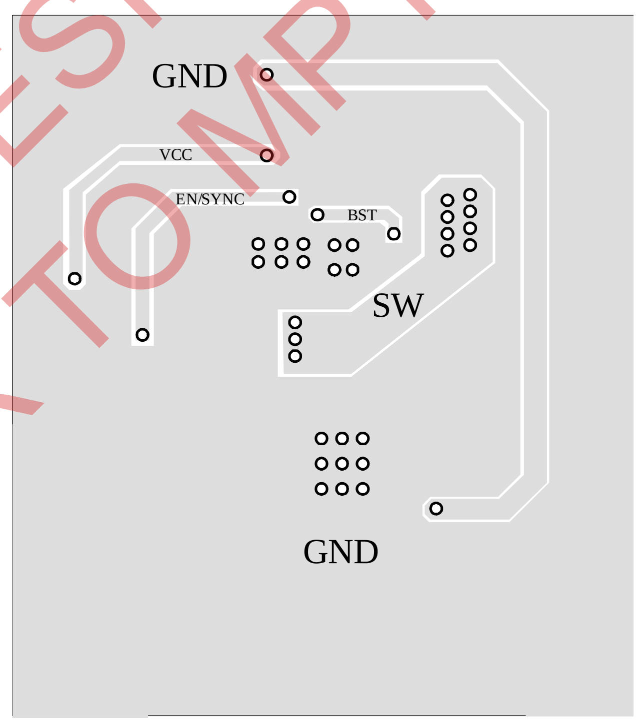
2) Place the VCC capacitor to VCC pin and GND pin as close as possible. Make the trace length of VCC pin-VCC capacitor anode-VCC capacitor cathode-chip GND pin as short as possible.

3) Place the ceramic input capacitor close to IN and GND pins. Keep the connection of input capacitor and IN pin as short and wide as possible.

4) Route SW, BST away from sensitive analog areas such as FB. It's not recommended to route SW, BST trace under chip's bottom side.

5) Place the T-type feedback resistor R9 close to chip to ensure the trace which connects to FB pin as short as possible





Notes:

8) The recommended layout is based on the Figure 8 Typical Application circuit on the next page.

TYPICAL APPLICATION CIRCUITS

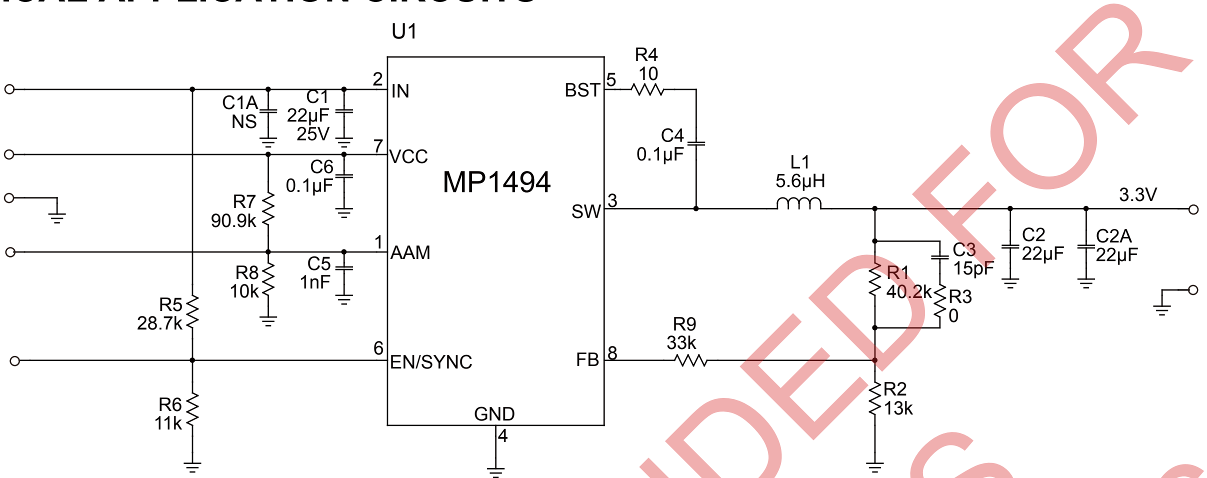
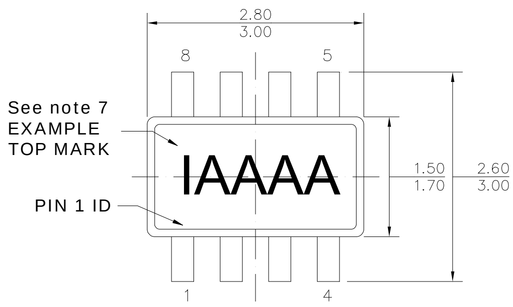


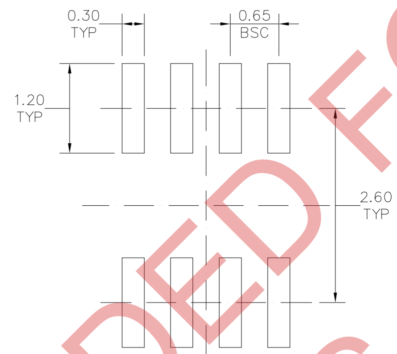
Figure 8: 12V$_{IN}$, 3.3V/2A

PACKAGE INFORMATION

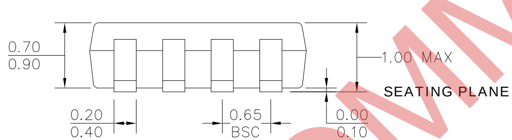
TSOT23-8



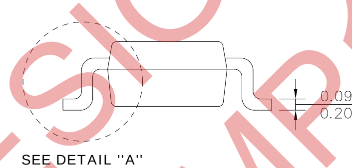
TOP VIEW



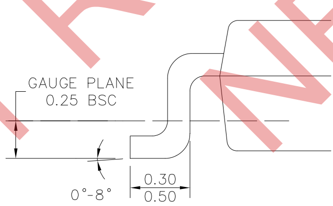
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)