

### DESCRIPTION

The MP172A is a primary-side regulator that provides accurate constant voltage (CV) regulation without an optocoupler. It supports buck, boost, buck-boost, and flyback topologies.

The device's integrated 700V MOSFET simplifies the structure and reduces cost. This feature optimizes the device for offline, low-power applications such as home appliances and standby power.

The MP172A is a green-mode operation regulator. Both the peak current and switching frequency lower as the load decreases. This feature provides excellent efficiency at light load, and improves the overall average efficiency.

Protection features include thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), short-circuit protection (SCP), and open-loop detection.

The MP172A is available in TSOT23-5 and SOIC-8 packages.

### FEATURES

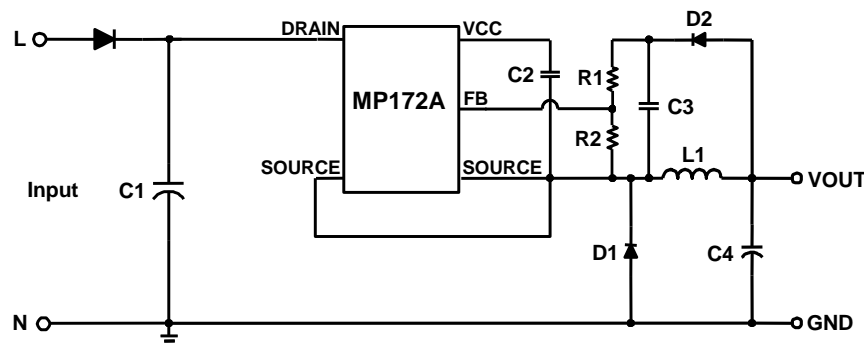
- Primary-Side CV Control
- Supports Buck, Boost, Buck-Boost, and Flyback Topologies
- Integrated 700V MOSFET and Current Source
- Under 30mW No-Load Power Consumption
- Up to 3W Output Power
- Maximum DCM Output Current below 80mA
- Maximum CCM Output Current below 120mA
- Low VCC Operating Current
- Frequency Foldback
- Limited Maximum Frequency
- Peak Current Compression
- Internally Biased VCC
- TSD, UVLO, OLP, SCP, and Open-Loop Detection
- Available in TSOT23-5 and SOIC-8 Packages

### APPLICATIONS

- Home Appliances, White Goods, and Consumer Electronics
- Industrial Controls
- Standby Power

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### TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP172AGJ*	TSOT23-5	See Below	1
MP172AGS**	SOIC-8	See Below	2

\* For Tape & Reel, add suffix – Z (e.g. MP172AGJ–Z).

\*\* For Tape & Reel, add suffix – Z (e.g. MP172AGS–Z).

### TOP MARKING (MP172AGJ)

| BMVY

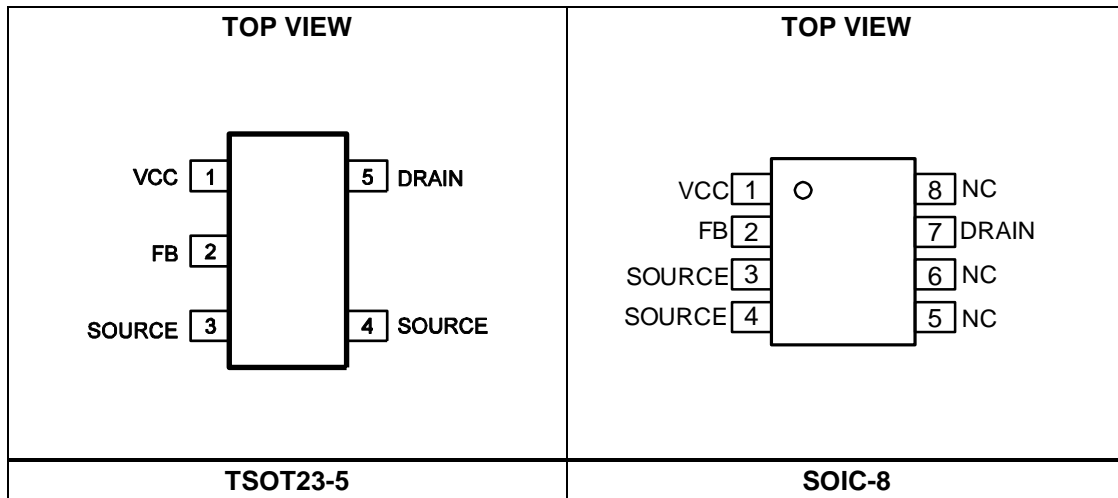
BMV: Product code  
Y: Year code

### TOP MARKING (MP172AGS)

MP172A  
LLLLLLLLL  
MPSYWW

MP172A: Part number  
LLLLLLLLL: Lot number  
MPS: MPS prefix  
Y: Year code  
WW: Week code

## PACKAGE REFERENCE



## PIN FUNCTIONS

Pin # TSOT23-5	Pin # SOIC8	Name	Description
1	1	VCC	<b>Control circuit power supply.</b>
2	2	FB	<b>Regulator feedback.</b>
3, 4	3, 4	SOURCE	<b>Internal power MOSFET source.</b> Ground reference for the VCC and FB pins.
5	7	DRAIN	<b>Internal power MOSFET drain.</b> High-voltage current source input.
	5, 6, 8	N/C	<b>Not connected.</b>

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Drain to source ( $T_J = 25^\circ\text{C}$ ).....	-0.3V to +700V
All other pins.....	-0.3V to +6.5V
Continuous power dissipation ..... ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup>	
TSOT23-5.....	1W
SOIC-8 .....	1W
Junction temperature .....	150°C
Lead temperature .....	260°C
Storage temperature.....	-60°C to +150°C

**ESD Rating**

Human-body model (HBM) .....	2.0kV
Charged-device model (CDM)	
TSOT23-5.....	1.2kV
SOIC-8.....	1.5kV

**Recommended Operating Conditions** <sup>(3)</sup>

Operating junction temp ( $T_J$ ) ....	-40°C to +125°C
Operating VCC range .....	5.5V to 5.7V

<b>Thermal Resistance</b> <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$
TSOT23-5 .....	100 .....	55 ... °C/W
SOIC-8.....	96 .....	45 ... °C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowance continuous power dissipation at any ambient temperature is calculated with  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowance power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuit protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

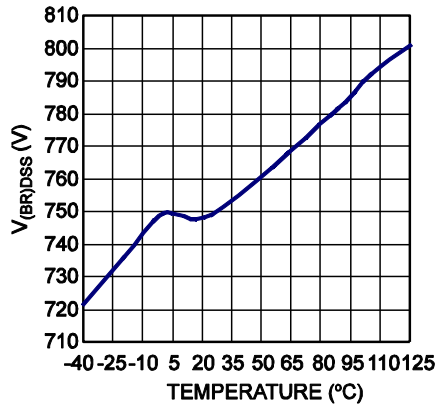
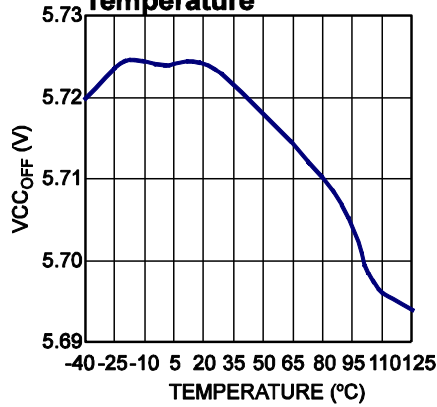
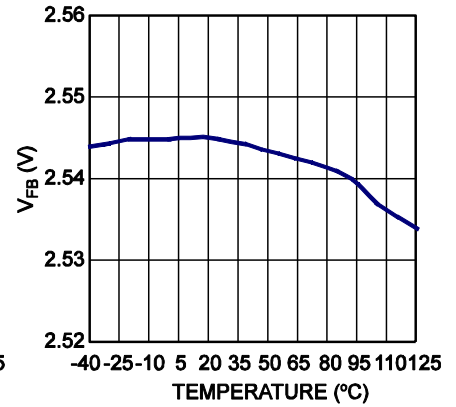
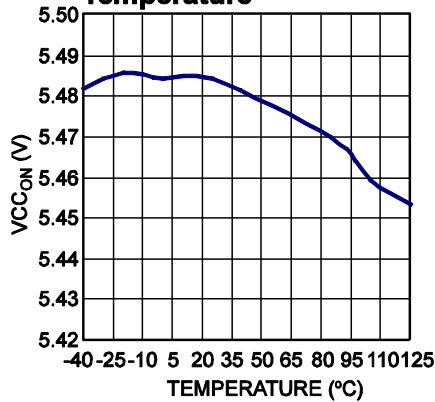
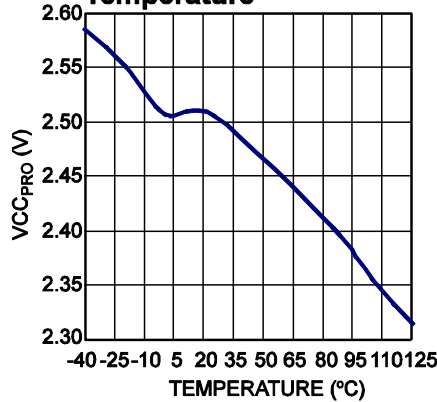
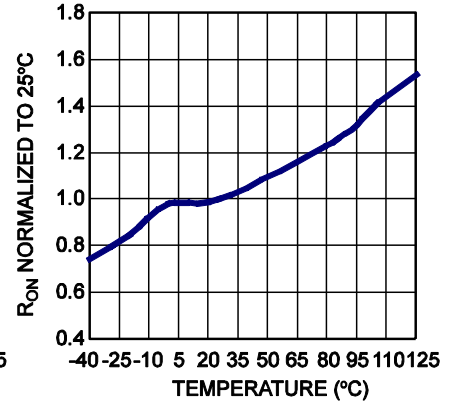
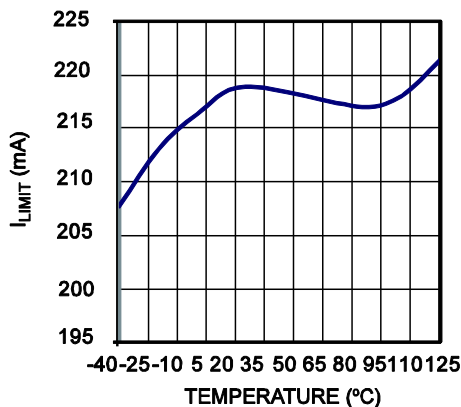
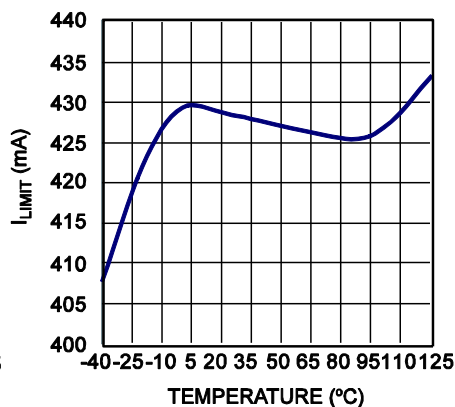
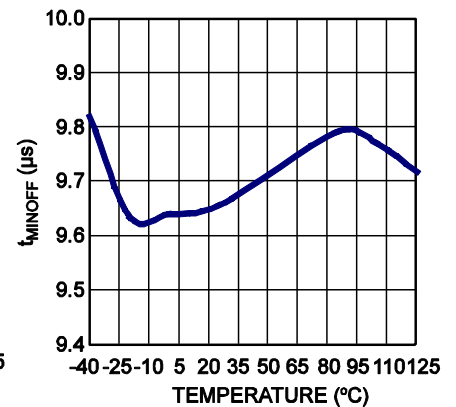
## ELECTRICAL CHARACTERISTICS

VCC = 5.5V, T<sub>J</sub> = -40°C to +125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Start-Up Current Source and Internal MOSFET (DRAIN)</b>						
Internal regulator supply current	I <sub>REGULATOR</sub>	VCC = 4V, V <sub>DRAIN</sub> = 100V	2.2	4.1	6	mA
DRAIN leakage current	I <sub>LEAK</sub>	VCC = 5.8V, V <sub>DRAIN</sub> = 400V		10	17	μA
Breakdown voltage	V <sub>(BR)DSS</sub>	T <sub>J</sub> = 25°C	700			V
On resistance	R <sub>ON</sub>	T <sub>J</sub> = 25°C		16	20	Ω
<b>Supply Voltage Management (VCC)</b>						
VCC increasing level where the internal regulator stops	VCC <sub>OFF</sub>		5.4	5.7	6	V
VCC decreasing level where the internal regulator turns on	VCC <sub>ON</sub>		5.1	5.5	5.8	V
VCC regulator on and off hysteresis			130	250		mV
VCC decreasing level where the IC stops	VCC <sub>STOP</sub>		3	3.4	3.6	V
VCC decreasing level where the protection phase ends	VCC <sub>PRO</sub>		2	2.5	2.8	V
Internal IC consumption	I <sub>CC</sub>	f <sub>sw</sub> = 36kHz, D = 64%			720	μA
Internal IC consumption (no switching)					200	μA
Internal IC consumption (latch-off phase)	ICCLATCH	VCC = 5.3V		16	24	μA
<b>Internal Current Sense</b>						
Peak current limit	I <sub>LIMIT</sub>	T <sub>J</sub> = 25°C	197	220	243	mA
Leading-edge blanking	t <sub>LEB1</sub>			350		ns
SCP threshold	I <sub>SCP</sub>	T <sub>J</sub> = 25°C	355	440	550	mA
Leading-edge blanking for SCP <sup>(5)</sup>	t <sub>LEB2</sub>			180		ns
<b>Feedback Input (FB)</b>						
Minimum off time	t <sub>MINOFF</sub>		7.5	10	12.5	μs
Maximum on time	t <sub>MAXON</sub>		13	18	23	μs
Primary MOSFET feedback turn-on threshold	V <sub>FB</sub>		2.45	2.55	2.65	V
OLP feedback trigger threshold	V <sub>FB_OLP</sub>		1.64	1.74	1.84	V
OLP delay time	t <sub>OLP</sub>	f <sub>sw</sub> = 36kHz		175		ms
Open-loop detection	V <sub>OLD</sub>		0.4	0.5	0.6	V
<b>Thermal Shutdown</b>						
Thermal shutdown threshold <sup>(5)</sup>				150		°C
Thermal shutdown recovery hysteresis <sup>(5)</sup>				30		°C

**Note:**

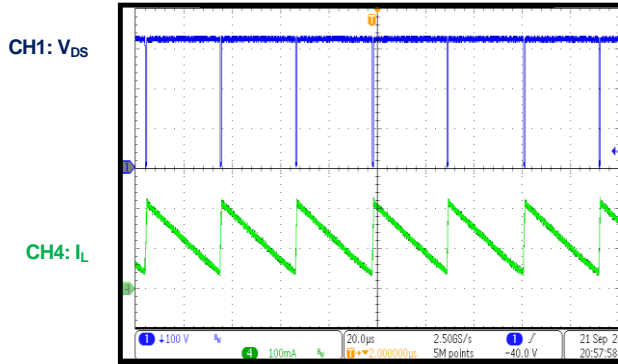
5) This parameter is guaranteed by design.

**TYPICAL CHARACTERISTICS**
**Breakdown Voltage vs. Temperature**

**VCC Increasing Level at which the Internal Regulator Stops vs. Temperature**

**Feedback Voltage vs. Temperature**

**VCC Decreasing Level at which the Internal Regulator Turns On vs. Temperature**

**VCC Decreasing Level at which the Protection Phase Ends vs. Temperature**

**On State Resistance vs. Temperature**

**Peak Current Limit vs. Temperature**

**SCP Point vs. Temperature**

**Minimum Off Time vs. Temperature**


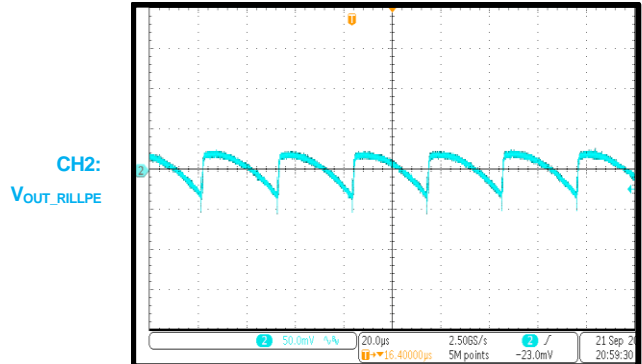
### TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 230VAC$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 120mA$ ,  $L = 1mH$ ,  $C_{OUT} = 47\mu F$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

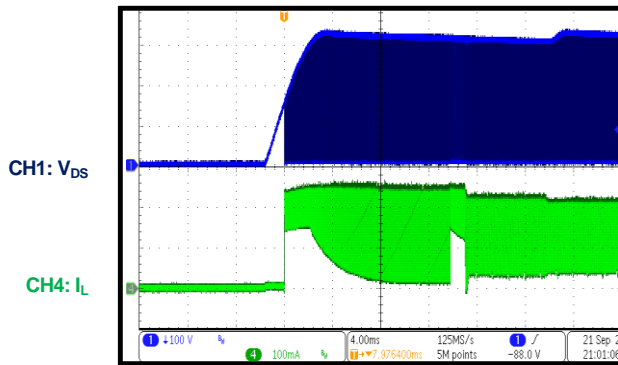
Steady State



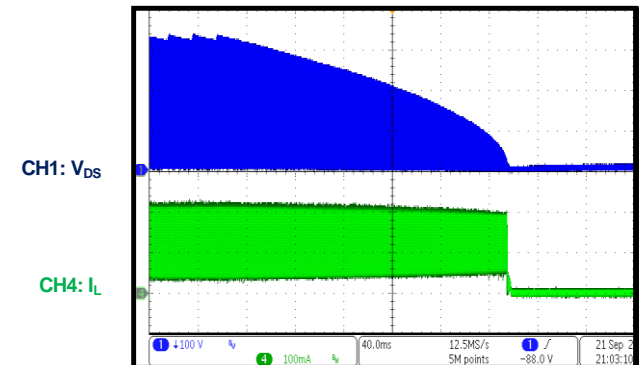
Output Ripple



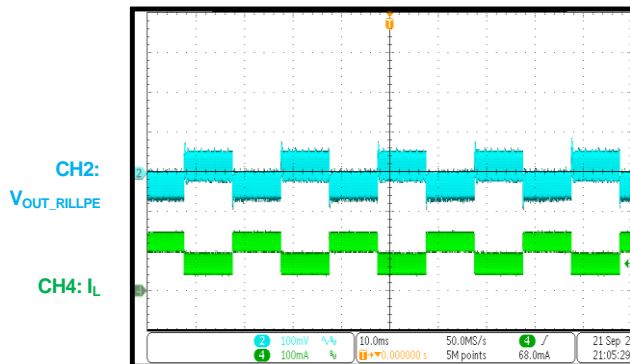
Start-Up



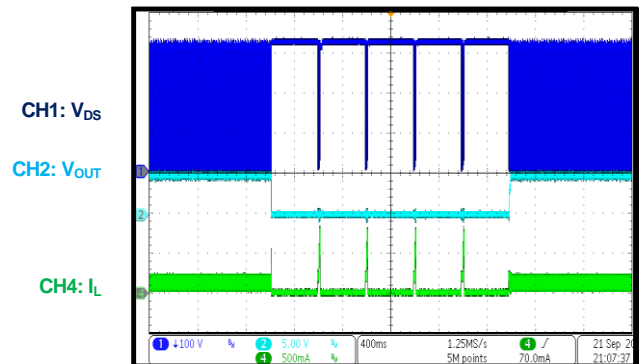
Shutdown



Load Transient  
Half-Load to Full Load



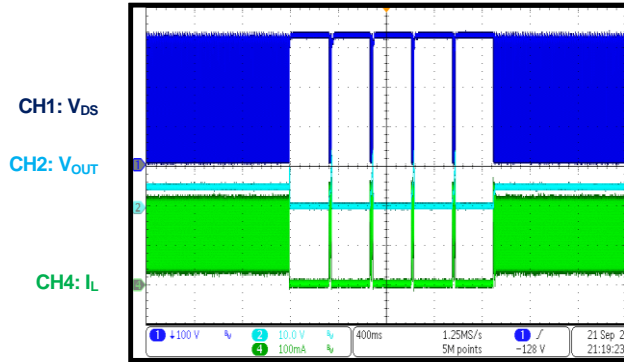
SCP Entry and Recovery



### TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 230VAC$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 120mA$ ,  $L = 1mH$ ,  $C_{OUT} = 47\mu F$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

#### Open-Loop Entry and Recovery





### FUNCTIONAL BLOCK DIAGRAM

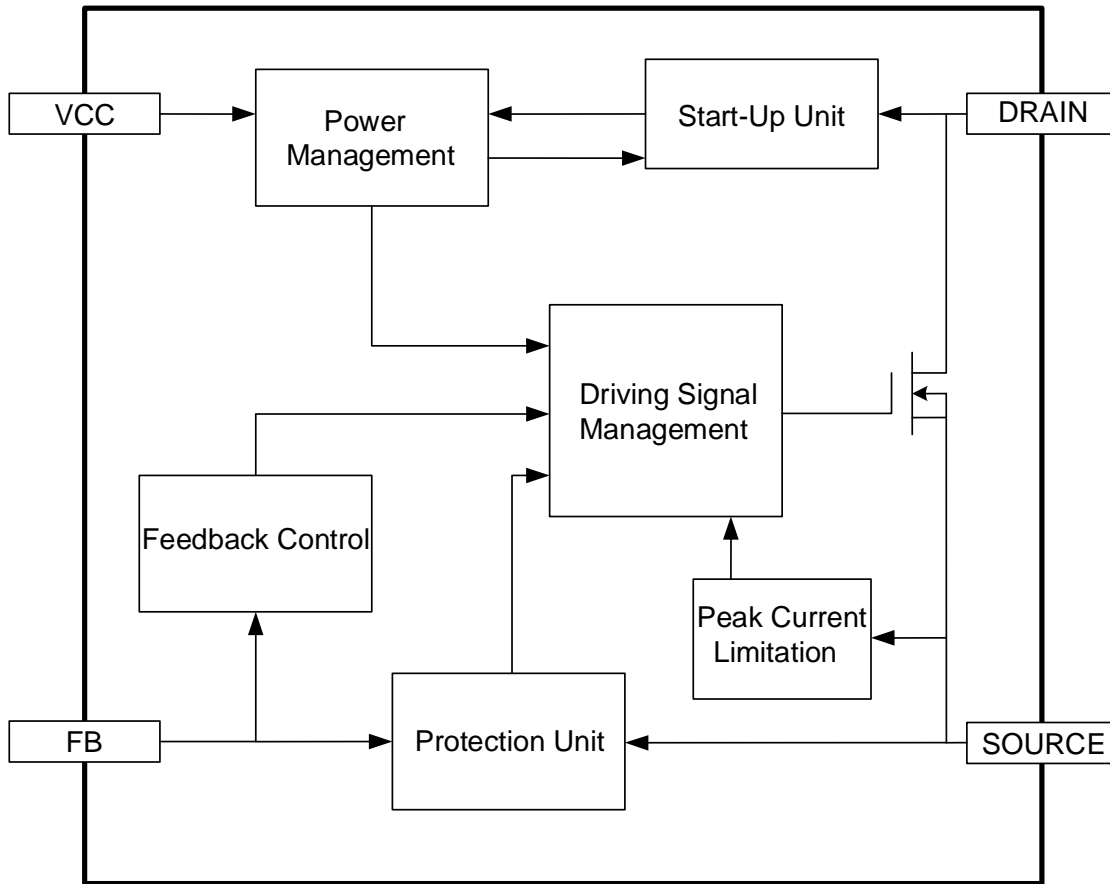


Figure 1: Functional Block Diagram

## OPERATION

The MP172A is a green-mode operation regulator. The peak current and the switching frequency both drop with a decreasing load. As a result, the device offers excellent light-load efficiency and improves overall efficiency. The regulator incorporates multiple features and operates with a minimal number of external components.

The device acts as a fully integrated regulator when used in buck topology (see Typical Application on page 1).

### Start-Up and Under-Voltage Lockout

The internal high-voltage regulator self-supplies the IC from DRAIN. When the VCC voltage reaches VCC<sub>OFF</sub>, the IC switches and the internal high-voltage regulator turns off. The internal high-voltage regulator turns on to charge the external VCC capacitor when the VCC voltage falls below VCC<sub>ON</sub>. A capacitor with a low μF value is recommended to maintain the VCC voltage, and **lowers** the capacitor cost.

The IC stops switching when the VCC voltage drops below VCC<sub>STOP</sub>.

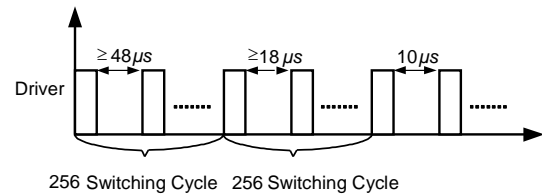
If a fault condition occurs, such as overload protection (OLP), short-circuit protection (SCP), or thermal shutdown (TSD), the IC stops switching. The internal current source, I<sub>CCLATCH</sub> (about 16μA), discharges the VCC capacitor. The internal high-voltage regulator does not charge the VCC capacitor until the VCC voltage drops below VCC<sub>PRO</sub>. The restart time can be estimated with Equation (1):

$$t_{\text{RESTART}} = C_{\text{VCC}} \times \left( \frac{V_{\text{CC}} - V_{\text{CC}_{\text{PRO}}}}{I_{\text{CCLATCH}}} + \frac{V_{\text{CC}_{\text{OFF}}} - V_{\text{CC}_{\text{PRO}}}}{I_{\text{REGULATOR}}} \right) \quad (1)$$

### Soft Start (SS)

The MP172A stops operation if the VCC voltage drops below VCC<sub>STOP</sub>. Operation resumes when VCC charges to VCC<sub>OFF</sub>. When the IC initiates operation, there is always a soft-start period. The soft start limits the minimum off time to prevent the inductor current from overshooting.

The MP172A adopts a two-phase minimum off time limit soft start. Each phase retains 256 switching cycles. During a soft start, the off time limit gradually shortens from 48μs to 18μs until it reaches the standard off time limit (see Figure 2).



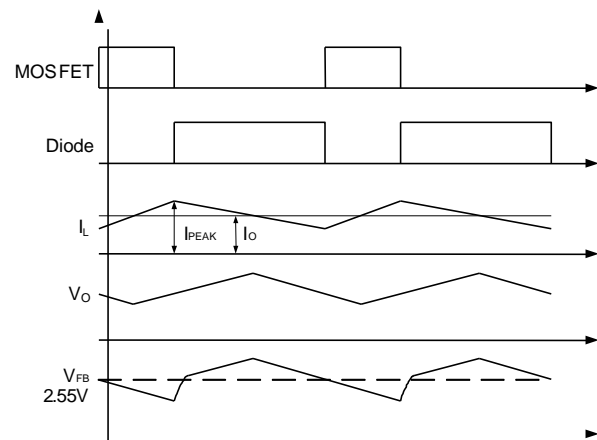
**Figure 2: t<sub>MINOFF</sub> at Start-Up**

### Constant Voltage (CV) Operation

Take Typical Application on page 1 for reference, the MP172A regulates the output voltage by monitoring the sampling capacitor (C3).

At the beginning of each cycle, the integrated MOSFET turns on when the feedback voltage (V<sub>FB</sub>) and indicates insufficient output. The peak current limitation determines the on period. After the on period, the integrated MOSFET turns off.

The sampling capacitor (C3) voltage charges to the output voltage when the freewheeling diode (D1) turns on. The sampling capacitor (C3) samples and holds the output voltage for output regulation. The sampling capacitor (C3) voltage decreases when the L1 inductor current falls below the output current. When the feedback voltage falls below the 2.55V reference voltage, a new switching cycle begins. Figure 3 shows this operation in continuous conduction mode (CCM).



**Figure 3: V<sub>FB</sub> vs. V<sub>O</sub>**

The output voltage (V<sub>O</sub>) can be estimated with Equation (2):

$$V_O = 2.55V \times \frac{R1 + R2}{R2} \quad (2)$$

### Frequency Foldback and Peak Current Compression

The MP172A automatically reduces the switching frequency to maintain high efficiency during light-load conditions.

Under light-load or no-load conditions, the output voltage drops slowly to increase the MOSFET off time. The frequency drops as the load drops.

The switching frequency can be calculated with Equation (3) and Equation (4) for CCM and DCM, respectively:

$$f_{SW} = \frac{(V_{IN} - V_O)}{2L \times (I_{PEAK} - I_O)} \times \frac{V_O}{V_{IN}} \quad (3)$$

$$f_{SW} = \frac{2(V_{IN} - V_O)}{L \times I_{PEAK}^2} \times \frac{I_O \times V_O}{V_{IN}} \quad (4)$$

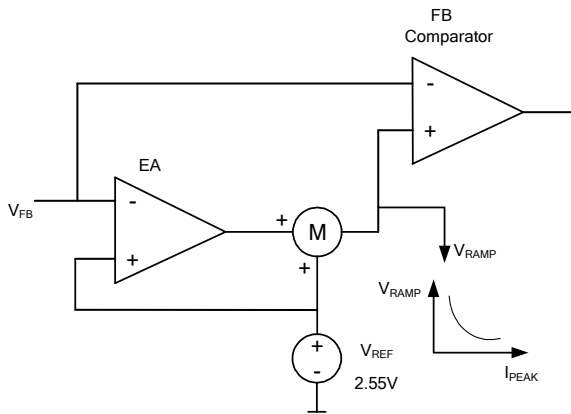
As the peak current limit drops from  $I_{LIMIT}$ , the off time increases. In standby mode, the frequency and the peak current are both minimized to allow for a smaller dummy load. As a result, peak current compression reduces no-load consumption. The peak current limit can be estimated with Equation (5):

$$I_{PEAK} = 220\text{mA} - (1.6\text{mA}/\mu\text{s}) \times (t_{OFF} - 10\mu\text{s}) \quad (5)$$

Where  $t_{OFF}$  is the off time of the power module.

### EA Compensation

The MP172A has an internal error amplifier (EA) compensation loop (see Figure 4). It samples the feedback voltage  $6\mu\text{s}$  after the MOSFET turns off, and regulates the output based on the 2.55V reference voltage.



**Figure 4: EA and Ramp Compensation**

### Ramp Compensation

An internal ramp compensation circuit improves the load regulation. An exponential voltage signal is added to pull down the feedback comparator's reference voltage (see Figure 4). The ramp compensation is a function of the load conditions: the compensation is about  $1\text{mV}/\mu\text{s}$  under full-load conditions. The compensation increases exponentially as the peak current decreases.

### Overload Protection (OLP)

The MP172A's maximum output power is limited by the minimum off time and peak current limit. If the load is too large, the output voltage drops with the feedback voltage.

An error occurs when  $V_{FB}$  drops below  $V_{FB\_OLP}$ , and the timer starts. If the timer reaches 170ms ( $f_{SW} = 36\text{kHz}$ ), overload protection (OLP) occurs. This timer duration avoids triggering OLP when the power supply starts up or the load transitions. The power supply should start up in less than 170ms ( $f_{SW} = 36\text{kHz}$ ). The OLP delay time is calculated with Equation (6):

$$t_{DELAY} \approx 170\text{ms} \times \frac{36\text{kHz}}{f_{SW}} \quad (6)$$

### Short-Circuit Protection (SCP)

The MP172A monitors the peak current, and shuts down when the peak current exceeds the short-circuit protection (SCP) threshold. The power supply resumes operation once the fault is removed. During soft start and the following 512 cycles, SCP is blanked to guarantee a successful start-up with a large output capacitor.

### Thermal Shutdown (TSD)

To prevent thermal damage, the MP172A stops switching when the junction temperature exceeds  $150^\circ\text{C}$ . During thermal shutdown (TSD), the VCC capacitor is discharged to  $V_{CC\_PRO}$ , and the internal high-voltage regulator recharges. The device recovers when the junction temperature falls below  $120^\circ\text{C}$ .

### Open-Loop Detection

If  $V_{FB}$  drops below  $V_{OLD}$ , the IC stops switching and initiates a restart period. During soft start and the following 512 cycles, open-loop detection is blanked. This guarantees successful start-up with a large output capacitor.

### Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit avoids premature switching pulse termination due to a turn-on spike. Turn-on spikes are caused by parasitic capacitance and reverse recovery of the freewheeling diode. During the blanking time, the current comparator is disabled and cannot turn off the external MOSFET. Figure 5 shows the leading-edge blanking.

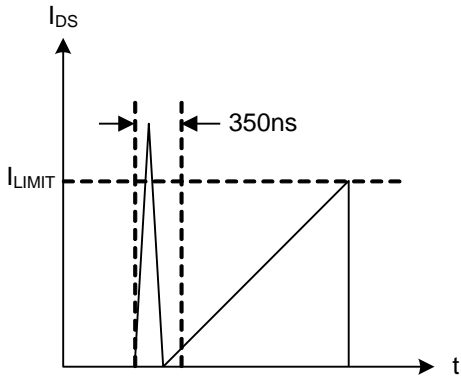


Figure 5: Leading-Edge Blanking

**APPLICATION INFORMATION**
**Table 1: Common Topologies for the MP172A**

Topology	Circuit Schematic	Features
High-side buck		<ul style="list-style-type: none"> <li>• No isolation</li> <li>• Positive output</li> <li>• Low cost</li> <li>• Direct feedback</li> </ul>
High-side buck-boost		<ul style="list-style-type: none"> <li>• No isolation</li> <li>• Negative output</li> <li>• Low cost</li> <li>• Direct feedback</li> </ul>
Boost		<ul style="list-style-type: none"> <li>• No isolation</li> <li>• Positive output</li> <li>• Low cost</li> <li>• Direct feedback</li> </ul>
Flyback		<ul style="list-style-type: none"> <li>• Isolation</li> <li>• Positive output</li> <li>• Low cost</li> <li>• Indirect feedback</li> </ul>

## Topology Options

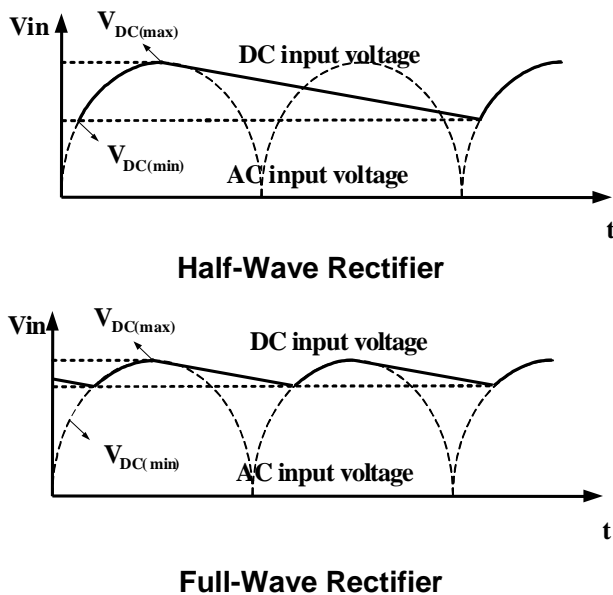
The MP172A can be used in common topologies, such as buck, boost, buck-boost, and flyback (see Table 1 on page 13).

Component selections below are based on the MP172A's typical application (see page 1).

## Component Selection

### Input Capacitor

The input capacitor supplies the DC input voltage for the converter. Figure 6 shows the typical DC bus voltage waveform of a half-wave rectifier and a full-wave rectifier.



**Figure 6: Input Voltage Waveform**

A half-wave rectifier typically requires an input capacitor (about 3 $\mu$ F/W) for the universal input condition. When using the full-wave rectifier, the input capacitor should be between 1.5 $\mu$ F/W and 2 $\mu$ F/W for the universal input condition.

Avoid a minimum DC voltage below 70V. A low DC input voltage can cause thermal instability. A half-wave rectifier is recommended for output applications that do not require more than 2W; otherwise, a full-wave rectifier is recommended for output applications that require more than 2W.

### Inductor

The MP172A has a minimum off time limit that determines the maximum power output. The maximum power increases as the inductor increases. A small inductor may cause a failure at full load, but a larger inductor means a higher

overload protection (OLP) load. It is recommended to select an inductor with the lowest value possible to supply the rated power.

The maximum power ( $P_{OMAX}$ ) can be estimated with Equation (7) and Equation (8) for CCM and DCM, respectively:

$$P_{OMAX} = V_O \times (I_{PEAK} - \frac{V_O \times t_{MINOFF}}{2L}) \quad (7)$$

$$P_{OMAX} = \frac{1}{2} L \times I_{PEAK}^2 \times \frac{1}{t_{MINOFF}} \quad (8)$$

For mass production, be sure to consider tolerance on the parameters (e.g. peak current limitation and minimum off time).

### Freewheeling Diode

The diode should be selected based on the maximum input voltage and peak current.

The freewheeling diode's reverse recovery can affect efficiency and circuit operation for CCM conditions. A diode such as the EGC10JH is recommended.

### Output Capacitor

The output capacitor is required to maintain the DC output voltage. The output voltage ripple can be calculated with Equation (9) and Equation (10) for CCM and DCM, respectively:

$$V_{CCM\_RIPPLE} = \frac{\Delta I}{8f_{SW} \times C_O} + \Delta I \times R_{ESR} \quad (9)$$

$$V_{DCM\_RIPPLE} = \frac{I_o}{f_{SW} \times C_O} \times \left( \frac{I_{PEAK} - I_o}{I_{PEAK}} \right)^2 + I_{PEAK} \times R_{ESR} \quad (10)$$

To reduce the output voltage ripple, use ceramic, tantalum, or low-ESR electrolytic capacitors. A maximum 470 $\mu$ F capacitance is recommended in typical applications to avoid triggering SCP during start-up.

### Feedback Resistors

The resistor divider determines the output voltage. Choose appropriate R1 and R2 values to maintain feedback voltage at 2.55V. R2 should typically be between 5k $\Omega$  and 10k $\Omega$ . Avoid a large R2 value.

### Feedback Capacitor

The feedback capacitor provides a sample and hold function. Small capacitors result in poor

regulation at light loads, and large capacitors affect the circuit operation. The optimal capacitor value can be estimated with Equation (11):

$$\frac{1}{2} \times \frac{V_o}{R1+R2} \times \frac{C_o}{I_o} \leq C_{FB} \leq \frac{V_o}{R1+R2} \times \frac{C_o}{I_o} \quad (11)$$

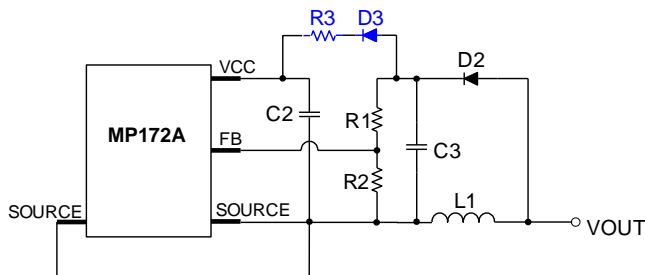
### Dummy Load

A dummy load is required to maintain the load regulation. This ensures there is sufficient inductor energy to charge the sample and hold capacitor to detect the output voltage. A 3mA dummy load is required; it can be adjusted according to the regulated voltage.

For applications that require a 30mW no-load consumption, there is a tradeoff between small no-load consumption and optimal no-load regulation. Use a Zener diode to reduce no-load consumption if no-load regulation is not vital for the application.

### Auxiliary VCC Supply

For an application where  $V_o$  exceeds 7V, the MP172A can meet a 30mW no-load power requirement. To do this, the chip requires an external VCC supply to reduce overall power consumption (see Figure 7).



**Figure 7: Auxiliary V<sub>CC</sub> Supply Circuit**

This auxiliary VCC supply is derived from the resistor connected between C2 and C3. C3 should be greater than the recommendation (see the Feedback Capacitor section on page 14). D3 is used in case VCC interferes with FB. R3 is determined using Equation (12):

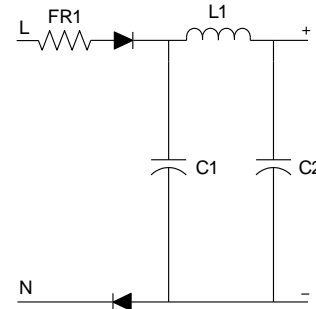
$$R3 \approx \frac{V_o - V_{FW} - 5.8V}{I_s} \quad (12)$$

Where  $I_s$  is the VCC consumption under a no-load condition, and  $V_{FW}$  is the forward voltage drop of D3. R3 should be adjusted to meet the actual  $I_s$ , because it varies in different

applications. In a particular configuration,  $I_s$  is measured at about 200µA.

### Surge Performance

Choose an appropriate input capacitor value to obtain an efficient surge performance. Figure 8 shows the half-wave rectifier.



**Figure 8: Half-Wave Rectifier**

Table 2 shows the capacitance required under normal conditions for different surge voltages. In this example, FR1 is a 20Ω/2W fused resistor and L1 is 1mH.

**Table 2: Recommended Capacitance**

Surge Voltage	500V	1000V	2000V
C1	1µF	2.2µF	3.3µF
C2	1µF	2.2µF	3.3µF

### Design Example

Table 3 shows a design example for the following application guideline specifications:

**Table 3: Design Example**

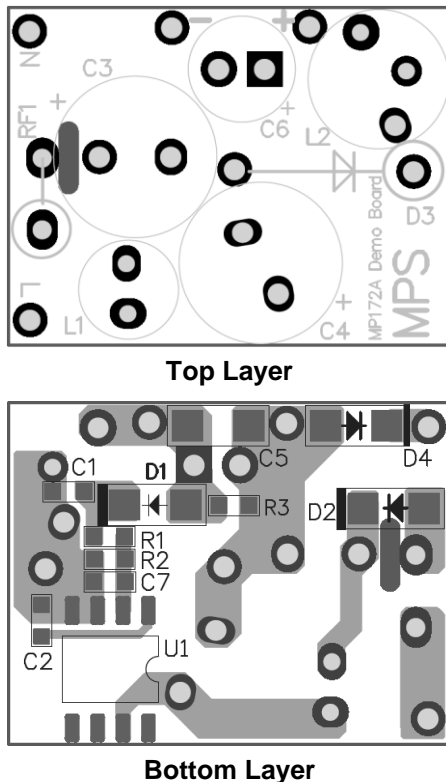
V <sub>IN</sub>	85VAC to 265VAC
V <sub>OUT</sub>	5V
I <sub>OUT</sub>	120mA

Figure 10 shows a detailed application schematic. For the typical performance and circuit waveforms for the device, see the Typical Performance Characteristics section on page 7. Refer to the related evaluation board datasheets for additional information.

### PCB Layout Guidelines

PCB layout is vital for stable operation, good EMI, and improved thermal performance. For the best results, refer to Figure 9 and follow the guidelines below:

1. Minimize the loop area formed by the input capacitor, IC, freewheeling diode, inductor, and output capacitor.
2. Place the power inductor away from the input filter.
3. Minimize the loop area to the inductor (see Figure 9).
4. Place a capacitor valued at several hundred pF between FB and SOURCE, as close to the IC as possible.
5. Connect the exposed pads or large copper area to DRAIN to improve thermal performance.

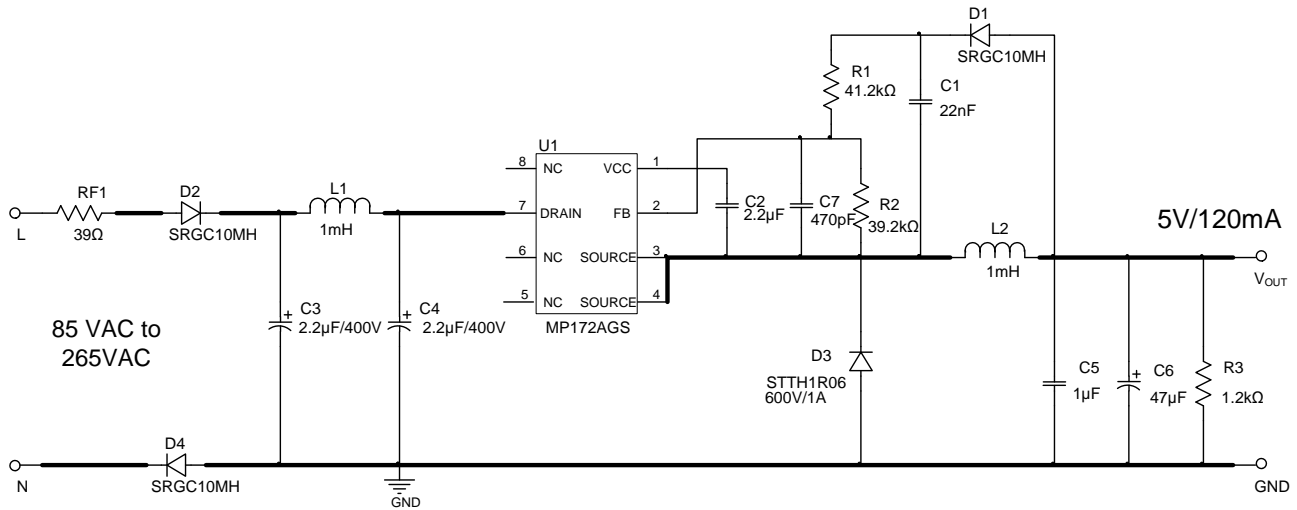


**Figure 9: Recommended PCB Layout**



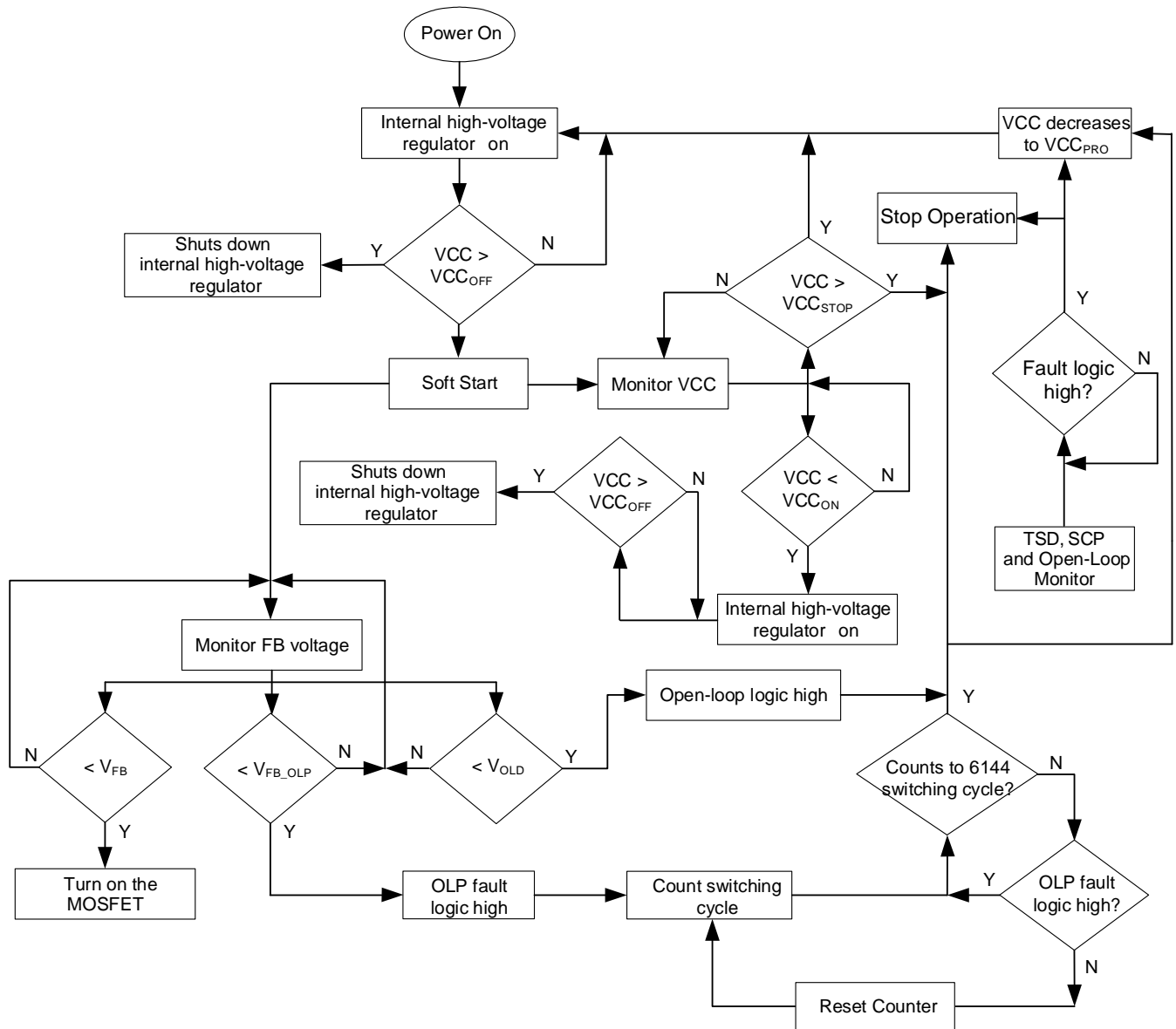
### TYPICAL APPLICATION CIRCUIT

Figure 10 shows a typical application example of a 5V, 120mA non-isolated power supply using the MP172A.



**Figure 10: Typical Application at 5V, 120mA**

FLOWCHART



UVLO, SCP, OLP, OTP and Open-Loop Protections are Auto Restart

Figure 11: Control Flow Chart

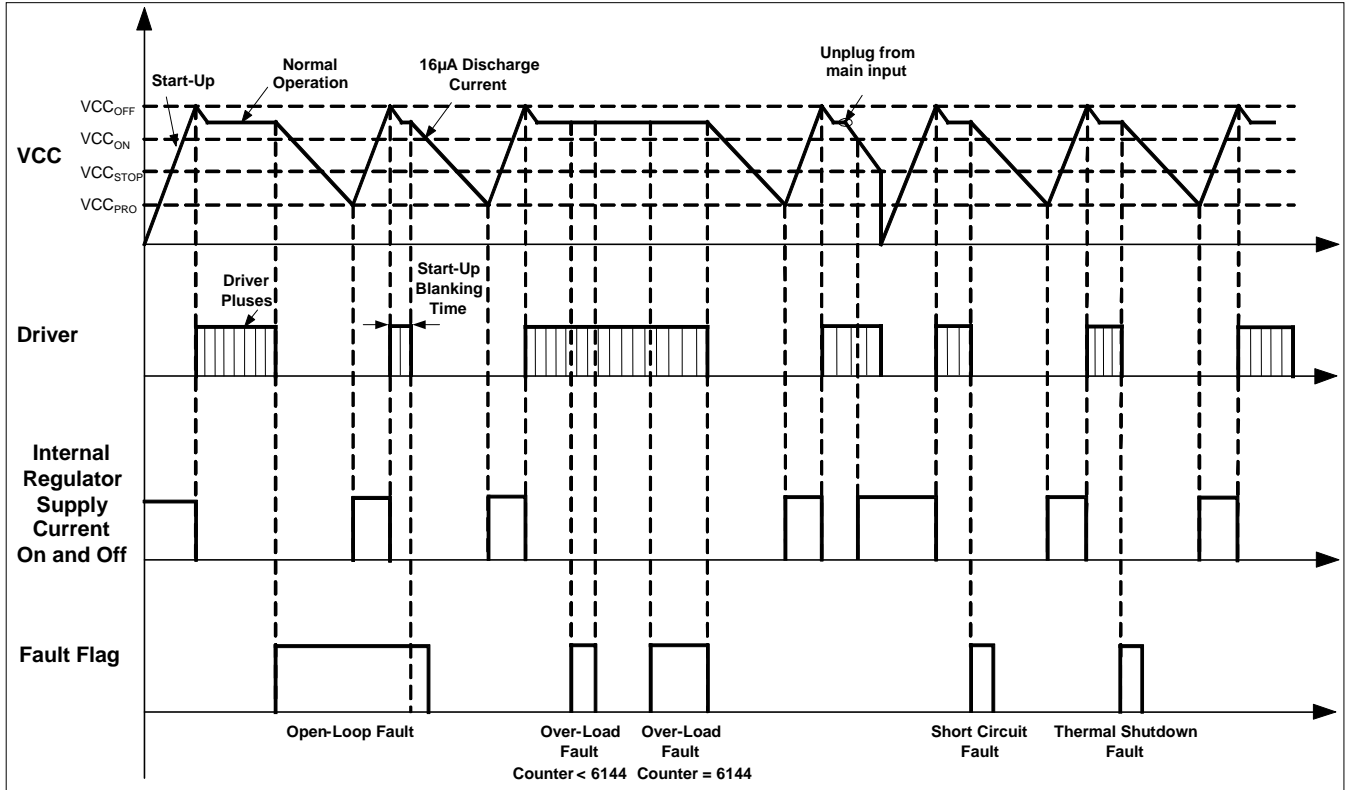
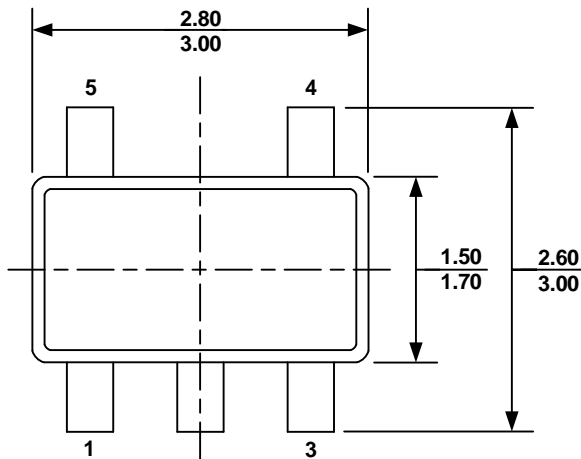
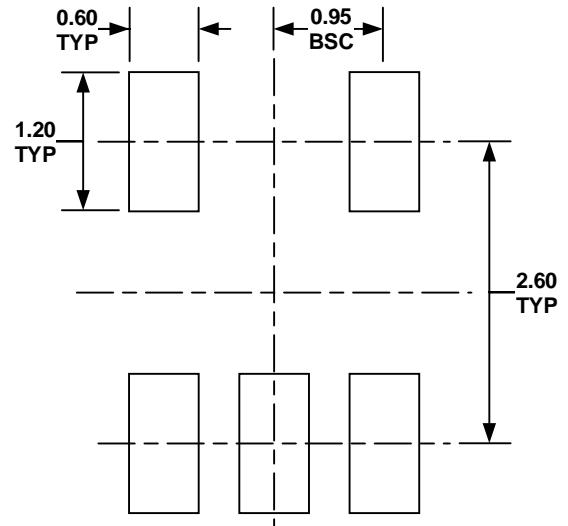
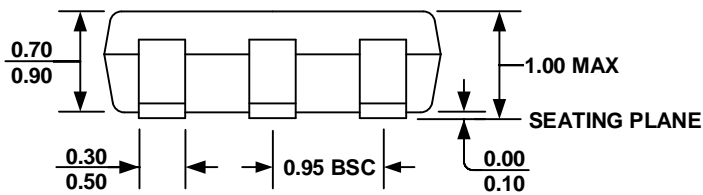
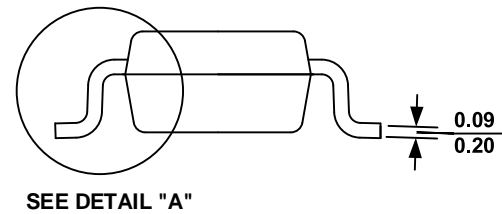
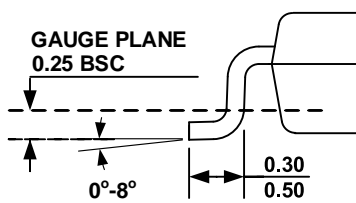


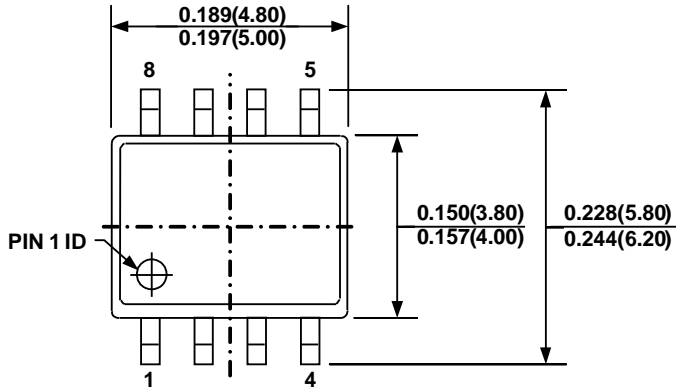
Figure 12: Signal Evolution in the Presence of a Fault

**PACKAGE INFORMATION**
**TSOT23-5**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL "A"**
**NOTE:**

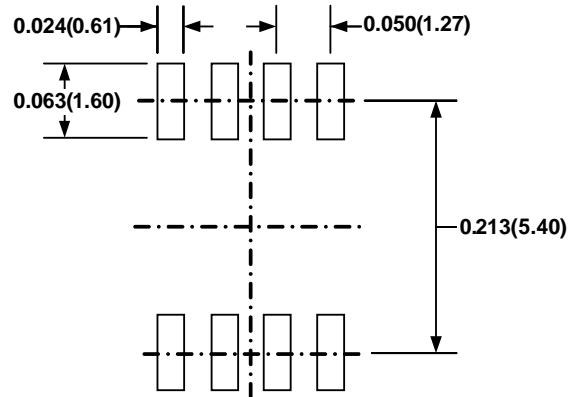
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

## PACKAGE INFORMATION

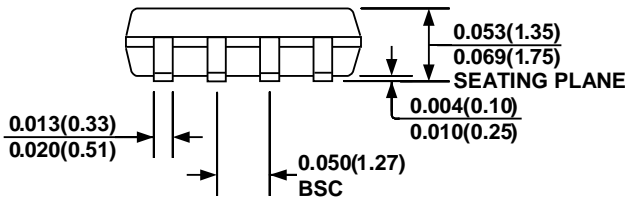
## SOIC-8



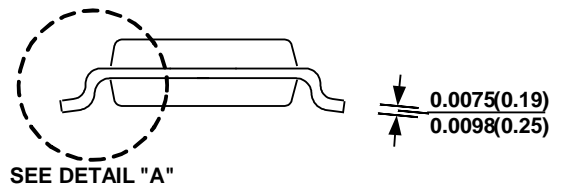
TOP VIEW



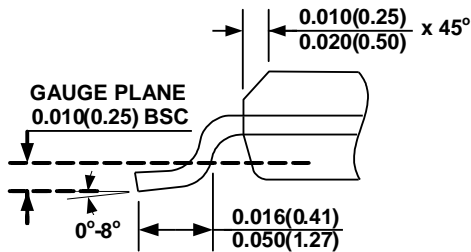
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

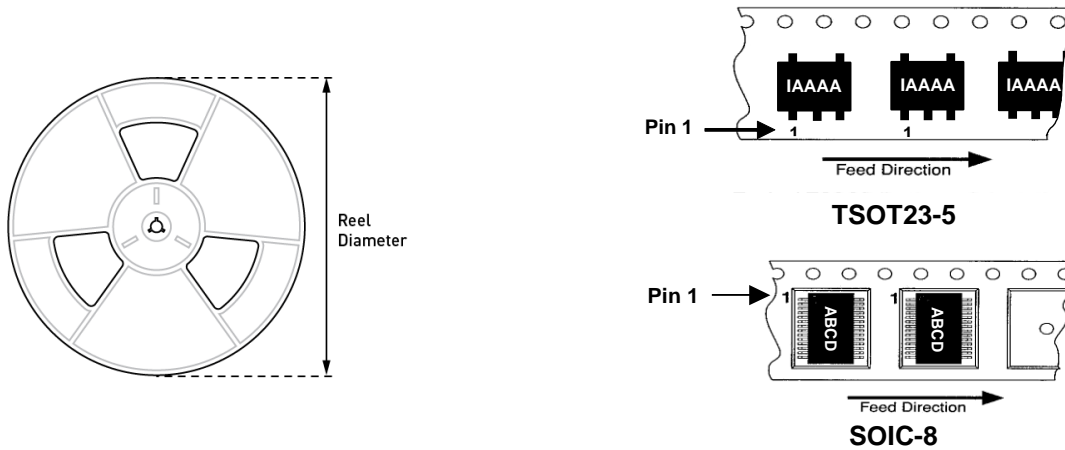


DETAIL "A"

## NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

### CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP172AGJ-Z	TSOT23-5	3000	N/A	7in	8mm	4mm
MP172AGS-Z	SOIC-8	2500	100	13in	12mm	8mm

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