



The Future of Analog IC Technology®

# MP2104

## 1.7MHz, 600mA Synchronous Step-Down Converter

### DESCRIPTION

The MP2104 is a 1.7MHz constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. It is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) battery. The MP2104 can supply 600mA of load current from a 2.5V to 6V input voltage. The output voltage for the MP2104DJ can be regulated as low as 0.6V, while the output voltages of the MP2104DJ-1.5 and MP2104DJ-1.8 are fixed at 1.5V and 1.8V, respectively. The MP2104 can also run at 100% duty cycle for low dropout applications.

The MP2104 is available in low profile (1mm) 5-pin TSOT and 0.75mm TQFN-6 packages.

### ORDERING INFORMATION

Part Number	Output Voltage
MP2104DJ-1.5	$V_{OUT} = 1.5V$
MP2104DJ-1.8	$V_{OUT} = 1.8V$
MP2104DJ	$V_{OUT} = 0.6V \text{ to } 6V$
MP2104DQT	$V_{OUT} = 0.6V \text{ to } 6V$

### EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV2104DJ-00A	2.0"X x 2.0"Y x 0.5"Z

### FEATURES

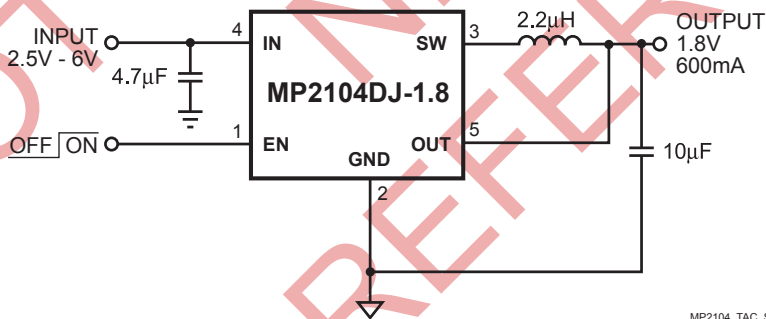
- High Efficiency: Up to 95%
- 1.7MHz Constant Switching Frequency
- 600mA Available Load Current
- 2.5V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Current Mode Control
- Short Circuit Protection
- Thermal Fault Protection
- $<0.1\mu A$  Shutdown Current
- 1.5V and 1.8V Fixed Output Versions
- Space Saving 5-Pin TSOT23 and 6-pin thin QFN Packages

### APPLICATIONS

- Cellular and Smart Phones
- Microprocessors and DSP Core Supplies
- PDAs
- MP3 Players
- Digital Still and Video Cameras
- Portable Instruments

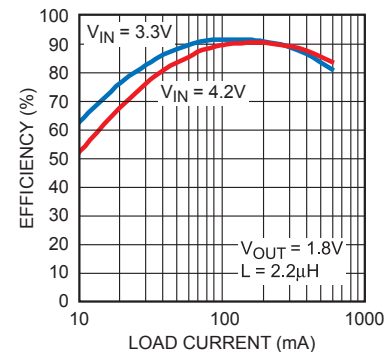
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### TYPICAL APPLICATION



MP2104\_TAC\_S01

#### Efficiency vs Load Current



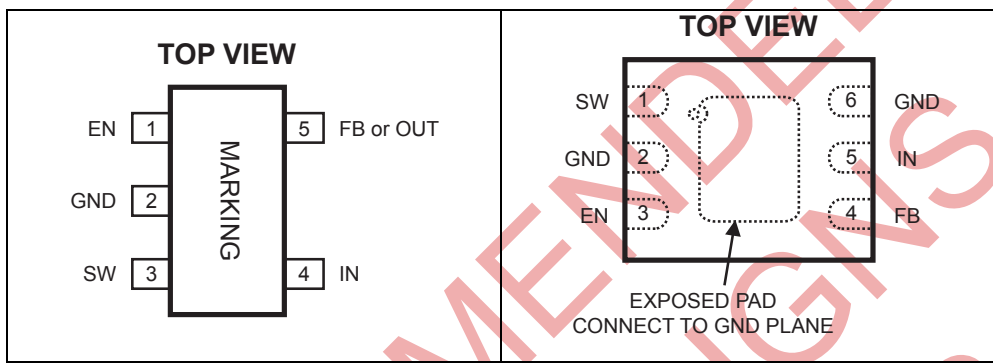
MP2104-EC01

### ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP2104DJ	TSOT23-5	C2	-40°C to +85°C
MP2104DJ-1.5	TSOT23-5	D7	
MP2104DJ-1.8	TSOT23-5	D8	
MP2104DQT	TQFN-6	3A	

\* For Tape & Reel, add suffix -Z (eg. MP2104DJ-Z).  
 For Lead Free, add suffix -LF (eg. MP2104DJ-LF-Z)

### PACKAGE REFERENCE



#### Absolute Maximum Ratings <sup>(1)</sup>

$V_{IN}$ to GND .....	-0.3V to +6.5V
$V_{SW}$ to GND .....	-0.3V to $V_{IN} + 0.3V$
.....	-1.5V to $V_{IN\_MAX} + 1.5V$ for < 50ns
$V_{FB}$ , $V_{EN}$ to GND .....	-0.3V to +6.5V
SW Peak Current .....	1.4A
Continuous Power Dissipation ( $T_A = +25^\circ C$ ) <sup>(2)</sup>	0.57W
Junction Temperature .....	+150°C
Lead Temperature <sup>(3)</sup> .....	+260°C
Storage Temperature .....	-65°C to +150°C

#### Recommended Operating Conditions <sup>(4)</sup>

Supply Voltage $V_{IN}$ .....	2.5V to 6V
Output Voltage $V_{OUT}$ .....	0.6V to 6V
Operating Temperature .....	-40°C to +85°C

Thermal Resistance <sup>(5)</sup>	$\theta_{JA}$	$\theta_{JC}$
TSOT23-5 .....	220	110
TQFN-6 .....	50	12

#### Notes:

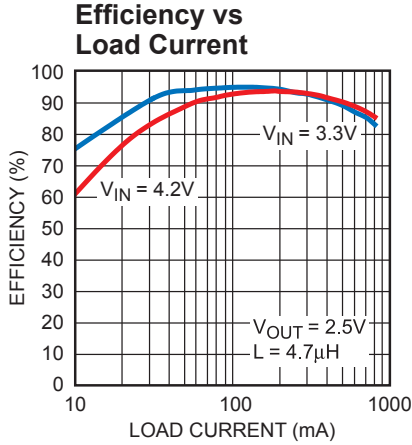
- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature  $T_{J(MAX)}$ , the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- For recommended IR reflow temperature information, refer to MPS document MP2104\_IRRTP.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS <sup>(6)</sup>**
 **$V_{IN} = V_{EN} = 3.6V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.**

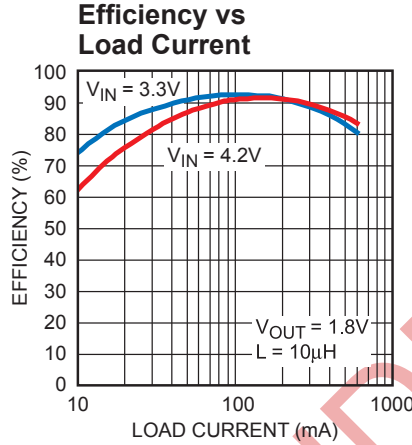
Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current		$V_{EN} = V_{IN}$ , $V_{FB} = 0.65V$		400	600	$\mu A$
Shutdown Current		$V_{EN} = 0V$ , $V_{IN} = 6V$		0.01	1	$\mu A$
IN Under Voltage Lockout Threshold		Rising Edge	2.10	2.27	2.45	V
IN Under Voltage Lockout Hysteresis				55		mV
Regulated FB Voltage		$T_A = +25^{\circ}C$ , MP2104DJ & MP2104DQT	0.588	0.600	0.612	V
		$-40^{\circ}C \leq T_A \leq +85^{\circ}C$	0.582	0.600	0.618	
FB Input Bias Current		$V_{FB} = 0.65V$ , MP2104DJ & MP2104DQT	-50	0.5	+50	nA
Regulated Output Voltage		MP2104DJ-1.5 $I_{OUT} = 50mA$ $-40^{\circ}C \leq T_A \leq +85^{\circ}C$	1.455	1.500	1.545	V
		MP2104DJ-1.8 $I_{OUT} = 50mA$ $-40^{\circ}C \leq T_A \leq +85^{\circ}C$	1.746	1.800	1.854	
PFET On Resistance		$I_{SW} = 100mA$		0.44		$\Omega$
NFET On Resistance		$I_{SW} = -100mA$		0.29		$\Omega$
SW Leakage Current		$V_{EN} = 0V$ , $V_{IN} = 6V$ $V_{SW} = 0V$ or $6V$	-1		+1	$\mu A$
PFET Current Limit		Duty Cycle = 100%, Current Pulse Width < 1ms	0.7	1.0	1.35	A
Oscillator Frequency			1.26	1.70	2.08	MHz
Thermal Shutdown Trip Threshold				145		$^{\circ}C$
EN Trip Threshold		$-40^{\circ}C \leq T_A \leq +85^{\circ}C$	0.3	0.96	1.5	V
EN Input Current		$V_{EN} = 0V$ to $6V$	-1		+1	$\mu A$

**Note:**

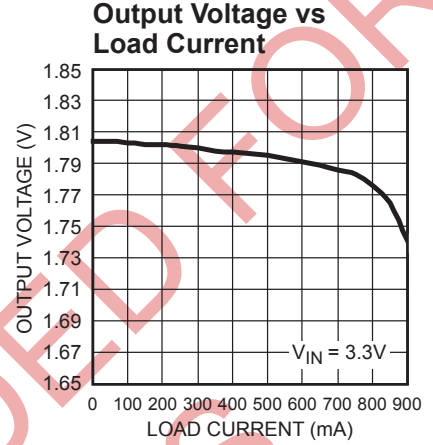
 6) 100% production test at  $+25^{\circ}C$ . Typical and temperature specifications are guaranteed by design and characterization.

**TYPICAL PERFORMANCE CHARACTERISTICS**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  $L1 = 10\mu H$ ,  $C1 = 4.7\mu F$ ,  $C3 = 10\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.


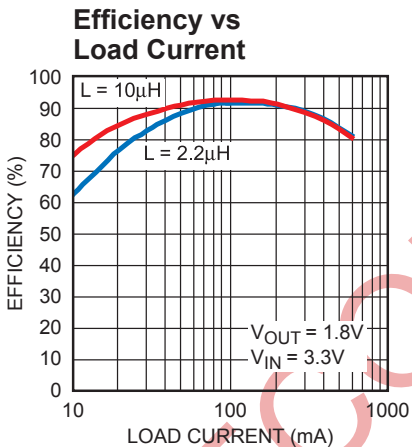
MP2104-TPC01



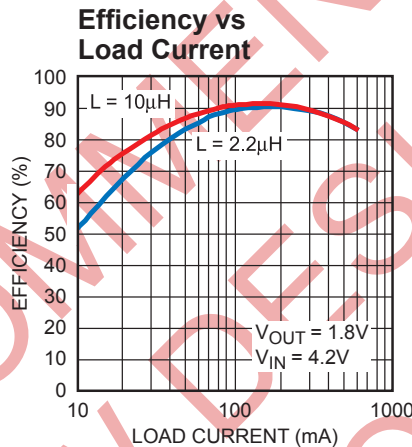
MP2104-TPC02



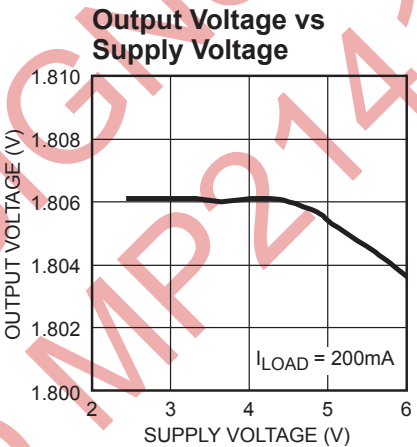
MP2104-TPC05



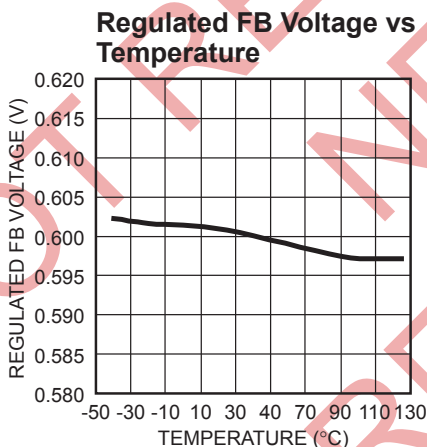
MP2104-TPC03



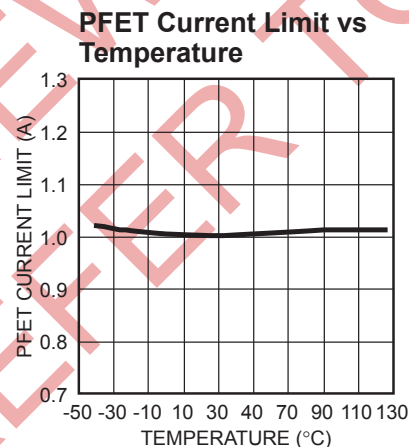
MP2104-TPC04



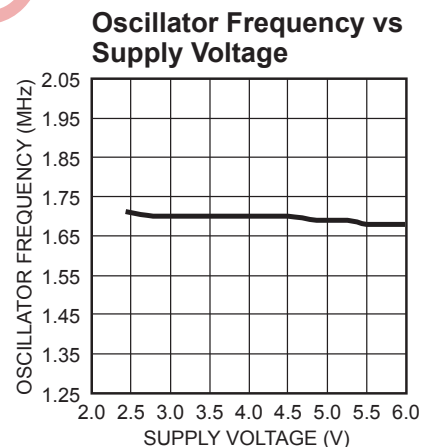
MP2104-TPC06



MP2104-TPC07

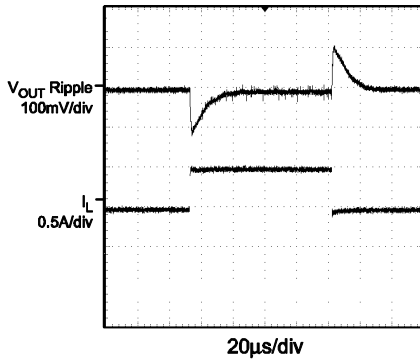


MP2104-TPC08

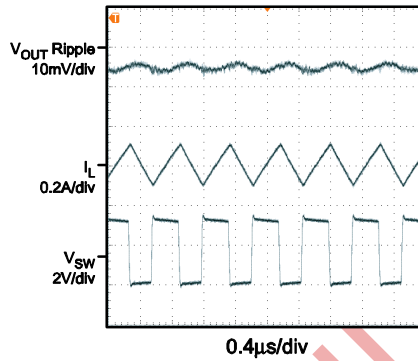


MP2104-TPC09

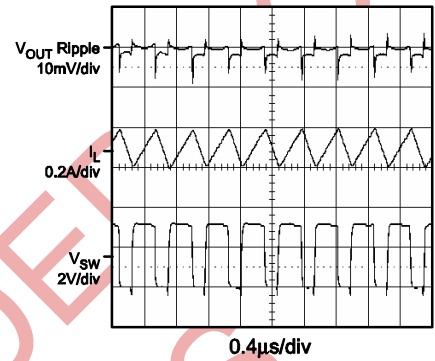
**TYPICAL PERFORMANCE CHARACTERISTICS** *(continued)*
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  $L1 = 10\mu H$ ,  $C1 = 4.7\mu F$ ,  $C3 = 10\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

**Load Transient**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  
 $I_{LOAD} = 0 - 500mA$  Step


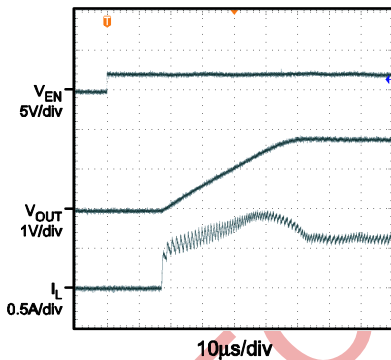
MP2104\_WF01

**Light Load Operation**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  
 $I_{LOAD} = 0A$ 


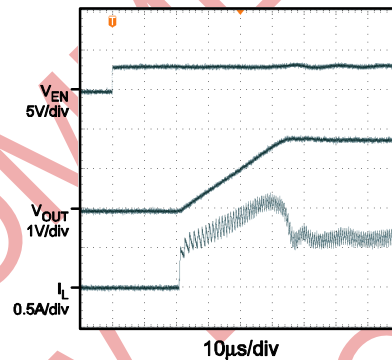
MP2104\_WF02

**Heavy Load Operation**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  
 $I_{LOAD} = 600mA$ 


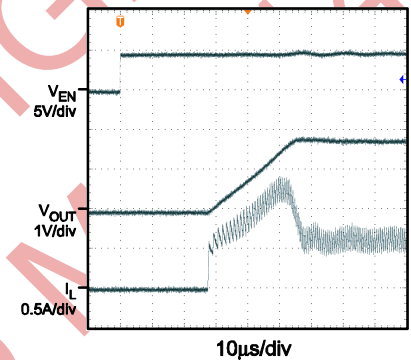
MP2104\_WF03

**Startup from Shutdown**
 $V_{IN} = 2.5V$ ,  $V_{OUT} = 1.8V$ ,  
 $I_{LOAD} = 600mA$  Resistive


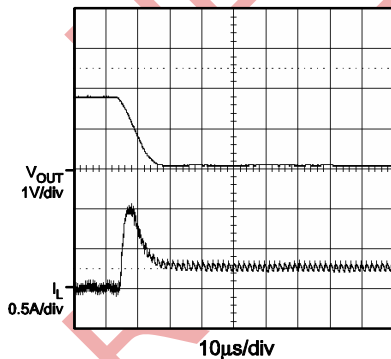
MP2104-WF04

**Startup from Shutdown**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  
 $I_{LOAD} = 600mA$  Resistive


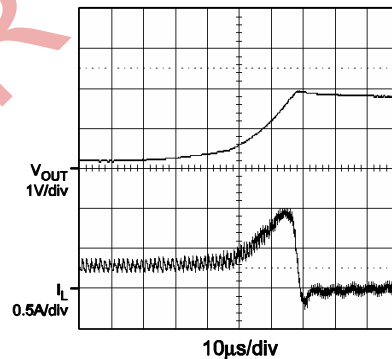
MP2104-WF05

**Startup from Shutdown**
 $V_{IN} = 5V$ ,  $V_{OUT} = 1.8V$ ,  
 $I_{LOAD} = 600mA$  Resistive


MP2104-WF06

**Short Circuit Protection**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  
 No Load


MP2104-WF07

**Short Circuit Recovery**
 $V_{IN} = 3.3V$ ,  $V_{OUT} = 1.8V$ ,  
 No Load


MP2104-WF08

## PIN FUNCTIONS

TSOT23-5 Pin #	TQFN-6 Pin #	Name	Description
1	3	EN	Regulator Enable Control Input. Drive EN above 1.5V to turn on the MP2104. Drive EN below 0.3V to turn it off (shutdown current < 0.1µA).
2	2, 6	GND Exposed Pad	Ground. Connect exposed pad (MP2104DQT) to GND plane for proper thermal performance.
3	1	SW	Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.
4	5	IN	Supply Input. Bypass to GND with a 2.2µF or greater ceramic capacitor.
5	4	FB	Feedback Input (MP2104DJ and MP2104DQT). Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
5	–	OUT	Output Voltage Sense Input (MP2104DJ-1.5 and MP2104DJ-1.8). An internal resistor divider is connected to this pin to set the proper output voltage.

## OPERATION

The MP2104 is a constant frequency current mode PWM step-down converter. The MP2104 is optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical. The MP2104 uses an external resistor divider to set the output voltage from 0.6V to 6V. The device integrates both a main switch and a synchronous rectifier, which provides high efficiency and eliminates

an external Schottky diode. The MP2104 can achieve 100% duty cycle. The duty cycle D of a step-down converter is defined as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where  $T_{ON}$  is the main switch on time,  $f_{OSC}$  is the oscillator frequency (1.7MHz),  $V_{OUT}$  is the output voltage and  $V_{IN}$  is the input voltage.

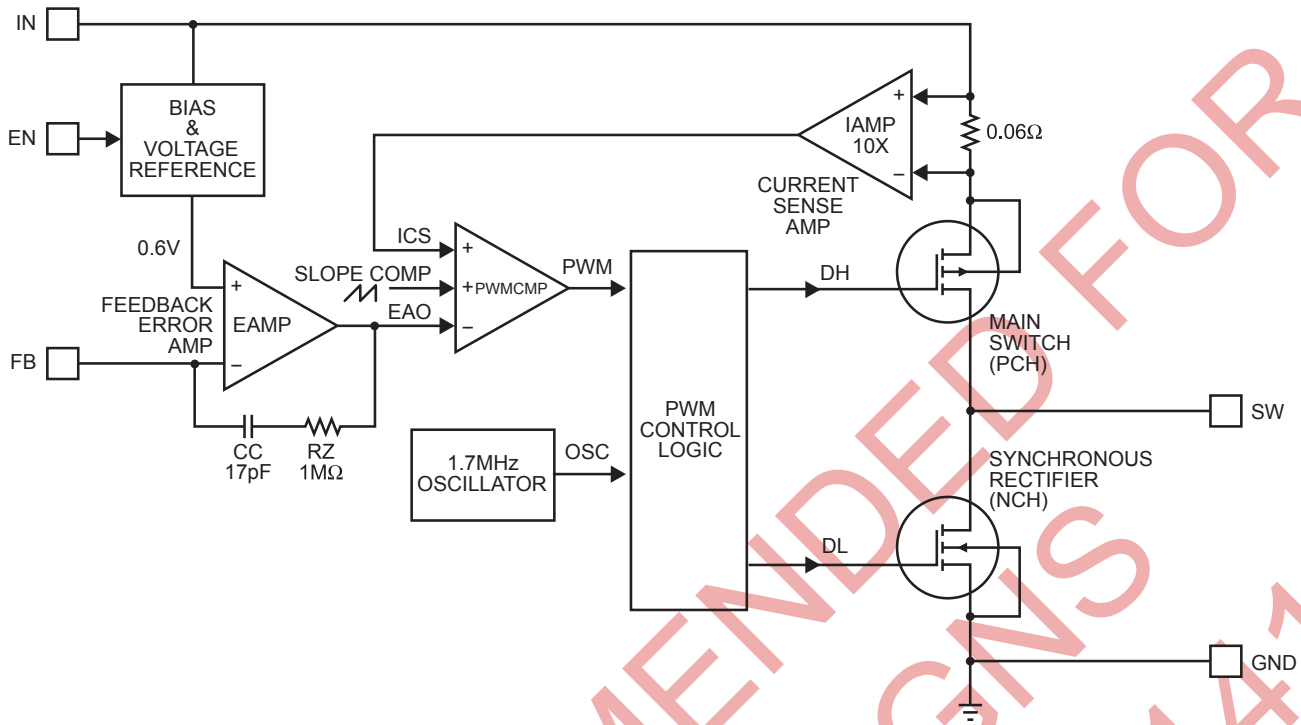
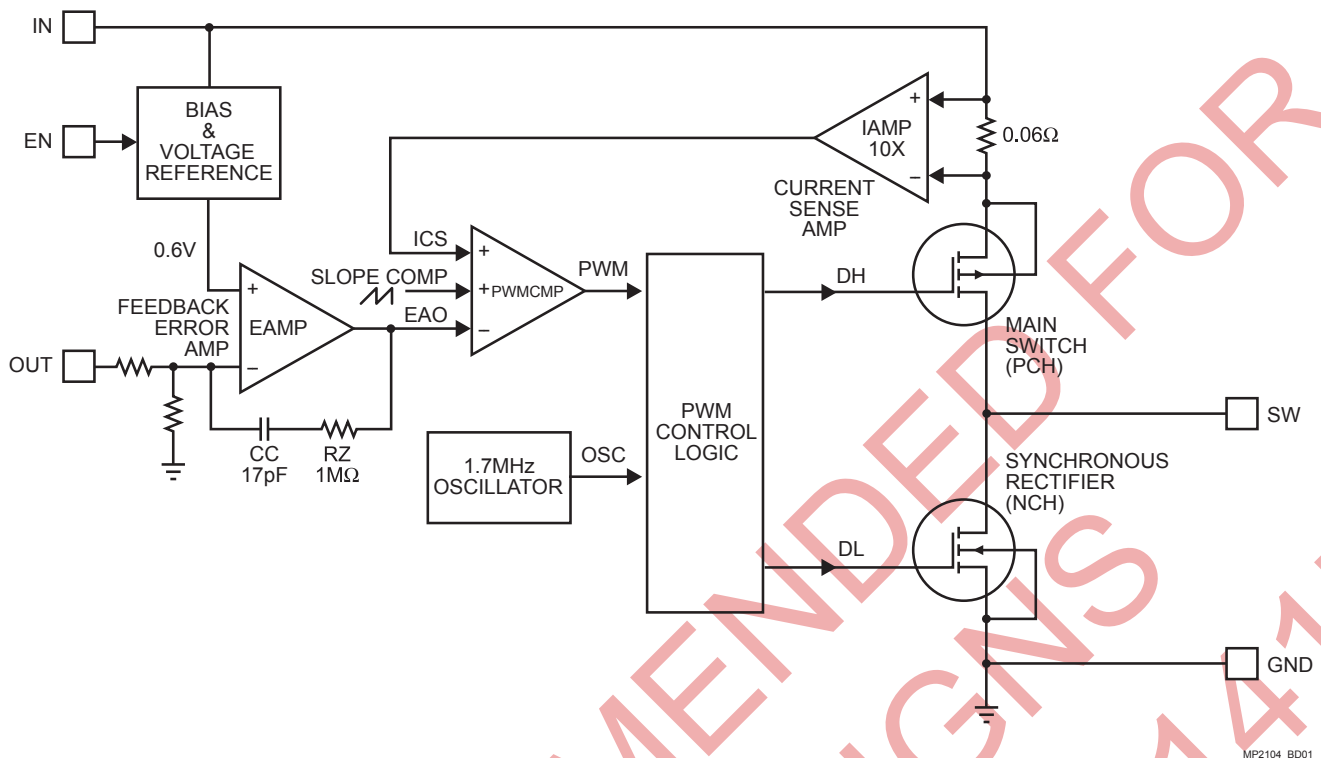


Figure 1—Function Block Diagram (MP2104)

MP2104\_BD01





**Figure 2—Functional Block Diagram (MP2104DJ-1.5 / MP2104DJ-1.8)**

### Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load and line response and protection of the internal main switch and synchronous rectifier. The MP2104 switches at a constant frequency (1.7MHz) and regulates the output voltage. During each cycle the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until either the next cycle starts.

### Dropout Operation

The MP2104 allows the main switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to

the PFET current limit. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor.

### Short Circuit Protection

The MP2104 has short circuit protection. When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

### Maximum Load current

The MP2104 can operate down to 2.5V input voltage, however the maximum load current decreases at lower input due to large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the duty cycle decreases.



## APPLICATION INFORMATION

### Output Voltage Setting (MP2104DJ)

The external resistor divider sets the output voltage (see Figure 3). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1).

Choose R1 around 300kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1}$$

**Table 1—Resistor Selection vs. Output Voltage Setting**

V <sub>OUT</sub>	R1	R2
1.2V	300kΩ (1%)	300kΩ (1%)
1.5V	300kΩ (1%)	200kΩ (1%)
1.8V	300kΩ (1%)	150kΩ (1%)
2.5V	300kΩ (1%)	95.3kΩ (1%)

### Inductor Selection

A 1μH to 10μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <200mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI<sub>L</sub> is the inductor ripple current. Choose inductor ripple current approximately 30% of the maximum load current, 600mA.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency. Table 3 lists inductors recommended for this purpose.

**Table 2—Suggested Surface Mount Inductors**

Manufacturer	Part Number	Inductance (μH)	Max DCR (Ω)	Saturation Current (A)	Dimensions LxWxH (mm <sup>3</sup> )
Coilcraft	LP1704-222M	2.2	0.07	1.7	6.5x5.3x2
Toko	D312C	2.2	0.14	1.0	3.6x3.6x1
Sumida	CDRH3D16	2.2	0.072	1.2	4x4x1.8
Taiyo Yuden	LBC2518	2.2	0.13	0.6	2.5x1.8x1.8

**Table 3—Inductors for Improved Efficiency at 25mA, 50mA, under 100mA Load.**

Manufacturer	Part Number	Inductance (μH)	Max DCR (Ω)	Saturation Current (A)	I <sub>RMS</sub> (A)
Coilcraft	DO1605T-103MX	10	0.3	1.0	0.9
Murata	LQH4C100K04	10	0.2	1.2	0.8
Sumida	CMD4D06-100	10	0.3	0.7	0.5
Sumida	CR32-100	10	0.2	1.0	0.7
Sumida	CR54-100	10	0.1	1.2	1.4

**Input Capacitor Selection**

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 4.7µF capacitor is sufficient.

**Output Capacitor Selection**

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. The output ripple  $\Delta V_{OUT}$  is approximately:

$$\Delta V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{OSC} \times L} \times \left( ESR + \frac{1}{8 \times f_{OSC} \times C3} \right)$$

### PCB layout guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance.

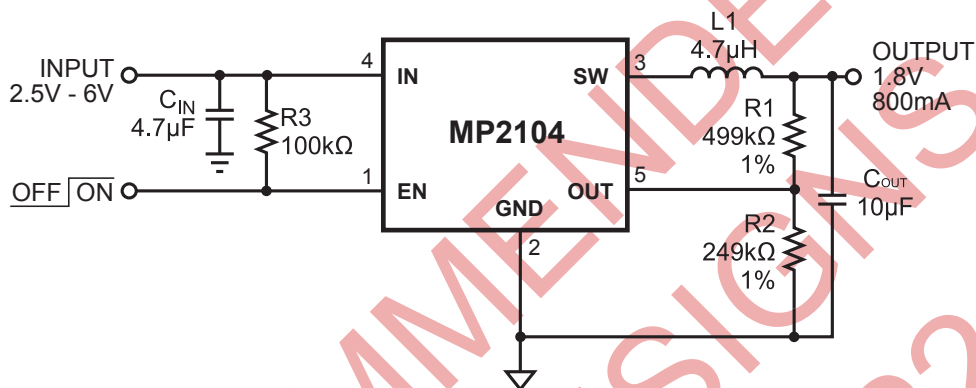
If change is necessary, please follow these guidelines and take figure 3 for reference.

- 1) Keep the path of switching current short and minimize the loop area formed by Input cap, high-side MOSFET and low-side MOSFET.
- 2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.
- 3) Ensure all feedback connections are short

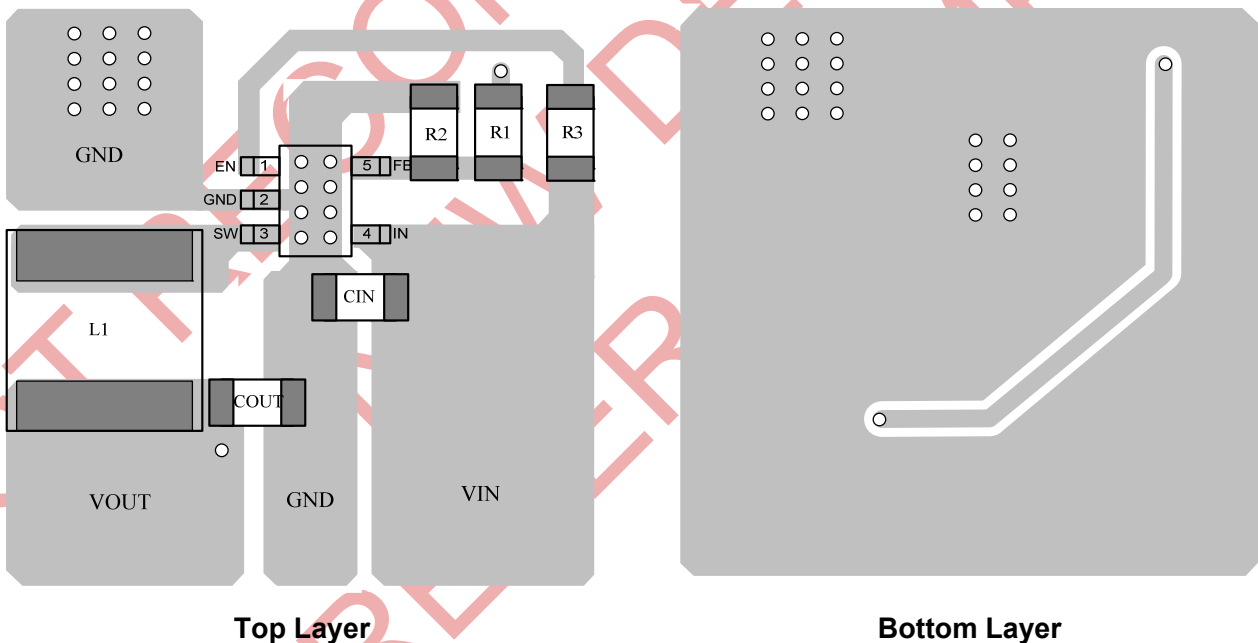
and direct. Place the feedback resistors and compensation components as close to the chip as possible.

- 4) Route SW away from sensitive analog areas such as FB.
- 5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

For the fixed output versions (MP2104DJ-1.5 and MP2104-1.8), R1 is shorted and R2 is open.



**Figure 3 —MP2104 Typical Application Circuit**



**Figure 4—MP2104 Suggested Layout (TQFN)**

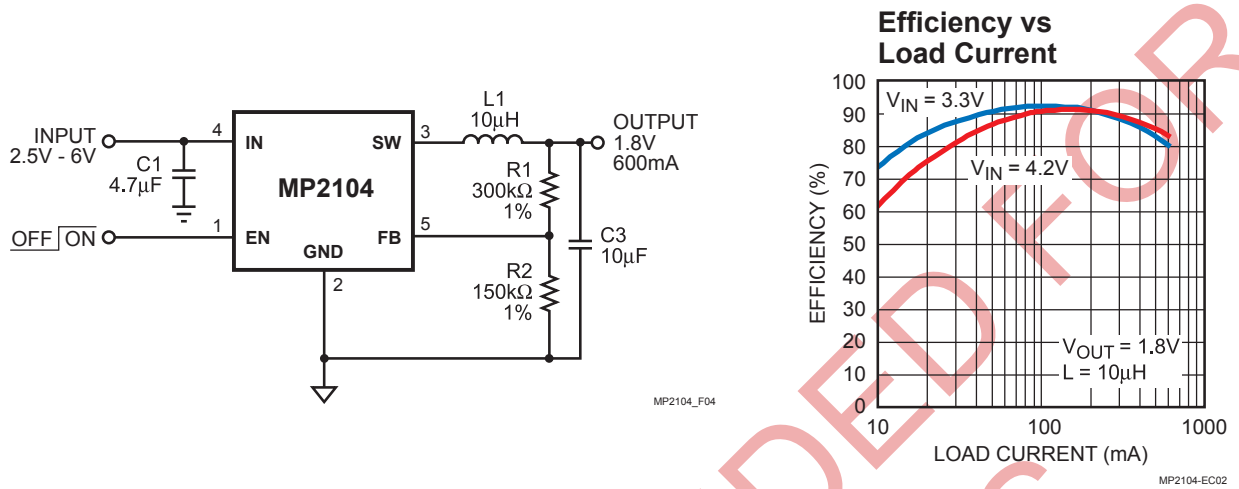
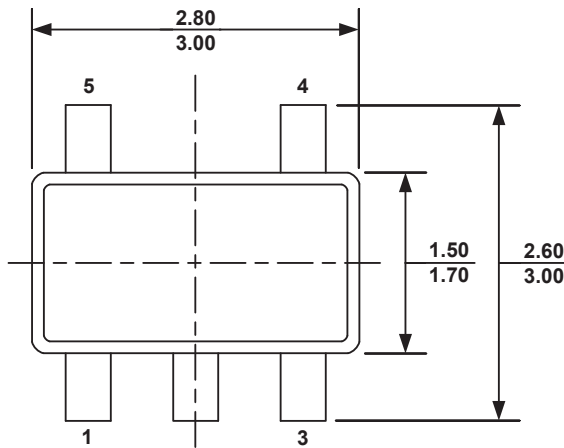
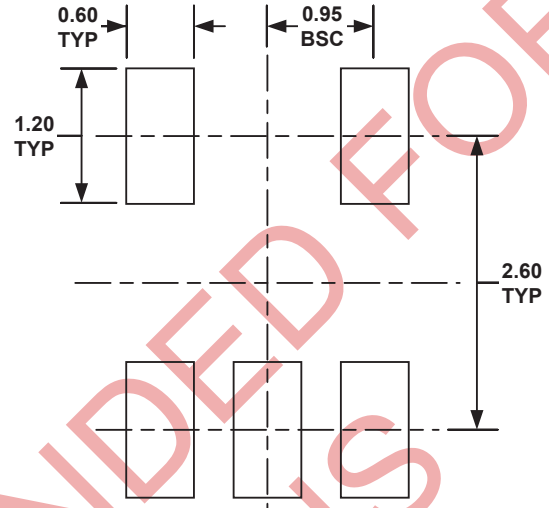
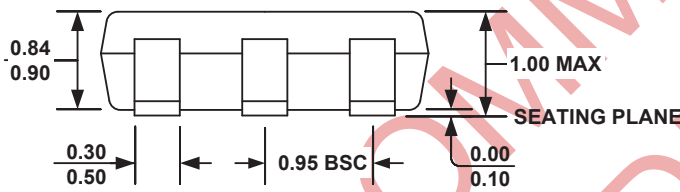
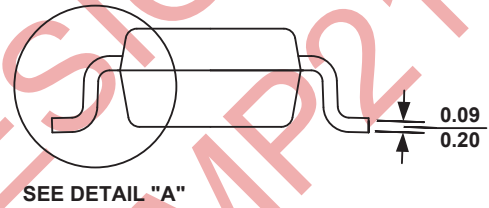
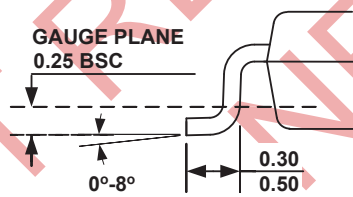
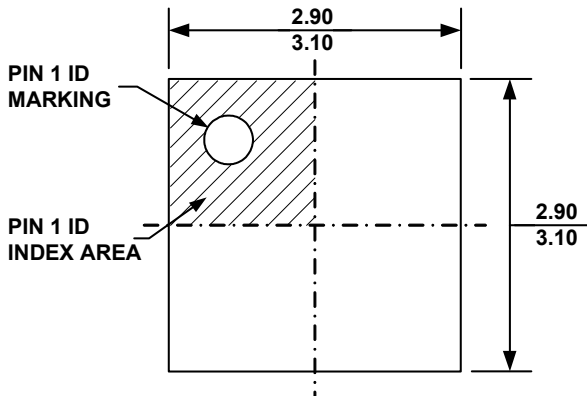
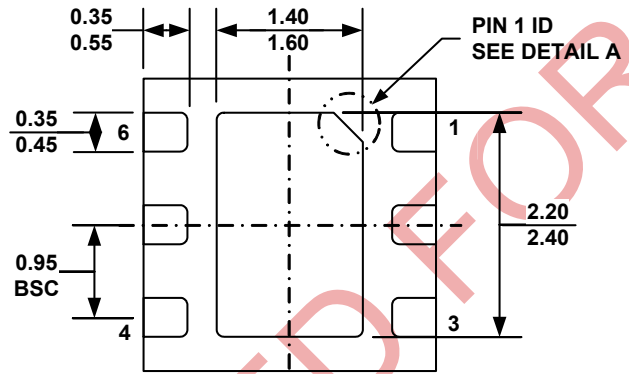
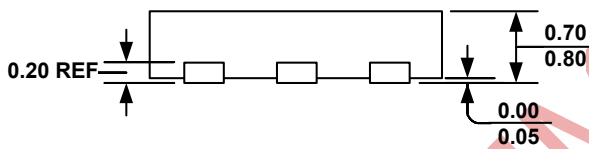


Figure 5—VIN = 2.5V to 6V, VOUT = 1.8V, ILOAD = 600mA Step-Down Circuit (L = 10µH for Higher Light-Load Efficiency)

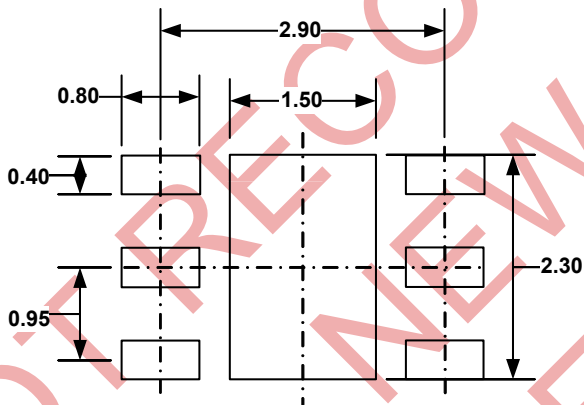
NOT RECOMMENDED FOR NEW DESIGNERS REFER TO MP2141N

**PACKAGE INFORMATION**
**TSOT23-5**

**TOP VIEW**

**RECOMMENDED LAND PATTERN**

**FRONT VIEW**

**SIDE VIEW**

**DETAIL A**
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

**TQFN-6**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**
**PIN 1 ID OPTION A**  
 0.30x45° TYP.

**PIN 1 ID OPTION B**  
 R0.20 TYP.

**DETAIL A**

**RECOMMENDED LAND PATTERN**
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) JEDEC REFERENCE IS MO-229, VARIATION WEEA-2.
- 5) DRAWING IS NOT TO SCALE.

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