

## DESCRIPTION

The MP2162A is a monolithic step-down, switch-mode converter with built-in internal power MOSFETs. It achieves 2A of continuous output current from a 2.5V to 6V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The constant-on-time control scheme provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP2162A is available in small QFN-8 (2.0x1.5mm), TQFN-8 (2.0x1.5mmx0.75mm) and UTQFN-8 (2.0mmx1.5mmx0.55mm) packages and requires only a minimal number of readily available, standard, external components.

The MP2162A is ideal for a wide range of applications, including high performance DSPs, FPGAs, PDAs, and portable instruments.

## FEATURES

- Very Low I<sub>Q</sub> of 17 $\mu$ A
- Default 1.5MHz Switching Frequency
- 1.5% V<sub>FB</sub> Accuracy
- EN and Power Good for Power Sequencing
- Wide 2.5V to 6V Operating Input Range
- Output Adjustable from 0.6V
- Up to 2A of Output Current
- 100% Duty Cycle in Dropout
- 110m $\Omega$  and 60m $\Omega$  Internal Power MOSFET Switches
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- Available in QFN-8 (2.0x1.5mm), TQFN-8 (2.0x1.5mmx0.75mm) and UTQFN-8 (2.0mmx1.5mmx0.55mm) Packages

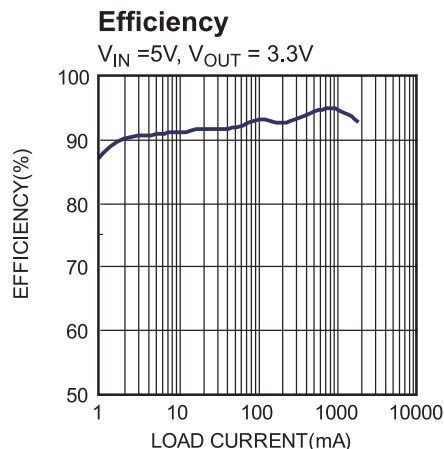
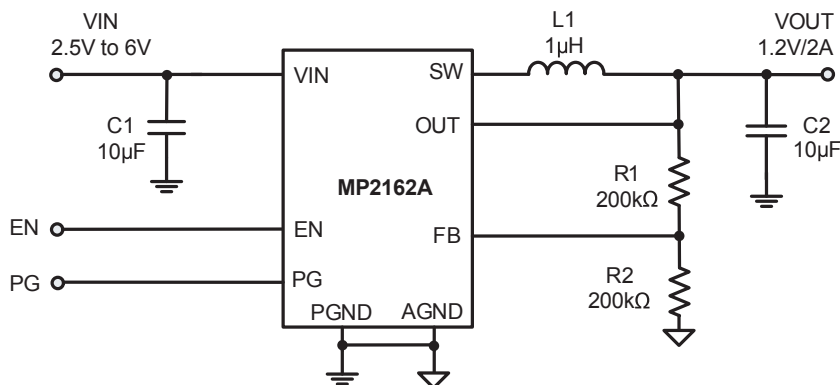
## APPLICATIONS

- Wireless/Networking Cards
- Portable Instruments
- Battery-Powered Devices
- Low Voltage I/O System Power

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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## TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number	Package	Top Marking
MP2162AGQH*	QFN-8 (2.0mmx1.5mm)	<i>See Below</i>
MP2162AGQHT**	TQFN-8 (2.0mmx1.5mmx0.75mm)	<i>See Below</i>
MP2162AGQHU***	UTQFN-8 (2.0mmx1.5mmx0.55mm)	<i>See Below</i>

\*For Tape & Reel, add suffix -Z (e.g. MP2162AGQH-Z)

\*\*For Tape & Reel, add suffix -Z (e.g. MP2162AGQHT-Z)

\*\*\*For Tape & Reel, add suffix -Z (e.g. MP2162AGQHU-Z)

### TOP MARKING

—  
EB  
LL

EB: Product code of MP2162AGQH and MP2162AGQHU

LL: Lot number

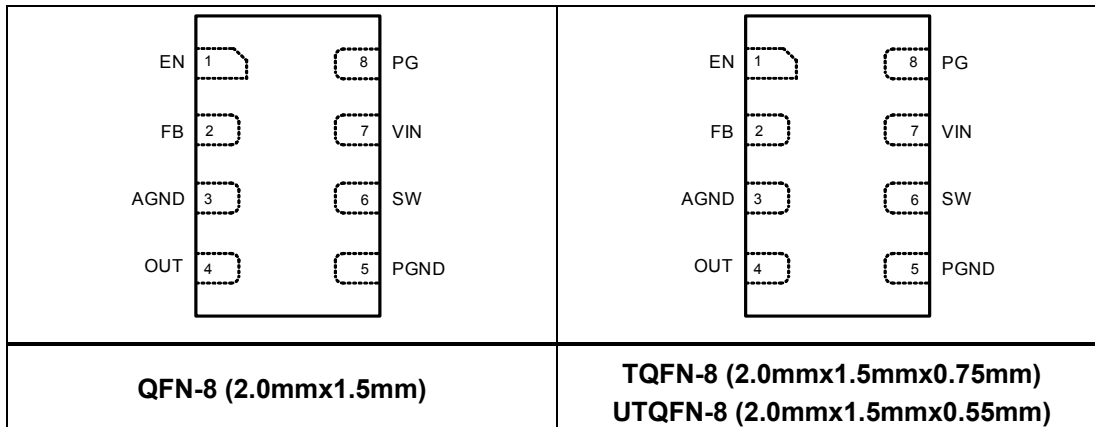
### TOP MARKING

—  
EQ  
LL

EQ: Product code of MP2162AGQHT

LL: Lot number

### PACKAGE REFERENCE



#### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply voltage ( $V_{IN}$ ) .....	6.5V
$V_{SW}$ .....-0.3V (-1.5V for <20ns and -4V for <8ns) to 6.5V (10V for <10ns)	
All other pins .....	-0.3V to 6.5 V
Junction temperature .....	150°C
Lead temperature .....	260°C
Continuous power dissipation ( $T_A = +25^\circ\text{C}$ ) <sup>(2)</sup>	
.....	1.14W
Storage temperature .....	-65°C to +150°C

#### Recommended Operating Conditions <sup>(3)</sup>

Supply voltage ( $V_{IN}$ ) .....	2.5V to 6V
Operating junction temp. ( $T_J$ )...	-40°C to +125°C

#### Thermal Resistance <sup>(4)</sup>      $\theta_{JA}$   $\theta_{JC}$

QFN-8 (2.0mmx1.5mm) .....	110 .. 55... °C/W
TQFN-8 (2.0mmx1.5mmx0.75mm).....	110 .. 55... °C/W
UTQFN-8 (2.0mmx1.5mmx0.55mm).....	110 55... °C/W

#### NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX)- $T_A$ )/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$ ,  $T_A = +25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback voltage	$V_{FB}$	$2.5V \leq V_{IN} \leq 6V$ , $T_A = 25^{\circ}C$	-1.5	0.600	+1.5	V/%
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ <sup>(6)</sup>	-2.5		+2.5	
Feedback current	$I_{FB}$	$V_{FB} = 0.6V$		10	50	nA
PFET switch-on resistance	$R_{DSON\_P}$			110		m $\Omega$
NFET switch-on resistance	$R_{DSON\_N}$			60		m $\Omega$
Switch leakage		$V_{EN} = 0V$ , $V_{IN} = 6V$ $V_{SW} = 0V$ and $6V$		0	1	$\mu A$
PFET current limit			2.6	3.2	4.0	A
On time	$T_{ON}$	$V_{IN} = 5V$ , $V_{OUT} = 1.2V$		166		ns
		$V_{IN} = 3.6V$ , $V_{OUT} = 1.2V$		220		
Switching frequency	$F_s$	$V_{OUT} = 1.2V$ , $T_A = 25^{\circ}C$	-20	1500	+20	kHz/%
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ <sup>(6)</sup>	-25	1500	+25	
Minimum off time <sup>(6)</sup>	$T_{MIN-OFF}$			60		ns
Soft-start time	$T_{SS-ON}$	$V_{OUT}$ from 10% to 90%	0.6	1.15	1.7	ms
Power good upper trip threshold	$PG_H$	FB voltage with respect to the regulation		+10		%
Power good lower trip threshold	$PG_L$			-10		%
Power good delay	$PG_D$			50		$\mu s$
Power good sink current capability	$V_{PG-L}$	Sink 1mA			0.4	V
Power good logic high voltage	$V_{PG-H}$	$V_{IN} = 5V$ , $V_{FB} = 0.6V$	4.9			V
Power good internal pull-up resistor	$R_{PG}$			550		k $\Omega$
Under-voltage lockout threshold rising			2.15	2.3	2.45	V
Under-voltage lockout threshold hysteresis				260		mV
EN input logic low voltage					0.4	V
EN input logic high voltage			1.2			V
EN input current		$V_{EN} = 2V$		1.5		$\mu A$
		$V_{EN} = 0V$		0		$\mu A$
Supply current (shutdown)		$V_{EN} = 0V$ , $V_{IN} = 3V$		20	100	nA
Supply current (quiescent)		$V_{EN} = 2V$ , $V_{FB} = 0.63V$ , $V_{IN} = 5V$		17	20	$\mu A$
Thermal shutdown <sup>(5)</sup>				150		$^{\circ}C$
Thermal hysteresis <sup>(5)</sup>				30		$^{\circ}C$

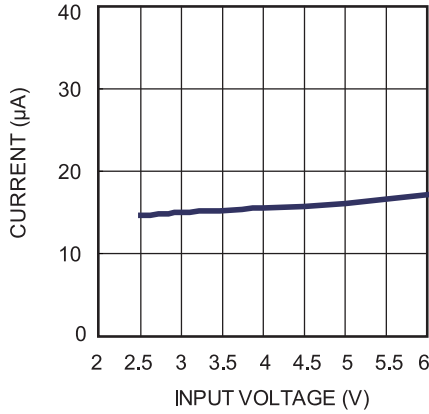
### NOTES:

- 5) Guaranteed by design.  
6) Guaranteed by characterization test.

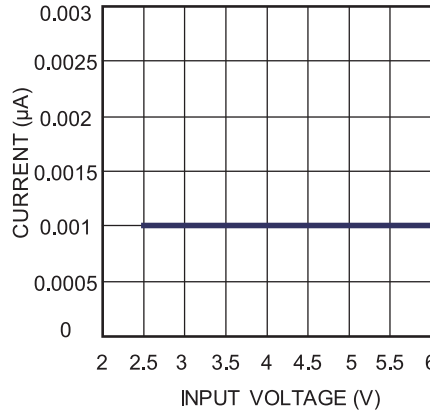
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1.0\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

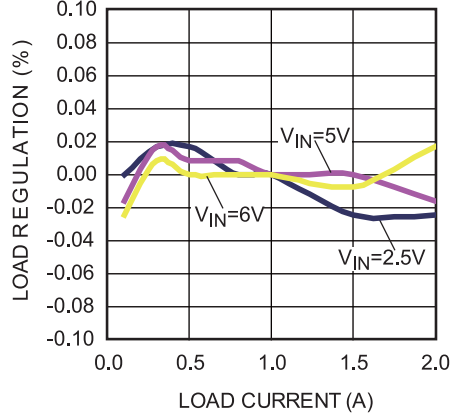
**Quiescent Current vs. Input Voltage**



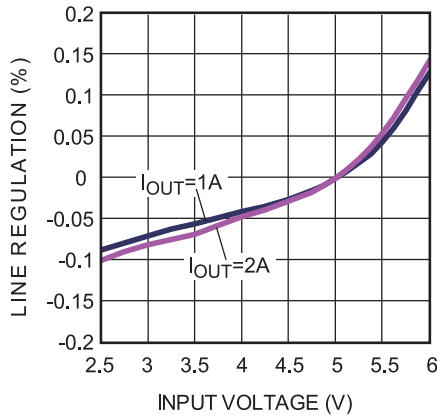
**Shutdown Current vs. Input Voltage**



**Load Regulation**

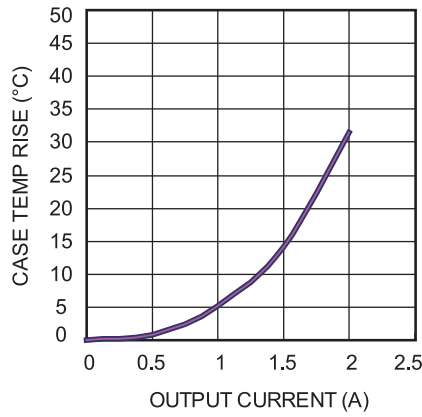


**Line Regulation**



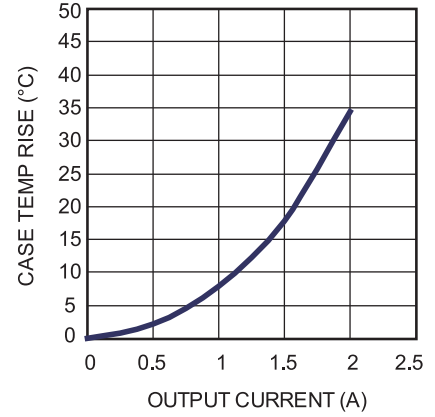
**Case Temperature Rise**

$V_{IN} = 3V$ ,  $V_{OUT} = 1.2V$

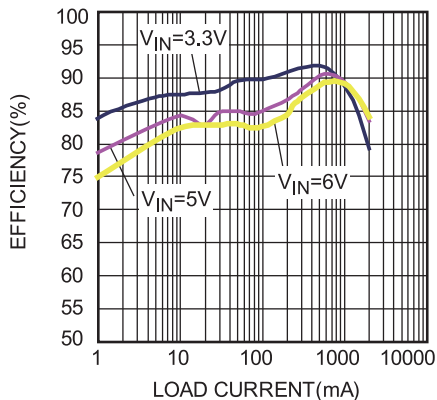


**Case Temperature Rise**

$V_{IN} = 5V$ ,  $V_{OUT} = 3.3V$

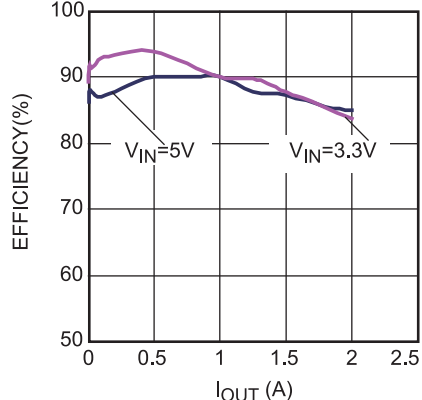


**Efficiency**



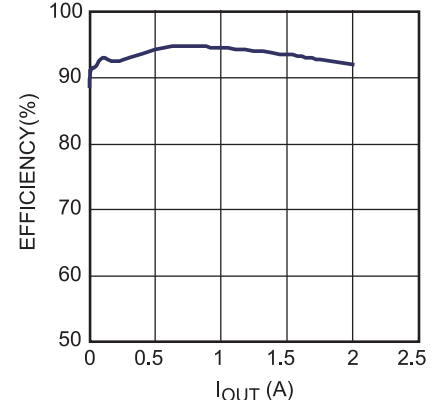
**Efficiency**

$5V/3.3V$   $V_{IN}$ ,  $1.8V$   $V_{OUT}$



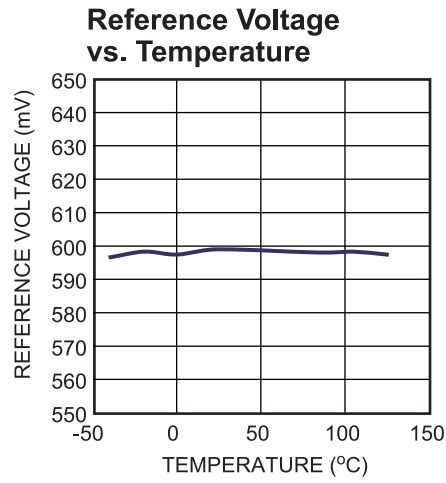
**Efficiency**

$5V$   $V_{IN}$ ,  $3.3V$   $V_{OUT}$

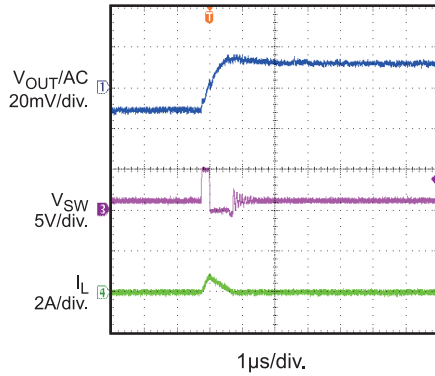
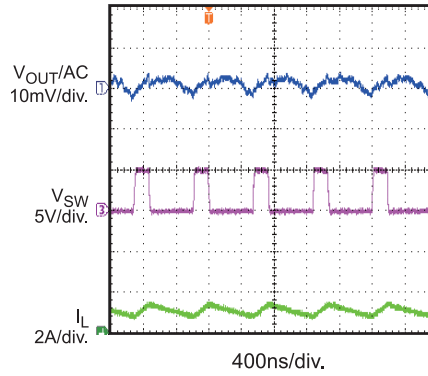
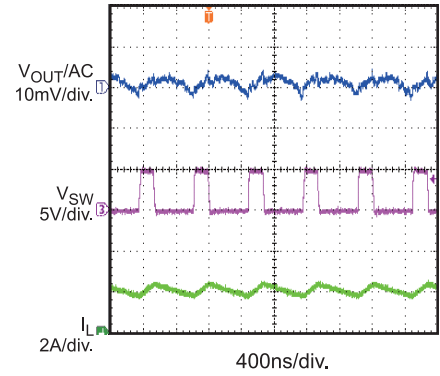
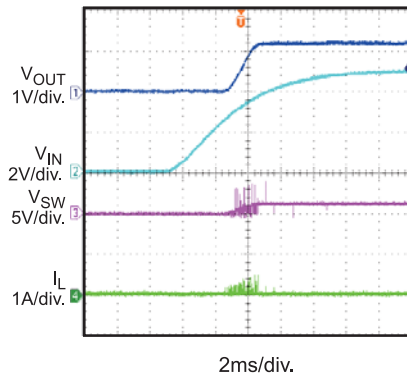
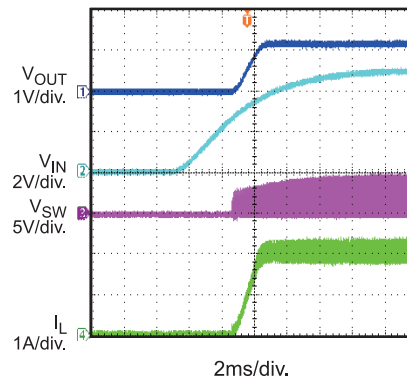
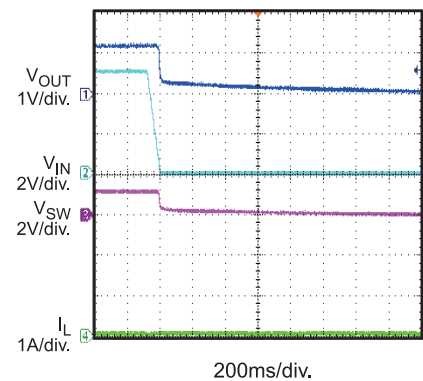
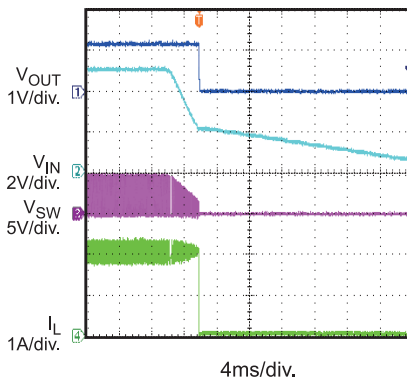
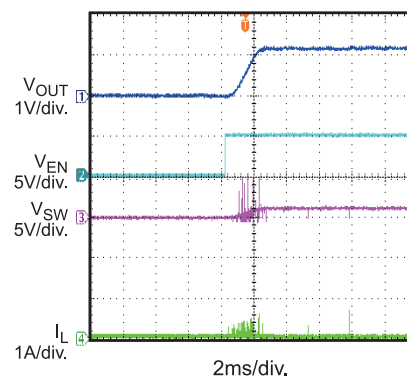
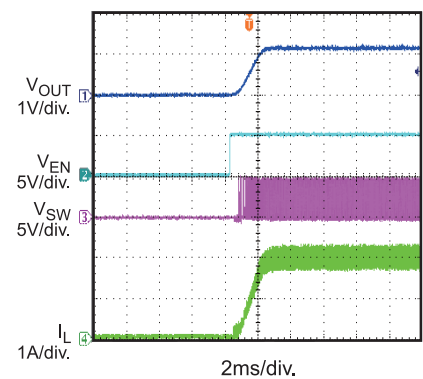


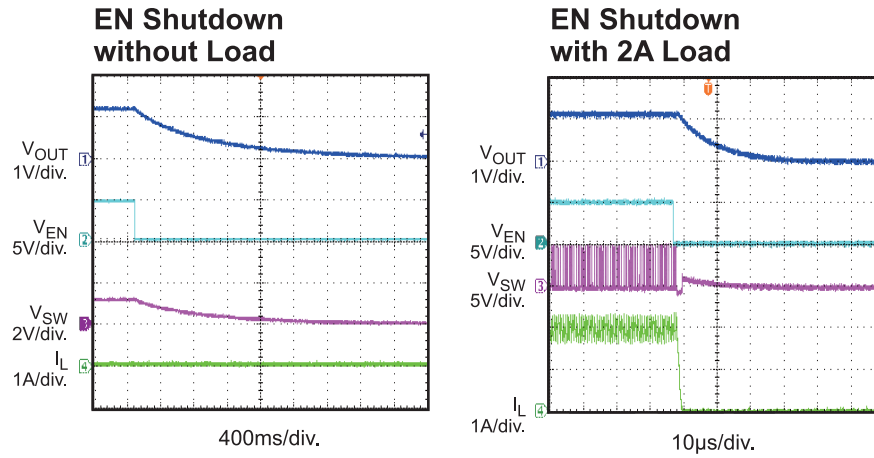
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

$V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1.0\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0\mu H, T_A = +25^\circ C$ , unless otherwise noted.

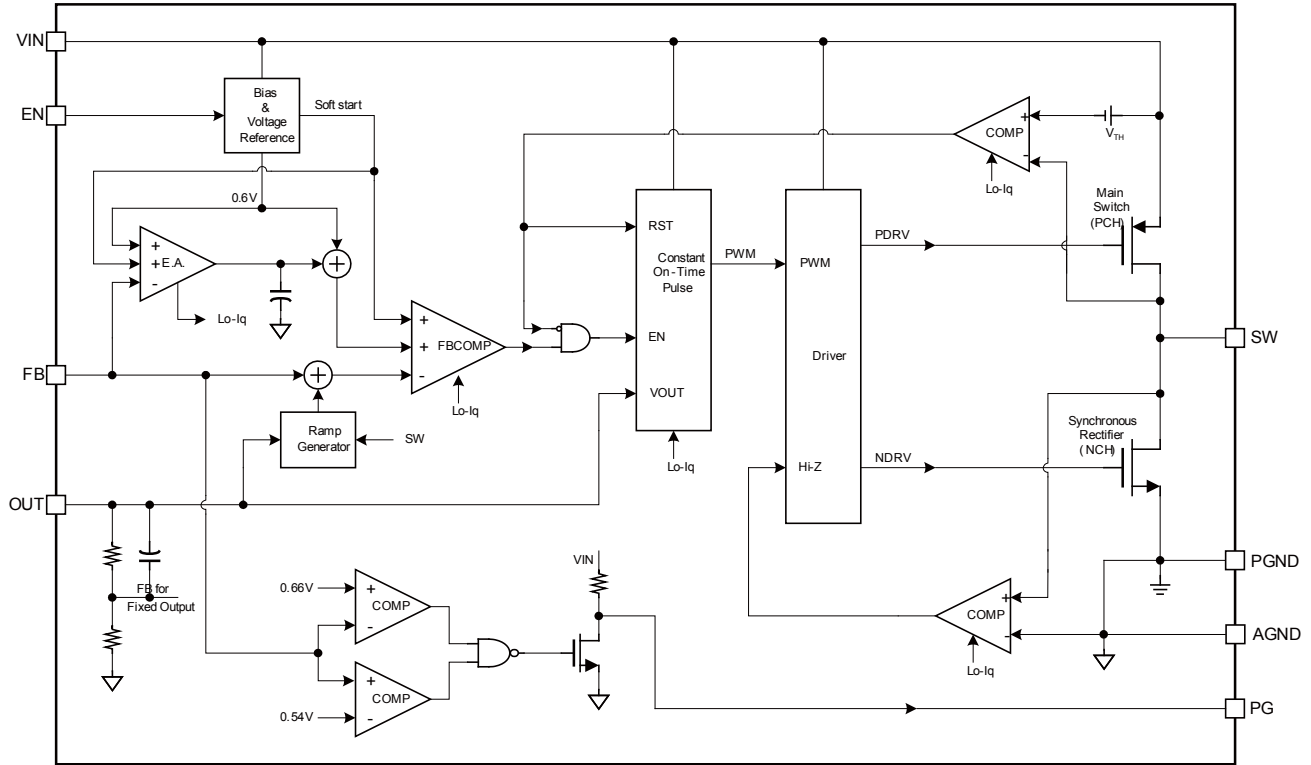
**Output Ripple**
 $I_{OUT}=0A$ 

**Output Ripple**
 $I_{OUT}=1A$ 

**Output Ripple**
 $I_{OUT}=2A$ 

**VIN Power-Up without Load**

**VIN Power-Up with 2A Load**

**VIN Shutdown without Load**

**VIN Shutdown with 2A Load**

**EN Start-Up without Load**

**EN Start-Up with 2A Load**


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 5V$ ,  $V_{OUT} = 1.2V$ ,  $L = 1.0\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.




**PIN FUNCTIONS**

Pin # (QFN-8)	Pin # (TQFN-8) (UTQFN-8)	Name	Description
1	1	EN	<b>On/off control.</b>
2	2	FB	<b>Feedback.</b> An external resistor divider from the output to AGND (tapped to FB) sets the output voltage.
3	3	AGND	<b>Analog ground for the internal control circuit.</b>
4	4	OUT	<b>Input sense for output voltage.</b>
5	5	PGND	<b>Power ground.</b>
6	6	SW	<b>Switch output.</b>
7	7	VIN	<b>Supply voltage.</b> The MP2162A operates from a +2.5V to +6V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
8	8	PG	<b>Power good indicator.</b> The output of PG is an open drain with an internal pull-up resistor to VIN. PG is pulled up to VIN when the FB voltage is within $\pm 10\%$ of the regulation level. If the FB voltage is out of that regulation range, it is low.

**FUNCTIONAL BLOCK DIAGRAM**

**Figure 1: The MP2162A Block Diagram**

## OPERATION

The MP2162A uses constant-on-time control with an input voltage feed-forward to stabilize the switching frequency over a full input voltage range. During light loads, the MP2162A employs proprietary control of the low-side switches and inductor currents to eliminate ringing on the switching node and improve efficiency.

### Constant-On-Time Control

Compared to the fixed frequency PWM control, the constant-on-time control offers the advantage of a simpler control loop and a faster transient response. By using input voltage feed-forward, the MP2162A maintains a near constant switching frequency across the input and output voltage ranges. The on time of the switching pulse can be estimated with Equation (1):

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.667\mu s \quad (1)$$

To prevent inductor current runaway during the load transient, the MP2162A has a fixed minimum off time of 60ns. However, this minimum off time limit does not affect the operation of the MP2162A in its steady state in any way.

### Light-Load Operation

In light-load conditions, the MP2162A uses a proprietary control scheme to save power and improve efficiency. The MP2162A uses a zero current cross circuit to detect if the inductor current is starting to reverse. The low-side switch turns off when the inductor current starts to reverse and then begins working in discontinuous conduction mode (DCM).

The delay for the internal circuit propagation time is typically 50ns. This means that the inductor current continues falling after the ZCD is triggered in this delay. If the inductor current falling slew rate is fast ( $V_{OUT}$  is high or close to  $V_{IN}$ ), then the low-side MOSFET turns off, the inductor current may be negative, and the MP2162A will not be able to enter DCM operation. If DCM mode is required, the off time of the low-side MOSFET in CCM should be longer than 100ns (2x the propagation delay).

For example, if  $V_{IN}$  is 3.6V and  $V_o$  is 3.3V, the off time in CCM is 55ns. It is difficult to enter DCM at a light load. Using a smaller inductor can help the MP2162A enter DCM more easily.

### Enable (EN)

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 2.3V), the MP2162A is enabled by pulling EN higher than 1.2V. Leaving EN floating or grounded disables the MP2162A. There is an internal 1M $\Omega$  resistor from EN to ground.

### Soft Start

The MP2162A has a built-in soft start that ramps up the output voltage at a controlled slew rate to avoid overshooting at start-up. The soft-start time is typically about 1.15ms.

### Power Good Indicator

The MP2162A uses an open drain with a 550k $\Omega$  pull-up resistor as a power good indicator (PG). When the FB voltage is within +/-10% of the regulation voltage (i.e. 0.6V), PG is pulled up to  $V_{IN}$  by an internal resistor. If the FB voltage is out of the +/-10% window, PG is pulled down to ground by an internal MOSFET. The MOSFET has a maximum  $R_{ds(on)}$  of less than 400 $\Omega$ .

### Current Limit

The MP2162A has a typical 3.2A current limit for the high-side switch. When the high-side switch hits its current limit, the MP2162A enters hiccup mode until the current drops. This prevents the inductor current from rising and possibly damaging the components.

### Short Circuit and Recovery

The MP2162A enters short-circuit protection mode when the current limit is hit; it tries to recover from the short circuit by entering hiccup mode. In short-circuit protection, the MP2162A disables the output power stage, discharges a soft-start capacitor, and automatically tries to soft start. If the short-circuit condition still holds after the soft start ends, the MP2162A repeats this operation until the short circuit disappears, and the output rises back to regulation levels.

## APPLICATION INFORMATION

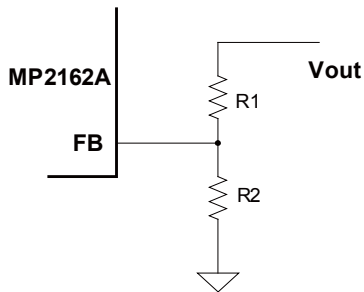
### COMPONENT SELECTION

#### Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). The feedback resistor R1 cannot be too large or too small, considering the trade-off between a dynamic circuit and stability in the circuit. Set R1 to around 120kΩ to 200kΩ. R2 is then given by Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown in Figure 2.



**Figure 2: Feedback Network**

Table 1 lists the recommended resistor values for common output voltages.

**Table 1: Resistor Selection for Common Output Voltages**

V <sub>OUT</sub> (V)	R1 (kΩ)	R2 (kΩ)
1.0	200 (1%)	300 (1%)
1.2	200 (1%)	200 (1%)
1.8	200 (1%)	100 (1%)
2.5	200 (1%)	63.2 (1%)
3.3	200 (1%)	44.2 (1%)

#### Selecting the Inductor

A 0.68μH to 2.2μH inductor is recommended for most applications. For the highest efficiency, choose an inductor with a DC resistance of less than 15mΩ. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI<sub>L</sub> is the inductor ripple current.

Set the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is calculated in Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

#### Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For a higher output voltage, a 47μF capacitor may be needed to improve system stability.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worse case condition occurs at V<sub>IN</sub> = 2V<sub>OUT</sub>, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (i.e. 0.1μF) and place it as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide a sufficient enough charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

### Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated by Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right) \quad (8)$$

Where  $L_1$  is the inductor value and  $R_{ESR}$  is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, which mainly causes output voltage ripples. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

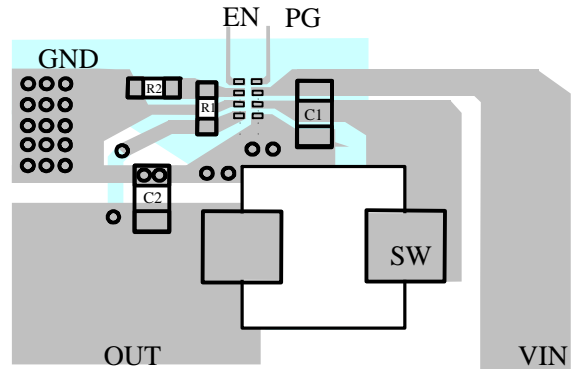
The characteristics of the output capacitor affect the stability of the regulation system.

### PCB Layout Guidelines

Efficient PCB layout is critical for achieving stable operation. A poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 3 and follow the guidelines below:

1. Place the high-current paths (GND, VIN, and SW) as close to the device as possible with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.

3. Place the external feedback resistors next to FB.
4. Keep the switching node (SW) short and away from the feedback network.



**Figure 3: PCB Layout Recommendation**

### Design Example

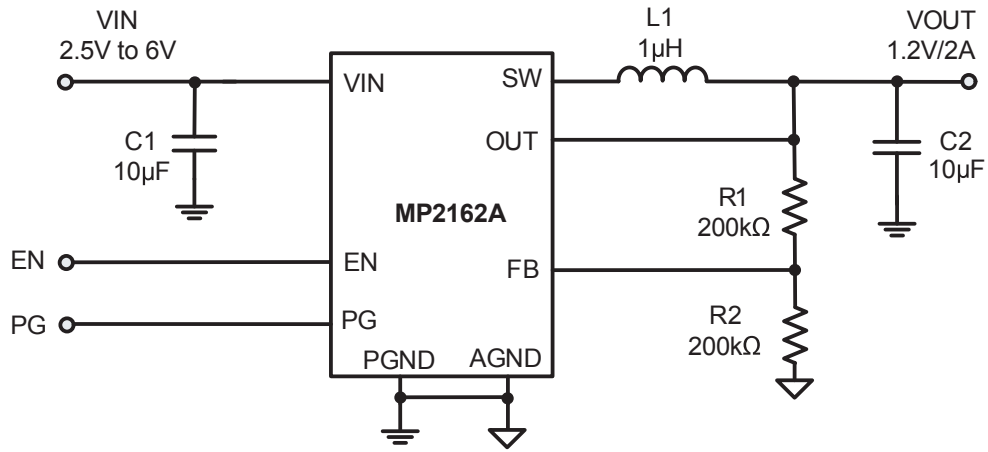
Below is a design example following the application guidelines for the specifications below:

**Table 2: Design Example**

$V_{IN}$	5V
$V_{OUT}$	1.2V
$f_{sw}$	1500kHz

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 5. For more device applications, please refer to the related evaluation board datasheets.

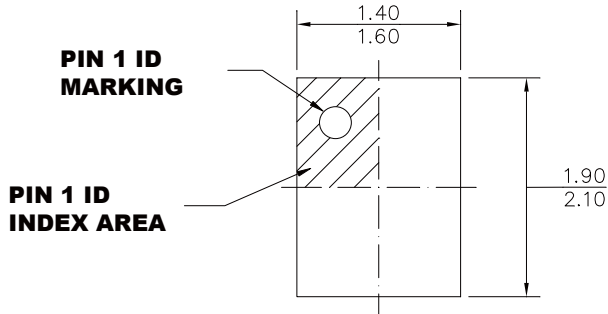
**TYPICAL APPLICATION CIRCUITS**



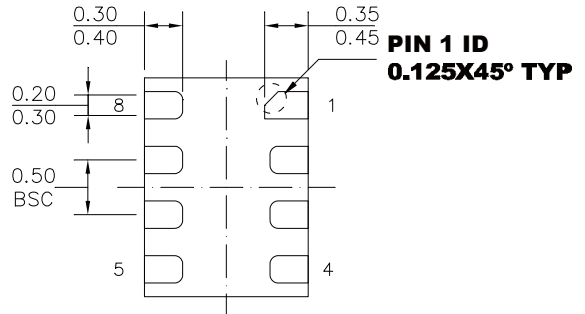
**Figure 4: Typical Application Circuit**

**PACKAGE INFORMATION**

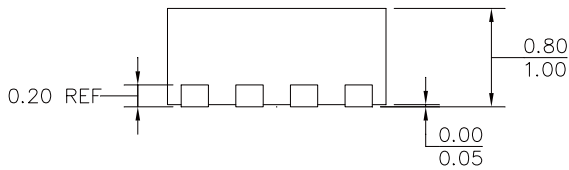
**QFN-8 (2.0mmx1.5mm)**



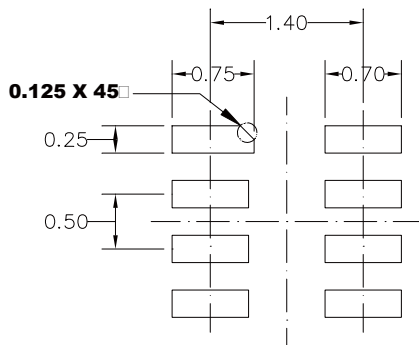
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**

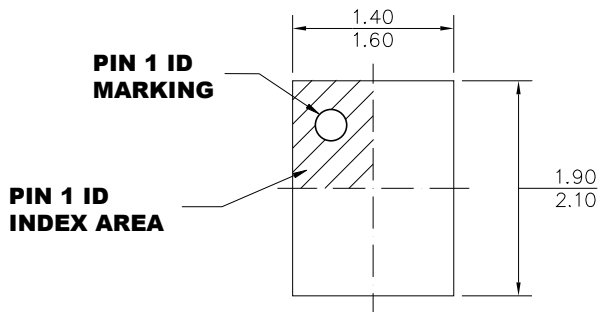


**RECOMMENDED LAND PATTERN**

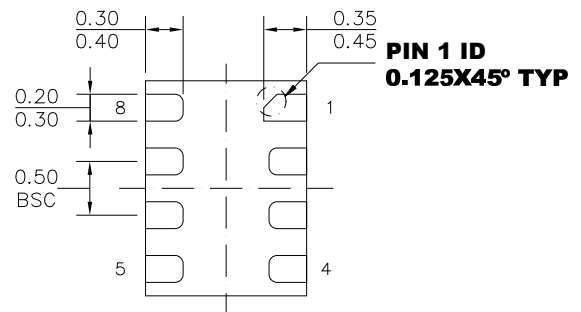
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.

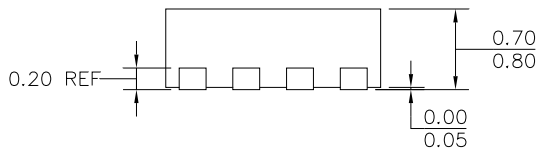
**TQFN-8 (2.0mmx1.5mmx0.75mm)**



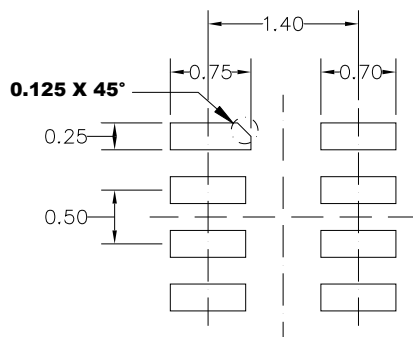
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



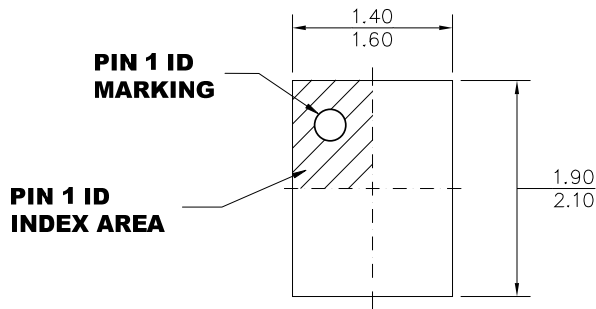
**RECOMMENDED LAND PATTERN**

**NOTE:**

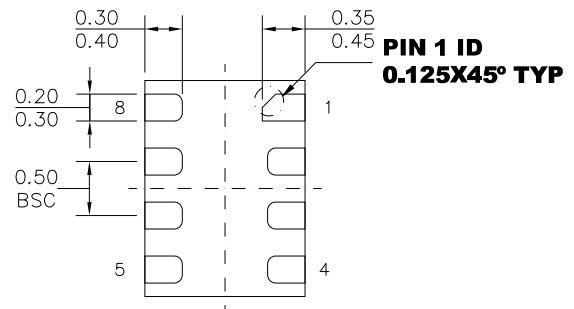
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.



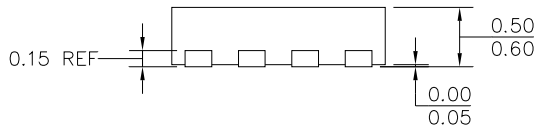
UTQFN-8 (2.0mmx1.5mmx0.55mm)



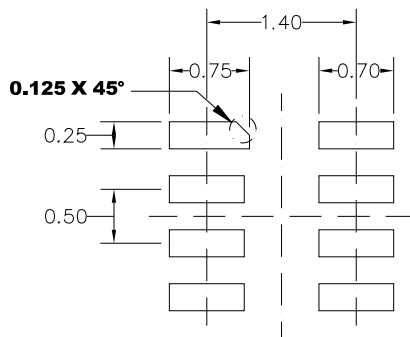
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

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