MP2386C

24V, 8A, Low I_Q, Synchronous Buck Converter with Forced Continuous Conduction Mode

DESCRIPTION

The MP2386C is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter. The MP2386C offers a super-compact solution that achieves 8A of continuous output current over a wide input supply range.

The MP2386C operates at high efficiency over a wide output current load range based on MPS's proprietary switching loss reduction technique and internal low $R_{DS(ON)}$ power MOSFETs.

Adaptive constant-on-time (COT) control provides fast transient response and eases loop stabilization. The DC auto-tune loop, combined with the remote differential sense, provides good load and line regulation.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The converter requires a minimal number of external components, and is available in a QFN-11 (2mmx2mm) package.

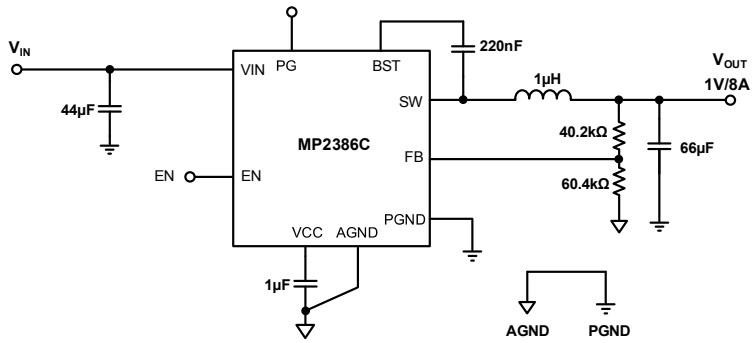
FEATURES

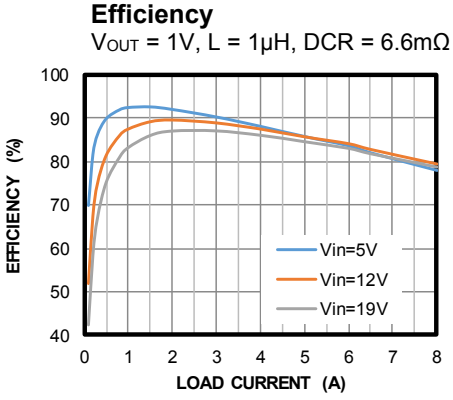
- Wide 4.5V to 24V Operating Input Range
- 105μA Low Quiescent Current
- 8A Continuous Output Current
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Forced PWM Operation Mode
- Proprietary Switching Loss Reduction Technique
- Power Good (PG) Indication
- Fixed 700kHz Switching Frequency
- Stable with POSCAP and Ceramic Capacitors
- Internal Soft Start (SS)
- Output Discharge
- OCP, OVP, UVP, and Thermal Shutdown with Auto-Retry
- Available in a QFN-11 (2mmx2mm) Package
- The MPL-AL6050 Inductor Series Matches Best Performance

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2386CGG	QFN-11 (2mmx2mm)	*See Below*	1

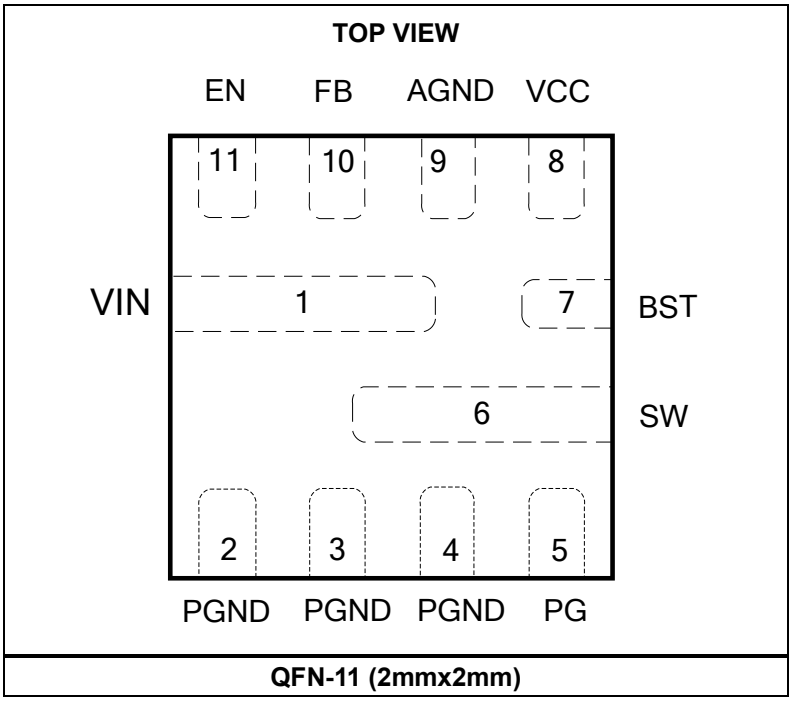
* For Tape & Reel, add suffix –Z (e.g. MP2386CGG–Z).

TOP MARKING

KKY
LLLL

KK: Product code of MP2386CGG
Y: Year code
LLLL: Lot number

PACKAGE REFERENCE



QFN-11 (2mmx2mm)

PIN FUNCTIONS

PIN #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power to the internal MOSFET and regulator. The MP2386C operates from a 4.5V to 24V input rail. An input capacitor is needed to decouple the input rail. Connect VIN with wide PCB traces and multiple vias. Apply at least two layers to this input trace.
2, 3, 4	PGND	**Power ground.** Connect PGND with wide PCB traces and multiple vias.
5	PG	**Power good output.** The output of PG is an open drain.
6	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on time of the PWM duty cycle. The inductor current drives SW negative during the off time. The on resistance of the low-side switch and the internal diode fixes the negative voltage. Connect SW with wide and short PCB traces.
7	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
8	VCC	**Internal VCC LDO output.** VCC powers the driver and control circuits. Decouple VCC with a minimum 1µF ceramic capacitor placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
9	AGND	**Signal logic ground.** AGND is the Kelvin connection to PGND.
10	FB	**Feedback.** An external resistor divider from the output to GND tapped to FB sets the output voltage. Place the resistor divider as close to FB as possible. Avoid vias on the FB traces and V_{SEN} trace. Keep the V_{SEN} trace far away from the SW node.
11	EN	**Buck enable.** EN is a digital input that turns the buck regulator on or off. When the power supply of the control circuit is ready, drive EN high to turn on the buck regulator. Drive EN low to turn off the buck regulator. Connect EN to VIN through a resistive voltage divider for automatic start-up. Do not let the EN voltage exceed 4.5V at any time. Do not float EN.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 26V
V_{SW} (DC)..... -1V to V_{IN} + 0.3V
V_{SW} (transient)..... -9V for <2ns,
-5V to V_{IN} + 4V for <25ns (2)
V_{BST}..... V_{SW} + 4.5V
All other pins ..... -0.3V to +4.5V
Continuous power dissipation (T_A = 25°C) (3) (5)
QFN-11 (2mmx2mm)..... 3.6W
Junction temperature ..... 150°C
Lead temperature..... 260°C
Storage temperature .....-65°C to +150°C

ESD Rating

Human-body model (HBM).....1.8KV
Charged-device model (CDM).....2KV

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 4.5V to 24V
Output voltage (V_{OUT})..... 0.6V to 13V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-11 (2mmx2mm)			
EV2386C-G-00A (5)	34	9	°C/W
JESD51-7 (6)	55	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured by using a differential oscilloscope probe.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV2386C-G-00A, 4-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical value tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (quiescent)	I_{IN}	V_{EN} = 3.3V, V_{FB} = 0.62V		105	145	μA
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			2	μA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}			34		mΩ
Low-side switch on resistance	LS_{RDS-ON}			10		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	5	μA
Current Limit						
Low-side valley current limit	I_{LIMIT_LS}		7	9	11	A
Negative current limit	I_{NEG}	V_{OUT} = 3.3V, L_O = 2.2μH		-1.5		A
Switching Frequency and Minimum Off Timer						
Switching frequency	f_{SW}	V_{IN} = 12V, V_{OUT} = 3.3V	600	700	800	kHz
Minimum on time [8]	t_{ON_Min}			50		ns
Minimum off time [8]	t_{OFF_Min}			200		ns
Over-Voltage and Under-Voltage Protection (OVP, UVP)						
OVP threshold	V_{OVP}	V_{FB}	125%	130%	135%	V_{REF}
UVP-1 threshold	V_{UVP}	V_{FB}	70%	75%	80%	V_{REF}
UVP-1 hold off timer [8]	t_{OC}	V_{OUT} = 60% V_{REF}		32		μs
UVP-2 threshold	V_{UVP}	V_{FB}	45%	50%	55%	V_{REF}
Reference and Soft Start (REF, SS)						
REF voltage	V_{REF}		590	600	610	mV
Soft-start time [8]	t_{SS}		1.1	1.7	2.3	ms
Enable and Under-Voltage Lockout (EN, UVLO)						
Enable rising threshold	V_{EN_Rising}		1.15	1.25	1.35	V
Enable hysteresis	V_{EN_HYS}			150		mV
Enable input current	I_{EN}	V_{EN} = 3.3V		3.3		μA
VCC UVLO threshold rising	VCC_{Vth_R}		3.1	3.3	3.5	V
VCC UVLO threshold hysteresis	VCC_{HYS}			420		mV
VIN UVLO threshold rising	VIN_{VTH_R}		4.2	4.35	4.48	V
VIN UVLO threshold hysteresis	VIN_{HYS}			550		V
VCC Regulator						
VCC voltage	V_{CC}		3.45	3.65	3.85	V
VCC load regulation	V_{CC_Reg}	I_{VCC} = 5mA		5		%
Thermal Protection						
Thermal shutdown [8]	T_{SD}			150		°C
Thermal shutdown hysteresis [8]	T_{SD_HYS}			25		°C

Notes:

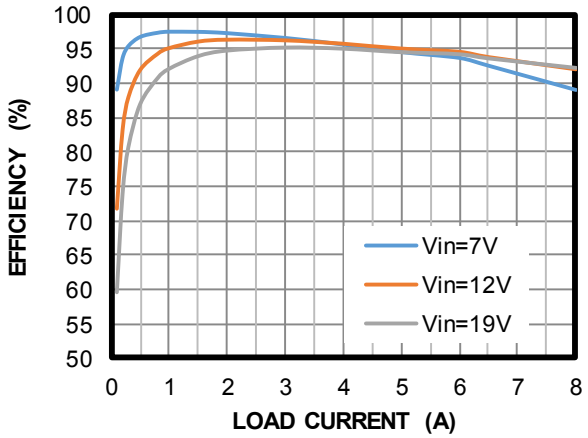
7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

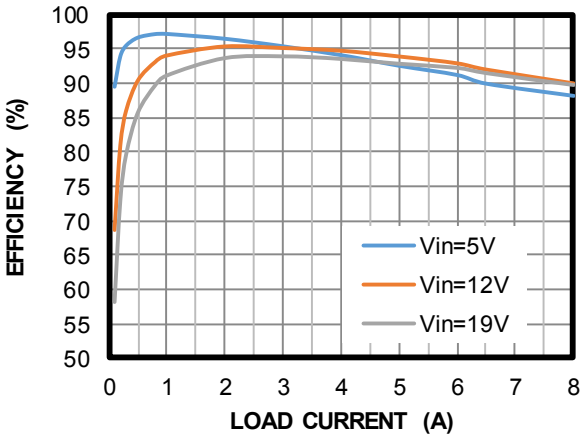
Efficiency

V_{OUT} = 5V, L = 3.3µH, DCR = 9mΩ



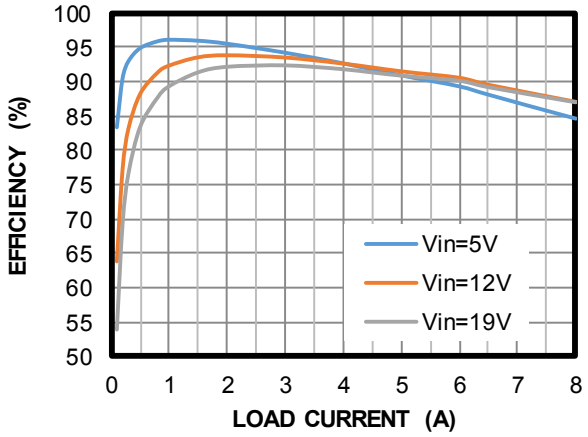
Efficiency

V_{OUT} = 3.3V, L = 3.3µH, DCR = 9mΩ



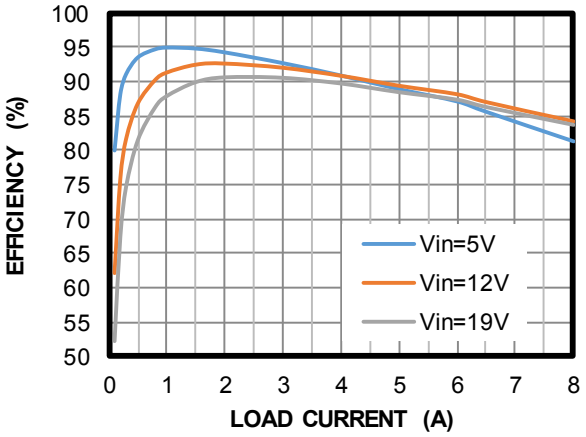
Efficiency

V_{OUT} = 2.5V, L = 2.2µH, DCR = 11.4mΩ



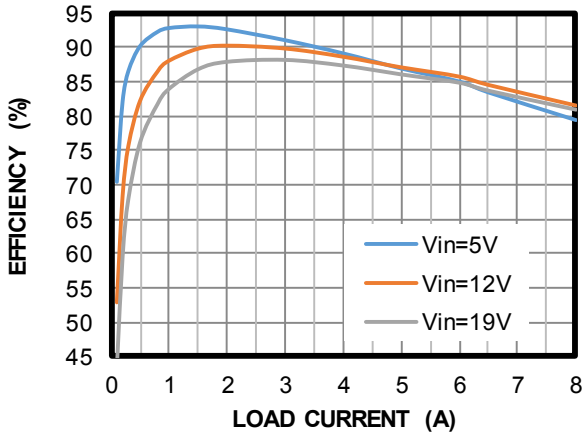
Efficiency

V_{OUT} = 1.8V, L = 2.2µH, DCR = 11.4mΩ



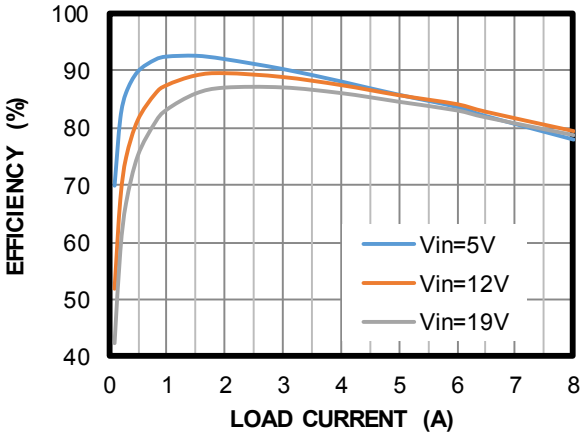
Efficiency

V_{OUT} = 1.2V, L = 1.5µH, DCR = 6.6mΩ



Efficiency

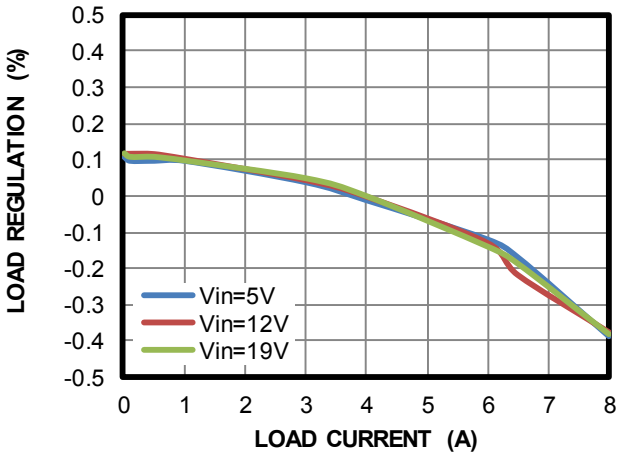
V_{OUT} = 1V, L = 1µH, DCR = 6.6mΩ



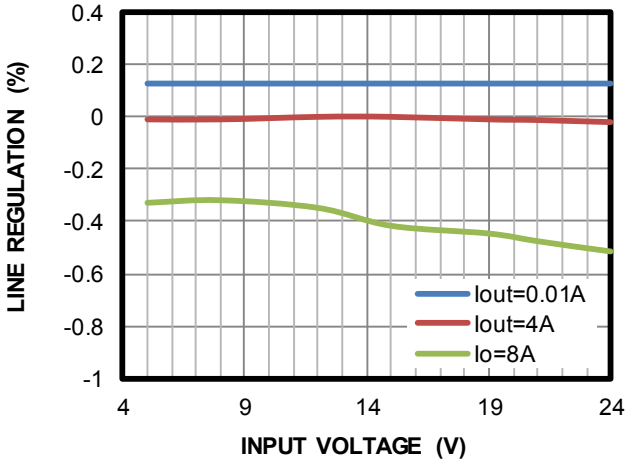
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

Load Regulation

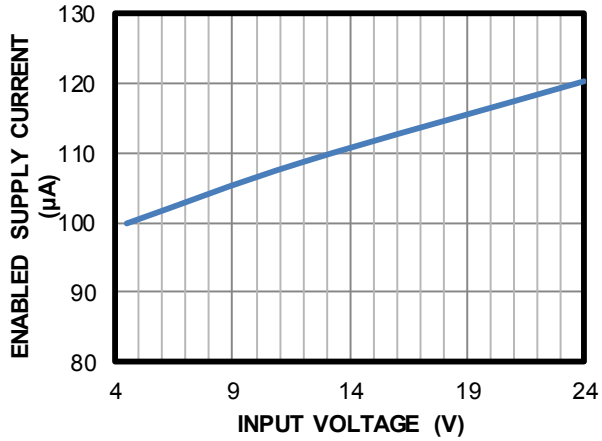


Line Regulation



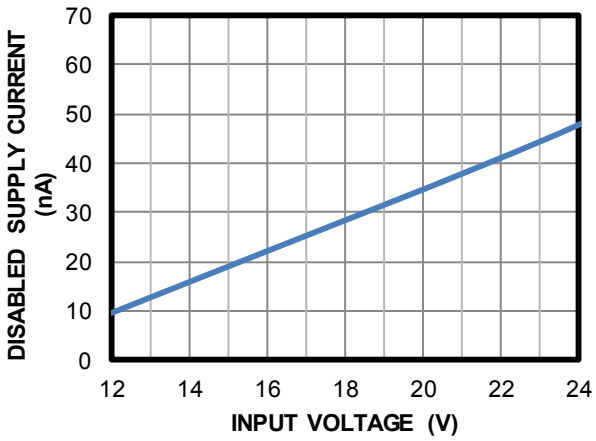
Enabled Supply Current vs. Input Voltage

V_{EN} = 3.3V, V_{FB} = 0.62V



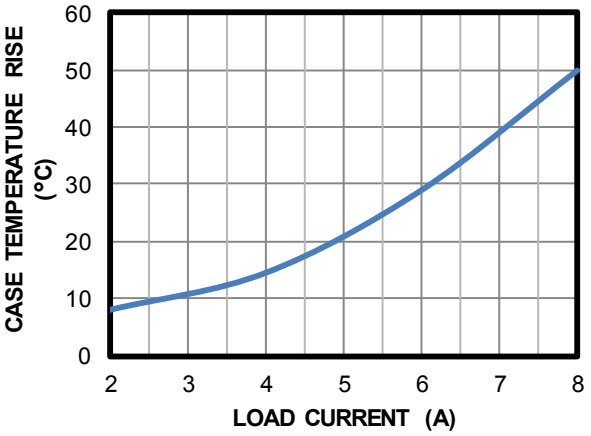
Disabled Supply Current vs. Input Voltage

V_{EN} = 0V

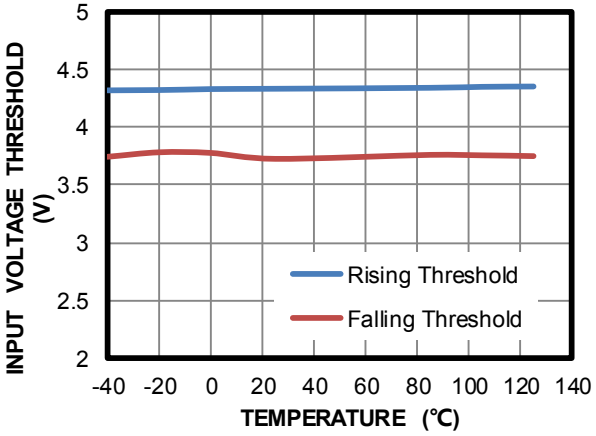


Case Temperature Rise vs. Load Current

V_{IN} = 12V, V_{OUT} = 1V



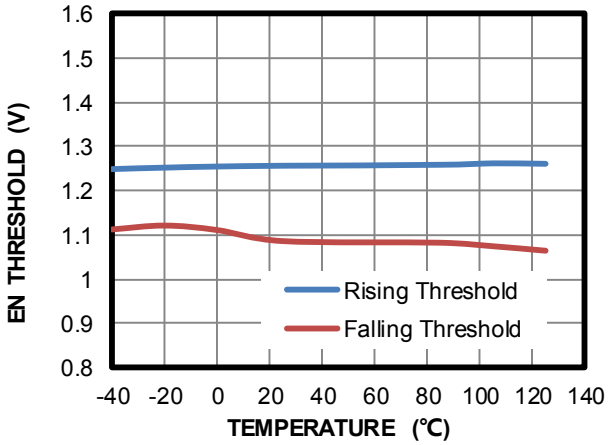
Input Voltage Threshold vs. Temperature



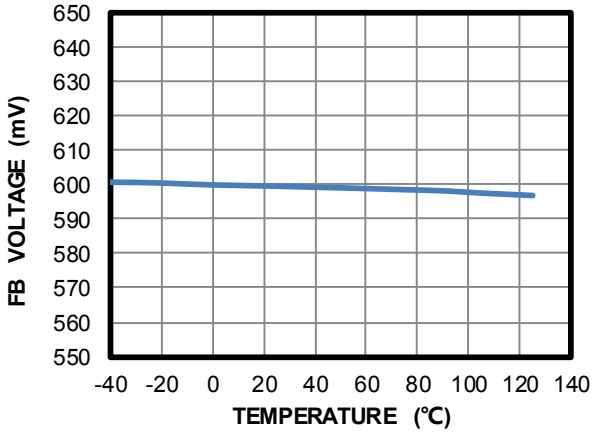
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

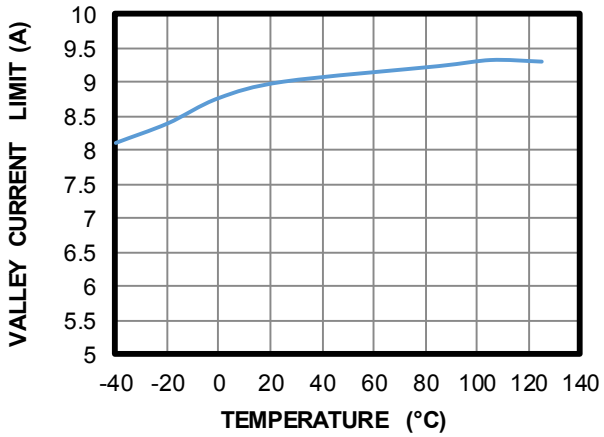
EN Threshold vs. Temperature



FB Voltage vs. Temperature

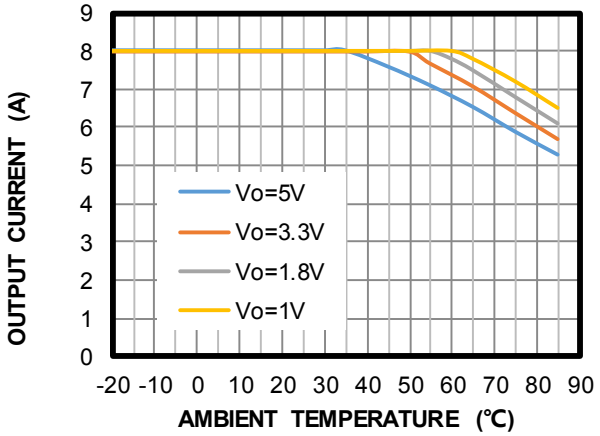


Valley Current Limit vs. Temperature



Output Current Derating vs. Ambient Temperature

V_{IN} = 12V, T_J < 125°C, 4-layer PCB, 6.4cmx6.4cm size

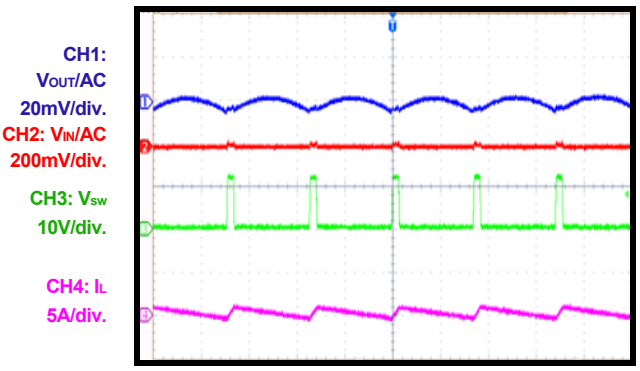


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

Input/Output Ripple

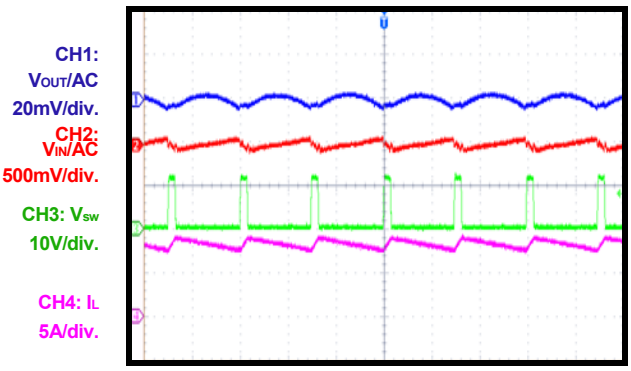
I_{OUT} = 0A



1µs/div.

Input/Output Ripple

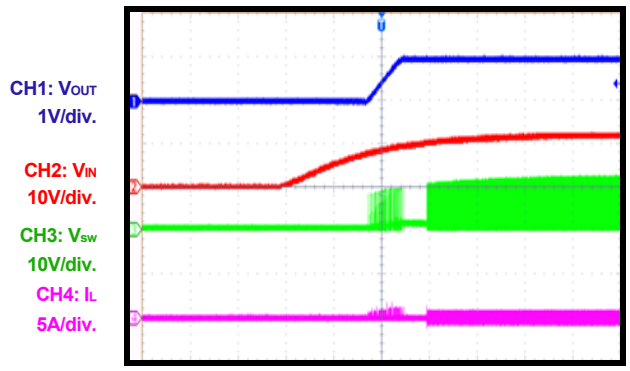
I_{OUT} = 8A



1µs/div.

Start-Up through Input Voltage

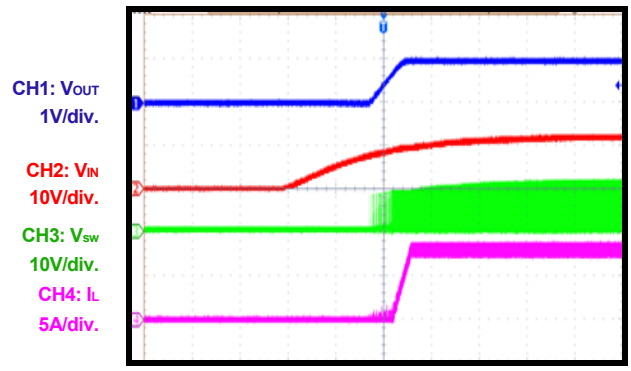
I_{OUT} = 0A



2ms/div.

Start-Up through Input Voltage

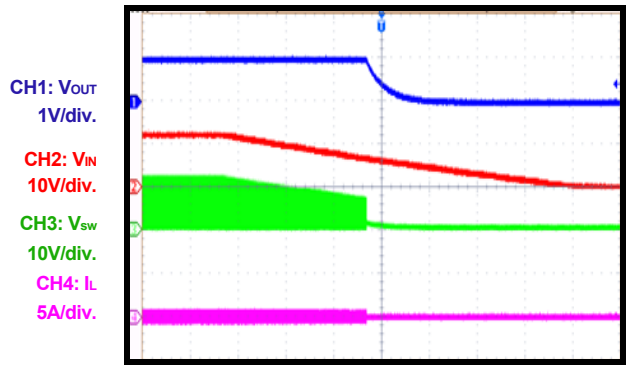
I_{OUT} = 8A



2ms/div.

Shutdown through Input Voltage

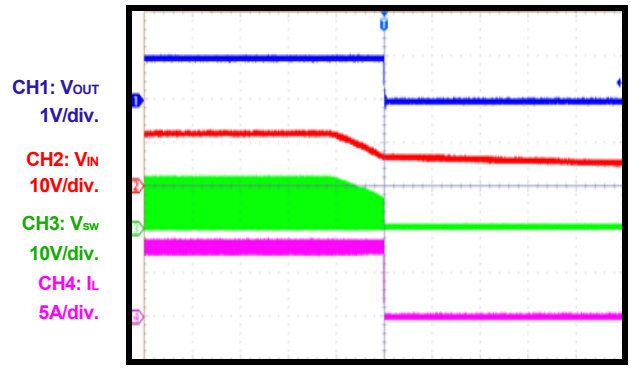
I_{OUT} = 0A



10ms/div.

Shutdown through Input Voltage

I_{OUT} = 8A



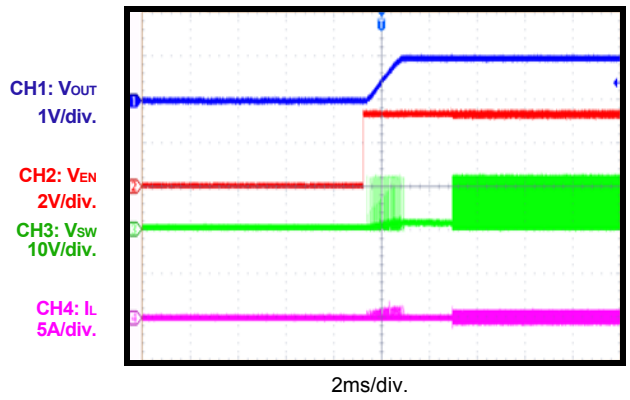
2ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

Start-Up through Enable

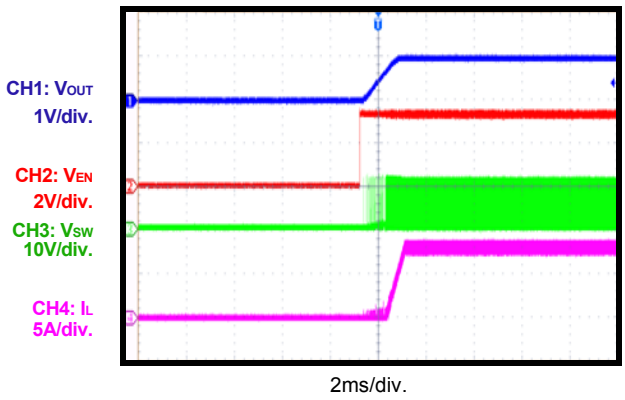
I_{OUT} = 0A



2ms/div.

Start-Up through Enable

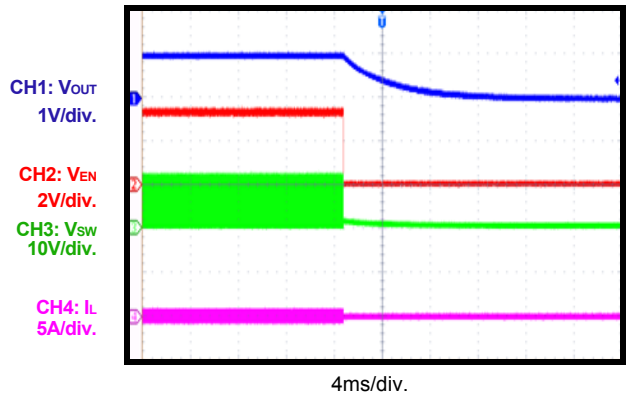
I_{OUT} = 8A



2ms/div.

Shutdown through Enable

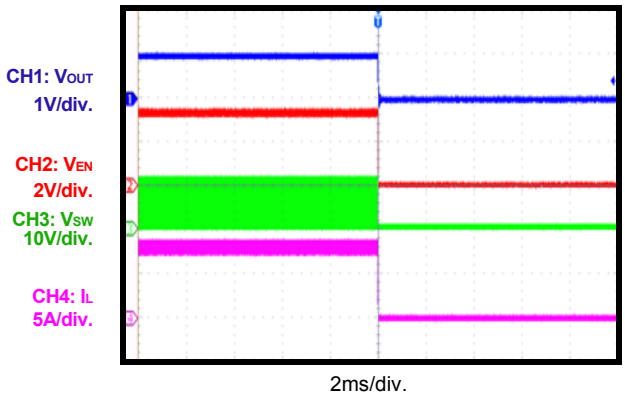
I_{OUT} = 0A



4ms/div.

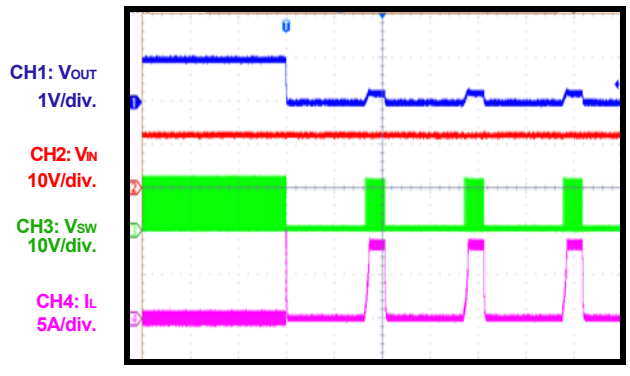
Shutdown through Enable

I_{OUT} = 8A



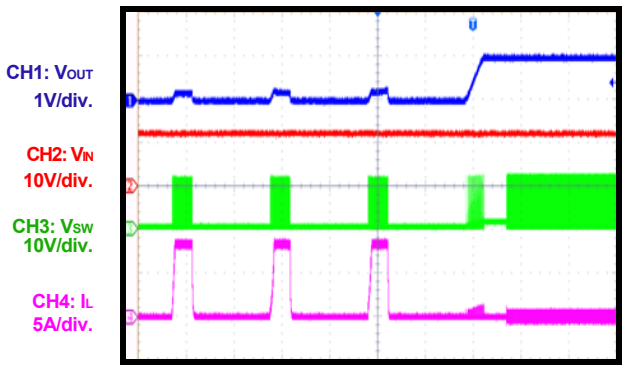
2ms/div.

Short-Circuit Entry



4ms/div.

Short-Circuit Recovery



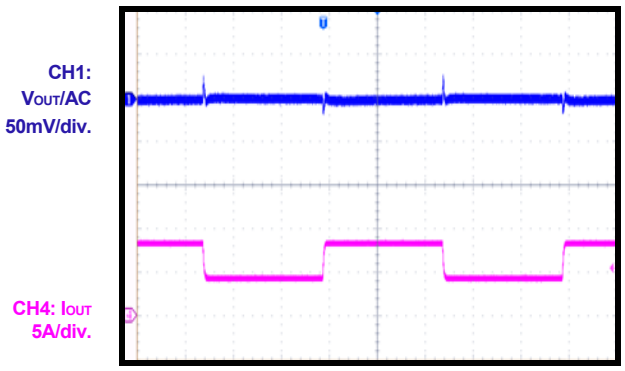
4ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 1µH, T_A = 25°C, unless otherwise noted.

Load Transient

I_{OUT} = 4A to 8A, slew rate = 2.5A/µs
by CCDH e-load



200µs/div.

FUNCTIONAL BLOCK DIAGRAM

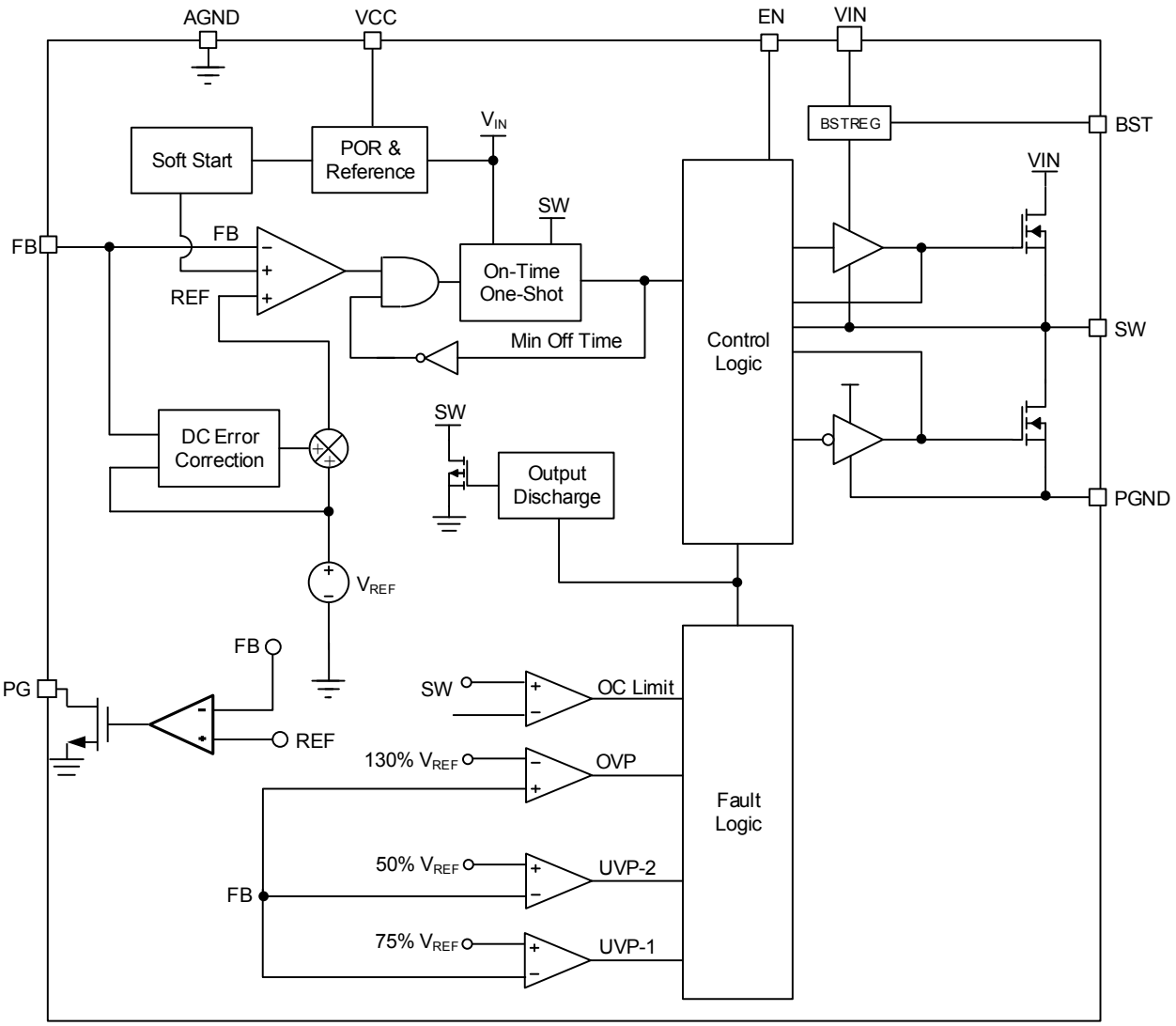


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The MP2386C is a fully integrated, synchronous, rectified, step-down, switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET turns off, or enters its off state. It turns on again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize the conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time, called shoot-through. To avoid shoot-through, a dead time (DT) is internally generated between the HS-FET off and LS-FET on periods, or vice versa.

The MP2386C operates in forced continuous conduction mode (CCM). The low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. To prevent shoot-through, a dead time is generated internally between the HS-FET off and LS-FET on periods, or vice versa.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

Large Duty Cycle Operation

When V_{IN} is below 7V and V_{OUT} is above 4.2V, the MP2386C reduces the switching frequency to about 280kHz to support large duty cycle operation. If V_{OUT} is below 3.9V, the part returns to its normal switching frequency.

Jitter and FB Ramp

Jitter occurs in both PWM and skip mode when noise in the V_{FB} ripple propagates a delay to the HS-FET driver (see Figure 2 and Figure 3). Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope, so the jitter in DCM is usually larger than that one in CCM, however, the V_{FB} ripple does not directly affect noise immunity.

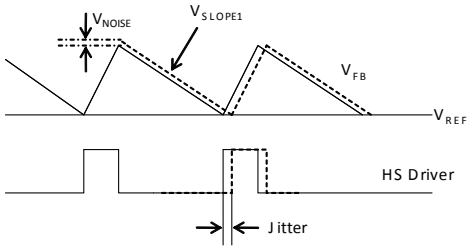


Figure 2: Jitter in PWM Mode

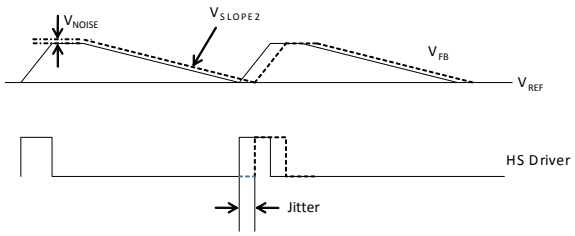


Figure 3: Jitter in Skip Mode

Operating with External Ramp Compensation

The MP2386C is usually able to support ceramic output capacitors without an external ramp. However, in some cases, the internal ramp may not be enough to stabilize the system, or the jitter may be too big, and external ramp compensation is needed. See the Application Information section on page 15 for design steps with external ramp compensation.

Configuring the EN Control

The EN pin enables or disables the whole chip. Pull EN high to turn on the regulator, and pull EN low to turn it off. Do not float this pin.

For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from VIN to EN) and the pull-down resistor (R_{DOWN} from EN to GND) to determine the automatic start-up voltage using Equation

(1):

$$V_{IN-START} = 1.25 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} (V) \quad (1)$$

For example, for R_{UP} = 150kΩ and R_{DOWN} = 51kΩ, $V_{IN-START}$ is set at 4.92V.

The EN voltage must not exceed 4.5V to avoid damaging the internal circuit.

Power Good

The power good indicates whether the output voltage is in the normal range compared to the internal reference voltage. It is an open-drain structure. An external pull-up supply is needed. During power-up, the power good output is pulled low. This indicates to the system to remain off and keep the load on the output to a minimum, which helps to reduce inrush current at start-up.

When the output voltage is above 92% and below 117% of the internal reference voltage and soft start is finished, the power good signal is pulled high. When the output voltage is below 87% after soft start finishes, the PG signal remains low. When the output voltage is above 117% of the internal reference, PG switches to low. The PG signal goes back to high after the output voltage drops below 105% of the internal reference voltage.

The PG output is pulled low when EN UVLO, input UVLO, OCP, or OTP is triggered.

Soft Start

The MP2386C employs a soft start (SS) mechanism to ensure a smooth output during power-up. When the EN pin goes high, the internal reference voltage ramps up gradually. Therefore, the output voltage also ramps up smoothly. Once the reference voltage reaches the target value, soft start finishes and the part enters steady state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side switches until the internal reference voltage exceeds the sensed output voltage at the FB node.

Over-Current Limit

The MP2386C has cycle-by-cycle over-current limiting control. The current-limit circuit employs a valley current-sensing algorithm. The part uses the $R_{DS(ON)}$ of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle even if FB is lower than REF. Figure 4 shows the detailed operation of valley current limit control.

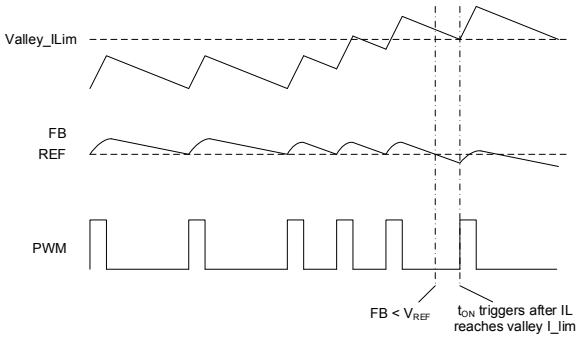


Figure 4: Valley Current Limit Control

Since the comparison is done during the LS-FET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at over-current threshold (I_{OC}) can be calculated with Equation (2):

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

The OCL limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, and the output voltage tends to fall off. If it continues to fall, it crosses the under-voltage protection (UVP) threshold and the part enters hiccup protection mode.

Over-Voltage and Under-Voltage Protection (OVP/UVP)

The MP2386C monitors a resistor-divided feedback voltage to detect over-voltage and under-voltage. When the feedback voltage exceeds 130% of the target voltage, the OVP comparator output goes high, the circuit latches, the HS-FET driver turns off, and the LS-FET turns on to act as a current source.

When the feedback voltage is below 75% and above 50% of V_{REF}, the UVP-1 comparator output goes high. The part enters hiccup mode if V_{FB} stays in this range for about 32µs. The LS-FET remains on until the inductor current goes to zero. During this period, the valley

current limit helps control the inductor current.

When V_{FB} falls below 50% of V_{REF}, the UVP-2 comparator output goes high, and the part enters hiccup mode directly after the comparator and logic delay.

UVLO Protection

The MP2386C has two under-voltage lockout (UVLO) protections: 3.3V VCC UVLO and 4.35V V_{IN} UVLO. The part can start up only when both VCC and V_{IN} exceed their respective UVLO thresholds. It shuts down if either the VCC voltage is below the UVLO falling threshold voltage (typically 2.88V) or V_{IN} is below the 3.8V V_{IN} falling threshold. Both UVLO protections are non-latch protections.

If an application requires a higher under-voltage lockout (UVLO), use the EN pin to adjust the input voltage UVLO with two external resistors (see Figure 5).

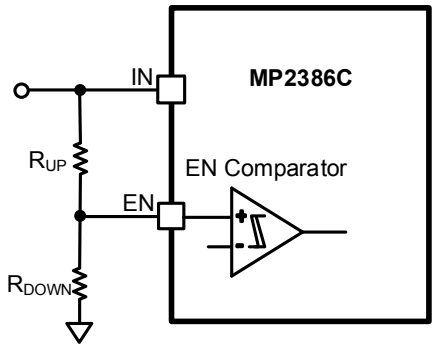


Figure 5: Adjustable UVLO

Thermal Shutdown

Thermal shutdown is employed in the MP2386C. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typically 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a soft start.

Output Discharge

The MP2386C discharges the output if the controller is turned off by the protection functions (UVP, OCP, OVP, UVLO, and thermal shutdown). The discharge resistor on the output is typically 6Ω.

APPLICATION INFORMATION

Setting the Output Voltage without External Compensation

The MP2386C has an internal ramp. When the internal compensation is sufficient for stable operation with ceramic output capacitors, the MP2386C does not require external ramp compensation. The output voltage is then set by feedback resistors R1 and R2 (see Figure 6).

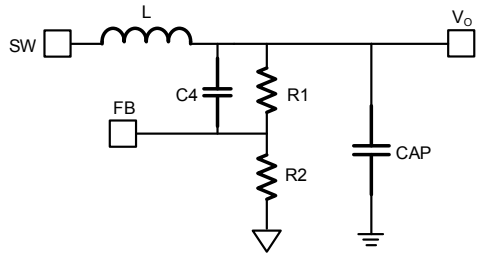


Figure 6: Simplified Circuit without an External Ramp

First, choose a value for R2. R2 should be chosen carefully, since a small R2 leads to considerable quiescent current loss, but a large R2 makes FB more sensitive to noise. Set R2 between 5kΩ and 100kΩ. Considering the output ripple, R1 can be determined with Equation (3):

$$R_1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (3)$$

C4 acts as a feed-forward capacitor to improve the transient. A larger C4 leads to better transient, but more noise sensitivity.

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Parameters Selection for Common Output Voltages (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C4 (pF)	L (µH)
5	40.2	5.49	33	3.3
3.3	40.2	8.87	33	3.3
2.5	40.2	12.7	33	2.2
1.8	40.2	20	33	2.2
1.5	40.2	26.7	33	1.5
1.2	40.2	40.2	33	1.5
1	40.2	60.4	33	1

Note:

9) For additional component parameters, see the Typical Application Circuits on page 18.

Setting the Output Voltage with External Compensation

If the system is not stable enough or the jitter is too large when ceramic capacitors are used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4. Since an internal ramp has already been added in the system, a 1MΩ (R4), 220pF (C4) ramp is typically sufficient.

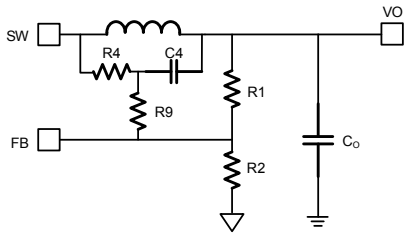


Figure 7: Simplified Circuit with External Ramp

The output voltage is influenced by R4 in addition to the R1 and R2 divider (see Figure 7). R2 should be chosen carefully, since a small R2 leads to considerable quiescent current loss while a large R2 makes FB more sensitive to noise. Set R2 between 5kΩ and 100kΩ. R1 can then be determined with Equation (4):

$$R_1 = \frac{1}{\frac{V_{REF}}{V_{OUT} - V_{REF}} - \frac{R2}{R4}} \cdot R_2 \quad (4)$$

Usually, R9 is set to 0Ω. To get a pole for better noise immunity, R9 can also be set using Equation (5):

$$R_9 = \frac{1}{2\pi \times C_4 \times 2f_{SW}} \quad (5)$$

R9 should be set in the range of 100Ω to 1kΩ to reduce its influence on the ramp.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance, and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended since they are fairly stable amid temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification. The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (10)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be estimated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

The maximum output capacitor limitation should also be considered in the design application. The MP2386C has a soft-start time of about 1.7ms. If the output capacitor value is too high, the output voltage cannot reach the design value during soft start and fails to regulate. The maximum output capacitor value (C_{O_MAX}) can be limited approximately with Equation (13):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and t_{ss} is the soft-start time.

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be 30% to 50% of the maximum output current, and to ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (14):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, including a short current.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
Select family series (MPL-AL)	1μH to 3.3μH	MPS
MPL-AL6050-1R0	1μH	MPS
MPL-AL6050-1R5	1.5μH	MPS
MPL-AL6050-2R2	2.2μH	MPS
MPL-AL6050-3R3	3.3μH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A 4-layer layout is recommended for better thermal performance. For best results, refer to Figure 8 and follow the guidelines below:

1. Place the high-current paths (PGND, VIN, SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitors as close to VIN and PGND as possible.
3. Place the decoupling capacitor as close to VCC and AGND as possible.
4. Keep the switching node (SW) short and away from the feedback network.
5. Keep the BST voltage path as short as possible.
6. Keep the VIN and PGND pads connected with large copper planes to achieve better thermal performance.
7. Add several vias close to the VIN and PGND pads to help with thermal dissipation.

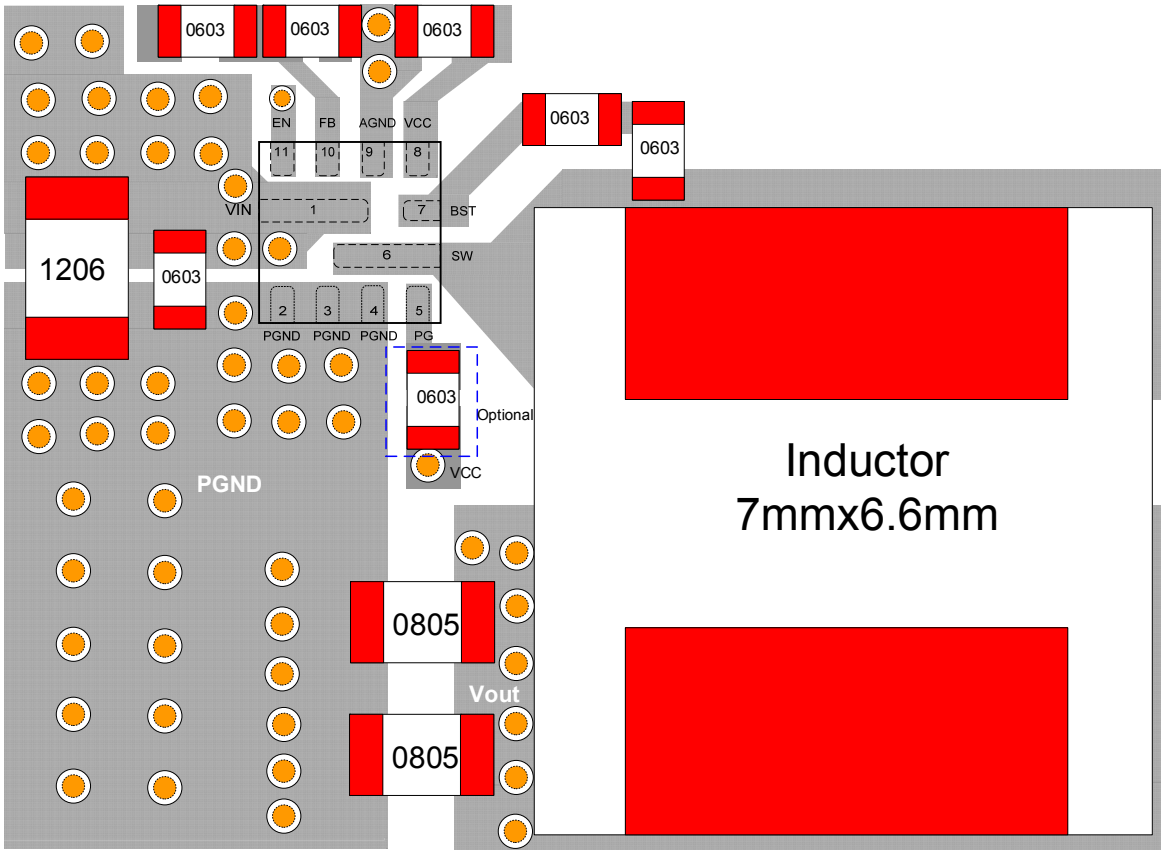


Figure 8: Recommended PCB Layout

Design Example

Table 3 shows a design example when ceramic capacitors are applied.

Table 3: Design Example

V_{IN}	8V to 24V
V_{OUT}	1V
I_{OUT}	8A

Figure 9 through Figure 15 show the detailed application schematics. For typical performance and waveforms, see the Typical Characteristics section on page 5. For more device applications, refer to the related evaluation board datasheet.

TYPICAL APPLICATION CIRCUITS (10)

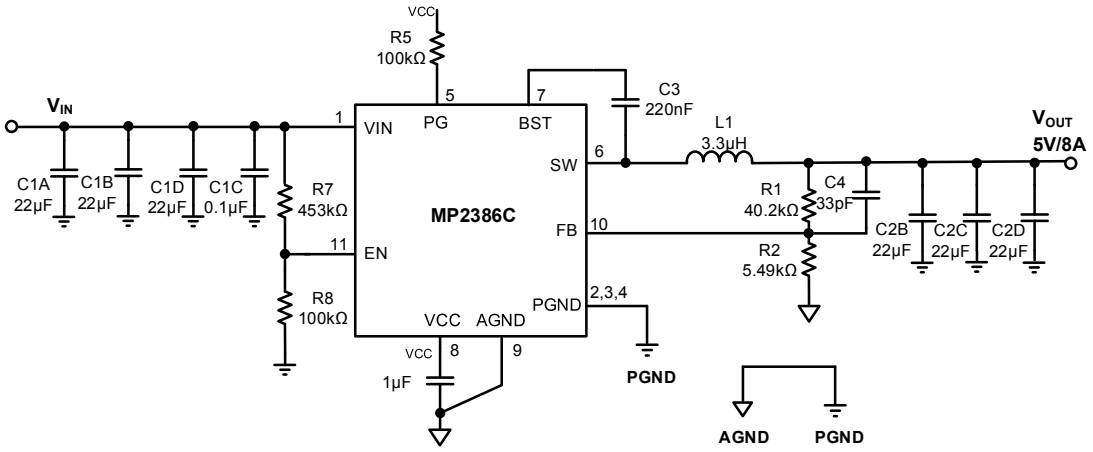


Figure 9: V_{IN} = 19V, V_{OUT} = 5V/8A

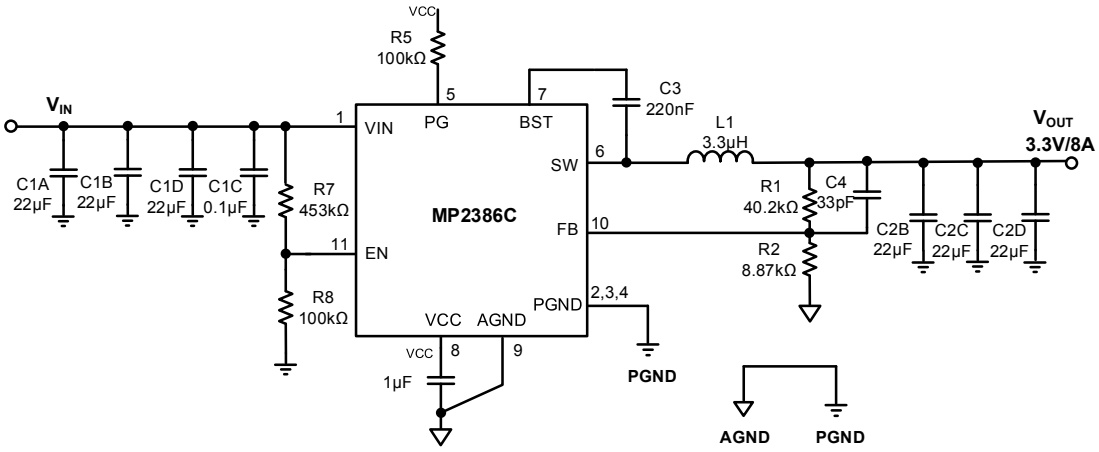


Figure 10: V_{IN} = 19V, V_{OUT} = 3.3V/8A

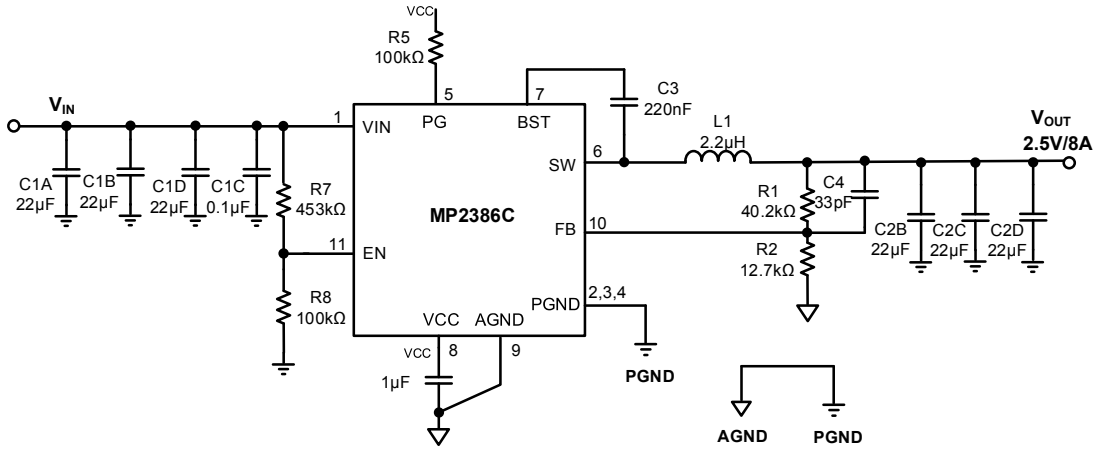


Figure 11: V_{IN} = 19V, V_{OUT} = 2.5V/8A

TYPICAL APPLICATION CIRCUITS (10) *(continued)*

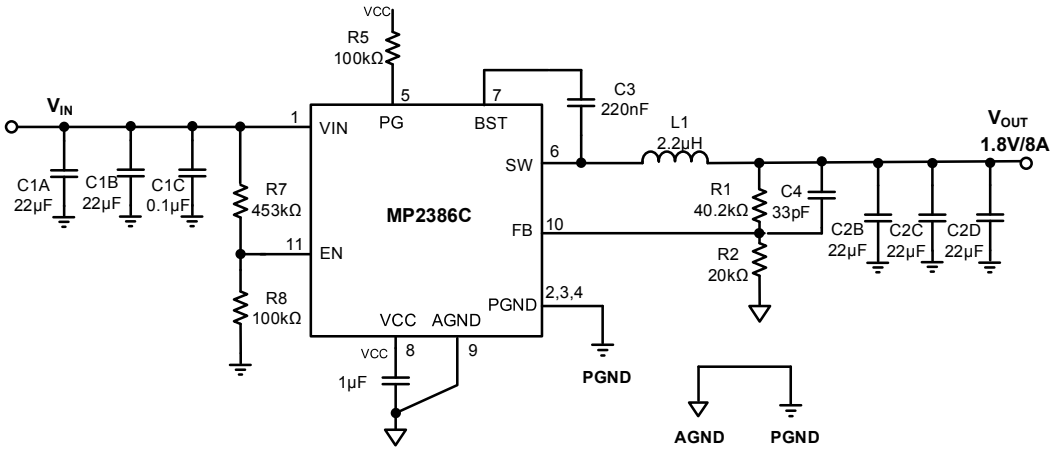


Figure 12: V_{IN} = 19V, V_{OUT} = 1.8V/8A

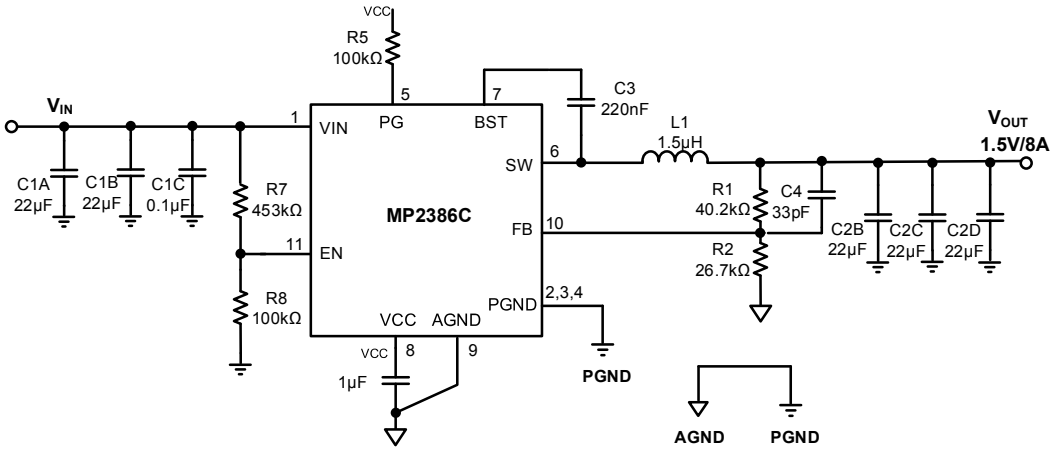


Figure 13: V_{IN} = 19V, V_{OUT} = 1.5V/8A

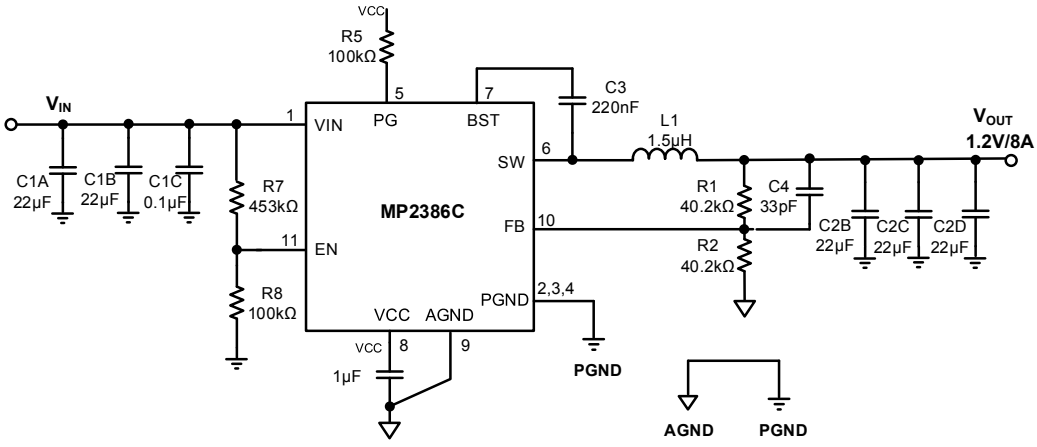


Figure 14: V_{IN} = 19V, V_{OUT} = 1.2V/8A

TYPICAL APPLICATION CIRCUITS (10) *(continued)*

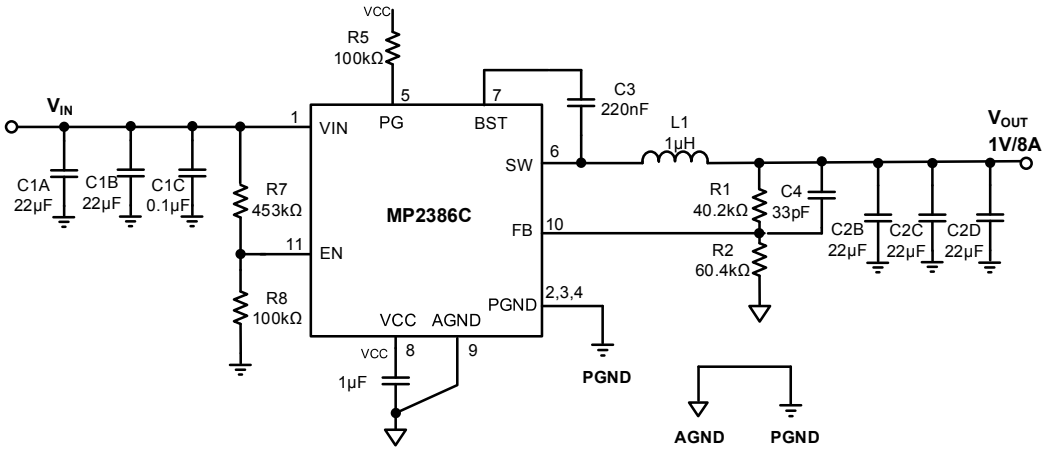


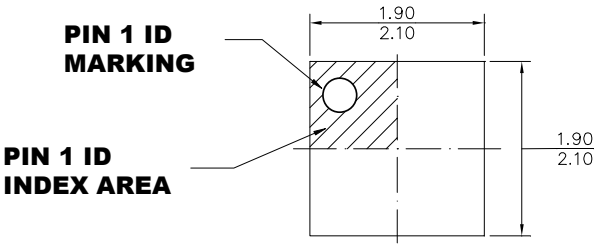
Figure 15: V_{IN} = 19V, V_{OUT} = 1V/8A

Note:

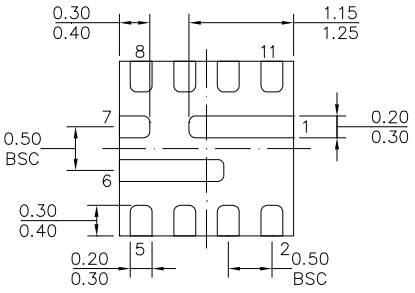
10) An EN resistor divider sets the VIN threshold to 7.5V. For 5V input applications, change the EN resistor accordingly.

PACKAGE INFORMATION

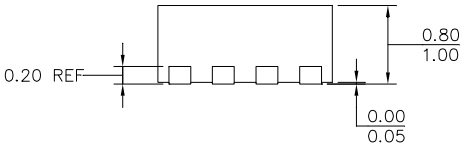
QFN-11 (2mmx2mm)



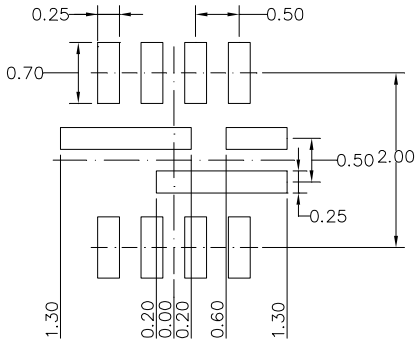
TOP VIEW



BOTTOM VIEW



SIDE VIEW

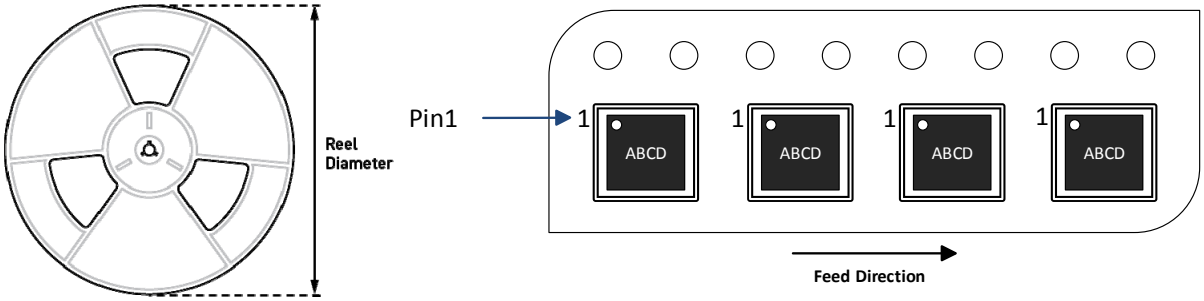


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1 AND PIN6 HAVE THE SAME LENGTH AND WIDTH
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/Reel	Quantity/Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2386CGG–Z	QFN-11 (2mmx2mm)	5000	N/A	13in.	12mm	8mm