MP2660

5V USB, 500mA, I^2C-Controlled Linear Charger with Power Path Management for Single-Cell Li-Ion Battery

The Future of Analog IC Technology®

DESCRIPTION

The MP2660 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power path management for space-limited portable applications. This device takes input power from either an AC adapter or a USB port to supply the system load and charge the battery independently. The charger section features constant current pre-charge, constant current fast charge (CC) and constant voltage (CV) regulation, charge termination, and auto-recharge.

The power path management function ensures continuous power to the system even with a dead battery by automatically selecting the input, the battery, or both to power the system. This power stage features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2660 provides system short-circuit protection (SCP) by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged due to excessively high currents. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below the programmable battery UVLO threshold, which prevents the Li-ion battery from being over-discharged. An integrated I^2C control interface allows the MP2660 to program the charging parameters including the input current limit, input minimum voltage regulation, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2660 is available in a 9-pin WLCSP (1.55mmx1.55mm) package.

FEATURES

- Compatible with 5V USB Power Sources
- Fully Autonomous Charger for Single-Cell Li-Ion/Li-Polymer Batteries
- Complete Power Path Management for Simultaneously Powering the System and Charging the Battery
- Programmable Input Current Limit and Input Minimum Voltage Regulation Thresholds
- ±0.5% Charging Voltage Accuracy
- 13V Maximum Voltage for the Input Source
- I^2C Interface for Programming Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- Built-In Battery Disconnection Function for Shipping Mode
- Thermal Limiting Regulation on the Chip
- Available in an Ultra-Compact WLCSP-9 (1.55mmx1.55mm) Package

APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smart Watches
- Bluetooth Headphones

TYPICAL APPLICATION

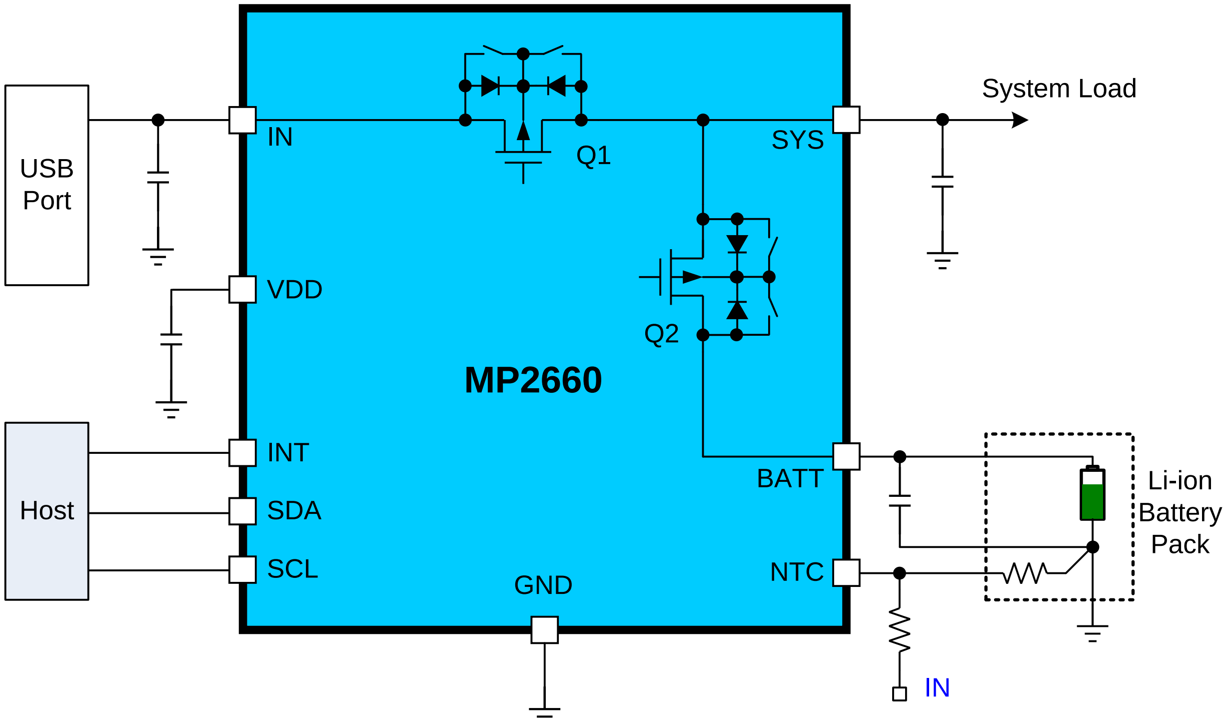


Table 1: Operation Mode Table

FET On/Off Change By Control	I²C Control		
	EN_HIZ = 1	**CEB = 1**	**FET_DIS = 1**
	Enter Hi-Z Mode	**Charge Control**	**Enter Shipping Mode**
LDO FET	OFF	x	x
Battery FET (charging)	x	OFF	OFF
Battery FET (discharging)	x	x	OFF

x = Don't Care

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2660GC-xxxx**	WLCSP-9 (1.55mmx1.55mm)	*See Below*
EVKT-MP2660	Evaluation kit	

* For Tape & Reel, add suffix -Z (e.g. MP2660GC-xxxx-Z)
**“xxxx” is the register setting option. The factory default is “0000”. This content can be viewed in the I^{2}C register map. Please contact an MPS FAE to obtain an “xxxx” value.

TOP MARKING

$\overline{}$
DPY
LLL

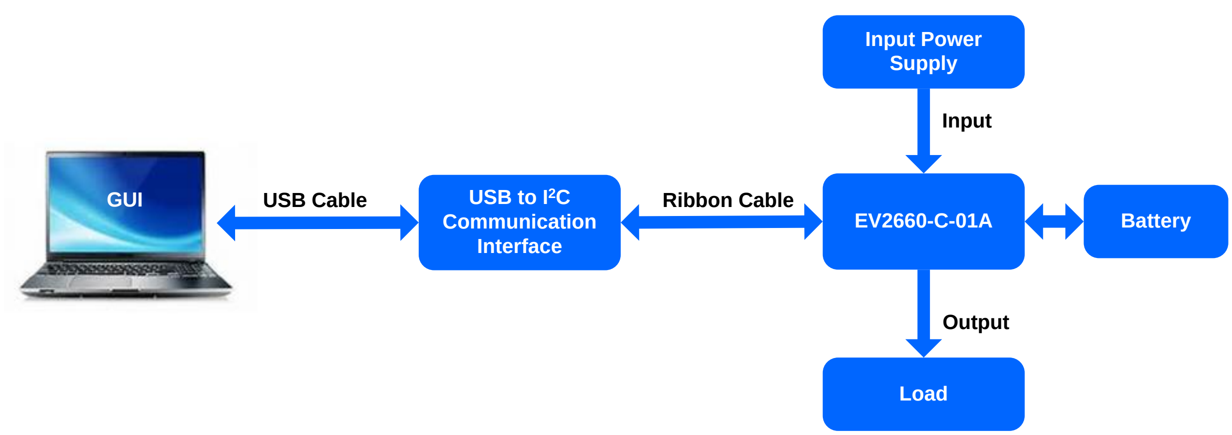
DP: Product code of MP2660GC
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-MP2660

EVKT-MP2660 kit contents (items below can be ordered separately):

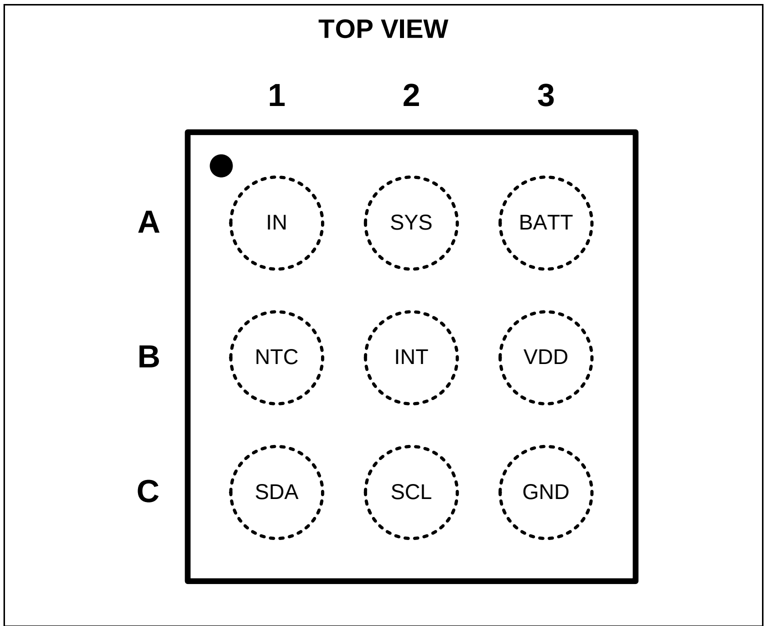
#	Part Number	Item	Quantity
1	EV2660-C-01A	MP2660 evaluation board	1
2	EVKT-USBI2C-02-bag	Includes one USB to I^{2}C communication interface, one USB cable, and one ribbon cable	1
3	Online resources	Include datasheet, user guide, product brief, and GUI	1

Order direct from MonolithicPower.com or our distributors.



EVKT-MP2660 Evaluation Kit Set-Up

PACKAGE REFERENCE



WLCSP-9 (1.55mmx1.55mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
A1	IN	Power	**Input power.** Place a ceramic capacitor from IN to GND as close to the IC as possible.
A2	SYS	Power	**System power supply.** Place a ceramic capacitor from SYS to GND as close to the IC as possible.
A3	BATT	Power	**Battery.** Place a ceramic capacitor from BATT to GND as close to the IC as possible.
B1	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from IN to NTC to GND. The charge is suspended when NTC is out of the range.
B2	INT	I/O	**Interrupt signal.** INT sends the charging status and fault interruption to the host. INT can also disconnect the system from the battery. Pull INT low for >8s to disconnect the battery from the system. Use a ≥100kΩ external pull-up resistor for INT.
B3	VDD	Power	**Internal control power supply.** Connect a ceramic capacitor (0.1µF) from VDD to GND. No external load is allowed.
C1	SDA	I/O	**I²C Interface data.** Connect SDA to the logic rail through a 10kΩ resistor.
C2	SCL	I	**I²C Interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
C3	GND	Power	**Ground.**

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .... -0.3V to +13V
All other pins to GND .... -0.3V to +6.0V
Continuous power dissipation (T_A = 25°C) (2)
.... 0.88W
Junction temperature .... 150°C
Lead temperature (solder) .... 260°C
Storage temperature .... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .... 4.35V to 5.5V (USB input)
I_{IN} .... up to 455mA
I_{SYS} .... up to 1.6A
I_{CHG} .... up to 455mA
V_{BATT} .... up to 4.545V
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
WLCSP-9 (1.5mmx1.55mm)	114	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the device to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Source and Battery Protection						
Input voltage range	V_{IN}				13	V
Input operation voltage	V_{IN}		4.35	5.0	5.5	V
BATT input voltage (5)	V_{BATT}				4.5	V
Input over-voltage protection threshold	V_{IN_OVP}	Input rising threshold	5.85	6.00	6.15	V
Input OVP hysteresis				335		mV
Input under-voltage lockout threshold	V_{IN_UVLO}	Input rising threshold	3.8	3.9	4.0	V
Input under-voltage lockout threshold hysteresis				180		mV
Input vs. battery headroom threshold	V_{HDRM}	Input rising vs. battery	90	110	130	mV
Input vs. battery headroom threshold hysteresis				66		mV
Battery under-voltage lockout threshold	V_{BATT_UVLO}	BATT voltage falling, programmable, V_{BATT_UVLO} = 2.8V	2.6	2.8	3.0	V
Battery UVLO range		Programmable using I2C	2.4		3.1	V
Battery under-voltage lockout threshold hysteresis		V_{BATT_UVLO} = 2.8V		235		mV
Battery over-voltage protection	V_{BATT_OVP}	Rising, higher than V_{BATT_REG}		120		mV
		Falling, higher than V_{BATT_REG}		65		
Power Path Management						
Regulated system output voltage	V_{SYS_REG}	V_{IN} = 5.5V, I_{SYS} = 10mA, I_{CHG} = 0A	4.85	5.00	5.15	V
Input current limit range		I2C programmable	85		455	mA
Input current limit	I_{IN_LIM}	REG00h, bits[2:0] = 000 - 85mA	63	70	85	mA
		REG00h, bits[2:0] = 001 - 130mA	102	116	130	
		REG00h, bits[2:0] = 100 - 265mA	230	247	265	
		REG00h, bits[2:0] = 111 - 455mA	400	428	455	
Input minimum voltage regulation	V_{IN_MIN}	I2C programmable range	3.88		5.08	V
		I2C setting V_{IN_MIN} = 4.20V	4.10	4.20	4.30	
SYS output voltage	V_{SYS}	Charging mode, V_{IN} = 5.5V, V_{BATT} = 3.7V	4.85	5.00	5.15	V
		Supplement mode, V_{BATT} = 3.7V, I_{BATT} = 100mA	3.6			
		$V_{IN} < V_{IN\_UVLO}$ and $V_{BATT} < V_{BATT\_UVLO}$	0			
IN to SYS switch on resistance	R_{ON_SYS}	V_{IN} = 5V, I_{SYS} = 100mA		300	400	mΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input quiescent current	I_{IN_Q}	V_{IN} = 5.5V, CEB = 0, charge enable, I_{CHG} = 0A, I_{SYS} = 0A		610		µA
		V_{IN} = 5.5V, CEB = 1, charge disable		470		
Battery quiescent current	I_{BATT_Q}	V_{IN} = 5V, CEB = 0, I_{SYS} = 0A, V_{BATT} = 4.3V		33		µA
		V_{IN} = 0V, CEB = 1, I_{SYS} = 0A, V_{BATT} = 4.35V		11	14	
		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, FET_DIS = 1, disconnect mode		4.512	5.017	
BATT input to SYS switch on resistance	R_{ON_BATT}	V_{IN} < 2V, V_{BATT} = 3.5V, I_{SYS} = 100mA		100	150	mΩ
Battery current regulation in discharge mode	I_{DSCHG}	Program range	200		1600 (5)	mA
BATT to SYS switch leakage		V_{BATT} = 4.5V, V_{IN} = V_{SYS} = GND, disconnect mode			1	µA
SYS reverse to BATT switch leakage		V_{SYS} = 6V, V_{IN} = 4.5V, V_{BATT} = GND, CEB = 1			1.2	µA
Battery discharge function controlled by INT (5)	t_{INT}	INT pull low lasting time to turn off the battery discharge function		8		s
		Battery FET lasts for the off time before auto-on		500		ms
Battery Charger						
Battery voltage regulation range	V_{BATT_REG}	Programmable using I²C	3.600		4.545	V
Battery voltage regulation (V_{BATT_REG} = 4.2V)	V_{BATT}	T = 25°C, I_{BATT} = 15mA	4.179	4.200	4.221	V
Battery charge voltage regulation	V_{BATT_REG}	V_{BATT_REG} = 4.2V, REG04h, bits[7:2] = 101000	4.179	4.200	4.221	V
		V_{BATT_REG} = 4.35V, REG04h, bits[7:2] = 110010	4.328	4.350	4.372	
Fast charge current	I_{CC}	V_{IN} = 5V, V_{BATT} = 3.8V, programmable range	8		535 (5)	mA
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 76mA	65	76	87	
		V_{IN} = 5V, V_{BATT} = 3.8V, $I_{CC\_SETTING}$ = 246mA	220	245	270	
Junction temperature regulation(5)	T_{J_REG}	Junction temperature regulation REG06h, bits[1:0] = 11 - Thermal_limit = 120°C		120		°C
Pre-charge current	I_{PRE}	Program range	6		27	mA
		$I_{PRE\_SETTING}$ = 20mA, REG03h, bits[1:0] = 10	13.0	16.5	20.0	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Charge termination current threshold	I_{TERM}	$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 6mA	4.0	6.5	8.5	mA
		$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 13mA	10.0	13.0	16.5	
		$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 20mA	16	20	24	
		$I_{CC\_SETTING}$ ≤ 263mA, (REG02h, bit[4] = 0), $I_{PRE\_SETTING}$ = 27mA	22	27	31	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 6mA	10.0	13.0	16.5	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 13mA	22	27	32	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 20mA	34	41	48	
		$I_{CC\_SETTING}$ ≥ 280mA, (REG02h, bit[4] = 1), $I_{PRE\_SETTING}$ = 27mA	48.0	56.5	65.0	
Pre-charge threshold voltage	V_{BATT_PRE}	V_{BATT} rising, set V_{BATT_PRE} = 3.0V	2.8	3.0	3.1	V
Pre-charge voltage hysteresis				88		mV
Recharge threshold below V_{BATT_REG}	V_{RECH}	REG04h, bit[0] = 0	130	170	210	mV
		REG04h, bit[0] = 1	270	320	370	
Thermal Protection						
Thermal shutdown rising threshold (5)	T_{J_SHDN}			150		°C
Thermal shutdown hysteresis (5)				20		°C
NTC output current	I_{NTC}	CEB = 0, V_{NTC} = 3V	-100	0	100	nA
NTC cold temp rising threshold	V_{COLD}	As a percentage of V_{IN}	64	66	68	%
NTC cold temp rising threshold hysteresis				28		mV
NTC hot temp falling threshold	V_{HOT}	As a percentage of V_{IN}	33	35	37	%
NTC hot temp falling threshold hysteresis				65		mV
Logic I/O Pin Characteristics (5)						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface (SDA, SCL)						
Input high threshold level	V_{IH}	V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level	V_{IL}	V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level	V_{OL}	I_{SINK} = 5mA			0.4	V
I²C clock frequency	F_{SCL}				400	kHz
Digital Clock and Watchdog Timer						
Digital clock 2	F_{DIG2}			32		kHz
Watchdog timer	t_{WDT}	Programmable (REG05h, bits[5:4] = 11)	140	160	180	s
Safety timer	t_{ST}	Programmable (REG05h, bits[2:1] = 00), t_{ST} = 3hrs	2.7	3.0	3.3	hrs
		Programmable (REG05h, bits[2:1] = 01), t_{ST} = 5hrs	4.5	5.0	5.5	
		Programmable (REG05h, bits[2:1] = 10), t_{ST} = 8hrs	7.2	8.0	8.8	
		Programmable (REG05h, bits[2:1] = 11), t_{ST} = 12hrs	10.8	12.0	13.2	

Note:

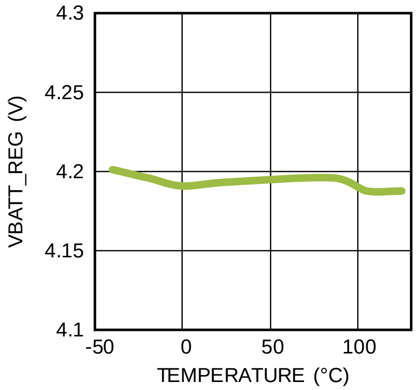
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

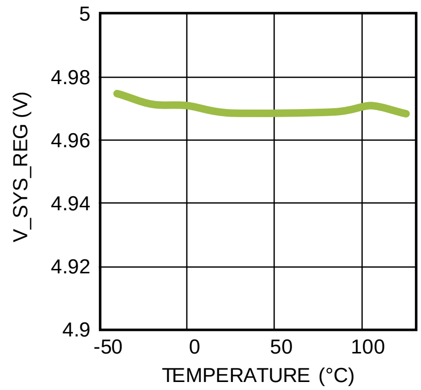
V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

Battery Regulation Voltage vs. Temperature

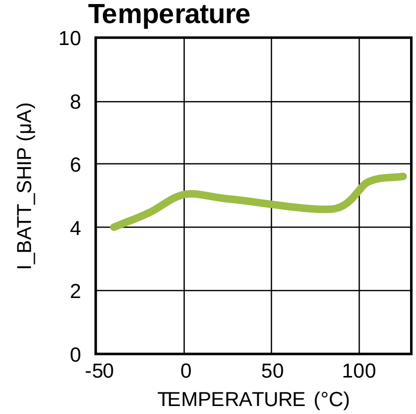
V_{BATT_REG}=4.2V



System Reguation Voltage vs. Temperature

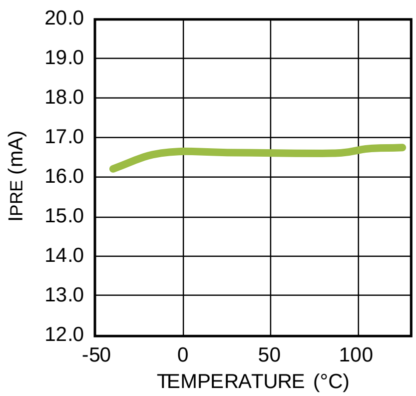


Battery Current under Shipping Mode vs. Temperature



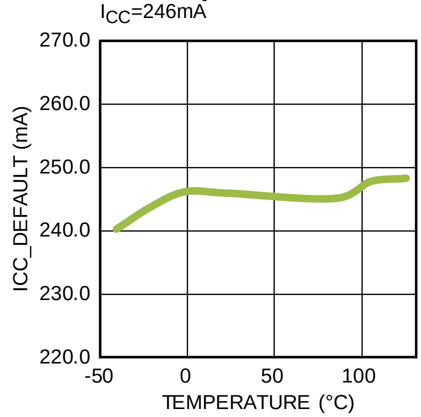
Pre-Charge Current vs. Temperature

I_{PRE}=20mA



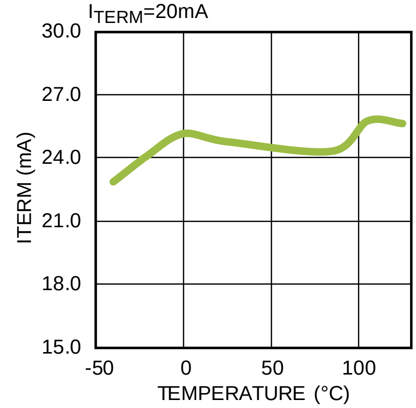
Fast Charge Current vs. Temperature

I_{CC}=246mA

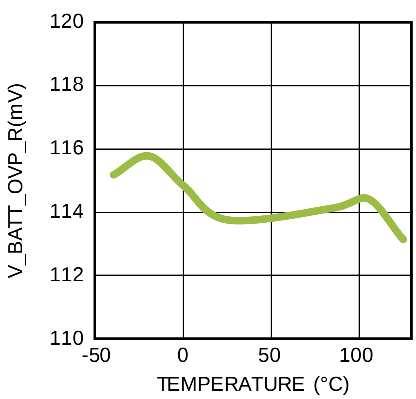


Battery Termination Current vs. Temperature

I_{TERM}=20mA

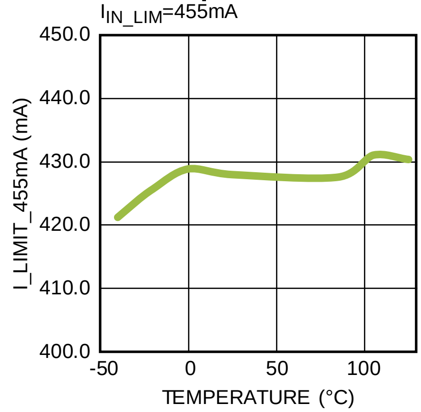


Battery OVP Voltage vs. Temperature



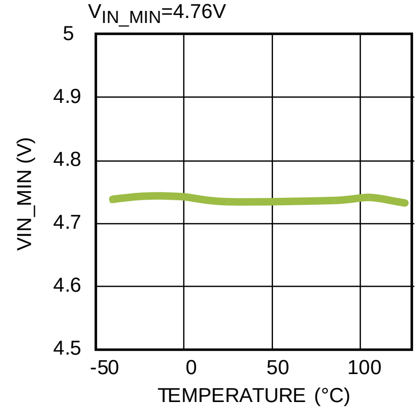
I_Limit_455mA vs. Temperature

I_{IN_LIM}=455mA



Input Regulation Voltage vs. Temperature

V_{IN_MIN}=4.76V

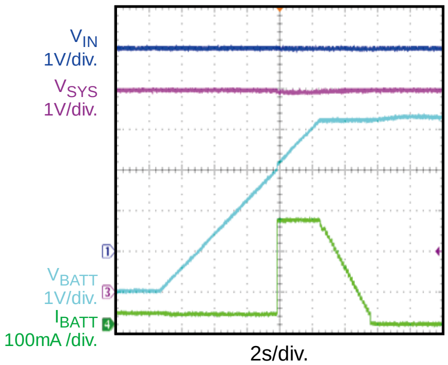


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

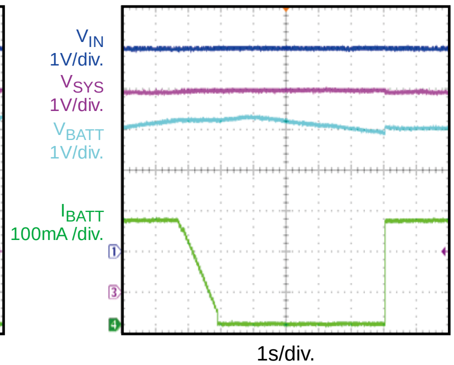
Battery Charge Curve

I_{SYS}=0A



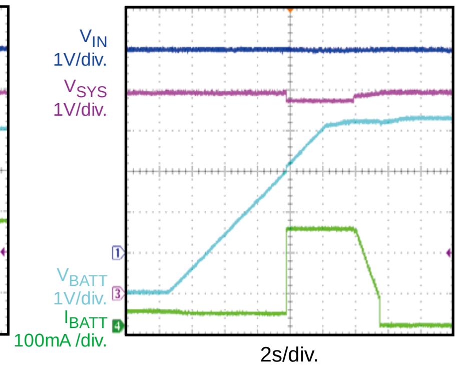
Auto-Recharge

I_{SYS}=0A



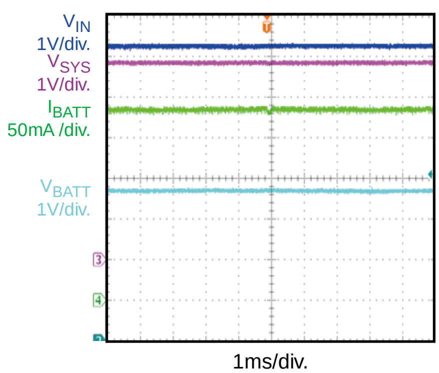
Battery Charge Curve

I_{SYS}=200mA



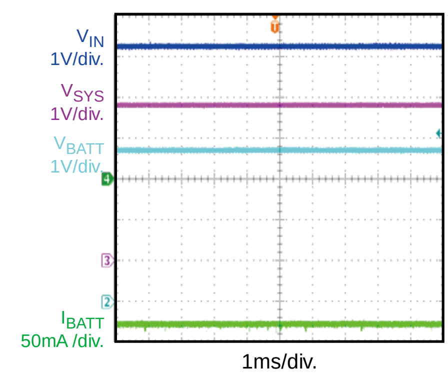
CC Charge Steady State

V_{BATT}=3.7V, I_{SYS}=200mA



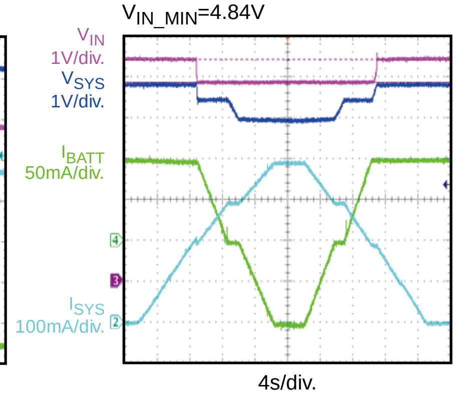
Supplement Mode Steady State

V_{BATT}=3.7V, I_{SYS}=600mA



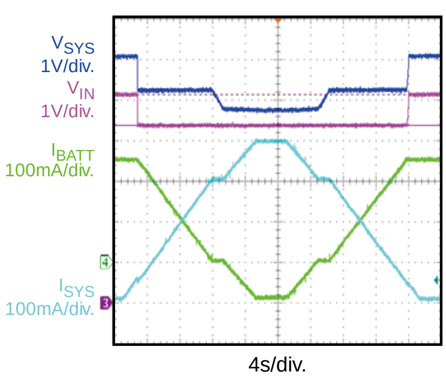
Input Voltage Regulation based PPM

V_{IN}=5V/300mA, V_{BATT}=4.2V, V_{IN_MIN}=4.84V



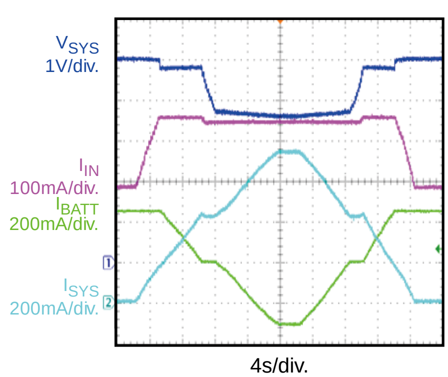
Input Voltage Regulation based PPM

V_{IN}=5V/300mA, V_{BATT}=3.7V



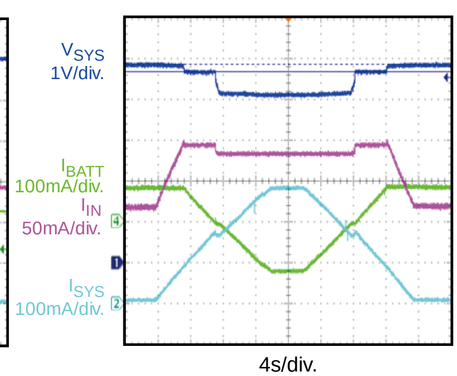
Input Current Limit based PPM

V_{BATT}=3.7V



Input Current Limit based PPM

I_{IN_LIM}=175mA

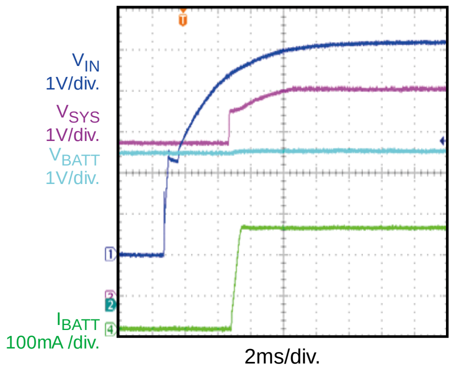


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

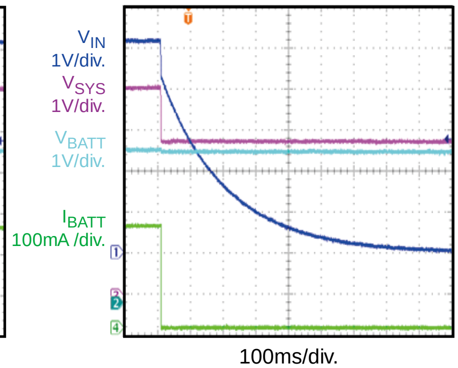
Power On

V_{BATT}=3.7V, I_{SYS}=0A



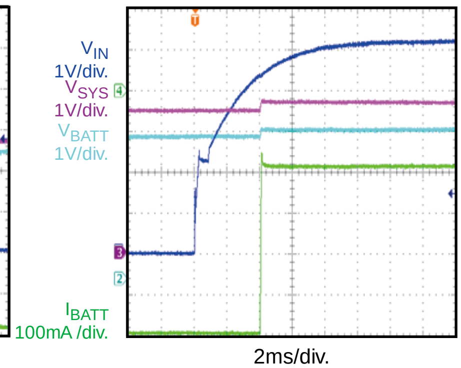
Power Off

V_{BATT}=3.7V, I_{SYS}=0A



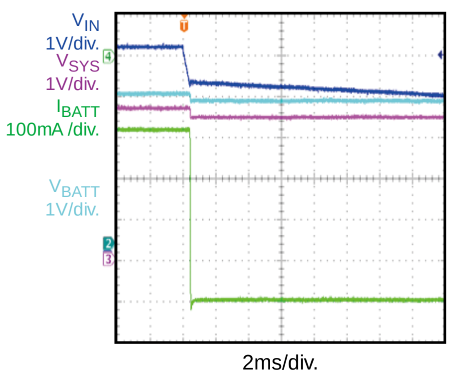
Power On
@ Supplement Mode

V_{BATT}=3.7V, I_{SYS}=600mA



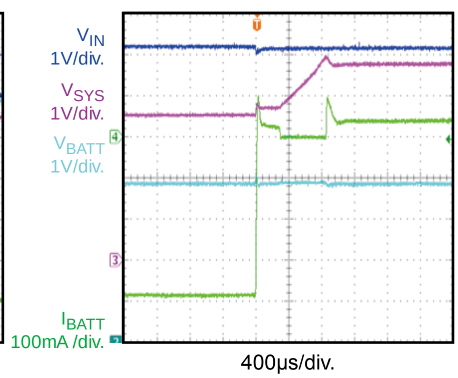
Power Off
@ Supplement Mode

V_{BATT}=3.7V, I_{SYS}=600mA



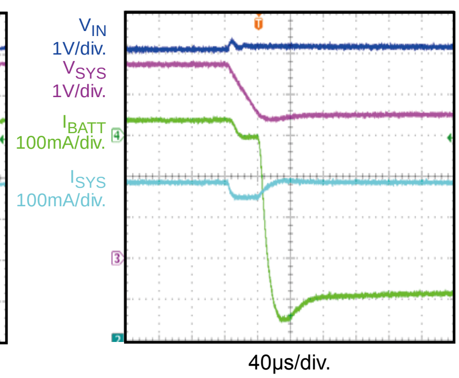
EN On
@ Input Current Limit Based PPM

V_{BATT}=3.7V, I_{SYS}=400mA



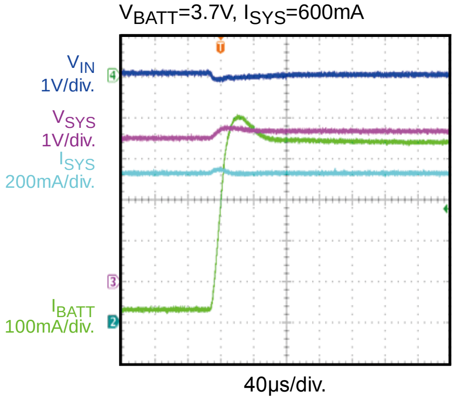
EN Off
@ Input Current Limit Based PPM

V_{BATT}=3.7V, I_{SYS}=400mA



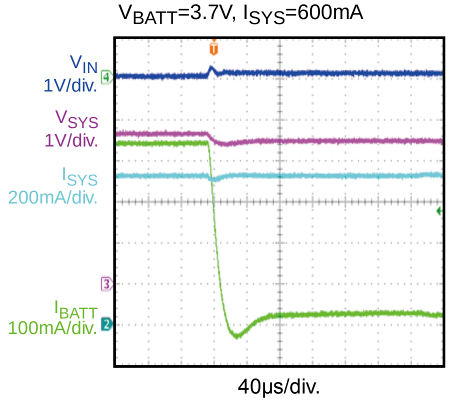
EN On
@ Supplement Mode

V_{BATT}=3.7V, I_{SYS}=600mA



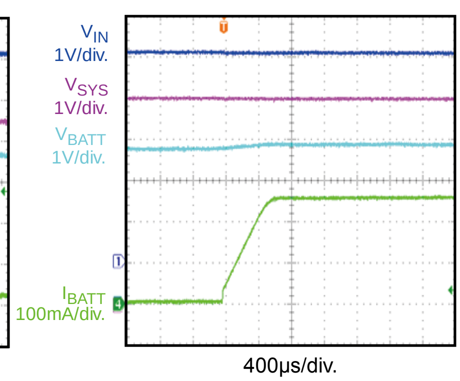
EN Off
@ Supplement Mode

V_{BATT}=3.7V, I_{SYS}=600mA



Charge On

V_{BATT}=3.7V, I_{SYS}=0A

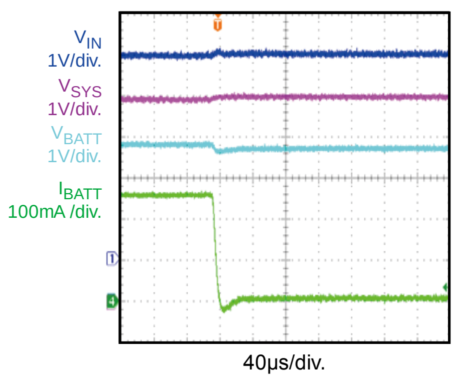


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_A = 25°C, I_{IN_LIM} = 455mA, I_{CC} = 246mA, V_{IN_MIN} = 4.76V, unless otherwise noted.

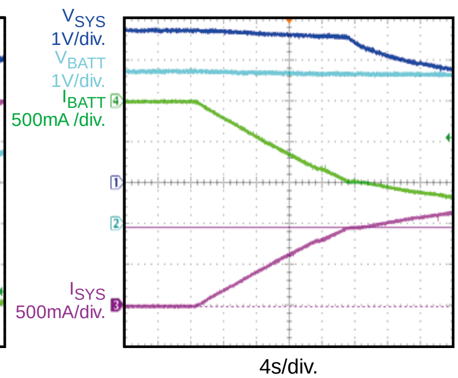
Charge Off

V_{BATT}=3.7V, I_{SYS}=0A



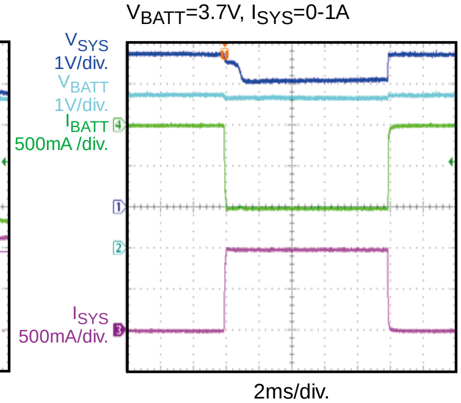
Adding Load @ Discharge Mode

V_{BATT}=3.7V



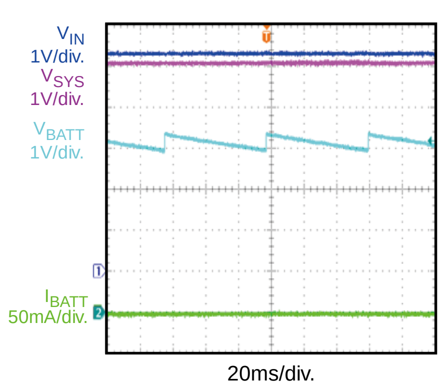
Load Transient @ Discharge Mode

V_{BATT}=3.7V, I_{SYS}=0-1A



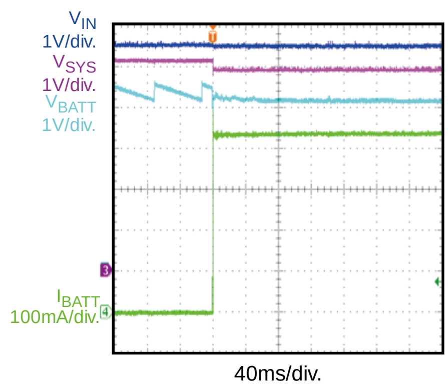
BATT Float Operation

I_{SYS}=0A



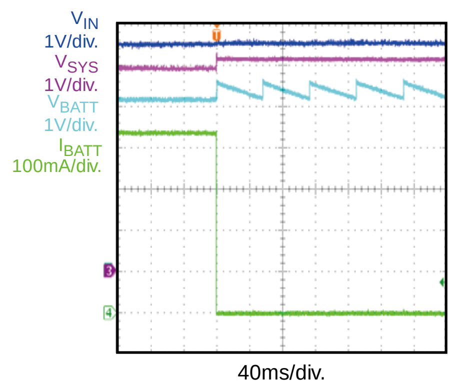
BATT Insertion

V_{BATT}=3.7V, I_{SYS}=0A



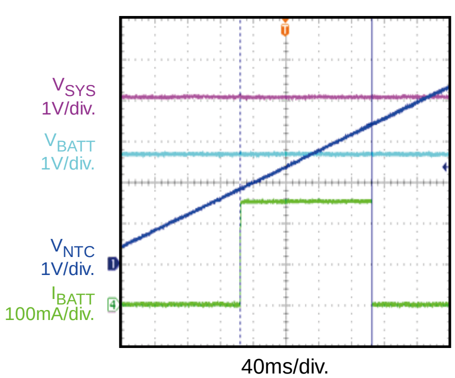
BATT Removal

V_{BATT}=3.7V, I_{SYS}=0A



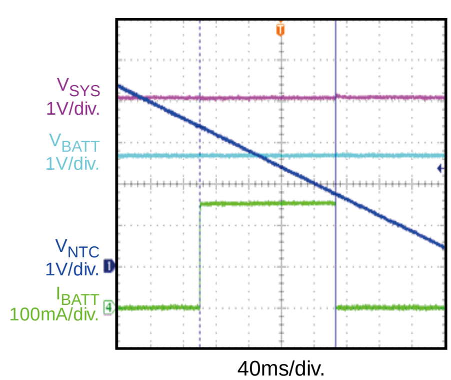
NTC On/Off

V_{BATT}=3.7V, I_{SYS}=0A



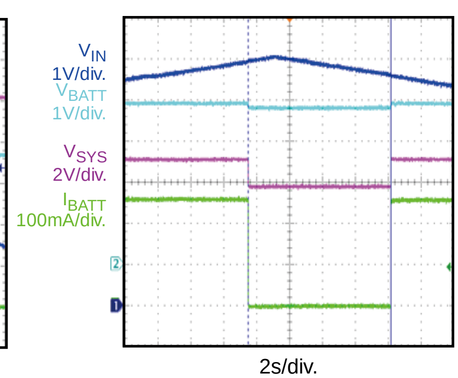
NTC On/Off

V_{BATT}=3.7V, I_{SYS}=0A



V_{IN} OVP Operation

V_{BATT}=3.7V, I_{SYS}=0A



FUNCTIONAL BLOCK DIAGRAM

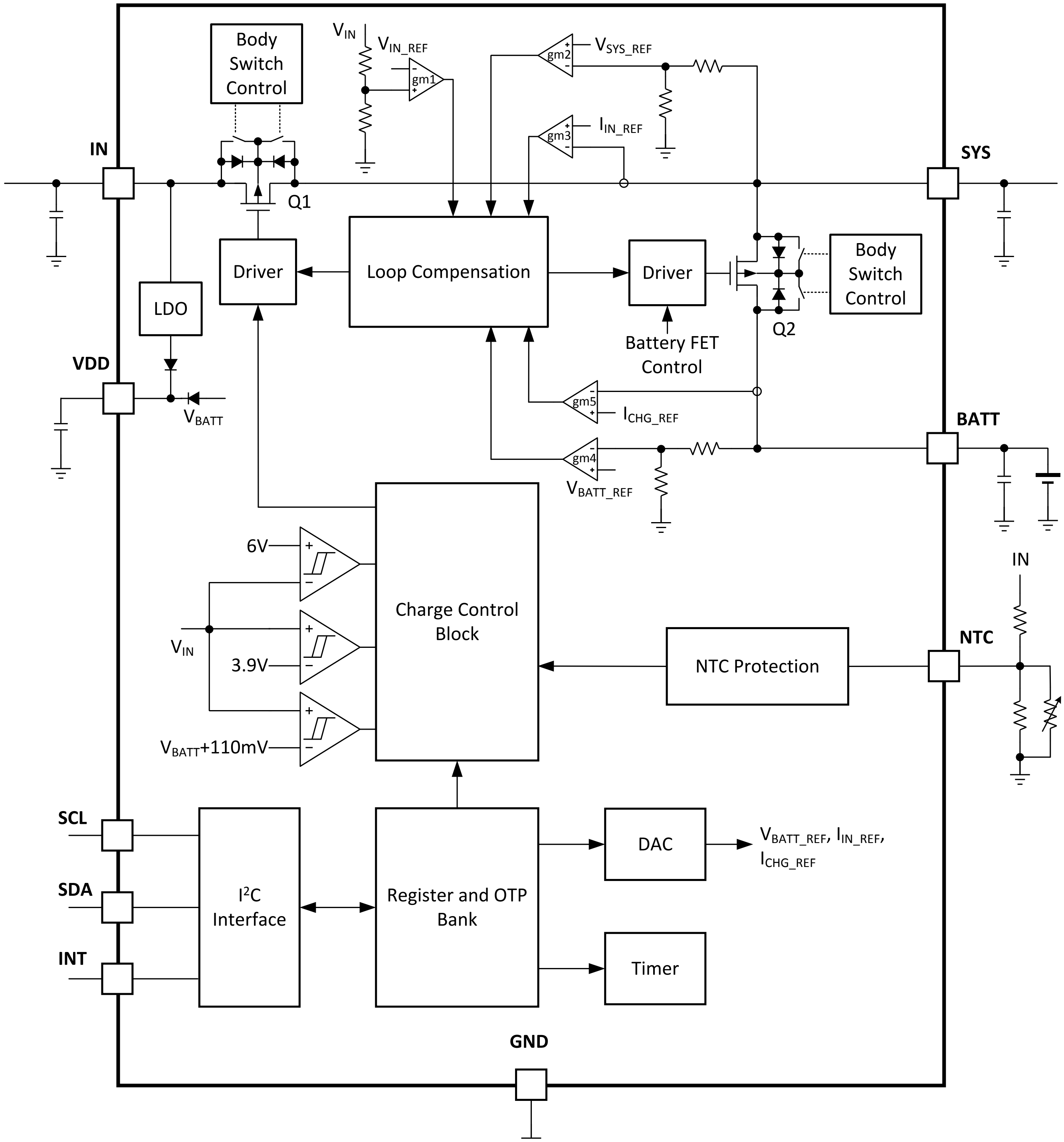


Figure 1: Functional Block Diagram

OPERATION

The MP2660 is an I²C-controlled, single-cell, Li-ion or Li-polymer battery charger with complete power path management. The full charge function features constant current pre-charge (PRE.C), constant current fast-charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. If the power source cannot supply enough current to the system load and to charge the battery, then the charge current will be reduced until it is necessary for the battery to supplement system power.

The IC integrates a 300mΩ LDO FET between IN and SYS and a 100mΩ battery FET between SYS and BATT.

During charging mode, the on-chip 100mΩ battery FET works as a full-featured linear charger with pre-charging, CC and CV charging, charge termination, auto-recharging, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I²C interface. The IC limits the charge current when the die temperature exceeds the programmable thermal regulation threshold (120°C default).

When the input power is not sufficient for powering the system load, the MP2660 enters supplement mode by fully turning on the 100mΩ battery FET. When the input is removed, the 100mΩ battery FET is also fully turned on, allowing the battery to power up the system.

When the system load is satisfied, the remaining current is used to charge the battery. The IC reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity or if either the input current or voltage loops are active.

Figure 2 shows the power path management structure for the MP2660.

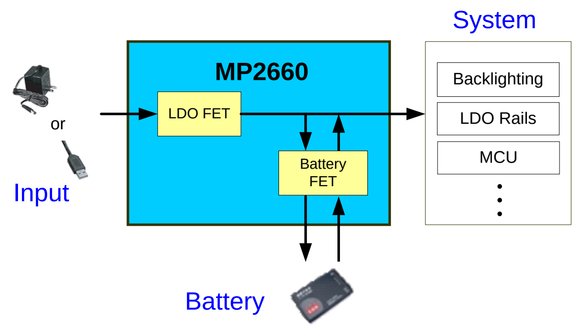


Figure 2: Power Path Management Structure

Power Supply

The internal bias circuit of the IC is powered from the higher voltage of IN or BATT. When IN or BATT rises above the respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and the battery FET driver are active. The I²C interface is ready for communication and all registers are reset to the default value. The host can access all registers.

Input OVP and UVLO

The MP2660 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once the input voltage transitions out of the normal input voltage range, the Q1 FET is turned off immediately.

When the input voltage is identified as a good source, a 200µs immunity timer is active. If the input power is still sufficient when the 200µs timer expires, the system starts up. Otherwise, Q1 remains off (see Figure 3).

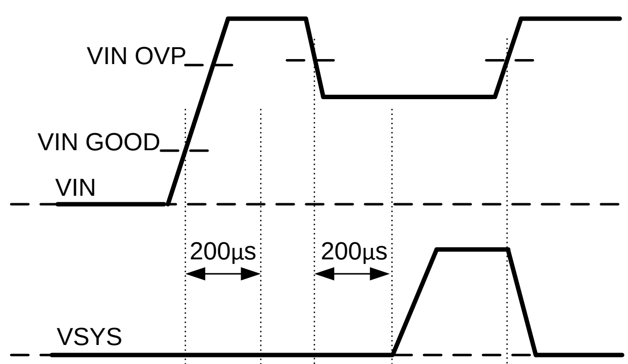


Figure 3: Input Power Detection Operation

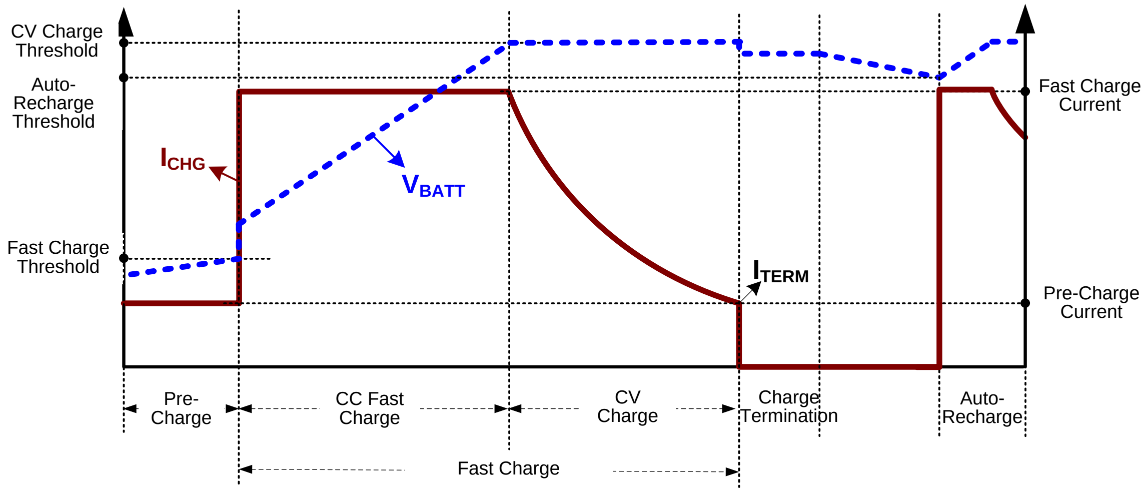


Figure 4: Battery Charge Profile

Power Path Management (PPM)

The IC employs a direct power path structure with the battery FET decoupling the system from the battery, which allows for separate control between the system and the battery. The system is given the priority to start up even with a deeply discharged or missed battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDO FET.

As shown in Figure 2, the direct power structure is composed of a frond-end LDO FET between IN and SYS pin and a battery FET between SYS and BATT pin.

The input LDO (using an LDO FET) provides power to the system, which drives the system load directly and charges the battery through the battery FET.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDO FET is fully on in drop-out with an input current limit.

Battery Charge Profile

The IC provides three main charging phases: pre-charge, constant-current charge, and constant-voltage charge (see Figure 4).

1. Phase 1 (constant-current pre-charge): The IC is able to safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to the fast charge threshold (V_{BATT_PRE}). The pre-charge current is programmable via REG03h, bits[1:0]. If V_{BATT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle is stopped, and a corresponding timeout fault signal is asserted.
2. Phase 2 (constant-current fast charge): When the battery voltage exceeds V_{BATT_PRE}, the IC enters a constant-current charge (fast charge) phase. The fast charge current is programmable via REG02h, bits[4:0].
3. Phase 3 (constant-voltage charge): When the battery voltage rises to the pre-programmable charge full voltage (V_{BATT_REG}) set via REG04h, bits[7:2], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.

The end of charge (EOC) current threshold (I_{TERM}) value setting is shown in Table 2.

Table 2: I_{TERM} Value Table

REG02h, bit[4]	I_{TERM} Value
0 ($I_{CC\_SETTING} \leq$ 263mA)	100% x I_{PRE}
1 ($I_{CC\_SETTING} \geq$ 280mA)	200% x I_{PRE}

Once the charge current reaches the EOC current threshold (I_{TERM}) and the CV loop is still dominated, the IC has three possible actions after a 500µs delay depending on the settings of EN_TERM (REG05h, bit[6]) and TERM_TMR (REG05h, bit[0]):

1. EN_TERM = 1, TERM_TMR = 0, (default spec): The IC terminates the charge and changes the charge status to "charge done."
2. EN_TERM = 1, TERM_TMR = 1: The IC changes the charge status to "charge done," but the charge current continues tapering off until it reaches 0.
3. EN_TERM = 0, TERM_TMR = x: The charge status stays at "charge," but the charge current continues tapering off until it reaches 0.

During the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation or thermal regulation. Refer to the Input Current- and Input Voltage-Based Power Management section for details.

If I_{TERM} is not reached before the safety charge timer expires (*see Safety Timer section*), the charge cycle is ceased and corresponding timeout fault signal is asserted.

The following conditions can start a new charge cycle:

- The input power is recycled
- Battery charging is enabled by the I²C
- Auto-recharge kicks in

However, these conditions can stop a charge cycle:

- Thermistor fault at NTC
- Safety timer fault
- Battery over voltage
- Battery FET is forced to turn off

Automatic Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to the system consumption or a self-discharge. When the battery voltage is discharged below the recharge threshold, and V_{IN} is still in the operating range, the IC begins another new charging cycle automatically without the requirement of restarting a charging cycle manually. The auto-recharge function is valid only when EN_TERM = 1 and TERM_TMR = 0.

Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage limit about 120mV higher than V_{BATT_REG}. When the battery over-voltage event occurs, the IC suspends the charging immediately and asserts a fault.

Input Current- and Input Voltage-Based Power Management

To meet the input source (usually USB) maximum current limit specification, the IC uses an input current-based power management by monitoring the input current continuously. The total input current limit can be programmable via the I²C to prevent the input source from overloading.

If the pre-set input current limit is higher than the rating of the input source, back-up input voltage-based power management also works to prevent the input source from being overloaded. If either the input current limit or the input voltage regulation is reached, the Q1 FET between IN and SYS is regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to the minimum value of 4.8V or V_{IN} - 160mV, the charge current is reduced to prevent the system voltage from dropping further.

The voltage-based dynamic power management (DPM) regulates the input voltage to V_{IN_MIN} when the load is over the input power capacity. V_{IN_MIN} set via the I²C should be at least 400mV higher than V_{BATT_REG} to ensure the stable operation of the regulator.

Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero and the input source is still overloaded due to a heavy system load, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the IC enters battery supplement mode.

When the system voltage is 30mV below the battery voltage, the ideal diode mode is enabled. The battery FET is regulated to maintain V_{BATT} - V_{SYS} at 22.5mV. If the voltage drop of the battery FET (I_{DSCHG} x R_{ON_BATT}) is higher than 22.5mV, the battery FET is fully turned on to keep the ideal forward voltage. When the system load decreases and V_{SYS} is higher than V_{BATT} + 20mV, ideal diode mode is disabled.

Figure 5 shows the dynamic power management and battery supplement mode operation profile.

When V_{IN} is not available, the IC operates in discharge mode, and the battery FET is always fully on to reduce loss.

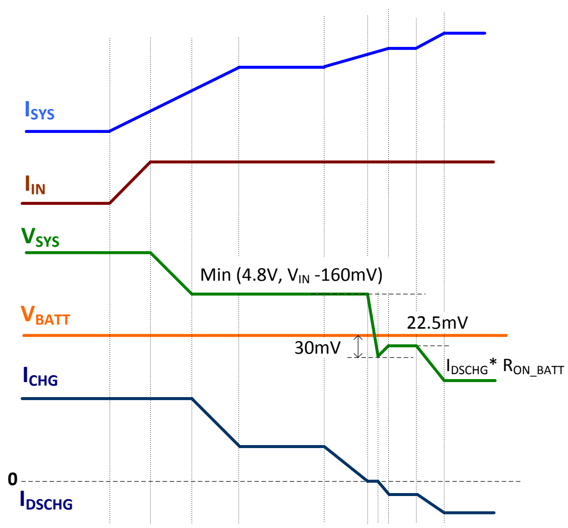


Figure 5: Dynamic Power Management and Battery Supplement Operation Profile

Battery Charge Full Voltage

The battery voltage for the constant voltage regulation phase is V_{BATT_REG}. When V_{BATT_REG} is 4.2V, it has a ±0.5% accuracy over the ambient temperature range of 0°C to +50°C. When the battery is removed, the BATT voltage is between V_{BATT_REG} - V_{RECH} and V_{BATT_REG}.

Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and prevent the chip from overheating. When the internal junction temperature reaches the pre-set limit of T_{J_REG} (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via REG06h, bits[1:0]. When the junction temperature reaches 150°C, both Q1 and Q2 are turned off.

Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment of the chip. A resistor with an appropriate value should be connected from IN to NTC, and the thermistor should be connected from NTC to ground. The voltage on NTC is determined by the resistor divider, whose divide ratio depends on the battery temperature. The IC sets a pre-determined upper and lower bound of the divide ratio internally for NTC cold and NTC hot.

The NTC function works in charge mode only. Once the NTC voltage falls out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging and reports it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

Safety Timer

The IC provides both a pre-charge and a fast-charge safety timer to prevent extended charging cycles due to abnormal battery conditions. If the battery voltage drops below V_{BATT_PRE}, then the safety timer is one hour. The fast-charge safety timer begins once the battery enters fast-charge mode. Figure 4 on page 16 shows the fast-charge timer's battery profile. The fast-charge safety timer can be programmed via the I^2C. The safety timer feature can also be disabled via the I^2C.

The following actions can restart the safety timer:

- A new charge cycle is initiated
- Charge enable toggling
- Hi-Z disable toggling

During power path management (PPM), the charge current is reduced due to an insufficient input power (input current limit, input voltage limit). The timer period can be extended 2 times by setting TMR2X_EN (REG06h, bit[6]) to 1.

- TMR2X_EN = 1: 2x extended safety timer enabled during PPM
- TMR2X_EN = 0 (default): 2x extended safety timer disabled during PPM

This feature avoids a false trigger indication for a bad battery that delivers a small charge current to the battery as a result of the insufficient input power.

Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset, the IC starts up in the watchdog timer expiration state or default mode. All registers are in the default settings.

Any write to the IC switches it into host mode. All charge parameters are programmable. If the watchdog timer (REG05h, bits[5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to REG01h, bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled by the host control. When there is no V_{IN}, the watchdog timer is suspended.

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no V_{IN}
- Register reset REG01h, bit[7] is reset

Battery Discharge Function

If the battery is connected and the input source is missing, the battery FET is fully on when V_{BATT} is above the V_{BATT_UVLO} threshold. The 100mΩ battery FET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11µA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once I_{BATT} exceeds the programmable discharge current limit (default 1.0A), the battery FET is regulated to limit the discharge current.

Similarly, when the battery voltage falls below the programmable V_{BATT_UVLO} threshold (default 2.8V), the battery FET is turned off to prevent over-discharge.

System Short-Circuit Protection (SCP)

The MP2660 features SYS node short-circuit protection (SCP) for both the IN to SYS path and the BATT to SYS path.

The system voltage is monitored continuously. Once V_{SYS} is lower than 1.5V, the over-current protection threshold for the BATT to SYS path is limited to 2A (fast off). For details, please refer to the flow chart in Figure 19.

If the system short-circuit occurs when both the input and the battery are present, the protection mechanism of both paths work, with the faster one (the IN_to_SYS path protection mechanism) dominating the hiccup operation.

Interrupt to Host (INT)

The IC also has an alert mechanism, which can output an interrupt signal via INT pin to notifyces the system ofn the operation by outputting a 256µs low-state INT pulse. Any of the below events can will trigger the INT output:

- Good input source detected(PG_STAT)
- Charge completed
- Charging status change
- Any fault in REG08h (watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in REG08h. After the IC exits the fault state, the fault bit can be released to 0 after the host reads REG08h.

Note that the INT needs the external pull up resistor for its open-drain connection. Suggest the resistance not lower than 100kΩ.

Battery Disconnection Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system to shipping mode, in stock mode, or to system reset mode for different applications (shown in Table3).

1. Shipping Mode:

   Entering shipping mode: The register bit FET_DIS (REG06h, bit[5]), makes the IC enter shipping mode. During normal operation, the battery FET is turned on (the bit is 0). If this bit is set to 1 through the I²C, the battery FET is turned off, and the MP2660 enters shipping mode.

   The FET_DIS bit is reset to 0 automatically after the battery FET is turned on.

   Exiting shipping mode: The IC can exit shipping mode by pulling INT down for a very short time (>500ms).

2. Reset Mode:

   The IC can use INT to cut off the path from the battery to the system under the condition needed to reset the system manually.

   If the battery FET is on, once the logic at INT is set to low for more than 8s, the battery is disconnected from the system by turning off the battery FET. The battery can be connected in and out of the system by controlling INT (see Figure 6).

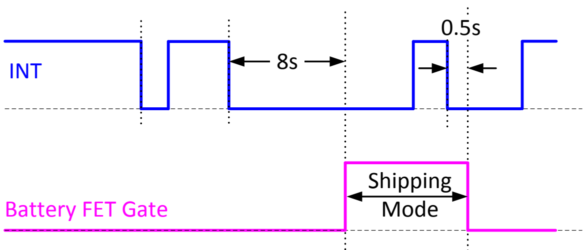


Figure 6: Disconnection Function Operation Profile

Table 3: Battery Disconnection Control

<table>
<tr><th rowspan="3">FET On/Off Change By Control</th><th colspan="2">INT Pin</th></tr>
<tr><th>H to L for 8s</th><th>H to L for 500ms</th></tr>
<tr><th>Reset Mode</th><th>Exit Shipping Mode</th></tr>
<tr><td>LDO FET</td><td>x</td><td>x</td></tr>
<tr><td>Battery FET (charging)</td><td>OFF</td><td>ON</td></tr>
<tr><td>Battery FET (discharging)</td><td>OFF</td><td>ON</td></tr>
</table>

I²C Interface

The MP2660's I²C interface allows a user to flexibly configure the charging parameters. It also provides instant device status reporting. The I²C is a 2-wire serial interface with two bus lines: a serial data line (SDA) and a serial clock line (SCL). Both the SDA and SCL lines are open drains. Do not connect the SDA and SCL lines to the positive supply voltage via a pull-up resistor.

The IC operates as a slave device, receiving control inputs from the master device (e.g. a microcontroller). The SCL line is driven by the master device. The I²C interface supports both standard mode (up to 100kbit/s) and fast mode (up to 400kbit/s).

All transactions begin with a start (S) condition and are terminated by a stop (P) condition. Start and stop conditions are generated by the master. A start condition is defined as a high to low transition on the SDA line while the SCL line is high. A stop condition is defined as a low to high transition on the SDA line while the SCL line is high.

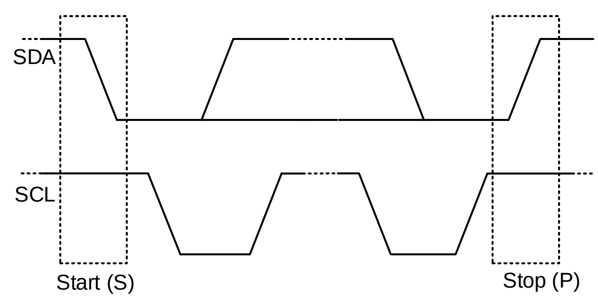


Figure 7: Start (S) and Stop (P) Conditions

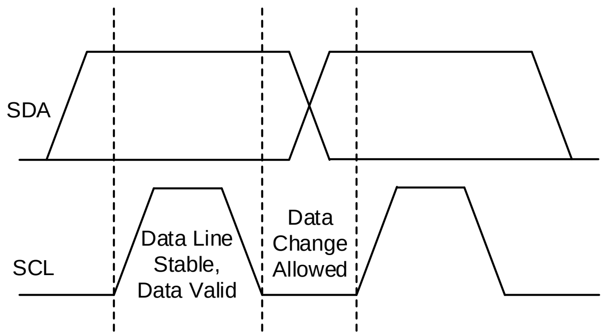


Figure 8: I²C Bus Bit Transfer

For data validity, the SDA line data should remain stable during the high period of the clock. The SDA line's high/low state can change while the SCL line's clock signal is low. Each byte on the SDA line should be 8 bits long. The number of bytes transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB).

Each byte is followed by an acknowledge (ACK) bit generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as the transmitter releasing the SDA line during the ACK clock pulse, so that the SDA line can be pulled low by the receiver and remain low during the high period of the 9th clock.

The not acknowledge (NACK) signal is defined as the SDA line remaining high during the 9th clock. Then the master generates either a stop (P) to abort the transfer or a repeated start (S) to start a new transfer.

After the start signal, a slave address is sent. This address is 7-bits long, and is followed by an 8th bit as a data direction bit (R/W). A 0 indicates a write (W) signal transmission, while a 1 indicates a read (R) signal data request. Figure 9 shows the address bit arrangement.

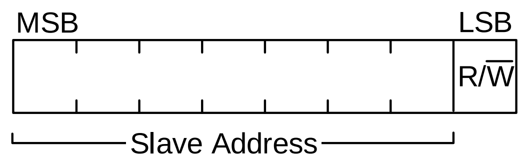


Figure 9: 7-Bit Addressing

See Figures 10–14 for more details on the R/W signal sequences.

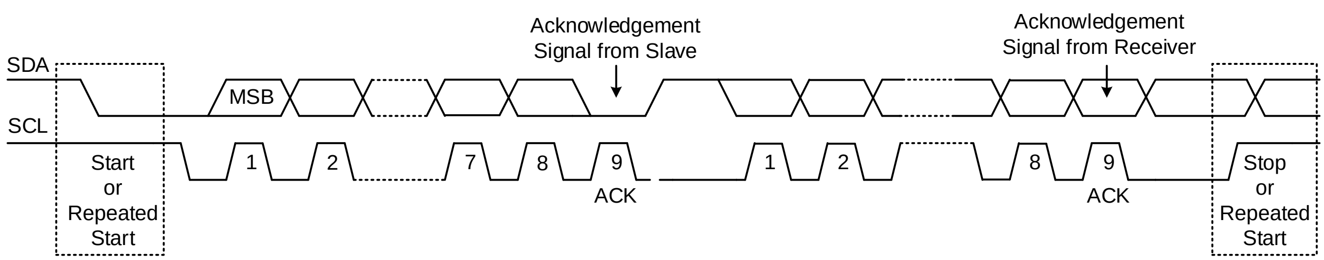


Figure 10: I²C Bus Data Transfer

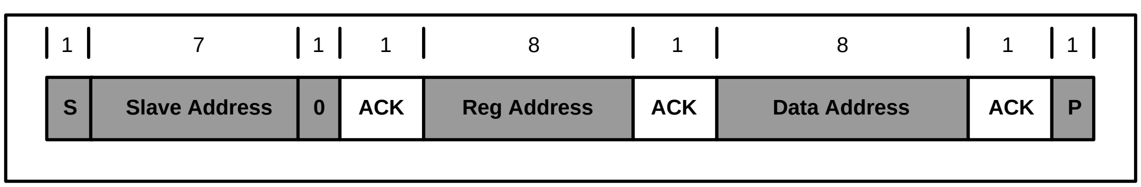


Figure 11: Single Write

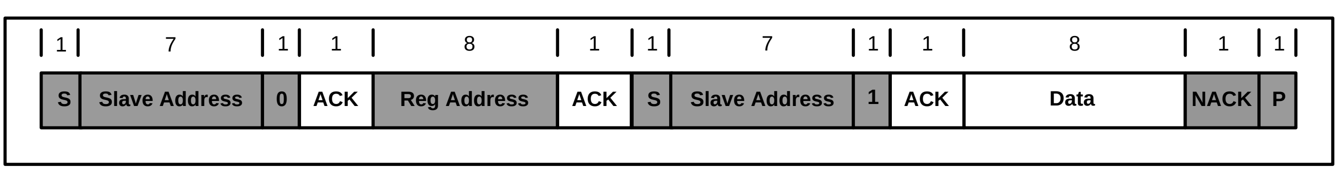


Figure 12: Single Read

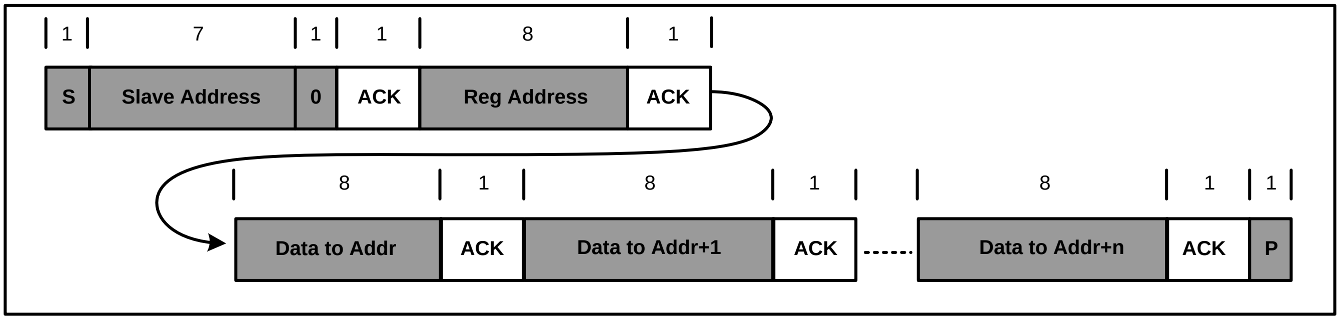


Figure 13: Multi-Write

Figure 14: Multi-Read

I²C REGISTER MAP

IC Address: 09h

Input Source Control Register/Address: 00h (Default: 0100 1111)

Bit	Symbol	Description	Read/Write	Default
Bit 7	EN_HIZ (6)	0: Disable 1: Enable	Read/Write	Disable (0)
Input Voltage Regulation				
Bit 6	V_{IN_MIN} [3]	640mV	Read/Write	Offset: 3.88V Range: 3.88V - 5.08V Default: 4.60V (1001)
Bit 5	V_{IN_MIN} [2]	320mV		
Bit 4	V_{IN_MIN} [1]	160mV		
Bit 3	V_{IN_MIN} [0]	80mV		
Input Current Limit				
Bit 2	I_{IN_LIM} [2]	000: 85mA 001: 130mA 010: 175mA 011: 220mA 100: 265mA 101: 310mA 110: 355mA 111: 455mA	Read/Write	455mA (111)
Bit 1	I_{IN_LIM} [1]			
Bit 0	I_{IN_LIM} [0]			

Note:

6) This bit only controls the on and off of the LDO FET.

Power-On Configuration Register / Address: 01h (Default: 0000 0100)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Register reset	0: Keep current setting 1: Reset	Read/Write	Keep current register setting (0)
Bit 6	I²C watchdog timer reset	0: Normal 1: Reset	Read/Write	Normal (0)
Bit 5	Reserved	Reserved	NA	
Bit 4	Reserved	Reserved	NA	
Charger Configuration				
Bit 3	CEB	0: Charge enable 1: Charge disable	Read/Write	Charge enable(0)
Battery UVLO Threshold				
Bit 2	V_{BATT_UVLO} [2]	0.4V	Read/Write	Offset: 2.4V Range: 2.4V - 3.1V Default: 2.8V (100)
Bit 1	V_{BATT_UVLO} [1]	0.2V		
Bit 0	V_{BATT_UVLO} [0]	0.1V		

I²C REGISTER MAP *(continued)*

Charge Current Control Register/ Address: 02h (Default: 0000 1110)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved	Reserved	NA	
Bit 6	Reserved	Reserved	NA	
Bit 5	Reserved	Reserved	NA	
Charge Current Setting				
Bit 4	I_{CC} [4]	272mA	Read/Write	Offset: 8mA Range: 8mA - 535mA Default: 246mA (01110)
Bit 3	I_{CC} [3]	136mA		
Bit 2	I_{CC} [2]	68mA		
Bit 1	I_{CC} [1]	34mA		
Bit 0	I_{CC} [0]	17mA		

Pre-Charge/ Termination Current/ Address: 03h (Default: 0100 1010)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved	Reserved	NA	
BATT to SYS Discharge Current Limit				
Bit 6	I_{DSCHG}[3]	800mA	Read/Write	Offset: 200mA Range: 200mA - 1.6A Default: 1.0A (1001)
Bit 5	I_{DSCHG} [2]	400mA		
Bit 4	I_{DSCHG} [1]	200mA		
Bit 3	I_{DSCHG} [0]	100mA		
Bit 2	Reserved	Reserved	NA	
Pre-Charge / Terminal Current				
Bit 1	I_{PRE} [1]	14mA	Read/Write	Offset: 6mA Range: 6mA - 27mA Default: 20mA (10)
Bit 0	I_{PRE} [0]	7mA		

I²C REGISTER MAP *(continued)*

Charge Voltage Control Register/ Address: 04h (Default: 1010 0011)

Bit	Symbol	Description	Read/Write	Default
Battery Regulation Voltage				
Bit 7	V_{BATT_REG} [5]	480mV	Read/Write	Offset: 3.60V Range: 3.60V - 4.545V Default: 4.2V (101000)
Bit 6	V_{BATT_REG} [4]	240mV		
Bit 5	V_{BATT_REG} [3]	120mV		
Bit 4	V_{BATT_REG} [2]	60mV		
Bit 3	V_{BATT_REG} [1]	30mV		
Bit 2	V_{BATT_REG} [0]	15mV		
Pre-Charge Threshold				
Bit 1	V_{BATT_PRE}	0: 2.8V 1: 3.0V	Read/Write	3.0V (1)
Battery Recharge Threshold (below V_{BATT_REG})				
Bit 0	V_{RECH}	0: 150mV 1: 300mV	Read/Write	300mV (1)

Charge Termination/Timer Control Register / Address: 05h (Default: 0100 1010)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved	Reserved	NA	
Termination Setting (control of the termination is allowed or not)				
Bit 6	EN_TERM	0: Disable 1: Enable	Read/Write	Enable (1)
I²C Watchdog Timer Limit				
Bit 5	WATCHDOG [1]	00: Disable timer 01: 40s 10: 80s 11: 160s	Read/Write	Disable timer (00)
Bit 4	WATCHDOG [0]			
Safety Timer Setting				
Bit 3	EN_TIMER	0: Disable 1: Enable	Read/Write	Enable timer (1)
Safety Timer for Fast Charging Cycle				
Bit 2	CHG_TMR [1]	00: 3hrs 01: 5hrs 10: 8hrs 11: 12hrs	Read/Write	5hrs (01)
Bit 1	CHG_TMR [0]			
Termination Timer Control (when TERM_TMR is enabled, the IC will not suspend the charge current after charge termination)				
Bit 0	TERM_TMR	0: Disable 1: Enable	Read/Write	Disable (0)

I²C REGISTER MAP *(continued)*

Miscellaneous Operation Control Register/ Address: 06h (Default: 0000 1011)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved	Reserved	NA	
Bit 6	TMR2X_EN	0: Disable 2X extended safety timer during PPM 1: Enable 2X extended safety timer during PPM	Read/Write	Disable (0)
Bit 5	FET_DIS (7)	0: Enable 1: Turn off	Read/Write	Enable (0)
Bit 4	Reserved	Reserved	NA	
Bit 3	EN_NTC	0: Disable 1: Enable	Read/Write	Enable (1)
Bit 2	Reserved	Reserved	NA	
Thermal Regulation Threshold				
Bit 1	T_{J_REG} [1]	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Read/Write	120°C (11)
Bit 0	T_{J_REG} [0]			

Note:

7) This bit only controls the turn off function of the battery FET, including charge and discharge.

System Status Register/ Address: 07h (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved	Reserved	NA	
Revision				
Bit 6	Rev [1]	Revision number	Read only	(00)
Bit 5	Rev [0]			
Bit 4	CHG_STAT [1]	00: Not charging 01: Pre-charge 10: Charge 11: Charge done	Read only	Not charging (00)
Bit 3	CHG_STAT [0]			
Bit 2	PPM_STAT	0: No PPM 1: In PPM	Read only	No PPM (0) (no power-path management happens)
Bit 1	PG_STAT	0: Power fail 1: Power good	Read only	Power fail (0)
Bit 0	THERM_STAT	0: No thermal regulation 1: In thermal regulation	Read only	No thermal regulation (0)

I²C REGISTER MAP *(continued)*

Fault Register/ Address: 08h (Default: 0000 0000)

Bit	Symbol	Description	Read/Write	Default
Bit 7	Reserved	Reserved	NA	
Bit 6	WATCHDOG_ FAULT	0: Normal 1: Watchdog timer expiration	Read only	Normal (0)
Bit 5	VIN_FAULT	0: Normal 1: Input fault (OVP or bad source)	Read only	Normal (0)
Bit 4	THEM_SD	0: Normal 1: Thermal shutdown	Read only	Normal (0)
Bit 3	BAT_FAULT	0: Normal 1: Battery OVP	Read only	Normal (0)
Bit 2	STMR_FAULT	0: Normal 1: Safety timer expiration	Read only	Normal (0)
Bit 1	Reserved	Reserved	NA	
Bit 0	Reserved	Reserved	NA	

ONE TIME PROGRAMMING MAP

<table>
<tr><th>#</th><th>Bit7</th><th>Bit6</th><th>Bit5</th><th>Bit4</th><th>Bit3</th><th>Bit2</th><th>Bit1</th><th>Bit0</th></tr>
<tr><td>0x02</td><td colspan="3">N/A</td><td colspan="5">I_{CC}: 8mA-535mA / 17mA step</td></tr>
<tr><td>0x03</td><td colspan="6">N/A</td><td colspan="2">I_{PRE}: 6mA-27mA / 7mA step</td></tr>
<tr><td>0x04</td><td colspan="6">V_{BATT_REG}: 3.60V-4.545V / 15mV step</td><td colspan="2">N/A</td></tr>
<tr><td>0x05</td><td colspan="2">N/A</td><td colspan="2">WATCHDOG</td><td colspan="4">N/A</td></tr>
</table>

ONE TIME PROGRAMMING DEFAULT

One Time Programmable Items	Default
I_{CC}	246mA
I_{PRE}	20mA
V_{BATT_REG}	4.2V
WATCHDOG	Disable Timer

STATE CONVERSION CHART

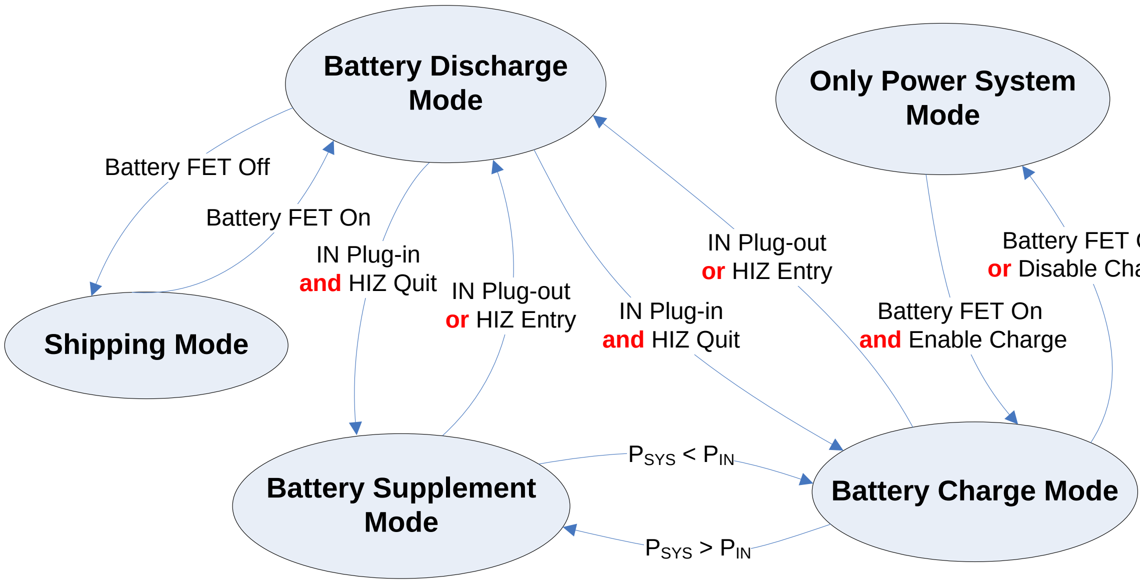


Figure 15: State Machine Conversion

CONTROL FLOW CHART

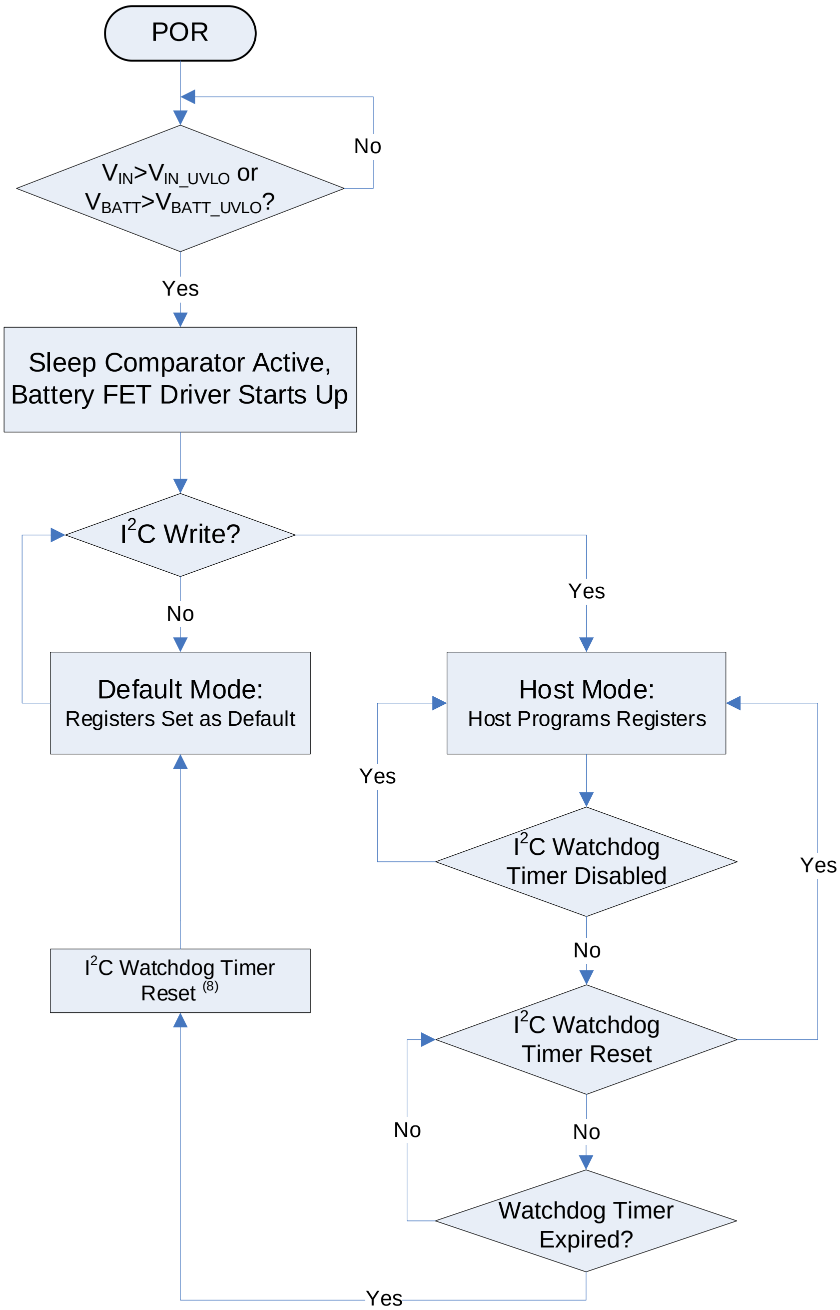


Figure 16: Default Mode and Host Mode Selection (9)

Notes:

8) Once the watchdog timer expires, the I²C watchdog timer reset is required, or the watchdog timer is not valid in the next cycle.
9) The watchdog timer is held when V_{IN} is not present.

CONTROL FLOW CHART *(continued)*

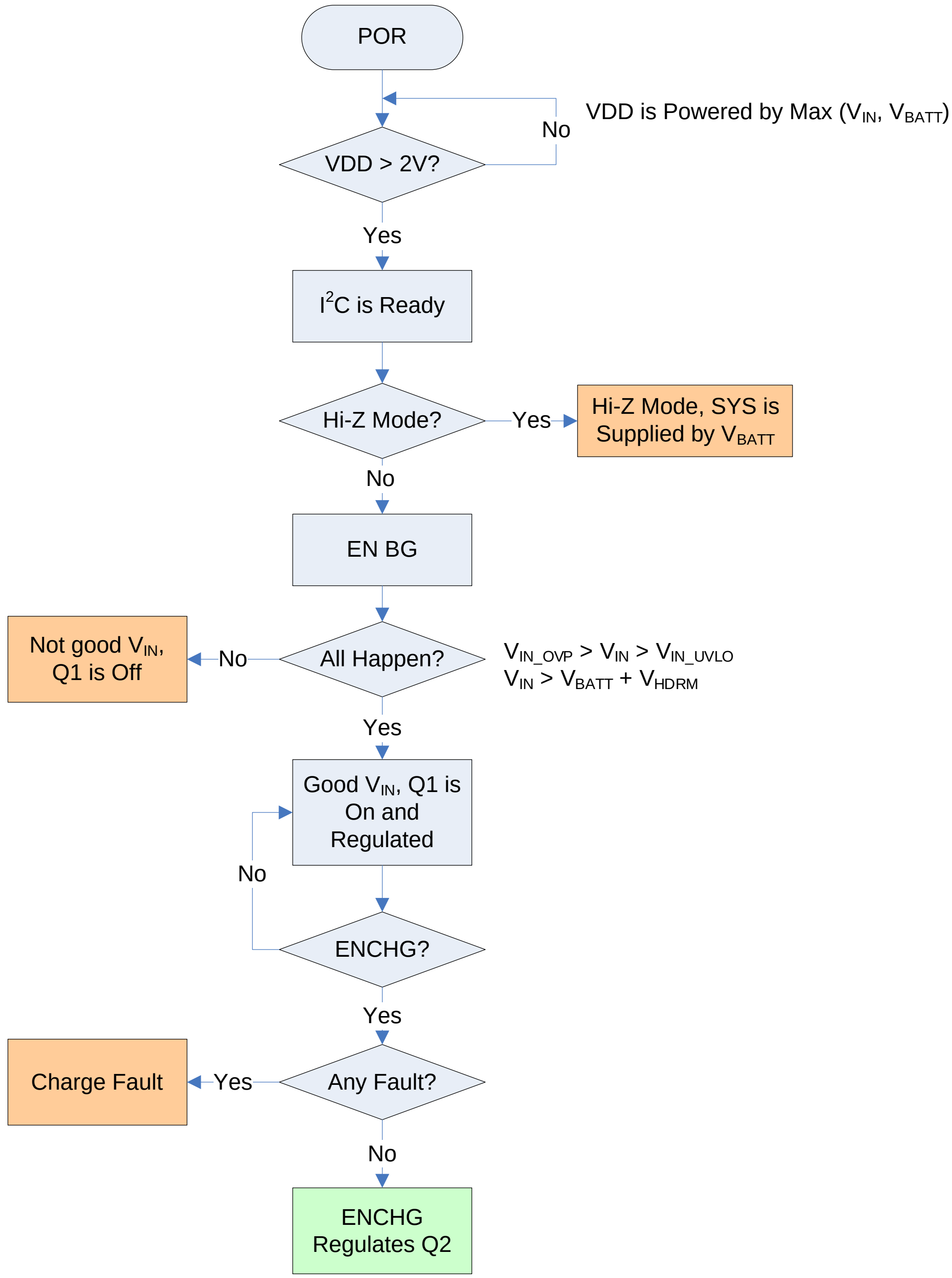


Figure 17: Input Power Start-Up Flow Chart

CONTROL FLOW CHART *(continued)*

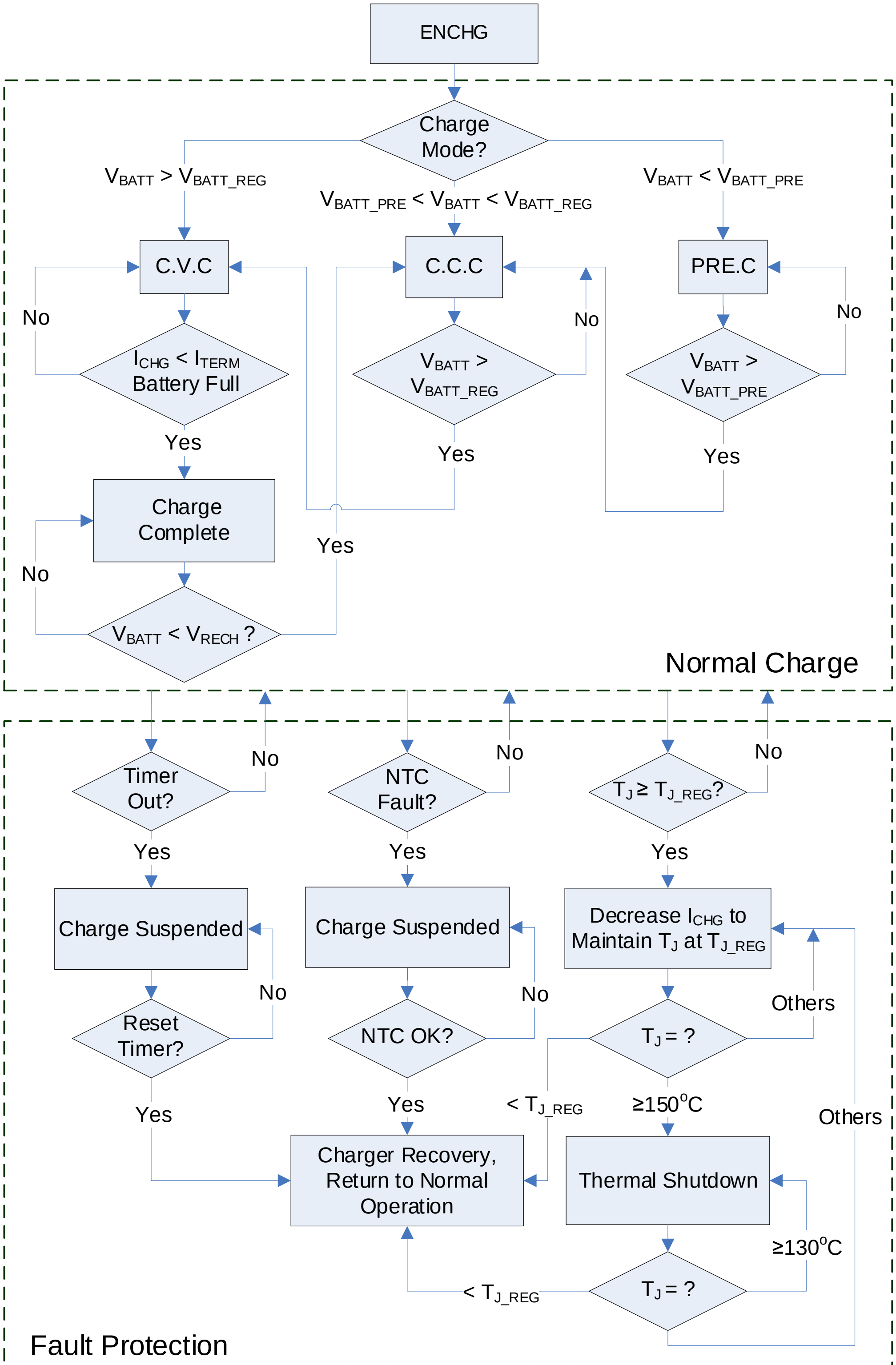


Figure 18: Charging Process

CONTROL FLOW CHART *(continued)*

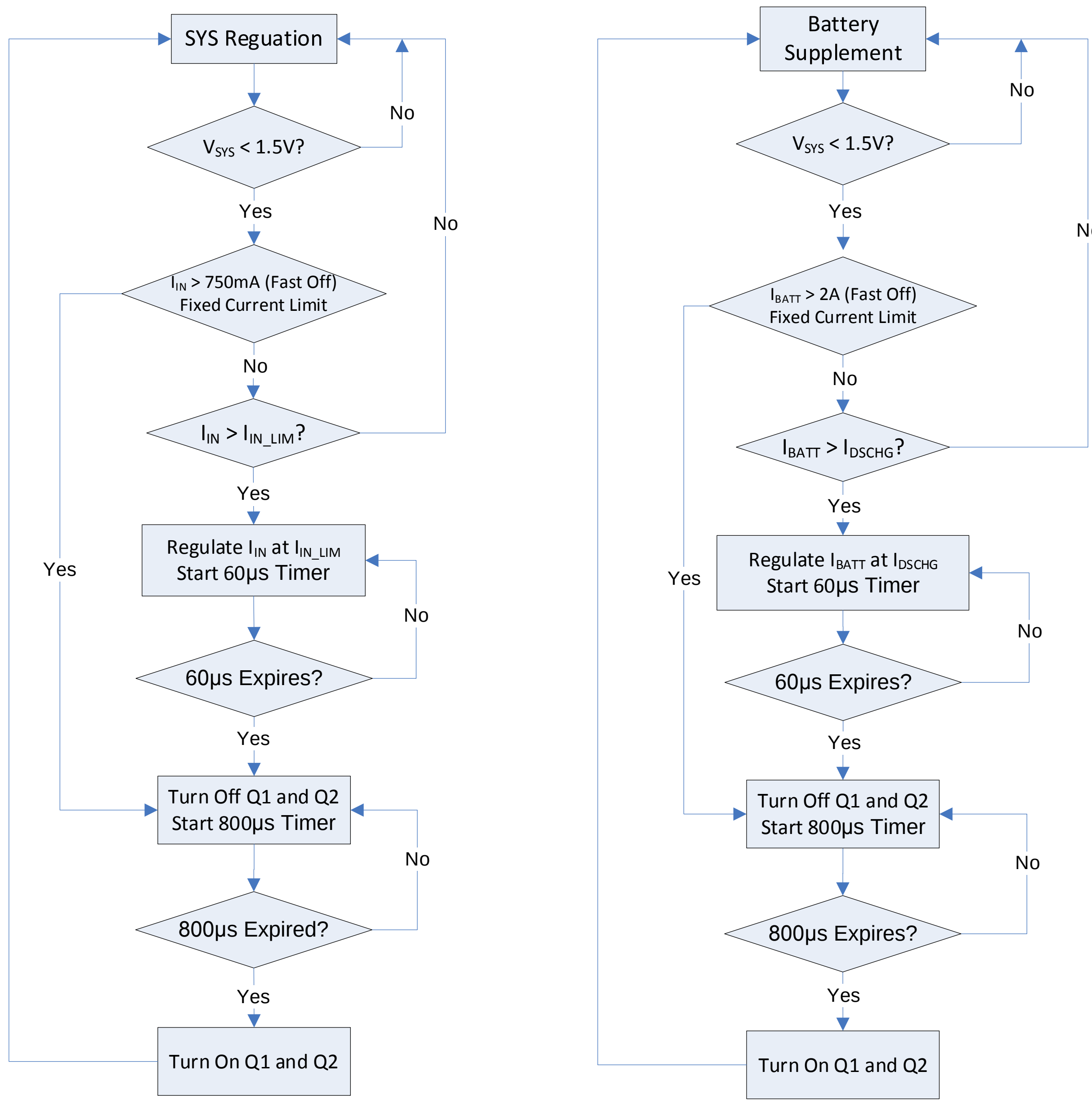


Figure 19: System Short-Circuit Protection

APPLICATION INFORMATION

Selecting a Resistor for the NTC Sensor

Figure 20 shows an internal resistor divider reference circuit to limit the low temperature threshold and high temperature threshold at V_{HOT} and V_{COLD}, respectively.

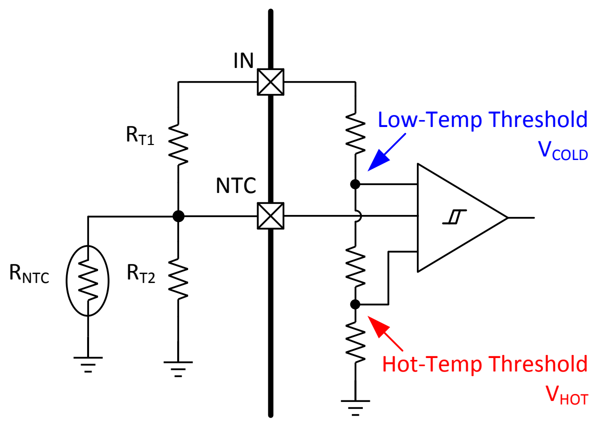


Figure 20: NTC Function Block

For a given NTC thermistor, set the NTC window by selecting appropriate R_{T1} and R_{T2} values with Equation (1) and Equation (2):

$$\frac{R_{T2} // R_{NTC\_Cold}}{R_{T1} + R_{T2} // R_{NTC\_Cold}} = V_{COLD} \quad (1)$$

$$\frac{R_{T2} // R_{NTC\_Hot}}{R_{T1} + R_{T2} // R_{NTC\_Hot}} = V_{HOT} \quad (2)$$

Where R_{NTC_Hot} is the value of the NTC resistor at the high end of the required temperature operation range, and R_{NTC_Cold} is NTC resistor value at a low temperature. The two resistors (R_{T1} and R_{T2}) allow the high temperature limit and low temperature limit to be programmed independently. With this feature, the MP2660 can fit most NTC resistor types and different temperature operation range requirements.

The R_{T1} and R_{T2} values depend on the type of NTC resistor used. For example, for the thermistor NCP18XH103, R_{NTC_Cold} is 27.219kΩ at 0°C, and R_{NTC_Hot} is 4.161kΩ at 50°C.

Equation (1) and Equation (2) can be used to calculate R_{T1} = 6.59kΩ and R_{T2} = 24.15kΩ, assuming that the NTC window is between 0°C and 50°C and using the V_{COLD} and V_{HOT} values from the EC table.

Selecting the External Capacitor

Like most low-dropout regulators, the MP2660 requires external capacitors for regulator stability and voltage spike immunity. The device is designed specifically for portable applications requiring minimum board space and small components. These capacitors must be selected correctly for optimal performance.

An input capacitor is required for stability. A capacitor of at least 1µF must be connected between IN to GND for stable operation over the entire load current range. There can be more output capacitance than input as long as the input is at least 1µF.

The IC is designed specifically to work with a very small ceramic output capacitor (typically 2.2µF). A ceramic capacitor with X5R or X7R type dielectrics at least 2.2µF is suitable in the MP2660 application circuit. For the MP2660, the output capacitor should be connected between SYS and GND with thick traces and small loop area.

A capacitor from BATT to GND is also necessary for the MP2660, and the typical capacitance value is 10µF. A ceramic capacitor with X5R or X7R type dielectrics at least 10µF is suitable for the application circuit.

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. Place the external capacitors as close to the IC as possible to ensure the smallest input inductance and the ground impedance.
2. Place the PCB trace connecting the capacitor between VDD and GND very close to the IC.
3. Keep the signal GND for the I²C wire clean and away from power GND.
4. Route the I²C wires (SDA, SCL) parallel with each other.

TYPICAL APPLICATION CIRCUIT

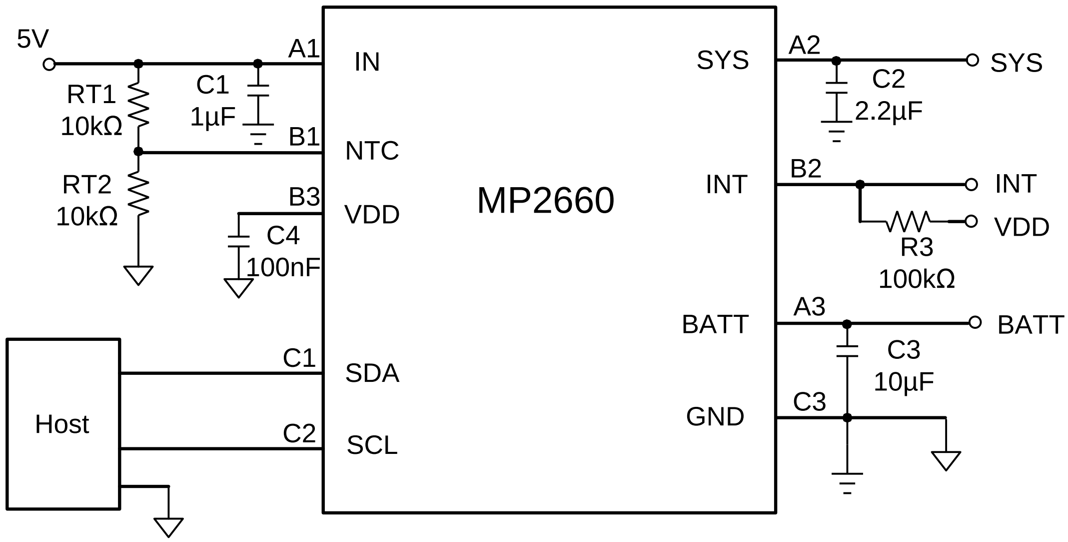


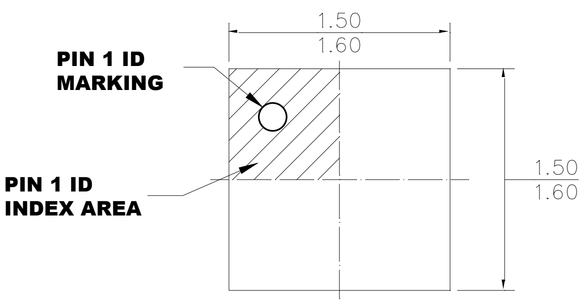
Figure 21: MP2660 Typical Application Circuit with 5V Input

Table 4: The Key BOM of Figure 21

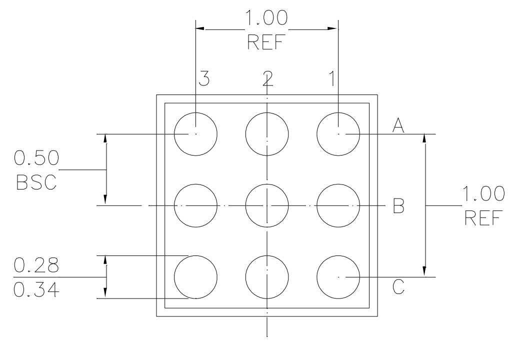
Qty	Ref	Value	Description	Package	Manufacture
1	C1	1µF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	C2	2.2µF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	C3	10µF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
1	C4	100nF	Ceramic Capacitor; 16V; X5R or X7R	0603	Any
2	R_{T1}, R_{T2}	10kΩ	Film Resistor;1%	0603	Any

PACKAGE INFORMATION

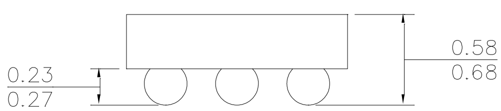
WLCSP-9 (1.55mmx1.55mm)



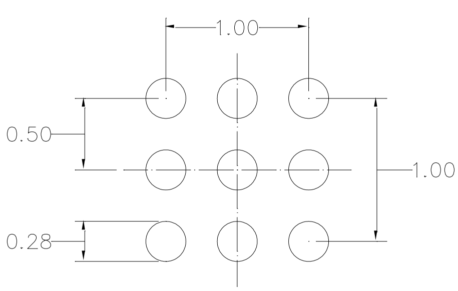
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211, VARIATION BC.
4) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.1	4/29/2021	Updated the footnote below the Applications section	
		Updated the INT pin description	4
		Updated “CE = L” to “CEB = 0”; updated “CE = H” to “CEB = 1”	6–8
		Updated the conditions for the Typical Performance Characteristics section	10–13
		Updated the Safety Timer section	18–19
		Added the I²C Interface section	20–22
		Updated the conditions and symbols in Figure 17, Figure 18, and Figure 19 in the Control Flow Chart section	31–33
		Updated “I_{TC}” to “I_{PRE}”; updated “I_{BF}” to “I_{TERM}”; updated “V_{IN_REG}” to “V_{IN_MIN}”; grammar and formatting updates	All
1.12	10/15/2021	grammar corrections	All