MP2698

5V, All-in-One Power Bank Solution IC with 3.6A Boost Current and 5.0A Fast-Charging Capability

DESCRIPTION

The MP2698 is a highly integrated, flexible, switch-mode, battery charge management and system power-path management device designed for single-cell Li-ion and Li-polymer batteries for use in a wide range of portable applications.

The IC uses two operating modes, charge mode and boost mode, to manage system and battery power based on the state of the input and output.

When input power is present, the MP2698 operates in charge mode. The device detects the battery voltage automatically and charges the battery in four phases: trickle current charge, pre-charge, constant-current charge, and constant-voltage charge.

In the absence of an input source, the MP2698 switches to boost mode to power SYS from the battery. The IC supports BC1.2 output by identifying the request through DP2/DM2.

To guarantee safe operation, the IC includes input over-voltage protection (OVP), battery over-voltage protection (OVP), thermal shutdown, battery temperature monitoring, and a programmable timer to prevent the prolonged charging of an abnormal battery.

With the I²C interface, the IC can flexibly program the charging and boosting parameters, such as input current limit, charging current, battery regulation (charge-full) voltage, safety timer, boost output current limit, and so on. The IC can also provide the operation status through the I²C registers and battery status via four LEDs.

The MP2698 is available in a QFN-28 (4mmx4mm) package.

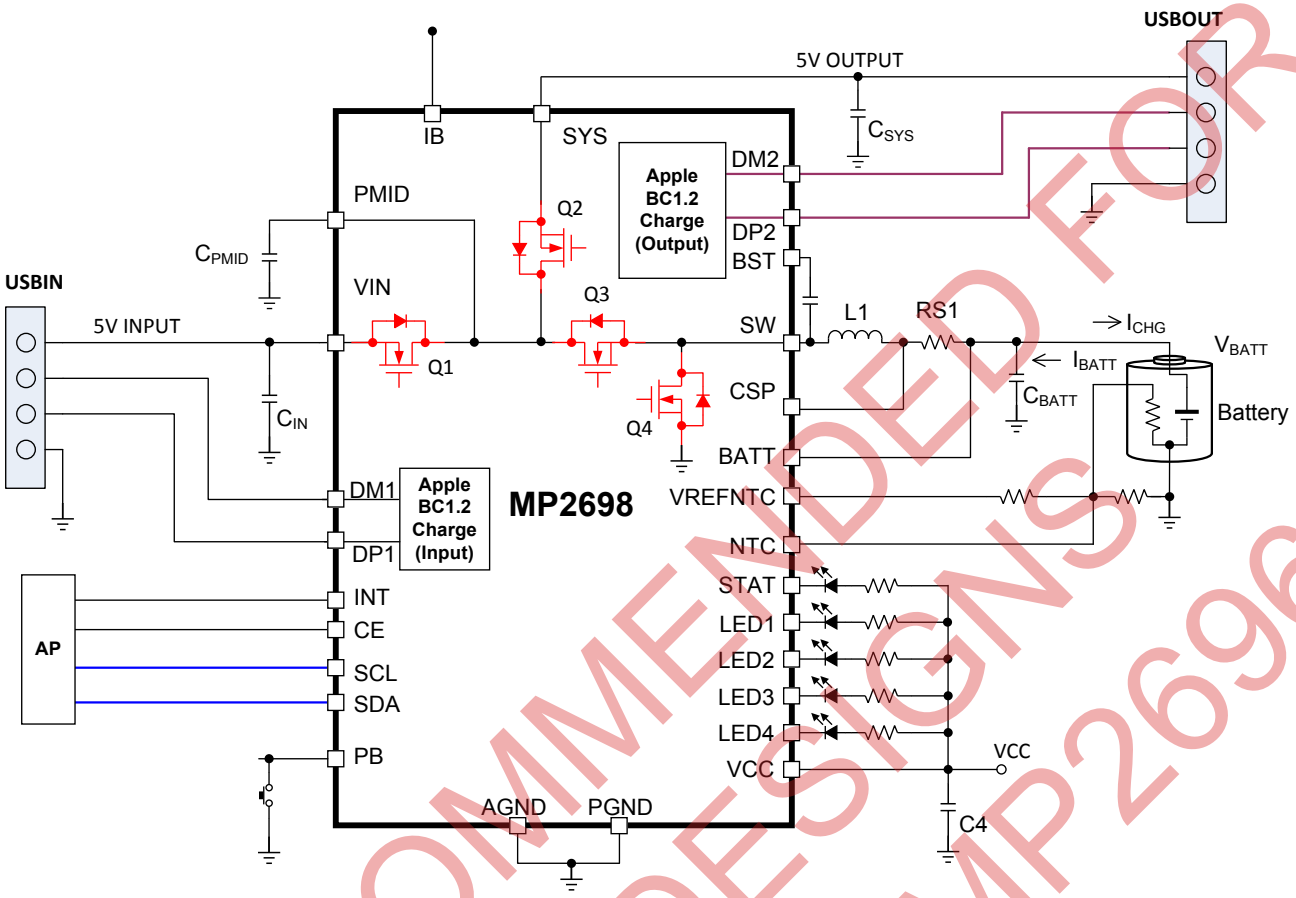
FEATURES

- 4.0V to 6.0V Operating Voltage Range
- Up to 24V Sustainable Input Voltage
- Input Source BC1.2 and Non-Standard Adapter Detection
- Integrated Input Current-Based and Input Voltage-Based Power Management Function
- Up to 5.0A Programmable Charge Current
- Reverse Boost Operation Mode with up to 3.6A Boost Current and 5V Voltage for System Power
- Output USB Type Detection
- Analog Voltage Output IB Pin for Battery-Current Monitoring
- Programmable 3.1V to 4.675V Charge Voltage with 0.5% Accuracy
- Four LEDs Battery Gauge Indicators
- JEITA-Compatible Negative Temperature Coefficient (NTC) Protection
- Programmable Timer Back-Up Protection
- Thermal Regulation and Thermal Shutdown
- USB Output Cable Impedance Compensation
- Integrated Short-Circuit Protection (SCP) and Over-Voltage Protection (OVP) for Pass-Through Path
- Integrated SCP and OVP for Boost Mode
- Integrated 8-Bit SAR ADC for Battery Voltage Measurement
- Available in a QFN-28 (4mmx4mm) Package

APPLICATIONS

- Sub-Battery Applications
- Power-Bank Applications for Smartphones, Tablets, and Other Portable Devices

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2698GR-xxxx**	QFN-28 (4mmx4mm)	*See Below*
EV2698-R-00A	Evaluation Kit (w/ MCU)	*See Below*
EVKT-2698	Evaluation Kit (w/ USB Dongle)	*See Below*

*For Tape & Reel, add suffix –Z (e.g.: MP2698GR–xxxx-Z).
**"xxxx" is the register setting option. The factory default is "0000". This content can be viewed in the I²C Register Map section on page 25. For customized options, please contact an MPS FAE to obtain an "xxxx" value.

TOP MARKING

MPSYWW
MP2698
LLLLLL

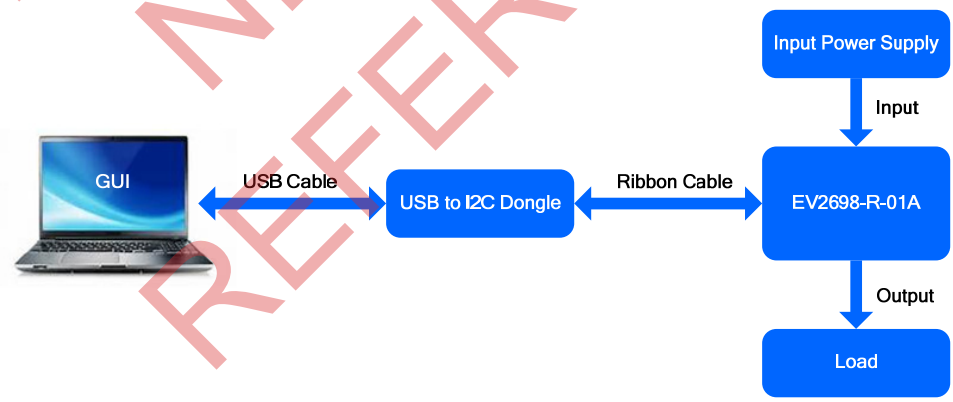
MPS: MPS prefix
Y: Year code
WW: Week code
MP2698: Part number
LLLLLL: Lot number

EVALUATION KIT EVKT-2698

EVKT-2698 Kit contents: (Items below can be ordered separately)

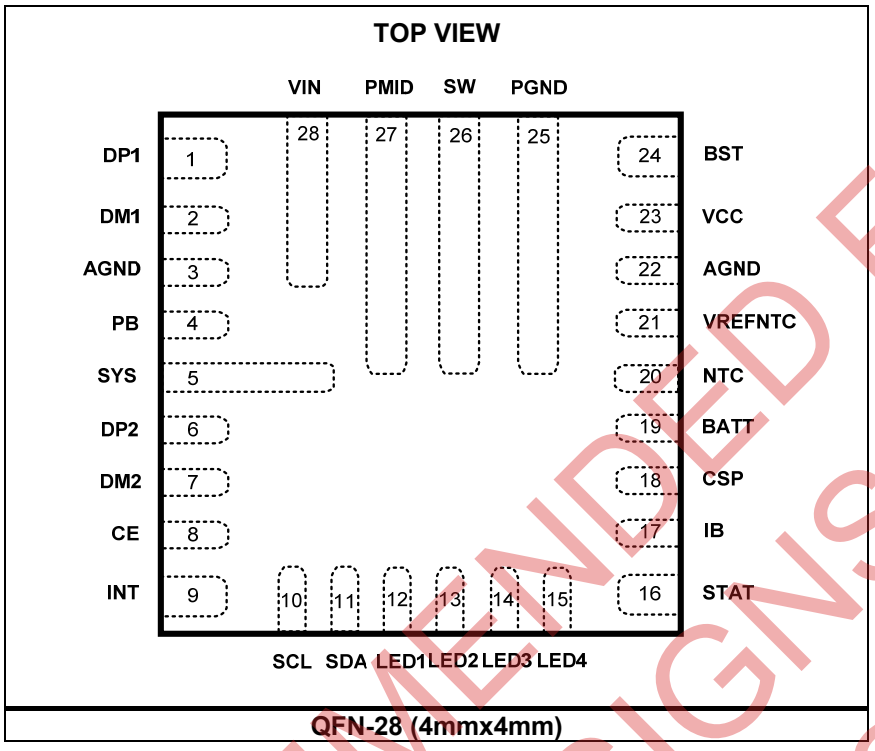
#	Part Number	Item	Quantity
1	EV2698-R-01A	MP2698 evaluation board	1
2	EVKT-USBI2C-02-Bag	Includes one USB-to-I2C dongle, one USB cable, one ribbon cable	1
3	Tdrive-2698	USB thumb drive that stores the GUI installation file and supplemental documents.	1

Order direct from MonolithicPower.com or our distributors.



EVKT-2698 Evaluation Kit Set-Up

PACKAGE REFERENCE



PIN FUNCTIONS

Package Pin #	Name	I/O	Description
1	DP1	I/O	**Positive line of the USB data line pair for BC1.2 detection.** Connect a 3MΩ resistor from DP1 to GND.
2	DM1	I/O	**Positive line of the USB data line pair for BC1.2 detection.** Connect a 3MΩ resistor from DM1 to GND.
3	AGND	Power	**Analog ground.** Connect AGND (pin 3) with PGND.
4	PB	I	**Press button input.** A low-to-high edge invokes the USB2 detection and power output. PB should be tied high when not in use.
5	SYS	Power	**System power supply.** Place a >1μF ceramic capacitor from SYS to PGND.
6	DP2	I/O	**Positive line of the output USB data line pair for output.** DP2 together with DM2 implements USB2 host port detection automatically. Connect a 1MΩ resistor from DP2 to GND.
7	DM2	I/O	**Negative line of the output USB date line pair for output.** DM2 together with DP2 implements USB2 host port detection automatically. Connect a 1MΩ resistor from DM2 to GND.
8	CE	I	**Logic input pin to charge and discharge the battery.** CE at active high enables the battery charging and discharging operation.
9	INT	O	**Open-drain interrupt output.** INT can send a charging status and fault interrupt signal to the host.
10	SCL	I/O	**I²C interface clock.** Connect SCL to the logic rail through a 10kΩ resistor.
11	SDA	I/O	**I²C interface data.** Connect SDA to the logic rail through a 10kΩ resistor.

PIN FUNCTIONS *(continued)*

Package Pin #	Name	I/O	Description
12	LED1	O	**Battery gauge indicator output.** Connect a resistor and an LED in series from LEDx to VCC.
13	LED2	O	
14	LED3	O	
15	LED4	O	
16	STAT	O	**Indicator for charging operation.**
17	IB	O	**Battery current representation.** The IB current indicates the charge current to the battery in charge mode and the discharge current out of the battery in boost mode. Connect a resistor from IB to AGND to get proper current information.
18	CSP	I	**Positive battery terminal / battery charge current sense negative input.**
19	BATT	I	**Battery positive terminal.**
20	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VREFNTC to NTC to GND. Charging is suspended when the NTC voltage is out of its range.
21	VREFNTC	O	**Reference voltage output for powering up the NTC.**
22	AGND	Power	**Analog ground.** Place AGND (pin 22) far away from the noisy power ground.
23	VCC	I	**Internal circuit power supply.** Bypass VCC to AGND with a 10μF ceramic capacitor. VCC *cannot* carry an external load higher than 30mA.
24	BST	I	**Bootstrap.** Connect a bootstrap capacitor between BST and SW to form a floating supply across the power switch driver to drive the power switch's gate above the supply voltage.
25	PGND	Power	**Power ground.**
26	SW	Power	**Switching output node.**
27	PMID	Power	**Power input of the power stage.** Connect PMID to the drain of the reverse-blocking MOSFET and the drain of the high-side MOSFET internally. Bypass PMID with ceramic capacitors (≥47μF) from PMID to PGND as close to the IC as possible.
28	VIN	Power	**Power input of the IC from USB1.** Place a ceramic capacitor (≥10μF) from VIN to PGND as close to the IC as possible.

ABSOLUTE MAXIMUM RATINGS (1)

VIN, PMID, SYS to PGND ..... -0.3V to +24V
SW to PGND .....-0.3V (-2V for 20ns) to +24V
BST to PGND..... SW to SW + 6V
BATT to PGND ..... -0.3V to +5.3V
All other pins to AGND..... -0.3V to +6.0V
Continuous power dissipation (T_A = +25°C) (2)
..... 2W
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C
Storage temperature .....-65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.0V to 6.0V
I_{IN} 3A
I_{SYS} .....up to 3.6A
I_{CC} .....up to 5.0A
V_{BATT} .....up to 4.5V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-28 (4mmx4mm).....44.....9 .... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VIN to PMID switch (Q1) on resistance	$R_{IN\ to\ PMID}$			32		mΩ
PMID to SYS switch (Q2) on resistance	$R_{PMID\ to\ SYS}$			32		mΩ
High-side switch on resistance	R_{HS}			18		mΩ
Low-side switch on resistance	R_{LS}			8		mΩ
Peak current limit for high-side switch	I_{PEAK_HS}	Charger CC mode		9.0		A
Peak current limit for low-side switch	I_{PEAK_LS}	Boost mode (REG0C[7:5] = 100)		8.0		A
Operating frequency	F_{SW}			550		kHz
VCC LDO output voltage	V_{VCC}	V_{IN} = 5V, I_{VCC} = 100mA	4.35	4.50	4.65	V
VCC UVLO	V_{CC_UVLO}	VCC rising	2.0	2.2	2.4	V
VCC UVLO hysteresis				280		mV
VCC POR for IIC	V_{CC_POR}	VCC rising		2		V
VCC POR hysteresis				150		mV
Charge Mode						
Input quiescent current	I_Q	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, charge disabled, SYS float		1.35	1.70	mA
		• V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT}, charge enabled, BATT and SYS float		2.0	2.4	mA
Input under-voltage lockout	V_{IN_ULVO}	V_{IN} falling		3.13	3.28	V
Input V_{ULVO} hysteresis				320		mV
V_{IN} vs. V_{BATT} headroom		V_{IN} rising	360	460	570	mV
		V_{IN} falling	60	140	210	mV
V_{IN} over-voltage protection	V_{IN_OVP}	V_{IN} rising		6		V
V_{IN} over-voltage protection hysteresis				180		mV
System over-current protection threshold	I_{SYSOCP}		4.0	5.5	6.5	A
System over-current blanking time	$T_{SYSOCBLK}$			3		ms
System over-current recover time	$T_{SYSRECVR}$			300		ms
V_{IN} under-voltage protection detection	V_{IN_UVP}	V_{IN} falling		3.15		V
V_{IN} under-voltage protection detection hysteresis				400		mV
Discharge dummy load at VIN	R_{IN_DUM}			55		Ω
Discharge dummy load at SYS	R_{SYS_DUM}			25		Ω

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery termination (charge full) voltage [I²C]	V_{BATT_REG}	Depends on the I²C setting	3.100		4.675	V
Charge voltage regulation accuracy		REG04[7:2] = 101100, V_{BATT_REG} = 4.2V	-0.5		0.5	%
		REG04[7:2] = 110010, V_{BATT_REG} = 4.35V	-0.5		0.5	
Constant-current charge current [I²C]	I_{CC}	Depends on the I²C setting	0.5		5.0	A
Charge current regulation accuracy		REG02[7:2] = 100011, I_{CC} = 4A	-5		5	%
		REG02[7:2] = 001010, I_{CC} = 1.5A	-5		5	%
		REG02[7:2] = 000000, I_{CC} = 0.5A	-15		15	%
Battery pre-charge threshold [I²C]	V_{BATT_PRE}	REG04[4] = 1, V_{BATT} rising	2.85	3.00	3.15	V
		REG04[4] = 0, V_{BATT} rising	2.65	2.80	2.95	
Battery pre-charge hysteresis		V_{BATT} falling		200		mV
Battery short threshold	V_{BATT_TC}	V_{BATT} rising	1.9	2.0	2.1	V
Battery short threshold hysteresis		V_{BATT} falling		250		mV
Trickle charge current	I_{TC}	V_{BATT} = 1V, RS1 = 10mΩ		100		mA
Pre-charge current [I²C]	I_{PRE}	Depends on the I²C setting, RS1 = 10mΩ	100		1600	mA
Pre-charge current accuracy		REG03[7:4] = 0011, I_{PRE} = 400mA, V_{BATT} = 2.6V, RS1 = 10mΩ	-20		20	%
Termination current [I²C]	I_{TERM}	Depends on the I²C setting	200		1700	mA
Termination current accuracy		REG03[3:0] = 0000, I_{TERM} = 200mA, V_{BATT_REG} = 4.2V, RS1 = 10mΩ	80		220	mA
Recharge threshold below V_{BATT_REG}	V_{RECH}	REG04[0] = 1		270		mV
Input Voltage- and Input Current-Based Power Path						
Input voltage regulation accuracy		REG00[6:3] = 1010, V_{IN} = 5V, V_{IN_REG} = 4.68V	-3		3	%
Input current limit	I_{IN_LMT}	REG00[2:0] = 111	2707	2850	3000	mA
Protection						
Battery over-voltage protection	V_{BATT_OVP}	Rising, as a percentage of V_{BATT_REG}		103.5 %		V_{BATT_REG}
Battery over-voltage protection hysteresis		Falling, as a percentage of V_{BATT_REG}		2.0%		V_{BATT_REG}
Thermal shutdown rising threshold (5)	T_{J_SHDN}	T_J rising		150		°C
Thermal shutdown hysteresis (5)				20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VREFNTC voltage	$V_{VREFNTC}$	V_{IN} = 5V, $I_{VREFNTC}$ = 1mA		4.8		V
NTC low temp rising threshold	V_{COLD}	As a percentage of $V_{VREFNTC}$	70.4%	71.0%	71.6%	V_{REFNTC}
NTC low temp rising threshold hysteresis		As a percentage of $V_{VREFNTC}$		0.7%		V_{REFNTC}
NTC cool temp rising threshold	V_{COOL}	As a percentage of $V_{VREFNTC}$	68.5%	69.0%	69.5%	V_{REFNTC}
NTC cool temp rising threshold hysteresis		As a percentage of $V_{VREFNTC}$		0.7%		V_{REFNTC}
NTC warm temp falling threshold	V_{WARM}	As a percentage of $V_{VREFNTC}$	55.5%	56.1%	56.7%	V_{REFNTC}
NTC warm temp falling threshold hysteresis		As a percentage of $V_{VREFNTC}$		1.2%		V_{REFNTC}
NTC hot temp falling threshold	V_{HOT}	As a percentage of $V_{VREFNTC}$	47.6%	48.1%	48.6%	V_{REFNTC}
NTC hot temp falling threshold hysteresis		As a percentage of $V_{VREFNTC}$		1.2%		V_{REFNTC}
Boost Mode						
Standby quiescent current	I_{Q_STB}	V_{IN} < V_{IN_UVLO}, V_{BATT} = 4.2V, boost off (sleep mode)		18	22	µA
Boost quiescent current	I_{Q_BST}	I_{SYS} = 0, V_{PMID} = 5.5V, boost enabled, V_{BATT} = 4.2V		2.3		mA
Boost output voltage at PMID	V_{PMID_BST}	REG07[5:4] = 00, $V_{OUT(BST)}$ = 5V, I_{SYS} = 10mA	5.05	5.15	5.25	V
Boost output voltage accuracy		As a percentage of $V_{OUT(BST)}$, I_{SYS} = 10mA	-2		2	%
Boost output PMID power good		V_{PMID} rising		4.75		V
Boost output under-voltage protection	$V_{PMID\_BST\_UVLO}$	V_{BATT} = 3.6V, V_{PMID} falling		3.85		V
		V_{BATT} = 4.2V, V_{PMID} falling, higher than V_{BATT}		160		mV
Boost output over-voltage protection threshold	$V_{OVP\_BST\_5V}$	REG07[5:4] = 00, 5V boost mode, V_{BATT} = 3.7V, boost is enabled, force a voltage at SYS until switching is off	5.8	6.1	6.3	V
Boost output over-voltage protection threshold hysteresis				400		mV
Boost output current limit [I²C]	I_{BST_LIMT}	Programmable range	0.9		3.6	A
		REG05[2:0] = 111, V_{BATT} = 3.7V, 5V output	3.6			A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Battery voltage UVLO	V_{BATT_UVLO}	During boosting		2.5		V
		Before boost starts		2.9		V
System no load to turn-off boost automatically	I_{BST_OFF}	Output current in boost mode, V_{SYS} = 5V, V_{BATT} = 3.7V	50	80	110	mA
Delay for light load turn-off		Battery current is below I_{OFF} in boost mode		36		S
IB voltage output	V_{IB}	I_{BATT} = 1A (discharge)		0.4		V
		Battery current indication tolerance, I_{BATT} = 1A	-5		5	%
Logic IO Pin Characteristics						
Low logic voltage threshold	V_L				0.4	V
High logic voltage threshold	V_H		1.3			V
Input DP1/DM1 USB Detection						
DP1 voltage source	V_{DP1_SRC}	I_{DP1_SRC} < 250μA	0.5	0.6	0.7	V
DM1 voltage source	V_{DM1_SRC}	I_{DM1_SRC} < 250μA	0.5	0.6	0.7	V
DP1 pull-up voltage source	V_{DP1_UP}		3	3.3	3.6	V
DM1 pull-up voltage source	V_{DM1_UP}		3	3.3	3.6	V
Data detect voltage	V_{DAT_REF}		0.25	0.325	0.4	V
Data connect detect current source	I_{DP_SRC}		7		13	μA
DM1 pull-down resistance	R_{DM_DOWN}		14.3	20	24.8	kΩ
DM1 sink current	I_{DM1_SINK}		50	100	150	μA
DP1 sink current	I_{DP1_SINK}		50	100	150	μA
Leakage current input DP1/DM1	I_{DP_LKG}		-1		1	μA
	I_{DM_LKG}		-1		1	μA
Output DP2/DM2 USB Detection						
DP2 starting voltage	V_{DP2_LGC}		2.5	2.7	2.9	V
DM2 starting voltage	V_{DM2_LGC}		2.5	2.7	2.9	V
DP2/DM2 short resistance	R_{SHORT}			85	200	Ω
Pull-down resistor in DM2	R_{PULL_DOWN}		14.3	20	24.8	kΩ
DCP detection voltage	V_{DCP}		0.3		1.1	V
DCP delay time	T_{DCP}		0.8	1	1.2	s
I²C Interface (SDA, SCL) (5)						
Input high threshold level		V_{PULL_UP} = 1.8V, SDA and SCL	1.3			V
Input low threshold level		V_{PULL_UP} = 1.8V, SDA and SCL			0.4	V
Output low threshold level		I_{SINK} = 5mA			0.4	V
I²C clock frequency	F_{SCL}				400	kHz
Indication and Logic						
LED1, LED2, LED3, LED4, STAT pin output low voltage	V_{LED_Low}	Sink 5mA			0.4	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, V_{BATT} = 3.5V, RS1 = 10mΩ, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Press Button (PB)						
PB pull-up resistance	R_{PB}	PB pulled up to VCC		350		kΩ
PB input logic low voltage	V_{L_PB}				0.4	V
PB input logic high voltage	V_{H_PB}		1.2			V
Digital Clock and Watchdog Timer						
Digital clock	F_{DIG1}	VREF LDO enabled		1000		kHz
Watchdog timer	t_{WDT}	REG05H bit[5:4] = 01		40		s
ADC for Battery Voltage						
Effective resolution (current)					8	bits
Conversion time (5)	t_{SR_CONV}			20		µs

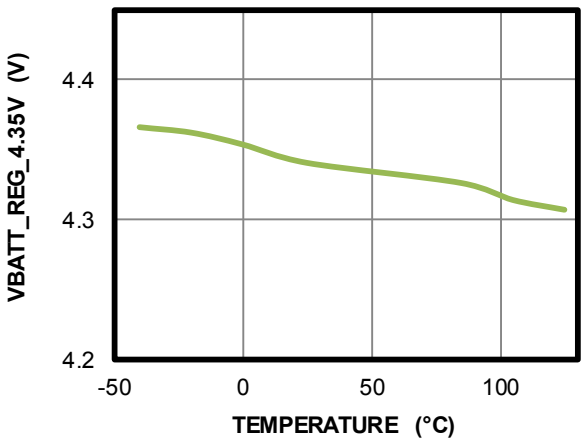
NOTE:

5) Guaranteed by design

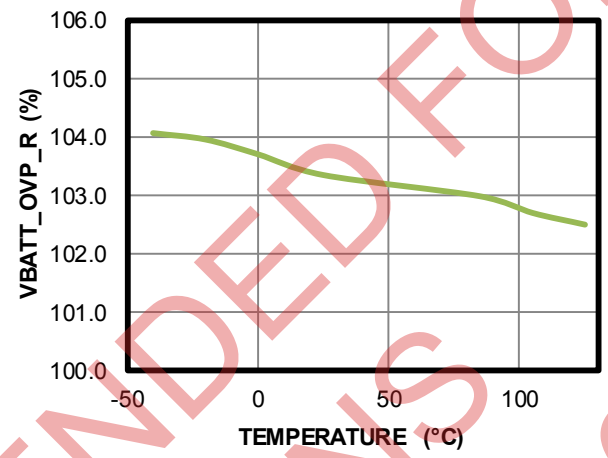
TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 10µF, C_{BATT} = 44µF, C_{PMID} = 22µF, C_{SYS} = 1µF, L1 = 2.2µH, RS1 = 10mΩ, real/simulation battery load, T_A = 25°C, unless otherwise noted.

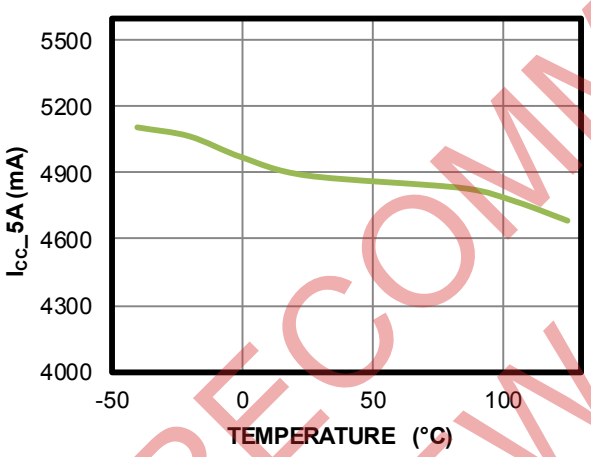
V_{BATT_REG} vs. Temperature



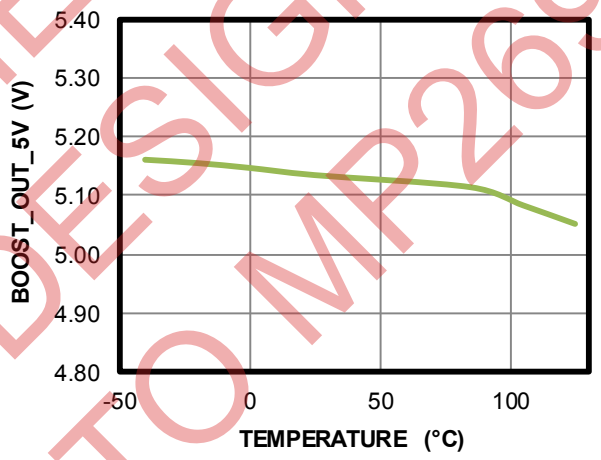
$V_{BATT\_OVP\_R}$ vs. Temperature



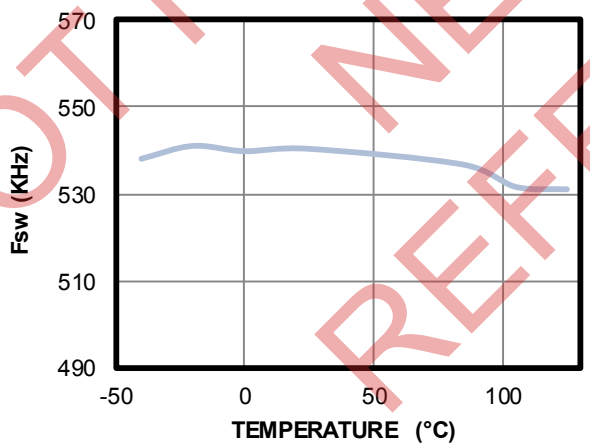
I_{CC}_5A vs. Temperature



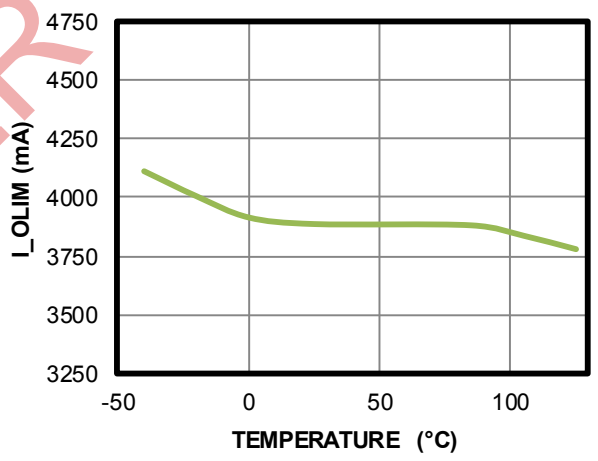
Boost_Out_5V vs. Temperature



F_{SW} vs. Temperature



I_OLIM vs. Temperature

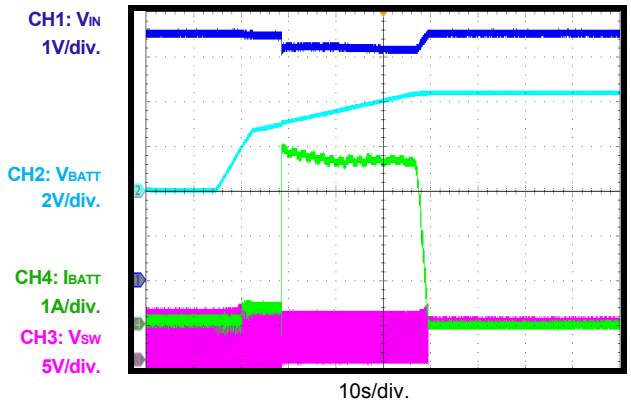


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{BATT} = 44µF, C_{PMID} = 22µF, C_{SYS} = 1µF, L1 = 2.2µH, RS1 = 10mΩ, real/simulation battery load, T_A = 25°C, unless otherwise noted.

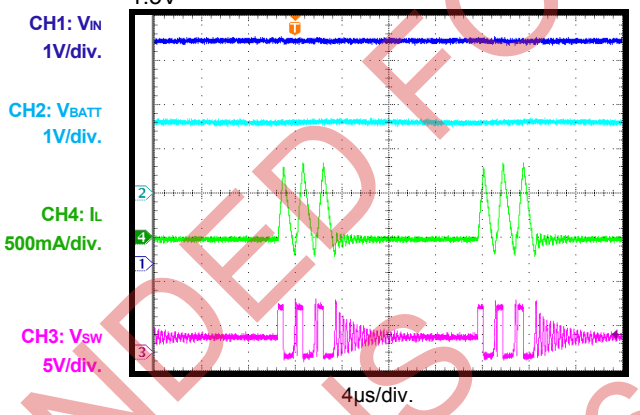
Charge Profile

Ramp-up BATT, V_{IN} = 5.5V, I_{CC} = 4A



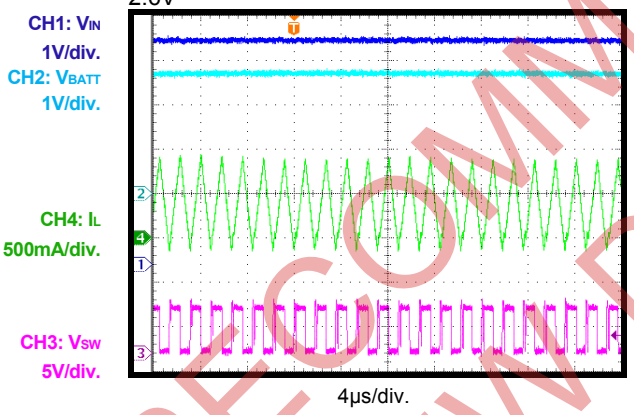
Steady State Waveform

Pre-charge, V_{IN} = 5V, I_{TC} = 100mA, V_{BATT} = 1.5V



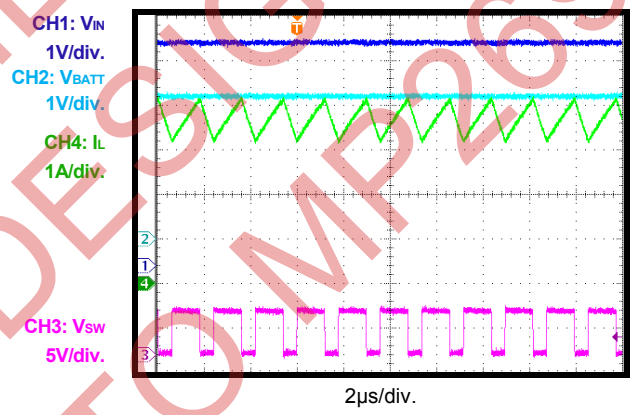
Steady State Waveform

Pre-charge, V_{IN} = 5V, I_{PRE} = 400mA, V_{BATT} = 2.6V



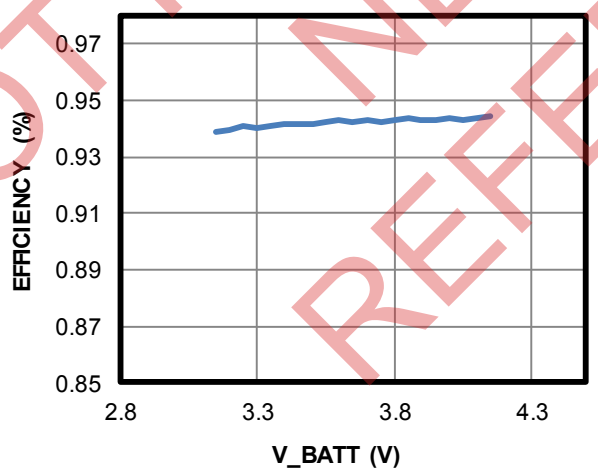
Steady State Waveform

CC charge, V_{IN} = 5V, I_{CC} = 4A, V_{BATT} = 3V



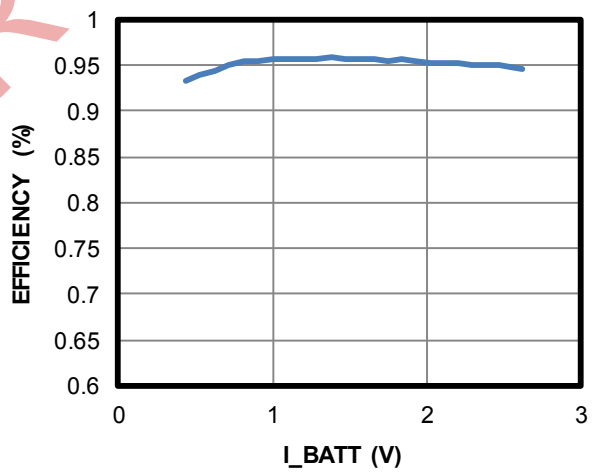
CC Charge Efficiency

I_{CC} = 3A



CV Charge Efficiency

V_{BATT} = 4.2V

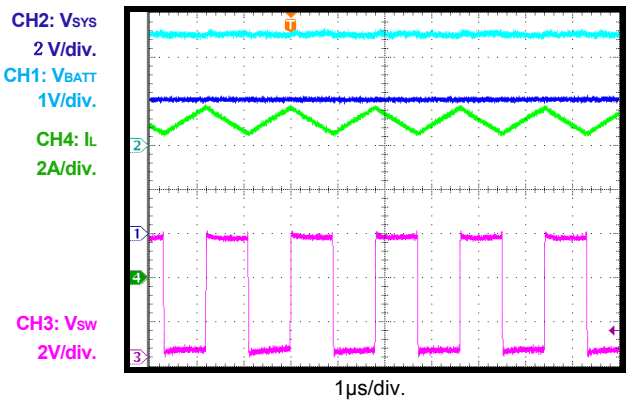


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 10µF, C_{BATT} = 44µF, C_{PMID} = 22µF, C_{SYS} = 1µF, L1 = 2.2µH, RS1 = 10mΩ, real/simulation battery load, T_A = 25°C, unless otherwise noted.

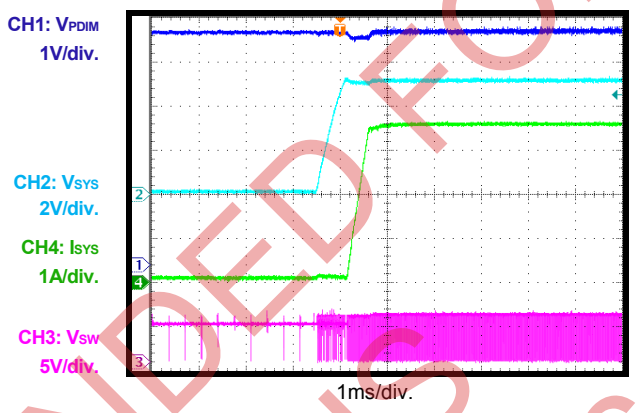
Steady State Waveform

Boost, SYS = 5V/3.6A, V_{BATT} = 3.0V



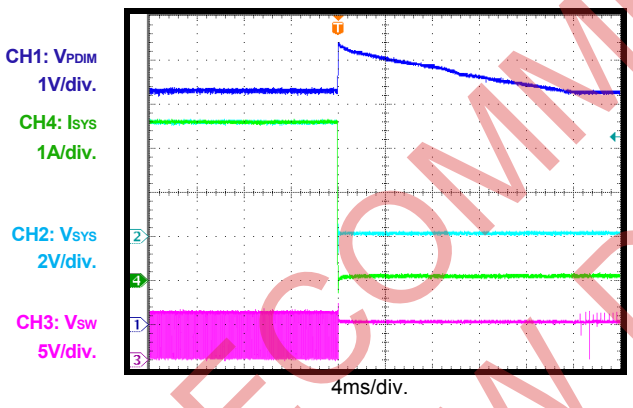
EN On Waveform

Boost, SYS = 5V/3.6A, V_{BATT} = 3.0V



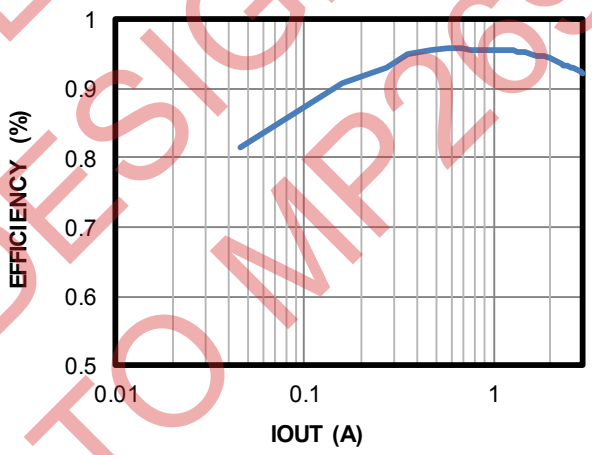
EN Off Waveform

Boost, SYS = 5V/3.6A, V_{BATT} = 3.0V



Discharge Efficiency @ BATT = 3.7V

V_{SYS} = 5V



BLOCK DIAGRAM

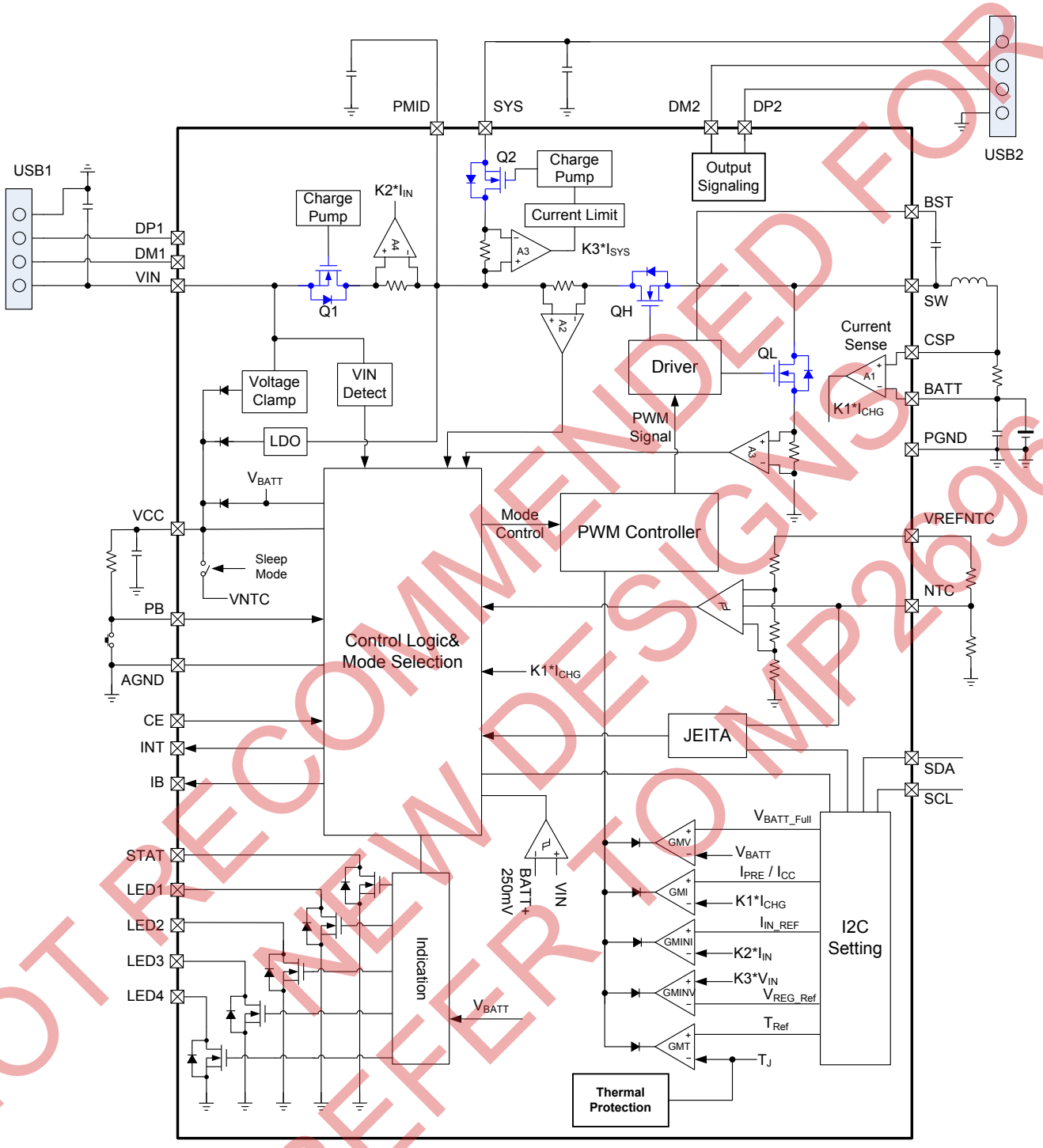


Figure 1: Charge Mode

BLOCK DIAGRAM *(continued)*

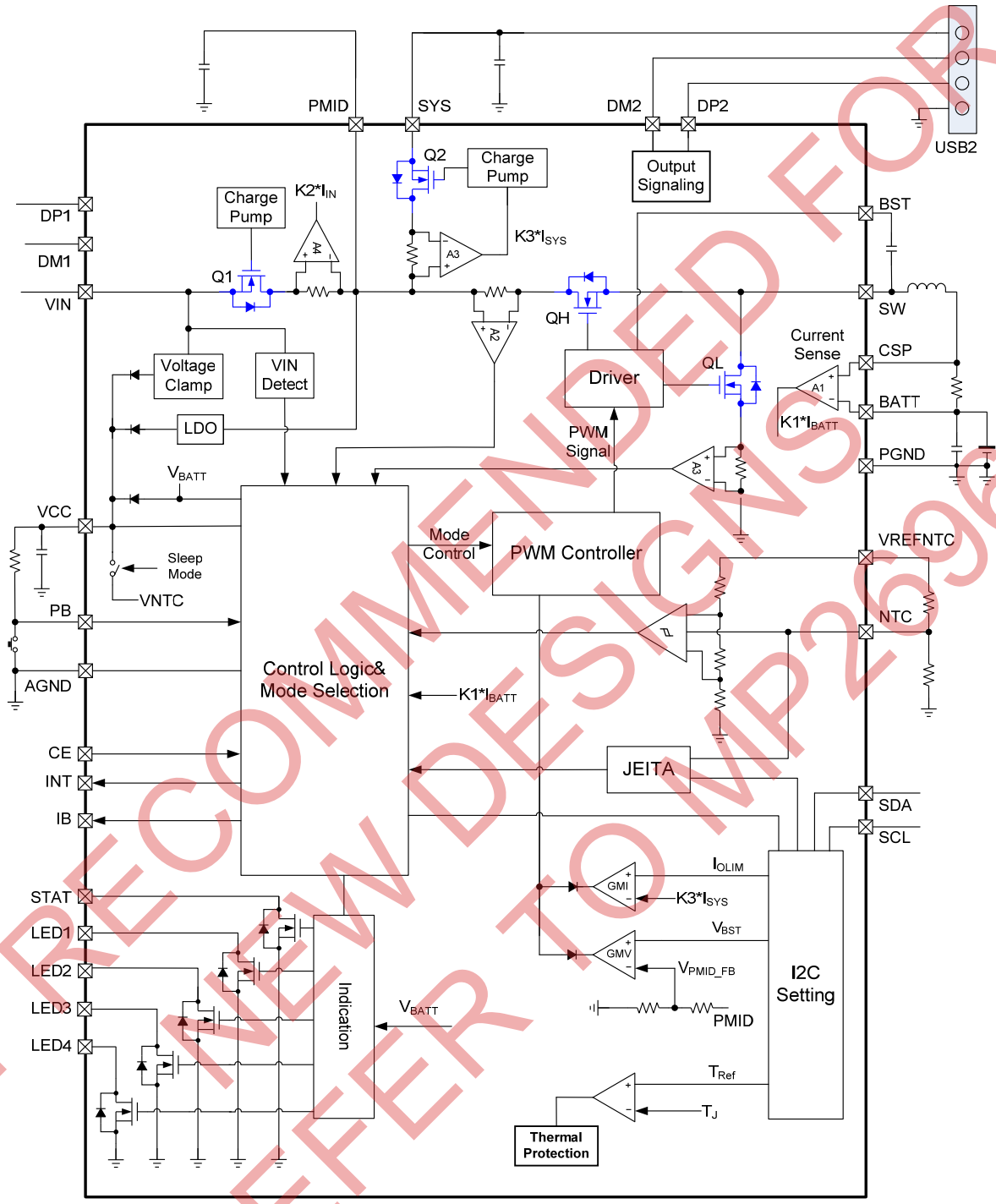


Figure 2: Boost Mode

OPERATION

The MP2698 is an I²C-controlled, synchronous switching charger with bidirectional operation for a boost function that can step up battery voltage to power the system. Depending on the input and output status, the MP2698 operates in one of the three modes: charge mode, boost mode, or sleep mode. In charge mode, the IC supports a precision Li-ion or Li-polymer charging system for single-cell applications. In boost mode, the IC boosts the battery voltage to SYS for powering systems. In sleep mode, the IC stops charging or boosting and operates at a low current from the input or the battery to reduce power consumption when the IC is not operating. The IC monitors USB1 and USB2 to ensure a smooth transition between different modes of operation.

Power Supply

The internal bias circuit of the IC is powered by the highest voltage of either V_{PMID} or V_{BATT}. When VCC rises above the V_{CC_POR} threshold, the I²C interface is ready for communication, and all registers are reset to the default value. The host can access all registers.

VCC supplies the internal bias circuits and the high-side and low-side MOSFET gate drivers. The pull-up rail of STAT can also be connected to VCC (see Figure 3).

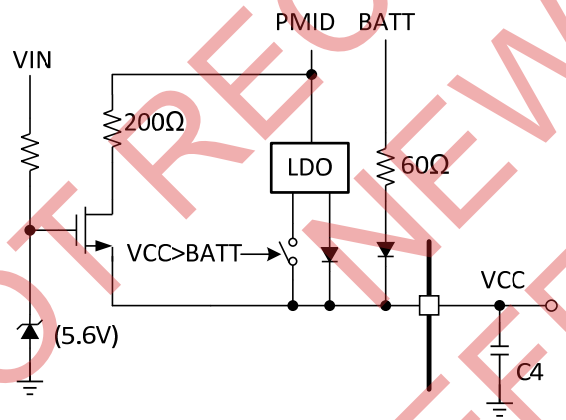


Figure 3: VCC Power Supply Circuit

In boost mode, the VCC LDO is enabled once boost is enabled.

In charge mode, the internal VCC LDO is enabled when the following conditions are valid:

- $V_{PMID} > V_{CC\_POR}$ (2V)
- No thermal shutdown

The VCC load capability should not be higher than 30mA.

Input Power Status Indication

The IC qualifies the voltage and current of the input source before start-up. The input source must meet the following requirements:

- $V_{IN} > V_{BATT}$ + 460mV
- $V_{IN} > V_{IN\_UVLO}$

Once the input power source meets the conditions above, the system status register REG08 bit[2] asserts that the input power is good, and DP1/DM1 detection begins if enabled. Then the step-down converter is ready to operate.

All of the above conditions are monitored continuously, and the charge cycle is suspended once one of the conditions exits the limit.

CHARGER MODE OPERATION

Charge Cycle

In charge mode, the IC has five control loops to regulate the input voltage, input current, charge current, charge voltage, and device junction temperature.

When the input power is qualified as a good power supply, the IC checks the battery voltage to provide four main charging phases: trickle-charge, pre-charge, constant-current charge, and constant-voltage charge.

1. Phase 1 (trickle-charge): If the battery voltage is lower than V_{BATT_TC} (2.1V), a trickle-charging current of 100mA is applied on the battery, which helps reset the protection circuit in the battery pack.
2. Phase 2 (pre-charge): When the battery voltage exceeds V_{BATT_TC}, the IC starts to pre-charge the deeply depleted battery safely until the battery voltage reaches the pre-charge to fast-charge threshold (V_{BATT_PRE}). The pre-charge current can be programmed via the I²C register REG03 bit[7:4].

3. Phase 3 (constant-current charge): When the battery voltage exceeds V_{BATT_PRE} (set via REG04 bit[1]), the IC enters a constant-current charge (fast-charge) phase. The fast charge current can be programmed as high as 5A via REG02 bit[7:2].
4. Phase 4 (constant-voltage charge): When the battery voltage rises to the pre-programmed battery regulation (charge-full) voltage (V_{BATT_REG}) set via REG04 bit[7:2], the charge current begins to taper off.

The charge cycle is considered completed when the charge current reaches the battery-full termination threshold (I_{TERM}) set via REG03 bit[3:0], assuming that the termination function is enabled via REG05 bit[7].

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input current or input voltage loops) or thermal regulation. The thermal regulation reduces the charge current so the IC junction temperature does not exceed the preset limit. The multiple thermal regulation thresholds from 60 - 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via REG06 bit[1:0]. A new charge cycle begins when the following conditions are valid:

- The input power is re-plugged, and USB1 ready.
- Battery charging is enabled by the I²C, and CE is forced to a high logic.
- No thermistor fault.
- No battery over-voltage.

Automatic Recharge

When the battery is charged completely or charging is terminated, the battery may be discharged because of the system consumption or self-discharge function. When the battery voltage is discharged below the recharge threshold (programmable via REG04 bit[0]), the IC begins another new charging cycle automatically without having to restart a charging cycle manually if the input power is valid.

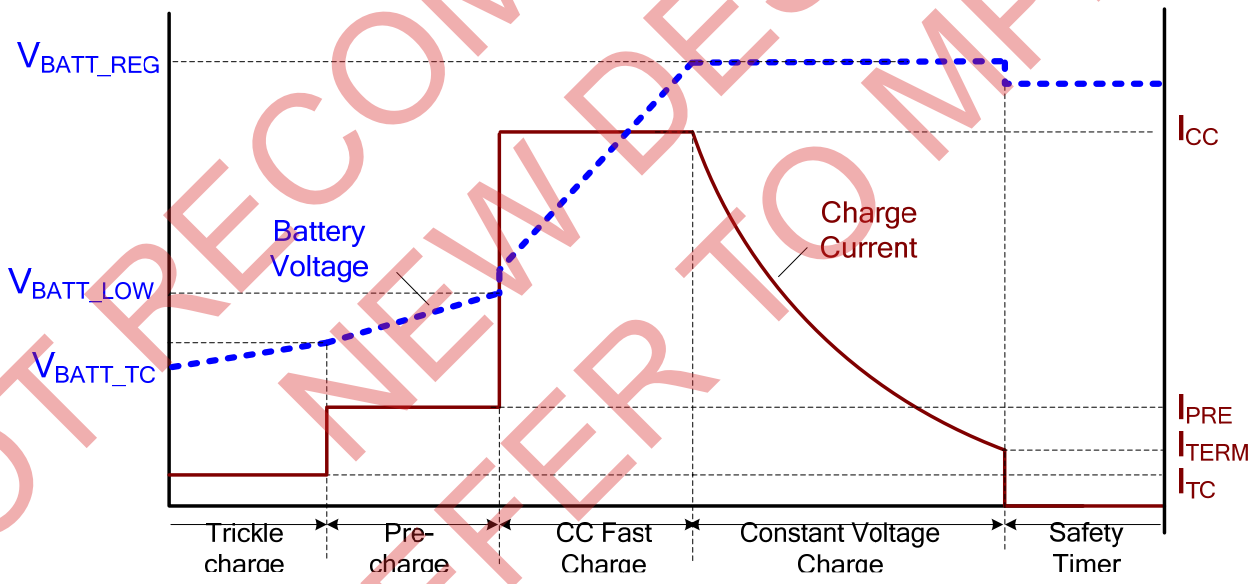


Figure 4: Battery Charge Profile

Battery Over-Voltage Protection (OVP)

The IC has battery over-voltage protection (OVP). If the battery voltage exceeds the battery over-voltage threshold (103.5% of the battery regulation voltage), charging is disabled. Under this condition, an internal current source draws a current from BATT to decrease the battery voltage and protect the battery.

When battery OVP occurs, only the charging is disabled, and the pass-through path is still on.

CE Control

CE is a logic input pin for enabling or disabling battery charging or restarting a new charging cycle. Battery charging is enabled when REG01 bit[5:4] is set to 01 and CE is pulled to logic low.

Indication

Apart from multiple status bits designed in the I²C register, the IC also has a hardware status output pin (STAT). The status of STAT in different cases is shown in Table 1.

Table 1: Operation Indications

Charging State	STAT
In charging	Low
Charging complete, sleep mode, charge disable	High
Charging suspend, battery float	Blinking at 1Hz

Safety Timer

The IC provides both a pre-charge and complete-charge safety timer to prevent extending the charging cycle due to abnormal battery conditions. The total safety timer for both trickle charge and pre-charge is one hour when the battery voltage is lower than V_{BATT_PRE}. The complete charge safety timer starts when the battery enters fast-charge mode. The fast-charge safety timer can be programmed through the I²C. The safety timer feature can be disabled via the I²C. The safety timer does not operate in boost mode.

The safety timer is reset at the beginning of a new charging cycle and can also be reset by toggling VIN or CE. The following actions can restart the safety timer:

- A new charge cycle is kicked in.
- Toggle CE high to low to high (charge enabled).
- Write REG05 bit[3] from 0 to 1 (safety timer enabled).
- Write REG01 bit[7] from 0 to 1 (software reset) with REG0B bit[6] = 1.

The IC can suspend the timer automatically when any fault occurs.

Input Voltage-Based and Input Current-Based Power Management

To meet the maximum current limit in USB specifications and avoid overloading the adapter, the IC features both input current and input voltage power management by monitoring the input current and input voltage continuously. The total input current limit can be programmed in the MP2698 to prevent the input source from being overloaded. When the input current reaches the limit, the charge current tapers off to keep the input current from increasing further.

If the preset input current limit is higher than the adapter rating, the back-up input voltage-based power management also works to prevent the input source from being overloaded. When the input voltage falls below the input voltage regulation point due to the heavy load, the charge current is also reduced to keep the input voltage from dropping further.

System Over-Current Protection (OCP)

The MP2698 also features a system over-current protection (OCP) threshold in charge mode. If the current still exceeds the OCP current (4.5A) after 3ms of blanking time, Q2 is turned off. A fast-off function turns off Q2 quickly when the system current exceeds 8A. After 300ms, Q2 is turned on again to check if the OCP has been removed or not.

Negative Temperature Coefficient (NTC) Thermistor

The IC monitors the battery's temperature continuously by measuring the voltage at the NTC pins in both charge mode and discharge mode. This voltage is determined by the resistive divider, whose ratio is produced by different resistances of the NTC thermistor under different ambient temperatures of the battery.

The IC sets a pre-determined upper and lower bound of the range internally. If the NTC voltage exits this range, then the temperature is outside of the safe operating limit. At this time, charging is stopped unless the operating temperature returns to the safe range.

To satisfy the JEITA requirement, there are four temperature thresholds: the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} < 60°C), and the hot battery threshold (T_{NTC} > 60°C). For a given NTC thermistor, these temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT}.

When V_{NTC} < V_{HOT} or V_{NTC} > V_{COLD}, the charging is suspended. When V_{HOT} < V_{NTC} < V_{WARM}, the battery regulation (charge-full) voltage (V_{BATT_REG}) is reduced by 150mV compared to the programmable threshold. When V_{COOL} < V_{NTC} < V_{COLD}, the charging current is reduced to half of the programmable charge current.

NTC protection can be disabled via REG07 bit[3]. When REG07 bit[3] is set to 0, NTC is disabled, and the VREFNTC is disconnected from VCC.

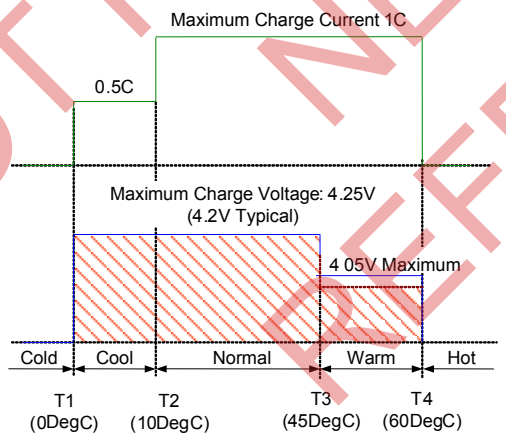


Figure 5: NTC Window

Input USB BC1.2 Detection

The IC contains a DP1/DM1-based input source detection to set the input current limit automatically. DP1/DM1 detection includes a standard USB BC1.2 and non-standard adapter. USB1 BC1.2 detection can be forced in host mode by writing 1 to REG0B bit[0] (see Table 2).

When the input source is plugged in, the USB BC1.2 can identify a standard downstream port (SDP), charging downstream port (CDP), and dedicated charging port (DCP).

Table 2: Input Current Limit vs. USB Type

DP1/DM1 Detection	REG0F [3:0]
Apple 1A	0010
Apple 2.1A	0011
Apple 2.4A	0100
SDP	0101
CDP	0110
DCP	0111

Interrupt to Host (INT)

The IC also has an alert mechanism, which can output an interrupt signal via INT to alert the system of the operation by outputting a 400μs low-state INT pulse. All of the below events can trigger the INT output:

- Good input source detected
- USB2 load is plugged in
- Charge is enabled
- Charge done
- Pre-charge to CC charge
- Battery short
- VIN or IN PPM
- Any fault in REG09

The INT output is designed as an open-drain structure and requires an external pull-up voltage source in real operation.

Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power deliver and avoid overheating the chip. When the internal junction temperature reaches the preset limit, the IC begins reducing the charge current to prevent higher power dissipation.

When the junction temperature reaches 150°C, the pulse-width modulation (PWM) step-down converters are shut down.

Battery Current Analog Output

The IC has an IB pin to get the real-time battery current value in both charge and boost mode. The IB voltage is a fraction of the charge current and indicates the charge current flowing in and out of the battery during charge/boost mode. Calculate this voltage with Equation (1):

$$V_{IB} = I_{BATT} \times 0.41(V) \quad (1)$$

BOOST MODE OPERATION

The IC is able to supply a regulated 5V/3.6A output at SYS for powering the system. The IC does not enter the boost mode if the battery is below the weak battery threshold to ensure that the battery is not drained. To enable boost mode, the input voltage at VIN must be below 1.0V. The boost operation can be enabled when CE is high.

The boost output current limit can be selected as 900mA - 3.6A via I²C (REG05 bit[2:0]). During boost mode, the status register REG08 bit[7:6] is set to 11. Boost operation can be enabled only when the following conditions are valid.

- $V_{BATT} > V_{BATT\_UVLO}$ (2.9V)
- CE is high
- $V_{IN} < 1V$
- REG0DH bit[6] = 0

Once boost is enabled, the IC boosts the PMID to 5.2V first. Then, the block MOSFET (Q2) is regulated linearly with the current limit of I_{OLIM}. When V_{SYS} is charged above 4.75V within 3ms, Q2 is fully turned on. Otherwise, Q2 turns back off and attempts to turn on again after 300ms.

In boost mode, the IC employs a fixed 550kHz PWM step-up switching regulator that switches from PWM operation to pulse-skipping operation at light load.

Battery Under-Voltage Protection (UVLO)

During boost operation, once the battery voltage is below 2.5V, the boost is latched off, and the REG0DH bit[6] is set to 1. When the battery is charged again and V_{BATT} is higher than 2.9V, the REG0DH bit[6] can be reset to 0.

Boost Over-Voltage Protection (OVP)

The MP2698 also features boost output OVP. The IC monitors the voltage at SYS continuously in boost mode. Once V_{SYS} exceeds VOVP_BST, the MP2698 stops switching and turn off Q2. Simultaneously, the REG09 bit[6] is set to 1, and a 25Ω discharge dummy load is turned on to discharge the system voltage to protect the rear-end device. Once VPMID returns to the normal range, the boost and Q2 are turned on again.

Boost Over-Current Limit and Short-Circuit Protection

In normal boost operation, the MP2698 monitors the current flowing through Q2 continuously. When the boost output current exceeds the boost output current limit set via REG05 bit[2:0], the output current loop takes control, and the boost output voltage drops. When V_{SYS} drops below the minimum of 4V and VBATT + 200mV, Q2 is forced off. After 300ms, Q2 turns on again. If V_{SYS} rises higher than 4.75V within 3ms, Q2 is fully on. Otherwise, Q2 is turned off again.

USB2 Plug-In Detection

In sleep mode, SYS is pulled up to VCC with an internal 6kΩ resistor, and the SYS voltage is monitored. Once the system voltage drops to 80% of VCC, the USB2 plug-in is detected, and DP2/DM2 detection is initiated.

Output DP2/DM2 Detection

Once the USB2 plug-in is detected or the PB falling edge is detected, the IC begins DP2/DM2 detection.

Initially, DP2 and DM2 are connected to 2.7V with an internal resistance of 23kΩ, and the DP2/DM2 voltage is monitored. If DP2 or DM2 is lower than 1.7V for 8ms, the 2.7V reference is disconnected, and DP2 and DM2 are tied together with a 100Ω resistor.

Automatic Off at Light Load

The boost turns off automatically if the load current flowing out from SYS is below 80mA for 36s.

Thermal Shutdown Protection in Boost Mode

Thermal shutdown protection is active in boost mode. Once the junction temperature rises above 150°C, the IC enters thermal shutdown and does not resume normal operation until the junction temperature drops below 120°C.

Sleeping Mode

When the input power source is missing and boost is disabled, the IC enters sleep mode. During sleep mode, all MOSFETs are turned off to minimize leakage and extend the battery run-time.

Impedance Compensation for Boost Output

The IC allows the user to compensate the intrinsic resistance of Q2 and the USB2 output cable voltage drop by adjusting the boost output voltage according to the system load current. Additionally, a maximum allowed regulated voltage is set for safety conditions. Calculate the BST system voltage with Equation (2):

$$V_{BST\_SYS} = V_{OUT(BST)} + (I_{SYS} \times R_{SYS\_COMP}) \quad (2)$$

Where V_{BST_SYS} is the boost regulation voltage, $V_{OUT(BST)}$ is the system boost voltage set via the I²C, I_{SYS} is the real-time system load current during the operation, and R_{SYS_COMP} is the line resistance compensation setting in REG01 bit[3:1].

Four Led Drivers for Voltage-Based Battery

The IC provides four LED drivers for voltage-based fuel gauge indication. When USB1 is present, LED1 - LEDx is on with the highest bit blinking. When USB2 is plugged in and boost is enabled, LED1 - LEDx are blinking until the boost is turned off (see Table 3).

The LEDx indication can be controlled by the host. The host determines the LED1 - LEDx on/off function according to the battery voltage result in REG12 and sends a control command to REG13 bit[3:0].

During the voltage measurement, the battery impedance should be compensated via the I²C REG06 bit[7:5] based on the battery current to get a precise battery voltage.

PB Control

PB is used to control the boost mode enable function. A low-to-high rising edge wakes up the device and the boost.

Series Interface

The IC uses an I²C-compatible interface for flexible charging parameters setting and instantaneous device status reporting. The I²C is a bidirectional, two-wire serial interface. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL).

The I²C interface supports both standard mode (up to 100kbits) and fast mode (up to 400kbits).

Table 3: LED Indication Table

Mode	V_{BATT}	SOC	LED1	LED2	LED3	LED4
Charging	V_{BATT} < 3.6V	<25%	Flash	Off	Off	Off
	[3.6V, 3.8V)	[25%, 50%)	On	Flash	Off	Off
	[3.8V, 4.0V)	[50%, 75%)	On	On	Flash	Off
	CV mode,[4.0V, 4.2V), Not terminated	[75%, 100%)	On	On	On	Flash
	V_{BATT} ≥ 4.0, terminated	100%	On	On	On	On
Discharging (all off after 5s)	V_{BATT} ≥ 4.05V	>75%	Flash	Flash	Flash	Flash
	[3.85V, 4.05V)	[50%, 75%)	Flash	Flash	Flash	Off
	[3.65V, 3.85V)	[25%, 50%)	Flash	Flash	Flash	Off
	[V_{BAT_ULVO}, 3.65V)	[0%, 25%)	Flash	Off	Off	Off
	<V_{BAT_ULVO}	[0%, 5%)	Off	Off	Off	Off

Both SDA and SCL are bidirectional lines connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are high. The SDA and SCL are both open-drain pins.

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. One clock pulse is generated for each data bit transferred.

All transactions begin with a start (S) command and can be terminated by a stop (P) command. A high-to-low transition on the SDA line while SCL is high defines a start condition. A low-to-high transition on the SDA line when the SCL is high defines a stop condition.

Start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered to be free after the stop condition. Every byte on the SDA line must be eight bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte must be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed another function, it can hold the clock line (SCL) low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and releases the clock line (SCL).

The acknowledge bit takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was received successfully and another byte may be sent. All clock pulses, including the acknowledge bit (the ninth clock pulse), are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so that the receiver can pull the SDA line low and remains high during the ninth clock pulse. This is the “not acknowledge” signal. The master can then generate either a stop to abort the transfer or a repeated start to begin a new transfer.

After the start, a slave address is sent. This address is seven bits long followed by an eighth data direction bit (r/w). A zero indicates a transmission (write), and a one indicates a request for data (read).

If the register address is not defined, the charger IC sends back NACK and returns to an idle state.

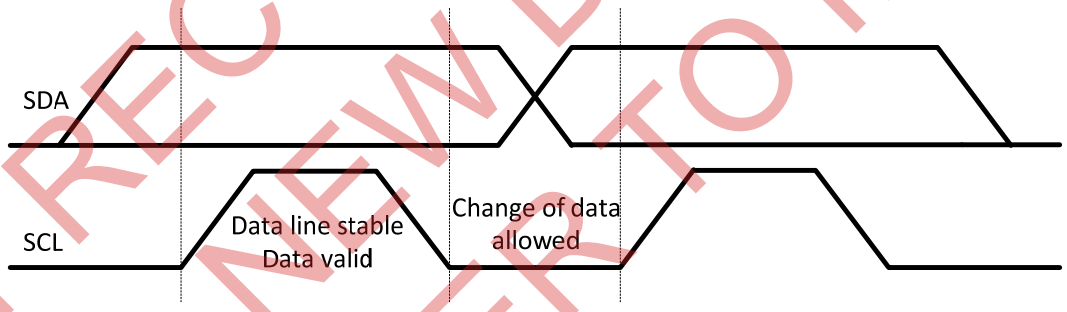


Figure 6: Bit Transfer on the I²C Bus

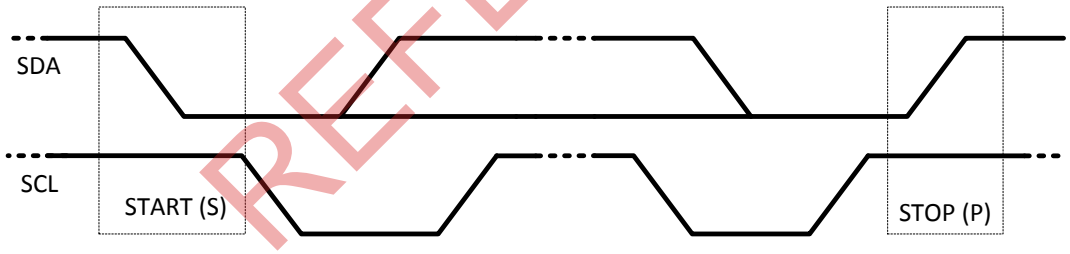


Figure 7: Start and Stop Conditions

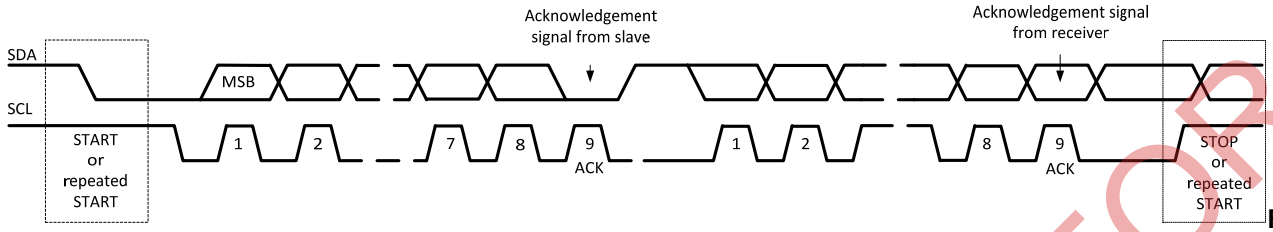


Figure 8: Data Transfer on the I²C Bus

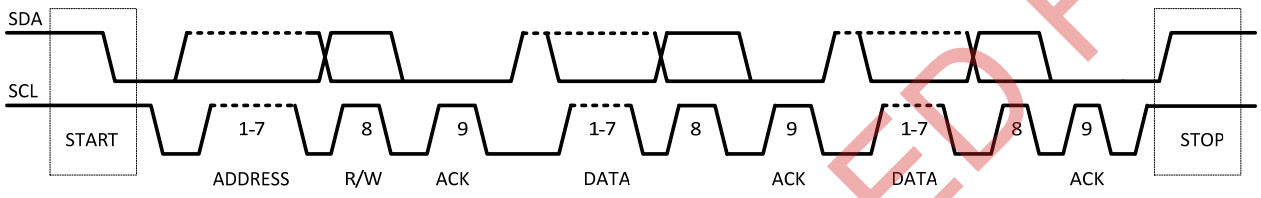


Figure 9: Complete Data Transfer

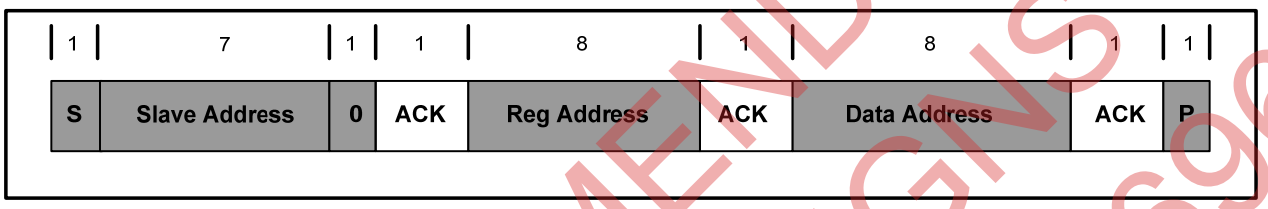


Figure 10: Single Write

Figure 11: Single Read

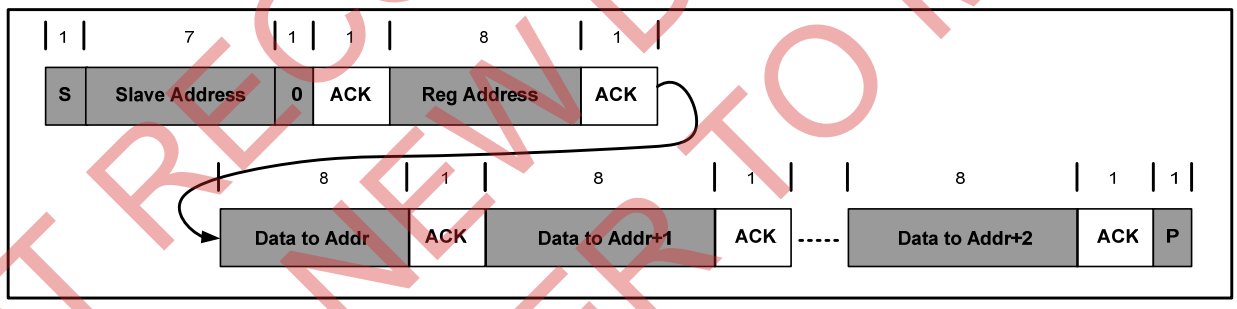


Figure 12: Multi Write

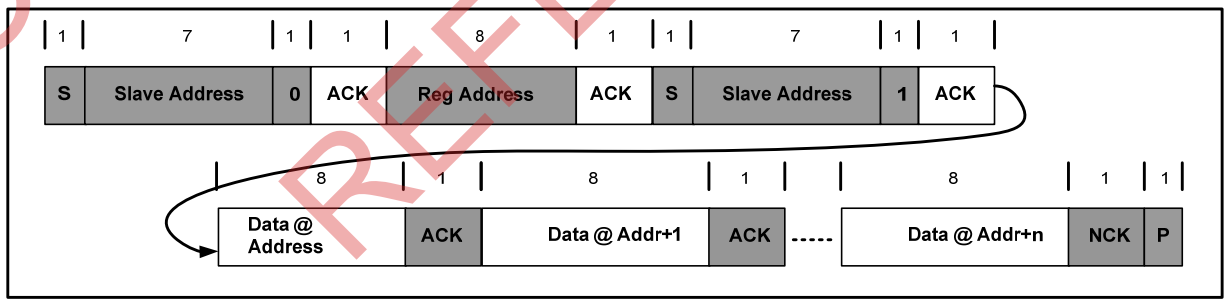


Figure 13: Multi Read

I²C REGISTER MAP

IC Address: 6BH

Register Name	Address	R/W	Description
REG00	0x00	r/w	Input voltage regulation setting and input current limit setting.
REG01	0x01	r/w	USB2 cable impedance compensation and register reset enable.
REG02	0x02	r/w	Charge current setting and safety timer setting.
REG03	0x03	r/w	Pre-charge current setting and termination current level setting.
REG04	0x04	r/w	Battery regulation voltage, pre-charge to CC threshold and auto-recharge threshold.
REG05	0x05	r/w	Boost output current limit setting, charge termination setting.
REG06	0x06	r/w	Battery impedance compensation and junction temperature loop setting.
REG07	0x07	r/w	Miscellaneous control.
REG08	0x08	r	Status register.
REG09	0x09	r	Fault register.
REG0A	0x0A	na	Part information.
REG0B	0x0B	r/w	Charge control register.
REG0C	0x0C	r/w	USB2 protocol control register.
REG0D	0x0D	r	USB2 status register.
REG0E	0x0E	r	USB1 status register.
REG0F	0x0F	r	USB2 detection results.
REG12	0x12	r	Battery real percentage against the battery regulation (charge-full) voltage.
REG13	0x13	r	LED indication control.

REG 00H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_HIZ	0	Y	N	r/w	0: disable 1: enable	Turn off Q1, Q2, Q3, Q4
6	V_{IN_REG} [3]	1	Y	Y	r/w	640mV	Input voltage regulation setting. Offset: 3.88V Range: 0 to 1.2V Default: 800mV (4.68V)
5	V_{IN_REG} [2]	0	Y	Y	r/w	320mV	
4	V_{IN_REG} [1]	1	Y	Y	r/w	160mV	
3	V_{IN_REG} [0]	0	Y	Y	r/w	80mV	
2	IIN_LIM [2]	1	Y	Y	N/A	000: 100mA 001: 500mA 010: 1000mA 011: 1500mA 100: 1800mA 101: 2100mA 110: 2400mA 111: 3000mA	Input current limit setting. Default: 3000mA
1	IIN_LIM [1]	1	Y	Y	N/A		
0	IIN_LIM [0]	1	Y	Y	N/A		

REG 01H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	REG_RST	0	Y	Y	r/w	0: keep current setting 1: reset	Used to reset all registers to default. After reset, this bit goes back to 0 automatically.
6	WTD_TMR_RST	0	Y	N	r/w	0: normal 1: reset	Used to reset the watchdog timer. After reset, this bit goes back to 0 automatically.
5	Q2_EN	0	Y	N	r/w	0: Q2 disable 1: Q2 enable	Only valid when REG0BH bit[6] = 1 .
4	BST_EN	0	Y	Y	r/w	0: boost disable 1: boost enable	Only valid when REG0BH bit[6] = 1.
3	R_{SYS_CMP} [2]	0	Y	Y	r/w	80mΩ	Used to compensate for the USB cable voltage drop. Default: 0mΩ
2	R_{SYS_CMP} [1]	0	Y	Y	r/w	40mΩ	
1	R_{SYS_CMP} [0]	0	Y	Y	r/w	20mΩ	
0	Reserved	0	N/A	N/A	N/A	N/A	Bit reserved.

REG 02H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I_{CC} [5]	0	Y	Y	r/w	3200mA	Charge current setting. RS1: 10mΩ Offset: 500mA Range: 500mA - 5A Default: 2500mA
6	I_{CC} [4]	1	Y	Y	r/w	1600mA	
5	I_{CC} [3]	0	Y	Y	r/w	800mA	
4	I_{CC} [2]	1	Y	Y	r/w	400mA	
3	I_{CC} [1]	0	Y	Y	r/w	200mA	
2	I_{CC} [0]	0	Y	Y	r/w	100mA	
1	CHG_TMR [1]	1	Y	Y	r/w	00: 5hrs 01: 8hrs 10: 12hrs 11: 20hrs	Charge cycle timer setting, if the timer expires, charging is stopped. Default: 20hrs
0	CHG_TMR [0]	1	Y	Y	r/w		

REG 03H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	I_{PRE} [3]	0	Y	Y	r/w	800mA	RS1: 10mΩ Offset: 100mA Range: 100mA - 1600mA Default: 400mA (0011)
6	I_{PRE} [2]	0	Y	Y	r/w	400mA	
5	I_{PRE} [1]	1	Y	Y	r/w	200mA	
4	I_{PRE} [0]	1	Y	Y	r/w	100mA	
3	I_{TERM} [3]	0	Y	Y	r/w	800mA	RS1: 10mΩ Offset: 200mA Range: 200mA - 1700mA Default: 200mA (0000)
2	I_{TERM} [2]	0	Y	Y	r/w	400mA	
1	I_{TERM} [1]	0	Y	Y	r/w	200mA	
0	I_{TERM} [0]	0	Y	Y	r/w	100mA	

REG 04H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	V_{BATT_REG} [5]	1	Y	Y	r/w	800mV	Offset: 3.1V Range: 3.1V - 4.675V Default: 4.35V (110010)
6	V_{BATT_REG} [4]	1	Y	Y	r/w	400mV	
5	V_{BATT_REG} [3]	0	Y	Y	r/w	200mV	
4	V_{BATT_REG} [2]	0	Y	Y	r/w	100mV	
3	V_{BATT_REG} [1]	1	Y	Y	r/w	50mV	
2	V_{BATT_REG} [0]	0	Y	Y	r/w	25mV	
1	V_{BATT_PRE}	1	Y	Y	r/w	0: 2.8V 1: 3.0V	Default: 3.0V
0	V_{RECH}	1	Y	Y	r/w	0: 100mV 1: 200mV	Default: 200mV

REG 05H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	EN_TERM	1	Y	Y	r/w	0: disable 1: enable	Default: enable
6	TERM_STAT	0	Y	Y	r/w	0: match I_{TERM} 1: indicate before the actual termination (500mA higher) on STAT	Default: match I_{TERM}
5	WTD_TMR [1]	0	Y	N	r/w	00: disable timer 01: 40s 10: 80s 11: 160s	Default: 40s
4	WTD_TMR [0]	1	Y	N	r/w		
3	EN_ TIMER	1	Y	Y	r/w	0: disable 1: enable	Used to enable the charge cycle timer. Default: enable
2	I_{OLIM}[2]	1	Y	Y	r/w	000: 900mA 001: 1200mA 010: 1500mA 011: 1800mA 100: 2000mA 101: 2400mA 110: 3000mA 111: 3600mA	Default: 3600mA
1	I_{OLIM}[1]	1	Y	Y	r/w		
0	I_{OLIM}[0]	1	Y	Y	r/w		

REG 06H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	R_{BATT_CMP} [2]	0	Y	Y	r/w	80mΩ	Used to compensate for the battery internal resistance and protection IC resistance. Default: 0mΩ
6	R_{BATT_CMP} [1]	0	Y	Y	r/w	40mΩ	
5	R_{BATT_CMP} [0]	0	Y	Y	r/w	20mΩ	
4	Reserved	0	N/A	N/A	N/A	N/A	Bit reserved.
3	Reserved	0	N/A	N/A	N/A	N/A	
2	Reserved	0	N/A	N/A	N/A	N/A	
1	T_{REG} [1]	1	Y	Y	r/w	00: 60°C 01: 80°C 10:100°C 11:120°C	Default: 120°C
0	T_{REG} [1]	1	Y	Y	r/w		

REG 07H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	USB_DET_EN	0	Y	Y	r/w	0: not in DP/DM detection 1: forced DP/DM detection	Used to detect DM1/DP1 and DM2/DP2. After reset, this bit go back to 0 automatically.
6	Reserved	0	N/A	N/A	r/w	N/A	Bit reserved.
5	Reserved	0	Y	Y	r/w	N/A	Must be set to 0.
4	Reserved	0	Y	Y	r/w	N/A	Must be set to 0.
3	EN_NTC	1	Y	Y	r/w	0: disable 1: enable	Default: enable
2	Q1_DIS	0	Y	N	r/w	0: Q1 is forced on 1: Q1 is forced off	Default: forced on
1	INT_MASK [1]	1	Y	Y	r/w	0: no INT during CHG_FAULT 1: INT in CHG_FAULT	Default: INI in CHG_FAULT
0	INT_MAST [0]	1	Y	Y	r/w	0: no INT during BAT_FAULT 1: INT in BAT_FAULT	Default: INI in BAT_FAULT

REG 08H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	CHIP_STAT [1]	0	Y	Y	r	00: none 01: USB1 is SDP or CDP 10: USB1 is DCP or Apple 11: boost	
6	CHIP_STAT [0]	0	Y	Y	r		
5	CHG_STAT [1]	0	Y	Y	r	00: not charging 01: trickle charge 10: charge 11: charge done	
4	CHG_STAT [0]	0	Y	Y	r		
3	PPM_STAT	0	Y	Y	r	0: no PPM 1: VINPPM or IINPPM	
2	PG_STAT	0	Y	Y	r	0: VIN not good 1: VIN good	V_{IN} > 3.45V and V_{IN} > V_{BATT} + 460mV
1	THERM_ STAT	0	Y	Y	r	0: normal 1: thermal regulation	
0	Reserved	0	N/A	N/A	N/A	N/A	Bit reserved.

REG 09H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	WATCHDOG _FAULT	0	Y	N	r	0: normal 1: watchdog timer expiration	
6	BST_ FAULT	0	Y	Y	r	0: normal 1: SYS short circuit, or PMID OVP, battery UVLO	
5	IC_FAULT [1]	0	Y	Y	r	000: normal 010: USB1 UV or OV 101: thermal shutdown 110: safety timer expiration 001: battery OVP	
4	IC_FAULT [0]	0	Y	Y	r		
3	IC_FAULT	0	Y	Y	r		
2	NTC_ FAULT [2]	0	Y	Y	r	000: normal 001: NTC cold 010: NTC cool 011: NTC warm 100: NTC hot	
1	NTC_ FAULT [1]	0	Y	Y	r		
0	NTC_ FAULT [0]	0	Y	Y	r		

REG 0AH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
6	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
5	PN [2]	0	N	N	r	011: MP2698	
4	PN [1]	1	N	N	r		
3	PN [0]	1	N	N	r		
2	NTC_ TYPE	1	N	N	r	0: standard 1: JEITA	
1	Rev [1]	0	N	N	r	00: first rev	
0	Rev [0]	0	N	N	r		

REG 0BH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VIN_DSG	0	Y	Y	w	0: disable VIN discharge 1: enable VIN discharge	
6	I2C_CTRL	1	Y	N	w	1: enable I²C control mode	1: I²C mode, the protocol can be implemented step-by-step by the MCU. Write this bit to 1 after power-up.
5	USB1_ RDY	1	Y	N	w	0: disable USB1 charge 1: enable USB1 charge	
4	Reserved	0	Y	Y	w	N/A	Bit reserved.
3	Reserved	0	Y	Y	w	N/A	Bit reserved.
2	Reserved	0	Y	Y	w	N/A	Bit reserved.
1	Reserved	0	Y	Y	w	N/A	Bit reserved.
0	USB1_EN_ DET	0	Y	Y	w	0: disable USB1 type detection 1: start USB1 type detection	Used to detect DM1/DP1. After reset, this bit goes back to 0 automatically.

REG 0CH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	IBATT_P K[2]	1	Y	Y	r/w	000: 3.3A 001: 5.7A 010: 4.5A 011: 6.8A 100: 8.0A	Program the peak current limit of the switching MOSFETs. In buck mode, set these bits to 100.
6	IBATT_P K[1]	0	Y	Y	r/w		
5	IBATT_P K[0]	0	Y	Y	r/w		
4	SYS_DSG	0	Y	Y	r/w	0: disable SYS discharge 1: enable SYS discharge	
3	Reserved	1	N/A	N/A	N/A	N/A	Bit reserved.
2	Reserved	0	N/A	N/A	N/A	N/A	Bit reserved.
1	USB2_EN_DET	0	Y	Y	r/w	0: disable USB2 type detection 1: start USB2 type detection	Used to detect DM2/DP2. After reset, this bit goes back to 0 automatically.
0	USB2_EN_PLUG	0	Y	Y	r/w	0: disable USB2 plug-in detection 1: enable USB2 plug-in detection	

REG 0DH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
6	BATT_UVLO	0	Y	N	r	0: battery not ULVO 1: battery UVLO	When battery UVLO occurs, this bit is set to 1. Boost is latched off. This bit is reset to 0 when the battery is charged again and V_{BATT} is higher than 2.9V.
5	Q2_OC	0	Y	Y	r	0: Q2 not over current 1: Q2 over current	REG01H bit[7] > 0 to clear this bit.
4	Reserved	0	N/A	N/A	N/A	N/A	Bit reserved for SYS short circuit.
3	PMID_OK	0	Y	Y	r	0: PMID voltage is not good 1: PMID voltage is good	
2	USB2_plug_in	0	Y	Y	r	0: USB2 is not plugged in 1: USB2 is plugged in	
1	USB1_plug_in	0	Y	Y	r	0: USB1 is not plugged in 1: USB1 is plugged in	V_{IN} > 3.45V and V_{IN} > V_{BATT} + 460mV
0	USB1_GT_1V	0	Y	Y	r	0: USB1 voltage is not greater than 1V 1: USB1 voltage is greater than 1V	

REG 0EH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
6	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
5	USB1_OV	0	Y	Y	r	0: USB1 not over voltage 1: USB1 over voltage	
4	USB1_UV	0	Y	Y	r	0: USB1 not under voltage 1: USB1 under voltage	
3	Reserved	0	Y	Y	r	N/A	Bit reserved.
2	Reserved	0	Y	Y	r	N/A	Bit reserved.
1	Reserved	0	Y	Y	r	N/A	Bit reserved.
0	Reserved	0	Y	Y	r	N/A	Bit reserved.

REG 0FH

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
6	USB2_ TYPE[2]	0	Y	Y	r	000: none 001: SDP 010: Apple 011: DCP	Auto-generated by USB2-type detection.
5	USB2_ TYPE[1]	0	Y	Y	r		
4	USB2_ TYPE[0]	0	Y	Y	r		
3	USB1_ TYPE[3]	0	Y	Y	r	0000: none 0001: SAMSUNG 1.2V 0010: Apple 1A 0011: Apple 2.1A 0100: Apple 2.4A 0101: SDP 0110: CDP 0111: DCP	Auto-generated by the USB1-type detection.
2	USB1_ TYPE[2]	0	Y	Y	r		
1	USB1_ TYPE[1]	0	Y	Y	r		
0	USB1_ TYPE[0]	0	Y	Y	r		

REG 12H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	VBATT [7]	0	Y	Y	r	$V_{BATT\_REG}/2$	
6	VBATT [6]	0	Y	Y	r	$V_{BATT\_REG}/4$	
5	VBATT [5]	0	Y	Y	r	$V_{BATT\_REG}/8$	
4	VBATT [4]	0	Y	Y	r	$V_{BATT\_REG}/16$	
3	VBATT [3]	0	Y	Y	r	$V_{BATT\_REG}/32$	
2	VBATT [2]	0	Y	Y	r	$V_{BATT\_REG}/64$	
1	VBATT [1]	0	Y	Y	r	$V_{BATT\_REG}/128$	
0	VBATT [0]	0	Y	Y	r	$V_{BATT\_REG}/256$	

REG 13H

Bit	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
7	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
6	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
5	Reserved	N/A	N/A	N/A	N/A	N/A	Bit reserved.
4	EN_LED_CTRL	0	Y	N	r/w	0: disable I^2C write FG_LEDs on/off 1: enable I^2C write FG_LEDs on/off	
3	LED[3]	0	Y	N	r/w	0: off 1: on	
2	LED[2]	0	Y	N	r/w	0: off 1: on	
1	LED[1]	0	Y	N	r/w	0: off 1: on	
0	LED[0]	0	Y	N	r/w	0: off 1: on	

OTP MAP

#	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	**N/A**	Vin regulation voltage				Iin limit		
0x02	Charge current						**N/A**	
0x03	Pre-charge current				Termination current			
0x04	Battery regulation voltage						**N/A**	
0x05	**N/A**					SYS output current limit		
0x0B	**N/A**		USB1 Charge enabled/disabled	**N/A**				

OTP DEFAULT

OTP Items	Default
Vin regulation voltage	4.68V
Iin limit	3000mA
Charge current	2500mA
Pre-charge current	400mA
Termination current	200mA
Battery regulation voltage	4.35V
SYS output current limit	3.6A
USB1 charge enabled/disabled	Enable USB1 charge

APPLICATION INFORMATION

NTC Function in Charge Mode

An internal resistor divider sets the low temperature threshold (V_{COLD}) and high temperature threshold (V_{HOT}) at 71%·$V_{VREFNTC}$ and 48.1%·$V_{VREFNTC}$, respectively. For a given NTC thermistor, select an appropriate R_{T1} and R_{T2} to set the NTC window using Equation (3) and Equation (4):

$$\frac{V_{COLD}}{V_{VREFNTC}} = \frac{R_{T2} // R_{NTC\_COLD}}{R_{T1} + R_{T2} // R_{NTC\_COLD}} = T_{COLD} = 71\% \quad (3)$$

$$\frac{V_{HOT}}{V_{VREFNTC}} = \frac{R_{T2} // R_{NTC\_HOT}}{R_{T1} + R_{T2} // R_{NTC\_HOT}} = T_{HOT} = 48.1\% \quad (4)$$

Where R_{NTC_HOT} is the value of the NTC resistor at the upper bound of its operating temperature range, and R_{NTC_COLD} is the value of the NTC resistor at the lower bound of its operating temperature range.

The two resistors, R_{T1} and R_{T2}, determine the upper and lower temperature limits independently. This flexibility allows the MP2638 to operate with most NTC resistors for different temperature range requirements. Calculate R_{T1} and R_{T2} with Equation (5) and Equation (6):

$$R_{T1} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (T_{COLD} - T_{HOT})}{T_{COLD} \times T_{HOT} \times (R_{NTC\_COLD} - R_{NTC\_HOT})} \quad (5)$$

$$R_{T2} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (T_{COLD} - T_{HOT})}{T_{HOT} \times (1 - T_{COLD}) \times R_{NTC\_COLD} - T_{COLD} \times (1 - T_{HOT}) \times R_{NTC\_HOT}} \quad (6)$$

For example, the NCP18XH103 thermistor has the following electrical characteristics:

- At 0°C, R_{NTC_Cold} = 27.22kΩ
- At 50°C, R_{NTC_Hot} = 4.16kΩ

Based on Equation (5) and Equation (6), R_{T1} = 3.29kΩ and R_{T2} = 11.46kΩ are suitable for an NTC window between 0°C and 50°C. Choose approximate values (e.g.: R_{T1} = 3.32kΩ and R_{T2} = 11.5kΩ).

If no external NTC is available, connect R_{T1} and R_{T2} to keep the voltage on the NTC pin within the valid NTC window (e.g.: R_{T2} = 10kΩ, R_{T1} = 5.1kΩ).

For convenience, an NTC thermistor design spreadsheet is available for reference. Contact an MPS FAE for this spreadsheet if necessary.

Selecting the Inductor

Inductor selection is a trade-off between cost, size, and efficiency. A lower inductance value corresponds with smaller size but results in higher current ripple, higher magnetic hysteretic losses, and higher output capacitances. However, a higher inductance value benefits from lower ripple current and smaller output filter capacitors, but results in higher inductor DC resistance (DCR) loss.

Choose an inductor that will not saturate under the worst-case load condition.

When the MP2698 works in charge mode (as a buck converter), estimate the required inductance with Equation (7):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L\_MAX}} \times \frac{V_{BATT}}{V_{IN} \times f_{SW}} \quad (7)$$

Where V_{IN} is the typical input voltage, V_{BATT} is the CC charge threshold, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to-peak inductor current (usually 30 - 40% of the CC charge current).

For a typical 5V input voltage and 35% inductor current ripple at the corner point between trickle charge and CC charge (V_{BATT} = 3V, I_{CC} = 2.5A), an inductance of 2.2μH fits best.

When the MP2698 works in boost mode (as a boost converter), the required inductance value can be calculated with Equation (8), Equation (9), and Equation (10):

$$L = \frac{V_{BATT} \times (V_{SYS} - V_{BATT})}{V_{SYS} \times f_{SW} \times \Delta I_{L\_MAX}} \quad (8)$$

$$\Delta I_{L\_MAX} = 30\% \times I_{BATT(MAX)} \quad (9)$$

$$I_{BATT(MAX)} = \frac{V_{SYS} \times I_{SYS(MAX)}}{V_{BATT} \times \eta} \quad (10)$$

Where V_{BATT} is the minimum battery voltage, f_{SW} is the switching frequency, ΔI_{L_MAX} is the peak-to-peak inductor ripple current (approximately 30% of the maximum battery current $I_{BATT(MAX)}$), $I_{SYS(MAX)}$ is the system current, and η is the efficiency.

The worst-case inductor current ripple occurs when the battery voltage is 3V and the boost output (V_{SYS}) is 5V. Considering 90% efficiency and 1.5µH inductance, a 30% inductor current ripple results.

For best results, use an inductor with an inductance of 2.2µH with a DC current rating no lower than the peak current of the MOSFET.

For higher efficiency, minimize the inductor's DC resistance.

Selecting the Input Capacitor (C_{IN})

The input capacitor (C_{IN}) reduces both the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high-frequency switching current from passing to the input. For best results, ceramic capacitors with X7R dielectrics are recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Selecting the PMID Capacitor (C_{PMID})

Select C_{PMID} at PMID based on the demand of the system current ripple.

In charge mode, the capacitor (C_{PMID}) acts as the input capacitor of the buck converter. The input current ripple can be calculated with Equation (11):

$$I_{RMS\_MAX} = I_{CC\_MAX} \times \frac{\sqrt{V_{TC} \times (V_{IN\_MAX} - V_{TC})}}{V_{IN\_MAX}} \quad (11)$$

In boost mode, the capacitor (C_{PMID}) is the output capacitor of the boost converter. C_{SYS} keeps the system voltage ripple small and ensures feedback loop stability. The system current ripple can be calculated with Equation (12):

$$I_{RMS\_MAX} = I_{SYS\_MAX} \times \frac{\sqrt{V_{TC} \times (V_{SYS\_MAX} - V_{TC})}}{V_{SYS\_MAX}} \quad (12)$$

Since the input voltage passes to the system directly, V_{IN_MAX} = V_{SYS_MAX}, and both charge mode and boost mode have the same system current ripple.

For I_{CC_MAX} = 5.0A while I_{SYS_MAX} = 3.6A, V_{TC} = 3V, V_{IN_MAX} = 6V, the maximum ripple current is about 2A. Select the PMID capacitors based on the ripple current temperature rise not exceeding 10°C. For best results, use ceramic capacitors with X7R dielectrics with low ESR and small temperature coefficients. For most applications, use three 22µF capacitors.

Selecting the Battery Capacitor (C_{BATT})

The battery capacitor (C_{BATT}) is in parallel with the battery to absorb the high-frequency switching ripple current.

In charge mode, the capacitor (C_{BATT}) is the output capacitor of the buck converter. The output voltage ripple can be calculated with Equation (13):

$$\Delta r_{BATT} = \frac{\Delta V_{BATT}}{V_{BATT}} = \frac{1 - V_{BATT} / V_{SYS}}{8 \times C_{BATT} \times f_{SW}^{2} \times L} \quad (13)$$

In boost mode, the capacitor (C_{BATT}) is the input capacitor of the boost converter. The input voltage ripple is the same as the output voltage ripple calculated from Equation (13).

Both charge mode and boost mode have the same battery voltage ripple. The capacitor (C_{BATT}) can be calculated with Equation (14):

$$C_{BATT} = \frac{1 - V_{TC} / V_{SYS\_MAX}}{8 \times \Delta r_{BATT\_MAX} \times f_{SW}^{2} \times L} \quad (14)$$

To guarantee ±0.5% BATT voltage accuracy, the maximum BATT voltage ripple must not exceed 0.5% (e.g.: 0.2%). The worst-case scenario occurs at the minimum battery voltage of the CC charge with the maximum input voltage.

For V_{SYS_MAX} = 6V, V_{CC_MIN} = V_{TC} = 3V, L = 2.2µH, f_{SW} = 550kHz, Δr_{BATT_MAX} = 0.2%, and C_{BATT} is 39µF.

Two 22µF ceramic capacitors with X7R dielectrics capacitor in parallel are sufficient.

PCB Layout Guide Lines

Efficient PCB layout is critical for meeting specified noise, efficiency, and stability requirements. Use a star-ground design to keep the circuit block currents isolated (power-signal/control-signal), which reduces noise-coupling and ground-bounce issues. A single ground plane for this design provides good results. For best results, follow the guidelines below.

1. Minimize the high-side switching node (SW, inductor) trace lengths in the high-current paths.
2. Keep the switching node short and away from all small control signals, especially the feedback network.
3. Place the input capacitor as close to VIN and PGND as possible.
4. Place the local power capacitors, connected from the PMID to PGND, as close to the IC as possible.
5. Place the output inductor close to the IC.
6. Connect the output capacitor between the inductor and PGND of the IC.
7. Connect the power pads for VIN, PMID, SYS, SW, BATT, and PGND to as many coppers planes on the board as possible for high-current applications.

   This improves thermal performance because the board conducts heat away from the IC.

TYPICAL APPLICATION CIRCUIT

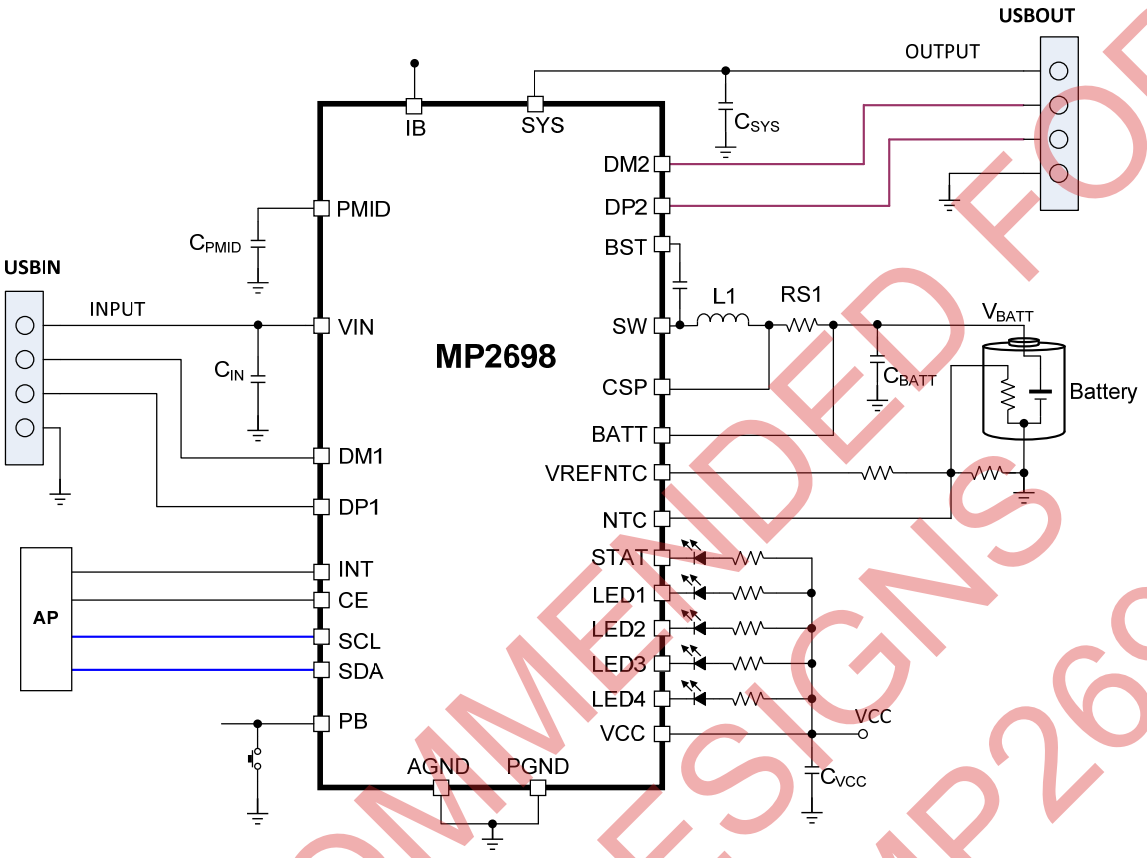


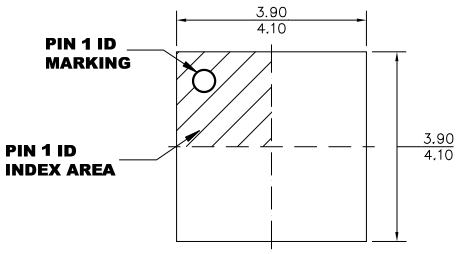
Figure 14: MP2698 Application Circuit

Table 4: Key BOM of Figure 14

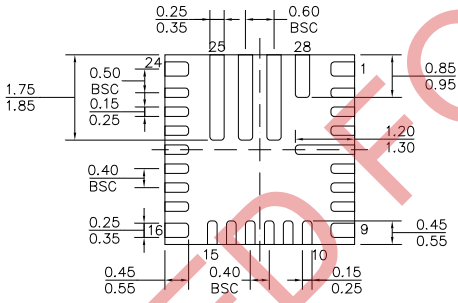
Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	10μF	Ceramic Capacitor;10V; X5R or X7R	1206	Any
3	C_{PMID}	22μF*3	Ceramic Capacitor;10V; X5R or X7R	1206	Any
1	C_{SYS}	1μF	Ceramic Capacitor;10V; X5R or X7R	0603	Any
2	C_{BATT}	22μF*2	Ceramic Capacitor;6.3V; X5R or X7R	0805	Any
1	C_{VCC}	10uF	Ceramic Capacitor;6.3V; X5R or X7R	0603	Any
1	RS1	10mΩ	Film Resistor;1%	1210	Any
1	L1	2.2μH	Inductor;2.2μH;Low DCR;I_{SAT}>6A	SMD	Any

PACKAGE INFORMATION

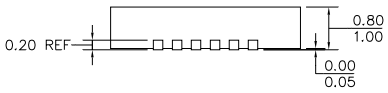
QFN-28 (4mmx4mm)



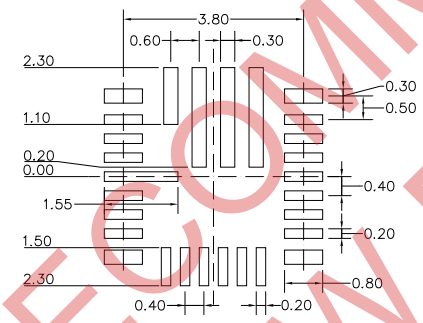
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN 1,9,16 AND 24 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 25~27 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-220.
6) DRAWING IS NOT TO SCALE.