The Future of Analog IC Technology

MP2910

Synchronous Buck PWM DC-DC and Linear Power Controller

DESCRIPTION

The MP2910 is a dual output with one synchronous buck PWM and one linear controller. The part is used to generate logic-supply voltages for PC based systems. MP2910 includes internal soft-start, frequency-compensation networks, power good signaling with specific sequence, and it comes all of the logic control, output adjustment, power monitoring and protection functions into a small footprint package. The part is operated at fixed 300 kHz frequency providing an optimum compromise between efficiency, external component size, and cost. The linear controller is implemented to drive an external MOSFET for regulation and it's adjustable by setting external resistors. Moreover the specific internal PG sequence and indicator is also implemented to conform to Intel® new platform requirement on FSB_VTT power plane. An adjustable over-current protection (OCP) is proposed to monitor the voltage drop across the $R_{DS(ON)}$ of the lower MOSFET for synchronous buck PWM DC-DC controller.

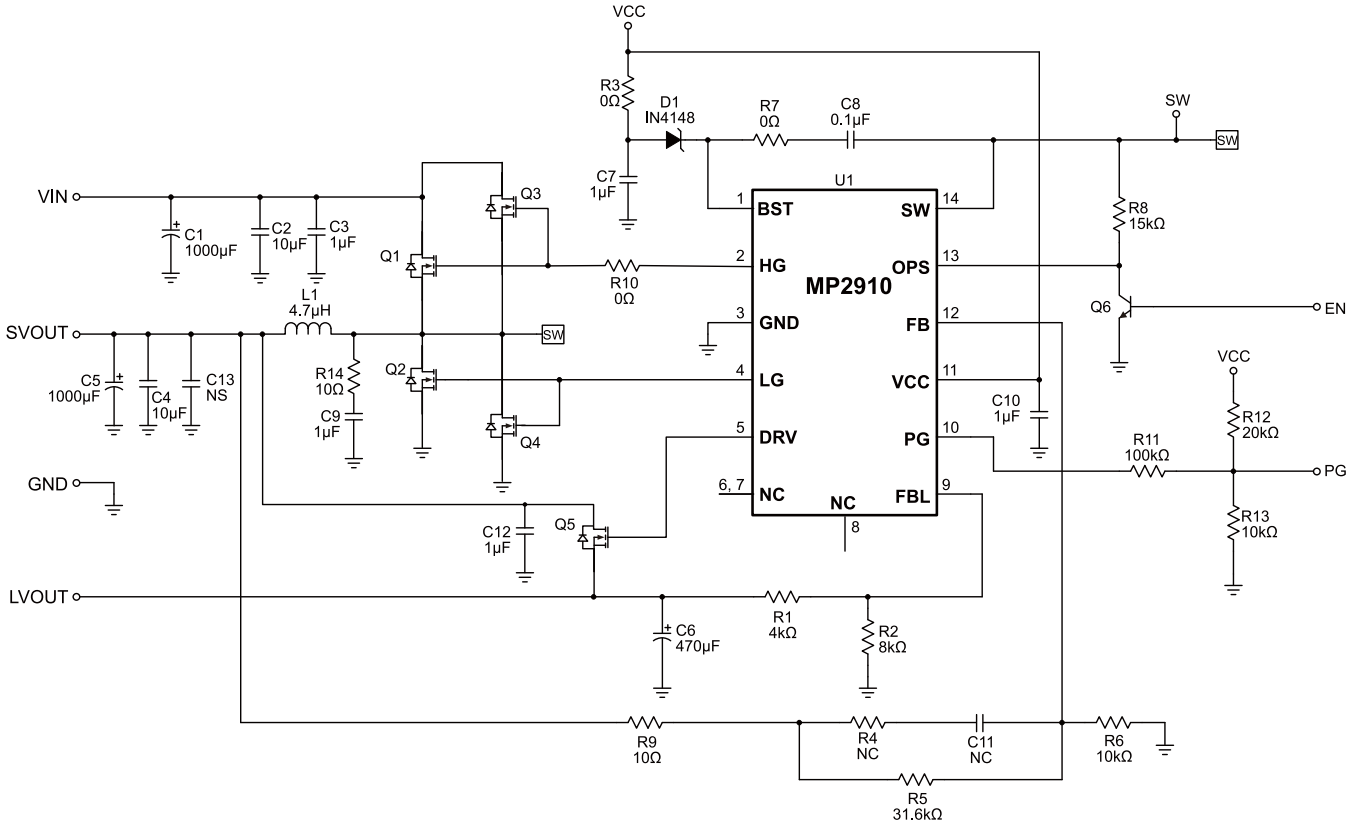
FEATURES

- Operating with 5V or 12V Supply Voltage
- Drives ALL Low Cost N-Channel MOSFETs
- Voltage Mode PWM Control
- 300kHz Fixed Frequency Oscillator
- Fast Transient Response:
  - High speed GM Amplifier
  - Full 0 to 100% Duty Ratio
- Internal Soft-Start
- Adaptive Non-Overlapping Gate Driver
- Over-Current Fault Monitor on MOSFET, No Current Sense Resistor Required
- Specific Power Good Indicator for Intel® Grantsdale FSB_VTT Power Sequence
- Available in a SOIC-14 Package and a SOIC8E Package.

APPLICATIONS

- Graphic Card
- Motherboard, Desktop Servers
- IA Equipments
- Telecomm Equipments
- High Power DC-DC Regulators

TYPICAL APPLICATION



ORDERING INFORMATION

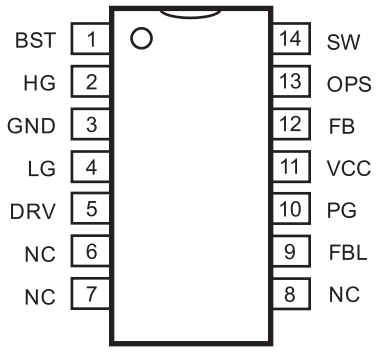
Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP2910ES*	SOIC14	MP2910ES	–20°C to +85°C
MP2910EN**	SOIC8E	MP2910EN	

* For Tape & Reel, add suffix –Z (e.g. MP2910ES–Z);
For RoHS, compliant packaging, add suffix –LF (e.g. MP MP2910ES–LF–Z).

** For Tape & Reel, add suffix –Z (e.g. MP2910EN–Z);
For RoHS, compliant packaging, add suffix –LF (e.g. MP MP2910EN–LF–Z).

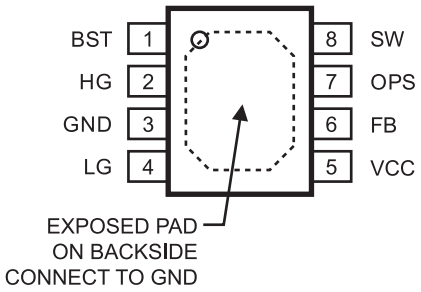
PACKAGE REFERENCE

TOP VIEW



SOIC14

TOP VIEW



SOIC8E

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{CC} 16V
BST, V_{BST}-V_{SW} 16V
SW to GND
DC……..-5 to 15V
<200nS……-10 to 30V
HG……V_{SW}-0.3V to V_{BST}+0.3V
LG……..-0.3V to VCC+0.3V
All Other Pins .....–0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC14 ..... 1.5W
SOIC8E..... 2.6W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{CC} .....5V±5%,12±10%
Operating Junct. Temp (T_J)..... –20°C to +125°C
Ambient Temperature range ..... –20°C to +85°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC8E.....48 ..... 10 ... °C/W
SOIC14 .....86 ..... 38 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V/12V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Nominal Supply Current	I_{CC}	UGATE AND LGATE OPEN		2.7	4	mA
Power-On Reset						
POR Threshold	V_{CCRTH}	V_{CC} Rising	3.8	4.1	4.4	V
Hysteresis	V_{CCHYS}		0.15	0.4		V
Switcher Reference						
Reference Voltage	V_{REF}	V_{CC}=12V	0.784	0.8	0.816	V
Oscillator						
Free Running Frequency	f_{OSC}	V_{CC}=12V	240	290	340	kHz
Ramp Amplitude	ΔV_{OSC}			1.5		V
Error Amplifier						
EA Transconductance	Gm			0.2		ms
Open Loop DC Gain	A_O			85		DB
Linear Regulator						
DRV Driver Source	I_{DS}	V_{DRV}=6V		2.3		mA
Reference Voltage	V_{REF}	V_{CC}=12V	0.784	0.8	0.816	V
PWM Controller Gate Drivers (VCC=12V)						
Upper Gate Source	I_{HG}	$V_{BST} - V_{SW}$ = 12V $V_{HG} - V_{SW}$ = 6V	0.6	1		A
Upper Gate Sink	R_{HG}	$V_{BST} - V_{SW}$ = 12V $V_{HG} - V_{SW}$ = 1V		4	6	Ω
Lower Gate Source	I_{LG}	V_{CC} = 12V, V_{LG} = 6V	0.6	1		A
Lower Gate Sink	R_{LG}	V_{CC} = 12V, V_{LG}= 1V		2.8	3.8	Ω
Dead Time	T_{DT}			25	100	ns
Protection						
FB Under-Voltage Trip		FB Falling	75	82.5	90	%
FBL Under-Voltage Trip		FB and FBL Falling	75	82.5	90	%
OC Current Source	I_{OC}	V_{SW} = 0V		38		μA
Soft-Start Interval	T_{SS}			2.5		ms
Power Good						
Power Good Rising Threshold		V_{CC}=12V		90		%
Power Good Hysteresis		V_{CC}=12V		10		%
PG Sink Capability		V_{CC}=12V, 1mA		0.02	0.4	V
Power Good Rising Delay		V_{CC}=12V	1	4	10	ms
Power Good Falling Delay		V_{CC}=12V		15		μs

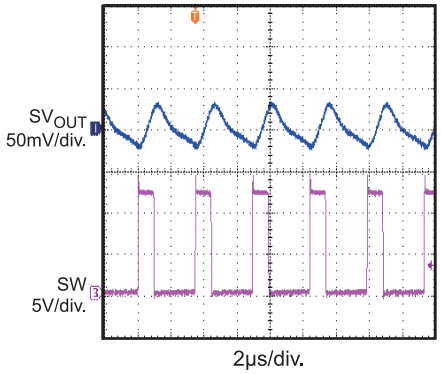
PIN FUNCTIONS

SOIC14 Pin #	SOIC8E Pin #	Name	Description
1	1	BST	Bootstrap supply pin for the upper gate driver. Connect the bootstrap capacitor between BST pin and the SW pin
2	2	HG	Upper gate driver output. Connect to gate of the high side power N-MOSFET.
3	3	GND	Both signal and power ground for the IC
4	4	LG	Lower gate drive output. Connect to gate of the low-side power N-MOSFET
5		DRV	This pin provides the drive for the linear regulator's pass transistor/MOSFET.
6, 7, 8		NC	No internal connection
9		FBL	Linear regulator feedback voltage.
10		PG	PG is an open-drain output used to indicate that the regulator is within normal operating voltage ranges
11	5	V_{CC}	Connect this pin to a well-decoupled 5V or 12V bias supply. It is also the positive supply for the lower gate driver, LG.
12	6	FB	Switcher feedback voltage. This pin is the inverting input of the error amplifier.
13	7	OPS	This pin provides multi-function of the over-current setting, HG turn-on POR sensing, and shut-down features.
14	8	SW	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET.

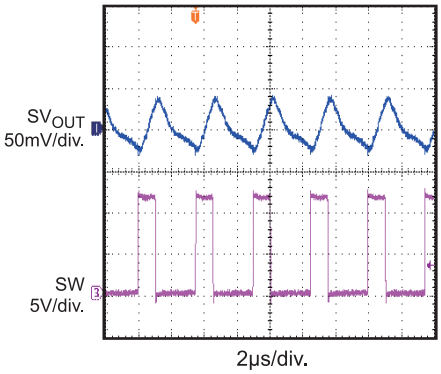
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, SV_{OUT}=3.3V, L1=4.7µF, C_5=1000µF, LVout=1.2V, T_A=25°C, unless otherwise noted.

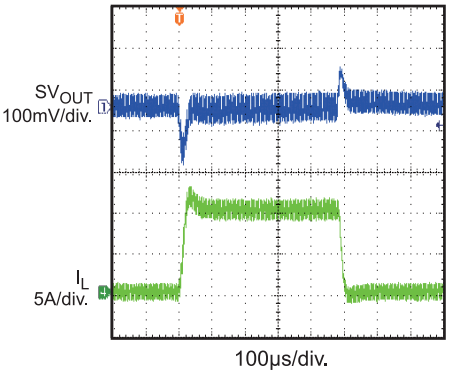
Output Ripple
V_{CC}=12V, I_{LOAD}=0A



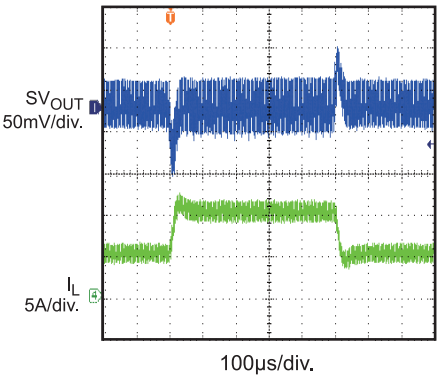
Output Ripple
V_{CC}=12V, I_{LOAD}=10A



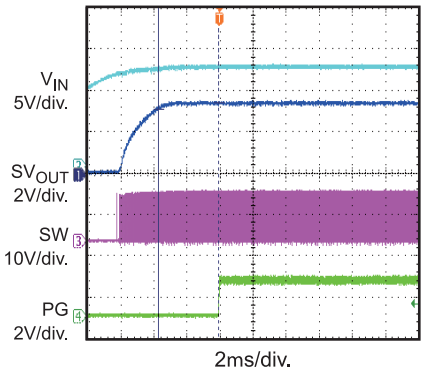
Tansient Response
I_{OUT}=0A to 10A resistive load, slew rate=2.5A/µs



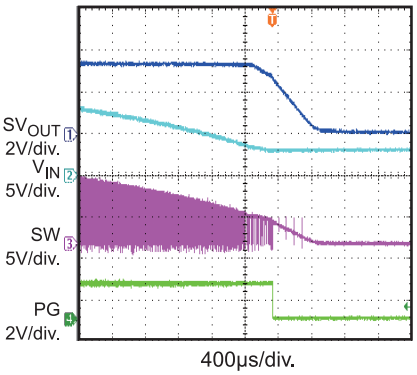
Tansient Response
I_{OUT}=5A to 10A resistive load, slew rate=2.5A/µs



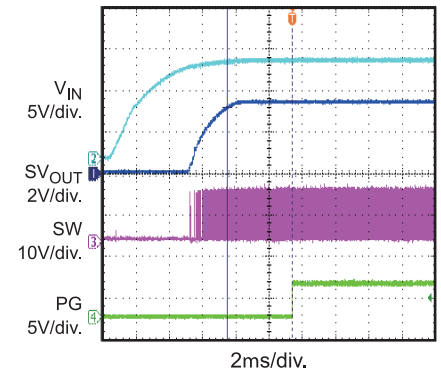
Power Good
V_{CC}=5V, I_{LOAD}=5A



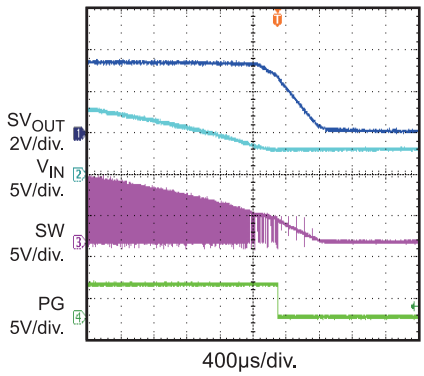
Power Good
V_{CC}=5V, I_{LOAD}=5A



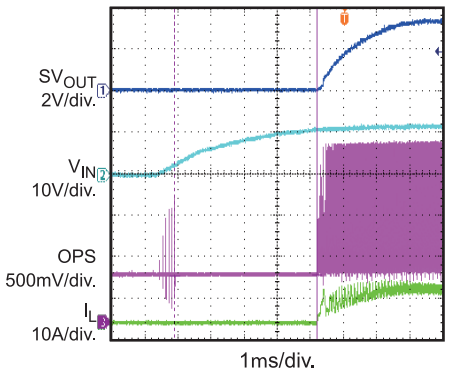
Power Good
V_{CC}=12V, I_{LOAD}=5A



Power Good
V_{CC}=12V, I_{LOAD}=5A



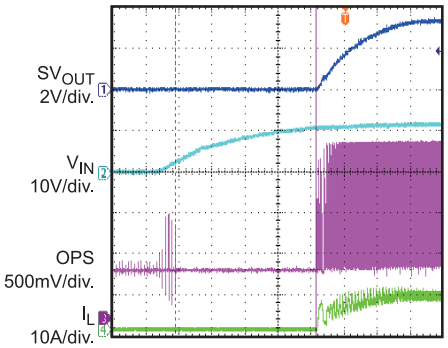
V_{IN} Start Up
V_{CC}=5V, I_{LOAD}=8A



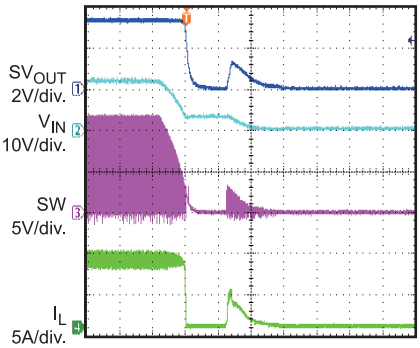
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, SV_{OUT}=3.3V, L1=4.7µF, C_5=1000µF, LVout=1.2V, T_A=25°C, unless otherwise noted.

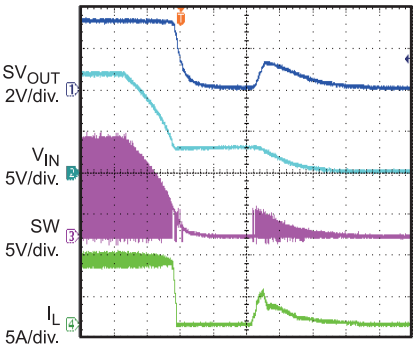
V_{IN} Start Up
V_{CC}=12V, I_{LOAD}=8A



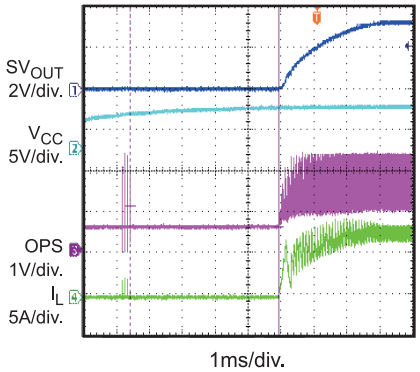
V_{IN} Shut Down
V_{CC}=5V, I_{LOAD}=8A



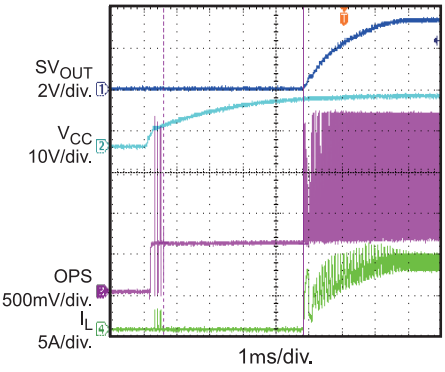
V_{IN} Shut Down
V_{CC}=12V, I_{LOAD}=8A



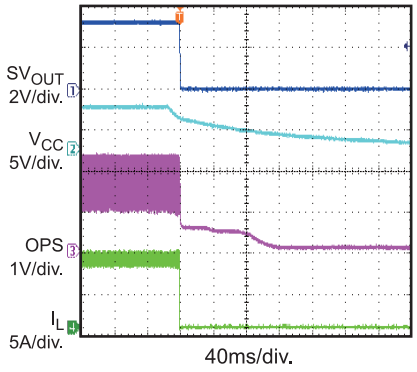
V_{CC} Start Up
V_{CC}=5V, I_{LOAD}=8A



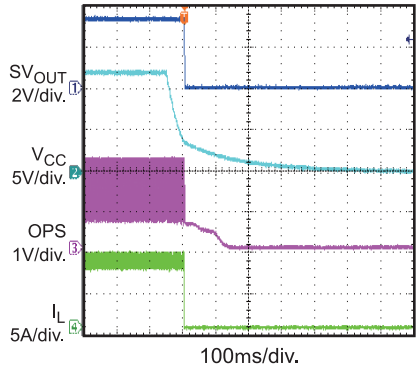
V_{CC} Start Up
V_{CC}=12V, I_{LOAD}=8A



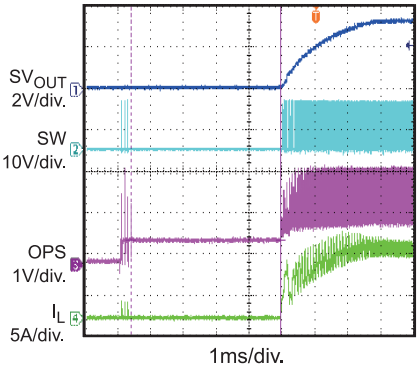
V_{CC} Shut Down
V_{CC}=5V, I_{LOAD}=8A



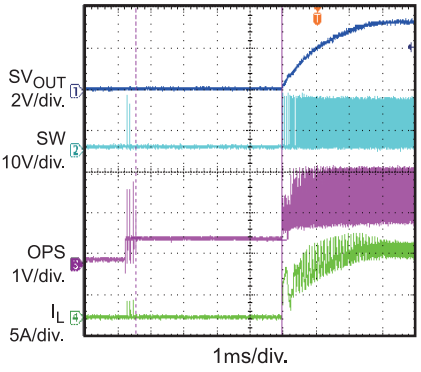
V_{CC} Shut Down
V_{CC}=12V, I_{LOAD}=8A



En Start Up
V_{CC}=5V, I_{LOAD}=8A



En Start Up
V_{CC}=12V, I_{LOAD}=8A

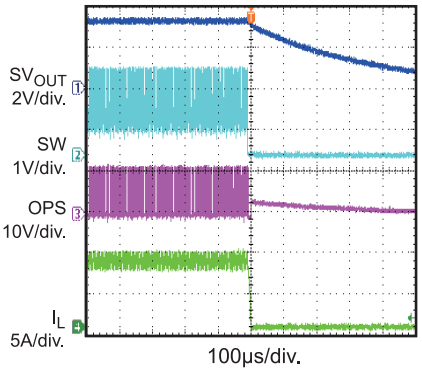


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN}=12V, SV_{OUT}=3.3V, L1=4.7µF, C_5=1000µF, LVout=1.2V, T_A=25°C, unless otherwise noted.

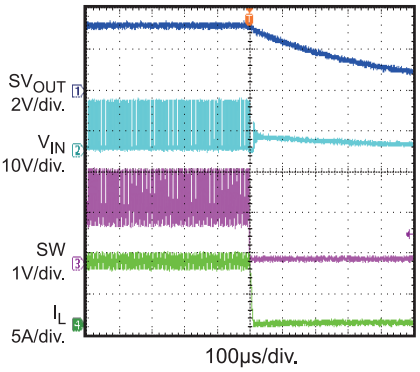
En Shut Down

V_{CC}=5V, I_{LOAD}=8A



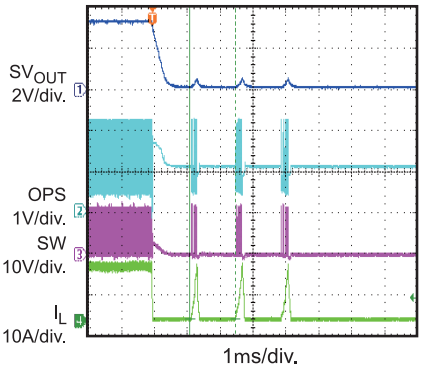
En Shut Down

V_{CC}=12V, I_{LOAD}=8A



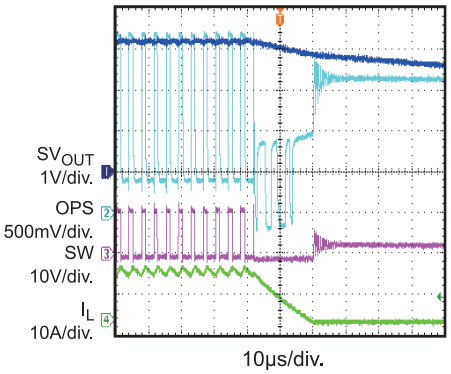
OCP

V_{CC}=12V, I_{OCSET}=12.3A,
R_{OCSET}=13.7kΩ



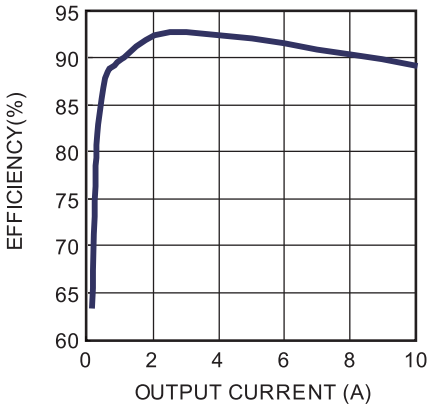
OCP

V_{CC}=12V, I_{OCSET}=12.3A,
R_{OCSET}=13.7kΩ



Efficiency

V_{CC}=5V,
MOSFET Q1&Q4: NC
Q2: AM4842, Q3: AP4224



FUNCTION BLOCK DIAGRAM

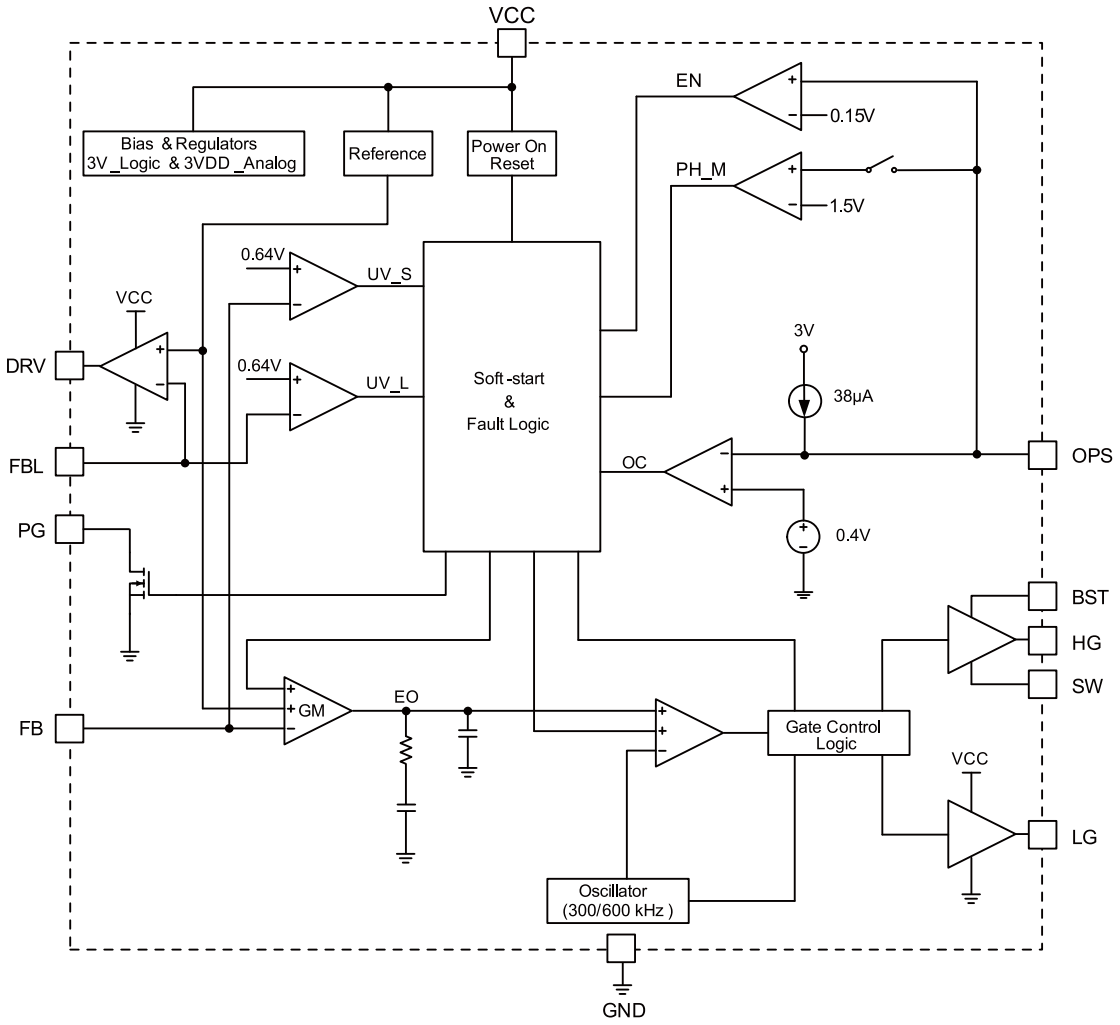
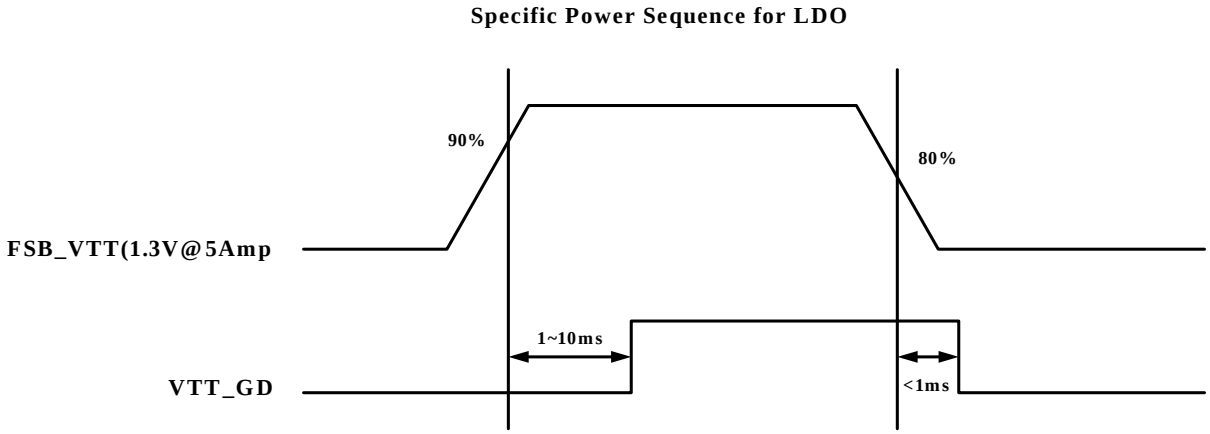


Figure 1 — Function Block Diagram

TIMING DIAGRAM



OPERATION

The MP2910 is a 5V/12V synchronous buck PWM DC/DC and linear power controller. It adopts voltage mode PWM control and includes internal soft-start, frequency-compensation networks, power good signaling with specific sequence. The part is operated at fixed 300 kHz frequency providing an optimum compromise between efficiency, external component size, and cost. The linear controller is implemented to drive an external MOSFET for regulation and it's adjustable by setting external resistors. An adjustable over-current protection (OCP) is proposed to monitor the voltage drop across the $R_{DS(ON)}$ of the lower MOSFET for synchronous buck PWM DC-DC controller.

VCC Under-Voltage Lockout (UVLO)

VCC Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP2910 UVLO's rising threshold is about 4.1V with a hysteresis of 400mV. It's not-latch protection.

Internal Soft-Start

The soft-start is employed to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. The output voltage smoothly ramps up with the SS voltage. When SS is higher than REF, REF regains control. The circuit enters into steady stage operation. The SS time's typical value is 2.5ms.

Power Good Indicator

The PG pin is the open drain of a MOSFET, it should be connected to supply power by a resistor network. When the FB voltage reaches 90% of REF voltage, the PG pin is pulled high after an about 4ms delay. When the FB voltage drops to 80% of REF voltage, the PG pin will be pulled low.

Internal Loop Compensation

MP2910 is a voltage mode buck controller with internal loop compensation using a high gain transconductance error amplifier as shown in Figure 2.

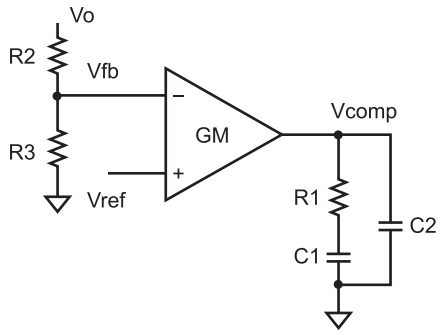


Figure 2 — Compensation Loop with Transconductance Error Amplifier

The pole and zero of the compensation network are:

$$f_P = \frac{1}{2\pi \times R_1 C_2}$$

$$f_Z = \frac{1}{2\pi \times R_1 C_1}$$

MP2910 internal compensation network parameters:

$GM=0.2mS$, $R_1=75k\Omega$, $C_1=2.5nF$, $C_2=5pF$

OPS (Over Current Setting, VIN Power on Reset and Shutdown) (Pin 13)

OCP (Over Current Setting)

MP2910 senses the low-side MOSFET's $R_{DS(ON)}$ to set the over current trip point. Connect an over current setting resistor R_{OCSET} from this pin to SW (Pin 14), then the over current trip point can be estimated according to the following equation:

$$I_{OCSET} = \frac{38\mu A \times R_{OCSET} - 0.4V}{R_{DS(ON)} \text{ of the low-side MOSFET}}$$

The over current trip point is very sensitive to external parasitic capacitance because the OPS pin function is similar to RC charging/discharging circuit.

When OCP is trigged, a hiccup restart sequence will be initialized and only 4 times of trigger are allowed to latch off (Refer to OCP waveforms as shown in Typical Performance Characteristics).

VIN_POR (VIN Power On Reset)

Before V_{IN} is ready, the HG pin will continuously generate a 10kHz clock with 1% duty cycle. V_{IN} is recognized ready by sensing the voltage of OPS pin crossing 1.5V four times (rising & falling). R_{OCSET} must be lower than 39.5kΩ, otherwise, an internal 38μA current source flowing through R_{OCSET} will keep the voltage of OPS pin always higher than 1.5V. If so, the VIN_POR function will be disabled. It is highly recommended that R_{OCSET} be lower than 30kΩ.

Shutdown

Connect a small transistor from the OPS pin to ground, then enabling the transistor can shutdown the MP2910 as shown in typical application circuit.

UVP (Under Voltage Protection)

To protect against UV, the voltage of FB and FBL pins is monitored in MP2910. The UV threshold typical value is 82.5% of the FB or FBL rated value. Once UVP_FBL is trigged, a hiccup restart sequence will be initialized and only 4 times of trigger are allowed to latch off. During soft-start interval hiccup is disabled. UVP_FB has some difference from OCP and UVP_FBL, it will always trigger V_{IN} Power sensing even after 4 times hiccup. So the controller will restart when the voltage of FB pin recovers.

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is set by using a resistive voltage divider from the output voltage to FB pin. First, choose a value for the feedback resistor R6, e.g. 10kΩ, and then R5 is determined as follows:

$$R_5 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_6$$

Selecting the Inductor

An inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications. A larger value inductor will result in less ripple current and lower output ripple voltage. However, the larger value inductor has a larger physical size, higher series resistance, and/or lower saturation current. Generally, choose the inductor ripple current approximately 30% of the maximum load current, then the inductance value can be calculated by:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S}$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the 300KHz switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

where I_{LOAD} is the load current.

Input Capacitor Selection

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The selection of input capacitor is mainly based on its maximum ripple current capability. The RMS value of ripple current flowing through the input capacitor is described as:

$$I_{RMS} = I_{LOAD} \sqrt{\frac{V_{OUT}}{V_{IN}} (1 - \frac{V_{OUT}}{V_{IN}})}$$

The worst-case condition occurs at $V_{IN}=2V_{OUT}$, where $I_{RMS}=I_{LOAD}/2$. So, the input capacitor you selected must be capable of handling this ripple current.

Output Capacitor Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stability. The output capacitor impedance should be low at the switching frequency. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right)$$

where C_O is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

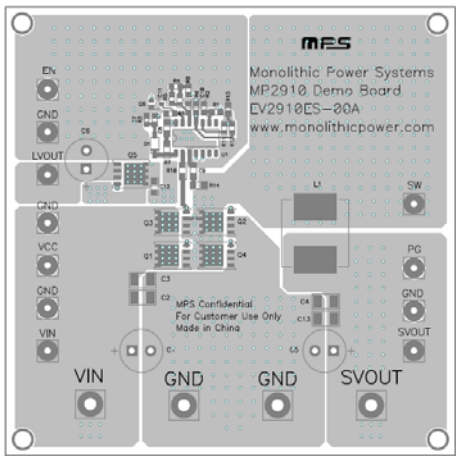
For tantalum or electrolytic capacitor application, the ESR dominates the impedance at the switching frequency. So the above formula can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

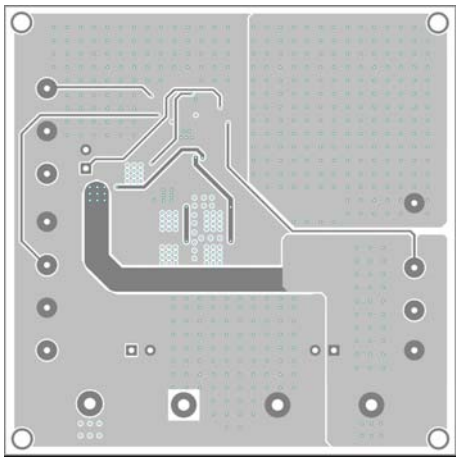
PCB Layout Guide

PCB layout is very important to achieve stable operation. A multi-layer PCB is highly recommended. The high current paths (GND, V_{IN} and SW) should be placed very close to the device with short, direct and wide traces. A RC low pass filter is recommended for V_{CC} supply. The V_{CC} decoupling capacitor must be placed as close to V_{CC} pin and GND pin as possible. The external feedback resistors should be placed next to the FB and FBL pins.

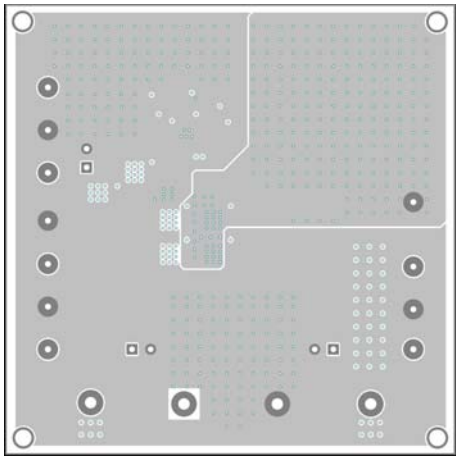
Below PCB layout files are our test board for your reference:



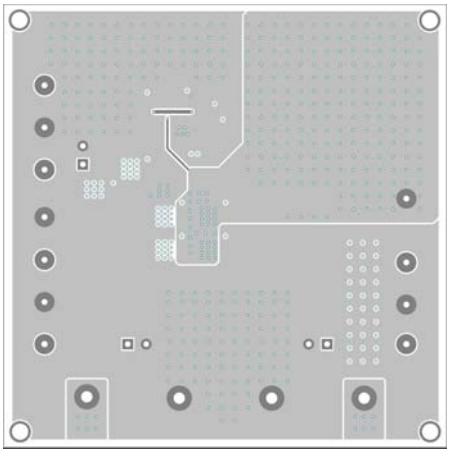
Top and Top Silk Layers



Inner Layer 2



Inner Layer 1

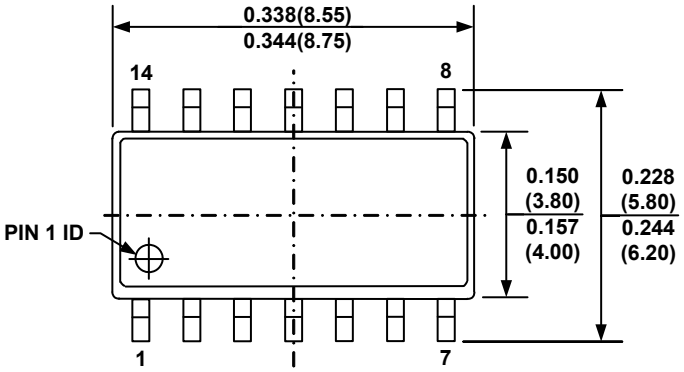


Bottom Layer

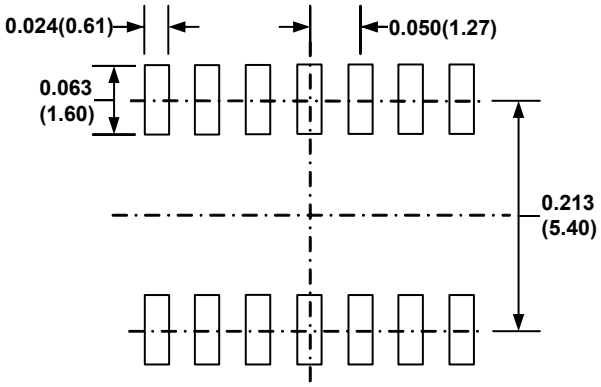
Figure 3 — MP2910DS PCB Layout

PACKAGE INFORMATION

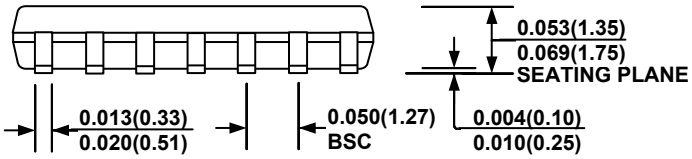
SOIC14



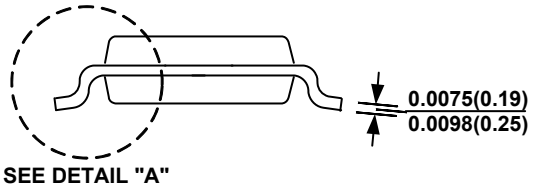
TOP VIEW



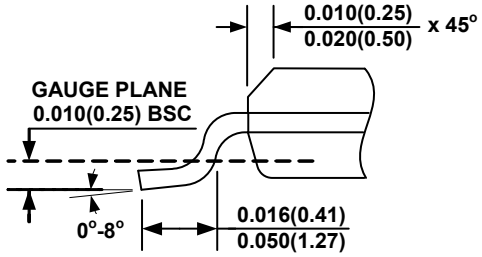
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

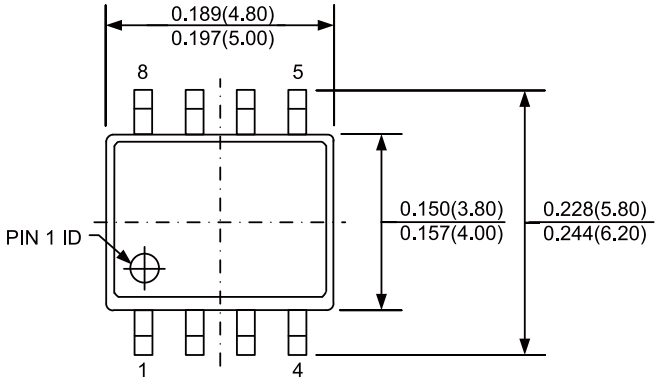


DETAIL "A"

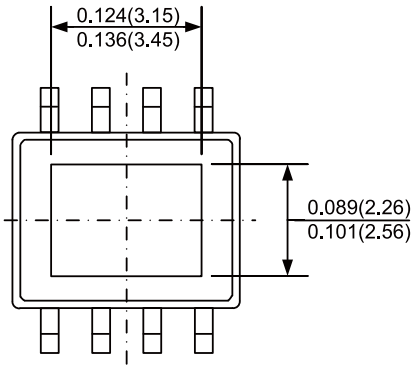
NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AB.
6) DRAWING IS NOT TO SCALE.

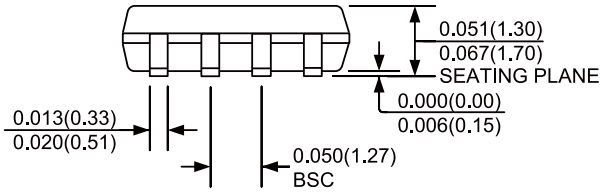
SOIC8E (EXPOSED PAD)



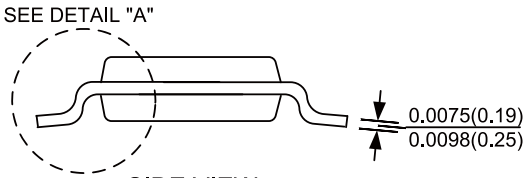
TOP VIEW



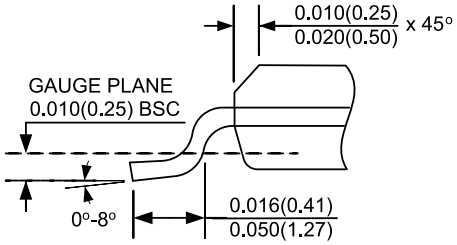
BOTTOM VIEW



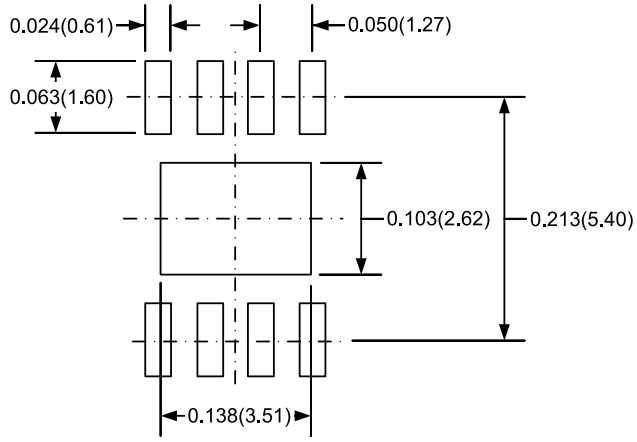
FRONT VIEW



SIDE VIEW



DETAIL "A"



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