MP2965

Dual-Loop, Digital, Multi-Phase Controller with PMBus Interface for VR13.HC/AVSBUS

The Future of Analog IC Technology

DESCRIPTION

The MP2965 is a dual-loop, digital, multi-phase controller that provides power for the core of the Intel VR13.HC platform and AVSBus control CPU. The MP2965 can work with MPS's Intelli-Phase products to complete the multi-phase voltage regulator (VR) solution with minimal external components. The MP2965 can be configured with up to 7-phase operation for Rail 1 and up to 3-phase operation for Rail 2.

The MP2965 provides an on-chip EEPROM to store and restore device configurations. Device configurations and fault parameters can be easily programmed or monitored via the PMBus/I²C interface. The MP2965 can monitor and report output current through the CS output from the Intelli-Phase products.

The MP2965 is based on a unique, digital, multi-phase, non-linear control to provide a fast transient response to the load transient with minimal output capacitors. With only one power loop control method for both steady state and the load transient, the power loop compensation is very easy to configure.

FEATURES

- Multi-Phase, Dual Output, Digital Controller
- Intel VR13.HC/IMVP9 Compliant
- PMBus/I²C and AVSBUS Compliant
- Switching Frequency up to 3MHz
- Pin Programmable for PMBus or Boot-Up Voltage
- Built-In EEPROM to Store Custom Configurations
- Automatic Loop Compensation
- Fewer External Components than a Conventional Analog Controller
- Overshoot Reduction with Non-Linear Control
- Flexible Phase Assignment for Dual Rails
- Auto Phase-Shedding to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing with Programmable Offsets for Thermal Balance
- Digital Load-Line Regulation
- Detection for Intelli-Phase MOSFET Fault Type and Auto-Record to EEPROM
- Supports 3-Bit PVID Mode
- Supports Over-Clocking Mode
- Line-Floating Detection
- Input and Output Voltage, Current, and Power Monitoring
- Regulator Temperature Monitoring
- UVLO, OVP, UVP, OCP, and OTP with No Action, Latch, Retry, or Hiccup Options
- Supports PMBus Write or Read Protection with Password or Pin Set
- Available in an RoHS-Compliant QFN-48 (6mmx6mm) Package

APPLICATIONS

- Server Core Voltage
- Graphic Card Core Regulators
- Telecom and Networking Systems
- Base Stations

TYPICAL APPLICATION

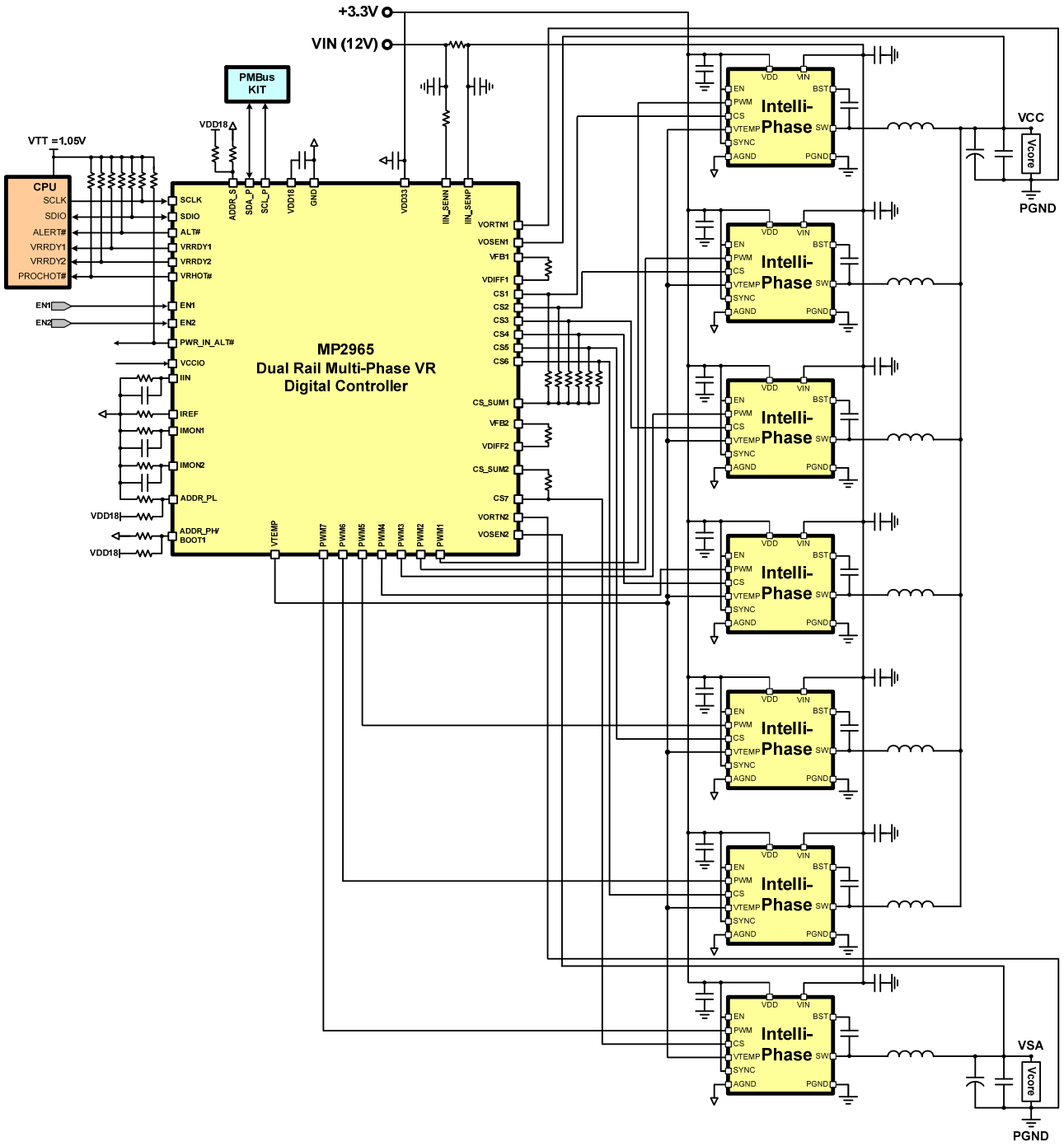


Figure 1: Intel SVID 6+1 Application

TYPICAL APPLICATION *(continued)*

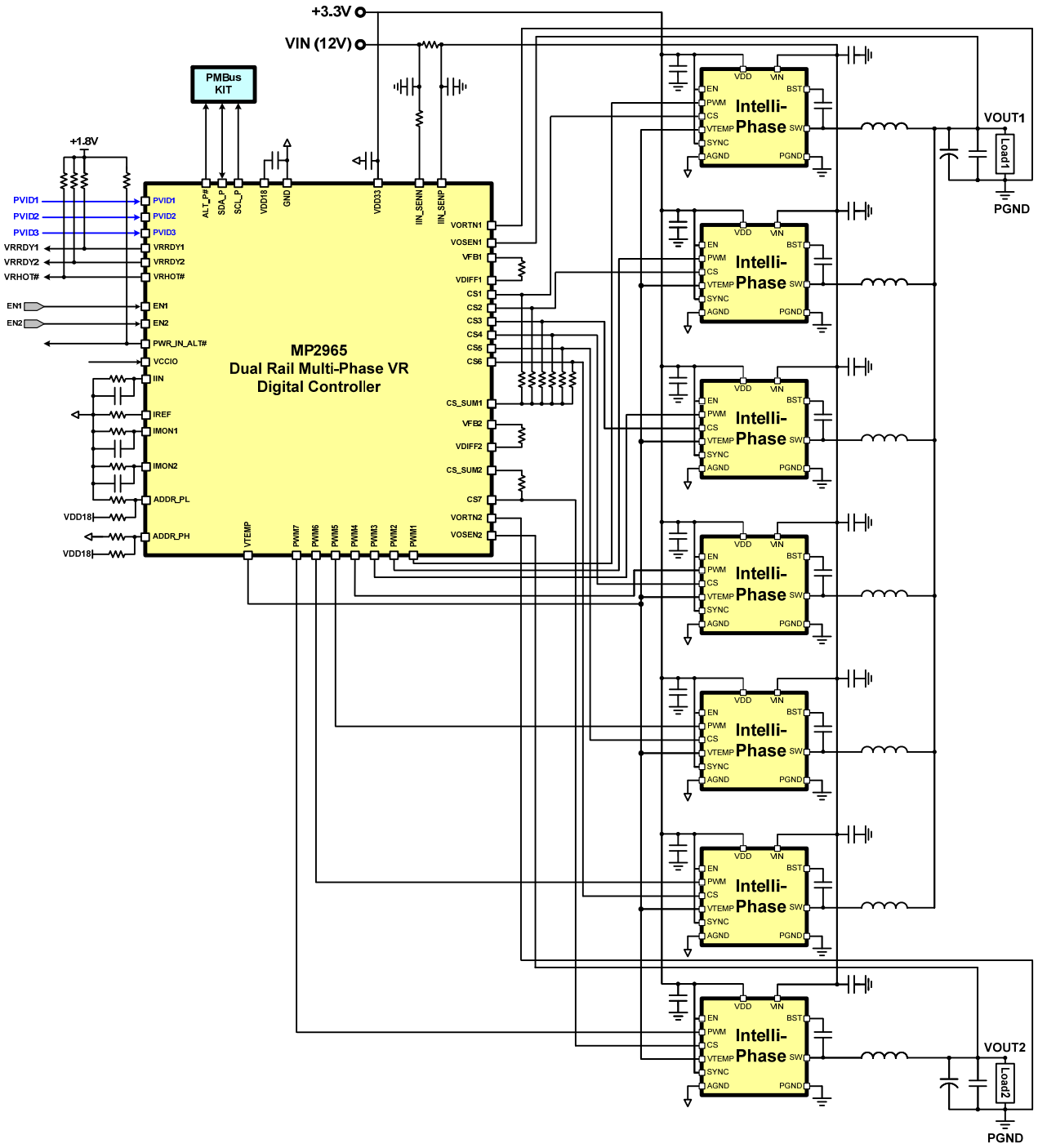


Figure 2: PVID 6+1 Application

TYPICAL APPLICATION *(continued)*

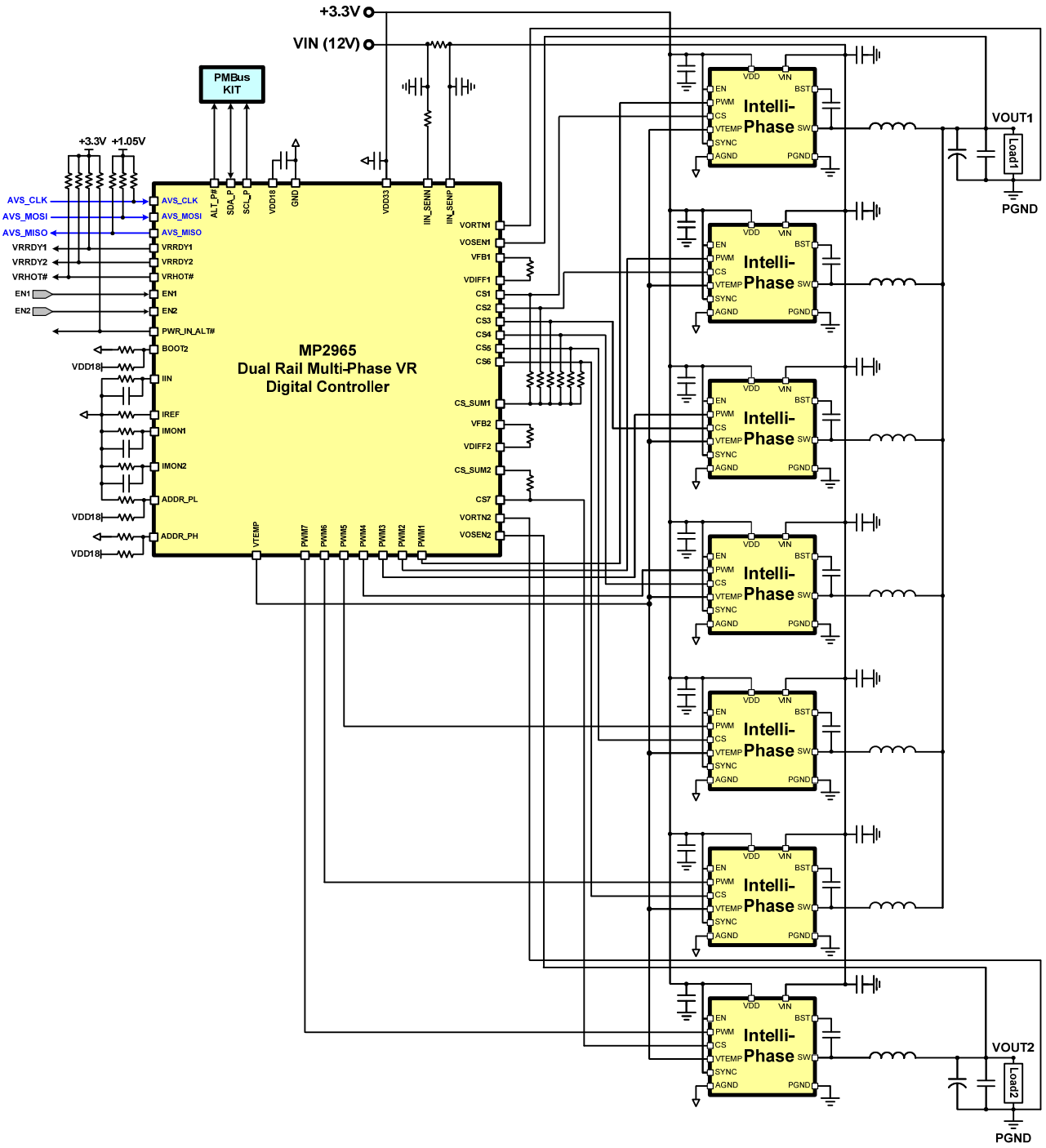


Figure 3: AVSBus 6+1 Application

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2965GQK-xxxx**	QFN-48 (6mmx6mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g.: MP2965GQK-xxxx-Z)
** "xxxx" is the configuration code identifier for the register settings stored in the EEPROM. Each "x" can have a hexadecimal value between 0 and F. Please contact an MPS FAE to create this unique number.

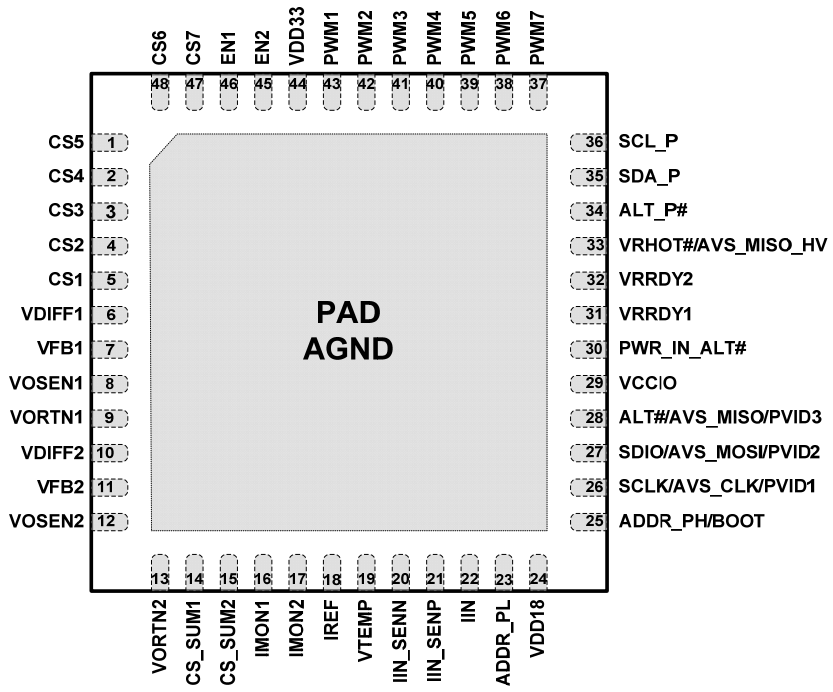
TOP MARKING

MPSYYWW
MP2965
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2965: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-48 (6mmx6mm)

ABSOLUTE MAXIMUM RATINGS (1)

VDD33 ..... -0.3V to +4V
VDD18 ..... -0.3V to +2.2V
VORTN1/2 ..... -0.3V to +0.3V
IIN_SENN, IIN_SENP ..... -0.3V to +15V
CS1 to CS7, PWM1 to PWM7, VFB1/2, VDIFF1/2, VOSEN1/2, VRRDY1/2, VRHOT#, SCL_P, SDA_P, ALT_P#, EN1/2, PWR_IN_ALT# ..... -0.3V to +4V
All other pins ..... -0.3V to +2.2V
Continuous power dissipation (T_A = +25°C) (2) 3.4W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

VDD33 ..... +3.0V to +3.6V
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-48 (6mmx6mm)	30	3	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 6-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD33 = 3.3V, EN1/2 = 1V, current going into pin is positive, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Remote Sense Amplifier						
Bandwidth (5)	$GBW_{(RSA)}$			20		MHz
VORTN1/2 current	$I_{VORTN1,2}$	EN = 1V, $V_{VOSEN1/2}$ = 3V, $V_{VORTN1/2}$ = 0V	-200	-40		µA
VOSEN1/2 current	$I_{VOSEN1,2}$	EN = 1V, $V_{VOSEN1/2}$ = 3V, $V_{ORTN1/2}$ = 0V		90	200	µA
Oscillator						
Frequency	f_{OSC}	V_{IREF} = 1.23V, R_{IREF} = 61.9kΩ		1.56		MHz
System Interface Control Inputs						
EN1, EN2						
Input low voltage	$VIL_{(EN)}$				0.4	V
Input high voltage	$VIH_{(EN)}$		0.8			V
Enable high leakage	$IIH_{(EN)}$	EN = 3.3V		3	8	µA
Thermal Throttling Control						
VRHOT# low output impedance		$I_{VRHOT\#}$ = 20mA,		8	13	Ω
VRHOT# high leakage current		V_{VRHOT} = 1.8V	-3		3	µA
IMON1, IMON2 Output						
Current gain	I_{MON}/I_{CS_SUM}	Measured from I_{CS_SUM} to I_{IMON}, I_{CS_SUM} = 2mA		1:16		A/A
Current gain accuracy		I_{CS_SUM} = 2mA, T_A=25°C	-1		1	%
IIN Sense (5)						
Digital I_{IN} error		V_{IN} = 12V, I_{IN_SENN} = 0.1mA	-1		1	%
I_{IN} amplifier input offset		V_{IN} = 12V	-0.2		0.2	mV
PWM Comparator (Rail 1/2) (5)						
Propagation delay	t_{PD}			10		ns
Common mode range			0		2.1	V
VFB- Window Comparator (Rail 1/2, VFB & VREF - 25mV) (5)						
Propagation delay	t_{PD}			10		ns
Common mode range			0		2.1	V
VFB+ Window Comparator (Rail 1/2, VFB & VREF + 20mV) (5)						
Propagation delay	t_{PD}			10		ns
Common mode range			0		2.1	V

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN1/2 = 1V, current going into pin is positive, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Protection Comparators (Rail 1/2, UVP, OVP, RVP)						
Under-voltage threshold	V_{DIFF} (UV)	Relative to reference DAC voltage, VDIFF unit gain, OV/UV_VTH_SEL = 1		−140		mV
		Relative to reference DAC voltage, VDIFF unit gain, OV/UV_VTH_SEL = 2		−220		mV
		Relative to reference DAC voltage, VDIFF gain = 1, OV/UV_VTH_SEL = 4		−300		mV
Over-voltage threshold	V_{DIFF} (OV2)	Relative to reference DAC voltage, VDIFF unit gain, OV/UV_VTH_SEL = 1		140		mV
		Relative to reference DAC voltage, VDIFF unit gain, OV/UV_VTH_SEL = 2		220		mV
		Relative to reference DAC voltage, VDIFF unit gain, OV/UV_VTH_SEL = 4		300		mV
	V_{DIFF} (OV1)	Relative to OVP1 DAC voltage, VOUT_MAX + VOUT_OFFSET = 2.3V, The maximum OVP1 voltage is 2.3V.		400		mV
Reverse-voltage detection threshold (5)	V_{VOSEN} (RV)	Relative to VORTN		300		mV
VDD33 Supply						
Supply current	I_{VDD33}	EN1/2 = high. 6+1-phase configuration.		30		mA
		EN1/2 = 0V, low-power mode		150		µA
UVLO threshold voltage	$VDD33_{UVLO}$	VDD33 is rising		2.86	2.98	V
		VDD33 is falling	2.68	2.82		
UVLO hysteresis	$VDD33_{HYS}$			40		mV
1.8V Regulator						
1.8V regulator output voltage	VDD18	I_{VDD18} = 0mA		1.8		V
1.8V regulator load capability	I_{VDD18}	VOL = VDD18 - 40mV		30		mA
PWM Outputs						
Output low voltage	$V_{OL\ (PWM)}$	$I_{PWM(SINK)}$ = 400µA		10	200	mV
Output middle voltage	$V_{OM\ (PWM)}$	$I_{PWM(SOURCE)}$ = -100µA	1.2	1.35	1.5	V
Output high voltage	$V_{OH\ (PWM)}$	$I_{PWM(SOURCE)}$ = -400µA	3.1	VDD33 - 0.02		V
Rise and fall time (5)		C = 10pF		10		ns
PWM tri-state leakage		PWM = 1.5V, EN = 0V	-1		1	µA

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN1/2 = 1V, current going into pin is positive, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SVID/AVSBUS Interface						
CPU interface voltage (SDIO, SCLK) (AVS_MOSI, AVS_CLK)	V_{IL}	Logic low			0.45	V
	V_{IH}	Logic high	0.65			V
	V_{HYS}	Hysteresis		50		mV
Leakage current (SDIO, SCLK, ALT#), (AVS_MOSI, AVS_CLK, AVS_MISO)	IL	0V to VTT	-10		10	µA
Pad capacitance (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO) (5)	C_{PAD}				4	pF
Pin capacitance (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO) (5)	C_{PIN}				5	pF
Buffer on resistance (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO) (5)	R_{ON}			7	12	Ω
Maximum voltage (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO) (5)	V_{MAX}	Transient voltage including ringing	-0.3		2.1	V
Slew rate (SDIO, SCLK, ALT#) (AVS_MOSI, AVS_CLK, AVS_MISO) (5)		2nH, 4pF load	0.5		2	V/ns
VR clock-to-data delay (5)			4		8.3	ns
Set-up time(5)				7		ns
Hold time (5)				14		ns
VID-DAC (Reference Voltage for Rail 1/2)						
Range	$FS_{DAC\ VID}$	5mV VID step mode, remote sense amplifier unit gain		1.36		V
		5mV VID step mode, remote sense amplifier unit gain		2.72		V
Resolution/LSB (5)	$\Delta_{DAC\ VID}$	5mV VID step mode		5		mV
		10mV VID step mode		10		mV
Output voltage slew rate (5)				100		mV/µs
ADC						
ADC Voltage Reference		TA=25℃	1.584	1.6	1.616	V
ADC resolution (5)				10		bits

ELECTRICAL CHARACTERISTICS *(continued)*

VDD33 = 3.3V, EN1/2 = 1V, current going into pin is positive, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
DNL (5)					1	LSB
Sample rate (5)				780		kHz
VOUT DC Calibration DAC (V_{OUT} DC Calibration for Rail 1/2) (5)						
Range	FS_{DAC_VO}			350		mV
Resolution/LSB	Δ_{DAC_VO}			8		bit
OCP_Phase DAC (OCP_Phase Protection for Rail 1/2)						
Range	FS_{DAC_OC-PH}		0.17		2.72	V
Resolution/LSB (5)	Δ_{DAC_OC-PH}			10		mV
Power Management Features						
V_{IN} UVLO turn-on threshold	$V_{IN\ ON}$	VIN_ON (35h) = 0xE850, adjustable via PMBus		10		V
V_{IN} UVLO turn-off threshold	$V_{IN\ OFF}$	VIN_ON (35h) = 0xE848, adjustable via PMBus		9		V
PMBus DC Characteristics (ALT_P, SDA_P, SCL_P)						
Input high voltage	V_{IH}	SCL_P, SDA_P	1.35			V
Input low voltage	V_{IL}	SCL_P, SDA_P			0.8	V
Input leakage current		SCL_P, SDA_P, ALT_P	-10		10	µA
Output low voltage (5)	V_{OL}	ALT_P sinks 2mA			400	mV
Maximum voltage (5)	V_{MAX}	Transient voltage including ringing	-0.3	3.3	3.6	V
Pin capacitance (5)	C_{PIN}				10	pF
PMBus Timing Characteristics (5) (6)						
Operating frequency range			10		1000	kHz
Bus free time		Between stop and start condition	0.5			µs
Holding time			0.26			µs
Repeated start condition set-up time			0.26			µs
Stop condition set-up time			0.26			µs
Data hold time			0			ns
Data set-up time			50			ns
Clock low time out			25		35	ms
Clock low period			0.5			µs
Clock high period			0.26		50	µs
Clock/data fall time					120	ns
Clock/data rise time					120	ns

NOTES:

5) Guaranteed by design or characterization data, not tested in production.

6) The device supports 100kHz, 400kHz, and 1MHz bus speeds. The PMBus timing parameters in this table is for operation at 1MHz. If the PMBus operating frequency is 100kHz and 400kHz, refer to the SMBus specification for timing parameters.

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	CS5	A[I]	**Phase1~5 current sense input.** Connected any unused CS pins to CS_SUM1 or CS_SUM2.
2	CS4	A[I]	
3	CS3	A[I]	
4	CS2	A[I]	
5	CS1	A[I]	
6	VDIFF1	A[O]	**Differential remote sense amplifier output of Rail 1.**
7	VFB1	A[I/O]	**Feedback of Rail 1.** VFB1 sources a current proportional to the sensed output current (I_{DROOP1}). This current flows through the resistor (R_{DROOP1}) between VFB1 and VDIFF1 to create a voltage drop proportional to the load current. Select a resistor between VDIFF1 and VFB1 to set a proper load line.
8	VOSEN1	A[I]	**Positive remote voltage sense input of Rail 1.** VOSEN1 is connected directly to the VR output voltage at the load and should be routed differentially with VORTN1.
9	VORTN1	A[I]	**Remote voltage sensing return input of Rail 1.** VORTN1 is connected directly to ground at the load and should be routed differentially with VOSEN1.
10	VDIFF2	A[O]	**Differential remote sense amplifier output of Rail 2.**
11	VFB2	A[I/O]	**Feedback of Rail 2.** VFB2 sources a current proportional to the sensed output current (I_{DROOP2}). This current flows through the resistor (R_{DROOP2}) between VFB2 and VDIFF2 to create a voltage drop proportional to the load current. Select the resistor between VDIFF2 and VFB2 to set a proper load line.
12	VOSEN2	A[I]	**Positive remote voltage sense input of Rail 2.** VOSEN2 is connected directly to the VR output voltage at the load and should be routed differentially with VORTN2.
13	VORTN2	A[I]	**Remote voltage sensing return input of Rail 2.** VORTN2 is connected directly to ground at the load and should be routed differentially with VOSEN2.
14	CS_SUM1	A[I]	**Total phase current sensing input of Rail 1.** CS_SUM1 is used for the load-line and over-current protections of Rail 1. Connect the active-phase CS signals of Rail 1 together to CS_SUM1 through the current sense resistors.
15	CS_SUM2	A[I]	**Total phase current sensing input of Rail 2.** CS_SUM2 is used for the load-line and over-current protections of rail2. Connect the active-phase CS signals of Rail 2 together to CS_SUM2 through the current sense resistors.
16	IMON1	A[I/O]	**Analog total average current sensing signal of Rail 1.** IMON1 sources a current proportional to the sensed total average current from CS_SUM1. IMON1 is used for load current reporting of Rail 1. Connect a resistor from IMON1 to AGND to convert the current into voltage.
17	IMON2	A[I/O]	**Analog total average current sensing signal of Rail 2.** IMON2 sources a current proportional to the sensed total average current from CS_SUM2. IMON2 is used for the load current reporting of Rail 2. Connect a resistor from IMON2 to AGND to convert the current into voltage.
18	IREF	A [I/O]	**Internal bias current set.** Connect a 61.9kΩ, 1% accuracy resistor to AGND.
19	VTEMP	A [I]	**Analog temperature report signal from the VR to the controller.** VTEMP indicates the maximum temperature of the power stage. The MP2965 supports temperature sensing from the Intelli-Phase. All VTEMP pins of the power stage tie together to produce the maximum voltage value of the VTEMP bus.

PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
20	IIN_SENN	A[I]	**Negative input of the remote input current sense amplifier.** Connect a voltage to the current converting resistor ($R_{I/V}$) from the positive node of the input current sensing resistor to IIN_SENN.
21	IIN_SENP	A[I]	**Positive input of the remote input current sense amplifier.** Connect IIN_SENP to the negative node of the input current sensing resistor.
22	IIN	A [I/O]	**Analog total input current signal.** IIN sources a current proportional to the sensed system input current from IIN_SENP and IIN_SENN. Connect a resistor from IIN to AGND to convert the current into voltage.
23	ADDR_PL	A[I]	**PMBus address 4-LSB setting.**
24	VDD18	Power	**1.8V LDO output.** VDD18 provides a power supply for the internal digital circuit. Connect a 1μF bypass capacitor to AGND.
25	ADDR_PH	A[I]	**PMBus address 3-MSB setting.**
	BOOT		**Boot-up voltage-setting pin.**
26	SCLK	D[I]	**Clock from CPU (SVID interface) to MP2965.** SCLK is an open-drain signal. Connect SCLK to an external pull-up resistor. Connect SCLK to GND if unused.
	AVS_CLK		**Clock from CPU (AVSBUS interface) to MP2965.**
	PVID1		**PVID control bit 1.**
27	SDIO	D[I/O]	**Data line between CPU (SVID interface) and MP2965.** SDIO is an open-drain signal. Connect SDIO to an external pull-up resistor. Connect SDIO to GND if unused.
	AVS_MOSI		**Data line from CPU (AVSBUS interface) to MP2965.**
	PVID2		**PVID control bit 2.**
28	ALT#	D[I/O]	**Alert# line from the MP2965 to CPU (SVID interface).** ALT# is an open-drain signal. Connect ALT# to an external pull-up resistor. Connect ALT# to GND if unused.
	AVS_MISO		**Data line from MP2965 to CPU (AVSBUS interface with ≤1.8V bus voltage).**
	PVID3		**PVID control bit 3.**
29	VCCIO	A[I]	**VCCIO input pin.** If VCCIO falls below 0.65V ± 50mV, both rails enter protection mode.
30	PWR_IN_ ALT#	D[O]	**Open-drain VR input power exceeding Pin_Max indicator.** Connect PWR_IN_ALT# to the processor to notify the CPU to reduce the power.
31	VRRDY1	D[O]	**Open-drain VR ready indicator of Rail 1.** VRRDY1 stays low until the soft-start is finished and the output voltage is in the valid zone.
32	VRRDY2	D[O]	**Open-drain VR ready indicator of Rail 2.** VRRDY2 stays low until the soft-start is finished and the output voltage is in the valid zone.
33	VRHOT#	D[O]	**Open-drain VR thermal monitor output.** VRHOT# pulls low if the temperature exceeds the programmed VRHOT# temperature threshold.
	AVS_MISO _HV		**Data line from the MP2965 to CPU (AVSBus interface with 1.8V~3.3V bus voltage).**

PIN FUNCTIONS *(continued)*

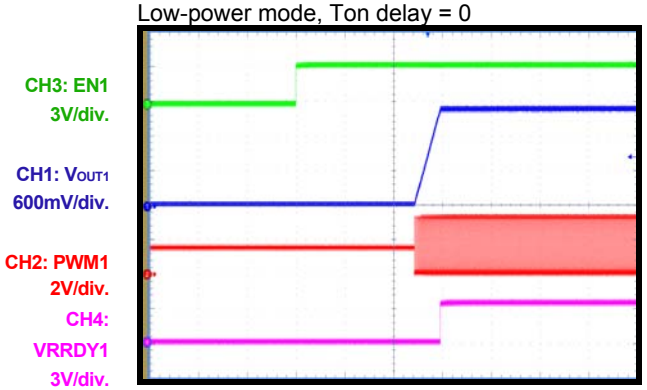
Pin #	Name	I/O	Description
34	ALT_P#	D[O]	**PMBus open-drain VR warning indictor.**
35	SDA_P	D[I/O]	**PMBus data signal.**
36	SCL_P	D[I]	**PMBus clock signal.**
37	PWM7	D[O]	**Tri-state logic-level PWM outputs.** Each output is connected to the PWM input of the Intelli-Phase. The logic level is 0V for low, 3.3V for high, and Hi-Z or 1.5V for mid-state. Float these pins if they are not being used.
38	PWM6	D[O]	
39	PWM5	D[O]	
40	PWM4	D[O]	
41	PWM3	D[O]	
42	PWM2	D[O]	
43	PWM1	D[O]	
44	VDD33	Power	**3.3V power supply input.** Connect a 1μF bypass capacitor to AGND.
45	EN2	D[I]	**Enable control for the Rail 2.**
46	EN1	D[I]	**Enable control for the Rail 1.**
47	CS7	A[I]	**Phase6~7 current sense input.** Connected any unused CS pins to CS_SUM1 or CS_SUM2.
48	CS6	A[I]	
PAD	AGND	Power	**Analog ground.**

TYPICAL PERFORMANCE CHARACTERISTICS

Rail 1: 6-phase, V_{IN} = 12V, V_{OUT1} = 1.82V, F_{SW1} = 800kHz, L_1 = 100nH, C_{OUT1} = 44*47µF + 59*22µF.
Rail 2: 1-phase, V_{IN} = 12V, V_{OUT2} = 0.95V, F_{SW2} = 800kHz, L_2 = 180nH, C_{OUT2} = 3*47µF + 5*22µF + 1*470µF.
T_A = +25°C, unless otherwise noted.

Rail 1 Enable On

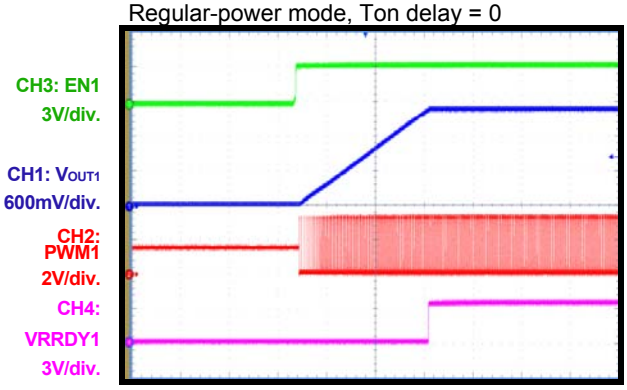
V_{IN} = 12V, V_{OUT1} = 1.7V
Low-power mode, Ton delay = 0



500µs/div.

Rail 1 Enable On

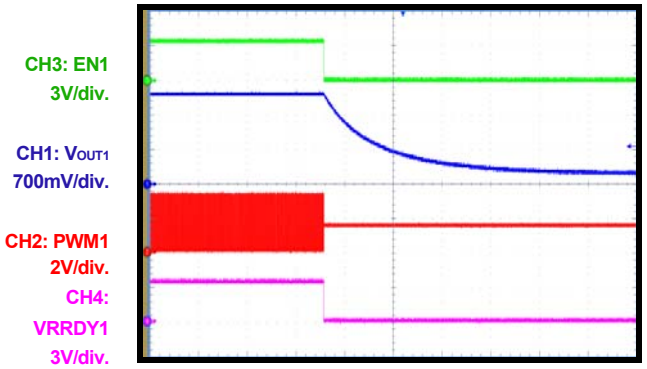
V_{IN} = 12V, V_{OUT1} = 1.7V
Regular-power mode, Ton delay = 0



100µs/div.

Rail 1 Enable Off

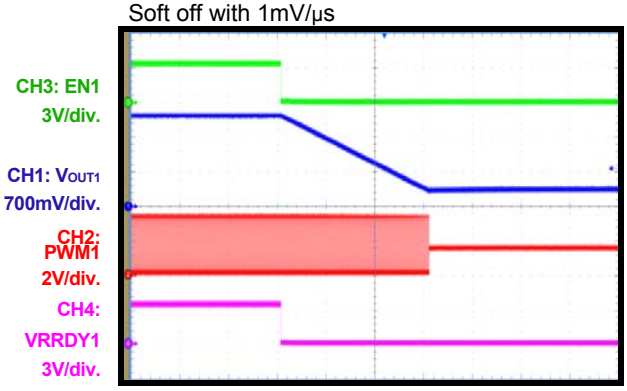
V_{IN} = 12V, V_{OUT1} = 1.82V
Hi-Z off



500ms/div.

Rail 1 Enable Off

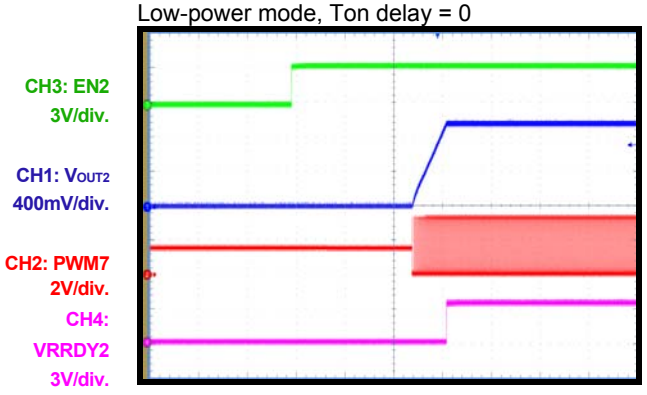
V_{IN} = 12V, V_{OUT1} = 1.82V
Soft off with 1mV/µs



500µs/div.

Rail 2 Enable On

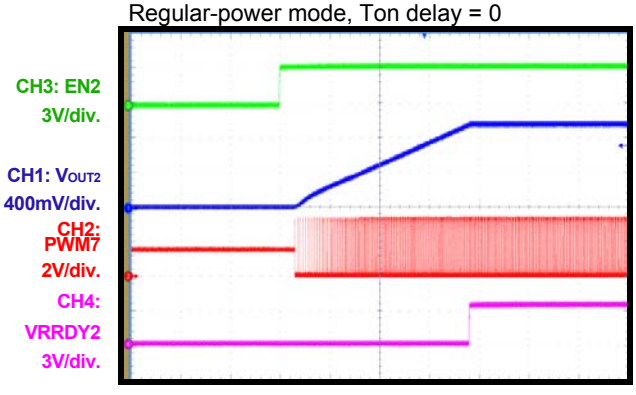
V_{IN} = 12V, V_{OUT2} = 0.95V
Low-power mode, Ton delay = 0



500µs/div.

Rail 2 Enable On

V_{IN} = 12V, V_{OUT2} = 0.95V
Regular-power mode, Ton delay = 0



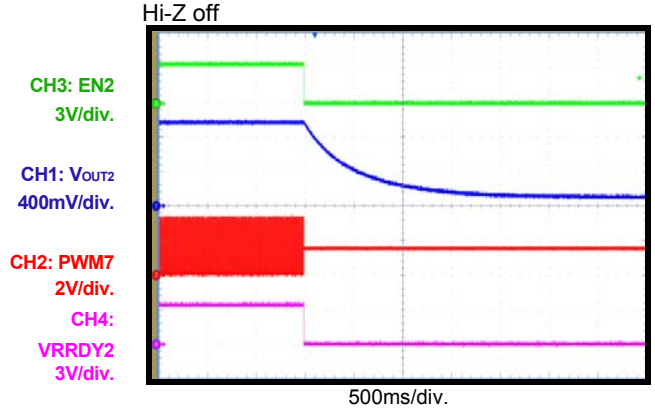
100µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Rail 1: 6-phase, V_{IN} = 12V, V_{OUT1} = 1.82V, F_{SW1} = 800kHz, L_1 = 100nH, C_{OUT1} = 44*47µF + 59*22µF.
Rail 2: 1-phase, V_{IN} = 12V, V_{OUT2} = 0.95V, F_{SW2} = 800kHz, L_2 = 180nH, C_{OUT2} = 3*47µF + 5*22µF + 1*470µF.
T_A = +25°C, unless otherwise noted.

Rail 2 Enable Off

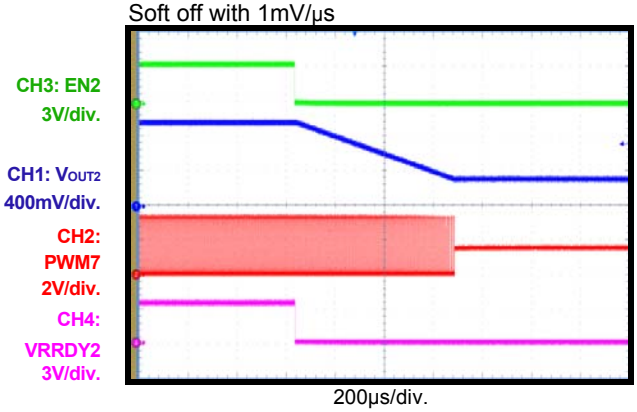
V_{IN} = 12V, V_{OUT2} = 0.95V
Hi-Z off



500ms/div.

Rail 2 Enable Off

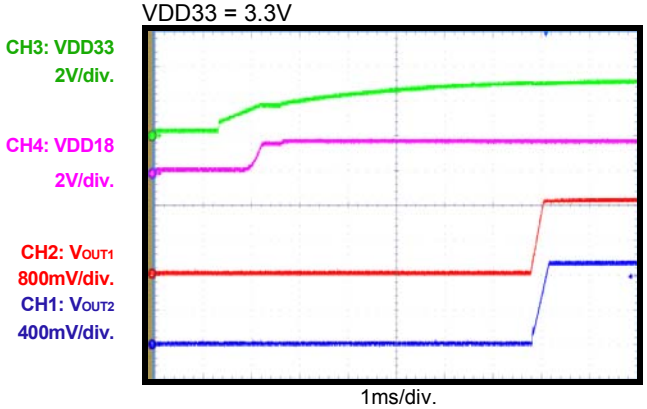
V_{IN} = 12V, V_{OUT2} = 0.95V
Soft off with 1mV/µs



200µs/div.

VDD33 On

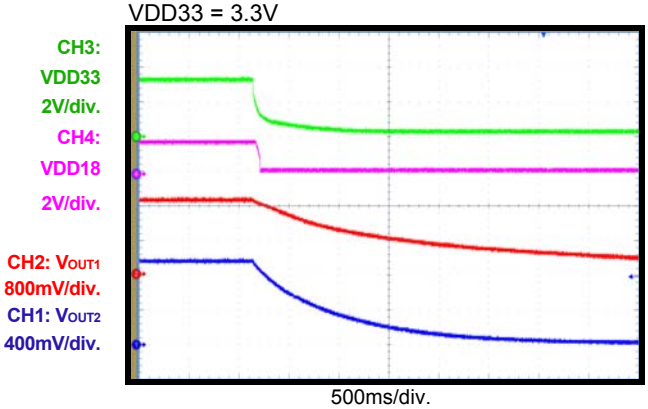
V_{IN} = 12V, V_{OUT1} = 1.7V, V_{OUT2} = 0.95V,
VDD33 = 3.3V



1ms/div.

VDD33 Off

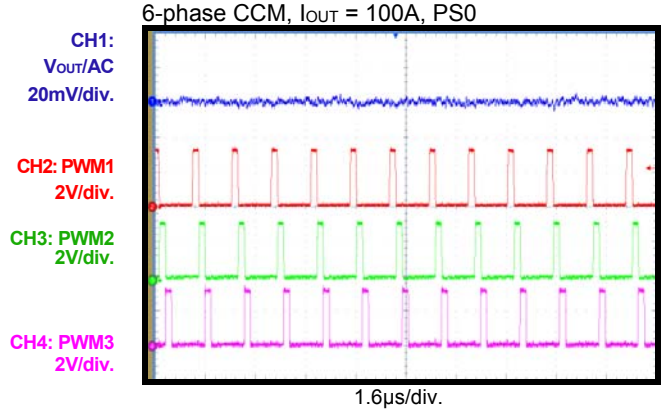
V_{IN} = 12V, V_{OUT1} = 1.7V, V_{OUT2} = 0.95V,
VDD33 = 3.3V



500ms/div.

Steady State

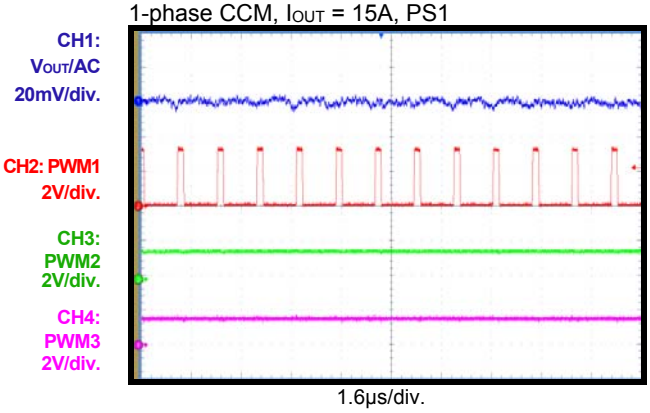
V_{IN} = 12V, V_{OUT1} = 1.82V,
6-phase CCM, I_{OUT} = 100A, PS0



1.6µs/div.

Steady State

V_{IN} = 12V, V_{OUT1} = 1.82V
1-phase CCM, I_{OUT} = 15A, PS1



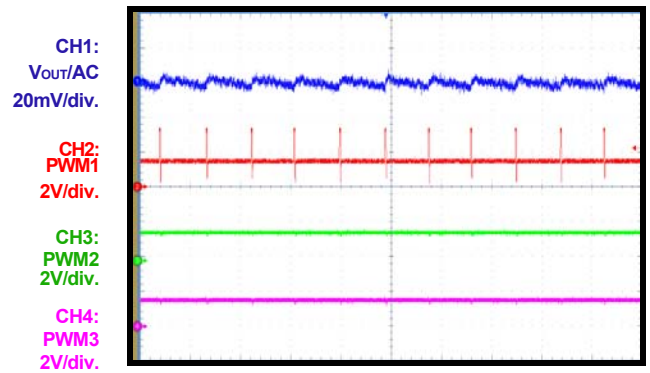
1.6µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Rail 1: 6-phase, V_{IN} = 12V, V_{OUT1} = 1.82V, F_{SW1} = 800kHz, L_1 = 100nH, C_{OUT1} = 44*47µF + 59*22µF.
Rail 2: 1-phase, V_{IN} = 12V, V_{OUT2} = 0.95V, F_{SW2} = 800kHz, L_2 = 180nH, C_{OUT2} = 3*47µF + 5*22µF + 1*470µF.
T_A = +25°C, unless otherwise noted.

Steady State

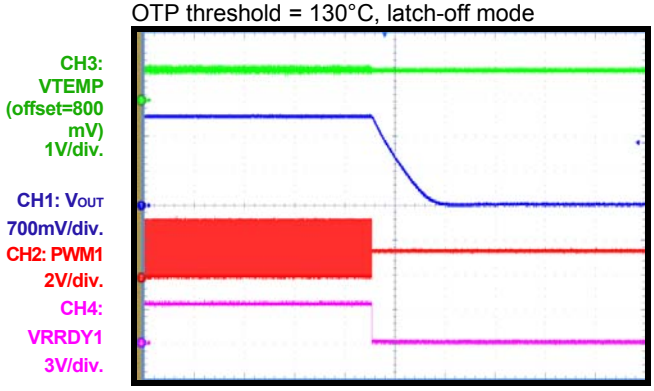
V_{IN} = 12V, V_{OUT1} = 1.82V
1-phase CCM, I_{OUT} = 1A, PS2



8µs/div.

OTP

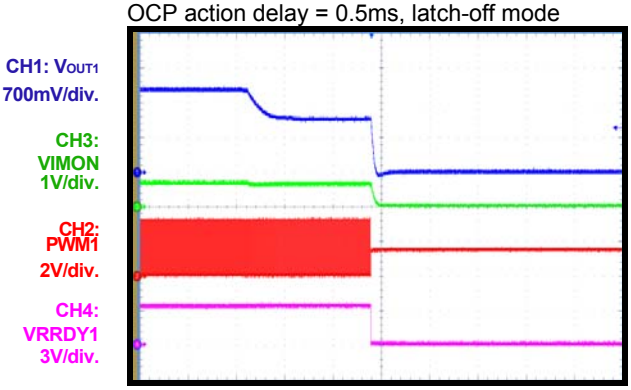
V_{IN} = 12V, V_{OUT1} = 1.82V, T_J =
(125°C/V)*VTEMP-75°C
OTP threshold = 130°C, latch-off mode



200µs/div.

OCP

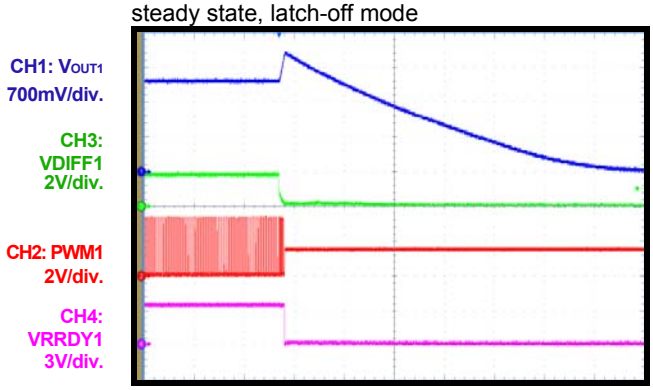
V_{IN} = 12V, V_{OUT1} = 1.82V, OCP-Total = 240A,
OCP action delay = 0.5ms, latch-off mode



200µs/div.

VDIFF SCP

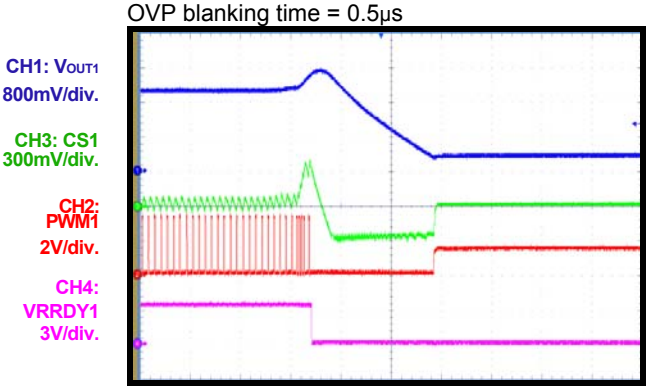
V_{IN} = 12V, V_{OUT1} = 1.82V, short VDIFF to GND at steady state, latch-off mode



50µs/div.

OVP

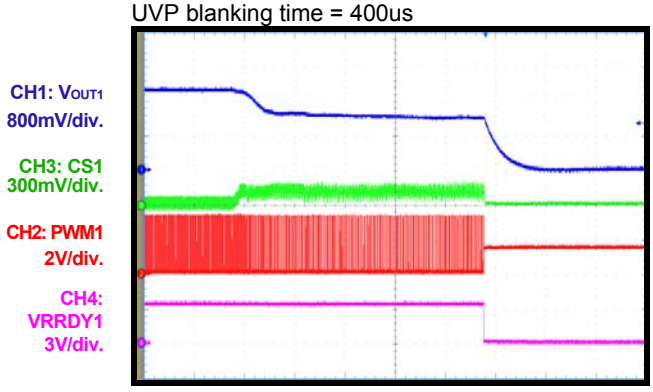
V_{IN} = 12V, V_{OUT1} = 1.82V, F_{SW} = 800kHz
OVP blanking time = 0.5µs



10µs/div.

UVP

V_{IN} = 12V, V_{OUT1} = 1.82V, F_{SW} = 800kHz
UVP blanking time = 400us



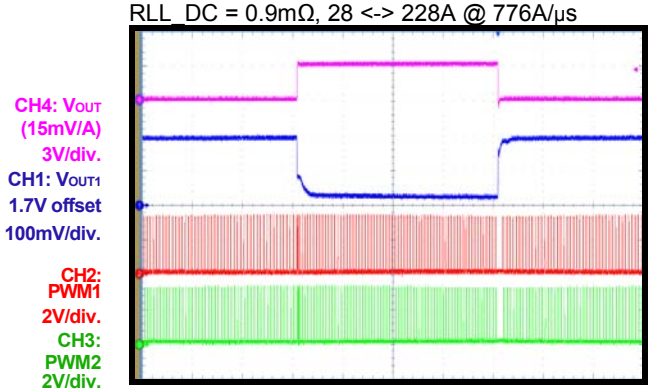
100µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Rail 1: 6-phase, V_{IN} = 12V, V_{OUT1} = 1.82V, F_{SW1} = 800kHz, L_1 = 100nH, C_{OUT1} = 44*47µF + 59*22µF.
Rail 2: 1-phase, V_{IN} = 12V, V_{OUT2} = 0.95V, F_{SW2} = 800kHz, L_2 = 180nH, C_{OUT2} = 3*47µF + 5*22µF + 1*470µF.
T_A = +25°C, unless otherwise noted.

Load Transient with DC Load Line

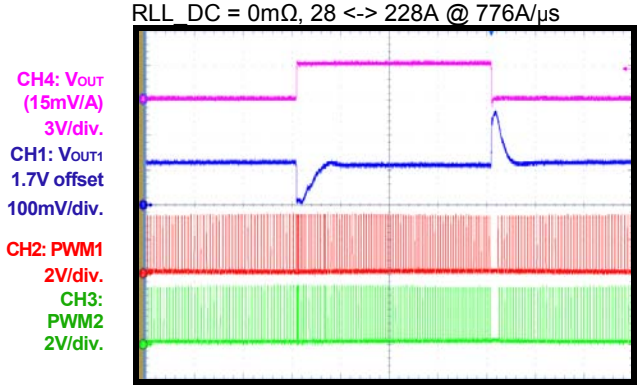
V_{IN} = 12V, V_{OUT1} = 1.82V
RLL_DC = 0.9mΩ, 28 <-> 228A @ 776A/µs



20µs/div.

Load Transient with AC Load Line

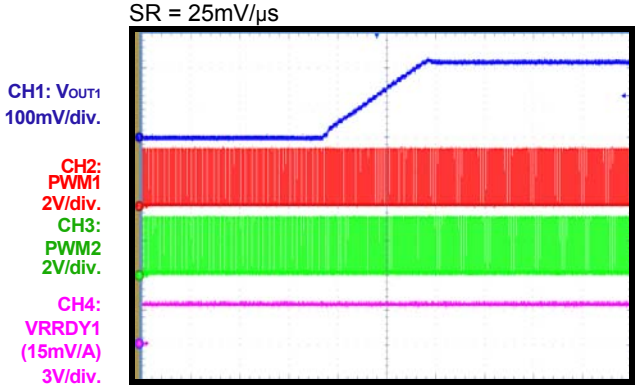
V_{IN} = 12V, V_{OUT1} = 1.82V
RLL_DC = 0mΩ, 28 <-> 228A @ 776A/µs



20µs/div.

DVID Up

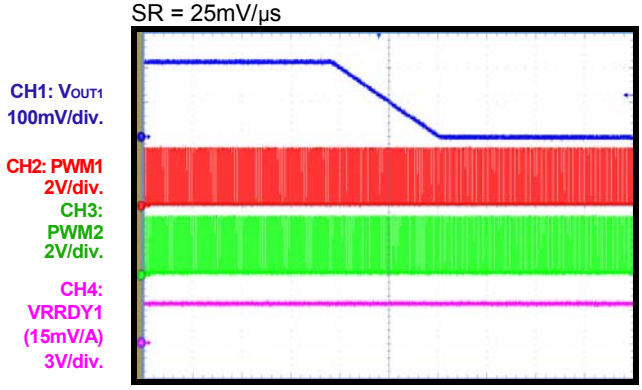
DVID from 1.6V to 1.82V
SR = 25mV/µs



100µs/div.

DVID Down

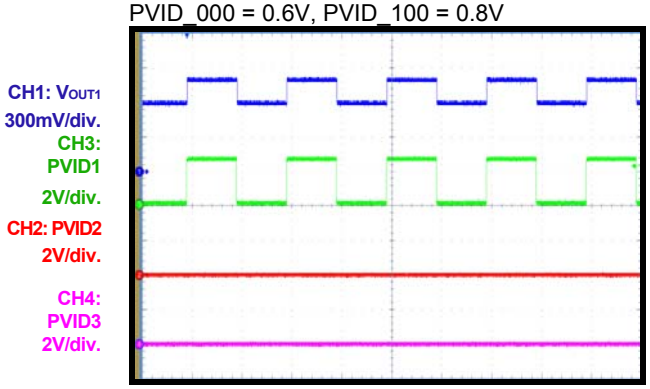
DVID from 1.82V to 1.6V
SR = 25mV/µs



100µs/div.

PVID Transition

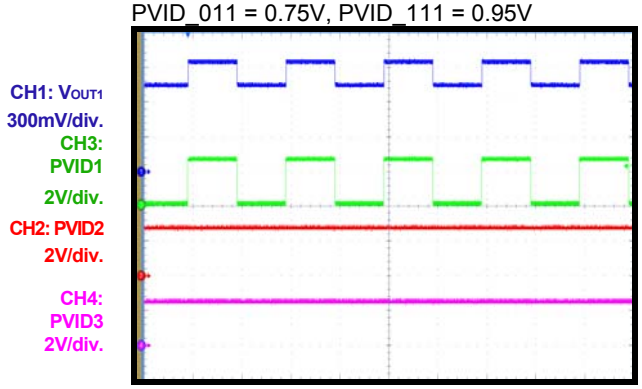
V_{IN} = 12V, PVID0 = 0 <-> 1, PVID2 = PVID3 = 0
PVID_000 = 0.6V, PVID_100 = 0.8V



5ms/div.

PVID Transition

V_{IN} = 12V, PVID0 = 0 <->1, PVID2 = PVID3 = 1
PVID_011 = 0.75V, PVID_111 = 0.95V



5ms/div.

BLOCK DIAGRAM

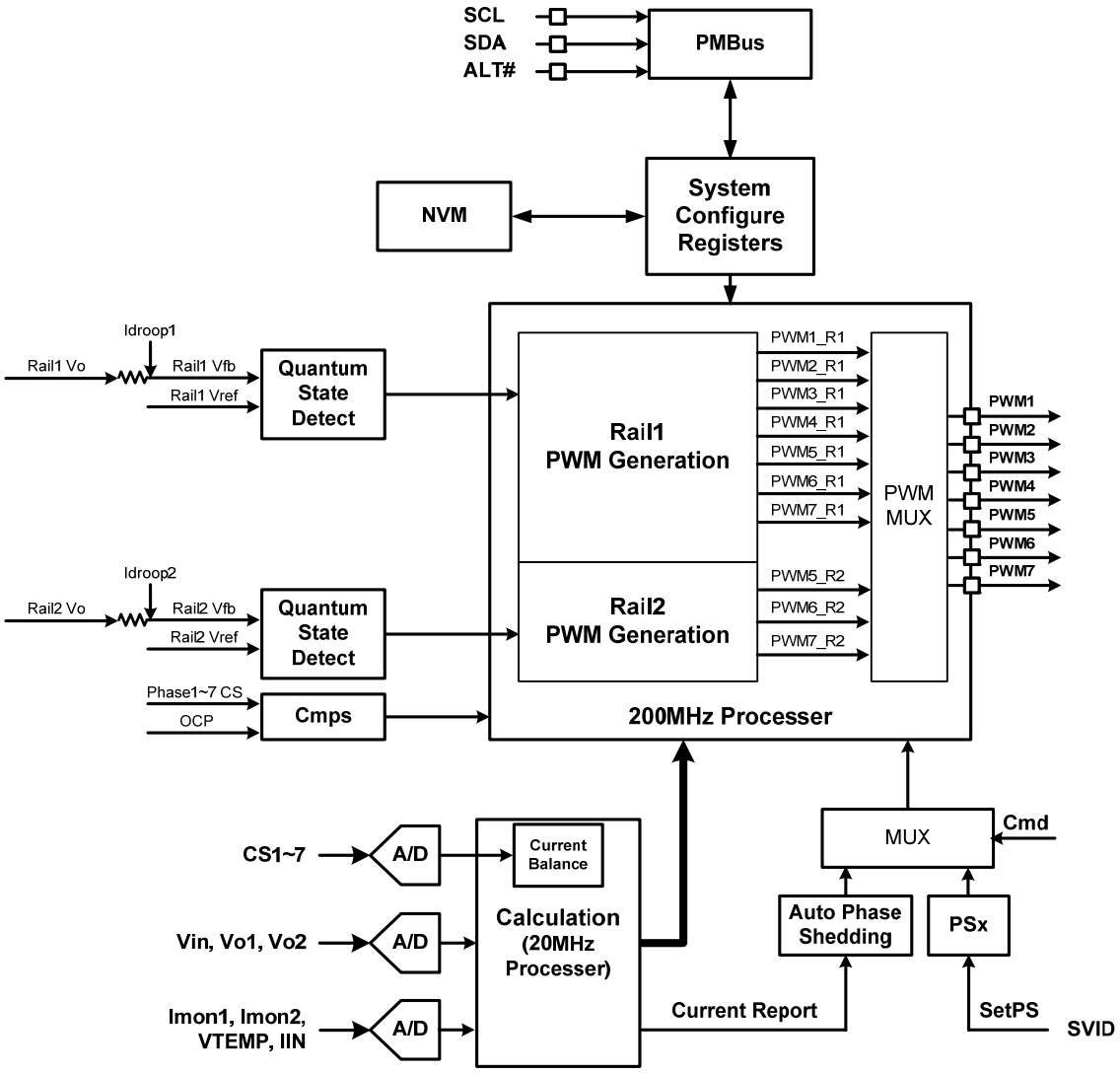


Figure 4: System Functional Block Diagram

OPERATION

The MP2965 is a dual-output, digital, multi-phase voltage regulator (VR) controller for Intel VR13, AVSBus communication, and PVID applications.

The MP2965 adopts MPS's unique loop compensation strategy to balance and optimize the steady and transient performances. The MP2965 also adopts adaptive phase-shedding and phase-adding strategies to optimize the overall VR efficiency according to the load current.

The MP2965 contains a high-precision digital-to-analog converter (DAC) and analog-to-digital converter (ADC), differential remote voltage sense amplifier, fast comparators, current sense amplifiers, internal slope compensation, digital load-line setting, power good monitor, and temperature monitor.

The MP2965 provides rich programmable functions with PMBus 1.3 interface. On-chip EEPROM can store custom configurations flexibly and auto-records the fault type when a protection occurs.

Fault protection features include V_{IN} under-voltage lockout (UVLO), V_{IN} over-voltage protection (OVP), V_{OUT} over-voltage protection (OVP), V_{OUT} under-voltage protection (UVP), V_{OUT} reverse-voltage protection (RVP), output over-current protection (OCP), and over-temperature protection (OTP).

PMBus-programmable functions include phase assignment, switching frequency, reference voltage, loop stability parameters, protection thresholds and behaviors, load-line parameters and so on.

The MP2965 can also detect the fault type of the Intelli-Phase when a protection occurs. The MP2965 can record all faults into the EEPROM automatically in case the power supply shuts off after the fault occurs.

The MP2965 system state machine is shown in Figure 5.

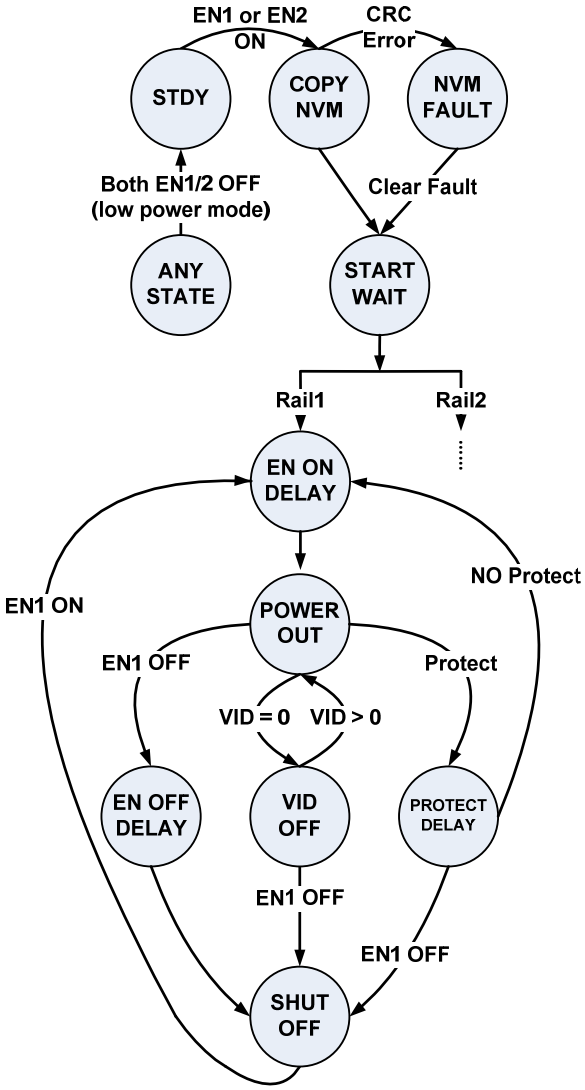


Figure 5: System State Machine

PWM Control and Switching Frequency

The MP2965 applies MPS's unique, digital, pulse-width modulation (PWM) control to provide fast load transient response and easy loop compensation. The switching frequency can be set with the PMBus command MFR_FS (ECh).

The PWM on time of each phase updates in real time according to the input voltage, output voltage, and the phase switching frequency adaptively. Calculate the on time with Equation (1):

$$T_{on} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_s} \quad (1)$$

Where V_{OUT} is the real-time output voltage (in V), V_{IN} is the input voltage (in V), and Fs is the switching frequency set by the PMBus (in Hz).

Voltage Reference

The MP2965 has an 8-bit VID-DAC, which provides the reference voltage (V_{REF}) for the individual output.

When VID = 0, V_{REF} is 0V, and the VR is in power-off state.

When VID > 0, the relationship between V_{REF} and VID in decimal format is shown in Equation (2):

$$V_{REF}(V) = \frac{(VID + OFFSET) \times VID\_STEP(mV)}{1000} \times G_{RS} \quad (2)$$

VID is the commanded voltage identification value from SVID, PMBus, AVSBus interface or PVID control (in decimal format).

OFFSET is an offset value. OFFSET = 29 when the Intel IMVP9 10mV VID table is selected by setting MFR_VBOOT_SET (E5h) bit[8] = 1. For others, OFFSET = 49.

VID_STEP is either 5mV or 10mV. This is determined by the register MFR_VR_CONFIG (E4h) bit[8].

G_{RS} is the gain of the remote sense amplifier. The value is 1 with unit gain and 0.5 with half gain, which is determined by the register VOUT_SENSE_SET (29h) bit[11].

In the MP2965, VID is a 9-bit value and can be from an SVID interface, AVSBus interface, PMBus interface or PVID control. The VID control starts with VID mode selection. Figure 6 shows the VID control-related commands.

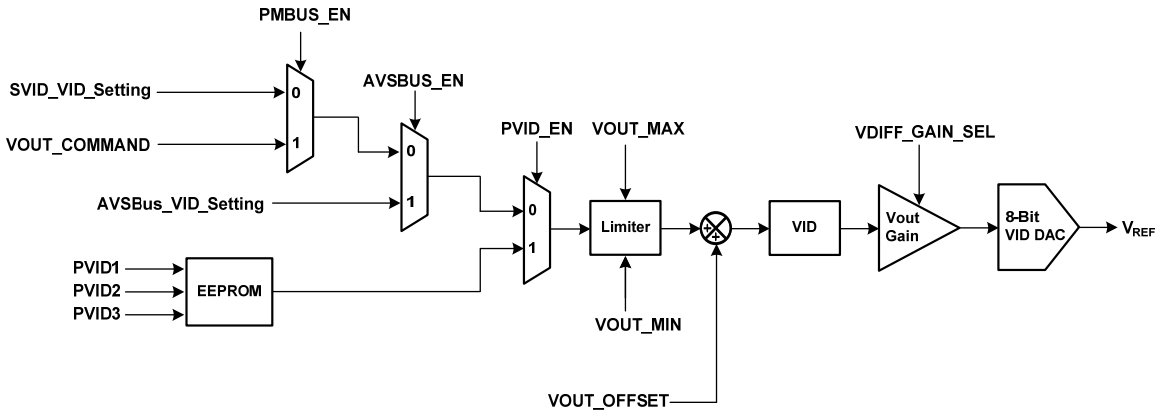


Figure 6: VID Control-Related Commands

The register listed below shows the VID mode selection bits and related registers.

- PMBUS_EN: MFR_VR_CONFIG2 (09h) bit[9]
- PVID_EN: MFR_VR_CONFIG2 (09h) bit[10]
- AVSBUS_EN: OPERATION (01h) bit[5:4]

After VID mode selection, the commanded voltage developed is compared with the output voltage limit set by the VOUT_MAX (24h) and VOUT_MIN (2Bh) commands. If the calculated voltage command creates an output voltage higher than the VOUT_MAX value or less than the VOUT_MIN value, the PMBus device limits the command voltage passed to the controller to the VOUT_MAX or VOUT_MIN value. The PMBus ALT_P# pin can be asserted as a warning to the master.

After the VID limitation, the value from the VOUT _OFFSET (23h) is added to the VID. The VOUT_OFFSET register is in two's complement format with 1-VID step/LSB. VOUT_OFFSET can range from -0.64V to +0.635V with 5mV VID table and -1.28V to +1.27V with 10mV VID table. This allows users to adjust the target VID to achieve over-clocking operation. After the VOUT_OFFSET setting, the final VID is formed. A unit gain or half-gain is used to calculate the

final input value of the 8-bit VID-DAC. The VID-DAC generates the final reference voltage, which compares with the sensed output voltage to adjust the duty cycle of the PWM.

Output Voltage Setting

In Figure 7, the voltage at the load is sensed with the differential voltage sense amplifier. This type of sensing provides better load regulation. The remote sense amplifier can be programmed with half gain with the PMBus command VOUT_SENSE_SET (29h) bit[11].

After remote sensing, the VOUT_TRIM (22h) command adds a voltage trimming value over the remote sensing output to fine-tune the output voltage. The VOUT_TRIM is 0.5mV/LSB with remote sense unit gain, and 0.8mV/LSB with remote sense half gain. This command is used to fine-tune the output voltage, which can either add or subtract an offset from the remote sensed output voltage. This can adjust the output voltage for better VOUT accuracy for the end user's system.

After the voltage trim, the MP2965 senses the voltage either on VDIFF or VFB with ADC for DC voltage calibration, thus providing high-accuracy voltage regulation. The ADC sense also provides unit gain or half gain to ensure that the voltage is within the ADC sensing range.

Table 1 shows the voltage supporting range for different VID steps and voltage sensing gains.

Table 1: Voltage Support Range

External V_{OUT} Divider	VID Table	RS Gain	VDIFF/VFB ADC Gain	V_{OUT} Range
N	5mV	1	1	0~1.25V
N	5mV	0.5	1	0~2.5V
N	10mV	1	1	0~1.6V
N	10mV	1	0.5	0~2.2V
N	10mV	0.5	1	0~3V
Y	5mV/ 10mV	1	1	>3V

For non-Intel applications with V_{OUT} > 3V, an external resistive divider is required from VOUT to VORTN and tapped to VOSEN (see Figure 7). Set the resistive dividing ratio into the MP2965 with PMBus command VOUT_SENSE_SET (29h).

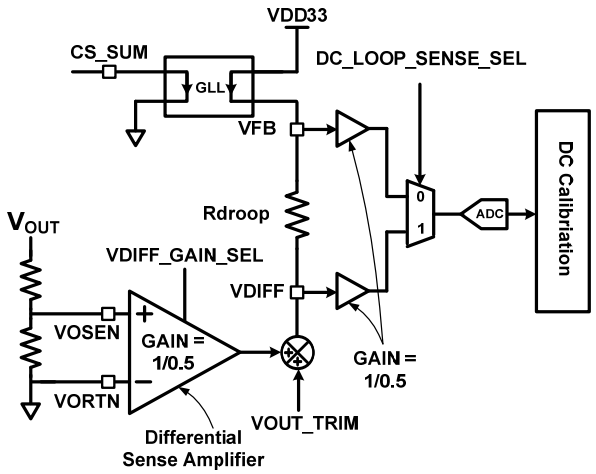


Figure 7: DC Loop Gain Selection

Active Voltage Positioning (AVP)

The MP2965 supports active voltage positioning (AVP) by connecting a droop resistor (R_{DROOP}) between VDIFF and VFB. With this function, the output voltage drops gradually as the load current increases. This is also known as load line. The relationship of the output voltage and load current is shown in Equation (3):

$$V_{OUT@IOUT} = V_{OUT@NO\ LOAD} - I_{OUT} \times R_{LL} \quad (3)$$

Where R_{LL} is the load line resistor.

The MP2965 provides a PMBus-programmable load-line range. The final load line value is determined by R_{DROOP} and the value in register MFR_IDROOP_CTRL (4Eh). The load line is calculated in Equation (4):

$$R_{LL} = \left(\frac{IDROOP\_SET + 4}{64}\right) \times K_{CS} \times R_{DROOP} \times \frac{1}{G_{RS}} \quad (4)$$

Where K_{CS} is the current sense gain of the Intelli-Phase (in A/A), IDROOP_SET is the decimal value in register IDROOP_SET (4Eh) (ranging from 0-15), R_{DROOP} is the resistor across VFB and VDIFF (in Ω), and G_{RS} is the remote sense gain. G_{RS} can be half or unit gain. When IDROOP_SET = 0, the AVP function is disabled.

For no-load line VR applications, the MP2965 provides an AC-DROOP function to increase

the phase margin of the loop regulation. The AC-DROOP function block can extract the AC part of the total inductor current, thereby letting the AC current flow through R_{DROOP}. Use a 200 ~ 500Ω R_{DROOP} resistor to achieve the AC-DROOP function. The AC-DROOP related parameters can be programmed with PMBus command MFR_SLOPE_ADV_CTRL (2Ch) bit[3]. Refer to the MFR_SLOPE_ADV_CTRL (2Ch) section on page 61 for more information.

Boot-Up Voltage Set

The MP2965 can set the boot-up voltage via the register MFR_VBOOT (E5h) or the BOOT pin.

There are eight registers (81h~88h, Page 29) in the EEPROM to set the boot-up voltage with BOOT. These VID values should be pre-programmed into the EEPROM via the PMBus. In Page 29, the PMBus can read or write the VID value via Table 2.

Figure 8 shows how BOOT sets the boot-up voltage. The MP2965 reads the boot-up VID from the EEPROM before the VR soft start.

Table 1 gives the recommended resistor value to set the boot-up voltage accordingly.

Table 2: Boot-Up Voltage Set by BOOT

BOOT Rail 1	BOOT Rail 2	Setting Voltage (V)	R_{TOP} (kΩ) 1%	R_{BOTTOM} (kΩ) 1%
81h[15:8]	81h[7:0]	0	-	0
82h[15:8]	82h[7:0]	0.057	3.32	0.11
83h[15:8]	83h[7:0]	0.116	3.32	0.226
84h[15:8]	84h[7:0]	0.205	3.32	0.43
85h[15:8]	85h[7:0]	0.340	3.32	0.768
86h[15:8]	86h[7:0]	0.540	3.32	1.43
87h[15:8]	87h[7:0]	0.844	3.32	2.94
88h[15:8]	88h[7:0]	1.301	3.32	8.66

The boot-up slew rate is the slow slew rate of the MP2965, which is proportional to the fast slew rate (see Table 3). The highest order bit with “1” sets the slow slew rate, with all lower order bits being ignored. As an example, 4’b0100 and 4’b0111 both result in a slow rate of FAST_SR/8.

Table 3: Boot-Up Slew Rate of MP2965

MFR_VID_SLEW_SLOW (0Dh) bit[3:0]	BOOT Slew Rate
4’b1xxx	FAST_SR/16
4’b01xx	FAST_SR/8
4’b001x and 4’b0000	FAST_SR/4
4’b0001	FAST_SR/2

The FAST_SR is the fast slew rate of MP2965 which is determined by the register MFR_VID_SLEW_FAST (0Eh) bit[5:0] can be calculated with Equation (5):

$$FAST\_SR = \frac{VID\_STEP(mV)}{SLEW\_FAST\_CNT \times 0.05(\mu s)} \quad (5)$$

Where VID_STEP can be set to 5mV or 10mV, and SLEW_FAST_CNT ranges from 1~63.

For example, of VID_STEP = 5mV and SLEW_FAST_CNT = 40, then set MFR_SR_SLOW_SEL to 4’b0001 to get the boot-up slew rate as 1.25mV/μs.

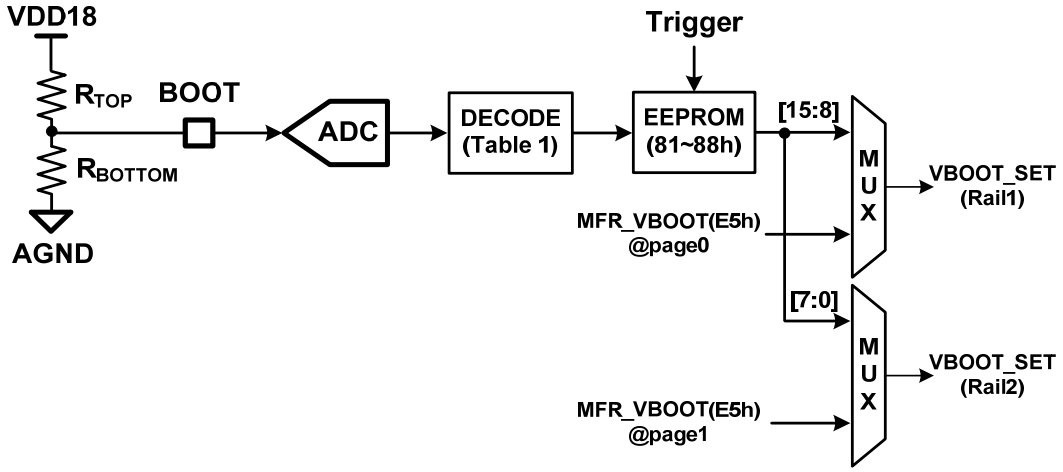


Figure 8: Boot Up Voltage Set-Up

PVID Mode

The MP2965 supports 3-bit PVID mode to control V_{OUT} by setting the PVID_EN bit in register 09h (see Figure 9).

The PVID mode pins (PVID1, PVID2, and PVID3) are multiplexed (muxed) from SCLK, SDIO, and ALT#. In PVID mode, SVID and AVSBus communication are disabled. Figure 9 shows the diagram of the PVID control process.

When any of the PVID pins are toggled, the corresponding VID value is read from the EEPROM as the new target VID.

There are eight types of PVID voltages with eight different combinations of H/L of PVID1, PVID2, and PVID3 (see Table 4). These PVID voltage values should be pre-programmed into the EEPROM via the PMBus.

The PVID voltage is also read from the register 81~88h in EEPROM Page 29. The PVID voltage can be executed by toggling the PVID pins.

Table 4: Set PVID Voltage by PVID Pins

PVID Rail 1	PVID Rail 2	PVID1 (Pin 26)	PVID2 (Pin 27)	PVID3 (Pin 28)
81h[15:8]	81h[7:0]	L	L	L
82h[15:8]	82h[7:0]	L	L	H
83h[15:8]	83h[7:0]	L	H	L
84h[15:8]	84h[7:0]	L	H	H
85h[15:8]	85h[7:0]	H	L	L
86h[15:8]	86h[7:0]	H	L	H
87h[15:8]	87h[7:0]	H	H	L
88h[15:8]	88h[7:0]	H	H	H

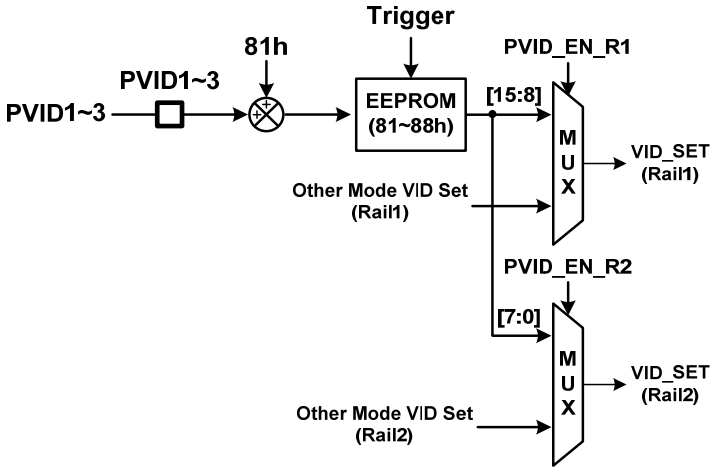


Figure 9: PVID Voltage Set-Up

Dynamic Voltage Identification (DVID)

The MP2965 supports a dynamic output voltage transition by changing the VID code with the PMBus interface, AVSBus interface, SVID interface, or PVID pins toggling.

The DVID process is active after V_{OUT} is settled. The V_{OUT} change can be either upwards- or downwards-stepping.

At the PMBus-VID control mode and PVID control mode, the DVID slew rate is set with the register VOUT_TRANSITION_RATE (27h) shown in Equation (6):

$$DVID\_SR = \frac{VID\_STEP(mV)}{VOUT\_TRANS\_CNT \times 0.1(\mu s)} \quad (6)$$

Where VID_STEP is either 5mV or 10mV, VOUT_TRANS_CNT is the decimal value in VOUT_TRANSITION_RATE (27h) bit[8:0], which ranges from 1 ~ 511.

In SVID control mode, the DVID slew rate is determined by the SetVID command. The slew rate of the SetVID_Fast command is shown in Equation (5). The slew rate of SetVID_Slow command is shown in Table 3. The slew rate of SetVID_Decay command is determined by the C_{OUT} value and the load current. The PMBus VOUT_OFFSET (23h) command is used to achieve the over-clocking function in SVID control mode. Dynamic voltage transition caused by VOUT_OFFSET (23h) follows the slow slew rate.

At the AVSBUS VID control mode, the DVID slew rate is determined by the V_{OUT} transition rate write command, which is an integer with 1LSB = 1mV/μs. In one V_{OUT} transition rate command, the rise slew rate is sent first, followed by the fall slew rate. The initial rise and fall slew rate is determined by the register VOUT_TRANSITION_RATE (27h), as shown in Equation (7):

$$AVS\_SR\_INI = \frac{100(mV/\mu s)}{VOUT\_TRANS\_CNT} \quad (7)$$

Where VOUT_TRANS_CNT is the decimal value in VOUT_TRANSITION_RATE (27h) bit[8:0], which ranges from 1 ~ 511.

During a VID transient, the MP2965 forces the VR into full-phase continuous conduction mode (CCM), regardless of the power state setting. For example, if the controller is configured for 6-phase mode but is running in 1-phase DCM due to auto-phase shedding, a VID transition command leads the controller to enter 6-phase CCM immediately.

Inductor Current Sensing and Reporting

The MP2965 works with MPS Intelli-Phase to initiate inductor current sensing (see Figure 10). The cycle-by-cycle sensed inductor current is used for multi-phase current balancing, thermal balancing, and per-phase current limitation.

The resistor (R_{CS}) is connected from CS to CS_SUM. CS_SUM is a 1.23V constant voltage which can sink/source current and provide a voltage shift to meet the operating voltage range of the Intelli-Phase CS pin.

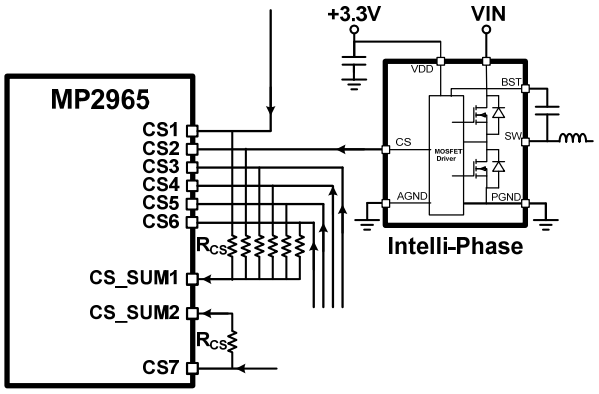


Figure 10: Phase Current Sense

Different types of Intelli-Phase products have different operating voltage ranges for CS (V_{CS_MIN} and V_{CS_MAX}). Refer to each Intelli-Phase datasheet to determine the minimum and maximum operating voltage ranges. Design a proper R_{CS} value with Equation (8):

$$V_{CS\_MIN} < I_{LOAD} \times K_{CS} \times R_{CS} + 1.23V < V_{CS\_MAX} \quad (8)$$

By working with the Intelli-Phase, the MP2965 does not need to use temperature compensation and impendence matching as traditional DCR sensing to achieve an accurate current sense.

Connect the Rail 1 CS signals to CS_SUM1 with CS resistors. Connect Rail 2 CS signals to CS_SUM2 with CS resistors. For any unused

CS pins, short them to either CS_SUM1 or CS_SUM2.

Total Current Sense

The total current is summed into CS_SUM, and generates a 1/16 proportional current to IMON. Connect a resistor from IMON to ground to generate a voltage proportional to the output current. The IMON voltage is sampled, calculated, and stored in the I_{OUT} reporting register. The value in the I_{OUT} register is reported to the processor to avoid exceeding the thermal design point and maximum current capability of the system.

If the auto-phase shedding function is enabled via the PMBus, the total current report is used to determine whether to enter or exit phase-shedding mode to flatten the overall efficiency over the operating current range.

The MP2965 provides a user-programmable scaling factor and a user-programmable current offset. The programmable parameters allow users to match the IMON scaling to the design's voltage regulator tolerance band (VRTOB) calculation. This provides the most accurate current reporting across the entire load range and maximizes the performance of the processor turbo. Figure 11 shows the MP2965 IMON sense and report block diagram.

In Figure 11, the PMBus command MFR_IMON_DGTL_GAIN (4Dh) is used to fine-tune the ADC sense value with 0.1% resolution.

The PMBus command IOUT_CAL_GAIN_PMBUS (38h) converts the ADC-sensed V_{IMON} value to the direct format with 0.25A/LSB, which is reported via the PMBus command READ_IOUT (8Ch). The maximum report current is 522A.

The IOUT_RPT_GAIN_HC (A7h) and IOUT_RPT_GAIN_SVID_AVS (A8h) registers convert the sensed V_{IMON} value to the SVID current-reported format (FFh = IccMAX, IccMAX can be set greater than 255A to be compliant with the VR13.HC spec) or the AVSBus current reported format (10mA/LSB, and maximum report with 655.36A).

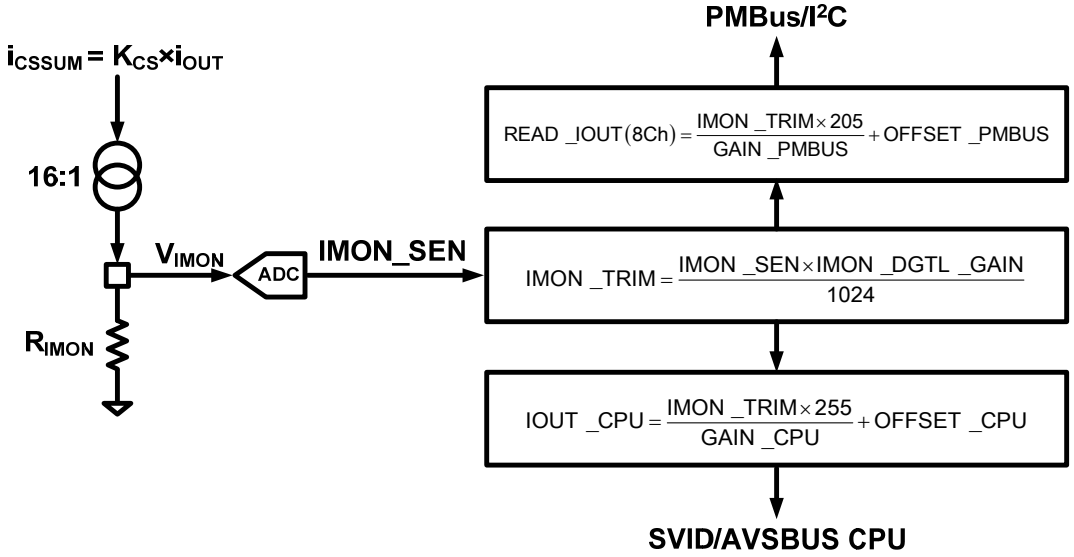


Figure 11: Total Current Sense and Report

Auto-Phase Shedding (APS)

To improve efficiency over the entire load range, the MP2965 supports automatic phase shedding (APS) according to the load current report. If APS mode is enabled, any SVID SetPS commands are ACK but do not affect the actual operating phase count.

In APS mode, the VR can be optimized to adjust the phase count to balance the performance between the transient and power consumption automatically.

As shown in Figure 12 (using 7-phase as an example), the VR works in 7-phase CCM at heavy load and 1-phase CCM at light load to

optimize efficiency. The VR enters 1-phase DCM at extremely light load reduce the switching loss further.

The APS function is implanted by comparing the sensed load current with each power state current threshold. The MP2965 provides three registers to program the APS current thresholds. The MFR_APS_LEVEL_XXP (C5h, C6h) register sets the power-state dropping threshold. A hysteresis is set with register MFR_APS_SET (C7h) to prevent the converter from changing the power state back and forth at a steady load current. Figure 13 shows the APS current thresholds setting from 1-phase CCM to 1-phase DCM.

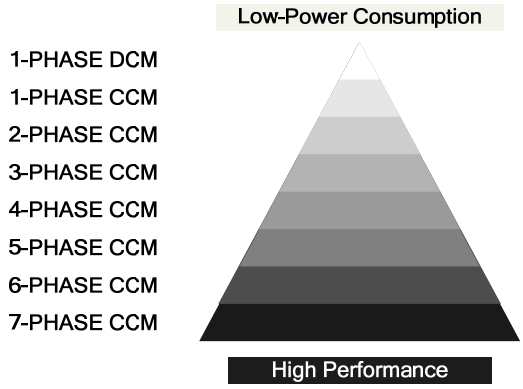


Figure 12: APS Function Diagram at 7-Phase Mode

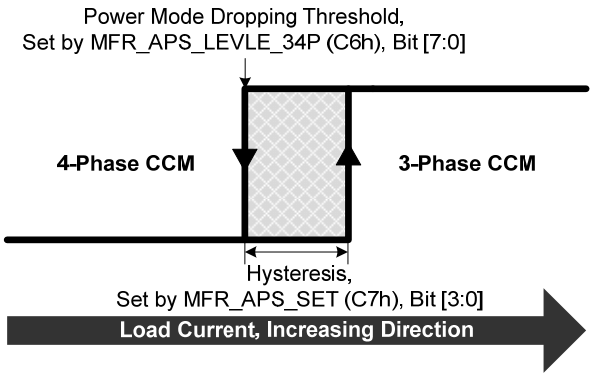


Figure 13: APS Threshold Setting between 4-Phase CCM and 3-Phase CCM

Table 5 lists the phase-shedding and -adding entry conditions based on the current report for 7-phase applications.

Table 5: Phase Shedding / Adding Based on Current Report for 7-Phase Applications in Rail1

Condition	Power State
I_{LOAD} > DROP_LEVEL_6P + MFR_APS_HYS	7-PH CCM
DROP_LEVEL_5P + MFR_APS_HYS < I_{LOAD} ≤ DROP_LEVEL_6P	6-PH CCM
DROP_LEVEL_4P + MFR_APS_HYS < I_{LOAD} ≤DROP_LEVEL_5P	5-PH CCM
DROP_LEVEL_3P + MFR_APS_HYS < I_{LOAD} ≤MFR_DROP_LEVEL_4P	4-PH CCM
DROP_LEVEL_2P + MFR_APS_HYS < I_{LOAD} ≤DROP_LEVEL_3P	3-PH CCM
DROP_LEVEL_1P + MFR_APS_HYS < I_{LOAD} ≤DROP_LEVEL_2P	2-PH CCM
I_{LOAD}< DROP_LEVEL_1P	1-PH CCM/DCM

Besides the sensed output current comparison, the MP2965 provides three conditions (listed below) to exit auto-phase shedding mode immediately and run in full-phase CCM operation to accelerate the load transient response and reduce the output voltage undershoot.

1. The VID on-the-fly (DVID) process makes the controller runs in full-phase CCM. After the output voltage is settled to the target value, new power state is determined by the load current.
2. A load step-up causing a VFB- window trip triggers full-phase CCM running to reduce the output voltage undershoot.
3. A load step-up causing the frequency changes to exceed a programmable limited threshold triggers full-phase running.

Current Balance and Thermal Balance Loop

The MP2965 provides a current-balance loop to achieve fair current sharing in multi-phase mode when different circuit impedance leads to the phase current difference.

The phase current is sensed and calculated with the current reference in the current loop.

Each phase's PWM on time is adjusted individually to balance the currents accordingly.

The MP2965 applies Σ-Δ modulation and delay line-loop technology in the current balance modulation to increase the resolution of the current balance modulation and reduce PWM jitter greatly. The time resolution of the digital system is 5ns. By applying Σ-Δ modulation and DLL technology, the digital PWM resolution can be increased to 0.08ns.

In the current balance loop, the MP2965 provides a current offset setting with the PMBus register MFR_CS_OFFSET1 (A5h, Page 0) and MFR_CS_OFFSET2 (A6h, Page 0) to achieve thermal balance. The phases with better cooling capability due to more proximity to the airflow can take more phase current by adding an offset to the sensed CS voltage.

The bandwidth of the current loop is relatively lower than the output voltage regulation loop, so it will not impact the output voltage regulation.

Input Voltage Sensing

The input power-supply voltage is sampled at IIN_SENP (see Figure 14). The sensed input voltage is used for PWM on time calculation, VIN_UVLO, VIN_OVP fault protection, VIN_UV warning, and input voltage monitoring.

There is an internal 16:1 resistive divider connected to the IIN_SENP pin to reduce the input voltage signal proportionally within the 1.6V ADC sense range.

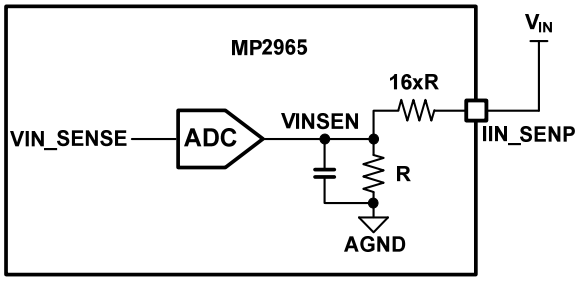


Figure 14: VIN Sensing Block Diagram

Input Current Sense

The MP2965 can sense the input current via an input current sensing resistor. The input current sense resistor is placed between the 12V input filter inductor and bulk capacitors placed on the local 12V plane feeding the domain voltage regulator circuits.

As shown in Figure 15, there are four stages to sample the input current:

1. The IIN_SENP and IIN_SENN pins senses the voltage over R_{IIN_SEN} into the chip.
2. The sensed voltage is converted to a current signal by the resistor $R_{I/V}$ ($R_{I/V}$ should be 100Ω or 200Ω).
3. The mirrored input current signal is sourced via IIN to the resistor R_{IIN} to generate a voltage signal for ADC sensing.
4. The MP2965 converts the sensed signal into direct current mode (0.0625A/LSB) for input current/power monitoring and indicates the over-input power warning via PWR_IN_ALT#.

V_{IIN} can be calculated with Equation (9):

$$V_{IIN} = \frac{I_{IN} \times R_{IIN\_SEN} \times R_{IIN}}{R_{I/V}} \quad (9)$$

Two 0.1 ~ 1μF ceramic capacitors (C_{IINn}, C_{IINp}) are recommended at both sides of the input current sensing resistor (R_{IIN_SEN}). Place these capacitors close to the MP2965 to bypass the noise from the input power plane. Refer the GND nodes of both capacitors to the internal quiet system GND plane. Do not refer the GND nodes to a noisy GND plane like the GND plane of the power state input decoupling capacitor.

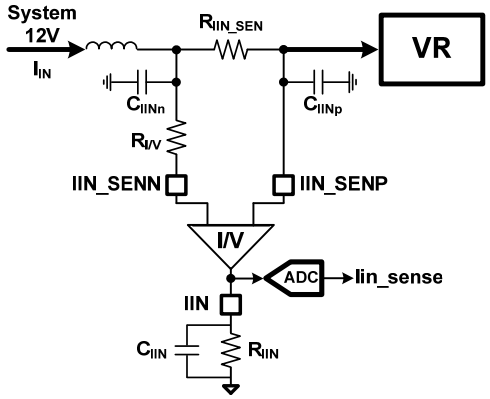


Figure 15: Input Current Sense Block Diagram

Temperature Sense

The MP2965 senses the Intelli-Phase's temperature by connecting the Intelli-Phase VTEMP pin to the MP2965 VTEMP pin (see Figure 16). The sensed temperature is used for over-temperature fault protection, over-temperature warning (assert VRHOT#), and power stage temperature monitoring.

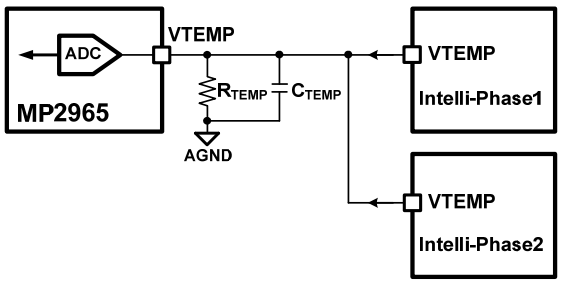


Figure 16: Temperature Sense for MP2965 with Intelli-Phase

C_{TEMP} is a VTEMP pin filtering capacitor. It is recommend to use a low, 1 ~ 10nF, ceramic capacitor for C_{TEMP}.

R_{TEMP} is a discharging resistor when the junction temperature is falling, ranging from 10 ~ 49.9kΩ.

The VTEMP pin of the Intelli-Phase reports a voltage output proportional to the junction temperature in Equation 10):

$$T_{JUNCTION}(℃) = a \times V_{TEMP}(V) + b \quad (10)$$

Where a is the temperature gain (in °C/V), and b is the temperature offset (in °C). For example, with a = 100°C /V, b = 10°C, and VTEMP = 700mV, then the junction temperature of the Intelli-Phase is 80°C. Refer to the Intelli-Phase datasheet for details on the values of a and b.

Operation of EEPROM

The MP2965 provides an EEPROM to store custom configurations. A 4-digit part number suffix is assigned for each application. The default configuration values for each 4-digit part can be pre-programmed at the MPS factory. The data can be programmed again by using the STORE_USER_ALL (15h) command via the PMBus. This requires 400ms of wait time for the process of storing data to the EEPROM. The EEPROM is read automatically during a power-on sequence or by the RESTORE_USER_ALL (16h) command via the PMBus. This requires at least 1ms of wait time for the process of restoring data from the EEPROM.

The operation of the EEPROM can be accomplished easily with the MPS GUI software.

The PMBus command WRITE_PROTECT (10h) ≠ 0x63 enables EEPROM write protection.

The EEPROM can be erased or written for more than 100,000 cycles. When the EEPROM is write-protected, the write into EEPROM action is ineffective.

EEPROM CRC Fault

If the data from the EEPROM is invalidated by the cyclic redundancy code (CRC) check during the system initialization process, the system enters an EEPROM CRC fault state and disables the output of both rails to wait for the error clear command. The configuration from the EEPROM is ignored.

The steps below describe how to clear the EEPROM fault and start up again:

1. Store the correct configuration into the EEPROM with the PMBus command STORE_USRE_ALL (15h).
2. Restart with a VDD33 power recycle or low-power mode EN toggle.

Low-Power Mode

The MP2965 can be programmed to operate in low-power mode or regular-power mode with the PMBus command MFR_VR_CONFIG3 (44h) bit[6].

When both EN1 and EN2 are low in low-power mode, the PMBus communication is disabled, and the VDD33 supply current can be reduced to 120μA.

In regular-power mode, the PMBus communication is available, and users can change the configurations in the EEPROM when both EN1 and EN2 are low.

Power On

The MP2965 is supplied by a +3.3V voltage at VDD33. VDD33 provides the bias supply for the analog circuit and internal 1.8V LDO. The 1.8V

LDO produces the +1.8V supply for the digital circuit. The system is reset by the internal power-on reset signal (POR) after the VDD33 supply is ready. After the system exits POR, the data in the EEPROM is loaded into the operating registers to configure the VR operation.

Figure 17a shows the power-on sequence of the MP2965 in regular-power mode.

t0~t1: at t0, VDD33 is supplied by a +3.3V voltage and reaches the VDD33 UVLO on threshold at t1. VDD18 reaches +1.8V when VDD33 is >1.8V.

t1~t2: at t1, the data in the EEPROM starts loading into the operating registers. The entire EEPROM copy process takes about 1.1ms, typically. During this stage, the PMBus address is detected if users select the voltage on ADDR_PL or ADDR_PH to set the PMBus address, or the boot-up voltage is detected if users select the voltage on BOOT to set the boot-up voltage.

t2~t3: at t2, after the EEPROM copy is finished, the MP2965 waits for either EN pin to pull high. The PMBus is available at this stage.

t3~t4: after EN1 pulls high, if the PMBus command OPERATION (01h, Page 0) is pre-set to the off state, Rail 1 halts at this stage and waits for an OPERATION on command. If OPERATION (01h, Page 0) is pre-programmed to the on state, the turn-on delay time (T_{on_delay}) begins counting. T_{on_delay} is PMBus programmable from 0 to 3276.75ms with the PMBus command TON_DELAY (60h, Page 0).

t4~t5: when T_{on_delay} expires, the Rail 1 VID-DAC begins ramping up VREF1 with the programmed slew rate to the boot-up voltage. During the soft-start process, OCP_Total protection, OVP2, and UVP are masked until VREF1 reaches the target value. The Rail 1 power-on sequence is completed at t5.

t6~t7: at t6, EN2 asserts, and OPERATION (01h, Page 1) is set to command on. Rail 2 begins the T_{on_delay} process. T_{on_delay} of Rail 2 is PMBus-programmable with register TON_DELAY (60h, Page 1).

t7~t8: when T_{on_delay} expires, the Rail 2 VID-DAC output begins ramping up VREF2. This is the soft-start process of Rail 2. At t8, the power-on sequence of both rails is completed.

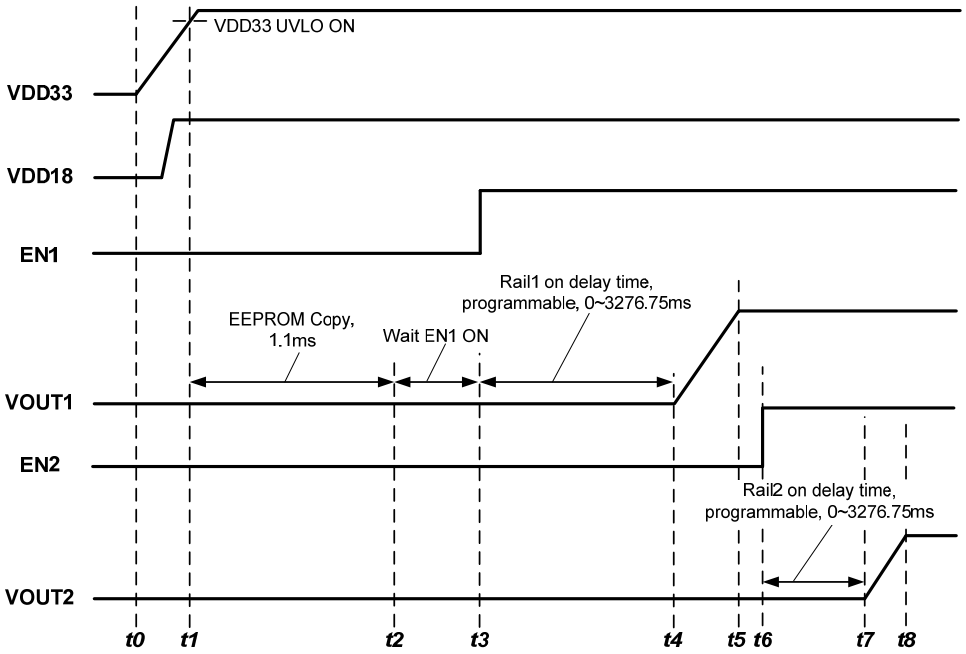


Figure 17a: Power-On Sequence at Regular Power Mode

Figure 17b shows the power-on sequence of the MP2965 in low-power mode.

t0~t1: at t0, VDD33 is supplied by a +3.3V voltage and reaches the VDD33 UVLO on threshold at t1. VDD18 reaches +1.8V when VDD33 is >1.8V.

t1~t2: at t1, VDD33 rises above the UVLO on threshold. The MP2965 waits for either EN pin to pull high. The PMBus is unavailable at this stage.

t2~t3: at t2, EN1 pulls high, and the data in the EEPROM begins loading into the operating registers. The entire EEPROM copy process takes about 1.1ms, typically. During this stage, the PMBus address is detected if users select the voltage on ADDR_PL to set the PMBus address, or the boot-up voltage is detected if users select the voltage on BOOT to set the boot-up voltage.

t3~t4: after the EEPROM copy is finished, if OPERATION (01h, Page 0) is pre-set to the off state, Rail 1 halts at this stage and waits for an OPERATION on command. If OPERATION (01h, Page 0) is pre-programmed to the on state, the turn-on delay time (T_{on_delay}) begins counting.

t4~t5: when T_{on_delay} expires, the VID-DAC starts ramping up VREF1 with a programmed slew rate to the boot-up voltage. During the soft-start process, OCP_Total protection, OVP2, and UVP are masked until VREF1 reaches the target value.

t6~t8: at t6, EN2 asserts, and the Rail 2 power-on sequence is the same as that in regular-power mode.

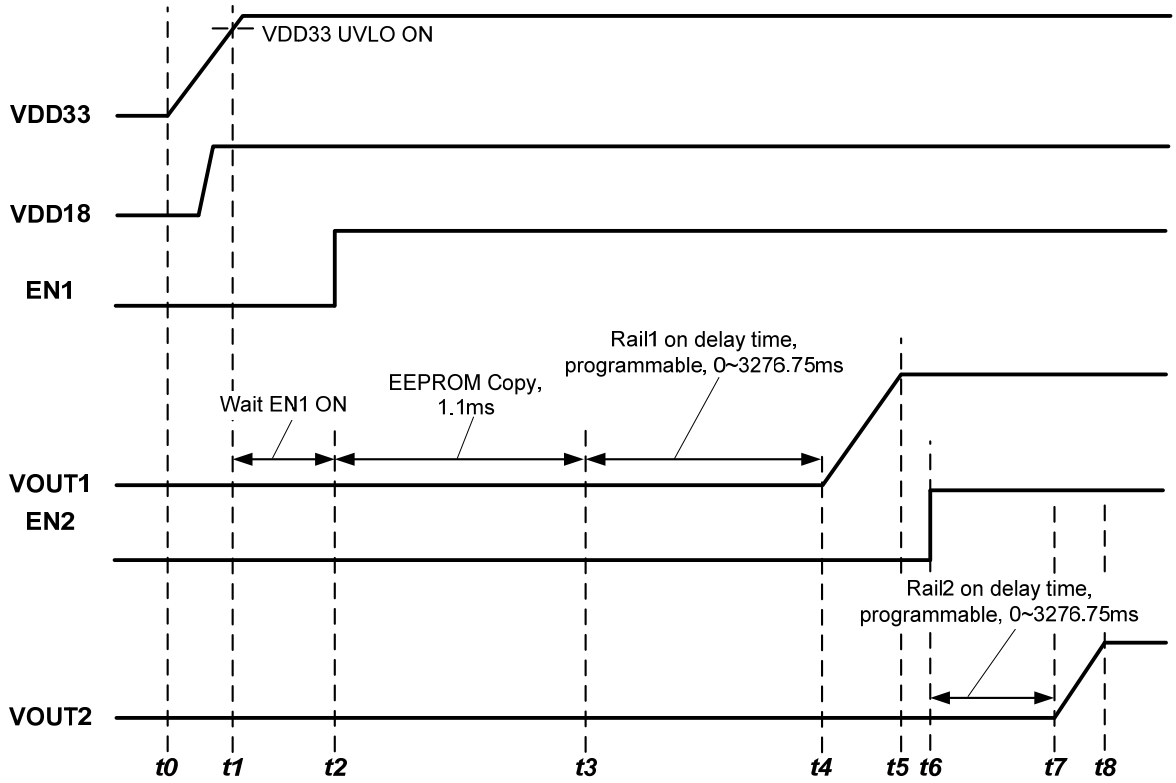


Figure 17b: Power-On Sequence at Low-Power Mode

Power-Off

The MP2965 can be powered off by the OPERATION command, SVID command, EN, VCCIO, VDD33 UVLO, or a protection shutdown.

1. VDD33 power off: Once the power supply on VDD33 falls below the falling threshold of the VDD33 UVLO, the MP2965 is powered off immediately.
2. EN off: The MP2965 provides Hi-Z off and soft-off via EN off in regular-power mode. When set to soft-off, V_{OUT} shuts down with the slew rate selected by register MFR_VR_CONFIG3 (44h) bit[5:4] until V_{REF} falls to the VID shutdown level. A turn-off delay time can be added via register TOFF_DELAY (64h).

   At low-power mode with both EN pins off, the MP2965 will Hi-Z off immediately without a turn-off delay, and the MP2965 enters standby mode with the smallest power consumption. The PMBus is unavailable until either EN1 or EN2 are pulled high.
3. Operation command off: The MP2965 provides Hi-Z off and soft-off with the OPERATION command off. When the OPERATION command is Hi-Z off, all PWMs enter tri-state when the OPERATION off command is received, and V_{OUT} is discharged by the load current. When the OPERATION command is soft off, V_{OUT} shuts down softly with the slow slew rate until V_{REF} reaches the VID shutdown level set by register MFR_VR_CONFIG2 (09h) bit [8:0]. Afterward, all PWMs enters tri-state.

   A turn-off delay time can be added at the operation command soft off via register TOFF_DELAY (64h).
4. SVID command off: When the MP2965 receives a SetVID command that set VID to 0V, the MP2965 begins to shut down immediately. After the MP2965 enters the VID off state, it waits until the next SetVID command is greater than 0V to boot up again without T_{on_delay}.

   VCCIO shutdown: If the VCCIO shutdown function is enabled, and the voltage on VCCIO falls below 0.65V, the VR shuts down softly with half of the fast slew rate immediately. After V_{REF} ramps below the VID shutdown level, the VR enters Hi-Z off. Each rail provides an independent bit to enable the VCCIO shutdown function.
5. Protection shutdown: Once a fault (VIN OVP/UVLO, VOUT UVP, IOUT OCP, OTP, CS fault, or VTEMP fault from Intelli-Phase) is triggered, the VR enters Hi-Z off immediately. When VOUT OVP is triggered, the VR turns on all active low-side MOSFETs to discharge C_{OUT} and shut down immediately until V_{OUT} falls below 300mV (RVP).

Figure 18a shows the EN soft-off power sequence in regular-power mode.

Figure 18b shows the EN Hi-Z off power sequence in low-power mode. When both EN pins are pulled low, the VR shuts down immediately without an off time delay.

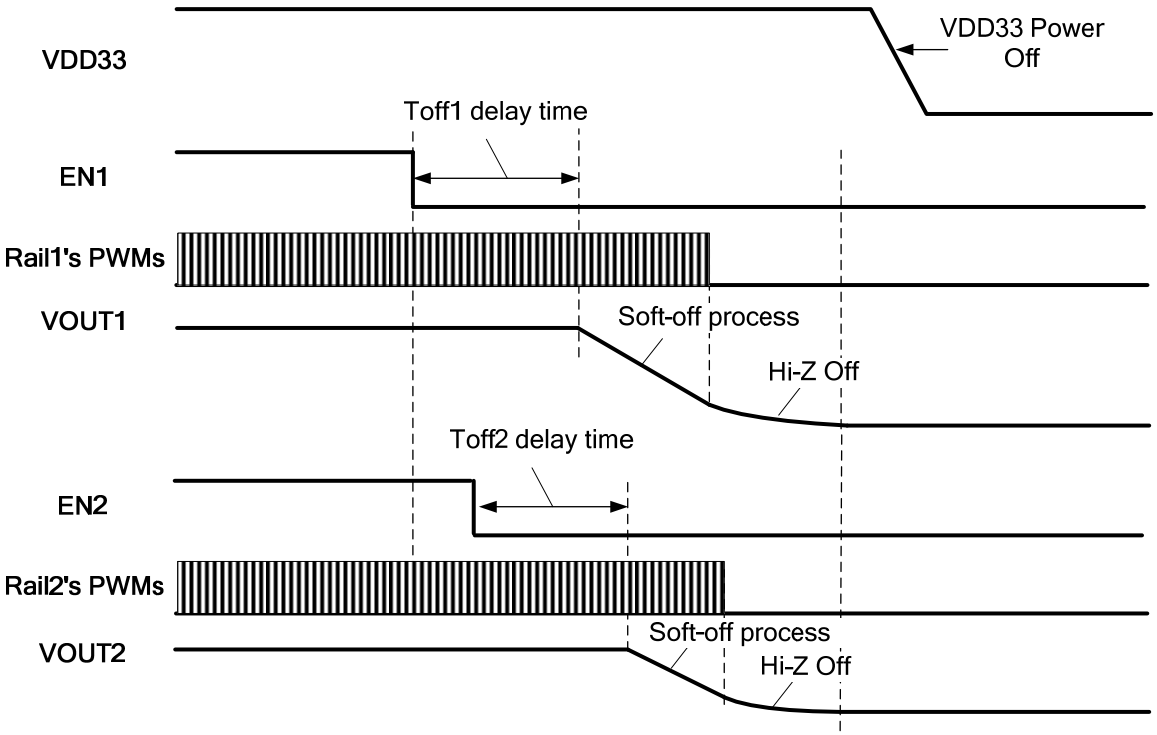


Figure 18a: Power-Off Sequence in Regular-Power Mode with Soft-Off

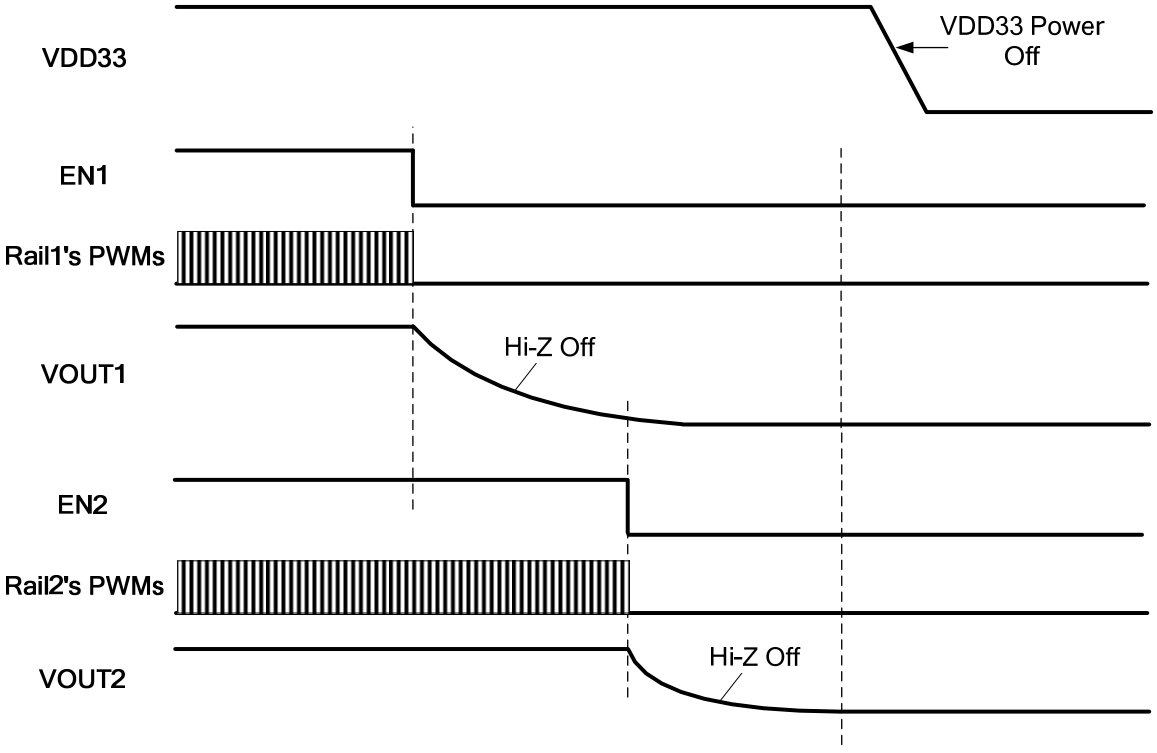


Figure 18b: Power-Off Sequence in Low-Power Mode with Hi-Z Off

Power Good Indication

The MP2965 indicates a power good with VRRDY1 (Rail 1) and VRRDY2 (Rail 2). There are two modes available for the MP2965 VRRDY assertion: non-Intel mode and Intel mode.

Non-Intel Mode

The power good on and off thresholds are programmable via the registers POWER_GOOD_ON (5Eh) and POWER_GOOD_OFF (5Fh).

During the soft-start process, when V_{REF} rises above the POWER_GOOD_ON threshold, the MP2965 starts delay time counting and asserts VRRDY when the delay time ends. The delay time is programmable via the register MFR_PGOOD_SET (5Dh). The POWER_GOOD_ON threshold must be lower than the boot-up voltage value.

After the boot-up finishes, when V_{REF} is below the POWER_GOOD_OFF threshold, the MP2965 de-asserts VRRDY immediately. The POWER_GOOD_OFF threshold must be set lower than the VID value that will be regulated at the normal operation process.

If the MP2965 is in Hi-Z off status for the fault protections, the PMBus command off status, or EN pulls low, VRRDY is de-asserted immediately.

Figure 19 shows the power good indication in regular-power mode.

Intel Mode

When the MP2965's boot-up voltage is 0V, VRRDY asserts when T_{ON_DELAY} expires.

When the MP2965's boot-up voltage is greater than 0V, VRRDY asserts when the boot-up voltage is settled.

After boot-up, if the CPU sends the VID command to 0V with the register MUL_VR_CONFIG is 0, VRRDY is de-asserted immediately. If the register MUL_VR_CONFIG is 1, VRRDY continues asserting with VID = 0V.

At PG Intel mode, the associated VRRDY de-asserts immediately when the VR shuts off for the fault protections. When the PMBus is operation command off or EN pulls low, VRRDY is de-asserted immediately.

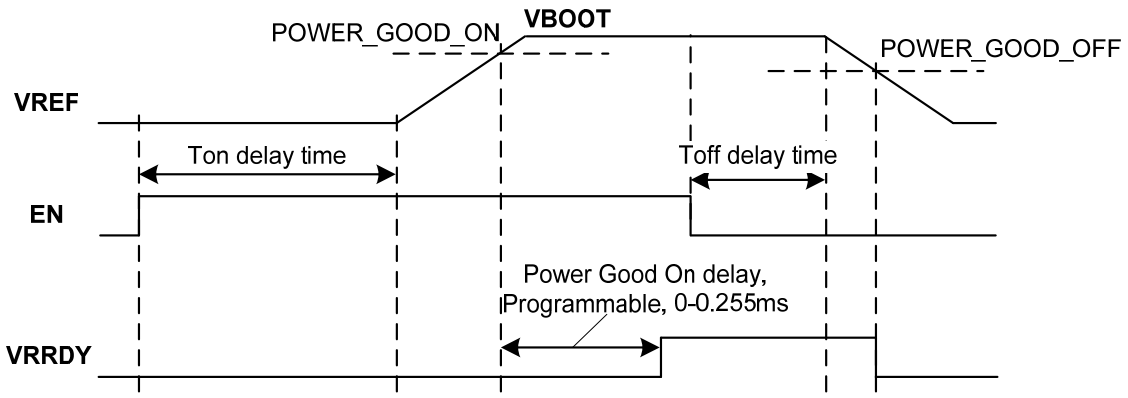


Figure 19: Power Good On/Off Sequence at Regular-Power Mode and EN Soft-Off

Fault and Protections

The MP2965 supports the fault monitoring and protections listed below.

V_{IN} UVLO and OVP

The VR shuts off immediately by forcing the PWM signals into tri-state if the sensed input voltage is below the VIN_OFF threshold. The VR restarts again when the sensed input voltage is above the VIN_ON threshold. The VIN UVLO threshold is programmable with register VIN_ON (35h) and VIN_OFF (36h) with 0.125V/LSB.

The VR shuts off if the input voltage is above the VIN OVP threshold set with register VIN_OV_FAULT_LIMIT (55h). VIN OVP can be set to either latch-off or auto-retry mode.

Over-Current Protection (OCP)

Over-current protection applies a dual OCP mechanism with two types of thresholds. The first type OCP_Total is a time- and current-based threshold. The OCP_Total limit is programmable via the PMBus command MFR_OCP_TOTAL_SET (EEh). OCP_Total trips when the sensed average output current exceeds the setting threshold for a period of time (OCP blanking time). OCP_Total can be programmed to no action, hiccup, retry six times, and latch-off mode via the PMBus.

The controller takes no action in no action mode and continues switching until another protection is tripped. The fault indication bit in register STATUS_IOUT (7Bh) and STATUS_WORD (79h) are not set to no action mode.

In hiccup mode, the controller forces the PWM signals into tri-state to disable the output and attempts to restart after 12.5ms of protection delay time.

In retry six times mode, the VR restarts six times at most. If the fault is removed within six restarts, the VR resumes normal operation. If the fault remains after six restarts, the VR shuts down until the VDD33 power is cycled, EN toggles, or the PMBus on command.

In latch mode, the VR shuts down until the VDD33 power cycles, EN toggles, or the PMBus off and on command.

The above four protections are available for OCP_Total, V_{OUT} UVP, and V_{OUT} OVP2.

The second type of threshold is OCP_Phase, a current-based limitation protection. The MP2965 monitors the phase current cycle-by-cycle. When the phase current exceeds the OCP_Phase threshold during the PWM off time, the PWM remains low to discharge the inductor current below the setting threshold. If the load current continues rising, the output voltage drops, since the inductor current is limited. OCP_Phase is implemented generally accompanying UVP. The OCP_Phase threshold is PMBus-programmable with register MFR_OCP_PHASE_SET (F0h).

Under-Voltage Protection (UVP)

The MP2965 provides under-voltage and over-voltage protection (UVP, OVP) by monitoring VDIFF.When VDIFF is lower than the UVP threshold for a given time (UVP blanking time), the controller forces the PWM signals into tri-state to disable the output power. The register MFR_OVP_UVP_SET (F1h) determines the UVP protection mode.

The MP2965 provides three UVP thresholds at the remote sense amplifier unit gain: V_{REF} - 300mV, V_{REF} - 220mV, and V_{REF} - 140mV. The UVP threshold is programmed via PMBus command MFR_VR_CONFIG3 (44h) bit[2:0]. Note that when the remote sensing amplifier is programmed to half gain, the UVP threshold is doubled.

As in the OCP_Total protection scheme, the UVP scheme also provides no action, hiccup, retry six times, and latch-off options.

Over-Voltage Protection (OVP)

The MP2965 applies dual OVP approaches: OVP1 and OVP2. When any OVP is tripped, the MP2965 turns on all low-side MOSFETs to discharge C_{OUT} until V_{OUT} falls below 300mV. Then Hi-Z off occurs.

OVP2 is the OVP type referred to VREF. OVP2 is tripped when VDIFF is higher than the OVP2 threshold for the blanking time. The MP2965 provides three OVP thresholds: V_{REF} + 300mV, V_{REF} + 220mV, and V_{REF} + 140mV at the remote sense amplifier unit gain.

The OVP threshold is programmed via PMBus command MFR_VR_CONFIG3 (44h) bit[2:0]. Note that when the remote sensing amplifier is programmed to half gain, the OVP threshold is doubled.

As in UVP, the MP2965 provides no action, hiccup, retry six times, and latch-off protection modes for OVP2.

The second type is referred to as OVP1, which is tripped when VDIFF is higher than the OVP1 threshold without triggering a delay time. The OVP1 threshold is set as VOUT_MAX (24h) + 400mV regardless of whether the gain of the remote sense is set to unit or half. The OVP1 fault is always in latch mode.

Over-Temperature Protection (OTP)

The MP2965 attains the junction temperature of the Intelli-Phase by connecting VTEMP from the power stage to the controller (see Figure 16).

If the sensed temperature is higher than the register OT_WARN_LIMIT (51h), VRHOT# asserts and informs the processor to reduce the power dissipation. When the sensed temperature falls below OT_WARN_LIMIT - 3°C, VRHOT# is de-asserted. If the sensed temperature is higher than the threshold set in register MFR_OTP_SET (EDh), the VR Hi-Z shuts down. OTP can be programmed to either latch-off or auto-retry mode with PMBus command MFR_OTP_SET (EDh).

VDIFF Short-Circuit Protection (SCP)

The MP2965 supports VDIFF short-circuit protection to prevent the VR from an over-voltage condition when VDIFF is shorted to GND by a fault. The VDIFF short-circuit can be enabled with PMBus command MFR_VR_CONFIG4 (1Fh) bit[10]. VDIFF short-circuit protection is active when the boot-up starts. When a VDIFF short-circuit is detected, the associated rail is shut down immediately, and the fault is reported with STATUS_VOUT (7Ah) bit[0]. VDIFF short-circuit is only recommended when no external remote sensing divider is applied.

Line Floating Detection

The MP2965 supports remote sensing line (VOSEN, VORTN) floating detection at the system initialization process after VDD33 power-on or EN power-on from low-power mode. The MP2965 latches down if a line float is detected and reports the fault with the PMBus command STATUS_VOUT (7Ah) bit[1]. Line float detection can be enabled with MFR_LINE_FLOAT_EN (04h, Page 1).

CS Fault Detection and VTEMP Fault Detection

The MP2965 supports VTEMP fault and CS fault detection. When the device detects VTEMP to be above 1.25V, the output is disabled for the VTEMP fault. If any CS pin is pulled below 200mV, the CS fault shuts off the output. When either fault occurs, the MP2965 can be enabled to start Intelli-Phase fault type detection.

The MPS Intelli-Phase supports fault reporting by pulling FAULT# low (e.g.: MP86945A) or pulling VTEMP high to 3.3V (e.g.: MP86936). The Intelli-Phase FAULT# pin can be connected to CS, or VTEMP pins of the controller and Intelli-Phase can be connected to shut down the VR and monitor the fault type when an Intelli-Phase fault occurs.

Figure 20a shows an Intelli-Phase fault type detection example when working with the MP86945A. The FAULT# signal of each MP86945A is tied to its own CS pin. When a fault occurs on any MP86945A, its FAULT# signal asserts and pulls CS low.

Figure 20b shows an Intelli-Phase fault type detection example when working with the MP86936. To prevent OTP from triggering VTEMP erroneously, a half-gain resistor divider is required from the MP86936 VTEMP output and the MP2965 VTEMP input.

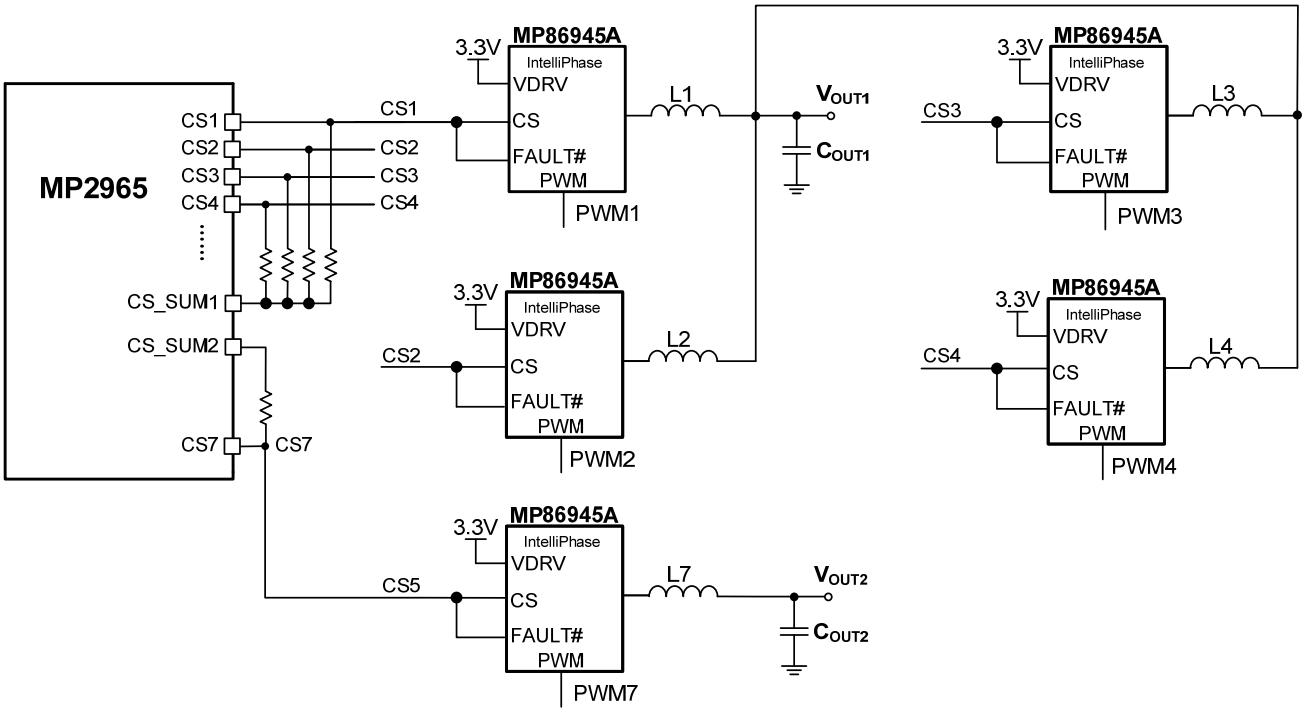


Figure 20a: Fault Detection from each CS Pin of MP86945A

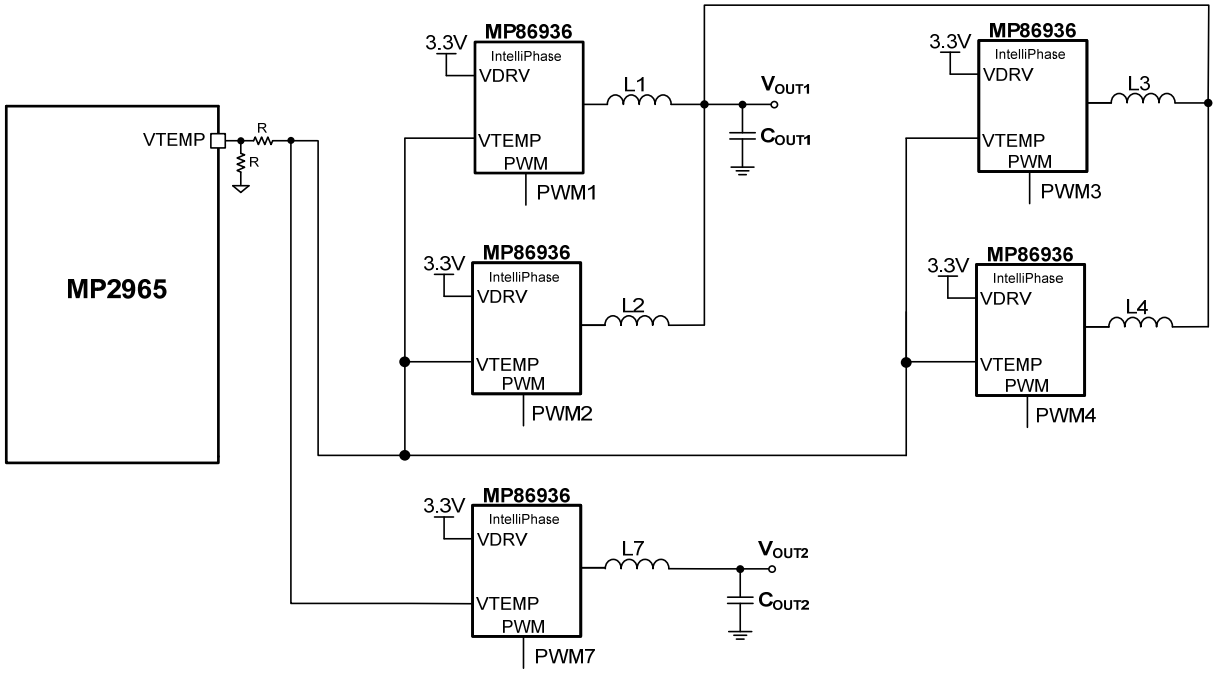


Figure 20b: Fault Detection from VTEMP Pin of MP86936

Intelli-Phase Fault Detection

The MP2965 supports Intelli-Phase fault type detection. There are several types of Intelli-Phase faults:

- Over-current limit
- Over-temperature
- Low-side MOSFET short
- High-side MOSFET short

MPS Intelli-Phase products support some or all of the fault types above. When any fault occurs, the Intelli-Phase indicates a fault status by pulling VTEMP to VDD or pulling FAULT# low. Some Intelli-Phase products report the fault type by setting the PWM unique impedance. Refer to the datasheet of the Intelli-Phase for details.

The MP2965 scans the PWM impedance after any of the following faults occur: VIN UVLO, VIN OVP, OTP, VOUT UVP, VOUT OVP, OCP_Total, VDIFF short to GND, VTEMP fault, and CS fault if the fault protection and PWM fault detection are both enabled.

As shown in Figure 21, when any of the above faults occur, the MP2965 operates as follows:

1. The associated rail(s) are shut off.
2. Intelli-Phase fault type scan for related rail(s) begins by detecting the impedance on the PWM pin.
3. Faults are reported to the Page 0's registers MFR_FAULTS1 (FCh), MFR_FAULTS2 (FDh), and MFR_FAULTS3 (FEh).
4. Faults are recorded to the EEPROM (FCh, FDh, and FEh, Page 29) when fault recording to the EEPROM is enabled. The fault type can be read back at the next power-on cycling. To store faults in the EEPROM, the EN signal should be kept high for at least 20ms after a fault occurs.

The related registers shown below are used to program the behavior of fault detection and recording to the EEPROM in case an Intelli-Phase fault occurs.

1. Enable bit(s) of the fault protections with individual fault protection registers.
2. Enable bit of ADC to sample the fault type on the PWM pin of the Intelli-Phase (MFR_VR_PROTECT (2Eh) bit[10]).
3. Enable bit to record the fault to the EEPROM (MFR_EEPROM_CTRL (1Dh) bit[1]).

The fault bits in the Page 0 fault registers FCh, FDh, and FEh are either live or latched. Refer to the Register Map section on page 44 for more information. Send the PMBus command CLEAR_FAULT (03h) to clear the latched bits if the fault status is gone.

To clear the fault recorded in the EEPROM register, write 0x0000 to FCh, FDh, and FEh after turning PAGE (00h) to Page 29. This is a direct access to the EEPROM registers. The time required for each write command is 5ms.

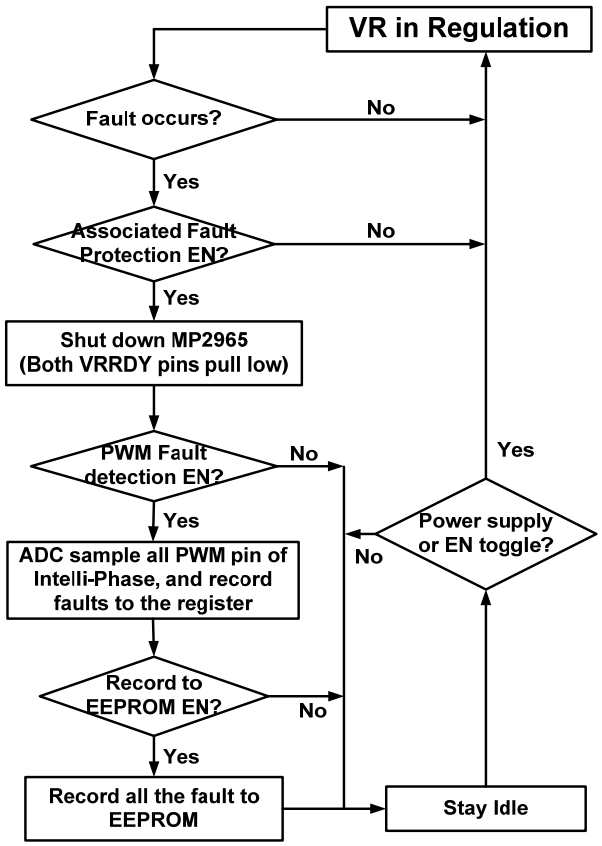


Figure 21: Flow Chart of Intelli-Phase Fault Detection

VFB Window

In MP2965 there is a feedback voltage (V_{FB}) window (V_{REF} - 25mV ~ VFB+20mV), which provides the advanced un-linear loop control to fasten the transient performance.

When V_{FB} is higher than V_{REF} + 20mV (VFB+ window), all PWM pins pull low and blank the PWM-set signal until V_{FB} falls below the VFB+ window. The VFB+ window is usually used to reduce the overshoot at the load release, especially at multi-phase operation.

When V_{FB} is lower than V_{REF} - 25mV (VFB- window), the VR exits auto-power mode

immediately and enters full-phase running to improve the transient response.

Phase Number Configuration

The MP2965 can be configured with a different phase number application via the PMBus (see Table 6).

Table 6: Phase Number Configuration and Active PWM Pins

MFR_VR_CONFIG (E4h)		Active PWM Pins	
Page 0, Bit[2:0]	Page 1, Bit[1:0]	Rail 1	Rail 2
3'b111	2'b00	1 ~ 7	N/A
3'b110	2'b01	1 ~ 6	7
3'b101	2'b10	1 ~ 5	6, 7
3'b101	2'b01	1 ~ 5	7
3'b100	2'b11	1 ~ 4	5~7
3'b100	2'b10	1 ~ 4	6, 7
3'b100	2'b01	1 ~ 4	7
3'b011	2'b11	1 ~ 3	5 ~ 7
3'b011	2'b10	1 ~ 3	6, 7
3'b011	2'b01	1 ~ 3	7
3'b010	2'b11	1,2	5 ~ 7
3'b010	2'b10	1,2	6, 7
3'b010	2'b01	1,2	7
3'b001	2'b11	1	5 ~ 7
3'b001	2'b10	1	6, 7
3'b001	2'b01	1	7

When the phage count is configured as 0, the VR operates in 1-phase DCM.

Any unused PWM enters tri-state. The active phase is interleaved automatically. Float any unused PWM pins, and connect any unused CS pins to either CS_SUM1 or CS_SUM2.

When Rail 2 of the MP2965 is unused, tie EN2 to AGND, connect VOSEN2 and VORTN2 to AGND, connect IMON2 to AGND, short VFB2 and VDIFF2 together, connect any unused CS pin to CS_SUM2, and float any unused PWM pins.

Couple Inductor Mode

The Rail 1 of the MP2965 supports couple inductor mode to reduce the overshoot during load releasing. The couple inductor mode can be enabled by the MFR_VR_CONFIG3 (44h) register on Page 0.

To achieve the correct couple inductor mode, the phase count should be programmed as an even number. Refer to Table 7 for coupled phases definition in the MP2965.

Table 7: Coupled Phases Group Requirement

Phase Count	Coupled Phases
2-phase	Phase 1 and Phase 4
4-phase	Phase 1 and Phase 4 Phase 2 and Phase 5
6-phase	Phase 1 and Phase 4 Phase 2 and Phase 5 Phase 3 and Phase 6

Figure 22 shows the phase connection for a 6-phase couple inductor application. If the application is 4-phase, disconnect Phase 3 and Phase 6 (float PWM3, PWM6). The MP2965 can interleave the left phase automatically.

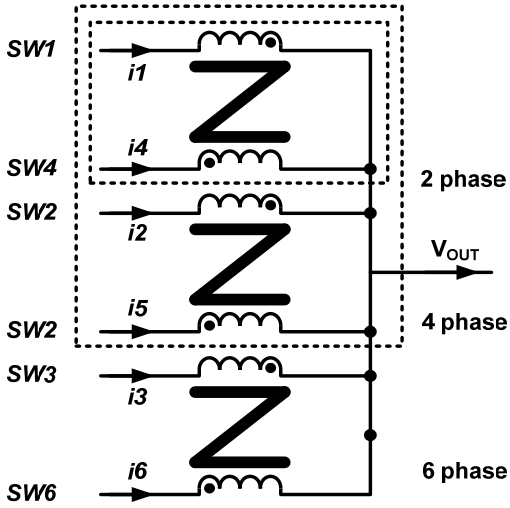


Figure 22: Couple Inductor Connection

The MP2965 supports the auto-phase shedding function in couple inductor mode to flatten the overall VR efficiency. The coupled Phase 3 and Phase 6, and Phase 2 and Phase 5 are shed together to prevent a coupling current from appearing on the tri-state phases via the couple inductor. In light load, the MP2965 sheds to Phase 1 during operation only.

As shown in Figure 23, when MP2965 sheds to only Phase 1 at light load, Phase 4's low-side MOSFET can be programmed to turn on simultaneously with PWM1 to let the coupling current from Phase 1 flow through the low-side MOSFET instead of the bode diode of Phase 4 to increase efficiency in light load.

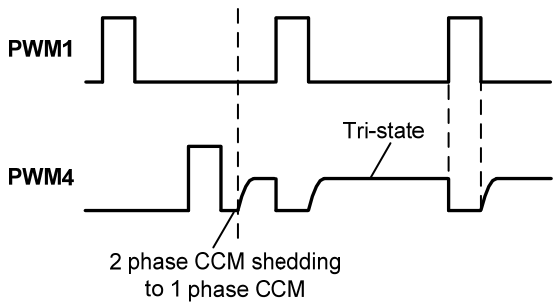


Figure 23: Phase Shedding to 1-Phase CCM

PMBUS/I²C COMMUNICATION

The Power Management Bus (PMBus) is an open-standard, power-management protocol that defines a means of communicating with power conversion and other devices. It is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. A master device connects to the line, generates the SCL signal and device address, and arranges the communication sequence. This is based on the principles of I²C operation.

The MP2965 supports 100kHz, 400kHz, and 1MHz bus timing requirements. Timing and electrical characteristics of the PMBus can be found in the Electrical Characteristics section on page 10 or in the PMB Power Management Protocol Specification, part 1, revision 1.3, which is available at http://PMBus.org.

PMBus/I²C Address

To support multiple VR devices used with the same PMBus/I²C interface, the MP2965 provides PMBus address programming through either the ADDR pin or register MFR_ADDR_PMBUS (E1h).

The device address is a 7-bit code and ranges from 0x00 to 0x7F. The 3MSB bits can be set either by the register or by ADDR_PH. The 4LSB bits can be set either by the register or by ADDR_PL.

The address of 00h is reserved as the all-call address. Do not set it as the MP2965 unique device address.

Register MFR_ADDR_PMBUS (E1h) is used to program or store the device addresses. Bit[7] sets the device address 4LSB bits configuration mode.

When bit[7] = 0, the 4LSB bits are determined by the ADDR_PL voltage and stored in register E1h bit[3:0]. When bit[7] = 1, the 4LSB is set with register E1h, bit[3:0]. Bit[8] sets the device address 3MSB bit configuration mode. When bit[8] = 0, the 3MSB bits are determined by the ADDR_PH voltage and stored in register E1h bit[6:4]. When bit[8] = 1, the 3MSB is set with register E1h bit[6:4]

The ADDR_PL and ADDR_PH voltage can be programmed by the resistor divider from VDD18 to AGND tapped to ADDR_PL and ADDR_PH. Figure 24 shows the recommended connections for the pin set. Table 8 shows the resistor values for the different device addresses.

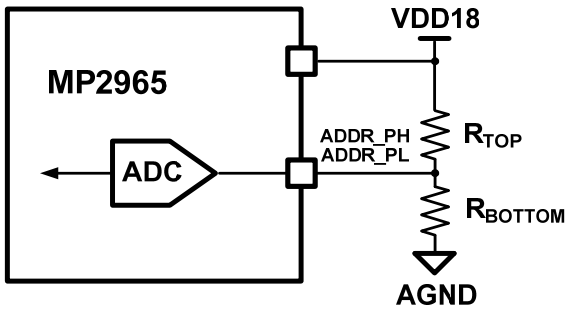


Figure 24: Recommend Circuit Design for PMBus Address Pin Set

Table 8: PMBus address from Pin Set

ADDR_PH		ADDR_PL	Setting Voltage (V)	R_{TOP} (kΩ) 1%	R_{BOT} (kΩ) 1%
PMBus W/R Hardware Protect	Address [6:4]	Address 4LSB			
Disable	0h	0h	0	-	0
Enable		1h	0.031	3.32	0.059
Disable	1h	2h	0.057	3.32	0.11
Enable		3h	0.084	3.32	0.162
Disable	2h	4h	0.116	3.32	0.226
Enable		5h	0.156	3.32	0.316
Disable	3h	6h	0.205	3.32	0.43
Enable		7h	0.266	3.32	0.576
Disable	4h	8h	0.340	3.32	0.768
Enable		9h	0.430	3.32	1.05
Disable	5h	Ah	0.540	3.32	1.43
Enable		Bh	0.675	3.32	2
Disable	6h	Ch	0.844	3.32	2.94
Enable		Dh	1.048	3.32	4.64
Disable	7h	Eh	1.301	3.32	8.66
Enable		Fh	1.500	3.32	16.5

Data and Numerical Format

The MP2965 uses the direct format internally to represent real-world values, such as voltage, current, power, temperature, time, etc.

For the voltage in a VID format, the real-world voltage follows Equation (11):

$$V_{REAL}(V) = \begin{cases} \frac{(VID + 29) \times VID\_STEP(mV)}{1000} & IMVP9\_10mV \\ \frac{(VID + 49) \times VID\_STEP(mV)}{1000} & others \end{cases} \quad (11)$$

Where V_{REAL} is the real-world voltage, VID_STEP is the VID voltage resolution (5mV or 10mV), and VID is the register value (in decimal). IMVP9_10mV refers to the Intel IMVP9 VID table with 10mV VID resolution. The Intel IMVP9 VID table can be enabled by register MFR_VBOOT_SET (E5h) bit[8].

All numbers with no suffixes in this document are decimals unless explicitly designated otherwise.

Numbers in a binary format are indicated by a prefix “n’b”, where n means the binary count, and b means binary format. For example, 3’b000 is a 3-bit binary data, and the binary data is 000.

The suffix “h” indicates a hexadecimal format, which is generally used for the register address number in this document.

The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0x88 is a 1-byte number whose decimal value is 136.

PMBus Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several types of data transmission faults listed below.

- Sending too few data
- Reading too few data
- The host sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure recorded in the register STATUS_CML (7Eh) of both pages. The CLEAR_FAULTS (03h) command can be used to clear the fault record for both pages.

PMBus/I²C Transmission Structure

The MP2965 supports five kinds of transmission structures with or without PEC:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

The MP2965 supports the packet error checking (PEC) mechanism, which can improve reliability and communication robustness. The PEC is a CRC-8 error-checking byte calculated on all the message bytes (including addresses and read/write bits). The MP2965 processes the message only if the PEC is correct.

The PEC is calculated in CRC-8 represented by the polynomial in Equation (12):

$$C(x) = x^8 + x^2 + x^1 + 1 \quad (12)$$

Figure 25a shows the supported PMBus/I²C transmission structure without PEC.

Figure 25b shows the supported PMBus/I²C transmission structure with PEC.

To read or write the registers of the MP2965, the PMBus/I²C command must be compliant with the byte number of the register in the register maps.

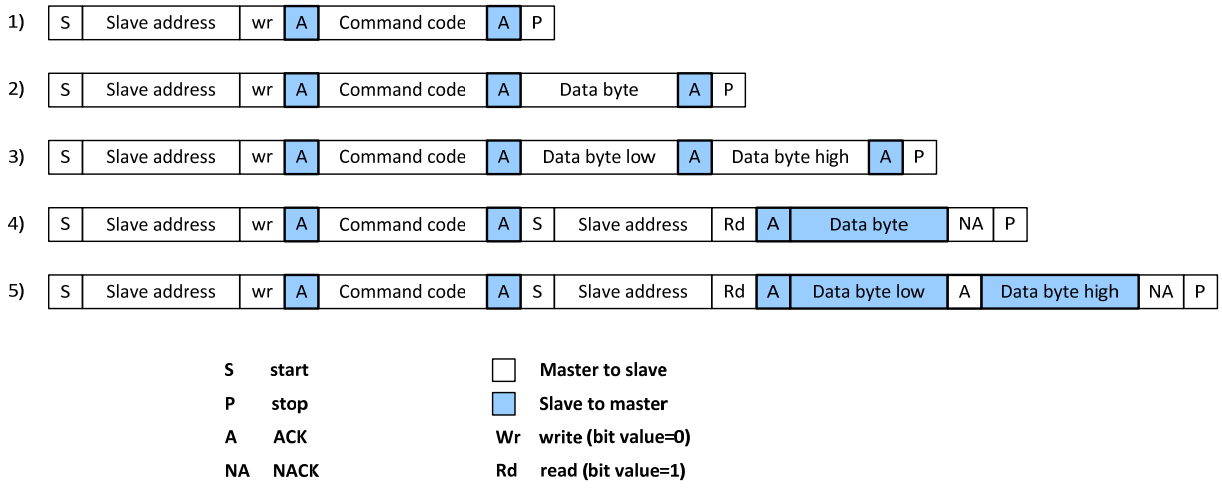


Figure 25a: Supported PMBus/I2C Transmission Structure without PEC

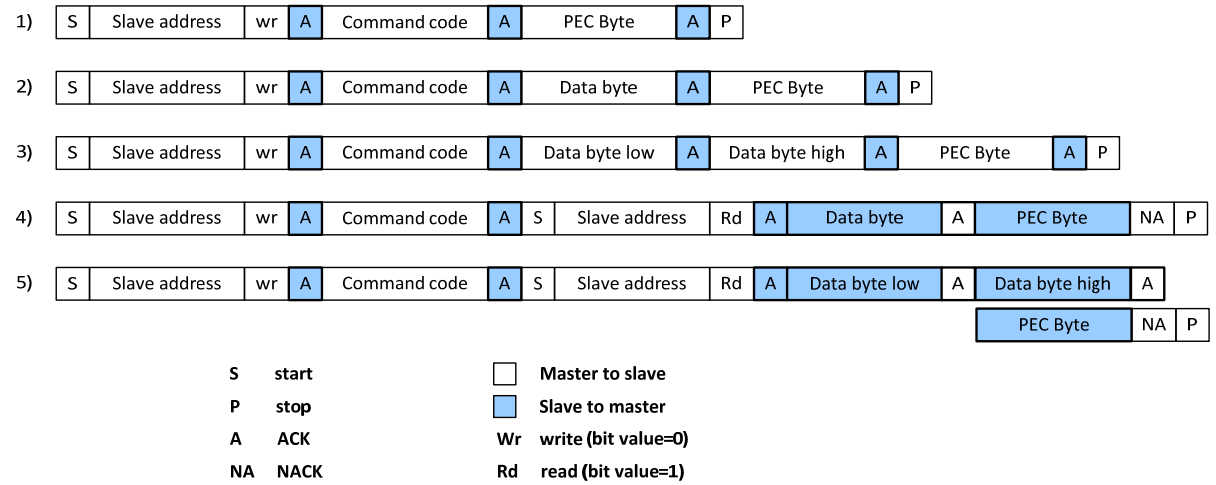


Figure 25b: Supported PMBus/I2C Transmission Structure with PEC

PMBus Reporting and Status Monitoring

The MP2965 supports real-time monitoring for the VR operation parameters and status with the PMBus interface.

Table 9 lists the monitored parameters.

Table 9: PMBus Monitored Parameters

Parameter	PMBus	Register
Input voltage	0.03125V/LSB	88h
Input current	0.0625A/LSB	89h
Output voltage	VID or 1mV/LSB	8Bh
Output current	0.25A/LSB	8Ch
Temperature	1°C/LSB	8Dh
Output power	1W/LSB	96h
Input power	1W/LSB	97h
Phase current	See register map 74h ~ 76h	
Power good	✓	79h
V_{OUT} OV fault	✓	7Ah
V_{OUT} UV fault	✓	7Ah
OC fault	✓	7Bh
OT fault	✓	7Dh
V_{IN} UVLO fault	✓	7Ch
V_{IN} OVP fault	✓	7Ch
PMBus fault	✓	7Eh
EEPROM fault	✓	7Eh
V_{OUT} UV warning	✓	7Ah
VID max/min extend warning	✓	7Ah
OC warning	✓	7Bh
OP warning	✓	7Bh
OT warning	✓	7Dh
V_{IN} UV warning	✓	7Ch
Over input power warning	✓	7Ch
PMBus PEC error	✓	7Eh
EEPROM CRC error	✓	7Eh

PMBus Write/Read (W/R) Limitation

The MP2965 supports PMBus write and read (W/R) protection through both software and hardware methods.

For the software method, set a non-zero, 16-bit code to register MFR_PWD_USER (A7h, Page 1) and store it in the EEPROM to enable the function. After the power-on recycle, PMBus W/R is limited until the correct 16-bit password is entered with the PMBus command PWD_CHECK_CMD (F2h, Page 0).

For the hardware method, by selecting the resistor divider value of ADDR_PH, PMBus W/R protection can be set until the resistor value is changed in the ADDR_PH pin (see Table 8). The hardware method has the highest priority to prevent the MP2965 from being accessed via the PMBus. A jumper or a switch can be used to achieve hardware protection for the PMBus W/R (see Figure 26).

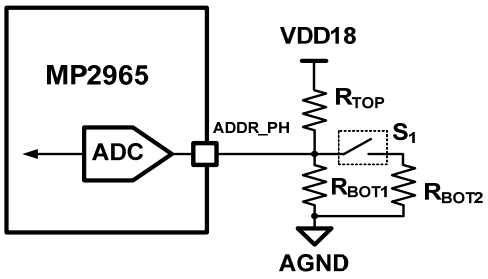


Figure 26: Circuit to Achieve Hardware Protection for PMBus W/R

When PMBus W/R protection is enabled, the registers listed in the PMBus Command List table on page 44 with a value of “Y” in column “PMBus W/R PRT?” are not accessible. The registers with a value of “N” in column “PMBus W/R PRT?” are still accessible. These accessible registers mean PMBus status monitor and dynamic VID transition are still available.

SVID Interface

To support multiple VR devices used on the same SVID bus, the register MFR_ADDR_SVID_AVSBUS (E6h) is used to program the SVID address.

The SVID address is a 4-bit code. There are 14 addresses for up to 14 voltage regulator controllers or voltage rails. The final addresses, 0Eh and 0Fh, are reserved as All Call addresses, and all VR controllers respond to them. The register MFR_ADDR_SVID_AVSBUS (E6h, Page 0) bit[11:10] can be programmed to select the All Call addresses as 0Eh or 0Fh.

The SVID address of Rail 1 and Rail 2 are set by MFR_ADDR_SVID_AVSBUS (E6h, Page 0) bit[9:0]. Refer to the Page 0 register map section on page 106 for more details.

If Rail 2 is configured as a point-of-load (POL) and does not need a SVID address, Rail 2 can be set to reject all SVID commands from the processor with the PMBus command MFR_DDR_SET (CFh, Page 0).

Over-Clocking

The MP2965 supports two types of over-clocking modes: tracking mode and fix mode.

1. Tracking Mode: In over-clocking tracking mode, the VR controller adds an offset VID with PMBus command VOUT_OFFSET (23h). When the CPU changes VID, the VR provides an output by summing the VID from the CPU SetVID command and VID offset from VOUT_OFFSET (23h). One exception is when the VR receives SetVID to 0V command from the CPU. The output voltage goes to 0V, and the VID offset is ineffective.

   VOUT_OFFSET (23h) provides -128 ~ +127 VID steps offset setting. In the 5mV VID table, the max offset is 0.635V, and the max V_{OUT} is 2.155V. In the 10mV VID table, the max offset is 1.27V, and the max V_{OUT} is 3V.

   Tracking mode is effective in SVID, PMBus, PVID, and AVSBus modes. To enable over-clocking tracking mode, set MFR_VR_CONFIG (E4h) bit[10] = 1.

2. Fix Mode: Fixed voltage margining is used in extreme over-clocking applications where the fixed voltage can provide additional stability. In this mode, a fixed voltage is commanded with the PMBus command VOUT_COMMAND (21h). The VR output voltage is fixed at this voltage regardless of the VID changing command from the CPU. When the CPU issues a SetVID command, the VR will ACK the command and asserts ALERT# immediately but keeps the voltage commanded by VOUT_COMMAND (21h). Meanwhile, the VR output voltage remains at the fixed VID.

   Fix mode is only available in SVID override mode. To enable over-clocking fixed mode, set MFR_VR_CONFIG (E4h) bit[3] = 1. In the 5mV VID table, the max V_{OUT} is 2.72V with the VID table extending. In the 10mV VID table, the max V_{OUT} is 3V.

AVSBus Mode

The MP2965 supports the AVSBUS control mode.

In AVSBus mode, the communication signals AVS_CLK and AVS_MOSI are mux from the SCLK and SDIO as input pins. The AVS_MISO pin must be configured according to the electrical voltage level of the AVSBus supply. For a ≤1.8V AVSBus supply application, the AVS_MISO pin is mux from ALT#. For a 1.8V ~ 3.3V AVSBus supply application, AVS_MISO is mux from VRHOT# as AVS_MISO_HV. The AVS_MISO and AVS_MISO_HV pins are open drain and require a pull-up resistor to the system AVSBus supply.

The MP2965 supports the following AVSBus protocol specified commands:

- Voltage read/write
- V_{OUT} transition rate read/write
- Current read
- Temperature read
- Voltage reset
- Power mode read/write
- AVSBus status read/write
- AVSBus version read

The MP2965 also supports a slave interrupt function.

In AVSBus mode, the SVID communication is disabled. The AVSBus address setting is the same as the SVID address with the register MFR_ADDR_SVID_AVSBUS (E6h, Page 0). Refer to the Page 0 Register Map section on page 106 for more details.

PMBUS COMMANDS FOR RAIL 1/2

Command Code	Command Name	Access	Byte	Page 0	Page 1	PMBus W/R PRT?
00h	PAGE	r/w	1	✓	✓	N
01h	OPERATION	r/w	1	✓	✓	Y
03h	CLEAR_FAULTS	send	0	✓	✓	N
04h	MFR_LINE_FLOAT_EN	r/w	1		✓	Y
05h	BIOS_UPDATE	r/w	0	✓	✓	N
09h	MFR_VR_CONFIG2	r/w	2	✓	✓	Y
0Dh	MFR_VID_SLEW_SLOW	r/w	1	✓	✓	Y
0Eh	MFR_VID_SLEW_FAST	r/w	2	✓	✓	Y
0Fh	DRMOS_CS_GAIN	r/w	2	✓		Y
10h	EEPROM_WRITE_PROTECT	r/w	1	✓		Y
15h	STORE_USER_ALL	send	0	✓	✓	Y
16h	RESTORE_USER_ALL	send	0	✓	✓	N
19h	PMBUS_CAPABILITY	r	1	✓		N
1Dh	MFR_EEPROM_CTRL	r/w	1	✓		Y
1Eh	MFR_PWM_TIME_LIMIT	r/w	2	✓	✓	Y
1Fh	MFR_VR_CONFIG4	r/w	2	✓	✓	Y
20h	PMBUS_VOUT_MODE	r	1	✓		N
21h	VOUT_COMMAND	r/w	2	✓	✓	N
22h	VOUT_TRIM	r/w	2	✓	✓	N
23h	VOUT_OFFSET	r/w	2	✓	✓	N
24h	VOUT_MAX	r/w	2	✓	✓	Y
27h	VOUT_TRANSITION_RATE	r/w	2	✓	✓	Y
29h	VOUT_SENSE_SET	r/w	2	✓	✓	Y
2Bh	VOUT_MIN	r/w	2	✓	✓	Y
2Ch	MFR_SLOPE_ADV_CTRL	r/w	2	✓	✓	Y
2Eh	MFR_VR_PROTECT_SET	r/w	2	✓	✓	Y
35h	VIN_ON	r/w	2	✓		Y
36h	VIN_OFF	r/w	2	✓		Y
38h	IOUT_CAL_GAIN_PMBUS	r/w	2	✓	✓	Y
39h	IOUT_CAL_OFFSET_PMBUS	r/w	2	✓	✓	Y
3Ah	MFR_AVSBUS_CONFIG	r/w	2	✓		Y
43h	VOUT_UV_WARN_LIMIT	r/w	2	✓	✓	Y
44h	MFR_VR_CONFIG3	r/w	2	✓	✓	Y
45h	MFR_APS_FS_CTRL	r/w	2	✓	✓	Y
46h	MFR_FS_LIMIT_12P	r/w	2	✓		Y
47h	MFR_FS_LIMIT_34P	r/w	2	✓		Y
48h	MFR_FS_LIMIT_56P	r/w	2	✓		Y
49h	MFR_FS_LIMIT_7P	r/w	1	✓		Y
4Ah	IOUT_OC_WARN_LIMIT	r/w	2	✓	✓	Y
4Dh	MFR_IMON_DGTL_GAIN	r/w	2	✓	✓	Y

PMBUS COMMANDS FOR RAIL 1/2 *(continued)*

Command Code	Command Name	Access	Byte	Page 0	Page 1	PMBus W/R PRT?
4Eh	MFR_IDROOP_CTRL	r/w	2	✓	✓	Y
51h	OT_WARN_LIMIT	r/w	1	✓		Y
55h	VIN_OV_FAULT_LIMIT	r/w	2	✓		Y
58h	VIN_UV_WARN_LIMIT	r/w	2	✓		Y
5Dh	MFR_PGOOD_SET	r/w	2	✓	✓	Y
5Eh	POWER_GOOD_ON	r/w	2	✓	✓	Y
5Fh	POWER_GOOD_OFF	r/w	2	✓	✓	Y
60h	TON_DELAY	r/w	2	✓	✓	Y
64h	TOFF_DELAY	r/w	2	✓	✓	Y
6Ah	POUT_OP_WARN_LIMIT	r/w	2	✓	✓	Y
74h	READ_CS12	r	2	✓		N
75h	READ _CS34	r	2	✓		N
	READ_CS67				✓	N
76h	READ _CS56	r	2	✓		N
	READ_CS5				✓	N
77h	READ _CS7	r	2	✓		N
78h	STATUS_BYTE	r	1	✓	✓	N
79h	STATUS_WORD	r	2	✓	✓	N
7Ah	STATUS_VOUT	r	1	✓	✓	N
7Bh	STATUS_IOUT	r	1	✓	✓	N
7Ch	STATUS_ INPUT	r	1	✓		N
7Dh	STATUS_ TEMPERATURE	r	1	✓		N
7Eh	STATUS_ CML	r	1	✓	✓	N
88h	READ_VIN	r	2	✓		N
89h	READ_IIN	r	2	✓		N
8Bh	READ_VOUT	r	2	✓	✓	N
8Ch	READ_IOUT	r	2	✓	✓	N
8Dh	READ_TEMPERATURE	r	2	✓		N
96h	READ_POUT	r	2	✓	✓	N
97h	READ_PIN	r	2	✓		N
A5h	MFR_CS_OFFSET1	r/w	2	✓		Y
A6h	MFR_CS_OFFSET2	r/w	2	✓		Y
A7h	IOUT_RPT_GAIN_HC	r/w	2	✓		Y
	MFR_PWD_USER				✓	Y
A8h	IOUT_RPT_GAIN_SVID_AVS	r/w	2	✓	✓	Y
A9h	IOUT_RPT_OFFSET_SVID_AVS	r/w	2	✓	✓	Y
ACh	MFR_PWM_STATE_ADV	r/w	1	✓		Y

PMBUS COMMANDS FOR RAIL 1/2 *(continued)*

Command Code	Command Name	Access	Byte	Page 0	Page 1	PMBus W/R PRT?
B0h	MFR_DROOP_CMPN1	r/w	2	✓	✓	Y
B2h	MFR_DROOP_CMPN2	r/w	2	✓	✓	Y
BDh	MFR_ICC_MAX	r/w	2	✓	✓	Y
BEh	MFR_PIN_MAX	r/w	2	✓		Y
	MFR_PIN_SET				✓	Y
BFh	SVID_VENDOR_PRODUCT_ID	r/w	2	✓		N
C0h	CONFIG_ID	r/w	2	✓		N
C1h	SVID_LOT_CODE_PROTOCOL_ID	r/w	2	✓	✓	N
C2h	SVID_CAPABILITY_DC_LL	r/w	2	✓	✓	N
C3h	SVID_SR_FAST_SR_SLOW	r/w	2	✓	✓	N
C4h	SVID_VR_TVRRDY_TOLERANCE1	r/w	2	✓		N
	SVID_VR_CONFIG_TOLERANCE2				✓	N
C5h	MFR_APS_LEVEL_1P	r/w	2	✓		Y
	MFR_APS_LEVEL_45P				✓	Y
C6h	MFR_APS_LEVEL_23P	r/w	2	✓		Y
	MFR_APS_LEVEL_6P				✓	Y
C7h	MFR_APS_SET	r/w	2	✓	✓	Y
C9h	MFR_IDROOP_OFFSET	r/w	1	✓	✓	Y
CBh	MFR_DC_LOOP_CTRL	r/w	2	✓	✓	Y
CCh	MFR_APS_CTRL	r/w	2	✓	✓	Y
CDh	MFR_OSR_SET	r/w	2	✓	✓	Y
CEh	MFR_BLANK_TIME	r/w	2	✓	✓	Y
CFh	MFR_DDR_SET	r/w	1	✓		Y
D4h	MFR_SLOPE_SR_4P	r/w	2	✓		Y
D5h	MFR_SLOPE_CNT_4P	r/w	2	✓		Y
D6h	MFR_SLOPE_SR_3P	r/w	2	✓		Y
	MFR_SLOPE_SR_5P				✓	Y
D7h	MFR_SLOPE_CNT_3P	r/w	2	✓		Y
	MFR_SLOPE_CNT_5P				✓	Y
D8h	MFR_SLOPE_SR_2P	r/w	2	✓		Y
	MFR_SLOPE_SR_6P				✓	Y
D9h	MFR_SLOPE_CNT_2P	r/w	2	✓		Y
	MFR_SLOPE_CNT_6P				✓	Y
DAh	MFR_SLOPE_SR_1P	r/w	2	✓		Y
	MFR_SLOPE_SR_7P				✓	Y
DBh	MFR_SLOPE_CNT_1P	r/w	2	✓		Y
	MFR_SLOPE_CNT_7P				✓	Y
DCh	MFR_SLOPE_SR_DCM	r/w	2	✓	✓	Y
DDh	MFR_SLOPE_CNT_DCM	r/w	2	✓	✓	Y

PMBUS COMMANDS FOR RAIL 1/2 *(continued)*

Command Code	Command Name	Access	Byte	Page 0	Page 1	PMBus W/R PRT?
DEh	MFR_SLOPE_TRIM1	r/w	2	✓	✓	Y
DFh	MFR_SLOPE_TRIM2	r/w	2	✓	✓	Y
E0h	MFR_SLOPE_TRIM3	r/w	2	✓		Y
E1h	MFR_ADDR_PMBUS	r/w	2	✓		Y
E2h	MFR_LOOP_PI_SET	r/w	2	✓	✓	Y
E3h	MFR_CB_LOOP_CTRL	r/w	1	✓	✓	Y
E4h	MFR_VR_CONFIG	r/w	2	✓	✓	Y
E5h	MFR_VBOOT_SET	r/w	2	✓	✓	Y
E6h	MFR_ADDR_SVID_AVSBUS	r/w	2	✓		Y
E7h	MFR_IIN_CAL_GAIN	r/w	2	✓		Y
	MFR_IIN_CAL_OFFSET				✓	Y
E8h	MFR_TEMP_CAL	r/w	2	✓		Y
E9h	MFR_CUR_GAIN	r/w	2	✓	✓	Y
EBh	MFR_FS_LOOP_CTRL	r/w	2	✓	✓	Y
ECh	MFR_FS	r/w	2	✓	✓	Y
EDh	MFR_OTP_SET	r/w	2	✓		Y
EEh	MFR_OCP_TOTAL_SET	r/w	2	✓	✓	Y
EFh	MFR_VCCIO_FAULT_SET	r/w	2	✓		Y
F0h	MFR_OCP_PHASE_SET	r/w	1	✓	✓	Y
F1h	MFR_OVP_UVP_SET	r/w	2	✓	✓	Y
F2h	PWD_CHECK_CMD	send	2	✓		N
FCh	MFR_FAULTS1	r	2	✓		N
FDh	MFR_FAULTS2	r	2	✓		N
FEh	MFR_FAULTS3	r	2	✓		N
FFh	CLEAR_EEPROM_FAULTS	send	0	✓		N

PMBUS COMMANDS FOR EERPOM (PAGE 29)

Command Code	Command Name	Access	Bytes	Page 29	PMBus W/R PRT?
81h	PVID_VID1_VBOOT1	rom	2	✓	Y
82h	PVID_VID2_VBOOT2	rom	2	✓	Y
83h	PVID_VID3_VBOOT3	rom	2	✓	Y
84h	PVID_VID4_VBOOT4	rom	2	✓	Y
85h	PVID_VID5_VBOOT5	rom	2	✓	Y
86h	PVID_VID6_VBOOT6	rom	2	✓	Y
87h	PVID_VID7_VBOOT7	rom	2	✓	Y
88h	PVID_VID8_VBOOT8	rom	2	✓	Y
F9h	PRODUCT_REV_USER	rom	2	✓	Y
FCh	MFR_STORE_FAULTS1	rom	2	✓	Y
FDh	MFR_STORE_FAULTS2	rom	2	✓	Y
FEh	MFR_STORE_FAULTS3	rom	2	✓	Y

PAGE 0 REGISTER MAP

PAGE (00h) *(Page 0)*

The PAGE command provides the ability to configure, control, and monitor all registers, including test mode and the EEPROM, through only one physical address.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	PAGE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	PAGE	Registers page selector. 0x00: Page 0, all PMBus commands address operating registers on Page 0 0x01: Page 1, all PMBus commands address operating registers on Page 1 0x02: Page 2, all PMBus commands address the test mode registers 0x28: Page 28, all PMBus commands address the EEPROM registers (00h~FFh) 0x29: Page 29, all PMBus commands address the EEPROM registers (100h~1FFh) others: ineffective Note: MFR_EEPROM_CTRL (06h) bit[2] (EE_WORD_WR_EN) determines if Page 28/29 is accessible or not. EE_WORD_WR_EN = 0: Page 28/29 is not accessible EE_WORD_WR_EN = 1: Page 28/29 is accessible

OPERATION (01h) *(Page 0)*

The OPERATION command on Page 0 is used to turn the Rail 1 output on/off in conjunction with the input from EN1. It also provides two bits to select PMBus override or AVSBus override mode and one bit to enable VOUT_COMMAND (21h), even in AVSBus override mode.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function					x	x		x

Bits	Bit Name	Description
7:6	OPERATION_MODE	Operation mode. 2'b00: Hi-Z off 2'b01: soft off 2'b1x: on
5:4	AVSBUS_EN	Selects the VID override mode between PMBus and AVSBus mode. 2'b00: disable AVSBus override mode 2'b11: enable AVSBus override mode Others: reserved
3:2, 0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	AVS_PMBUS_CTRL	Enables VOUT_COMMAND (21h) to control the VID at AVSBus mode. 1'b0: VID is controlled by AVSBus interface 1'b1: VID is controlled by PMBus command VOUT_COMMAND

CLEAR_FAULTS (03h) *(Page 0)*

The CLEAR_FAULTS command is used to clear any fault bit in all statuses and fault registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), STATUS_CML (7Eh), MFR_FAULTS1 (FCh), MFR_FAULTS2 (FDh), and MFR_FAULTS1 (FEh).

This command is write only. There is no data byte for this command.

BIOS UPDATE (05h) *(Page 0)*

The BIOS_UPDATE command is used to update the phase number and MFR_FS (ECh) value while the VR is outputting power. When the bios updates, the VR is commanded to calculate the on time with Equation (1) immediately.

This command is write only. There is no data byte for this command.

MFR_VR_CONFIG2 (09h) *(Page 0)*

The MFR_VR_CONFIG2 command on Page 0 sets the Rail 1 VBOOT-related options, PVID and PMBus override mode, and Hi-Z shutdown voltage level. The Hi-Z shutdown voltage level is effective only when VID slews down to 0V. VID slewing down to 0V may be caused by a soft off or DVID to 0V. Once the VID-DAC output is lower than the Hi-Z shutdown voltage level, the PWM enters tri-state. The output voltage is discharged by the load current naturally (see Figure 27).

Command	MFR_VR_CONFIG2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x						VID_SHUT_DOWN								

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates writes are ignored and reads are always 0.
13	PIN_VBOOT_MUX	Selects the boot-up voltage from pin 25 (BOOT) when the pin boot mode is enabled. 1'b0: unsupported 1'b1: pin boot voltage is from pin 25 (BOOT)
12	RESERVED	Always set this bit to 0.
11	BOOT_MODE_SEL	Selects the boot-up voltage from the register or pin. 1'b0: VBOOT is set by the register MFR_VBOOT (E5h) 1'b1: PMBus VBOOT is from the pin (BOOT). BOOT is assigned by bit[13] in this command.
10	PVID_EN	Enables Rail 1 PVID mode. 1'b0: disable PVID mode 1'b1: enable PVID mode
9	PMBUS_EN	Enables PMBus override mode. 1'b0: disable PMBus override mode 1'b1: enable PMBus override mode
8:0	VID_SHUT_DOWN	VID threshold at which all PWMs go into tri-state when the VID slews to 0V. This bit is in direct format with VID resolution. 1 VID step/LSB.

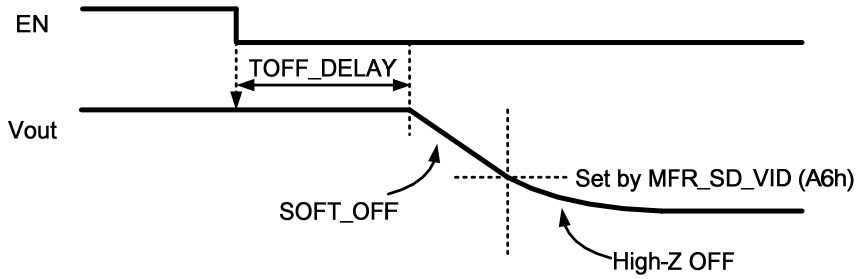


Figure 27: EN Soft-Off to High-Z Off Level

MFR_VID_SLEW_SLOW (0Dh) *(Page 0)*

THE MFR_VID_SLEW_SLOW COMMAND ON Page 0 SELECTS THE Rail 1 VID TRANSITION SLOW SLEW RATE. This command IS PROPORTIONAL WITH the VID FAST SLEW RATE, WHICH IS SET WITH COMMAND MFR_VID_SLEW_FAST (0EH). THE VID SLOW SLEW RATE DEFINES THE VID SLEW RATE during BOOT_UP, OPERATION COMMAND SOFT_OFF, AND SVID INTERFACE SET VID SLOW COMMAND.

Command	MFR_VID_SLEW_SLOW							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x			SLEW_SLOW_SR			

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5	VR13_HC_SUPPORT	1’b0: VR13.HC mode not supported 1’b1: VR13.HC mode supported
4	VR13_HC_ACTIVE_INI	Enable VR13.HC initially. The CPU can enable or disable VR13.HC mode with SVID command SLOW SLEW SELECTOR (2Ah). Per VR13.HC spec, the default is to disable it, initially. 1’b0: disable VR13.HC initially 1’b1: enable VR13.HC initially, the parameters setting for VR13.HC is effective and is returned to the SVID interface
3:0	SLEW_SLOW_SR	4’b1xxx: SLEW_SLOW_SR = FAST_SR/16 4’b01xx: SLEW_SLOW_SR = FAST_SR/8 4’b001x and 4’b0000: SLEW_SLOW_SR = FAST_SR/4 4’b0001: SLEW_SLOW_SR = FAST_SR/2 Where FAST_SR is the VID fast slew rate defined in register MFR_VID_SLEW_FAST (0Eh) bit [5:0]. The value of “x” does not matter.

MFR_VID_SLEW_FAST (0Eh) *(Page 0)*

The MFR_VID_SLEW_FAST command on Page 0 sets the VID fast slew rate and extra VID steps when VID is ramping up. The fast slew rate defines the SVID interface, Set VID fast slew rate, and EN soft-off fast slew rate.

Command	MFR_VID_SLEW_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x			SLEW_FAST_CNT					

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:6	VID_PLUS_STEP	Sets the count of extra VID steps when DVID is up. The extra VID steps are used to compensate for the droop voltage caused by the charging output capacitor during DVID up. This bit is only effective after the boot-up voltage is settled. 1 VID step/LSB.
5:0	SLEW_FAST_CNT	Sets the VID fast slew rate by setting the time interval of each VID step. It is in direct format. 50ns/LSB. The slew rate can be calculated with the equation below: $FAST\_SR(mV/\mu s) = \frac{VID\_STEP(mV)}{SLEW\_FAST\_CNT \times 0.05(\mu s)}$ Where VID_STEP is 5mV or 10mV determined by bit[8] of MFR_VR_CONFIG (E4h).

DRMOS_CS_GAIN (0Fh) *(Page 0)*

The DRMOS_CS_GAIN command inputs the typical current sensing gain of the Intelli-Phase for both Rail 1 and Rail 2.

Command	DRMOS_CS_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	DRMOS_CS_GAIN_R2				DRMOS_CS_GAIN_R1			

Bits	Bit Name	Description
15:8	RESERVED	Unused.
7:4	DRMOS_CS_GAIN_R2	Sets the Intelli-Phase current sensing gain for Rail 2. 4'b0000: 8.5μA/A 4'b0001: 9.7μA/A 4'b0010: 10μA/A 4'b0011: 5μA/A Others: TBD
3:0	DRMOS_CS_GAIN_R1	Sets the Intelli-Phase current sensing gain for Rail 1. 4'b0000: 8.5μA/A 4'b0001: 9.7μA/A 4'b0010: 10μA/A 4'b0011: 5μA/A Others: TBD

EEPROM_WRITE_PROTECT (10h) *(Page 0)*

The EEPROM_WRITE_PROTECT command is used to enable EEPROM write protection.

Command	EEPROM_WRITE_PROTECT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EEPROM_WP							

Bits	Bit Name	Description
7:0	EEPROM_WP	Enables EEPROM write protection. 0x63: disable EEPROM write protection Others: enable EEPROM write protection

STORE_USER_ALL (15h) *(Page 0)*

The STORE_USER_ALL command instructs the PMBus device to copy the Page 0 and Page 1 contents of the operating memory to the matching locations in the EEPROM. During the copying process, the device calculates the CRC for all saved bits and saves the CRC result into the EEPROM. The CRC code is used to check if the data is valid or not at the next power-up or restore.

This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h) *(Page 0)*

The RESTORE_USER_ALL command instructs the PMBus device to copy the Page 0 and Page 1 contents from the EEPROM and overwrite the matching locations in the operating memory. In this process, the device calculates the CRC for all restored bits. If the calculated CRC is not matching with the CRC value saved in the EEPROM, the device reports the CRC error via bit[4] of register STATUS_CML (7Eh). The CRC error protection can be enabled by bit[0] of MFR_EEPROM_CTRL (1Dh).

After the power-on reset (POR), the device triggers the memory copy operation from the EEPROM. This process is the same as the operating RESTORE_USER_ALL command.

It is *not* permitted to send the RESTORE_USER_ALL command while the device is outputting power; otherwise, the command will be ignored.

This command is write only. There is no data byte for this command.

PMBUS_CAPABILITY (19h) *(Page 0)*

The PMBUS_CAPABILITY command on Page 0 provides one byte to return the key features that the MP2965 can support.

Command	PMBUS_CAPABILITY							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	1	1	0	1	0	1	0	0

Bits	Bit Name	Description
7	PACKET_ERROR_ CHECKING	Always returns 1’b1: packet error checking supported.
6:5	MAXIMUM_BUS_ SPEED	Always returns 2’b10: PMBus/I2C maximum bus speed is 1MHz.
4	SMBALERT#	Always returns 1’b1: the MP2965 has an ALT_P# pin and supports the SMBus alert response protocol.
3	NUMERIC_FORMAT	Always returns 1’b0: numeric data format is in LINEAR 11, ULNEAR 16, SLINEAR 16, and DIRECT format.
2	AVSBUS_SUPPORT	Always returns 1’b1: AVSBus supported.
1:0	RESERVED	Reserved. Always returns 2’b00.

MFR_EEPROM_CTRL (1Dh) *(Page 0)*

The MFR_EEPROM_CTRL is used to control the action of the operating memory and EEPROM.

Command	MFR_EEPROM_CTRL							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x							

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6	EE_BYTE_WR_EN	An enable bit to set the EEPROM data to be read or written via the PMBus when switching the Page to 28 or 29. 1'b1: enable EEPROM byte write or read via PMBus when turning Page to 28 or 29 1'b0: disable EEPROM byte write or read via PMBus when turning Page to 28 or 29
5	PMBUS_RW_PIN_EN	Hardware protects PMBus write and read command by configuring the voltage on ADDR_PH. 1'b0: disables hardware to protect PMBus write and read 1'b1: enables hardware to protect PMBus write and read by setting the voltage setting on ADDR_PH. Refer to Table 8 for a detailed voltage list. When PMBus write and read is protected, the registers marked with column "PMBUS W/R PRT = Y" in the PMBus Commands for Rail 1/2 table on page 47 are protected.
4	RESERVED	Reserved. This bit is always set to 0.
3	PMBUS_RW_PWD_EN	Software protects the PMBus write and read command by setting a password. The MP2965 provides a password to protect the registers from both reading and writing. If the password input is incorrect, users cannot read or write the PMBus registers marked with column "PMBUS W/R PRT = Y" in the PMBus Commands for Rail 1/2 table on page 47. 1'b0: disable password to protect the register from reading and writing 1'b1: enable password to protect the register from reading and writing
2	OPERATION_ALL_ CALL_EN	Enables the OPERATION command (01h) addresses on both rails regardless of the value of the PAGE (00h) command to control the power-up sequence of both Rail 1 and Rail 2. 1'b0: OPERATION command (01h) only addresses an associated single rail 1'b1: OPERATION command (01h) addresses both rails
1	FLT_SAVE_EEPROM_ EN	Enables auto-saving fault status into the EEPROM. 1'b0: disable fault status auto-saving into EEPROM 1'b1: enable fault status auto-saving into EEPROM
0	CRC_PROTECT_EN	Enables CRC fault protection. 1'b0: EEPROM CRC fault will not stop the output power 1'b1: EEPROM CRC fault stops the output power. The device then enters shutdown mode. In the process of storing memory data to the EEPROM, the device calculates the CRC for all saved bits and saves the CRC result in the EEPROM. In the process of restoring the EEPROM data to the memory, the device calculates the CRC for all restored bits. At the end of the restore process, the device checks the CRC results saved in the EEPROM with the calculated CRC. If they are not matched, the device reports the CRC fault and sets bit[4] of STATUS_CML (7Eh).

MFR_PWM_TIME_LIMIT (1Eh) *(Page 0)*

This MFR_PWM_TIME_LIMIT command on Page 0 sets the PWM minimum on-time and minimum off-time for Rail 1.

Command	MFR_PWM_TIME_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	TON_LIMIT_TO_VCAL				MIN_ON_TIME			MIN_OFF_TIME				

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	TON_LIMIT_TO_VCAL	Sets the T_{ON} limit below which the DC loop regulation will never be held. In the MP2965, the DC loop can be held if the PWM period meets the condition set in MFR_DC_LOOP_CTRL (CBh) bit[13:7]. However, if the calculated PWM on time from Equation (1) is less than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation. 5ns/LSB.
7:5	MIN_ON_TIME	Sets the PWM minimum on-time. 5ns/LSB.
4:0	MIN_OFF_TIME	Sets PWM minimum off-time with 15ns offset. 20ns/LSB. The minimum off-time of Rail 1 can be calculated with: $PWM\_MIN\_OFF\_TIME(ns) = MIN\_OFF\_TIME \times 20(ns) + 15(ns)$

MFR_VR_CONFIG4 (1Fh) *(Page 0)*

The MFR_VR_CONFIG4 command on Page 0 sets some basic configurations for Rail 1.

Command	MFR_VR_CONFIG4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function		PMBUS_TIMEOUT														

Bits	Bit Name	Description
15	VID_>2LSB_ALT_MODE	Selects the SVID ALT# behavior when the DVID step is greater than two. This bit is only effective when the VID resolution is 5mV/step. 1'b0: ALT# asserts after VR_SETTLE 1'b1: ALT# asserts two VID steps before VR_SETTLE
14:11	PMBUS_TIMEOUT	Sets the PMBus timeout time with the following equation: $PMBUS\_TIMEOUT \times 1.6ms + 1.5ms$ If SCL_P is low for longer than PMBUS_TIMEOUT, the controller resets the PMBus communication and stays idle.
10	VDIFF_SCP_EN	Enables VDIFF short to GND protection. 1'b0: disable VDIFF SCP 1'b1: enable VDIFF SCP
9:7	VDIFF_SC_BLANK_TIME	Sets the blanking time of VDIFF short to GND protection. When VDIFF shorts to GND for longer than the blanking time, the controller shuts down the associated rail accordingly. 400ns/LSB with +200ns offset.
6	OCP_PHASE_SS_EN	Enables OCP phase during the soft-start process. Active on both Rail 1 and Rail 2. 1'b0: disable OCP phase during soft-start process 1'b1: enable OCP phase during soft-start process

5:4	OCP_PHASE_PWM_ BLANK_TIME	Sets the PWM-set signal blanking time when the OCP_Phase limit is tripped. If the phase current remains higher than OCP_Phase after the PWM-set blanking time, the present phase is skipped, and the next phase is turned on. The time setting is active for both rails. 20ns/LSB with 15ns offset. BLANK_TIME= 20ns/LSB × OCP_PHASE_SET +15ns
3	IOUT_DGTL_FLT_EN	Enables the IMON 2-point digital filter internal IC. 1'b0: enable the IMON 2-point digital filter 1'b1: disable the IMON 2-point digital filter
2	OVP/OCP_PHASE/ COMP_DAC_DBG	Enable V_{OUT} OVP/OCP_Phase/COMP DAC debug mode. Once in enable debug mode, the OVP threshold, OCP_Phase limit, and VCOMP DAC input can be set with specific registers. The associated register setting on Page 0 is not effective anymore. This bit is for ATE trimming. 1'b0: normal mode 1'b1: enable V_{OUT} OVP/OCP_Phase/COMP DAC debug mode. The OCP_Phase limit is directly from register F0h bit[7:0] on Page 0 with 10mV/LSB. The V_{OUT} OV threshold is directly from register 24h bit[8:0] on Page 0 with 10mV/LSB. V_{COMP} is directly from register 6Ch bit[7:0] on Page 2 with 1.37mV/LSB.
1:0	DECAY_LENGTH	Sets the minimum time of each VID step in decay mode. It is used to set the maximum decay slew rate. VID is forced to ramp down one VID step once the present VID step is longer than the time set by DECAY_LENGTH. 100ns/LSB.

PMBUS_VOUT_MODE (20H) (PAGE 0)

The PMBUS_VOUT_MODE command on Page 0 provides one byte to return V_{OUT}.

Command	PMBUS_VOUT_MODE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	0	0	1	0	0	0	0	1

Bits	Bit Name	Description
7:5	DEVICE_VOUT_MODE	Always returns 3'b001: VOUT is in VID mode
4:0	VID_CODE_TYPE	Always returns 5'b00001: indicates that the VID code is for Intel CPU

VOUT_COMMAND (21h) *(Page 0)*

The VOUT_COMMAND command on Page 0 sets the reference voltage VID at PMBus override mode and sets the over-clocking fixed mode at AVSBus and SVID override mode.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	VOUT_COMMAND								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_COMMAND	Sets the reference voltage VID at PMBus override mode. It is in Intel VID format with 5mV or 10mV per step. The VID resolution is determined by bit[8] of MFR_VR_CONFIG (E4h). 1 VID step/LSB.

VOUT_TRIM (22h) (Page 0)

The VOUT_TRIM command on Page 0 instructs the device to fine-tune the Rail 1 output voltage. The VOUT_TRIM is added to the remote sense amplifier output to change the final output voltage. Note that the output PMBus-reported value in READ_VOUT (8Bh) is not affected by VOUT_TRIM. VOUT_TRIM can be used to fine-tune the output voltage.

Command	VOUT_TRIM															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	VOUT_TRIM						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	VOUT_TRIM	Fine-tune the output voltage. This bit is in direct two's complement format. The resolution is related with the VDIFF gain set by VOUT_SENSE_SET (29h, bit[11]). 0.5mV/LSB with VDIFF unit gain 0.8mV/LSB with VDIFF half gain The table below shows the binary data and real-world value.

VOUT_TRIM	VDIFF Unit Gain	VIDFF Half Gain
7'b 000 0000	0	0
7'b 000 0001	+0.5mV	+0.8mV
7'b 011 1111	+31.5mV	+50.4mV
7'b 100 0000	-32mV	-51.2mV
7'b 100 0001	-31.5mV	-50.4mV
7'b 111 1111	-0.5mV	-0.8mV

VOUT_OFFSET (23h) *(Page 0)*

The VOUT_OFFSET command on Page 0 instructs the device to add an offset over the VID from the SVID, AVSBus, or PMBus interface and affects the final reference voltage. The data is in a direct format. It is also referred to as over-clocking tracking mode.

Command	VOUT_OFFSET															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	VOUT_OFFSET							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_OFFSET	Add an offset over the VID from the SVID, AVSBus, or PMBus interface and affects the final reference voltage. This bit is in direct format. 1 VID step/LSB. This value is in two's complement format. Bit[7] is the sign bit. The values listed below shows the binary data and real-world value. 8'b 0000 0000: 0 8'b 0000 0001: +1 VID step 8'b 0111 1111: +127 VID steps 8'b 1000 0000: -128 VID steps 8'b 1000 0001: -127 VID steps 8'b 1111 1111: -1 VID step

VOUT_MAX (24h) *(Page 0)*

The VOUT_MAX command on Page 0 sets the maximum reference voltage of the Rail 1 VID-DAC to set the maximum output voltage. When an external resistor divider is applied, the maximum voltage is clamped to VOUT_MAX/K_R. K_R is the dividing ratio of the resistor divider.

Command	VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	X	x	x	VOUT_MAX								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MAX	Sets the maximum reference voltage of the VID-DAC in VID format. 1 VID step/LSB.

VOUT_TRANSITION_RATE (27h) *(Page 0)*

The VOUT_TRANSITION_RATE command on Page 0 sets the Rail 1 dynamic VID transition slew rate at PMBus and PVID VID override mode and sets the AVSBus initial DVID slow rate. This command also sets the soft-off slew rate when selected by register MFR_VR_CONFIG3 (44h) bit[5:4]. This command is only effective after the soft start-up ends.

Command	VOUT_TRANSITION_RATE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	X	x	x	VOUT_TRANS_CNT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRANS_CNT	Sets the Rail 1 dynamic VID transition slew rate at AVSBus and PMBus VID override mode. 100ns/LSB. The PMBus, PVID DVID, and EN soft-off slew rate can be calculated with: $DVID\_SR(mV/\mu s) = \frac{VID\_STEP(mV)}{VOUT\_TRANS\_CNT \times 0.1(\mu s)}$ The AVSBus initial DVID slew rate and also the maximum DVID slew rate that the VR can handle can be calculated with: $DVID\_SR\_INI(mV/\mu s) = \frac{10(mV)}{VOUT\_TRANS\_CNT \times 0.1(\mu s)}$ Where VID_STEP is 5mV or 10mV (determined by the VID resolution determined by bit[8] of MFR_VR_CONFIG (E4h)), and VOUT_TRANS_CNT is the decimal value defined in VOUT_ TRANSITION_RATE (27h).

VOUT_SENSE_SET (29h) *(Page 0)*

The VOUT_SENSE_SET command on Page 0 sets the V_{OUT} sense-related options. This command is for Rail 1 only.

Command	VOUT_SENSE_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x				VOUT_SCALE									

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	DC_LOOP_SNS_SEL	Sets the sensing point of V_{OUT} DC loop calibration. 1'b0: VFB pin 1'b1: VDIFF pin
11	VDIFF_GAIN_SEL	Selects the gain of the remote sense amplifier. 1'b0: unity gain. VOUT is limited to 2.0V. 1'b1: half gain
10:9	VDIFF_VFB_ADC_GAIN	ADC sensing gain selector of VDIFF and VFB. 2'b00: half gain 2'b01: unity gain 2'b10 and 2'b11: three-quarter gain Set the ADC sense gain to 2'b01 when the remote sense amplifier gain is set to half gain, or the device works erroneously.
8:0	VOUT_SCALE	Sets the Rail 1 VREF-to-VOUT dividing ratio when an external resistor divider is used. VREF ranges from 0.25 - 2V. Equation (15) shows the calculation of VOUT_SCALE.

When V_{OUT} is larger than 3V, the output voltage must be divided to the reference voltage within 0.25 - 2V. The MP2956 provides two methods of output voltage sensing: remote sense and local sense. Remote sense provides better load regulation. Figure 28 shows the typical connections when V_{OUT} is larger than 3V and a remote sense is applied.

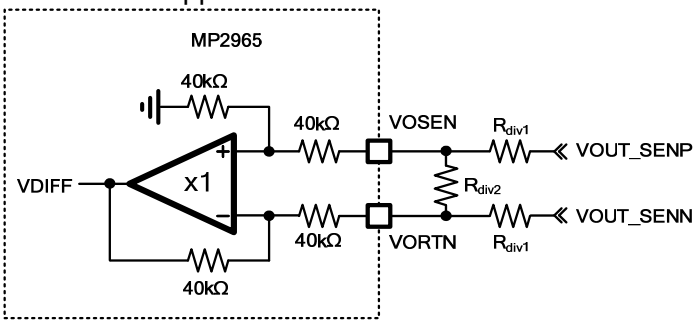


Figure 28: Output Divider Connections with Remote Sense

VOUT_SENP and VOUT_SENN are from the load and must be routed as a differential pair on quiet areas. Calculate the voltage divider ratio in Figure 28 using Equation (13):

$$K_{R\_RS} = \frac{V_{REF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{div1}} + \frac{2}{R_{div2}} + \frac{1}{40K}) \times R_{div1}} \quad (13)$$

To prevent the output voltage from being out of regulation, ensure that the voltage on VOSEN is lower than the maximum allowed sensing voltage (VDD33 - 0.3V) at any time.

For output voltage designs above the VOSEN pin specification, connect the output divider as shown in Figure 29. VORTN is connected to AGND directly to disable the remote sense.

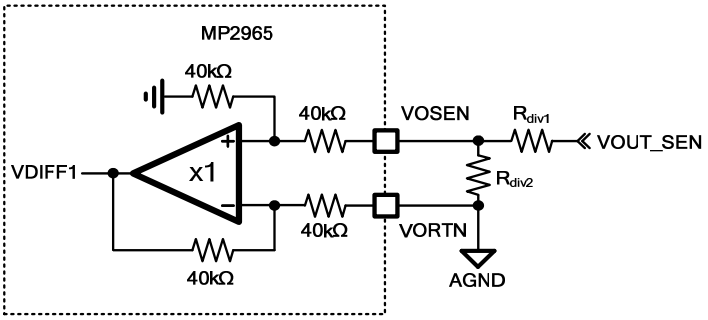


Figure 29: Output Divider Connections with Local Sense

Calculate the voltage divider ratio in Figure 29 using Equation (14):

$$K_{R\_LS} = \frac{V_{REF}}{V_{OUT}} = \frac{1}{(\frac{1}{R_{div1}} + \frac{1}{R_{div2}} + \frac{1}{80K}) \times R_{div1}} \quad (14)$$

Where K_{R_RS} and K_{R_RS} must be programmed into the MP2965 by the PMBus command VOUT_SENSE_SET (29h) bit[8:0] (i.e.: VOUT_SCALE). The calculation of VOUT_SCALE is shown in Equation (15):

$$VOUT\_SCALE = \frac{2^5}{K_R} \quad (15)$$

Where VOUT_SCALE is the programmed decimal value in register VOUT_SENSE_SET (29h), and K_R is the value of K_{R_RS} and K_{R_RS}.

The MP2965 uses VOUT_SCALE to determine the reference voltage.

The reference voltage calculation in the MP2965 is shown in Equation (16):

$$V_{REF} = \frac{2^5}{VOUT\_SCALE} \times V_{OUT} \quad (16)$$

Table 10a shows the recommended output divider resistors and PMBus register settings for typical POL output voltages. Table 10a shows the resistor values in Figure 28 when remote sense is applied. Table 10b shows the resistor values in Figure 29 when local sense is applied.

Table 10a: Recommended Output Dividers with Remote Sensing

V_{OUT} (V)	R_{div1} (kΩ)	R_{div2} (kΩ)	K_R	VOUT_SENSE_SET (29h)	V_{REF} (V)
3.3	3.01	2.05	0.25	0x0020	0.825
5	3.01	1.2	0.164	0x0015	0.82

Table 10b: Recommended Output Dividers with Local Sense

V_{OUT} (V)	R_{div1} (kΩ)	R_{div2} (kΩ)	K_R	VOUT_SENSE_SET (29h)	V_{REF} (V)
3.3	6.04	2.05	0.25	0x0020	0.825
5	6.04	1.2	0.164	0x0015	0.82

Note: NS means not stuffed.

VOUT_MIN (2Bh) *(Page 0)*

The VOUT_MIN command on Page 0 instructs the device to limit the minimum output voltage of Rail 1. When the output voltage decoded from the SVID, AVSBus, and PMBus interface is lower than what is set by VOUT_MIN (2Bh), the output voltage is clamped to VOUT_MIN.

When an external resistor divider is applied on VOSEN, the minimum output voltage is clamped to VOUT_MIN/K_R. K_R is the dividing ratio of the divider.

Command	VOUT_MIN															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	VOUT_MIN								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MIN	Sets the minimal VID of Rail 1. Any VID lower than this value is clamped to VOUT_MIN. This bit is in VID format with 5mV or 10mV per LSB.

MFR_SLOPE_ADV_CTRL (2Ch) *(Page 0)*

The MFR_SLOPE_ADV_CTRL command on Page 0 programs the slope compensation-related options.

Command	MFR_SLOPE_ADV_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x		SLOPE_INI_ISOURCE								x		

Bits	Bit Name	Description
15:12, 2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	SLOPE_INI_EN	Enables initial slope compensation before soft start. 1'b0: disable initial slope compensation 1'b1: enable initial slope compensation
10:5	SLOPE_INI_ISOURCE	Sets the current source value for initial slope compensation. The slope voltage can be calculated with the equation below: $V_{SLOPE\_INI}(mV) = 0.845 \times SLOPE\_INI\_ISOURCE$ Design the initial slope voltage to be 1.5 ~ 2 times of the full-phase nominal slope voltage. Refer to Equation (17) to calculate the full-phase slope voltage.
4	SLOPE_RST_SEL	Selects the slope compensation resetting time. 1'b0: slope compensation is reset during SLOPE_RST_TIME defined with PMBus command MFR_BLANK_TIME (CEh) bit[11:6] 1'b1: slope compensation is reset when PWM is high
3	AC_DC_DROOP_SEL	Selects DC or AC droop injection. 1'b0: select DC droop injection 1'b1: select AC droop injection
1	DVIDUP_PRE-BIAS_MODE	Sets the PWM behavior at DVID up. 1'b0: pre-bias mode, all PWM signals enter Hi-Z-to-Hi individually 1'b1: PWM1 Hi-Z-to-Hi, other PWMs pull low first and pull high when the individual set signal comes

0	DCM_EXIT_SLOPE_ CTRL	Resets the slope compensation counter when the VR exits DCM. After the counter is reset, the slope compensation starts and follows the slew rate definition of the activated power state. 1'b0: reset slope compensation counter when DCM is exited 1'b1: does not reset slope compensation counter when DCM is exited

MFR_VR_PROTECT_SET (2Eh) *(Page 0)*

The MFR_VR_PROTECT_SET command on Page 0 sets some protection-related options of the MP2965.

Command	MFR_VR_PROTECT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x				x	VIN_PRT_DIS						

Bits	Bit Name	Description
15:11, 7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	PWM_FLT_DTCT_EN	Enables the Rail 1 Intelli-Phase fault type detection with the PWM pin. This bit is only effective when the Intelli-Phase supports fault type reporting at the PWM pin. 1'b1: enable PWM pin fault-type detection 1'b0: disable PWM pin fault-type detection
9	CS_FLT_EN	Enables VR shutdown when the CS fault is detected on Rail 1. The MP2965 monitors the voltage level on CS. Once CS is lower than 200mV, the MP2965 detects that a CS fault has occurred and latches down immediately. 1'b0: disable CS fault detection 1'b1: enable CS fault detection
8	VTEMP_FLT_EN	Enables the VTEMP fault to shut down Rail 1. The MP2965 monitors the voltage level on VTEMP. Once VTEMP is higher than 1.25V, the MP2965 detects that a VTEMP fault has occurred and latches down immediately. VTEMP fault detection does not affect power stage temperature sensing done by the VTEMP pin. VTEMP fault detection does not affect over-temperature protection, either. 1'b0: disable VTEMP fault protection 1'b1: enable VTEMP fault protection
6:4	VIN_PRT_DIS	3'b110: disable VIN UVLO and OVP Others: enable VIN UVLO and OVP
3:2	OVP1_DIS	Disables the VOUT OVP1 protection for debugging purposes. It is recommended to enable OVP1 at normal mode. 2'b01: disable VOUT OVP1 protection Others: enable VOUT OVP1 protection
1:0	OTP_DIS	Disables over-temperature protection for debugging purposes. 2'b01: disable OTP Others: enable OTP

VIN_ON (35h) *(Page 0)*

The VIN_ON command is used to set the V_{IN} UVLO rising threshold.

Command	VIN_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	1	1	1	0	1	x	x	x	VIN_ON							

Bits	Bit Name	Description
15:11	EXPONENT	Fixed to 5'b11101.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VIN_ON	Set the V_{IN} UVLO rising threshold. 0.125V/LSB.

VIN_OFF (36h) *(Page 0)*

The VIN_OFF command is used to set the V_{IN} UVLO falling threshold.

Command	VIN_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	1	1	1	0	1	x	x	x	VIN_OFF							

Bits	Bit Name	Description
15:11	EXPONENT	Fixed to 5'b11101.
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VIN_OFF	Sets V_{IN} UVLO falling threshold. 0.125V/LSB.

IOUT_CAL_GAIN_PMBUS (38h) *(Page 0)*

The IOUT_CAL_GAIN_PMBUS command on Page 0 sets the gain for Rail 1 output current PMBus reporting. The MP2965 senses the output current by sensing the voltage on IMON. The reported output current is returned with the PMBus command READ_IOUT (8Ch, Page 0).

Command	IOUT_CAL_GAIN_PMBUS															
Format	Linear, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EXPONENT					MANTISSA										

Bits	Bit Name	Description
15:11	EXPONENT	This value is in two's complement format. 5'b10001: exponent = -15 5'b10010: exponent = -14 5'b10011: exponent = -13 Others: invalid

10:0	MANTISSA	Calculate the mantissa with the equation below: $MANTISSA = \frac{R_{IMON} \times K_{CS}}{16000} \times 2^{-(EXPONENT)}$ Where R_{IMON} is the resistor connected from IMON to ground (in kΩ), and K_{CS} is the current sense gain of the Intelli-Phase (in μA/A). Start the design with exponent = -15. When the mantissa > 2048 in low-current applications, increase the exponent from -15 to -13 gradually.

IOUT_CAL_OFFSET_PMBUS (39h) *(Page 0)*

The IOUT_CAL_OFFSET_PMBUS command on Page 0 sets the offset for Rail 1 output current PMBus reporting. The reported output current is returned with the PMBus command READ_IOUT (8Ch, Page 0).

Command	IOUT_CAL_OFFSET_PMBUS															
Format	Linear, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EXPONENT					x	x	x	x	MANTISSA						

Bits	Bit Name	Description
15:11	EXPONENT	Exponent for the linear format. This bit is in two's complement format. The value is fixed to: Binary: 11110 Decimal: -2 Real-world value: 0.25A
10:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	MANTISSA	The final current report offset can be calculated with: $IOUT\_REPORT\_OFFSET = MANTISSA \times 2^{EXPONENT}$ Where EXPONENT is always -2, the IOUT_REPORT_OFFSET is set with 0.25A/LSB, and MANTISSA is in two's complement format. Bit[6] is the sign bit. The mantissa list below shows the binary data and real-world I_{OUT} report offset values: 7'b 000 0000: 0 7'b 000 0001: 0.25A 7'b 011 1111: 15.75A 7'b 100 0000: -16A 7'b 100 0001: -15.75A 7'b 111 1111: -0.25A

MFR_AVSBUS_CONFIG (3Ah) *(Page 0)*

THE MFR_AVSBUS_CONFIG COMMAND ON Page 0 IS USED TO PROGRAM THE OPTIONS (PARAMETERS RELATED TO AVSBUS OVERRIDE MODE).

Command	MFR_AVSBUS_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	SETTLE_PREFIX_ MODE	Selects the behavior of issuing the Status Response Frame at the AVSBus DVID. 1'b0: slave only issues Status Response Frame when a Get Status of the corresponding rail is required 1'b1: slave also issues the Status Response Frame if VDONE flag of the status response frame is 1
8	DIS_PREFIX_MODE	Selects the behavior mode of the Status Response Frame at AVSBus mode. VID is controlled by the PMBus interface. 1'b0: Status Response Frame is issued from the VR to CPU when any of the AVSBus status bits OCW/UVW/OTW/OPW flags are changed 1'b1: Status Response Frame is not issued from the VR to CPU when any of the AVSBus status bits OCW/UVW/OTW/OPW flags are changed
7	AVSBUS_PREFIX_ MODE	Selects when the MP2965 issues a status response frame to the CPU at dynamic VID transition. This bit is only effective at AVSBus override mode. 1'b0: the MP2965 issues Status Response Frame when either VR rail is settled 1'b1: THE MP2965 issues Status Response Frame when both VR rails are settled
6	VDONE_MASK	Mask VDONE to trigger the slave to issue Status Response Frame to the CPU. 1'b0: does not mask VDONE 1'b1: mask VDONE
5	OCW_MASK	Mask the OC warning flag to trigger slave to issue the Status Response Frame to the CPU. 1'b0: does not mask OCW 1'b1: mask OCW
4	UVW_MASK	Mask the UV warning flag to trigger the slave to issue the Status Response Frame to the CPU. 1'b0: does not mask UVW 1'b1: mask UVW
3	OPW_MASK	Masks the OP warning flag to trigger the slave to issue the Status Response Frame to the CPU. 1'b0: does not mask OPW 1'b1: mask OPW
2	OTW_MASK	Mask the OT warning flag to trigger the slave to issue the Status Response Frame to the CPU. 1'b0: does not mask OTW 1'b1: mask OTW
1:0	COMM_PORTS_CFG	Selects which pins are muxed as AVSBus communication lines in AVSBus override mode. 2'b01: mux ALT# (pin 28) to AVS_MISO, mux SDIO (pin 27) to AVS_MOSI, mux SCLK (pin 26) to AVS_CLK 2'b10: mux VRHOT# (pin 33) to AVS_MISO, mux SDIO (pin 27) to AVS_MOSI, mux SCLK (pin 26) to AVS_CLK 2'b00: no pins are muxed for AVSBus Others: not supported

VOUT_UV_WARN_LIMIT (43h) *(Page 0)*

The VOUT_UV_WARN_LIMIT command on Page 0 sets the Rail 1 V_{OUT} UV warning threshold. The device sets bit[15] of STATUS_WORD (79h) and bit[5] of register STATUS_VOUT (7Ah) and asserts ALT_P# once a VOUT UV warning occurs.

Command	VOUT_UV_WARN_LIMIT															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	VOUT_UV_WARN_LIMIT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_UV_WARN_ LIMIT	Sets the VOUT UV warning threshold. This bit is in VID format with 5mV or 10mV/LSB, determined by MFR_VR_CONFIG (E4h) bit[8]. 1-VID step/LSB.

MFR_VR_CONFIG3 (44h) *(Page 0)*

The MFR_VR_CONFIG3 command on Page 0 provides two bytes to program some basic functions for Rail 1.

Command	MFR_VR_CONFIG3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X								OV/UV_VTH_SEL		

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9	OCW_PWRALT_EN	Enable bit to assert PWR_IN_ALT# when the sensed output current is higher than IOUT_OC_WARN_LIMIT. IOUT_OC_WARN_LIMIT is set with the PMBus command IOUT_OC_WARN_LIMIT (4Ah). 1'b0: does not assert PWR_IN_ALT# when IOUT exceeds the OC warning limit 1'b1: assert PWR_IN_ALERT# when IOUT exceeds the OC warning limit
8	PH1_CPL_EN	Enable couple inductor mode in 1-phase operation. This bit is for Rail 1 only. When enabled, at 1-phase mode, PWM4 also pulls low when PWM1 is high, so the low-side MOSFET of Phase 4 is on to conduct the Phase 4 coupled current. 1'b0: disable couple inductor mode for 1-phase operation 1'b1: enable couple inductor mode for 1-phase operation
7	CPL_MODE_EN	Enables Rail 1 couple inductor mode. 1'b0: disable couple inductor mode 1'b1: enable couple inductor mode
6	LOW_PWR_MODE_EN	Enables low-power mode. 1'b0: regular-power mode. In regular-power mode, the EEPROM and PMBus are live. EN is used to enable the output power. 1'b1: enable low-power mode. In low-power mode, the EEPROM is off and the device consumes around 120μA of current to minimize the power dissipation when both EN1/2 are low.

5:4	EN_OFF_MODE_SEL	Selects the EN power-off mode and soft-off slew rate. 2'b00: Hi-Z off 2'b01: soft-off with SVID mode slow DVID slew rate 2'b10: soft-off with SVID mode fast DVID slew rate 2'b11: soft-off with PMBus mode DVID slew rate
3	ON/OFF_DLY_CLK_SEL	Selects the clock frequency for the Rail 1 turn-on delay and turn-off delay counter. The counter is set with the PMBus command TON_DELAY (60h, Page 0) and TOFF_DELAY (64h, Page 0). Refer to TON_DELAY (60h) and TOFF_DELAY (64h) on page 74 for more information. 1'b0: 50kHz 1'b1: 20kHz
2:0	OV/UV_VTH_SEL	V_{OUT} OVP/UVP thresholds selection bits. The threshold is related with the remote sense amplifier gain set by register VOUT_SENSE_SETSCALE_SET (29h) bit[11]. With remote sense amplifier unit gain: 3'b100: OVP threshold = VREF + 300mV, UVP threshold = VREF - 300mV 3'b010: OVP threshold = VREF + 220mV, UVP threshold = VREF - 220mV 3'b001: OVP threshold = VREF + 140mV, UVP threshold = VREF - 140mV With remote sense amplifier half gain: 3'b100: OVP threshold = VREF + 600mV, UVP threshold = VREF - 600mV 3'b010: OVP threshold = VREF + 440mV, UVP threshold = VREF - 440mV 3'b001: OVP threshold = VREF + 280mV, UVP threshold = VREF - 280mV Others: invalid

MFR_APS_FS_CTRL (45h) *(Page 0)*

The MFR_APS_FS_CTRL command on Page 0 sets the threshold of the time interval between the consecutive phases' PWM rising edges to exit phase shedding. This register is also used to enable the exit-phase-shedding strategy by detecting the PWM frequency.

Command	MFR_APS_FS_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables the exit-phase-shedding according to the PWM1 off time. The time threshold is set by register MFR_FS_LIMIT_12P (46h) bit[7:0]. The PWM minimum off time is excluded (see Figure 30a). 1'b0: disable the PWM1 off time detection to exit APS 1'b1: enable the PWM1 off time detection to exit APS
10	FS_EXIT_APS_EN_NP	Enable exit-phase-shedding according to multi-phase PWM interval time between consecutive phases. The time threshold is set by register 46h, 47h, 48h, and 49h. The PWM blanking time is excluded (see Figure 30b). 1'b0: disable the multi-phase PWM interval time detection to exit APS 1'b1: enable the multi-phase PWM interval time detection to exit APS
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count of the PWM1 off-time condition to exit phase shedding. Once the PWM off time condition meets the counting threshold, the controller exits APS immediately.

6:3	RETURN_APS_DELAY	Sets the minimum full-phase running time after exiting APS. 20μs/LSB.
2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWM interval time to exit phase shedding. Once the PWM interval condition meets the counting threshold, the controller exits APS immediately.

Figure 30a: FS_LIMIT_1P/FS_LIMIT_7P Condition at 1-Phase Operation

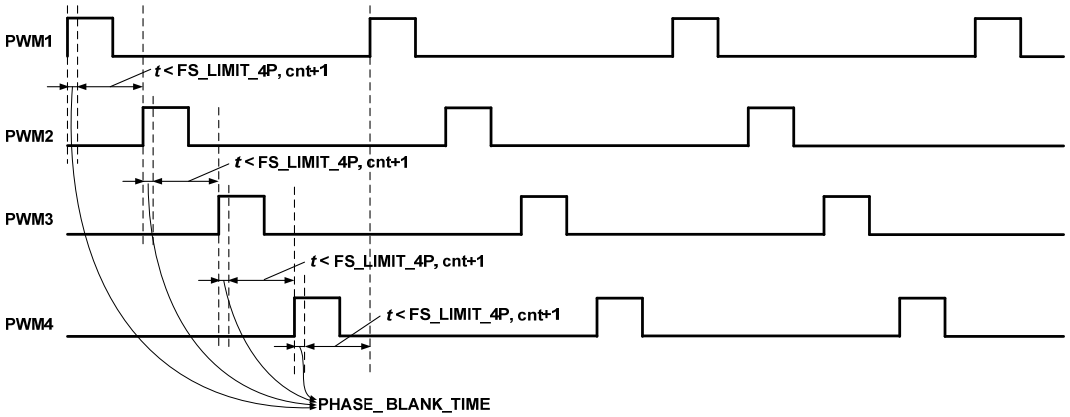


Figure 30b: FS_LIMIT_NP Condition at N-Phase Operation (N = 4)

MFR_FS_LIMIT_12P (46h) *(Page 0)*

This MFR_FS_LIMIT_12P command on Page 0 sets the threshold of the PWM interval time at 1-phase and 2-phase operation to detect fast load insertion and exit the phase-shedding state. This command is for Rail 1 only.

Command	MFR_FS_LIMIT_12P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FS_LIMIT_2P								FS_LIMIT_1P							

Bits	Bit Name	Description
15:8	FS_LIMIT_2P	Sets the exit-phase-shedding PWM interval time in 2-phase operation. If the time interval between two phases is less than FS_LIMIT_2P, the counter inside the MP2965 (count) will add one count. Figure 30b shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_1P	Sets the PWM1 off-time threshold to exit phase shedding. If the PWM1 off time after excluding the MIN_OFF_TIME is less than FS_LIMIT_1P, the counter inside the MP2965 (count) will add one count. Figure 30a shows the definition of FS_LIMIT_1P. 10ns/LSB.

MFR_FS_LIMIT_34P (47h) *(Page 0)*

This MFR_FS_LIMIT_34P command on Page 0 sets the threshold of the PWM interval time at 3-phase and 4-phase operation to detect fast load insertion and exit the phase-shedding state. This command is for Rail 1 only.

Command	MFR_FS_LIMIT_34P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FS_LIMIT_4P								FS_LIMIT_3P							

Bits	Bit Name	Description
15:8	FS_LIMIT_4P	Set exit-phase-shedding PWM interval time at Rail 1 4-phase operation. Figure 30b shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_3P	Set exit-phase-shedding PWM interval time at Rail 1 3-phase operation. Figure 30b shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

MFR _FS_LIMIT_56P (48h) *(Page 0)*

This MFR_FS_LIMIT_56P command on Page 0 sets the threshold of the PWM interval time to detect fast load insertion and exit the phase-shedding state.

Command	MFR_FS_LIMIT_56P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FS_LIMIT_6P								FS_LIMIT_5P							

Bits	Bit Name	Description
15:8	FS_LIMIT_6P	Sets the exit-phase-shedding PWM interval time at Rail 1 6-phase operation and Rail 2 2-phase operation. Figure 30b shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.
7:0	FS_LIMIT_5P	Sets the exit-phase-shedding PWM interval time at Rail 1 5-phase operation and Rail 2 3-phase operation. Figure 30b shows the definition of FS_LIMIT_NP when N = 4. 5ns/LSB.

MFR _FS_LIMIT_7P (49h) *(Page 0)*

This MFR_FS_LIMIT_7P command on Page 0 sets the threshold of the PWM interval time to detect fast load insertion and exit the phase-shedding state. This command is active for Rail 1 7-phase operation and Rail 2 1-phase operation.

Command	MFR_FS_LIMIT_7P							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	FS_LIMIT_7P							

Bits	Bit Name	Description
7:0	FS_LIMIT_7P	For Rail 1 7-phase operation, set the PWM interval time to maintain 7-phase operation. Figure 30b shows the definition of FS_LIMIT_NP when N = 4, in this case. 5ns/LSB. For Rail 2 1/2/3-phase operation, set the PWM1 off-time threshold to exit phase shedding. If the PWM1 off time after excluding MIN_OFF_TIME is less than FS_LIMIT_7P, the counter inside the MP2965 (count) will add one count.. Figure 30a shows the definition of FS_LIMIT_7P in this case. 10ns/LSB.

IOUT_OC_WARN_LIMIT (4Ah) *(Page 0)*

The IOUT_OC_WARN_LIMIT command on Page 0 sets the Rail 1 I_{OUT} over-current warning threshold.

Command	IOUT_OC_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	IOUT_OC_WARN_LIMIT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	IOUT_OC_WARN_LIMIT	Sets the I_{OUT} OC warning threshold in direct format. 1A/LSB. If the sensed output current is greater than IOUT_OC_WARN_LIMIT, bit[14] of register STATUS_WORD (79h) and bit[5] of register STATUS_IOUT (7Bh) are set. PWR_IN_ALT# is asserted if MFR_VR_CONFIG3 (44h) bit[9] = 1.

MFR_IMON_DGTL_GAIN (4Dh) *(Page 0)*

The MFR_IMON_DGTL_GAIN command on Page 0 sets the digital calculating gain for Rail 1 I_{OUT} reporting.

Command	MFR_ IMON_DGTL_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	IMON_DGTL_GAIN										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	IMON_DGTL_GAIN	Sets the digital calculating gain for I_{OUT} reporting. The gain is multiplied to the IMON ADC sensed values and forms the final IMON digital sense value. The IMON digital sense value is used for output current reporting. The final IMON sensed value can be calculated with the following equation: $IMON\_SNS\_FNL = 1023 \times \frac{I_{OUT} \times K_{CS} \times R_{IMON}}{1.6 \times 16} \times \frac{IMON\_DGTL\_GAIN}{1024}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase current-sense gain (A/A), R_{IMON} is the IMON resistor (in Ω), and IMON_DGTL_GAIN is the decimal value.

MFR_IDROOP_CTRL (4Eh) *(Page 0)*

The MFR_IDROOP_CTRL command on Page 0 is used to program the DC load line and AC droop current.

Command	MFR_IDROOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x			IDROOP_GAIN			

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

5:4	IDROOP_TRIM_SEL	The MP2965 provides 16 types of gain selection from I_{CS_SUM} to I_{DROOP}, which is controlled by IDROOP_SET (i.e.: MFR_IDROOP_CTRL (4Eh) bit[3:0]). The device also provides four ATE trimming results to trim the gain and offset of I_{DROOP}/I_{CS_SUM} to get a precise load-line value. Each of the four types of gain the share the same ATE trimming registers. 2'b00: select ATE trim 1 for IDROOP gain from 0, 5/64 ~ 7/64 2'b01: select ATE trim 2 for IDROOP gain from 8/64 ~ 11/64 2'b10: select ATE trim 3 for IDROOP gain from 12/64 ~ 15/64 2'b11: select ATE trim 4 for IDROOP gain from 16/64 ~ 19/64
3:0	IDROOP_GAIN	Sets the gain of I_{DROOP}/I_{CS_SUM}. The equation below shows the value of IDROOP_GAIN and the I_{DROOP} current. $I_{DROOP} = \begin{cases} 0 & IDROOP\_GAIN = 0 \\ \frac{IDROOP\_GAIN + 4}{64} \times I_{CS\_SUM} & IDROOP\_GAIN \neq 0 \end{cases}$ Where I_{CS_SUM} is the current sinking into the CS_SUM pin (in A).

OT_WARN_LIMIT (51h) *(Page 0)*

The OT_WARN_LIMIT command sets the over-temperature warning threshold.

Command	OT_WARN_LIMIT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OT_WARN_LIMIT							

Bits	Bit Name	Description
7:0	OT_WARN_LIMIT	Sets the over-temperature warning threshold. If the sensed temperature via VTEMP is higher than this threshold, bit[6] of STATUS_TEMPERATURE (7Dh) is set. 1°C/LSB.

VIN_OV_FAULT_LIMIT (55h) *(Page 0)*

The VIN_OV_FAULT_LIMIT command sets the VIN over-voltage protection threshold. This register is in linear format. If the sensed input voltage is higher than the VIN_OV fault limit, the VR shuts down immediately and asserts the PG signal. Always set the VIN_OV fault limit higher than the VIN_OV warning limit.

Command	VIN_OV_FAULT_LIMIT															
Format	Linear, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EXPONENT					x	x	x	MANTISSA							

Bits	Bit Name	Description
15:11	EXPONENT	This is the exponent for the linear format in two's complement format. The value is fixed to: Binary: 11101 Decimal: -3 Real-world value: 0.125V
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	MANTISSA	This is the mantissa for the linear format in two's complement format. The VIN_OV fault limit can be calculated with the equation below: $VIN\_OV\_FAULT\_LIMIT(V) = MANTISSA \times 0.125(V)$

VIN_UV_WARN_LIMIT (58h) *(Page 0)*

The VIN_UV_WARN_LIMIT command sets the VIN under-voltage warning threshold.

Command	VIN_UV_WARN_LIMIT															
Format	Linear, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Exponent					x	x	x	MANTISSA							

Bits	Bit Name	Description
15:11	Exponent	This is the exponent for the linear format in two's complement format. The value is fixed to: Binary: 11101 Decimal: -3 Real-world value: 0.125V
10:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	Mantissa	This is the mantissa for the linear format in two's complement format. The VIN_UV warning limit can be calculated with the equation below: $VIN\_UV\_WAUN\_LIMIT(V) = MANTISSA \times 0.125(V)$

MFR_PGOOD_SET (5Dh) *(Page 0)*

The MFR_PGOOD_SET command on Page 0 instructs the device when to assert VRRDY1 by setting the VRRDY1 action mode and VRRDY1 signal assertion delay time. The VRRDY assertion delay time is only effective in VRRDY non-Intel mode.

Command	MFR_PGOOD_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x		PGOOD_DELAY							

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	PGOOD_MODE	Sets the VRRDY action mode. 1'b0: Intel mode. VRRDY asserts once VID reaches VBOOT. 1'b1: non-Intel mode. VRRDY asserts when the condition set by the PMBus command POWER_GOOD_ON (5Eh) is met and the VRRDY delay time ends.
7:0	PGOOD_DELAY	Sets the VRRDY assertion delay time. This bit is only effective when VRRDY mode is set to non-Intel mode. 1μs/LSB.

POWER_GOOD_ON (5Eh) *(Page 0)*

This POWER_GOOD_ON command on Page 0 sets the output voltage threshold at which the VRRDY1 signal asserts. This command is only effective in VRRDY non-Intel mode.

Command	POWER_GOOD_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	POWER_GOOD_ON								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_ON	Sets the VID threshold at which the VRRDY signal asserts. This bit is in a direct format with VID resolution. This bit is only effective when MFR_PGOOD_SET (5Dh) bit[8] = 1. 1-VID step/LSB.

POWER_GOOD_OFF (5Fh) *(Page 0)*

The POWER_GOOD_OFF command on Page 0 sets the output voltage threshold at which the VRRDY1 signal de-asserts. This command is only effective in VRRDY non-Intel mode.

Command	POWER_GOOD_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	POWER_GOOD_OFF								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_OFF	Sets the V_{OUT} threshold at which the VRRDY signal de-asserts. This bit is in a direct format with VID resolution. This bit is only effective when MFR_PGOOD_SET (5Dh) bit[8] = 1. 1-VID step/LSB.

TON_DELAY (60h) *(Page 0)*

This TON_DELAY commands on Page 0 sets the delay time from when system initialization ends to when VREF1 starts to boot up.

Command	TON_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Sets the delay time from when the system initialization ends to when VREF boots up. The resolution is determined by the PMBus command MFR_VR_CONFIG3 (44h) bit[3] (ON/OFF_DLY_CLK_SEL). 20μs/LSB (ON/OFF_DLY_CLK_SEL = 0) 50μs/LSB (ON/OFF_DLY_CLK_SEL = 1)

TOFF_DELAY (64h) *(Page 0)*

This TOFF_DELAY command on Page 0 sets the delay time from when EN goes low to when VREF starts to soft-shutdown on Rail 1. This command is only effective at EN soft off.

Command	TOFF_DELAY															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Sets the delay time from when EN goes low to when VREF enters soft-shutdown. The resolution is determined by the PMBus command MFR_VR_CONFIG3 (44h) bit[3] (ON/OFF_DLY_CLK_SEL). 20μs/LSB (ON/OFF_DLY_CLK_SEL = 0) 50μs/LSB (ON/OFF_DLY_CLK_SEL = 1)

POUT_OP_WARN_LIMIT (6Ah) *(Page 0)*

This POUT_OP_WARN_LIMIT command on Page 0 sets the Rail 1 P_{OUT} warning limit.

Command	POUT_OP_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	POUT_OP_WARN_LIMIT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	POUT_OP_WARN_ LIMIT	Sets the output over-power warning threshold. If the sensed output power is higher than this threshold, bit[0] of STATUS_IOUT (7Bh) is set. 1W/LSB.

READ_CS12 (74h) *(Page 0)*

The READ_CS12 command on Page 0 returns the ADC-sensed average voltage on CS1 and CS2 in a direct format when they are assigned to Rail 1. An internal low-pass filer is used before the ADC.

Command	READ_CS12															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	READ_CS2								READ_CS1							

Bits	Bit Name	Description
15:8	READ_CS2	Returns the ADC sensed voltage on CS2 in direct format. 12.5mV/LSB.
7:0	READ_CS1	Returns the ADC sensed voltage on CS1 in direct format. 12.5mV/LSB.

READ_CS34 (75h) *(Page 0)*

The READ_CS34 command on Page 0 returns the ADC-sensed voltage on CS3 and CS4 in a direct format when they are assigned to Rail 1.

Command	READ_CS34															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	READ_CS4								READ_CS3							

Bits	Bit Name	Description
15:8	READ_CS4	Returns the ADC-sensed voltage on CS4 in direct format. 12.5mV/LSB.
7:0	READ_CS3	Returns the ADC-sensed voltage on CS3 in direct format. 12.5mV/LSB.

READ_CS56 (76h) *(Page 0)*

The READ_CS56 command on Page 0 returns the ADC-sensed voltage on CS5 and CS6 in a direct format when it is assigned to Rail 1.

Command	READ_CS56															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	READ_CS6								READ_CS5							

Bits	Bit Name	Description
15:8	READ_CS6	Returns the ADC-sensed voltage on CS6 in direct format. 12.5mV/LSB.
7:0	READ_CS5	Returns the ADC-sensed voltage on CS5 in direct format. 12.5mV/LSB.

READ_CS7 (77h) *(Page 0)*

The READ_CS7 command on Page 0 returns the ADC-sensed voltage on CS7 in a direct format when Phase 7 is assigned to Rail 1.

This register is the phase-current ADC value of Phase 7 of Rail 1. An internal low-pass filter is used before ADC.

Command	READ_CS7															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x								READ_CS7							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_CS7	Returns the ADC-sensed voltage on CS7 in direct format. 12.5mV/LSB.

STATUS_BYTE (78h) *(Page 0)*

The STATUS_BYTE command returns one byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function								x

Bits	Bit Name	Behavior	Description
7	EEPROM_BUSY	Live	Reports the live status of the EEPROM. 1’b0: EEPROM is idle 1’b1: EEPROM is busy

6	OFF	Live	Rail 1 output is off. This bit is in live mode and is asserted if the unit is not providing power to the output. The power-off may be caused by protections, EN low, or VID = 0. 1'b0: VOUT1 is off 1'b1: VOUT1 is on
5	VOUT_OV_FAULT	Latch	Rail 1 output voltage (OV) fault indicator. This bit is set and latched if Rail 1 OVP occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no V_{OUT} OV fault 1'b1: V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 1 output current (OC) fault indicator. This bit is set and latched if Rail 1 OCP occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no output OC fault 1'b1: output OC fault has occurred
3	VIN_UV_FAULT	Latch	V_{IN} under-voltage (UV) fault indicator. This bit is set and latched if an input voltage UV fault occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no V_{IN} UV fault 1'b1: V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature fault and warning indicator. This bit is set and latched once OTP or a warning occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no OT fault or warning 1'b1: OT fault or warning has occurred
1	CML	Latch	PMBus communication fault indicator. Once a communication, memory, or logic fault occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no CML fault 1'b1: a CML fault has occurred
0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_WORD (79h) *(Page 0)*

The STATUS_WORD (79h) command on Page 0 returns two bytes of information with a summary of the device fault/warning condition. The higher byte provides more detailed information of the fault conditions. The lower byte is same as in the STATUS_BYTE register.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function						x	x		STATUS_BYTE (78h)							

Bits	Bit Name	Behavior	Description
15	VOUT	Latch	Rail 1 VOUT fault and warning indicator. Once an output over-voltage or under-voltage protection or warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: no V_{OUT} fault/warning 1'b1: V_{OUT} fault/warning has occurred

14	IOUT/POUT	Latch	Rail 1 I_{OUT}/P_{OUT} fault and warning indicator. Once the output current fault and warning or output power warning occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no I_{OUT}/P_{OUT} fault and warning 1'b1: I_{OUT}/P_{OUT} fault or warning has occurred
13	INPUT	Latch	Input voltage, current, and power fault/warning indicator. Once any protection or warning of the input voltage, input current, or input power occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no input fault and warning 1'b1: input fault or warning has occurred
12	VCCIO FAULT	Latch	VCCIO under-voltage indicator. Once the VCCIO voltage falls below 0.65V, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no VCCIO under voltage 1'b1: VCCIO has been lower than 0.65V
11	PGOOD	Live	Rail 1 VRRDY status indicator. At VRRDY Intel mode, once V_{OUT} reaches the boot-up voltage level, this bit is set. This bit is reset when V_{OUT} is disabled or in a fault state. At VRRDY non-Intel mode, when V_{OUT} rises higher than the POWER_GOOD_ON level and the PGOOD delay time expires, this bit is asserted. It is de-asserted when V_{OUT} drops to the POWER_GOOD_OFF level or a fault occurs.
10:9	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
8	WATCH_DOG_OVF	Latch	The watchdog of the monitor block timer overflow indicator. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer are reset. Meanwhile, this bit is set. The CLEAR_FAULTS command can reset this bit. 1'b0: watchdog timer does not overflow 1'b1: watchdog timer has overflowed
7:0	STATUS_BYTE (78h)	/	Same value as register STATUS_BYTE (78h).

STATUS_VOUT (7Ah) *(Page 0)*

The STATUS_VOUT command on Page 0 returns one byte of information with the detailed V_{OUT} fault and warning status on Rail 1.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x				x		

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 1 V_{OUT} OV fault indicator. Once the output over-voltage protection occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no V_{OUT} OV fault 1'b1: V_{OUT} OV fault has occurred
6, 2	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.

5	VOUT_UV_WARNING	Latch	Rail 1 V_{OUT} UV warning indicator. Once the output under-voltage warning occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no V_{OUT} UV warning 1'b1: V_{OUT} UV warning has occurred
4	VOUT_UV_FAULT	Latch	Rail 1 V_{OUT} UV fault indicator. Once the output under-voltage fault occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no V_{OUT} UV fault 1'b1: V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Indicator that the Rail 1 V_{OUT} has reached VOUT_MAX and VOUT_MIN. Once the VID value exceeds the value set in VOUT_MAX (24h) and VOUT_MIN (2Bh), this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID is higher than VOUT_MAX or lower than VOUT_MIN
1	LINE_FLOAT	Latch	Rail 1 line float protection indicator. Once the line float fault is detected, the device shuts down the associated rail and sets the LINE_FLOAT bit. This bit is in latched mode. Send CLEAR_FAULTS (03h) to reset this bit. 1'b0: no line float fault 1'b1: line float fault has occurred
0	VDIFF_SC_FAULT	Latch	Rail 1 VDIFF short to GND fault indicator. Once the MP2965 detects that VDIFF is shorted to GND, VDIFF_SC_FAULT is set and latched. The output is shut down immediately. Send CLEAR_FAULTS (03h) to reset this bit. 1'b0: no VDIFF short to GND fault 1'b1: VDIFF has been shorted to GND

STATUS_IOUT (7Bh) *(Page 0)*

The STATUS_IOUT command on Page 0 returns one byte of information with the detailed I_{OUT} fault and warning status on Rail 1.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function				x	x	x	x	

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 1 output OC fault indicator. Once output OCP occurs, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no output over-current fault 1'b1: output over-current fault has occurred
6	OC_UV_FAULT	Latch	Rail 1 output OC and UV dual faults indicator. Once the output over-current occurs and the under-voltage comparator is set simultaneously, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no output over-current or under-voltage faults 1'b1: output over-current has occurred and the under-voltage comparator is set

5	IOUT_OC_WARNING	Latch	Rail 1 output OC warning indicator. Once the output over-current warning occurs, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no output over-current warning 1'b1: output over-current warning has occurred
4:1	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
0	POUT_OP_WARNING	Latch	Rail 1 output over-power warning indicator. Once an output over-power warning occurs, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset it. 1'b0: no output over-power warning 1'b1: output over-power warning has occurred

STATUS_ INPUT (7Ch) *(Page 0)*

The STATUS_INPUT command returns one byte of information with detailed input fault and warning conditions.

Command	STATUS_INPUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x				x	x	

Bits	Bit Name	Behavior	Description
7	VIN_OV_FAULT	Latch	Input voltage OV fault indicator. Once the sensed input voltage is higher than the VIN OV fault limit, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no VIN OV fault 1'b1: VIN OV fault has occurred
6, 2:1	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
5	VIN_UV_WARNING	Latch	Input voltage UV fault indicator. Once the sensed input voltage is lower than the VIN UV warning limit, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no VIN UV warning 1'b1: VIN UV warning has occurred
4	VIN_UVLO_LATCH	Latch	Input voltage UVLO fault indicator. Once the sensed input voltage is lower than the VIN_OFF (36h) threshold, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset it. 1'b0: no VIN UVLO fault 1'b1: VIN UVLO fault has occurred

3	VIN_UVLO_LIVE	Live	Input voltage UVLO live indicator. Once the sensed input voltage is lower than VIN_OFF, this bit is set. Once the sensed input voltage is higher than VIN_ON, this bit is reset. 1'b0: input voltage is lower than VIN_OFF (35h) 1'b1: input voltage is higher than VIN_ON (36h)
0	PIN_WARN	Latch	Input power over-power warning indicator. Once the sensed input power is higher than POUT_OP_WARN_LIMIT (6Ah), this bit is set and latched until a CLEAR_FAULTS (03h) command resets it.

STATUS_TEMPERATURE (7Dh) *(Page 0)*

The STATUS_TEMPERATURE command on Page 0 returns one byte of information with temperature-related fault and warning conditions.

Command	STATUS_ TEMPERATURE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function			x	x	x	x	x	x

Bits	Bit Name	Behavior	Description
7	TEMP_OT_FAULT	Latch	Over-temperature fault indicator. Once the sensed temperature via VTEMP pin is higher than the OT fault limit set by MFR_OTP_SET (Edh), this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no over-temperature fault 1'b1: over-temperature fault has occurred
6	TEMP_OT_WARNING	Latch	Over-temperature warning indicator. Once the sensed temperature via VTEMP pin is higher than the OT warning limit set by OT_WARN_LIMIT (51h), this is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no over-temperature warning 1'b1: over-temperature warning has occurred
5:0	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.

STATUS_ CML (7Eh) *(Page 0)*

The STATUS_CML command returns one byte of information with PMBus communication-related faults.

Command	STATUS_ CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function					x			
Bits	Bit Name		Behavior	Description				

7	INVALID_CMD	Latch	Invalid PMBus command indicator. This bit is set and latched when the MP2965 receives an unsupported command code. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no invalid PMBus command 1'b1: invalid PMBus command has been received
6	INVALID_DATA	Latch	Invalid PMBus data indicator. This bit is set and latched when the MP2965 receives unsupported data. Send the CLEAR_FAULTS (03h) command to reset it. 1'b0: no invalid PMBus data 1'b1: invalid PMBus data has been received
5	PEC_ERROR	Latch	PMBus PEC fault indicator. The PMBus interface supports the use of the packet error checking (PEC) byte defined in the SMBus standard. The PEC byte is transmitted by the MP2965 during a read transaction or sent to the MP2965 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed, and PEC_FAULT is set and latched. Send the CLEAR_FAULTS (03h) command to clear the fault. 1'b0: no PEC fault 1'b1: a PEC fault has been detected
4	CRC_FAULT	Latch	CRC fault indicator. In the process of storing operating memory data into the EEPROM, the MP2965 calculates a CRC code for each bit and saves the final CRC code into the EEPROM. In the process of restoring the EEPROM data to the operating memory, the MP2965 re-calculates the CRC code with each bit. The MP2965 checks the CRC results when the restore process is done. If the CRC result does not match what was stored during the storing process, the VR shuts down and sets the CRC_FAULT bit. This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to reset the fault. 1'b0: no EEPROM CRC fault 1'b1: an EEPROM CRC fault has been detected
3	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
2	CML_FLT_TRG	Latch	This bit is set when the EEPROM operation is blocked for the process of the controller recording faults to the EEPROM. This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to clear the fault. 1'b0: no EEPROM operation is blocked for fault recording 1'b1: EEPROM operation has been blocked for fault recording
1	CML_OTHER_FAULTS	Latch	This bit can be set when any of the faults below occur during PMBus communication: 1) Sending too few bits 2) Reading too few bits 3) Host sends or reads too few bytes 4) Reading too many bytes This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to clear the fault.
0	EEPROM_SIG_FAULT	Latch	While restoring data from the EEPROM to the memory, this bit first checks the signature register in address 00h of the EEPROM. If the signature is not 0x1234, the restore process is ceased immediately and sets EEPROM_SIG_FAULT. This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to clear the fault.

READ_VIN (88h) *(Page 0)*

The READ_VIN command returns two bytes of information with the sensed input voltage with a direct format.

Command	READ_VIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	1	0	1	0	0	0	READ_VIN									

Bits	Bit Name	Description
15:10	FIXED	Fixed to 101000.
9:0	READ_VIN	Returns the sensed input voltage with direct format. 31.25mV/LSB.

READ_IIN (89h) *(Page 0)*

The READ_IIN command returns the sensed input current in a direct format.

Command	READ_IIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	1	1	1	0	0	x	READ_IIN									

Bits	Bit Name	Description
15:11	EXPONENT	Fixed to 11100.
10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	READ_IIN	Returns the sensed input current in direct format. 62.5mA/LSB.

READ_VOUT (8Bh) *(Page 0)*

The READ_VOUT command on Page 0 returns two bytes of information with the V_{OUT} of Rail 1 in a direct format.

Command	READ_VOUT															
Format	VID or Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x	x	x	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the sensed voltage of VOSEN - VORTN. The voltage report is in VID format with VID resolution or direct format with 1mV resolution. The resolution is determined by the PMBus command MFR_LOOP_PI_SET (E2h, Page 0) bit[10] (VOUT_PMBUS_LSB). 1 VID step/LSB when VOUT_PMBUS_LSB = 0 1mV/LSB when VOUT_PMBUS_LSB = 1

READ_IOUT (8Ch) *(Page 0)*

The READ_IOUT command on Page 0 returns the sensed output current of Rail 1 in a direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	1	1	1	1	0	READ_IOUT										

Bits	Bit Name	Description
15:11	FIXED	Read-only registers. Fixed to 5'b11110.
10:0	READ_IOUT	Returns the sensed output current. 0.25A/LSB.

READ_TEMPERATURE (8Dh) *(Page 0)*

The READ_TEMPERATURE command on Page 0 returns the sensed temperature on VTEMP.

Command	READ_TEMPERATURE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x	x	x	x	x	x	x	READ_TEMPERATURE							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_TEMPERATURE	Returns the sensed temperature on VTEMP in direct format. 1°C/LSB.

READ_POUT (96h) *(Page 0)*

The READ_POUT command on Page 0 returns the sensed output power of Rail 1 in a direct format.

Command	READ_POUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x	x	x	x	x	x	READ_POUT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	READ_POUT	Returns the sensed output power in direct format. 1W/LSB.

READ_PIN (97h) *(Page 0)*

The READ_PIN command on Page 0 returns the sensed input power in a direct format.

Command	READ_PIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x	x	x	x	x	READ_PIN									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

9:0	READ_PIN	Returns the sensed input power in direct format. The resolution is determined by the PMBus command MFR_PIN_SET (BEh, Page 1), bit[9:8] (PIN_GAIN). 0.25W/LSB when PIN_GAIN = 2'b1x 0.5W/LSB when PIN_GAIN = 2'b01 1W/LSB when PIN_GAIN = 2'b00

MFR_CS_OFFSET1 (A5h) *(Page 0)*

The MFR_CS_OFFSET1 command sets the CS ADC sensing value offset for thermal balance adjusting.

Command	MFR_CS_OFFSET1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	CS4_OFFSET					CS3_OFFSET					CS2_OFFSET				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	CS4_OFFSET	Sets the offset on the ADC-sensed value of the CS4 voltage. This bit is in two's complement format. Bit[14] is the signed bit. The real-world current affected by the CS4_OFFSET can be calculated with the following equation: $I_{OFFSET} = 6.25 \times 10^{-3} \times \frac{CSx\_OFFSET}{K_{CS} \times R_{CS}}$ Where I_{OFFSET} is the real-world offset current, CSx_OFFSET is the real-world decimal value, K_{CS} is the current sensing gain (in A/A), and R_{CS} is the CS resistor (in Ω).
9:5	CS3_OFFSET	Sets the offset on the ADC-sensed value of the CS3 voltage. This bit is in two's complement format. Bit[9] is the signed bit.
4:0	CS2_OFFSET	Sets the offset on the ADC-sensed value of the CS2 voltage. This bit is in two's complement format. Bit[4] is the signed bit.

MFR_CS_OFFSET2 (A6h) *(Page 0)*

The MFR_CS_OFFSET2 command sets the CS ADC sensing value offset for thermal balance adjusting.

Command	MFR_CS_OFFSET2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	CS7_OFFSET					CS6_OFFSET					CS5_OFFSET				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

14:10	CS7_OFFSET	Sets the offset on the ADC-sensed value of the CS7 voltage. It is in a two's complement format. Bit[14] is the signed bit. The real-world current affected by CS4_OFFSET can be calculated with the following equation: $I_{OFFSET} = 6.25 \times 10^{-3} \times \frac{CSx\_OFFSET}{K_{CS} \times R_{CS}}$ Where CS_OFFSET is the real-world decimal value, K_{CS} is the current sensing gain (in A/A), and R_{CS} is the CS resistor (in Ω).
9:5	CS6_OFFSET	Sets the offset on the ADC-sensed value of the CS6 voltage. This bit is in two's complement format. Bit[9] is the signed bit.
4:0	CS5_OFFSET	Sets the offset on the ADC-sensed value of the CS5 voltage. This bit is in two's complement format. Bit[4] is the signed bit.

IOUT_RPT_GAIN_HC (A7h) *(Page 0)*

The IOUT_RPT_GAIN_HC command on Page 0 sets the Rail 1 IMON sensing gain for the VR13.HC output current report.

Command	IOUT_PRT_GAIN_HC															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x										

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	IMON_GAIN_HC	Sets the current sense gain for the VR13.HC output current report. The current sense gain can be calculated with the equation below: $IMON\_GAIN\_HC = 40 \times I_{CCMAX\_HC} \times K_{CS} \times R_{IMON} / 1000$ Where I_{CCMAX} is the maximum current of the VR13.HC CPU (in A), K_{CS} is the Intelli-Phase current sense gain (in μA/A), and R_{IMON} is the IMON resistor (in kΩ).

IOUT_RPT_GAIN_SVID_AVS (A8h) *(Page 0)*

The IOUT_RPT_GAIN_SVID_AVS command on Page 0 sets the Rail 1 IMON gain for the VR13 CPU I_{OUT} report in SVID override mode and the AVSBus I_{OUT} reports in AVSBus VID override mode.

Command	IOUT_RPT_GAIN_SVID_AVS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	AVSBUS_GIMON_RES				IMON_GAIN									

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13:10	AVSBUS_GIMON_RES	Selects the current-sense resolution for the AVSBus interface I_{OUT} report. This bit is only effective in AVSbus VID override mode. Note that the resolution selection is for an intermediate variable only, which is used to improve the AVSBus I_{OUT} report accuracy. The final AVSBus I_{OUT} report is always in 0.1A/LSB. 4'b0001: 20mA/LSB, AVSBus maximum report current is 41A 4'b0010: 40mA/LSB, AVSBus maximum report current is 82A 4'b0100: 80mA/LSB, AVSBus maximum report current is 164A 4'b1000: 160mA/LSB, AVSBus maximum report current is 328A 4'b0000: 320mA/LSB, AVSBus maximum report current is 656A Others are invalid input.
9:0	IMON_GAIN	Sets the current-sensing gain for the VR13 IOUT report and AVSBus I_{OUT} report. At VR13 SVID override mode, calculate the IMON sense gain with the following equation: $IMON\_GAIN = 40 \times I_{CCMAX} \times K_{CS} \times R_{IMON} / 1000$ Where I_{CCMAX} is the maximum current of the VR13.HC CPU (in A), K_{CS} is the Intelli-Phase current sense gain (in μA/A), and R_{IMON} is the IMON resistor (in kΩ). In AVSBus VID override mode, calculate the IMON sense gain with the following equation: $IMON\_GAIN = \begin{cases} \frac{K_{CS} \times R_{IMON}}{16} \times \frac{1023}{1.6} \times \frac{256}{50} \times AVSBUS\_GIMON\_RES & AVSBUS\_GIMON\_RES > 0 \\ \frac{K_{CS} \times R_{IMON}}{16} \times \frac{1023}{1.6} \times \frac{256}{50} \times 16 & AVSBUS\_GIMON\_RES = 0 \end{cases}$ Where K_{CS} is the Intelli-Phase current sense gain (in A/A), R_{IMON} is the IMON resistor (in Ω), and AVSBUS_GIMON_RES is the decimal value set with IOUT_RPT_GAIN_SVID_AVS (A8h) bit[13:10].

IOUT_RPT_OFFSET_SVID_AVS (A9h) *(Page 0)*

The IOUT_RPT_OFFSET_SVID_AVS command on Page 0 sets the output current report offset for VR13, VR13.HC, and AVSBus VID override mode. This command is for Rail 1 only.

Command	IOUT_RPT_OFFSET_SVID_AVS															
Format	Two's complement, direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	OFFSET_CPU							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

7:0	OFFSET_CPU	Sets the output current report offset. The value is a two's complement format. The values listed below show the binary data and real-world values. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0111 1111: 127 8'b 1000 0000: -128 8'b 1000 0001: -127 8'b 1111 1111: -1 The current resolution at VR13 and VR13.HC VID override mode is ICCMAX/255 (A/LSB), where ICCMAX is the current value set with the PMBus command MFR_ICC_MAX (BDh). The current resolution in AVSBus VID override mode follows the setting in IOUT_RPT_GAIN_SVID_AVS (A8h) bit[13:10].

MFR_PWM_STATE_ADV (ACh) *(Page 0)*

The MFR_PWM_STATE_ADV command is used to program the PWM minimum low time for PWM Hi-Z to low to high (HiZ-Low-Hi). This command also sets the MP2965 tri-state output mode and sets the slope voltage clamp mode at DCM.

Command	MFR_PWM_STATE_ADV							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function		PWM_TMIN_HIZ-LOW-HI						

Bits	Bit Name	Description
7	PWM_TMIN_HIZ-LOW-HI_EN	Enable the minimal PWM low-time interval from PWM HiZ-Low-Hi. 1'b0: no PWM low-time limitation from PWM HiZ-Low-Hi 1'b1: enable PWM low-time limitation from PWM HiZ-Low-Hi
6:3	PWM_TMIN_HIZ-LOW-HI	Sets the minimal PWM low-time interval from PWM HiZ-Low-Hi. 5ns/LSB.
2	PWM_TRI-S_MODE	Sets the PWM tri-state type. 1'b0: Hi-Z 1'b1: middle voltage of VDD33
1	DCM_SLOPE_VCLAMP_EN	Enables the slope voltage to a fixed VCLAMP at DCM when the slope CNT expires. 1'b0: disable slope clamping 1'b1: enable slope clamping when slope CNT expires.
0	DCM_SLOPE_LLKG_SW_EN	Enable low leakage switch for slope voltage generation block. 1'b0: disable slope low leakage switch 1'b1: enable slope low leakage switch at DCM when slope CNT expires.

MFR_DROOP_CMPN1 (B0h) *(Page 0)*

The MFR_DROOP_CMPN1 command on Page 0 sets the options to compensate for the voltage drop caused by an extra droop current on DVID up and a droop resistor is applied.

Command	MFR_DROOP_CMPN1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EN										DROOP_CMPN_LIMIT					

Bits	Bit Name	Description
15	DROOP_CMPN_EN	Droop compensation enable bit. 1'b0: disable droop compensation 1'b1: enable droop compensation
14:9	CNT_DROOP_CMPN_DEC	Sets the time interval for each VID step to decrease droop compensation after DVID up ends. 50ns/LSB.
8:6	CNT_DROOP_CMPN_INC	Sets the time interval for each VID step to add droop compensation when DROOP_CMPN_EN bit[15] = 1. 50ns/LSB.
5:0	DROOP_CMPN_LIMIT	Sets the maximum VID steps for droop compensation in a direct format. 1 VID step/LSB.

MFR_DROOP_CMPN2 (B2h) *(Page 0)*

The MFR_DROOP_CMPN2 command on Page 0 is used to compensate for the voltage offset caused by an extra droop current at DVID when a droop resistor is applied.

Command	MFR_DROOP_CMPN2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function											VID_FLTR_ACT_CTRL					

Bits	Bit Name	Description
15:14	VID_FLTR_SEL	Selects the VID-DAC output filter when DVID is down. 2'b00: 2.14µs 2'b01: 4.28µs 2'b10: 6.42µs 2'b11: 8.56µs
13	VID_FLTR_EN	Enables the VID-DAC output filter. 1'b0: disable VID-DAC filter 1'b1: enable VID-DAC filter
12	VID-DAC_CMPN_EN	A comparator is designed between the VID-DAC output and VID-DAC filter output. This bit is used to smooth the transition between DVID down and preemptive with DIVD up. 1'b0: disable VID-DAC comparator 1'b1: enable VID-DAC comparator
11:6	DLY_RST_DROOP_CMPN	Sets the delay time after VR_SETTLE to reset the droop compensation when DVID is up. 50ns/LSB.
5:0	VID_FLTR_ACT_CTRL	Sets the VID filter effective threshold in a direct format when droop compensation is resetting. This bit is only effective when bit[13] (VID_FLT_EN) = 1. 1 VID step/LSB.

MFR_ICC_MAX (BDh) *(Page 0)*

The MFR_ICC_MAX command on Page 0 sets the Rail 1 SVID maximum report current (FFh). The data is used for current scaling in the SVID command I_{OUT} (15h). This command also sets the value returned to the SVID command ICC_MAX (21h).

Command	MFR_ICC_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Function	ICCMAX_HC_ADD	ICCMAX_VR13

Bits	Bit Name	Description
15:8	ICCMAX_HC_ADD	Sets the VR13.HC SVID maximum report current with bit[7:0] (ICCMAX_VR13). For VR13.HC, the maximum SVID reported current can be calculated with the following equation: $ICCMAX = ICCMAX\_VR13 + ICCMAX\_HC\_ADD \times 2$ 2A/LSB.
7:0	ICCMAX_VR13	Sets the VR13 SVID maximum report current (FFh). Note that the output will not boot if ICCMAX_VR13 is set to 0.1A/LSB.

MFR_PIN_MAX (BEh) *(Page 0)*

The MFR_PIN_MAX command on Page 0 sets the Rail 1 maximum reported current of the SVID interface. This command is used for input power report scaling in SVID command PWR_IN (1Bh). The value in the command also sets the value return to the SVID command PWR_IN_MAX (2Eh) and the initial input power alert threshold.

Command	MFR_PIN_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PINMAX_HC_ADD								PINMAX_VR13							

Bits	Bit Name	Description
15:8	PINMAX_HC_ADD	Sets the VR13.HC maximum reported input power with the following equation: $PINMAX\_HC = PINMAX\_VR13 \times 2 + PINMAX\_HC\_ADD \times 4$ 4W/LSB.
7:0	PINMAX_VR13	Sets the VR13 maximum reported input power of SVID interface. It also sets the value return to the SVID command PWR_IN_MAX (2Eh) and the initial power alert threshold. 2W/LSB.

SVID_VENDOR_ PRODUCT_ID (BFh) *(Page 0)*

The SVID_VENDOR_PRODUCT_ID command sets the vendor ID and product ID of the MP2965.

Command	SVID_VENDOR_PRODUCT_ID															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	VENDOR_ID								PRODUCT_ID							

Bits	Bit Name	Description
15:8	VENDOR_ID	Sets the vendor ID for users. Default is 0x25, which presents “MPS corporation” in the Intel vendor list.
7:0	PRODUCT_ID	Sets the product ID for users. Default is 0x65, which presents “MP2965”.

CONFIG_ID (C0h) *(Page 0)*

The CONFIG_ID command provides two bytes to set the 4-digit product part number suffix. Contact an MPS FAE to get the 4-digit code.

Command	CONFIG_ID															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	CONFIG_ID															

Bits	Bit Name	Description
15:0	CONFIG_ID	Sets the 4-digit part number suffix for the MP2965.

SVID_LOT_CODE_PROTOCOL_ID (C1h) *(Page 0)*

The SVID_LOT_CODE_PROTOCOL_ID command provides two bytes to record the product lot code and Intel SVID protocol versions.

Command	SVID_LOT_CODE_PROTOCOL_ID															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	LOT_CODE								PROTOCOL_ID							

Bits	Bit Name	Description
15:8	LOT_CODE	Defines the part's lot code.
7:0	PROTOCOL_ID	Identifies Rail 1's version of the SVID protocol the controller supports. 01h: VR12.0, IMPV7 02h: VR12.5 03h: VR12.6 04h: VR13.0 10mV VID table 05h: IMVP8 06h: VR12.1 07h: VR13.0 5mV table 08h: IMVP9

SVID_CAPABILITY_DC_LL (C2h) *(Page 0)*

The SVID_CAPABILITY_DC_LL command sets the Intel VR13 specified CAPABILITY and DC_LL.

Command	SVID_CAPABILITY_DC_LL															
Format	Binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	CAPABILITY								DC_LL							

Bits	Bit Name	Description
15:8	CAPABILITY	Bit-mapped register. This bit identifies the SVID VR capabilities and which optional telemetry register is supported. 00h indicates that only required registers are supported.
7:0	DC_LL	Data register containing the programmed load line or AVP of the platform based on the output capacitance and R_{PATH}. If the PWM IC supports resistor LL or AVP programming, this register is not used. The master will not read this register. 0.1mΩ/LSB.

SVID_SR_FAST_SR _SLOW (C3h) *(Page 0)*

The SVID_SR_FAST_SR_SLOW command sets the Intel VR13 specified SR_FAST and SR_SLOW.

Command	SVID_SR_FAST_SR_SLOW															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	SR_FAST								SR_SLOW							

Bits	Bit Name	Description
15:8	SR_FAST	Data register containing the fast slew rate capability of the slew rate that Rail 1 can sustain. 1(mV/µs)/LSB.
7:0	SR_SLOW	Data register containing the capability of Rail 1's slow slew rate. 1(mV/µs)/LSB.

SVID_VR_TVRRDY_TOLERANCE1 (C4h) *(Page 0)*

The SVID_VR_TVRRDY_TOLERANCE1 command sets the Intel VR13 specified EN2SVID_RDY and VR tolerance1.

Command	SVID_VR_TVRRDY_TOLERANCE1															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EN2SVID_RDY								VR_TOLERANCE1							

Bits	Bit Name	Description
15:8	EN2SVID_RDY	This register holds an encoded value that represents VR enable to VR ready for SVID command latency. 1µs/LSB.
7:0	VR_TOLERANCE1	Data register containing the VR tolerance band (TOB) of Rail 1 based on board parts (inductor DCR and inductance tolerance, current sense errors etc). 1mV/LSB.

MFR_APS_LEVEL_1P (C5h) *(Page 0)*

When APS is enabled by setting MFR_VR_CONFIG (E4h) bit[5:4] = 2'b1x, this command sets the Rail 1 auto-phase shedding current threshold to 2-/1-phase.

Command	MFR_APS_LEVEL_1P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	DROP_LEVEL_1P								DROP_LEVEL_DCM							

Bits	Bit Name	Description
15:8	DROP_LEVEL_1P	Sets the auto-phase shedding current threshold to 1-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_DCM	Sets the auto-phase shedding current threshold to DCM. 1A/LSB.

MFR_APS_LEVEL_23P (C6h) *(Page 0)*

When APS is enabled by setting MFR_VR_CONFIG (E4h) bit[5:4] = 2'b1x, this command sets the Rail 1 auto-phase shedding current threshold to 4-phase and 3-phase operation.

Command	MFR_APS_LEVEL_23P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Function	DROP_LEVEL_3P	DROP_LEVEL_2P

Bits	Bit Name	Description
15:8	DROP_LEVEL_3P	Sets the auto-phase shedding current threshold to 3-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_2P	Sets the auto-phase shedding current threshold to 2-phase CCM. 1A/LSB.

MFR_APS_SET (C7h) *(Page 0)*

When APS is enabled by setting MFR_VR_CONFIG (E4h) bit[5:4] = 2'b1x, this sets the Rail 1 auto-phase shedding current hysteresis and phase via the phase-dropping time interval.

Command	MFR_APS_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	DROP_PHASE_WAITTIME							x	x	x	x	MFR_APS_HYS			

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	DROP_PHASE_ WAITTIME	Sets the phase-by-phase dropping time intervals. This bit is only effective when MFR_APS_SET (C7h), bit[8] = 1. 1µs/LSB.
8	MFR_AUTOPS_CTRL	Sets the auto-phase shedding behavior. 1'b0: drop phase count to target immediately 1'b1: shed phases one-by-one with a programmed delay time. The delay time is set with MFR_APS_SET (C7h) bit[14:9].
7:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	MFR_APS_HYS	Sets the current hysteresis between 1-phase shedding and adding. This bit is used to prevent phase shedding back and forth when APS is enabled. 1A/LSB.

MFR_IDROOP_OFFSET (C9h) *(Page 0)*

The MFR_IDROOP_OFFSET command on Page 0 provides one byte for users to add an offset over the Rail 1 droop current.

Command	MFR_IDROOP_OFFSET							
Format	Signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	IDROOP_OFFSET					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

<table>
<tr><td>5:0</td><td>IDROOP_OFFSET</td><td>Adds an offset to the droop current for users.
<table>
<tr><th>Bit[5] = 0</th><th>Positive</th><th>Bit[5] = 1</th><th>Negative</th><th>Unit</th></tr>
<tr><td>bit[4]</td><td>13</td><td>bit[4]</td><td>13</td><td>µA</td></tr>
<tr><td>bit[3]</td><td>6.48</td><td>bit[3]</td><td>6.48</td><td>µA</td></tr>
<tr><td>bit[2]</td><td>3.24</td><td>bit[2]</td><td>3.24</td><td>µA</td></tr>
<tr><td>bit[1]</td><td>1.62</td><td>bit[1]</td><td>1.62</td><td>µA</td></tr>
<tr><td>bit[0]</td><td>0.81</td><td>bit[0]</td><td>0.81</td><td>µA</td></tr>
</table></td></tr>
</table>

MFR_DC_LOOP_CTRL (CBh) *(Page 0)*

The MFR_DC_LOOP_CTRL command on Page 0 sets the DC loop calibration-related holding condition. This command also provides two bits to program the PWM behavior during phase adding.

Command	MFR_DC_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function			HOLD_LP_PRD_TIME										DC_CAL_MIN_THOLD			

Bits	Bit Name	Description
15	PRD_ADD_PH_MODE	Sets phase-adding mode when the PWM period meets the condition set with bit[13:7] in this command. 1'b0: add phases with a PWM low time inserted between HiZ-to-Hi 1'b1: add phases with a PWM HiZ-to-Hi directly
14	VFB-_ADD_PH_MODE	Sets phase-adding mode when VFB is lower than the VFB- window (i.e.: VID - 25mV window). 1'b0: add phases with a PWM low time inserted between HiZ-to-Hi 1'b1: add phases with a PWM HiZ-to-Hi directly
13:7	HOLD_LP_PRD_TIME	Sets the period changing time to hold the DC loop and current balance loop. If the PWM period meets the condition below, and the associated enable bit is set, the DC loop and CB loop are held. All loop hold functions related with this time setting are ineffective in DCM. $\left\|T_{PWM} - T_{PWM\_REF}\right\| \le HOLD\_LP\_PRD\_TIME \times 80ns$ Where TPWM is the real-time PWM period, and TPWM_REF is the nominal period set with MFR_FS (ECh). 80ns/LSB.
6	PRD_HOLD_DC_EN	1'b0: disable fs change condition to hold the DC loop 1'b1: enable fs change condition to hold the DC loop
5	PS_HOLD_DC_EN	1'b0: disable phase number change to hold the DC loop 1'b1: enable phase number change to hold the DC loop
4	TRANS_HOLD_DC_EN	1'b0: disable VFB+/- window condition to hold the DC loop 1'b1: enable VFB+/- window condition to hold the DC loop
3:0	DC_CAL_MIN_THOLD	Sets the DC loop minimal holding time in direct format. 200µs/LSB with +100µs offset.

MFR_APS_CTRL (CCh) *(Page 0)*

The MFR_APS_CTRL command on Page 0 sets the APS exiting conditions for Rail 1.

Command	MFR_APS_CTRL
Format	Unsigned binary

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:3	MIN_TIME_PS0	Sets the minimal full-phase running time when the VR exits APS for OCP_Phase, VFB- window, and FS limit events. This bit is active for both rails. 20µs/LSB.
2	APS_EXIT_UV_EN	When VFB falls below the VFB- window, the VR can be enabled to exit APS and run with full phase. 1'b0: disable VFB- window event to exit APS 1'b1: enable VFB- window event to exit APS
1	APS_EXIT_FS_EN	When the FS limit condition is met, the VR can be enabled to exit APS and run with full phase. The FS limit is set with PMBus commands 45h, 46h, 47h, 48h, and 49h. 1'b0: disable FS limit event to exit APS 1'b1: enable FS limit event to exit APS
0	APS_EXIT_OC_EN	When the Rail 1 phase 1 triggers OCP_Phase, the device can be enabled to exit APS and run with full phase. 1'b0: disable Rail 1 phase 1 OCP_Phase event to exit APS 1'b1: enable Rail 1 phase 1 OCP_Phase event to exit APS

MFR_OSR_SET (CDh) *(Page 0)*

The MFR_OSR_SET command on Page 0 sets the over-shot reduction (OSR) related parameters. This command is for Rail 1 only.

This register sets the minimum PWM off-time and block time of the OSR function on Rail 1.

Command	MFR_OSR_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	OSR_DEGLITCH_TIME						OSR_BLANK_TIME						

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	OSR_DEGLITCH_TIME	Sets the minimum PWM off-time in the OSR process. 5ns/LSB.
6:0	OSR_BLANK_TIME	Sets the blanking time between two OSR events. 10ns/LSB.

MFR_BLANK_TIME (CEh) *(Page 0)*

The MFR_BLANK_TIME command on Page 0 sets the slope compensation reset time and PWM blanking time between two consecutive phases. This command is for Rail 1 only.

Command	MFR_BLANK_TIME															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	SLOPE_RESET_TIME						PWM_BLANK_TIME					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	SLOPE_RESET_TIME	Sets the slope compensation resetting time. This bit is effective when register 2Ch bit[4] = 0. Note that the slope compensation reset time should be shorter than the PWM blanking time set by bit[5:0] (PWM_BLANK_TIME). 5ns/LSB.
5:0	PWM_BLANK_TIME	Sets the PWM blanking time between two consecutive phases. 5ns/LSB.

MFR_DDR_SET (CFh) *(Page 0)*

The MFR_DDR_SET command on Page 0 sets the DDR-related options when the MP2965 is used for memory power supply. This register is used to disable Rail 2's SVID address and 1/2 tracking mode.

Command	MFR_DDR_SET							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x		

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	REJ_SVID_ADDR2	Sets Rail 2 to reject any SVID command from the CPU. 1'b0: Rail 2 reacts to the SVID command sent to it 1'b1: Rail 2 rejects any SVID command from CPU
0	R2_HALF_TRK_EN	Enable bit for Rail 2 VOUT always tracking half of the Rail 1 VOUT. 1'b0: Rail 2 VOUT is independent of Rail 1 1'b1: Rail 2 VOUT is half of Rail 1 VOUT

MFR_SLOPE_SR_4P (D4h) *(Page 0)*

Slope compensation is used to provide enough noise immunity for PWM generation and make the PWM switches stable on the MP2965. Slope compensation is generated by a PMBus-programmable current source and a PMBus-programmable capacitor. The MP2965 provides a slope voltage programming command for any phase-count operation. The MFR_SLOPE_SR_4P command on Page 0 provides two bytes to program the slope compensation for 4-phase operation. This command is for Rail 1 only.

Command	MFR_SLOPE_SR_4P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

CCM operation can use same equation to calculate the slope slew rate, while the CURRENT_SOURCE and CAP value is programmed by a different register, shown in Equation (17):

$$SLOPE\_SR_{@NP} = 16892 \times \frac{CURRENT\_SOURCE}{(16 - CAP)} \quad (17)$$

Where $SLOPE\_SR_{@NP}$ is the slope voltage slew rate at n-phase CCM (in V/s). "N" is the phase count and can be 1~7.

Figure 31 shows a slope voltage curve at 4-phase CCM.

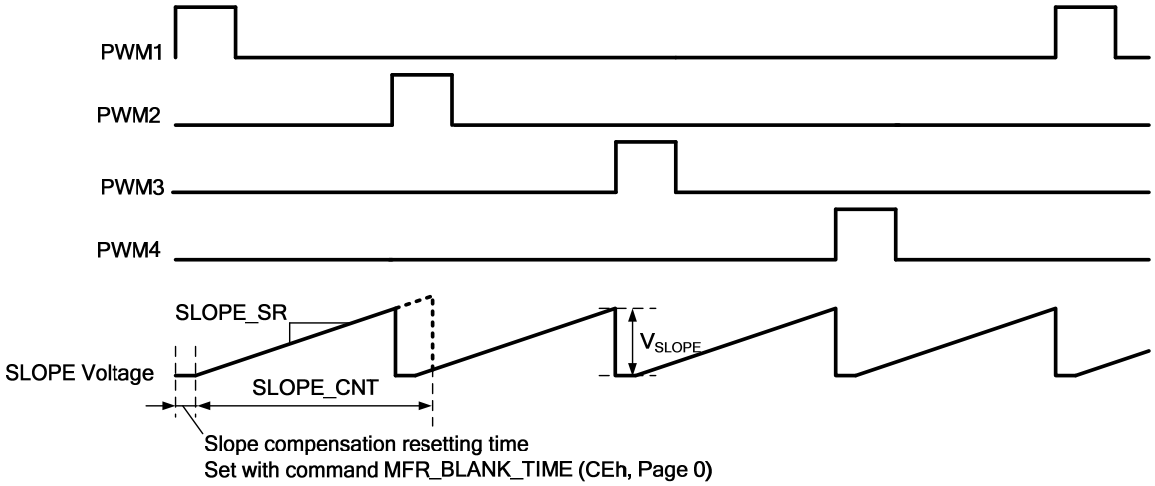


Figure 31: Slope Voltage at 4-Phase CCM

The slope voltage amplitude (V_{SLOPE}) can be calculated with Equation (18):

$$V_{SLOPE\_NP} = SLOPE\_SR_{@NP} \times \left(\frac{1}{N \times f_{SW}} - t_{RST}\right) \quad (18)$$

Where V_{SLOPE_NP} is the slope voltage of the N-phase CCM (in V), N is the phase count (between 1~7), $SLOPE\_SR_{@NP}$ is the slope voltage slew rate calculated with Equation (17), f_{SW} is the single-phase switching frequency set with command MFR_FS (Ech) (in Hz), and t_{RST} is the slope compensation resetting time set with command MFR_BLANK_TIME (Ceh) (in s).

In general design guidelines, a slope voltage amplitude (V_{SLOPE}) of 20mV to 40mV is used to cover all potential Ton, L, and Cout variations. A lower slope voltage results in faster load transient response, while a higher slope voltage results in better noise immunity (less PWM jittering).

MFR_SLOPE_CNT_4P (D5h) *(Page 0)*

The MFR_SLOPE_CNT_4P command on Page 0 is used to set the slope voltage clamp time at 4-phase operation. The clamp time is used to limit the slope voltage when the switching off-time is too long (e.g.: DCM operation or output load release transient). This command should cover the regular PWM switching off-time (see Figure 32). The slope voltage is clamped once the clamp timer expires, which means there is no more slope compensation. To provide enough time margin for slope compensation, it is recommend to design a slope clamp timer with the 130% of the switching off-time, as shown in Equation (19):

$$t_{SLOPE\_CLAMP} = 1.3 \times \left(\frac{1}{N \times f_{SW}} - t_{RST}\right) \quad (19)$$

Where t_{SLOPE_CLAMP} is the slope clamping timer (in s), f_{SW} is the single-phase switching frequency set with command MFR_FS (ECh) (in Hz), and t_{RST} is the slope compensation resetting time set with command MFR_BLANK_TIME (Ceh) (in s).

Command	MFR_SLOPE_CNT_4P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for 4-phase operation. 5ns/LSB.

MFR_SLOPE_SR_3P (D6h) *(Page 0)*

The MFR_SLOPE_SR_3P command on Page 0 provides two bytes to program the slope compensation slew rate for 3-phase operation. This command is for Rail 1 only. Use Equation (18) to calculate the slope voltage amplitude.

Command	MFR_SLOPE_SR_3P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_CNT_3P (D7h) *(Page 0)*

The MFR_SLOPE_CNT_3P command on Page 0 is used to set the slope voltage clamp time in 3-phase operation.

Command	MFR_SLOPE_CNT_3P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for 3-phase operation. 5ns/LSB.

MFR_SLOPE_SR_2P (D8h) *(Page 0)*

The MFR_SLOPE_SR_2P command on Page 0 provides two bytes to program the slope compensation for 2-phase operation. This command is for Rail 1 only. Use Equation (18) to calculate the slope voltage amplitude.

Command	MFR_SLOPE_SR_2P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB

MFR_SLOPE_CNT_2P (D9h) *(Page 0)*

The MFR_SLOPE_CNT_2P command on Page 0 is used to set the slope voltage clamp time in 2-phase operation.

Command	MFR_SLOPE_CNT_2P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for 2-phase operation. 5ns/LSB.

MFR_SLOPE_SR_1P (DAh) *(Page 0)*

The MFR_SLOPE_SR_1P command on Page 0 provides two bytes to program the slope compensation for 1-phase CCM operation. This command is for Rail 1 only. Use Equation (18) to calculate the slope voltage amplitude.

Command	MFR_SLOPE_SR_1P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x		CURRENT_SOURCE					

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_CNT_1P (DBh) *(Page 0)*

The MFR_SLOPE_CNT_1P command on Page 0 is used to set the slope voltage clamp time at 1-phase CCM operation.

Command	MFR_SLOPE_CNT_1P
Format	Unsigned binary

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for 1-phase CCM operation. 5ns/LSB.

MFR_SLOPE_SR_DCM (DCh) *(Page 0)*

The MFR_SLOPE_SR_DCM command on Page 0 sets the slew rate of slope compensation for Rail 1 at 1-phase DCM. Calculate the slope slew rate with Equation (17) with CAP = 0.

Command	MFR_SLOPE_SR_DCM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x	CURRENT_SOURCE					

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_CNT_DCM (DDh) *(Page 0)*

The MFR_SLOPE_CNT_DCM command on Page 0 is used to set the slope voltage clamp time at 1-phase DCM operation.

At 1-phase DCM, the off time is increased to reduce the switching frequency as the load current reduces. The slope voltage clamp time should be long enough to avoid the SW node freewheeling period when the zero-current detection (ZCD) turns off the low-side MOSFET to transition the SW node to Hi-Z (see Figure 32).

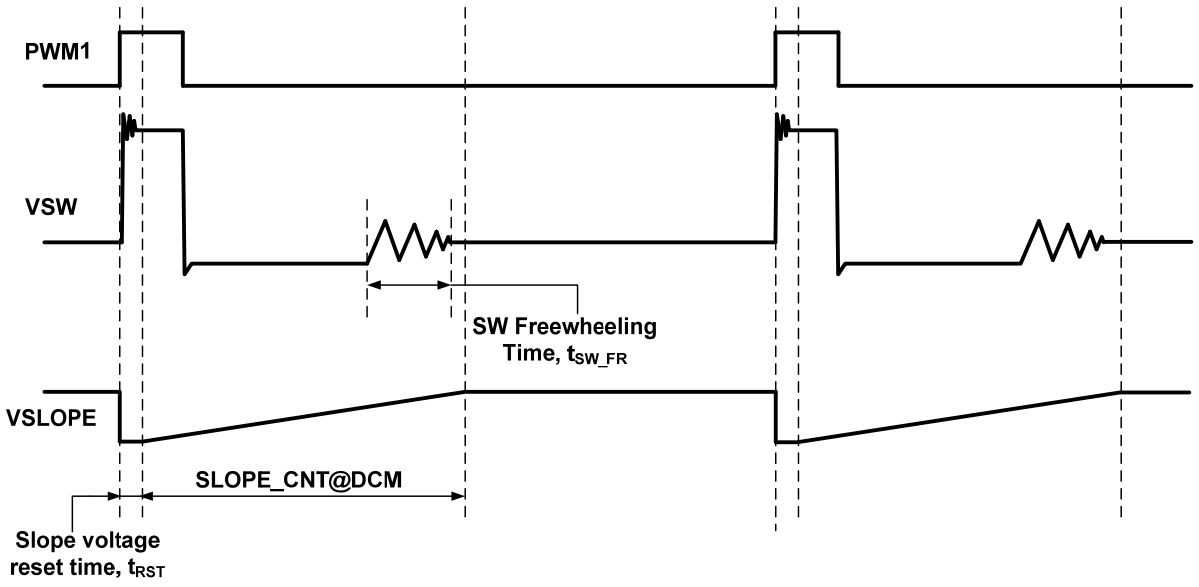


Figure 32: Slope Voltage Compensation at DCM

In general, it is recommend to design the slope clamp time for DCM operation using Equation (20):

$$t_{SLOPE\_CLAMP@DCM} = 1.1 \times \left(\frac{1}{f_{SW}} - t_{RST} + t_{SW\_FR} \right) \quad (20)$$

Where $t_{SLOPE\_CLAMT@DCM}$ is the slope clamp time at 1-phase DCM (in s), T_{SW} is the single-phase switching period set with command MFR_FS (Ech) (in s), t_{BLANK} is the PWM blanking time set with command MFR_BLANK_TIME (CEh) (in s), and t_{SW_FR} is the switch node freewheeling time (in s).

Command	MFR_SLOPE_CNT_DCM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for 1-phase DCM operation. 5ns/LSB.

MFR_SLOPE_TRIM1 (DEh) *(Page 0)*

When the DC loop is disabled, the actual V_{OUT} of the MP2965 can be calculated with Equation (21):

$$V_{OUT} = \frac{V_{REF} - V_{SLOPE}}{K_V} + \frac{\Delta V_{OUT}}{2} \quad (21)$$

Where V_{REF} is the reference voltage (in V), V_{SLOPE} is the slope voltage (in V), ΔV_{OUT} is the output voltage ripple (in V), and K_V is the output voltage divider, which may be caused by a remote sense amplifier sense gain or external VOSEN resistor divider.

The MP2965 provides a reference voltage trim (V_{TRIM}) to make the actual output voltage close the design target without DC loop calibration. V_{TRIM} is implanted by adding a negative offset over the reference voltage. In designs, design V_{TRIM} to equal to the voltage shift caused by V_{SLOPE} and the output voltage ripple. When SVID sets the PS command or when auto-phase shedding is enabled, the reference voltage trim also makes the DC loop output constant between different phases, improving the load transient response between different power states.

The MFR_SLOPE_TRIM1 command on Page 0 is used to trim the output voltage at 2-/1-phase CCM and 1-phase DCM of Rail 1.

Command	MFR_SLOPE_TRIM1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	VTRIM_2P					VTRIM_1P					VTRIM_DCM				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	VTRIM_2P	Sets the V_{OUT} trim for 2-phase operation. 2.35mV/LSB.
9:5	VTRIM_1P	Sets the V_{OUT} trim for 1-phase CCM operation. 2.35mV/LSB.

4:0	VTRIM_DCM	Sets the V_{OUT} trim for 1-phase DCM operation. 2.35mV/LSB.

MFR_SLOPE_TRIM2 (DFh) *(Page 0)*

The MFR_SLOPE_TRIM2 command on Page 0 is used to trim the output voltage at 5-/4-/3-phase operation of Rail 1.

Command	MFR_SLOPE_TRIM2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	VTRIM_5P					VTRIM_4P					VTRIM_3P				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	VTRIM_5P	Sets the V_{OUT} trim for 5-phase operation. 2.35mV/LSB.
9:5	VTRIM_4P	Sets the V_{OUT} trim for 4-phase operation. 2.35mV/LSB.
4:0	VTRIM_3P	Sets the V_{OUT} trim for 3-phase operation. 2.35mV/LSB.

MFR_SLOPE_TRIM3 (E0h) *(Page 0)*

The MFR_SLOPE_TRIM3 command on Page 0 is used to trim the output voltage at 7-/6-phase operation of Rail 1.

Command	MFR_SLOPE_TRIM3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	VTRIM_7P					VTRIM_6P				

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:5	VTRIM_7P	Sets the VOUT trim for 7-phase operation. 2.35mV/LSB.
4:0	VTRIM_6P	Sets the VOUT trim for 6-phase operation. 2.35mV/LSB.

MFR_ ADDR_PMBUS (E1h) *(Page 0)*

The MFR_ ADDR_PMBUS command on Page 0 sets the options related with a PMBus slave address.

Command	MFR_ ADDR_PMBUS															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x									
Bits	Bit Name				Description											
15:9	RESERVED				Unused. X indicates that writes are ignored and reads are always 0.											

8	ADDR_PH_MODE	This bit selects the 3MSB of the PMBus address to be set by the ADDR_PH pin or the register. 1'b0: 3MSB for PMBus address is set by ADDR_PH pin 1'b1: 3MSB for PMBus address is set by register MFR_PMBUS_ADDR (E1h) bit[6:4]
7	ADDR_PL_SET	This bit selects the 4LSB of the PMBus address to be set by the ADDR_PL pin or the register. 1'b0: 4LSB for PMBus address is set by ADDR_PL pin 1'b1: 4LSB for PMBus address is set by register MFR_PMBUS_ADDR (E1h) bit[3:0]
6:4	ADDR_PMBUS_3MSB	Sets or returns the 3MSB of the PMBus address. When bit[8] = 1'b0, the PMBus address 3MSB is set by ADDR_PH pin. Bit[6:4] returns the 3MSB of the PMBus address. When bit[7] = 1'b1, the 3MSB of PMBus address is set with bit[6:4].
3:0	ADDR_PMBUS_4LSB	Sets or returns the 4LSB of the PMbus address. When bit[7] = 1'b0, the PMBus address 4LSB is set by ADDR_PL pin. Bit[3:0] returns the 4LSB of the PMBus address. When bit[7] = 1'b1, the 4LSB of PMBus address is set with bit[3:0].

MFR_LOOP_PI_SET (E2h) *(Page 0)*

The MFR_LOOP_PI_SET command on Page 0 sets the Rail 1 V_{OUT} PMBus report resolution and PI parameters of the DC loop and current balance loop.

Command	MFR_LOOP_PI_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x		DC_LOOP_KI						CB_LOOP_KI			

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	VOUT_PMBUS_LSB	Sets the resolution of the PMBus V_{OUT} report with command READ_VOUT (8Bh). 1'b0: VID format 1'b1: 1mV/LSB
9:4	DC_LOOP_KI	Sets the PI parameter of the DC calibration loop.
3:0	CB_LOOP_KI	Sets the PI parameter of the current balance loop.

MFR_CB_LOOP_CTRL (E3h) *(Page 0)*

The MFR_CB_LOOP_CTRL command on Page 0 sets the current balance loop holding time and conditions for Rail 1.

Command	MFR_CB_LOOP_CTRL							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function					CB_LOOP_THOLD			
Bits	Bit Name		Description					

7	CB_TRANS_ HOLD_EN	Holds the current balance loop regulation when a load transient event is detected (i.e.: VFB exceeds the VFB+ or VFB- window). 1'b0: no action 1'b1: hold the current balance loop regulation when a load transient event is detected
6	CB_PRD_HOLD_EN	Holds the current balance loop when the PWM time interval meets the PWM switching period condition set with the PMBus command MFR_DC_LOOP_CTRL (CBh) bit[13:7]. 1'b0: no action 1'b1: hold the current balance loop when the PWM switching period condition is met
5	CB_PS_HOLD_EN	Holds the current balance loop when a phase count is changed. 1'b0: no action 1'b1: hold the current balance loop when the phase count is changed
4	CB_DVID_HOLD_EN	Holds the current balance loop when DVID occurs. 1'b0: no action 1'b1: hold the current balance loop when DVID occurs
3:0	CB_LOOP_THOLD	Sets the current balance loop holding time. During a load transient event, FS change event, power state changing, or a DVID event is detected and the corresponding enable bit is set, the current balance loop stops regulating for a period of time set with command CB_LOOP_THOLD. 100μs/LSB.

MFR_VR_CONFIG (E4h) *(Page 0)*

The MFR_VR_CONFIG command on Page 0 provides two bytes to program some basic system configurations of Rail 1.

Command	MFR_VR_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function														PHASE_CNT		

Bits	Bit Name	Description
15	DC_LOOP_EN_DCM	Enables DC loop calibration at DCM. 1'b0: disable DC loop calibration at DCM 1'b1: enable DC loop calibration at DCM
14	DC_LOOP_EN	Enables DC loop calibration in both DCM and CCM operation. 1'b0: disable DC loop calibration 1'b1: enable DC loop calibration
13	PSI_SEL	Enables forcing the power state. This bit is only effective when OPERATION (01h), bit [5:4] ≠ 2'b11. 1'b0: disable forcing power state with bit[12:11] of MFR_VR_CONFIG (E4h) 1'b1: enable forcing power state with bit[12:11] of MFR_VR_CONFIG (E4h)
12:11	PSI_PMBUS	Power state selection bits when MFR_VR_CONFIG (E4h) bit[13] = 1. 2'b00: full-phase CCM. The phase count is determined by MFR_VR_CONFIG (E4h) bit[2:0]. 2'b01: 1-phase CCM 2'b1x: 1-phase DCM

10	OVER_CLOCK1_EN	Enable over-clocking mode 1 (i.e.: adding an offset voltage over VID with the PMBus command VOUT_OFFSET (23h)). This bit is effective at SVID, PMBus, AVSBus, and PVID override mode. 1'b0: disable over-clocking mode 1. The VOUT_OFFSET (23h) is ineffective, and the VID offset from the SVID interface is effective. 1'b1: enable over-clocking mode 1. The PMBus command VOUT_OFFSET (23h) is active and added to the initial VID. The VID offset from SVID is ineffective.
9	DCM_TON_SET	Sets the PWM on time at DCM operation. 1'b0: PWM on time at DCM is the same as in CCM operation 1'b1: PWM on time at DCM is 3/4 that of CCM operation
8	VID_STEP_SEL	Selects the Rail 1 VID resolution. All PMBus commands on Page 0 in VID format follow the VID resolution definition with VID_STEP_SEL. 1'b0: 10mV per VID step 1'b1: 5mV per VID step
7	CB_LOOP_EN	Enables the current balance loop. 1'b0: disable current balance loop 1'b1: enable current balance loop
6	OSR_EN	Enables the overshoot reduction function. 1'b0: disable overshoot reduction function 1'b1: enable overshoot reduction function
5:4	APS_IVID_EN	Enables auto-phase shedding and IVID. 2'b00: disable APS and IVID 2'b01: enable IVID 2'b1x: enable APS
3	SVID_OVERCLK2_EN	Enable over-clocking mode 2 at SVID mode. 1'b0: disable SVID over-clocking mode 2 1'b1: enable SVID over-clocking mode 2. The VID is determined by the PMBus command VOUT_COMMAND (21h), but the MP2965 still responds to all CPU SVID commands.
2:0	PHASE_CNT	Sets the full-phase count of Rail 1 when MFR_VR_CONFIG (E4h) bit[12:11] = 2'b00. 3'b000: 1-phase DCM 3'b001: 1-phase CCM 3'b010: 2-phase 3'b011: 3-phase 3'b100: 4-phase 3'b101: 5-phase 3'b110: 6-phase 3'b111: 7-phase

MFR _VBOOT_SET (E5h) *(Page 0)*

The MFR_VBOOT_SET command on Page 0 programs the boot-up voltage if VBOOT is set with the register. This command also provides a bit to enable IMVP9 VID table format.

Command	MFR_VBOOT_SET															
Format	Unsigned binary, VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x		VBOOT_SET							

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	IMVP9_EN	Enables IMVP9 VID table format. 1'b0: disable IMVP9 VID table format 1'b1: enable IMVP9 VID table format
7:0	VBOOT_SET	Sets the boot-up voltage of Rail 1 when VBOOT is set with the register (i.e.: MFR_VR_CONFIG2 (09h) bit[12:11] = 2'b00). This bit is in VID format. 1 VID step/LSB.

MFR _ADDR_SVID_AVSBUS (E6h) *(Page 0)*

The MFR_ADDR_SVID_AVSBUS command on Page 0 sets the SVID and AVS address for both rails.

Command	MFR_ ADDR_SVID_AVSBUS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x					ADDR_OFFSET						SVID_AVS_ADDR1			

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	AVS_ADDR_EN1	Enables the AVSbus address of Rail 1. 1'b0: disable AVSBus address of Rail 1 1'b1: enable AVSBus address of Rail 1
12	AVS_ADDR_EN2	Enables the AVSbus address of Rail 2. 1'b0: disable AVSBus address of Rail 2 1'b1: enable AVSBus address of Rail 2
11:10	SVID_ALLCALL_CTRL	Selects the SVID all-call address. 2'b00: no all-call address 2'b01: SVID address 0x0E as all-call address 2'b10: SVID address 0x0F as all-call address 2'b11: SVID address 0x0E and 0x0F as all-call address
9:5	ADDR_OFFSET	Sets the Rail 2 SVID/AVSBus address offset based on Rail 1. It is in two's complement format. The Rail 2 SVID/AVSBus address can be calculated with the following equation: ADDRS_R2 = ADDRS_R1 + ADDR_OFFSET + 1 The values below list the binary data and real-world address offset: 5'b 0 0000: 0 5'b 0 0001: 1 5'b 0 1111: 15 5'b 1 0000: -16 5'b 1 0001: -15 5'b 1 1111: -1
4	SVID_AVS_ADDR_ MODE	Selects the SVID/AVSBus address setting mode from the register. 1'b0: not supported 1'b1: SVID/AVSBus address is from register E6h bit[3:0]
3:0	SVID_AVS_ADDR1	When bit [4] = 1, set the SVID/AVSBus address from the register.

MFR_IIN_CAL_GAIN (E7h) *(Page 0)*

The MFR_IIN_CAL_GAIN command on Page 0 set the input current sensing gain.

Command	MFR_IIN_CAL_GAIN															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	IIN_CAL_GAIN								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	IIN_CAL_GAIN	Sets the input current sensing gain. $IIN\_GAIN = 4100 \times \frac{R_{IIN} \times R_{IIN\_SEN}}{R_{I/V}}$ Where R_{IIN} is the resistor on IIN (in Ω), R_{IIN_SEN} is the current sensing resistor (in Ω), and $R_{I/V}$ is the input current converting resistor (in Ω). Refer to Figure 15 for a detailed definition.

MFR_TEMP_CAL (E8h) *(Page 0)*

The MFR_TEMP_CAL command on Page 0 sets the temperature sensing gain and offset.

Command	MFR_TEMP_CAL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TEMP_GAIN								TEMP_OFFSET							

Bits	Bit Name	Description
15:8	TEMP_GAIN	Sets the temperature sense gain to transfer the voltage to VTEMP to direct temperature (in degrees).
7:0	TEMP_OFFSET	Sets the temperature sense offset to transfer the voltage to VTEMP to direct temperature (in degrees). This bit is in two's complement format. Bit[7] is the sign bit. The list below shows the binary data and real-world values: 8'b 0000 0000: 0 8'b 0000 0001: 1°C 8'b 0111 1111: 127°C 8'b 1000 0000: -128°C 8'b 1000 0001: -127°C 8'b 1111 1111: -1°C

The MP2965 senses the power stage temperature by sensing the voltage of VTEMP. Intelli-Phases report the junction temperature to VTEMP. TEMP_GAIN and TEMP_OFFSET are used to program the junction temperature gain and offset of VTEMP into the MP2965. Generally, the Intelli-Phase junction temperature is calculated with Equation (22):

$$T_{JUNCTION}(°C) = a \times V_{TEMP} + b \quad (22)$$

Where V_{TEMP} is the voltage on the MP2965 VTEMP pin (in V), a is the temperature sense gain (in °C/V), and b is the temperature sense offset (in °C).

TEMP_GAIN and TEMP_OFFSET are determined by TEMP_OFFSET = b and TEMP_GAIN = 0.8×a.

MFR_CUR_GAIN (E9h) *(Page 0)*

The MFR_CUR_GAIN command on Page 0 sets the Rail 1 phase current sensing gain. The MP2965 senses the phase current by monitoring the voltage between CS and CS_SUM. The gain affects the per-phase current limit. The relationship of the current sensing gain/offset and the actual phase current limit is shown in Equation (23):

$$0.01\times\left(\frac{PHASE\_CUR\_GAIN\times OCP\_PHASE}{82}+106+PHASE\_CUR\_OFFSET\right)+0.17=I_{PH\_LMT}\times R_{CS}\times K_{CS}+1.23 \quad (23)$$

Command	MFR_CUR_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	PHASE_CUR_GAIN									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	PHASE_CUR_GAIN	Sets the phase current sensing gain with the following equation: $PHASE\_CUR\_GAIN=8200\times R_{CS}\times K_{CS}$ Where R_{CS} is the phase-current sensing resistor (in Ω), and K_{CS} is the current sensing gain of Intelli-Phase (in A/A).

MFR_FS_LOOP_CTRL (EBh) *(Page 0)*

The MFR_FS_LOOP_CTRL command on Page 0 sets frequency loop hold time and conditions for Rail 1.

Command	MFR_FS_LOOP_CTRL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	FS_TRANS_HOLD_EN	Holds the frequency loop regulation when a load transient event is detected (i.e.: VFB exceeds the VFB+ or VFB- window). 1'b0: no action 1'b1: hold frequency loop regulation when a load transient event is detected
13	FS_PS_HOLD_EN	Holds the frequency loop regulation when the phase count is changed. 1'b0: no action 1'b1: hold frequency loop regulation when phase count is changed
12	FS_DVID_HOLD_EN	Holds the frequency loop regulation when DVID occurs. 1'b0: no action 1'b1: hold frequency loop regulation when DVID occurs
11:8	FS_LOOP_HOLD_TIME	Sets the minimal holding time of the frequency loop when a load transient, phase count change, or DVID occurs. 100μs/LSB.

7	FS_LOOP_EN	Enables the frequency loop. 1'b0: disable frequency loop 1'b1: enable frequency loop
6:0	FS_LOOP_KI	Sets the frequency loop regulation parameter.

MFR_FS (ECh) *(Page 0)*

The MFR_FS command on Page 0 sets the switching frequency of Rail 1.

Command	MFR_FS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	MFR_FS								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	MFR_FS	Sets the switching frequency in a direct format. 10kHz/LSB.

MFR_OTP_SET (EDh) *(Page 0)*

The MFR_OTP_SET command on Page 0 sets the over-temperature protection (OTP) mode, threshold, and hysteresis. OTP is achieved by sensing the temperature on VTEMP.

Command	MFR_OTP_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	OTP_LIMIT									OTP_HYS						

Bits	Bit Name	Description
15:8	OTP_LIMIT	Sets the over-temperature protection threshold. 1° C/LSB.
7	OTP_MODE	Sets the over-temperature protection mode. 1'b0: hiccup mode 1'b1: latch mode
6:0	OTP_HYS	Sets the over-temperature protection recovery threshold when OTP is set to hiccup mode. 1°C/LSB.

MFR_OCP_TOTAL_SET (EEh) *(Page 0)*

The MFR_OCP_TOTAL_SET command on Page 0 sets the Rail 1 OCP_Total-related options and values.

Command	MFR_OCP_TOTAL_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x			OCP_TOTAL_TBLANK						OCP_TOTAL_CUR						

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

14:13	OCP_TOTAL_MODE	Sets the OCP_Total action mode. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
12:7	OCP_TOTAL_TBLANK	Sets the blanking time for OCP_Total in direct format. 100μs/LSB.
6:0	OCP_TOTAL_CUR	Sets the Rail 1 per-phase OCP_Total entry threshold in direct format. 1A/LSB.

MFR_VCCIO_FAULT_SET (EFh) *(Page 0)*

The MFR_VCCIO_FAULT_SET command on Page 0 sets the VCCIO fault-related options and values. If the MP2965 detects that VCCIO is lower than 0.65V for longer than the VCCIO fault blanking time, the VR shuts down.

Command	MFR_VCCIO_FAULT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x									

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	VCCIO_FLT_MODE	Sets the VCCIO fault action mode. 1'b0: auto-retry mode 1'b1: latch mode
7	VCCIO_FAULT_EN2	Enables the VCCIO fault on Rail 2. 1'b0: disable VCCIO fault on Rail 2 1'b1: enable VCCIO fault on Rail 2
6	VCCIO_FAULT_EN1	Enables the VCCIO fault on Rail 1. 1'b0: disable VCCIO fault on Rail 1 1'b1: enable VCCIO fault on Rail 1
5:0	VCCIO_FLT_TBLANK	Sets the VCCIO fault blanking time. If VCCIO is below 0.65V for longer than the time set with VCCIO_FLT_TBLANK, a VCCIO fault occurs. 50ns/LSB.

MFR_OCP_PHASE_SET (F0h) *(Page 0)*

The MFR_OCP_PHASE_SET command on Page 0 sets the Rail 1 per-phase valley current limit.

Command	MFR_OCP_PHASE_SET							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	PHASE_CUR_LIMIT						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	PHASE_CUR_LIMIT	Sets the per-phase valley current limit in direct format. 1A/LSB.

MFR_OVP_UVP_SET (F1h) *(Page 0)*

The MFR_OVP_UVP_SET command on Page 0 provides two bytes to program the options and values of Rail 1 V_{OUT} OVP and UVP.

Command	MFR_OVP_UVP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function				OVP2_BLANK_TIME							UVP_BLANK_TIME					

Bits	Bit Name	Description
15:14	OVP2_MODE	Selects the OVP2 action mode. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry three or six times, determined by bit[13] below
13	OVP2_RETRY_TIMES	Sets the number of retry times when bit[15:14] (OVP2_MODE) = 2'b11. 1'b1: retry three times 1'b0: retry six times
12:8	OVP2_BLANK_TIME	Sets the OVP2 blanking time. When the OV2 condition remains for longer than the OVP2 blanking time, the OVP2 fault takes action. 100ns/LSB.
7:6	UVP_MODE	Selects the UVP action mode. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
5:0	UVP_BLANK_TIME	Sets the UVP blanking time. When the UV condition remains for longer than the UVP blanking time, the UVP fault takes action. 20μs/LSB.

PWD_CHECK_CMD (F2h) *(Page 0)*

The PWD_CHECK_CMD command on Page 0 provides two bytes to input the password and check if it is effective. If the password input is mismatched with the value set with the PMBus command MFR_PWD_USER (A7h, Page 1), the PMBus commands and EEPROM cannot read or write.

Command	PWD_CHECK_CMD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PWD_CHECK_INPUT															

Bits	Bit Name	Description
15:0	PWD_CHECK_INPUT	Command to input and check the password value.

MFR_FAULTS1 (FCh) *(Page 0)*

The MFR_FAULTS1 command on Page 0 provides two bytes to return the fault type of the present power cycle. The fault bits are in latch mode. They can be cleared by the OPERATION command off/on, EN off/on, or by recycling the power of VDD33.

Command	MFR_FAULTS1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x		CS_FAULT_TRG												

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	VTEMP_FAULT_TRG	VTEMP pin fault indicator. When the voltage on the VTEMP pin is higher than 1.25V, this bit indicates that a fault has been triggered. 1’b0: no VTEMP fault 1’b1: a VTEMP fault has occurred
12:10	CS_FAULT_TRG	CS_FAULT indicators. 3’b000: no CS fault is detected 3’b001: a CS fault has been detected on pin CS1 3’b010: a CS fault has been detected on pin CS2 3’b011: a CS fault has been detected on pin CS3 3’b100: a CS fault has been detected on pin CS4 3’b101: a CS fault has been detected on pin CS5 3’b110: a CS fault has been detected on pin CS6 3’b111: a CS fault has been detected on pin CS7
9	VIN_OV_FLAG	VIN_OV fault indicator. 1’b0: no VIN_OV fault 1’b1: a VIN_OV fault has occurred
8	VIN_UVLO_FLAG	VIN_UVLO fault indicator. 1’b0: no VIN_UVLO fault 1’b1: a VIN_UVLO fault has occurred
7	VCCIO_FLAG	VCCIO fault indicator. 1’b0: no VCCIO fault 1’b1: a VCCIO fault has occurred
6	OTP_FLAG	Power stage over-temperature indicator. 1’b0: no power stage over-temperature fault has been detected on VTEMP 1’b1: an over-temperature fault has been detected on VTEMP
5	OVP_FLAG1	Rail 1 VOUT OVP fault indicator. 1’b0: no VOUT OV fault 1’b1: a VOUT OV fault has occurred
4	UVP_FLAG1	Rail 1 VOUT UVP fault indicator. 1’b0: no VOUT UV fault 1’b1: a VOUT UV fault has occurred
3	OCP_FLAG1	Rail 1 OCP_Total fault indicator. 1’b0: no OCP_Total fault 1’b1: an OCP_Total fault has occurred
2	OVP_FLAG2	Rail 2 VOUT OVP fault indicator. 1’b0: no VOUT OV fault 1’b1: a VOUT OV fault has occurred
1	UVP_FLAG2	Rail 2 VOUT UVP fault indicator. 1’b0: no VOUT UV fault 1’b1: a VOUT UV fault has occurred

0	OCP_FLAG2	Rail 2 OCP_Total fault indicator. 1'b0: no OCP_Total fault 1'b1: an OCP_Total fault has occurred

MFR_FAULTS2 (FDh) *(Page 0)*

The MFR_FAULTS2 command provides two bytes to return the PWM fault type of the present power cycle. The fault bits are in latch mode. They can be cleared by the OPERATION command off/on, EN off/on, or by recycling the power of VDD33.

Command	MFR_FAULTS2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	PWM1_FAULTS				PWM2_FAULTS				PWM3_FAULTS				PWM4_FAULTS			

Bits	Bit Name	Description
15:12	PWM1_FAULTS	Intelli-Phase fault type indication of phase 1. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM2_FAULTS	Intelli-Phase fault type indication of phase 2. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM3_FAULTS	Intelli-Phase fault type indication of phase 3. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM4_FAULTS	intelli-Phase fault type indication of phase 4. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: curren- limit protection 4'b0100: over-temperature protection 4'b1000: SW-GND short protection

MFR_FAULTS3 (FEh) *(Page 0)*

The MFR_FAULTS3 command provides two bytes to return the PWM fault type of the present power cycle. The fault bits are in latch mode. They can be cleared by the OPERATION command off/on, EN off/on, or by recycling the power of VDD33.

Command	MFR_FAULTS3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	PWM5_FAULTS				PWM6_FAULTS				Reserved				PWM7_FAULTS			

Bits	Bit Name	Description
15:12	PWM5_FAULTS	Intelli-Phase fault type indication of phase 5. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM6_FAULTS	Intelli-Phase fault type indication of phase 6. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
7:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	PWM7_FAULTS	Intelli-Phase fault type indication of phase 7. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection

CLEAR_EEPROM_FAULTS (FFh) *(Page 0)*

This command is used to clear the EEPROM fault. This command is write only. There is no data byte for this command.

PAGE 1 REGISTER MAP

PAGE (00h) *(Page 1)*

The PAGE command provides the ability to configure, control, and monitor all registers, including test mode and the EEPROM, through only one physical address.

Command	PAGE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	PAGE					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	PAGE	Registers page selector. 0x00: Page 0, all PMBus commands address operating registers on Page 0 0x01: Page 1, all PMBus commands address operating registers on Page 1 0x02: Page 2, all PMBus commands address the test mode registers 0x28: Page 28, all PMBus commands address the EEPROM registers (00h~FFh) 0x29: Page 29, all PMBus commands address the EEPROM registers (100h~1FFh) Others: ineffective Note: MFR_EEPROM_CTRL (06h) bit[2] (EE_WORD_WR_EN) determines if Page 28/29 is accessible or not. EE_WORD_WR_EN = 0: Page 28/29 is not accessible EE_WORD_WR_EN = 1: Page 28/29 is accessible

OPERATION (01h) *(Page 1)*

The OPERATION command on Page 1 is used to turn the Rail 2 output on/off in conjunction with the input from EN2. It also provides two bits to set the output voltage to follow PMBus VOUT_COMMAND (21h), remain at a MARGIN high/low level, or follow the AVSBus interface. It also provides one bit to enable VOUT_COMMAND (21h), even in AVSBus override.

Command	OPERATION							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function					x	x		x

Bits	Bit Name	Description
7:6	OPERATION_MODE	Operation mode. 2'b00: Hi-Z off 2'b01: soft off 2'b1x: on
5:4	AVSBUS_EN	Selects the VID override mode between PMBus and AVSBus mode 2'b00: PMBus override mode, V_{OUT} is determined by VOUT_COMMAND 2'b01: PMBus margin low 2'b10: PMBus margin high 2'b11: AVSBus override mode
3:2, 0	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	AVS_PMBUS_CTRL	Enables VOUT_COMMAND (21h) to control the VID at AVSBus mode. 1'b0: PMBus command VOUT_COMMAND (21h) will not change the VID value 1'b1: VID can be changed by the PMBus command VOUT_COMMAND

CLEAR_FAULTS (03h) *(Page 1)*

The CLEAR_FAULTS command is used to clear any fault bit in all statuses and fault registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), and STATUS_CML (7Eh).

This command is write only. There is no data byte for this command.

MFR_LINE_FLOAT_EN (04h) *(Page 1)*

The MFR_LINE_FLOAD_EN command on Page 1 provides two bits to enable line-float protection on both Rail 1 and Rail 2.

Command	MFR_LINE_FLOAT_EN							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x		

Bits	Bit Name	Description
7:2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1	VOSEN_FLOAT_EN	Enables VOSEN line-float detection and protection. 1'b0: disable 1'b1: enable VOSEN line-float detection and protection
0	VORTN_FLOAT_EN	Enables VORTN line-float detection and protection. 1'b0: disable 1'b1: enable VORTN line-float detection and protection

BIOS UPDATE (05h) *(Page 1)*

The BIOS_UPDATE command is used to update the phase number and MFR_FS (ECh) value while the VR is outputting power. When the bios updates, the VR is commanded to calculate the on time with Equation (1) immediately.

This command is write only. There is no data byte for this command.

MFR_VR_CONFIG2 (09h) *(Page 1)*

The MFR_VR_CONFIG2 command on Page 1 sets the Rail 2 VBOOT-related options, PVID and PMBus override mode, and Hi-Z shutdown voltage level. The Hi-Z shutdown voltage level is effective only when VID slews down to 0V. VID slewing down to 0 may be caused by a soft off or DVID to 0V. Once the VID-DAC output is lower than the Hi-Z shutdown voltage level, the PWM enters tri-state. The output voltage is discharged by the load current naturally (see Figure 27).

Command	MFR_VR_CONFIG2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x				VID_SHUT_DOWN								

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

11	BOOT_MODE_SEL	Selects the boot-up voltage from the register or pin. Sets the PMBus boot-up voltage options. 1'b0: PMBus VBOOT is from register MFR_VBOOT (E5h) 1'b1: PMBus VBOOT is from the pin. BOOT is assigned by bit[13] in this command.
10	PVID_EN	Enables Rail 1 PVID mode. 1'b0: disable PVID mode 1'b1: enable PVID mode
9	PMBUS_EN	Enables PMBus override mode. 1'b0: disable PMBus override mode 1'b1: enable PMBus override mode
8:0	VID_SHUT_DOWN	VID threshold at which all PWMs go into tri-state when VID slews to 0V. This bit is in direct format with VID resolution. 1 VID step/LSB.

MFR_VID_SLEW_SLOW (0Dh) *(Page 1)*

THE MFR_VID_SLEW_SLOW COMMAND ON Page 1 SELECTS THE Rail 2 VID TRANSITION SLOW SLEW RATE. This command IS PROPORTIONAL WITH the VID FAST SLEW RATE, WHICH IS SET WITH COMMAND MFR_VID_SLEW_FAST (0EH). THE VID SLOW SLEW RATE DEFINES THE VID SLEW RATE during BOOT_UP, OPERATION COMMAND SOFT_OFF, AND SVID INTERFACE SET VID SLOW COMMAND.

Command	MFR_VID_SLEW_SLOW							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x			SLEW_SLOW_SR			

Bits	Bit Name	Description
7:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	SLEW_SLOW_SR	4'b1xxx: SLEW_SLOW_SR = FAST_SR/16 4'b01xx: SLEW_SLOW_SR = FAST_SR/8 4'b001x and 4'b0000: SLEW_SLOW_SR = FAST_SR/4 4'b0001: SLEW_SLOW_SR = FAST_SR/2 Where FAST_SR is the VID fast slew rate defined in register MFR_VID_SLEW_FAST (0Eh) bit[5:0]. The value of "x" does not matter.

MFR_VID_SLEW_FAST (0Eh) *(Page 1)*

The MFR_VID_SLEW_FAST command on Page 1 sets the VID fast slew rate and extra VID steps when VID is ramping up. The fast slew rate defines the VID slew rate at the SVID interface, Set VID Fast command, and EN soft-off slew rate.

Command	MFR_VID_SLEW_FAST															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x			SLEW_FAST_CNT					

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

7:6	VID_PLUS_STEP	Sets the count of extra VID steps when DVID is up. The extra VID steps are used to compensate for the droop voltage caused by charging output capacitor during DVID up. This bit is effective only after the boot-up voltage is settled. 1 VID step/LSB.
5:0	SLEW_FAST_CNT	Sets the VID fast slew rate by setting the time interval of each VID step. It is in direct format. 50ns/LSB. The slew rate can be calculated with the equation below: $FAST\_SR(mV/\mu s) = \frac{VID\_STEP(mV)}{SLEW\_FAST\_CNT \times 0.05(\mu s)}$ Where VID_STEP is in 5mV or 10mV. It is determined by bit[8] of MFR_VR_CONFIG (E4h).

STORE_USER_ALL (15h) *(Page 1)*

The STORE_USER_ALL command instructs the PMBus device to copy the Page 0 and Page 1 contents of the operating memory to the matching locations in the EEPROM. During the copying process, the device calculates the CRC for all saved bits and saves the CRC result into the EEPROM. The CRC codes is used to check if the data is valid or not at the next power-up or restore.

This command is write only. There is no data byte for this command.

RESTORE_USER_ALL (16h) *(Page 1)*

The RESTORE_USER_ALL command instructs the PMBus device to copy the Page 0 and Page 1 contents from the EEPROM and overwrite the matching locations in the operating memory. In this process, the device calculates the CRC for all restored bits. If the calculated CRC is not matching with the CRC value saved in the EEPROM, the device reports the CRC error via bit[4] of register STATUS_CML (7Eh). The CRC error protection can be enabled by bit[0] of MFR_EEPROM_CTRL (1Dh).

After the power-on reset (POR), the device triggers the memory copy operation from the EEPROM. This process is the same as the operating RESTORE_USER_ALL command.

It is *not* permitted to send the RESTORE_USER_ALL command while the device is outputting power; otherwise, the command will be ignored.

This command is write only. There is no data byte for this command.

MFR_PWM_TIME_LIMIT (1Eh) *(Page 1)*

This MFR_PWM_TIME_LIMIT command on Page 1 sets the PWM minimum on-time and minimum off-time for Rail 2.

Command	MFR_PWM_TIME_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	TON_LIMIT_TO_VCAL				MIN_ON_TIME			MIN_OFF_TIME				

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:8	TON_LIMIT_TO_VCAL	The DC loop is held if the PWM period meets the condition set in MFR_DC_LOOP_CTRL (CBh) bit[13:7]. However, if the PWM on time calculated with Equation (1) is less than the time set by TON_LIMIT_TO_VCAL, the DC loop is always in regulation, so TON_LIMIT_TO_VCAL is used to set the on-time threshold that holds the DC loop calibration. 5ns/LSB.

7:5	MIN_ON_TIME	Sets the PWM minimum on-time. 5ns/LSB.
4:0	MIN_OFF_TIME	Sets PWM minimum off-time with 15ns offset. 20ns/LSB. The minimum off-time of Rail 1 can be calculated with: $PWM\_MIN\_OFF\_TIME(ns) = MIN\_OFF\_TIME \times 50(ns) + 15(ns)$

MFR_VR_CONFIG4 (1Fh) *(Page 1)*

The MFR_VR_CONFIG4 command on Page 1 sets some basic configurations for Rail 2.

Command	MFR_VR_CONFIG4															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x	x	x				

Bits	Bit Name	Description
15:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3	IOUT_DGTL_FLT_EN	Enables the IMON analog filter internal IC. 1'b0: no IMON analog filter 1'b1: IMON analog filter is enabled
2	OVP/OCP_PHASE/ COMP_DAC_DBG	Enables V_{OUT} OVP/OCP_Phase/COMP DAC debug mode. Once in enable debug mode, the OVP threshold, OCP_Phase limit, and VCOMP DAC input can be set with specific registers. The associated register setting on Page 1 is not effective anymore. This bit is for ATE trimming. 1'b0: normal mode 1'b1: enable V_{OUT} OVP/OCP_Phase/COMP DAC debug mode. The OCP_Phase limit is directly from register F0h bit[7:0] on Page 1 with 10mV/LSB. The V_{OUT} OV threshold is directly from register 24h bit[8:0] on Page 1 with 10mV/LSB. V_{COMP} is directly from register 6Ch bit[7:0] on Page 2 with 1.37mV/LSB.
1:0	DECAY_LENGTH	Sets the maximum time of each VID step in decay mode. It is used to set the minimum decay slew rate. VID is forced to ramp down one VID step once the present VID step is longer than the time set by DECAY_LENGTH. 100ns/LSB.

VOUT_COMMAND (21h) *(Page 1)*

The VOUT_COMMAND command on Page 1 set the reference voltage VID at PMBus override mode and over-clocking2 mode at AVSBus and SVID override mode. This register is used to set the output voltage on-the-fly for PMBus VID override mode on Rail 2.

Command	VOUT_COMMAND															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	VOUT_COMMAND								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_COMMAND	Sets the reference voltage VID at PMBus override mode. It is in VID format with 5mV or 10mV per step. The VID resolution is determined by bit[8] of MFR_VR_CONFIG (E4h). 1 VID step/LSB.

VOUT_TRIM (22h) *(Page 1)*

The VOUT_TRIM command on Page 1 instructs the device to fine-tune the Rail 2 output voltage with 0.7mV/LSB. The VOUT_TRIM is added to the remote sense amplifier output to change the final output voltage. Note that the output PMBus reported value in READ_VOUT (8Bh) is not affected by VOUT_TRIM. VOUT_TRIM can be used to fine-tune the output voltage.

Command	VOUT_TRIM															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	VOUT_TRIM						

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	VOUT_TRIM	Fine-tune the output voltage. This bit is in two's complement format. The resolution is related with the VDIFF gain set by VOUT_SENSE_SET (29h, bit[11]). 0.5mV/LSB with VDIFF unit gain 0.8mV/LSB with VDIFF half gain The table below shows the binary data and real-world value.

VOUT_TRIM	VDIFF Unit Gain	VIDFF Half Gain
7'b 000 0000	0	0
7'b 000 0001	+0.5mV	+0.8mV
7'b 011 1111	+31.5mV	+50.4mV
7'b 100 0000	-32mV	-51.2mV
7'b 100 0001	-31.5mV	-50.4mV
7'b 111 1111	-0.5mV	-0.8mV

VOUT_OFFSET (23h) *(Page 1)*

The VOUT_OFFSET command on Page 1 instructs the device to add an offset over the VID from the SVID, AVSBus, or PMBus interface and affects the final reference voltage at over-clocking1 mode. The data is in direct format. It is also referred to as over-clocking tracking mode.

Command	VOUT_OFFSET															
Format	Direct, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	VOUT_OFFSET							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	VOUT_OFFSET	Adds an offset over the VID from the SVID, AVSBus, or PMBus interface and affects the final reference voltage. This value is in direct and two's complement format. Bit[7] is the sign bit. The values listed below shows the binary data and real-world value. 8'b 0000 0000: 0 8'b 0000 0001: +1 8'b 0111 1111: +127 8'b 1000 0000: -128 8'b 1000 0001: -127 8'b 1111 1111: -1 The values above are in direct format with 1 VID step/LSB.

VOUT_MAX (24h) *(Page 1)*

The VOUT_MAX command on Page 1 sets the maximum reference voltage of the Rail 2 VID-DAC to set the maximum output voltage. It also sets the secondary over-voltage protection (referred to as OVP1). When V_{OUT} > VOUT_MAX + 400mV, the VR is shut down immediately.

Command	VOUT_MAX															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	VOUT_MAX								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MAX	Sets the maximum reference voltage of the VID-DAC in VID format. 1 VID step/LSB.

VOUT_TRANSITION_RATE (27h) *(Page 1)*

The VOUT_TRANSITION_RATE command on Page 1 sets the Rail 2 dynamic VID transition slew rate at PMBus and PVID VID override mode and sets the AVSBus initial DVID slow rate. This command is only effective after the soft start-up ends.

Command	VOUT_TRANSITION_RATE															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	VOUT_TRANS_CNT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_TRANS_CNT	Sets the Rail 2 dynamic VID transition slew rate at AVSBus and PMBus VID override mode. 100ns/LSB. The PMBus and PVID DVID slew rate can be calculated with: $DVID\_SR(mV/\mu s) = \frac{VID\_STEP(mV)}{VOUT\_TRANS\_CNT \times 0.1(\mu s)}$ The AVSBus initial DVID slew rate and also the maximum DVID slew rate that the VR can handle can be calculated with: $DVID\_SR\_INI(mV/\mu s) = \frac{10(mV)}{VOUT\_TRANS\_CNT \times 0.1(\mu s)}$ Where VID_STEP is 5mV or 10mV (determined by bit[8] of MFR_VR_CONFIG (E4h)), and VOUT_TRANS_CNT is the decimal value defined in VOUT_ TRANSITION _RATE (27h).

VOUT_SENSE_SET (29h) *(Page 1)*

The VOUT_SENSE_SET command on Page 1 sets the V_{OUT} sense-related options. This command is for Rail 2 only.

Command	VOUT_SENSE_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x					VOUT_SCALE								

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12	DC_LOOP_SNS_SEL	Sets the sensing point of V_{OUT} DC loop calibration. 1'b0: VFB pin 1'b1: VDIFF pin
11	VDIFF_GAIN_SEL	Selects the gain of the remote sense amplifier. 1'b0: unity gain. The resolution of the DC loop is 1.56mV. 1'b1: half gain. The resolution of the DC loop is 3.13mV.
10:9	VDIFF_VFB_ADC_GAIN	ADC sensing gain selector of VDIFF and VFB. 2'b00: half gain 2'b01: unity gain 2'b10 and 2'b11: three-quarter gain Set the ADC sense gain to 2'b01 when the remote sense amplifier gain is set to half gain, or the device works erroneously.
8:0	VOUT_SCALE	Sets the Rail 1 VREF-to-VOUT dividing ratio when an external resistor divider is used. VREF ranges from 0.25 - 2V. Equation (15) shows the calculation of VOUT_SCALE.

VOUT_MIN (2Bh) *(Page 1)*

The VOUT_MIN command on Page 1 instructs the device to limit the minimum output voltage of Rail 2. When the output voltage decoded from the SVID, AVSBus, and PMBus interface is lower than what is set by VOUT_MIN (2Bh), the output voltage is clamped to VOUT_MIN.

When an external resistor divider is applied on VOSEN, the minimum output voltage is clamped to VOUT_MIN/K_R. K_R is the dividing ratio of the divider.

Command	VOUT_MIN															
Format	VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	VOUT_MIN								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_MIN	Sets the minimal VID of Rail 2. Any VID lower than this value is clamped to VOUT_MIN. This bit is in VID format with 5mV or 10mV per LSB determined by MFR_VR_CONFIG (E4h) bit[8].

MFR_SLOPE_ADV_CTRL (2Ch) *(Page 1)*

The MFR_SLOPE_ADV_CTRL command on Page 1 programs the slope compensation-related options for Rail 2.

Command	MFR_SLOPE_ADV_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x		SLOPE_INI_ISOURCE								x		

Bits	Bit Name	Description
15:12, 2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	SLOPE_INI_EN	Enables initial slope compensation before soft start. 1'b0: disable initial slope compensation 1'b1: enable initial slope compensation
10:5	SLOPE_INI_ISOURCE	Sets the current source value for initial slope compensation. The slope voltage can be calculated with the equation below: $V_{SLOPE\_INI}(mV) = 0.845 \times SLOPE\_INI\_ISOURCE$ Design the initial slope voltage to be 1.5~2 times of the full-phase nominal slope voltage. Refer to Equation (17) to calculate the full-phase slope voltage.
4	SLOPE_RST_SEL	Selects the slope compensation resetting time. 1'b0: slope compensation is reset during SLOPE_RST_TIME defined with PMBus command MFR_BLANK_TIME (CEh) bit[11:6] 1'b1: slope compensation is reset when PWM is high
3	AC_DC_DROOP_SEL	Selects DC or AD droop injection. 1'b0: select DC droop injection 1'b1: select AC droop injection
1	DVIDUP_PRE-BIAS_MODE	Sets the PWM behavior at DVID up. 1'b0: pre-bias mode, all PWM signals enter HiZ-to-Hi individually 1'b1: PWM1 HiZ-to-Hi, other PWMs pull low first and pull high when the individual set signal comes.
0	DCM_EXIT_SLOPE_CTRL	Resets the slope compensation counter when the VR exits DCM. After the counter is reset, the slope compensation starts and follows the slew rate definition of the activated power state. 1'b0: reset slope compensation counter when DCM is exited 1'b1: does not reset slope compensation counter when DCM is exited

MFR_VR_PROTECT_SET (2Eh) *(Page 1)*

The MFR_VR_PROTECT_SET command on Page 1 sets some protection-related options of the MP2965.

Command	MFR_VR_PROTECT_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x								

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7	VIN_OVP_MODE	Sets the V_{IN} OVP. 1'b0: auto-retry mode 1'b1: latch-off mode
6	PWM_FLT_DTCT_EN	Enables Intelli-Phase fault type detection with the PWM pin. This bit is only effective when the Intelli-Phase supports fault type reporting at PWM. This bit is active for Rail 2 only. 1'b1: enable PWM fault type detection 1'b0: disable PWM fault type detection

5	CS_FLT_EN	Enables VR shutdown when a CS fault is detected on Rail 2. 1'b0: CS fault does not shut down Rail 2 1'b1: CS fault shuts down Rail 2
4	VTEMP_FLT_EN	Enables VTEMP fault to shut down Rail 2. 1'b0: VTEMP fault does not shut down Rail 2 1'b1: VTEMP fault shuts down Rail 2
3:1	OVP1_DIS	3'b011: disable output OVP1 Others: enable output OVP1
0	OTP_MODE	Sets over-temperature protection mode. 1'b0: auto-retry mode 1'b1: latch mode

IOUT_CAL_GAIN_PMBUS (38h) *(Page 1)*

The IOUT_CAL_GAIN_PMBUS command on Page 1 sets the gain for Rail 2 output current PMBus reporting. The MP2965 senses the output current by sensing the voltage on IMON. The reported output current is returned with the PMBus command READ_IOUT (8Ch, Page 1).

Command	IOUT_CAL_GAIN_PMBUS															
Format	Linear, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EXPONENT					MANTISSA										

Bits	Bit Name	Description
15:11	EXPONENT	This value is in two's complement format. 5'b10001: exponent = -15 5'b10010: exponent = -14 5'b10011: exponent = -13 Others: invalid
10:0	MANTISSA	Calculate the mantissa with the equation below: $MANTISSA = \frac{R_{IMON} \times K_{CS}}{16000} \times 2^{EXPONENT}$ Where R_{IMON} is the resistor connected from IMON to ground (in Ω), and K_{CS} is the current sense gain of the Intelli-Phase (in A/A). At high currents, start the design with exponent = -13. When R_{IMON} is too large for a mantissa < 2048 at low-current applications, decrease the exponent from -13 to -15 gradually.

IOUT_CAL_OFFSET_PMBUS (39h) *(Page 1)*

The IOUT_CAL_OFFSET_PMBUS command on Page 1 sets the offset for Rail 1 output current PMBus reporting. The reported output current is returned with PMBus command READ_IOUT (8Ch, Page 1).

Command	IOUT_CAL_OFFSET_PMBUS															
Format	Linear, two's complement															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	EXPONENT					x	x	x	x	MANTISSA						

Bits	Bit Name	Description
15:11	EXPONENT	Exponent for the linear format. This bit is in two's complement format. The value is fixed to: Binary: 11110 Decimal: -2 Real-world value: 0.25A
10:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	MANTISSA	The final current report offset can be calculated with: $IOUT\_REPORT\_OFFSET = MANTISSA \times 2^{EXPONENT}$ Where EXPONENT is always -2, the IOUT_REPORT_OFFSET is set with 0.25A/LSB, and MANTISSA is in two's complement format. Bit[6] is the sign bit. The mantissa list below shows the binary data and real-world I_{OUT} report offset value: 7'b 000 0000: 0 7'b 000 0001: 0.25A 7'b 011 1111: 15.75A 7'b 100 0000: -16A 7'b 100 0001: -15.75A 7'b 111 1111: -0.25A

VOUT_UV_WARN_LIMIT (43h) *(Page 1)*

The VOUT_UV_WARN_LIMIT command on Page 1 sets the Rail 2 V_{OUT} UV warning threshold. The device sets bit[15] of STATUS_WORD (79h) and bit[5] of register STATUS_VOUT (7Ah) and asserts ALT_P# once a VOUT UV warning occurs.

Command	VOUT_UV_WARN_LIMIT															
Format	VID Format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	X	X	X	X	X	X	X	VOUT_UV_WARN_LIMIT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	VOUT_UV_WARN_ LIMIT	Sets the VOUT UV warning threshold. This bit is in VID format with 5mV or 10mV/LSB.

MFR_VR_CONFIG3 (44h) *(Page 1)*

The MFR_VR_CONFIG3 command on Page 1 provides two bytes to program some basic functions for Rail 2.

Command	MFR_VR_CONFIG3															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x				OV/UV_VTH_SEL		

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

5:4	EN_OFF_MODE_SEL	Selects the EN power-off mode and soft-off slew rate. 2'b00: Hi-Z off 2'b01: soft-off with SVID mode slow DVID slew rate 2'b10: soft-off with SVID mode fast DVID slew rate 2'b11: soft-off with PMBus mode DVID slew rate
3	ON/OFF_DLY_CLK_SEL	Selects the clock frequency for the Rail 1 turn-on delay and turn-off delay counter. The counter is set with the PMBus command TON_DELAY (60h, Page 1) and TOFF_DELAY (64h, Page 1). Refer to TON_DELAY (60h) on page 127 and TOFF_DELAY (64h) on pae 128 for more information. 1'b0: 50kHz 1'b1: 20kHz
2:0	OV/UV_VTH_SEL	V_{OUT} OVP/UVP thresholds selection bits. The threshold is related with the remote sense amplifier gain set by register VOUT_SENSE_SET (29h) bit[11]. With remote sense amplifier unit gain: 3'b100: OVP threshold = VREF + 300mV, UVP threshold = VREF - 300mV 3'b010: OVP threshold = VREF + 220mV, UVP threshold = VREF - 220mV 3'b001: OVP threshold = VREF + 140mV, UVP threshold = VREF - 140mV With remote sense amplifier half gain: 3'b100: OVP threshold = VREF + 600mV, UVP threshold = VREF - 600mV 3'b010: OVP threshold = VREF + 440mV, UVP threshold = VREF - 440mV 3'b001: OVP threshold = VREF + 280mV, UVP threshold = VREF - 280mV Others: invalid

MFR_APS_FS_CTRL (45h) *(Page 1)*

The MFR_APS_FS_CTRL command on Page 1 sets the threshold of the time interval between the consecutive phases' PWM rising edges to detect a fast load increase. This register is also used to enable the exit-phase-shedding strategy by detecting the PWM frequency.

Command	MFR_APS_FS_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x												

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11	FS_EXIT_APS_EN_1P	Enables the exit-phase-shedding according to the PWM1 off time. The time threshold is set by register MFR_FS_LIMIT_12P (46h) bit[7:0]. The PWM minimum off time is excluded (see Figure 31a). 1'b0: disable PWM1 off time detection to exit APS 1'b1: enable PWM1 off time detection to exit APS
10	FS_EXIT_APS_EN_NP	Enable exit-phase-shedding according to multi-phase PWM interval time between consecutive phases. The time threshold is set by register 46h, 47h, 48h, and 49h. The PWM blanking time is excluded (see Figure 31b). 1'b0: disable multi-phase PWM interval time detection to exit APS 1'b1: enable multi-phase PWM interval time detection to exit APS
9:7	FS_EXIT_APS_CNT_1P	Sets the continuous count of the PWM1 off-time condition to exit phase shedding. Once the PWM off time conditions meets the counting threshold, the controller exits APS immediately.
6:3	RETURN_APS_DELAY	Sets the minimum full-phase running time after exiting APS. 20μs/LSB.

2:0	FS_EXIT_APS_CNT_NP	Sets the continuous count of the multi-phase PWM interval time to exit phase shedding. Once the PWMs interval condition meets the counting threshold, the controller exits APS immediately.

IOUT_OC_WARN_LIMIT (4Ah) *(Page 1)*

The IOUT_OC_WAIN_LIMIT command on Page 1 sets the Rail 2 I_{OUT} over-current warning threshold.

Command	IOUT_OC_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	IOUT_OC_WARN_LIMIT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	IOUT_OC_WARN_LIMIT	Sets the I_{OUT} OC warning threshold in direct format. 1A/LSB. If the sensed output current is greater than IOUT_OC_WARN_LIMIT, bit[14] of register STATUS_WORD (79h) and bit[5] of register STATUS_IOUT (7Bh) are set. PWR_IN_ALT# is asserted if MFR_VR_CONFIG3 (44h, Page 1) bit[9] = 1.

MFR_IMON_DGTL_GAIN (4Dh) *(Page 1)*

The MFR_IMON_DGTL_GAIN command on Page 1 sets the digital calculating gain for Rail 2 I_{OUT} reporting.

This register sets a digital gain used to fine-tune the IMON sense value for the output current report on Rail 1.

Command	MFR_ IMON_DGTL_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	IMON_DGTL_GAIN										

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10:0	IMON_DGTL_GAIN	Sets the digital calculating gain for I_{OUT} reporting. The gain is multiplied to the IMON ADC sensed values and forms the final IMON digital sense value. The IMON digital sense value is used for output current reporting. The final IMON sensed value can be calculated with the following equation: $IMON\_SNS\_FNL = 1023 \times \frac{I_{OUT} \times K_{CS} \times R_{IMON}}{1.6 \times 16} \times \frac{IMON\_DGTL\_GAIN}{1024}$ Where I_{OUT} is the output current (in A), K_{CS} is the Intelli-Phase current sense gain (in A/A), R_{IMON} is the IMON resistor (in Ω), and IMON_DGTL_GAIN is the decimal value.

MFR_IDROOP_CTRL (4Eh) *(Page 1)*

The MFR_IDROOP_CTRL command on Page 1 is used to program the DC load line and AC droop current.

Command	MFR_IDROOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x						IDROOP_GAIN				

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:6	INT_DROOP_SEL	Selects the Rail 2 internal droop resistor. 3'b000: open 3'b001: 2kΩ 3'b010: 200Ω 3'b111: short Others: not allowed
5:4	IDROOP_TRIM_SEL	The MP2965 provides 16 types of gain selection from I_{CS_SUM} to I_{DROOP}, which is controlled by IDROOP_SET (i.e.: MFR_IDROOP_CTRL (4Eh) bit[3:0]). The device also provides four ATE trimming results to trim the gain and offset of I_{DROOP}/I_{CS_SUM} to get a precise load-line value. Each of the four types of gain share the same ATE trimming registers. 2'b00: select ATE trim 1 for IDROOP gain from 0, 5/64 ~ 7/64 2'b01: select ATE trim 2 for IDROOP gain from 8/64 ~ 11/64 2'b10: select ATE trim 3 for IDROOP gain from 12/64 ~ 15/64 2'b11: select ATE trim 4 for IDROOP gain from 16/64 ~ 19/64
3:0	IDROOP_GAIN	Sets the gain of I_{DROOP}/I_{CS_SUM}. The equation below shows the value of IDROOP_GAIN and the I_{DROOP} current. $I_{DROOP} = \begin{cases} 0 & IDROOP\_GAIN = 0 \\ \frac{IDROOP\_GAIN + 4}{64} \times I_{CS\_SUM} & IDROOP\_GAIN \neq 0 \end{cases}$ Where I_{CS_SUM} is the current sinking into the CS_SUM pin (in A).

MFR_PGOOD_SET (5Dh) *(Page 1)*

The MFR_PGOOD_SET command on Page 1 instructs the device when to assert VRRDY2 by setting the VRRDY2 action mode and VRRDY2 signal assertion delay time. The VRRDY assertion delay time is only effective in VRRDY non-Intel mode.

Command	MFR_PGOOD_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x		PGOOD_DELAY							

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	PGOOD_MODE	Sets the VRRDY action mode. 1'b0: Intel mode. VRRDY asserts once VID reaches VBOOT. 1'b1: non-Intel mode. VRRDY asserts when the condition set by the PMBus command POWER_GOOD_ON (5Eh) is met and the VRRDY delay time ends.
7:0	PGOOD_DELAY	Sets the VRRDY assertion delay time. This bit is only effective when VRRDY mode is set to non-Intel mode. 1μs/LSB.

POWER_GOOD_ON (5Eh) *(Page 1)*

This POWER_GOOD_ON command on Page 1 sets the output voltage threshold at which the VRRDY2 signal asserts. This command is only effective in VRRDY non-Intel mode.

Command	POWER_GOOD_ON															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	POWER_GOOD_ON								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_ON	Sets the output voltage threshold at which VRRDY signal asserts. This bit is in a direct format with VID resolution. This bit is only effective when MFR_PGOOD_SET (5Dh) bit[8] = 1. 1 VID step/LSB.

POWER_GOOD_OFF (5Fh) *(Page 1)*

The POWER_GOOD_OFF command on Page 1 sets the output voltage threshold at which the VRRDY2 signal de-asserts. This command is only effective in VRRDY non-Intel mode.

Command	POWER_GOOD_OFF															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	POWER_GOOD_OFF								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	POWER_GOOD_OFF	Sets the output voltage threshold at which the VRRDY signal de-asserts. This bit is in a direct format with VID resolution. This bit is only effective when MFR_PGOOD_SET (5Dh) bit[8] = 1. 1 VID step/LSB.

TON_DELAY (60h) *(Page 1)*

This TON_DELAY commands on Page 1 sets the delay time from when system initialization ends to when Rail 2 VREF2 starts to boot up.

Command	TON_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TON_DELAY															

Bits	Bit Name	Description
15:0	TON_DELAY	Sets the delay time from when the system initialization ends to when VREF boots up. The resolution is determined by the PMBus command MFR_VR_CONFIG3 (44h) bit[3] (ON/OFF_DLY_CLK_SEL). 20μs/LSB (ON/OFF_DLY_CLK_SEL = 0) 50μs/LSB (ON/OFF_DLY_CLK_SEL = 1)

TOFF_DELAY (64h) *(Page 1)*

This TOFF_DELAY command on Page 1 sets the delay time from EN goes low to when VREF starts to soft-shutdown on Rail 2. This command is only effective at EN soft off.

Command	TOFF_DELAY															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	TOFF_DELAY															

Bits	Bit Name	Description
15:0	TOFF_DELAY	Sets the delay time from when EN goes low to when VREF enters soft-shutdown. The resolution is determined by the PMBus command MFR_VR_CONFIG3 (44h) bit[3] (ON/OFF_DLY_CLK_SEL). 20μs/LSB (ON/OFF_DLY_CLK_SEL = 0) 50μs/LSB (ON/OFF_DLY_CLK_SEL = 1)

POUT_OP_WARN_LIMIT (6Ah) *(Page 1)*

This POUT_OP_WARN_LIMIT command on Page 1 sets the Rail 2 P_{OUT} warning limit.

Command	POUT_OP_WARN_LIMIT															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	POUT_OP_WARN_LIMIT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	POUT_OP_WARN_ LIMIT	Sets the output over-power warning threshold. If the sensed output power is higher than this threshold, bit[0] of STATUS_IOUT (7Bh) is set. 1W/LSB.

READ_CS67 (75h) *(Page 1)*

The READ_CS67 command on Page 1 returns the ADC-sensed voltage on CS6 and CS7 pins in a direct format when they are assigned to Rail 2.

Command	READ_CS67															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	READ_CS6								READ_CS7							

Bits	Bit Name	Description
15:8	READ_CS6	Returns the ADC sensed voltage on CS6 in direct format. 12.5mV/LSB.
7:0	READ_CS7	Returns the ADC sensed voltage on CS7 in direct format. 12.5mV/LSB.

READ_CS5 (76h) *(Page 1)*

The READ_CS5 command on Page 1 returns the ADC-sensed voltage on CS5 in a direct format when it is assigned to Rail 2.

Command	READ_CS5
Format	Unsigned binary

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x	x	x	x	x	x	x	READ_CS5							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	READ_CS5	Returns the ADC-sensed voltage on CS5 in direct format. 12.5mV/LSB.

STATUS_BYTE (78h) *(Page 1)*

The STATUS_BYTE command returns one byte of information with a summary of the most critical statuses and faults.

Command	STATUS_BYTE							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function								x

Bits	Bit Name	Behavior	Description
7	EEPROM_BUSY	Live	Reports the live status of the EEPROM. 1’b0: EEPROM is idle. EEPROM writes and reads; the PMBus command is available. 1’b1: EEPROM is busy. EEPROM writes and reads; the PMBus command is unavailable.
6	OFF	Live	Rail 2 output is off. This bit is in live mode and is asserted if the unit is not providing power to the output, regardless of the reason. The power-off may be caused by protections, EN low, or VID = 0. 1’b0: VOUT1 is off 1’b1: VOUT1 is on
5	VOUT_OV_FAULT	Latch	Rail 2 output voltage (OV) fault indicator. This bit is set and latched if Rail 2 OVP occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1’b0: no V_{OUT} OV fault 1’b1: V_{OUT} OV fault has occurred
4	IOUT_OC_FAULT	Latch	Rail 2 output current (OC) fault indicator. This bit is set and latched if Rail 2 OCP occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1’b0: no output OC fault 1’b1: output OC fault has occurred
3	VIN_UV_FAULT	Latch	V_{IN} under-voltage (UV) fault indicator. This bit is set and latched if an input voltage UV fault occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1’b0: no V_{IN} UV fault 1’b1: V_{IN} UV fault has occurred
2	TEMPERATURE	Latch	Over-temperature fault and warning indicator. This bit is set and latched once OTP or a warning occurs. Send the CLEAR_FAULTS (03h) command to reset this bit. 1’b0: no OT fault or warning 1’b1: OT fault or warning has occurred

1	CML	Latch	PMBus communication fault indicator. Once a communication, memory, or logic fault occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no CML fault 1'b1: a CML fault has occurred
0	RESERVED	/	Unused. X indicates that writes are ignored and reads are always 0.

STATUS_WORD (79h) *(Page 1)*

The STATUS_WORD (79h) command on Page 1 returns two bytes of information with a summary of the device fault/warning condition. The higher byte provides more detailed information of the fault conditions. The lower byte is same as in the STATUS_BYTE register.

Command	STATUS_WORD															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function						x	x		STATUS_BYTE (78h)							

Bits	Bit Name	Behavior	Description
15	VOUT	Latch	Rail 2 V_{OUT} fault and warning indicator. Once an output over-voltage or under-voltage protection or warning occurs, this bit is set and latched. The CLEAR_FAULTS (03h) command can reset this bit. 1'b0: no V_{OUT} fault/warning 1'b1: V_{OUT} fault/warning has occurred
14	IOUT/POUT	Latch	Rail 2 I_{OUT}/P_{OUT} fault and warning indicator. Once output current fault and warning or output power warning occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no I_{OUT}/P_{OUT} fault and warning 1'b1: I_{OUT}/P_{OUT} fault or warning has occurred
13	INPUT	Latch	Input voltage, current, and power fault/warning indicator. Once any protection or warning of the input voltage, input current, or input power occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no input fault and warning 1'b1: input fault or warning has occurred
12	VCCIO FAULT	Latch	VCCIO under-voltage indicator. Once the VCCIO voltage falls below 0.65V, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no VCCIO under voltage 1'b1: VCCIO has been lower than 0.65V
11	PGOOD	Live	Rail 2 VRRDY status indicator. At VRRDY Intel mode, once V_{OUT} reaches the boot-up voltage level, this bit is set. This bit is reset when V_{OUT} is disabled or in a fault state. At VRRDY non-Intel mode, when the V_{OUT} rises higher than the POWER_GOOD_ON level and the PGOOD delay time expires, this bit is asserted. It is de-asserted when V_{OUT} drops to the POWER_GOOD_OFF level or a fault occurs.
10:9	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.

8	WATCH_DOG_OVF	Latch	The watchdog of the monitor block timer overflow indicator. The monitor value calculation has a watchdog timer. If the timer overflows, the monitor value calculation state machine and the timer is reset. Meanwhile, this bit is set. The CLEAR_FAULTS command can reset this bit. 1'b0: watchdog timer does not overflow 1'b1: watchdog timer has overflowed

STATUS_VOUT (7Ah) *(Page 1)*

The STATUS_VOUT command on Page 1 returns one byte of information with the detailed V_{OUT} fault and warning status on Rail 2.

Command	STATUS_VOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function		x				x		

Bits	Bit Name	Behavior	Description
7	VOUT_OV_FAULT	Latch	Rail 2 V_{OUT} OV fault indicator. Once the output over-voltage protection occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no V_{OUT} OV fault 1'b1: V_{OUT} OV fault has occurred
6, 2	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
5	VOUT_UV_WARNING	Latch	Rail 2 V_{OUT} UV warning indicator. Once the output under-voltage warning occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no V_{OUT} UV warning 1'b1: V_{OUT} UV warning has occurred
4	VOUT_UV_FAULT	Latch	Rail 2 V_{OUT} UV fault indicator. Once the output under-voltage fault occurs, this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: no V_{OUT} UV fault 1'b1: V_{OUT} UV fault has occurred
3	VOUT_MAX_MIN_ WARNING	Latch	Indicator that the Rail 2 V_{OUT} has reached VOUT_MAX and VOUT_MIN. Once the VID value exceeds the value set in VOUT_MAX (24h) and VOUT_MIN (2Bh), this bit is set and latched. The CLEAR_FAULTS command can reset this bit. 1'b0: VID is within VOUT_MAX and VOUT_MIN 1'b1: VID is higher than VOUT_MAX or lower than VOUT_MIN
1	LINE_FLOAT	Latch	Rail 2 line float protection indicator. Once the line float fault is detected, the device shuts down the associated rail and sets the LINE_FLOAT bit. This bit is in latched mode. Send CLEAR_FAULTS (03h) to reset this bit. 1'b0: no line float fault 1'b1: line float fault has occurred

0	VDIFF_SC_FAULT	Latch	Rail 2 VDIFF short to GND fault indicator. Once the MP2965 detects that VDIFF is shorted to GND, VDIFF_SC_FAULT is set and latched. The output is shut down immediately. Send CLEAR_FAULTS (03h) to reset this bit. 1'b0: no VDIFF short to GND fault 1'b1: VDIFF has been shorted to GND

STATUS_IOUT (7Bh) *(Page 1)*

The STATUS_IOUT command on Page 1 returns one byte of information with the detailed I_{OUT} fault and warning status on Rail 2.

Command	STATUS_IOUT							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function				x	x	x	x	

Bits	Bit Name	Behavior	Description
7	IOUT_OC_FAULT	Latch	Rail 2 output OC fault indicator. Once output OCP occurs, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no output over-current fault 1'b1: output over-current fault has occurred
6	OC_UV_FAULT	Latch	Rail 2 output OC and UV dual faults indicator. Once output over-current occurs and the under-voltage comparator is set simultaneously, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no output over-current and under-voltage faults 1'b1: output over-current has occurred and the under-voltage comparator is set
5	IOUT_OC_WARNING	Latch	Rail 2 output OC warning indicator. Once the output over-current warning occurs, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no output over-current warning 1'b1: output over-current warning has occurred
4:1	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
0	POUT_OP_WARNING	Latch	Rail 2 output over-power warning indicator. Once an output over-power warning occurs, this bit is set and latched. Send the CLEAR_FAULTS (03h) command to reset it. 1'b0: no output over-power warning 1'b1: output over-power warning has occurred

STATUS_ CML (7Eh) *(Page 1)*

The STATUS_CML command returns one byte of information with PMBus communication-related faults.

Command	STATUS_ CML							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function					x			

Bits	Bit Name	Behavior	Description
7	INVALID_CMD	Latch	Invalid PMBus command indicator. This bit is set and latched when the MP2965 receives an unsupported command code. Send the CLEAR_FAULTS (03h) command to reset this bit. 1'b0: no invalid PMBus command 1'b1: invalid PMBus command has been received
6	INVALID_DATA	Latch	Invalid PMBus data indicator. This bit is set and latched when the MP2965 receives unsupported data. Send the CLEAR_FAULTS (03h) command to reset it. 1'b0: no invalid PMBus data 1'b1: invalid PMBus data has been received
5	PEC_ERROR	Latch	PMBus PEC fault indicator. The PMBus interface supports the use of the packet error checking (PEC) byte defined in the SMBus standard. The PEC byte is transmitted by the MP2965 during a read transaction or sent to the MP2965 during a write transaction. If the PEC byte sent to the controller during a write transaction is incorrect, the command is not executed, and PEC_FAULT is set and latched. Send the CLEAR_FAULTS (03h) to clear the fault. 1'b0: no PEC fault 1'b1: a PEC fault has been detected
4	CRC_FAULT	Latch	CRC fault indicator. In the process of storing operating memory data into the EEPROM, the MP2965 calculates a CRC code for each bit and saves the final CRC code into the EEPROM. In the process of restoring the EEPROM data to the operating memory, the MP2965 re-calculates the CRC code with each bit. The MP2965 checks the CRC results when the restore process is done. If the CRC result does not match with what was stored during the storing process, the VR shuts down and sets the CRC_FAULT bit. This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to reset the fault. 1'b0: no EEPROM CRC fault 1'b1: an EEPROM CRC fault has been detected
3	RESERVED		Unused. X indicates that writes are ignored and reads are always 0.
2	CML_FLT_TRG	Latch	This bit is set when the EEPROM operation is blocked for the process of the controller recording faults to the EEPROM. This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to clear the fault. 1'b0: no EEPROM operation is blocked for fault recording 1'b1: EEPROM operation has been blocked for fault recording
1	CML_OTHER_FAULTS	Latch	This bit can be set when any of the faults below occur during PMBus communication. 1) Sending too few bits 2) Reading too few bits 3) Host sends or reads too few bytes 4) Reading too many bytes This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to clear the fault.

0	EEPROM_SIG_FAULT	Latch	While restoring data from the EEPROM to the memory, this bit first checks the signature register in address 00h of the EEPROM. If the signature is not 0x1234, the restore process is ceased immediately and sets EEPROM_SIG_FAULTS. This bit is in latch mode. Send the CLEAR_FAULTS (03h) command to clear the fault.

READ_VOUT (8Bh) *(Page 1)*

The READ_VOUT command on Page 1 returns two bytes of information with the V_{OUT} of Rail 2 in a direct format.

Command	READ_VOUT															
Format	VID or Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x	x	x	READ_VOUT											

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:0	READ_VOUT	Returns the sensed voltage of VOSEN - VORTN. The voltage report is in VID format with VID resolution or direct format with 1mV resolution. The resolution is determined by the PMBus command MFR_LOOP_PI_SET (E2h, Page 1) bit[10] (VOUT_PMBUS_LSB). 1 VID step/LSB when VOUT_PMBUS_LSB = 0 1mV/LSB when VOUT_PMBUS_LSB = 1

READ_IOUT (8Ch) *(Page 1)*

The READ_IOUT command on Page 1 returns the sensed output current of Rail 2 in a direct format.

Command	READ_IOUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	1	1	1	1	0	READ_IOUT										

Bits	Bit Name	Description
15:11	FIXED	Read-only registers. Fixed to 5'b11110.
10:0	READ_IOUT	Returns the sensed output current. 0.25A/LSB.

READ_POUT (96h) *(Page 1)*

The READ_POUT command on Page 1 returns the sensed output power of Rail 2 in a direct format.

Command	READ_POUT															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	x	x	x	x	x	x	x	READ_POUT								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.

8:0	READ_POUT	Returns the sensed output power in direct format. 1W/LSB.

MFR_PWD_USER (A7h) *(Page 1)*

The MFR_PWD_USER command on Page 1 sets password to protect PMBus communication from writes or reads. Users can input and check the password with the PMBus command PWR_CHK_CMD (F2h, Page 0).

Command	MFR_PWD_USER															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PWD_USER															

Bits	Bit Name	Description
15:0	PWD_USER	Sets the password to protect the PMBus communication from writes or reads.

IOUT_RPT_GAIN_SVID_AVS (A8h) *(Page 1)*

The IOUT_RPT_GAIN_SVID_AVS command on Page 1 sets the Rail 2 IMON gain for VR13 CPU I_{OUT} report in SVID override mode and the AVSBus I_{OUT} reports in AVSBus VID override mode.

Command	IOUT_RPT_GAIN_SVID_AVS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x				IMON_GAIN									

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:10	AVSBUS_GIMON_RES	Selects the current-sense resolution for the AVSBus interface I_{OUT} report. This bit is only effective in AVSbus VID override mode. Note that the resolution selection is for an intermediate variable only, which is used to improve the AVSBus I_{OUT} report accuracy. The final AVSBus I_{OUT} report is always in 0.1A/LSB. 3'b001: 10mA/LSB, AVSBus maximum report current is 20.5A 3'b010: 20mA /LSB, AVSBus maximum report current is 41A 3'b100: 40mA /LSB, AVSBus maximum report current is 82A 3'b000: 860mA /LSB, AVSBus maximum report current is164A Others: invalid input

9:0	IMON_GAIN	Sets the current sensing gain for the VR13 output current report and AVSBus I_{OUT} report. At VR13 SVID override mode, the IMON sense gain can be calculated with the equation below: $IMON\_GAIN = 40 \times I_{CCMAX} \times K_{CS} \times R_{IMON}$ Where I_{CCMAX} is the maximum current of VR13.HC CPU (in A), K_{CS} is the Intelli-Phase current sense gain (in μA/A), R_{IMON} is the IMON resistor (in kΩ). At AVSBus VID override mode, the IMON sense gain can be calculated with the following equation: $IMON\_GAIN = \begin{cases} \frac{K_{CS} \times R_{IMON}}{16} \times \frac{1023}{1.6} \times \frac{256}{100} \times AVSBUS\_GIMON\_RES & AVSBUS\_GIMON\_RES > 0 \\ \frac{K_{CS} \times R_{IMON}}{16} \times \frac{1023}{1.6} \times \frac{256}{100} \times 8 & AVSBUS\_GIMON\_RES = 0 \end{cases}$ Where K_{CS} is the Intelli-Phase current sense gain (in A/A), R_{IMON} is the IMON resistor (in Ω), and AVSBUS_GIMON_RES is the decimal value set with IOUT_RPT_GAIN_SVID_AVS (A8h) bit[12:10].

IOUT_RPT_OFFSET_SVID_AVS (A9h) *(Page 1)*

The IOUT_RPT_OFFSET_SVID_AVS command on Page 1 sets the output current report offset for VR13, VR13.HC, and AVSBus VID override mode. This command is for Rail 2 only.

Command	IOUT_RPT_OFFSET_SVID_AVS															
Format	Two's complement, direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	OFFSET_CPU							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	OFFSET_CPU	Sets the output current report offset. The value is a two's complement format. The values listed below show the binary data and real-world values. 8'b 0000 0000: 0 8'b 0000 0001: 1 8'b 0111 1111: 127 8'b 1000 0000: -128 8'b 1000 0001:-127 8'b 1111 1111:-1 The current resolution at SVID override mode is ICCMAX/255 (A/LSB), where ICCMAX is the current value set with the PMBus command MFR_ICC_MAX (BDh). The current resolution at AVSBus VID override mode follows the setting in IOUT_RPT_GAIN_SVID_AVS (A8h) bit[12:10].

MFR_DROOP_CMPN1 (B0h) *(Page 1)*

The MFR_DROOP_CMPN1 command on Page 1 sets the options to compensate for the voltage drop caused by an extra droop current on DVID up and a droop resistor is applied.

Command	MFR_DROOP_CMPN1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function											DROOP_CMPN_LIMIT					

Bits	Bit Name	Description
15	DROOP_CMPN_EN	Droop compensation enable bit. 1'b0: disable droop compensation 1'b1: enable droop compensation
14:9	CNT_DROOP_CMPN_DEC	Sets the time interval for each VID step to decrease droop compensation after DVID up ends. 50ns/LSB.
8:6	CNT_DROOP_CMPN_INC	Sets the time interval for each VID step to add droop compensation when, DROOP_CMPN_EN bit[15] = 1. 50ns/LSB.
5:0	DROOP_CMPN_LIMIT	Sets the maximum VID steps for droop compensation in a direct format. 1 VID step/LSB.

MFR_DROOP_CMPN2 (B2h) *(Page 1)*

The MFR_DROOP_CMPN2 command on Page 1 is used to compensate for the voltage offset caused by an extra droop current at DVID when a droop resistor is applied.

Command	MFR_DROOP_CMPN2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function											VID_FLTR_ACT_CTRL					

Bits	Bit Name	Description
15:14	VID_FLTR_SEL	Selects the VID-DAC output filter when DVID is down. 2'b00: 2.14μs 2'b01: 4.28μs 2'b10: 6.42μs 2'b11: 8.56μs
13	VID_FLTR_EN	Enables the VID-DAC output filter. 1'b0: disable VID-DAC filter 1'b1: enable VID-DAC filter
12	VID-DAC_CMPN_EN	A comparator is designed between VID-DAC output and VID-DAC filter output. This bit is used to smooth the transition between DVID is down and preemptive with DIVD up. 1'b0: disable the VID-DAC comparator 1'b1: enable VID-DAC comparator
11:6	DLY_RST_DROOP_CMPN	Sets the delay time after VR_SETTLE to reset droop compensation when DVID up. 50ns/LSB.
5:0	VID_FLTR_ACT_CTRL	Sets the VID filter effective threshold in a direct format when droop compensation is resetting. This bit is only effective when bit[13] (VID_FLT_EN) = 1. 1 VID step/LSB.

MFR_ICC_MAX (BDh) *(Page 1)*

The MFR_ICC_MAX command on Page 1 sets the Rail 2 SVID maximum report current (FFh). The data is used for current scaling in the SVID command I_{OUT} (15h). This command also sets the value returned to SVID command ICC_MAX (21h).

Command	MFR_ICC_MAX															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Function	x	x	x	x	x	x	x	x	ICCMAX_VR13

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	ICCMAX_VR13	Sets the VR13 SVID maximum report current (FFh). Note that the output will not boot if ICCMAX_VR13 is set to 0. 1A/LSB.

MFR_PIN_SET (BEh) *(Page 1)*

The MFR_PIN_SET command on Page 1 sets the PWR_IN_ALT# assertion delay, PIN report resolution, and PIN report offset.

Command	MFR_PIN_SET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	PWR_IN_ALT_DLY								PIN_OFFSET							

Bits	Bit Name	Description
15:10	PWR_IN_ALT_DLY	Sets THE PWR_IN_ALERT de-assert delay time. When PWR_ALERT asserts, the timer counts for PWR_ALT_DLY x 6.4ms + 6.3ms and de-assert PWM_IN_ALERT.
9:8	PIN_LSB_SEL	Sets the input power report resolution in the PMBus command READ_PIN (97h). 2'b00: 1W/LSB 2'bx1: 0.5W/LSB 2'b10: 0.25W/LSB
7:0	PIN_OFFSET	Sets the PIN report offset. This bit is in two's complement format. Bit[7] is the sign bit. The resolution follows the definition of bit[9:8].

SVID_LOT_CODE_PROTOCOL_ID (C1H) (PAGE 1)

The SVID_LOT_CODE_PROTOCOL_ID command provides two bytes to record the Intel SVID protocol versions for Rail 2.

Command	SVID_LOT_CODE_PROTOCOL_ID															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	PROTOCOL_ID							

Bits	Bit Name	Description
15:8	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
7:0	PROTOCOL_ID	Identifies Rail 2's version of the SVID protocol the controller supports. 01h: VR12.0, IMPV7 02h: VR12.5 03h: VR12.6 04h: VR13.0 10mV VID table 05h: IMVP8 06h: VR12.1 07h: VR13.0 5mV table 08h: IMVP9

SVID_CAPABILITY_DC_LL (C2h) *(Page 1)*

The SVID_CAPABILITY_DC_LL command sets the Intel VR13 specified CAPABILITY and DC_LL.

Command	SVID_CAPABILITY_DC_LL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	CAPABILITY								DC_LL							

Bits	Bit Name	Description
15:8	CAPABILITY	Bit-mapped register. This bit identifies the SVID VR capabilities and which optional telemetry register is supported. 00h indicates that only required registers are supported.
7:0	DC_LL	Data register containing the programmed load line or AVP of Rail 2. 0.1mΩ/LSB.

SVID_SR_FAST_SR _SLOW (C3h) *(Page 1)*

The SVID_SR_FAST_SR_SLOW command sets the Intel VR13 specified SR_FAST and SR_SLOW.

Command	SVID_SR_FAST_SR_SLOW															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	SR_FAST								SR_SLOW							

Bits	Bit Name	Description
15:8	SR_FAST	Data register containing the fast slew rate capability of the slew rate that Rail 2 can sustain. 1mV/µs.
7:0	SR_SLOW	Data register containing the capability of Rail 2's slow slew rate. 1mV/µs.

SVID_ VR_CONFIG_TOLERANCE2 (C4h) *(Page 1)*

The SVID_VR_CONFIG_TOLERANCE2 command sets the Intel VR13 specified EN2SVID_RDY and VR tolerance2.

Command	SVID_ VR_CONFIG_TOLERANCE2															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x			VR_TOLERANCE2							

Bits	Bit Name	Description
15:10	RESERVED	Unused.
9	MUL_VR_CONFIG_R1	The bit is used to set the initial value for the SVID register MUL_VR_CONFIG, which determines whether to assert VRRDY1 when SetVID is 0 for Rail 1. 1'b0: VRRDY1 de-asserts when SetVID is 0 1'b1: VRRDY1 asserts when SetVID is 0
8	MUL_VR_CONFIG_R2	The bit is used to set the initial value for the SVID register MUL_VR_CONFIG, which determines whether to assert VRRDY2 when SetVID is 0 for Rail 2. 1'b0: VRRDY2 de-asserts when SetVID is 0 1'b1: VRRDY2 asserts when SetVID is 0

7:0	VR_TOLERANCE2	Data register containing the VR tolerance band (TOB) of Rail 2 based on board parts (inductor DCR and inductance tolerance, current sense errors, etc.). 1mV/µs.

MFR_APS_LEVEL_45P (C5h) *(Page 1)*

When APS is enabled by setting MFR_VR_CONFIG (E4h) bit[5:4] = 2'b1x, this command sets the Rail 1 auto-phase shedding current threshold to 5-/4-phase and Rail 2 auto-phase shedding current threshold to 2-/1-phase.

Command	MFR_APS_LEVEL_45P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	DROP_LEVEL_5P_R1/ DROP_LEVEL_1P_R2								DROP_LEVEL_4P							

Bits	Bit Name	Description
15:8	DROP_LEVEL_5P_R1 DROP_LEVEL_1P_R2	Sets the Rail 1 auto-phase shedding current threshold to 5-phase CCM or Rail 2 auto-phase shedding current threshold to 1-phase CCM. 1A/LSB.
7:0	DROP_LEVEL_4P_R1 DROP_LEVEL_2P_R2	Sets the Rail 1 auto-phase shedding current threshold to 4-phase CCM or Rail 2 auto-phase shedding current threshold to 2-phase CCM. 1A/LSB.

MFR_APS_LEVEL_6P (C6h) *(Page 1)*

When APS is enabled by setting MFR_VR_CONFIG (E4h) bit[5:4] = 2'b1x, this command sets the Rail 1 auto-phase shedding level to 6-phase operation or the Rail 2 auto-phase shedding current threshold to DCM operation.

Command	MFR_APS_LEVEL_6P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	DROP_LEVEL_6P/ DROP_LEVEL_DCM							

Bits	Bit Name	Description
15:8	RESERVED	Unused.
7:0	DROP_LEVEL_6P DROP_LEVEL_DCM	Sets the Rail 1 auto-phase shedding current threshold to 6-phase CCM and Rail 2 auto-phase shedding current threshold to DCM. 1A/LSB.

MFR_APS_SET (C7h) *(Page 1)*

When APS is enabled by setting MFR_VR_CONFIG (E4h) bit[5:4] = 2'b1x, this command sets the Rail 2 auto-phase shedding current hysteresis and phase via the phase-dropping time interval.

Command	MFR_APS_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	DROP_PHASE_WAITTIME							x	x	x	x	MFR_APS_HYS			

Bits	Bit Name	Description

15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:9	DROP_PHASE_ WAITTIME	Sets the phase-by-phase dropping time intervals. This bit is only effective when MFR_APS_SET (C7h) bit[8] = 1. 1μs/LSB.
8	SHED_PHASE_MODE	Sets the auto-phase shedding behavior. 1'b0: drop phase count to target immediately 1'b1: shed phases one-by-one with programmed delay time. The delay time is set with MFR_APS_SET (C7h) bit[14:9].
7:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	MFR_APS_HYS	Sets the current hysteresis between 1-phase shedding and adding. This bit is used to prevent phase shedding back and forth when APS is enabled. 1A/LSB.

MFR_IDROOP_OFFSET (C9h) *(Page 1)*

The MFR_IDROOP_OFFSET command on Page 1 provides one byte for users to add an offset over the Rail 2 droop current.

Command	MFR_IDROOP_OFFSET							
Format	Signed binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	IDROOP_OFFSET					

Bits	Bit Name	Description
7:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	IDROOP_OFFSET	Adds an offset to the droop current for users.

Bit[5] = 0	Positive	Bit[5] = 1	Negative	Unit
bit[4]	13	bit[4]	13	μA
bit[3]	6.48	bit[3]	6.48	μA
bit[2]	3.24	bit[2]	3.24	μA
bit[1]	1.62	bit[1]	1.62	μA
bit[0]	0.81	bit[0]	0.81	μA

MFR_DC_LOOP_CTRL (CBh) *(Page 1)*

The MFR_DC_LOOP_CTRL command on Page 1 sets the DC loop calibration-related holding condition. This command also provides two bits to program the PWM behavior when phase adding.

Command	MFR_DC_LOOP_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function			HOLD_LP_PRD_TIME										DC_CAL_MIN_THOLD			

Bits	Bit Name	Description
15	PRD_ADD_PH_MODE	Sets phase-adding mode when the PWM period meets the condition set with bit[13:7] in this command. 1'b0: add phases with a PWM low time inserted between HiZ-to-Hi 1'b1: add phases with a PWM HiZ-to-Hi directly

14	VFB-_ADD_PH_MODE	Sets phase-adding mode when VFB is lower than the VFB- window. 1'b0: add phases with a PWM low time inserted between HiZ-to-Hi 1'b1: add phases with PWM HiZ-to-Hi directly
13:7	HOLD_LP_PRD_TIME	Sets the period changing time to hold the DC loop and current balance loop. If the PWM period meets the condition below, and the associated enable bits is set, the DC loop and CB loop are held. All loop hold functions related with this time setting is ineffective in DCM. $\left\|T_{PWM} - T_{PWM\_REF}\right\| \leq HOLD\_LP\_PRD\_TIME \times 80ns$ Where TPWM is the real-time PWM period, and TPWM_REF is the nominal period set with MFR_FS (ECh). 80ns/LSB.
6	PRD_HOLD_DC_EN	1'b0: disable fs change condition to hold the DC loop 1'b1: enable fs change condition to hold the DC loop
5	PS_HOLD_DC_EN	1'b0: disable phase number change to hold the DC loop 1'b1: enable phase number change to hold the DC loop
4	TRANS_HOLD_DC_EN	1'b0: disable VFB+/- window condition to hold the DC loop 1'b1: enable VFB+/- window condition to hold the DC loop
3:0	DC_CAL_MIN_THOLD	Sets the DC loop minimal holding time in direct format. 200μs/LSB with +100μs offset.

MFR_APS_CTRL (CCh) *(Page 1)*

The MFR_APS_CTRL command on Page 1 sets APS exiting conditions for Rail 2.

Command	MFR_APS_CTRL															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x	x	x	x			

Bits	Bit Name	Description
15:3	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
2	APS_EXIT_UV_EN	When VFB falls below the VFB- window, the VR can be enabled to exit APS and run with full phase. 1'b0: disable VFB- window event to exit APS 1'b1: enable VFB- window event to exit APS
1	APS_EXIT_FS_EN	When the FS limit conditions is met, the VR can be enabled to exit APS and run with full phase. The FS limit is set with PMBus commands 45h, 46h, 47h, 48h, and 49h. 1'b0: disable FS limit event to exit APS 1'b1: enable FS limit event to exit APS
0	APS_EXIT_OC_EN	When Rail 2 phase 1 triggers OCP_Phase, the device can be enabled to exit APS and run with full phase. 1'b0: disable Rail 2 phase 1 OCP_Phase event to exit APS 1'b1: enable Rail 2 phase 1 OCP_Phase event to exit APS

MFR_OSR_SET (CDh) *(Page 1)*

The MFR_OSR_SET command on Page 1 sets the over-shot reduction (OSR) related parameters. This command is for Rail 2 only.

This register sets the minimum PWM off-time and block time of the OSR function on Rail 2.

Command	MFR_OSR_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	OSR_DEGLITCH_TIME						OSR_BLANK_TIME						

Bits	Bit Name	Description
15:13	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
12:7	OSR_DEGLITCH_TIME	Sets the minimum PWM off-time in the OSR process. 5ns/LSB.
6:0	OSR_BLANK_TIME	Sets the blanking time between two OSR events. 10ns/LSB.

MFR_BLANK_TIME (CEh) *(Page 1)*

The MFR_BLANK_TIME command on Page 1 sets the slope compensation reset time and PWM blanking time between two consecutive phases. This command is for Rail 2 only.

Command	MFR_BLANK_TIME															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	SLOPE_RESET_TIME						PWM_BLANK_TIME					

Bits	Bit Name	Description
15:12	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
11:6	SLOPE_RESET_TIME	Sets the slope compensation resetting time. This bit is effective when register 2Ch bit[4] = 0. Note that the slope compensation reset time should be shorter than the PWM blanking time set by bit[5:0] (PWM_BLANK_TIME). 5ns/LSB.
5:0	PWM_BLANK_TIME	Sets the PWM blanking time between two consecutive phases. 5ns/LSB.

MFR_SLOPE_SR_5P (D6h) *(Page 1)*

The MFR_SLOPE_SR_5P command on Page 1 provides two bytes to program the slope compensation slew rate for Rail 1 5-phase operation and Rail 2 3-phase operation. Use Equation (18) to calculate the slope voltage amplitude.

Command	MFR_SLOPE_SR_5P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_CNT_5P (D7h) *(Page 1)*

The MFR_SLOPE_CNT_5P command on Page 1 is used to set the slope voltage clamp time for Rail 1 5-phase operation and Rail 2 3-phase operation.

Command	MFR_SLOPE_CNT_5P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for Rail 1 5-phase operation and Rail 2 3-phase operation. 5ns/LSB.

MFR_SLOPE_SR_6P (D8h) *(Page 1)*

The MFR_SLOPE_SR_6P command on Page 1 provides two bytes to program the slope compensation for Rail 1 6-phase operation and Rail 2 2-phase operation. Use Equation (18) to calculate the slope voltage amplitude.

Command	MFR_SLOPE_SR_6P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	CAP				CURRENT_SOURCE					

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_CNT_6P (D9h) *(Page 1)*

The MFR_SLOPE_CNT_6P command on Page 1 is used to set the slope voltage clamp time for Rail 1 6-phase operation and Rail 2 2-phase operation.

Command	MFR_SLOPE_CNT_6P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for Rail 1 6-phase operation and Rail 2 2-phase operation. 5ns/LSB.

MFR_SLOPE_SR_7P (DAh) *(Page 1)*

The MFR_SLOPE_SR_7P command on Page 1 provides two bytes to program the slope compensation for Rail 1 7-phase operation and Rail 2 1-phase CCM operation. Use Equation (18) to calculate the slope voltage amplitude.

Command	MFR_SLOPE_SR_7P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x		CURRENT_SOURCE					

Bits	Bit Name	Description
15:7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6	CAP	Sets the capacitor value for slope compensation. 1.85pF/LSB.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_CNT_7P (DBh) *(Page 1)*

The MFR_SLOPE_CNT_7P command on Page 1 is used to set the slope voltage clamp time for Rail 1 7-phase operation and Rail 2 1-phase CCM operation.

Command	MFR_SLOPE_CNT_7P															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for Rail 1 7-phase operation and Rail 2 1-phase CCM operation. 5ns/LSB.

MFR_SLOPE_SR_DCM (DCh) *(Page 1)*

The MFR_SLOPE_SR_DCM command on Page 1 sets the slew rate of slope compensation for Rail 2 at 1-phase DCM. Calculate the slope slew rate with Equation (17) with CAP = 0.

Command	MFR_SLOPE_SR_DCM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x	CURRENT_SOURCE					

Bits	Bit Name	Description
15:6	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
5:0	CURRENT_SOURCE	Sets the current source value for slope compensation. 0.25μA/LSB.

MFR_SLOPE_CNT_DCM (DDh) *(Page 1)*

The MFR_SLOPE_CNT_DCM command on Page 1 is used to set the slope voltage clamp time for Rail 2 1-phase DCM operation.

Command	MFR_SLOPE_CNT_DCM															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	SLOPE_CNT									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	SLOPE_CNT	Sets the slope voltage clamp time for 1-phase DCM operation. 5ns/LSB.

MFR_SLOPE_TRIM1 (DEh) *(Page 1)*

The MFR_SLOPE_TRIM1 command on Page 1 is used to trim the output voltage at 2-/1-phase CCM and 1-phase CCM of Rail 2.

Command	MFR_SLOPE_TRIM1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	VTRIM_2P					VTRIM_1P					VTRIM_DCM				

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:10	VTRIM_2P	Sets the V_{OUT} trim for 2-phase operation. 2.35mV/LSB.
9:5	VTRIM_1P	Sets the V_{OUT} trim for 1-phase CCM operation. 2.35mV/LSB.
4:0	VTRIM_DCM	Sets the V_{OUT} trim for 1-phase DCM operation. 2.35mV/LSB.

MFR_SLOPE_TRIM2 (DFh) *(Page 1)*

The MFR_SLOPE_TRIM2 command on Page 1 is used to trim the output voltage at 5-/4-/3-phase operation of Rail 2.

Command	MFR_SLOPE_TRIM2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	x	x	x	x	VTRIM_3P				

Bits	Bit Name	Description
15:5	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
4:0	VTRIM_3P	Sets the V_{OUT} trim for 3-phase operation. 2.35mV/LSB.

MFR_LOOP_PI_SET (E2h) *(Page 1)*

The MFR_LOOP_PI_SET command on Page 1 sets the Rail 2 V_{OUT} PMBus report resolution and PI parameters of the DC loop and current balance loop.

Command	MFR_LOOP_PI_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x		DC_LOOP_KI						CB_LOOP_KI			

Bits	Bit Name	Description
15:11	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
10	VOUT_PMBUS_LSB	Sets the resolution of the PMBus V_{OUT} report with command READ_VOUT (8Bh). 1'b0: VID format 1'b1: 1mV/LSB
9:4	DC_LOOP_KI	Sets the PI parameter of the DC calibration loop.
3:0	CB_LOOP_KI	Sets the PI parameter of the current balance loop.

MFR_CB_LOOP_CTRL (E3h) *(Page 1)*

The MFR_CB_LOOP_CTRL command on Page 1 sets the current balance loop holding time and conditions for Rail 2.

Command	MFR_CB_LOOP_CTRL							
Format	Unsigned binary							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function					CB_LOOP_THOLD			

Bits	Bit Name	Description
7	CB_TRANS_ HOLD_EN	Holds the current balance loop regulation when a load transient event is detected (i.e.: VFB exceeds VFB+ or VFB- window). 1'b0: no action 1'b1: hold the current balance loop regulation when a load transient event is detected
6	CB_PRD_HOLD_EN	Holds the current balance loop when the PWM time interval meets the PWM switching period condition set with the PMBus command MFR_DC_LOOP_CTRL (CBh) bit[13:7]. 1'b0: no action 1'b1: hold the current balance loop when the PWM switching period condition is met
5	CB_PS_HOLD_EN	Holds the current balance loop when the phase count is changed. 1'b0: no action 1'b1: hold the current balance loop when the phase count is changed
4	CB_DVID_HOLD_EN	Holds the current balance loop when DVID occurs. 1'b0: no action 1'b1: hold the current balance loop when DVID occurs
3:0	CB_LOOP_THOLD	Sets the current balance loop holding time. During a load transient event, FS change event, power state changing, or a DVID event is detected and the corresponding enable bit is set, the current balance loop stops regulating for a period of time set with command CB_LOOP_THOLD. 100µs/LSB.

MFR_VR_CONFIG (E4h) *(Page 1)*

The MFR_VR_CONFIG command on Page 1 provides two bytes to program some basic system configurations of Rail 2.

Command	MFR_VR_CONFIG															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w

Function														x	

Bits	Bit Name	Description
15	DC_LOOP_EN_DCM	Enables DC loop calibration at DCM. 1'b0: disable DC loop calibration at DCM 1'b1: enable DC loop calibration at DCM
14	DC_LOOP_EN	Enables DC loop calibration in both DCM and CCM operation. 1'b0: disable DC loop calibration 1'b1: enable DC loop calibration
13	PSI_SEL	Enables forcing the power state. This bit is only effective when OPERATION (01h) bit[5:4] ≠ 2'b11. 1'b0: disable forcing power state with bit [12:11] of MFR_VR_CONFIG (E4h) 1'b1: enable forcing power state with bit[12:11] of MFR_VR_CONFIG (E4h)
12:11	PSI_PMBUS	Power state selection bits when MFR_VR_CONFIG (E4h) bit[13] = 1. 2'b00: full-phase CCM. The phase count is determined by MFR_VR_CONFIG (E4h) bit [1:0]. 2'b01: 1-phase CCM 2'b1x: 1-phase DCM
10	OVER_CLOCK1_EN	Enable over-clocking mode 1 (i.e.: adding an offset voltage over VID with PMBus command VOUT_OFFSET (23h)). This bit is effective at SVID, PMBus, AVSBus, and PVID override mode. 1'b0: disable over-clocking mode 1. The VOUT_OFFSET (23h) is ineffective, and the VID offset from SVID interface is effective. 1'b1: enable over-clocking mode 1. The PMBus command VOUT_OFFSET (23h) is active and added to initial VID. The VID offset from SVID is ineffective.
9	DCM_TON_SET	Sets the PWM on time at DCM operation. 1'b0: PWM on time at DCM is same as in CCM operation 1'b1: PWM on time at DCM is 3/4 that of CCM operation Bug: 1234
8	VID_STEP_SEL	Selects the Rail 2 VID resolution. All PMBus commands on Page 1 in VID format follow the VID resolution definition with VID_STEP_SEL. 1'b0: 10mV per VID step 1'b1: 5mV per VID step
7	CB_LOOP_EN	Enables the current balance loop. 1'b0: disable current balance loop 1'b1: enable current balance loop
6	OSR_EN	Enables the overshoot reduction function. 1'b0: disable overshot reduction function 1'b1: enable overshot reduction function
5:4	APS_IVID_EN	Enables auto-phase shedding and IVID. 2'b00: disable APS and IVID 2'b01: enable IVID 2'b1x: enable APS

3	SVID_OVERCLK2_EN	Enables over-clocking mode 2 at SVID mode. 1'b0: disable SVID over-clocking mode 2 1'b1: enable SVID over-clocking mode 2. The VID is determined by the PMBus command VOUT_COMMAND (21h), but the MP2965 still responds to all CPU SVID commands.
2	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
1:0	PHASE_CNT	Sets the full-phase count of Rail 2 when MFR_VR_CONFIG (E4h) bit[12:11] = 2'b00. 2'b00: 1-phase DCM 2'b01: 1-phase CCM 2'b10: 2-phase 2'b11: 3-phase

MFR _VBOOT_SET (E5h) *(Page 1)*

The MFR_VBOOT_SET command on page1 programs the boot up voltage if VBOOT is set with register. This command also provides a bit to enable IMVP9 VID table format.

Command	MFR_VBOOT_SET															
Format	Unsigned binary, VID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x		VBOOT_SET							

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8	IMVP9_EN	Enables IMVP9 VID table format. 1'b0: disable IMVP9 VID table format 1'b1: enable IMVP9 VID table format
7:0	VBOOT_SET	Sets the boot-up voltage of Rail 2 when VBOOT is set with the register (i.e.: MFR_VR_CONFIG2 (09h) bit[12:11] = 2'b00). This bit is in VID format. 1 VID step/LSB.

MFR_IIN_CAL_OFFSET (E7h) *(Page 1)*

The MFR_IIN_CAL_OFFSET command on Page 1 sets the input current sense offset.

Command	MFR_IIN_CAL_OFFSET															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	IIN_CAL_OFFSET								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	IIN_CAL_OFFSET	Sets the input current sense offset in direct and two's complement format. Bit[7] is the sign bit. 31.25mA/LSB.

MFR_CUR_GAIN (E9h) *(Page 1)*

The MFR_CUR_GAIN command on Page 1 sets the Rail 2 phase current sensing gain. The MP2965 senses the phase current by monitoring the voltage between CS and CS_SUM. The gain affects the

per-phase current limit. Equation (22) shows the relationship of the current sensing gain/offset and the actual phase current limit.

Command	MFR_CUR_GAIN															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	PHASE_CUR_GAIN									

Bits	Bit Name	Description
15:10	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
9:0	PHASE_CUR_GAIN	Sets the phase current sensing gain with the following equation: $PHASE\_CUR\_GAIN = 8200 \times R_{CS} \times K_{CS}$ Where R_{CS} is the phase-current sensing resistor (in Ω), K_{CS} is the current sensing gain of the Intelli-Phase (in μA/A).

MFR_FS_LOOP_CTRL (EBh) *(Page 1)*

The MFR_FS_LOOP_CTRL command on Page 1 sets the frequency loop hold time and conditions for Rail 2.

Command	MFR_FS_LOOP_CTRL															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x															

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14	FS_TRANS_HOLD_EN	Holds the frequency loop regulation when a load transient event is detected (i.e.: VFB exceeds the VFB+ or VFB- window). 1'b0: no action 1'b1: hold the frequency loop regulation when a load transient event is detected
13	FS_PS_HOLD_EN	Holds the frequency loop regulation when the phase count is changed. 1'b0: no action 1'b1: hold the frequency loop regulation when the phase count is changed
12	FS_DVID_HOLD_EN	Holds the frequency loop regulation when DVID occurs. 1'b0: no action 1'b1: hold the frequency loop regulation when DVID occurs
11:8	FS_LOOP_HOLD_TIME	Sets the minimal holding time of the frequency loop when a load transient, phase count change, or DVID occur. 100μs/LSB.
7	FS_LOOP_EN	Enables the frequency loop. 1'b0: disable frequency loop 1'b1: enable frequency loop
6:0	FS_LOOP_KI	Sets the frequency loop regulation parameter.

MFR_FS (ECh) *(Page 1)*

The MFR_FS command on Page 1 sets the switching frequency of Rail 2.

Command	MFR_FS															
Format	Direct															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	x	x	x	x	x	x	MFR_FS								

Bits	Bit Name	Description
15:9	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
8:0	MFR_FS	Sets the switching frequency in direct format. 10kHz/LSB.

MFR_OCP_TOTAL_SET (EEh) *(Page 1)*

The MFR_OCP_TOTAL_SET command on Page 1 sets the Rail 2 OCP_Total-related options and values.

Command	MFR_OCP_TOTAL_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x			OCP_TOTAL_TBLANK						OCP_TOTAL_CUR						

Bits	Bit Name	Description
15	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
14:13	OCP_TOTAL_MODE	Sets the OCP_Total action mode. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
12:7	OCP_TOTAL_TBLANK	Sets the blanking time for OCP_Total in direct format. 100μs/LSB.
6:0	OCP_TOTAL_CUR	Sets the Rail 2 per-phase OCP_Total entry threshold in direct format. 1A/LSB.

MFR_OCP_PHASE_SET (F0h) *(Page 1)*

The MFR_OCP_PHASE_SET command on Page 1 sets the Rail 2 per-phase valley current limit.

Command	MFR_OCP_PHASE_SET							
Format	Direct							
Bit	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	x	PHASE_CUR_LIMIT						

Bits	Bit Name	Description
7	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
6:0	PHASE_CUR_LIMIT	Sets the per-phase valley current limit in direct format. 1A/LSB.

MFR_OVP_UVP_SET (F1h) *(Page 1)*

The MFR_OVP_UVP_SET command on Page 1 provides two bytes to program the options and values of Rail 2 V_{OUT} OVP and UVP.

Command	MFR_OVP_UVP_SET															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function				OVP2_BLANK_TIME							UVP_BLANK_TIME					

Bits	Bit Name	Description
15:14	OVP2_MODE	Selects the OVP2 action mode. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry three or six times, determined by bit[13] below
13	OVP2_RETRY_TIMES	Sets the number of retry times when bit[15:14] (OVP2_MODE) = 2'b11. 1'b1: retry three times 1'b0: retry six times
12:8	OVP2_BLANK_TIME	Sets the OVP2 blanking time. When the OV2 condition remains for longer than the OVP2 blanking time, the OVP2 fault takes action. 50ns/LSB.
7:6	UVP_MODE	Selects the UVP action mode. 2'b00: no action 2'b01: latch off 2'b10: hiccup 2'b11: retry six times
5:0	UVP_BLANK_TIME	Sets the UVP blanking time. When the UV condition remains for longer than the UVP blanking time, the UVP fault takes action. 20μs/LSB.

CLEAR_EEPROM_FAULTS (FFh) *(Page 1)*

This command is used to clear the EEPROM fault. This command is write only. There is no data byte for this command.

PAGE 29 REGISTER MAP

PVID_VID1_VBOOT1 (81h) *(Page 29)*

The PVID_VID1_VBOOT1 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed by the BOOT pin.

Command	PVID_VID1_VBOOT1															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID1_VBOOT1_R1								PVID1_VBOOT1_R2							

Bits	Bit Name	Description
15:8	PVID1_VBOOT1_R1	Sets the Rail 1 PVID voltage when the PVID1/PVID2/PVID3 = 3'b000. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0V. Refer to Table 2 for more information.
7:0	PVID1_VBOOT1_R2	Sets the Rail 2 PVID voltage when the pins PVID1/PVID2/PVID3 = 3'b000. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0V. Refer to Table 2 for more information.

PVID_VID2_VBOOT2 (82h) *(Page 29)*

The PVID_VID2_VBOOT2 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed by the BOOT pin.

Command	PVID_VID2_VBOOT2															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID2_VBOOT2_R1								PVID2_VBOOT2_R2							

Bits	Bit Name	Description
15:8	PVID2_VBOOT2_R1	Sets the Rail 1 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b001. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.057V. Refer to Table 2 for more information.
7:0	PVID2_VBOOT2_R2	Sets the Rail 2 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b001. Refer to Table 4 for more information. Also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.057V. Refer to Table 2 for more information.

PVID_VID3_VBOOT3 (83h) *(Page 29)*

The PVID_VID3_VBOOT3 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed by the BOOT pin.

Command	PVID_VID3_VBOOT3															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID3_VBOOT3_R1								PVID3_VBOOT3_R2							

Bits	Bit Name	Description
15:8	PVID3_VBOOT3_R1	Sets the Rail 1 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b010. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.116V. Refer to Table 2 for more information.
7:0	PVID3_VBOOT3_R2	Sets the Rail 2 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b010. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.116V. Refer to Table 2 for more information.

PVID_VID4_VBOOT4 (84h) *(Page 29)*

The PVID_VID4_VBOOT4 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed by the BOOT pin.

Command	PVID_VID4_VBOOT4															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID4_VBOOT4_R1								PVID4_VBOOT4_R2							

Bits	Bit Name	Description
15:8	PVID4_VBOOT4_R1	Sets the Rail 1 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b011. Refer to Table 4 for more information. This bit also sets the boot up-voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.205V. Refer to Table 2 for more information.
7:0	PVID4_VBOOT4_R2	Sets the Rail 2 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b011. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.205V. Refer to Table 2 for more information.

PVID_VID5_VBOOT5 (85h) *(Page 29)*

The PVID_VID5_VBOOT5 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed the BOOT pin.

Command	PVID_VID5_VBOOT5															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID5_VBOOT5_R1								PVID5_VBOOT5_R2							

Bits	Bit Name	Description
15:8	PVID5_VBOOT5_R1	Sets the Rail 1 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b100. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.340V. Refer to Table 2 for more information.
7:0	PVID5_VBOOT5_R2	Sets the Rail 2 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b100. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.340V. Refer to Table 2 for more information.

PVID_VID6_VBOOT6 (86h) *(Page 29)*

The PVID_VID6_VBOOT6 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed by the BOOT pin.

Command	PVID_VID6_VBOOT6															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID6_VBOOT6_R1								PVID6_VBOOT6_R2							

Bits	Bit Name	Description
15:8	PVID6_VBOOT6_R1	Sets the Rail 1 PVID voltage when the pins PVID1/PVID2/PVID3 = 3'b101. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.540V. Refer to Table 2 for more information.
7:0	PVID6_VBOOT6_R2	Sets the Rail 2 PVID voltage when the pins PVID1/PVID2/PVID3 = 3'b101. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.540V. Refer to Table 2 for more information.

PVID_VID7_VBOOT7 (87h) *(Page 29)*

The PVID_VID7_VBOOT7 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed by the BOOT pin.

Command	PVID_VID7_VBOOT7															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID7_VBOOT7_R1								PVID7_VBOOT7_R2							

Bits	Bit Name	Description
15:8	PVID7_VBOOT7_R1	Sets the Rail 1 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b110. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.844V. Refer to Table 2 for more information.
7:0	PVID7_VBOOT7_R2	Sets the Rail 2 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b110. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 0.844V. Refer to Table 2 for more information.

PVID_VID8_VBOOT8 (88h) *(Page 29)*

The PVID_VID8_VBOOT8 register on Page 29 provides two bytes to pre-program the PVID voltage in PVID override mode and V_{BOOT} when the boot-up voltage is programmed by the BOOT pin.

Command	PVID_VID8_VBOOT8															
Format	VID format															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PVID8_VBOOT8_R1								PVID8_VBOOT8_R2							

Bits	Bit Name	Description
15:8	PVID8_VBOOT8_R1	Sets the Rail 1 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b111. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 1.301V. Refer to Table 2 for more information.
7:0	PVID8_VBOOT8_R2	Sets the Rail 2 PVID voltage when pins PVID1/PVID2/PVID3 = 3'b111. Refer to Table 4 for more information. This bit also sets the boot-up voltage when V_{BOOT} is set from the BOOT pin and the BOOT pin voltage is 1.301V. Refer to Table 2 for more information.

PRODUCT_REV_USER (F9h) *(Page 29)*

The PRODUCT_REV_USER command on Page 29 provides two bytes for users to record and trip the product revisions.

Command	PRODUCT_REV_USER															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PRODUCT_REV_USER															

Bits	Bit Name	Description
15:0	PRODUCT_REV_USER	Provides two bytes for users to record and trip the product revisions.

MFR_STORE_FAULTS1 (FCh) *(Page 29)*

The MFR_STORE_FAULTS1 register on Page 29 records the fault types of the last power cycle. To clear the fault bits, write 0x0000 to this register and wait 5ms.

Command	MFR_STORE_FAULTS1															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	x	x		CS_FAULT_TRG												

Bits	Bit Name	Description
15:14	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
13	VTEMP_FAULT_TRG	VTEMP pin fault indicator. When the voltage on the VTEMP pin is higher than 1.25V, this bit indicates that a fault has been triggered. 1'b0: no VTEMP fault 1'b1: VTEMP fault has occurred
12:10	CS_FAULT_TRG	CS_FAULT indicators. 3'b000: no CS fault is detected 3'b001: CS fault has been detected on pin CS1 3'b010: CS fault has been detected on pin CS2 3'b011: CS fault has been detected on pin CS3 3'b100: CS fault has been detected on pin CS4 3'b101: CS fault has been detected on pin CS5 3'b110: CS fault has been detected on pin CS6 3'b111: CS fault has been detected on pin CS7

9	VIN_OV_FLAG	VIN_OV fault indicator. 1'b0: no VIN_OV fault 1'b1: VIN_OV fault has occurred
8	VIN_UVLO_FLAG	VIN_UVLO fault indicator. 1'b0: no VIN_UVLO fault 1'b1: VIN_UVLO fault has occurred
7	VCCIO_FLAG	VCCIO fault indicator. 1'b0: no VCCIO fault 1'b1: VCCIO fault has occurred
6	OTP_FLAG	Power stage over-temperature indicator. 1'b0: no power stage over-temperature fault has been detected on VTEMP 1'b1: over-temperature fault has been detected on VTEMP
5	OVP_FLAG1	Rail 1 V_{OUT} OVP fault indicator. 1'b0: no V_{OUT} OV fault 1'b1: V_{OUT} OV fault has occurred
4	UVP_FLAG1	Rail 1 V_{OUT} UVP fault indicator. 1'b0: no V_{OUT} UV fault 1'b1: V_{OUT} UV fault has occurred
3	OCP_FLAG1	Rail 1 OCP_Total fault indicator. 1'b0: no OCP_Total fault 1'b1: OCP_Total fault has occurred
2	OVP_FLAG2	Rail 2 V_{OUT} OVP fault indicator. 1'b0: no V_{OUT} OV fault 1'b1: V_{OUT} OV fault has occurred
1	UVP_FLAG2	Rail 2 V_{OUT} UVP fault indicator. 1'b0: no V_{OUT} UV fault 1'b1: V_{OUT} UV fault has occurred
0	OCP_FLAG2	Rail 2 OCP_Total fault indicator. 1'b0: no OCP_Total fault 1'b1: an OCP_Total fault has occurred

MFR_ STORE_FAULTS2 (FDh) *(Page 29)*

The MFR_STORE_FAULTS2 register on Page 29 records the PWM fault types of the last power cycle. To clear the fault bits, write 0x0000 to this register and wait 5ms.

Command	MFR_ STORE_FAULTS2															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PWM1_FAULTS				PWM2_FAULTS				PWM3_FAULTS				PWM4_FAULTS			

Bits	Bit Name	Description
15:12	PWM1_FAULTS	Intelli-Phase fault type indication of phase 1. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over temperature protection 4'b1000: SW-PGND short protection

11:8	PWM2_FAULTS	Intelli-Phase fault type indication of phase 2. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
7:4	PWM3_FAULTS	Intelli-Phase fault type indication of phase 3. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
3:0	PWM4_FAULTS	intelli-Phase fault type indication of phase 4. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection

MFR_ STORE_FAULTS3 (FEh) *(Page 29)*

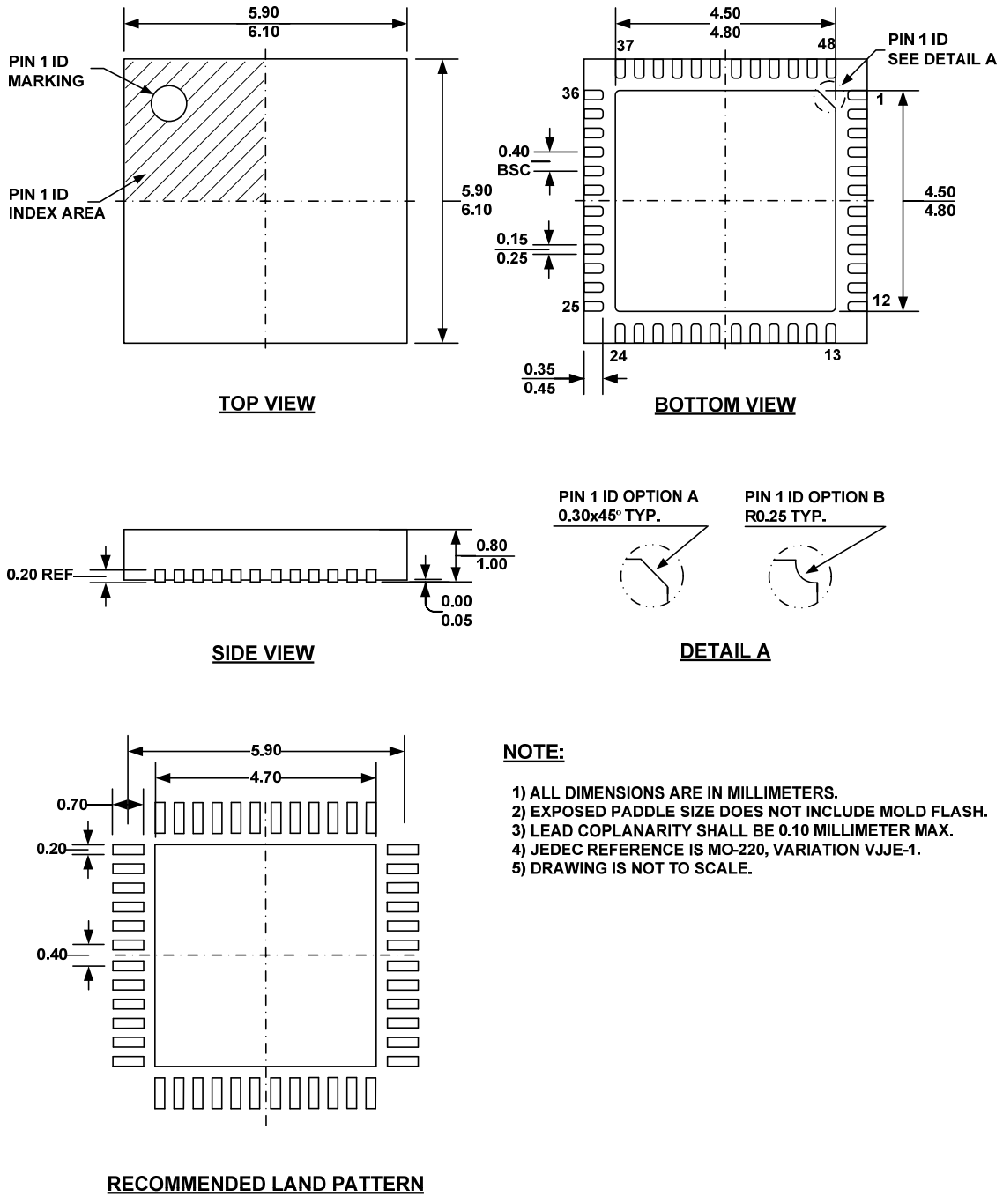
The MFR_STORE_FAULTS3 register on Page 29 records the PWM fault types of the last power cycle. To clear the fault bits, write 0x0000 to this register and wait 5ms.

Command	MFR_ STORE_FAULTS3															
Format	Unsigned binary															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom	rom
Function	PWM5_FAULTS				PWM6_FAULTS				x	x	x	x	PWM7_FAULTS			

Bits	Bit Name	Description
15:12	PWM5_FAULTS	Intelli-Phase fault type indication of phase 5. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
11:8	PWM6_FAULTS	Intelli-Phase fault type indication of phase 6. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection
7:4	RESERVED	Unused. X indicates that writes are ignored and reads are always 0.
3:0	PWM7_FAULTS	Intelli-Phase fault type indication of phase 7. 4'b0000: no fault 4'b0001: VIN-SW short 4'b0010: current-limit protection 4'b0100: over-temperature protection 4'b1000: SW-PGND short protection

PACKAGE INFORMATION

QFN-48 (6mmx6mm)



NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VJJE-1.
5) DRAWING IS NOT TO SCALE.