MP3359C

1/2/3/4-Channel, Max 160mA/Ch, Boost WLED Controller with High Dimming Ratio

DESCRIPTION

The MP3359C is a step-up controller with four channel current sources. The device is designed to drive white LED (WLED) arrays as backlighting for small- or medium-sized LCD panels.

The MP3359C as a boost controller uses peak current control mode as its pulse-width modulation (PWM) control architecture to regulate a boost converter, which is composed of input capacitors, inductor, MOSFET, diode, output capacitors, etc. It drives an external MOSFET to boost the output voltage (V_{OUT}) from a 3.5V to 40V input voltage (V_{IN}) supply. The switching frequency (f_{SW}) can be configured via a resistor or external clock.

Four channel current sources are applied to the LED cathode to adjust LED brightness. The MP3359C regulates the current in each LED string to the value set by an external current-setting resistor, with 2.5% current regulation accuracy between strings.

A low headroom voltage is provided to improve efficiency and IC thermal performance.

The MP3359C provides analog and PWM dimming with two separate input pins (EN/ADIM and PDIM). The device also has a fixed delay time between LED current channels to eliminate noise during PWM dimming.

Robust protections are included to guarantee safe device operation. Protection features include input current (I_{IN}) over-current protection (OCP), cycle-by-cycle current limiting, over-voltage protection (OVP), over-temperature protection (OTP), LED short/open protection, LEDx short-to-GND protection, and V_{OUT} short-to-GND protection.

The MP3359C is available in a QFN-20 (3mmx4mm) package.

FEATURES

- 3.5V to 40V Input Voltage (V_{IN}) Range
- 4 Channels with a Maximum of 160mA per Channel
- Configurable Switching Frequency (f_{SW}) Up to 2.2MHz
- External Sync Switching (SW) Function
- Pulse-Width Modulation (PWM) Dimming
- Analog Dimming
- Deep Dimming Ratio
- Excellent EMI Performance and Frequency Spread Spectrum (FSS)
- Fixed 100µs Delay Time between LED Current Channels during PWM Dimming (Replace Phase Shift)
- 2.5% Current Matching
- Cycle-by-Cycle Current Limiting
- Disconnect Output Voltage (V_{OUT}) from V_{IN}
- Input Over-Current Protection (OCP)
- LED String Open/Short Protection
- Over-Temperature Protection (OTP)
- LEDx Pin Short-to-GND Protection
- V_{OUT} Short-to-GND Protection
- Able to Disable LED4 if LED4 Is Unused
- Fault Indicator Signal Output
- Available in a QFN-20 (3mmx4mm) Package

APPLICATIONS

- Tablets
- Notebooks

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION (1) (2) (3) (4)

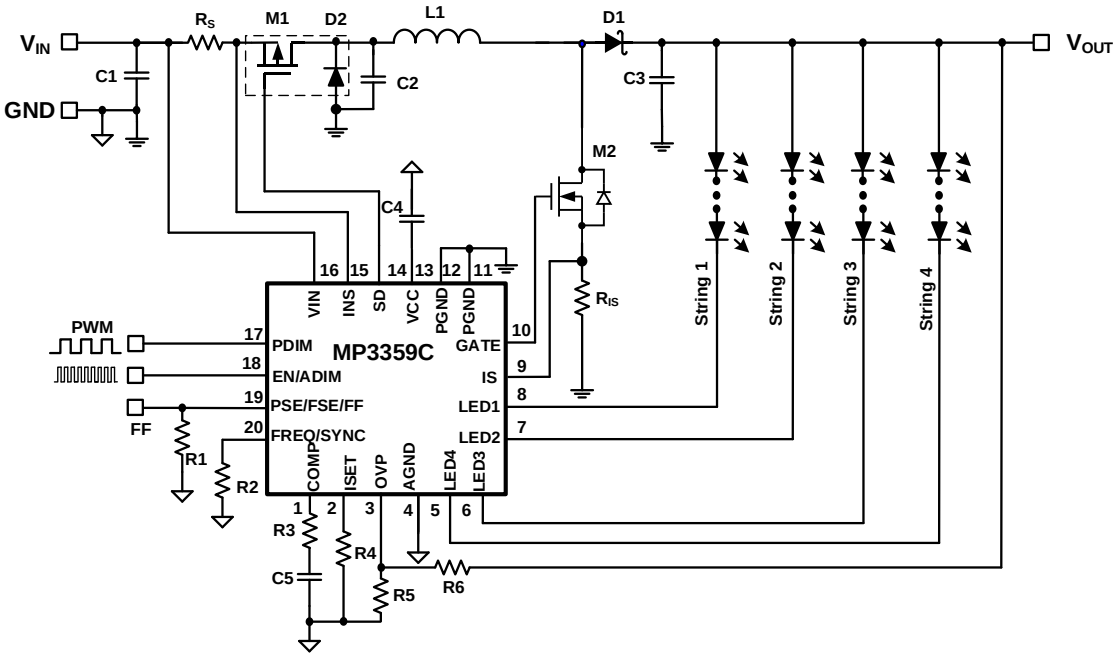


Figure 1: Typical Application Circuit with 4 Strings

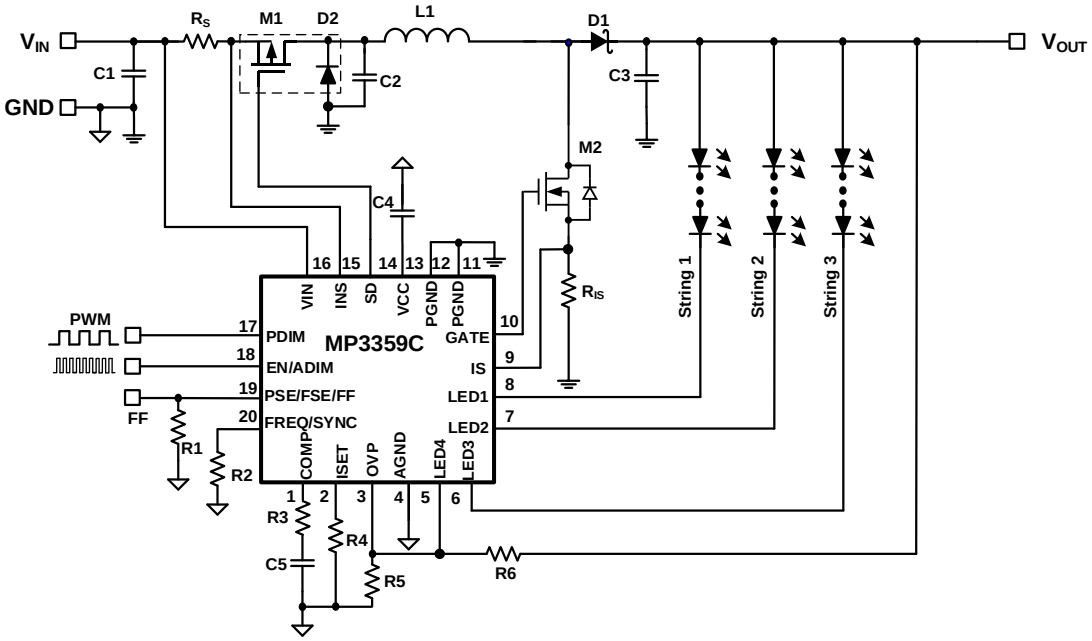


Figure 2: Typical Application Circuit with 3 Strings (Connect LED4 to the OVP Pin)

Notes:

1) For an application with one channel, tie the LED1~4 pins together.
2) For an application with two channels, tie the LED1~2 pins together, and tie the LED3~4 pins together.
3) For an application with three channels, connect the LED4 pin to the OVP pin.
4) M1 and D2 must be used together.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3359CGLE *	QFN-20 (3mmx4mm)	*See Below*	1

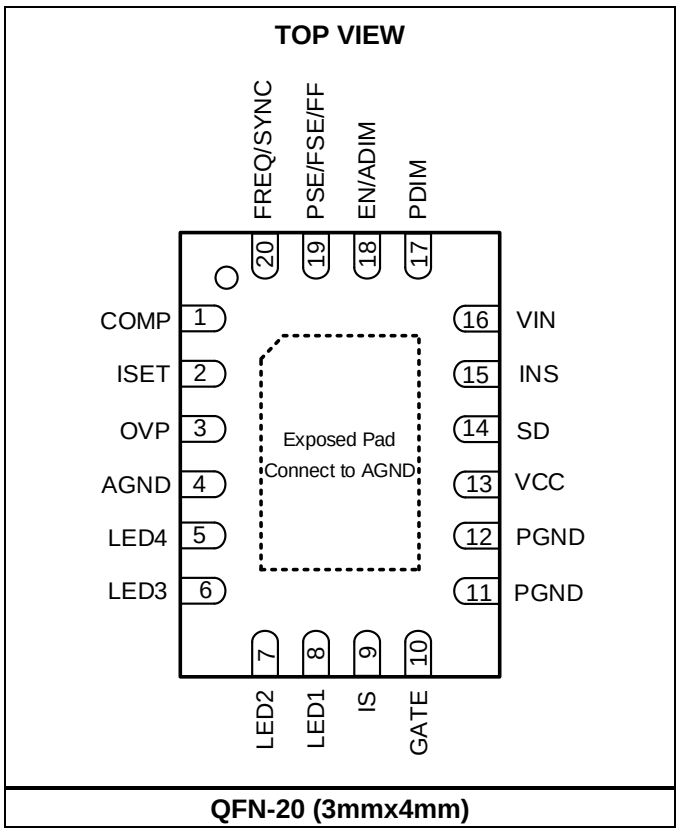
* For Tape & Reel, add suffix -Z (e.g. MP3359CGLE–Z).

TOP MARKING (MP3359CGLE)

MPYW
3359
CLLL
E

MP: MPS prefix
Y: Year code
W: Week code
3359C: Part number
LLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (3mmx4mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	COMP	**Compensation pin.**
2	ISET	**LED current setting.** Tie a current-setting resistor from ISET to GND to configure the current in each LED string.
3	OVP	**Over-voltage protection pin.** Connect a resistor divider from the output voltage (V_{OUT}) to the OVP pin and the OVP pin to AGND to configure the over-voltage protection (OVP) threshold.
4	AGND	**Analog ground.**
5	LED4	**LED string 4 current input.** Connect the LED string 4 cathode to this pin. If LED4 is not used, connect LED4 directly to the OVP pin.
6	LED3	**LED string 3 current input.** Connect the LED string 3 cathode to this pin.
7	LED2	**LED string 2 current input.** Connect the LED string 2 cathode to this pin.
8	LED1	**LED string 1 current input.** Connect the LED string 1 cathode to this pin.
9	IS	**Low-side MOSFET (LS-FET) current-sense (CS) pin.** During normal operation, the IS pin senses the voltage across the external inductor CS resistor (R_{IS}) for peak-current mode control. This pin also limits the inductor current (I_L) during every switching cycle.
10	GATE	**Power MOSFET driver output for the step-up converter.** The GATE pin drives the external N-channel MOSFET**.**
11, 12	PGND	**Step-up converter power ground.**
13	VCC	**5V LDO output pin.** VCC provides power to the internal logic and gate driver. Place a ceramic capacitor as close to this pin as possible to reduce noise.
14	SD	**External disconnect P-channel MOSFET gate drive pin.** The SD pin turns off the external P-channel MOSFET if a fault occurs. Float this pin if it is not used.
15	INS	**Input CS pin.** If the voltage across a current-sense resister (R_S) exceeds the input over-current protection (OCP) threshold, the MP3359C turns off the P-channel MOSFET. Connect this pin to VIN pin if it is not used.
16	VIN	**Power supply input.** The VIN pin supplies power to the IC.
17	PDIM	**Pulse-width modulation (PWM) dimming signal input pin.** Apply a PWM signal on the PDIM pin for PWM dimming. PDIM is pulled low internally; a 100Hz to 30kHz PWM signal is recommended.
18	EN/ADIM	**IC enable and analog dimming signal input pin.** Apply a PWM signal on the EN/ADIM pin for analog dimming. EN/ADIM is pulled low internally, and a >5kHz PWM signal is recommended. Pull this pin low for >60ms to shut down the IC.
19	PSE/FSE /FF	**Delay function enable, frequency spread spectrum (FSS) enable, and fault flag pin.** The PSE/FSE/FF pin is a current-source output (32μA). To configure the pin voltage, connect a resistor from this pin to AGND. After VIN and EN turn on, the IC detects the PSE/FSE/FF pin's voltage to enable the corresponding functions: • >2.85V: Enable the delay and FSS functions. • 2V to 2.55V: Enable only the delay function. • 1.27V to 1.8V: Enable only the FSS function. • <1.13V: Disable the delay and FSS functions. If the delay function is enabled, there is a fixed 100μs delay between the LED current channels to reduce system stress and eliminate noise during PWM dimming. FSS function improves EMI performance. The fault flag function indicates the status if a fault occurs, and is always enabled.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
20	FREQ/ SYNC	**Switching frequency (f_{SW}) setting and SYNC pin.** The FREQ/SYNC pin configures f_{SW}. Connect a resistor between FREQ/SYNC and GND to set the converter's f_{SW}, or connect an external clock to this pin to synchronize the boost f_{SW}.
Exposed pad	AGND	**Chip ground.** Connect the exposed pad to AGND.

ABSOLUTE MAXIMUM RATINGS (5)

Input voltage (V_{IN}) .....-0.3V to +42V
V_{LED1} to V_{LED4}.....-0.5V to +50V
V_{SD}, V_{INS} .....V_{IN} - 6V to V_{IN}
V_{SD}, V_{INS} .....> -0.3V
V_{IS} .....-0.3V to +5V
All other pins .....-0.3V to +6V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C
Continuous power dissipation (T_A = 25°C) (6)
QFN-20 (3mmx4mm)..... 3.59W

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±2kV

Recommended Operating Conditions (7)

Supply voltage (V_{IN}) .....3.5V to 40V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (8) θ_{JA} θ_{JC}

QFN-20 (3mmx4mm)…….....34.8……1.7....°C/W

Notes:

5) Exceeding these ratings may damage the device.
6) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on a JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating input voltage	V_{IN}		3.5		40	V
Quiescent supply current	I_Q	No switching		3		mA
Shutdown supply current	I_{ST}	V_{IN} = 12V, V_{EN} = 0V			1	μA
V_{IN} under-voltage lockout (UVLO) threshold	V_{IN_UVLO}	Rising edge		3.25	3.45	V
V_{IN} UVLO hysteresis				250		mV
Low-dropout (LDO) regulator output voltage	V_{CC}	V_{EN} = 2V, 6V < V_{IN} < 24V, 0mA < I_{VCC} < 10mA	4.8	5	5.4	V
Enable (EN) on threshold	V_{EN_ON}	V_{EN} rising	1.4			V
EN off threshold	V_{EN_OFF}	V_{EN} falling			0.5	V
EN/ADIM and PDIM pull-down resistance	$R_{EN/ADIM}$			1		MΩ
PSE/FSE/FF source current	I_{PSE}		29.7	32	34.3	μA
Step-Up Converter						
Gate driver sourcing impedance	R_{GATE_SO}	V_{GATE} = 5V		4		Ω
Gate driver sinking impedance	R_{GATE_SI}	V_{GATE} = 5V, I_{GATE} = 10mA		2.5		Ω
Switching frequency	f_{SW}	R_{FREQ} = 10kΩ	1.85	2.05	2.25	MHz
		R_{FREQ} = 50kΩ	400	440	480	kHz
FREQ voltage	V_{FREQ}		-5%	1.1	+5%	V
Maximum duty cycle	D_{MAX}	f_{SW} = 440kHz	92			%
Cycle-by-cycle current limiting	V_{LIM_CYC}		230	300		mV
SYNC low threshold	V_{SYNC_LO}	V_{SYNC} falling			0.5	V
SYNC high threshold	V_{SYNC_HI}	V_{SYNC} rising	1.4			V
COMP transconductance	G_{COMP}	ΔI_{COMP} ≤ 10μA		100		μA/V
COMP source current limit	I_{COMP_SO}			90		μA
COMP sink current limit	I_{COMP_SI}			90		μA
Current Dimming						
PDIM/ADIM input low threshold	V_{DIM_LO}	V_{DIM} falling			0.5	V
PDIM/ADIM input high threshold	V_{DIM_HI}	V_{DIM} rising	1.4			V
LED Current Regulator						
LEDx regulation voltage	V_{HD}	LED current (I_{LED}) = 20mA		350		mV
		I_{LED} = 100mA		650		mV
Current matching [9]		I_{LED} = 20mA	-2.5		+2.5	%
		I_{LED} = 100mA	-2.5		+2.5	%
ISET voltage	V_{ISET}			1.2		V
LED current	I_{LED}	R_{ISET} = 12kΩ	97	100	103	mA
		R_{ISET} = 24kΩ, ADIM duty = 2%, I_{LED} = 1/50 x 50mA = 1mA	0.7	0.9	1.1	mA
Delay time	t_{DELAY}	Between LED current channels		100		μs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Protection						
Over-voltage protection (OVP) threshold	V_{OVP}		1.9	2	2.1	V
OVP hysteresis				200		mV
OVP UVLO threshold	V_{OVP_UV}	Step-up converter fails		100		mV
Input over-current protection (OCP) threshold	V_{IN_OCP}	Input current sense	80	100	120	mV
INS sink current	I_{INS}		16	20	24	µA
LEDx over-voltage (OV) threshold	V_{LEDX_OV}			5		V
LEDx OV fault timer	t_{LEDX_OV}			7.7		ms
LEDx UVLO threshold	V_{LEDX_UV}			100		mV
Thermal shutdown threshold (10)	T_{ST}	Rising edge		170		°C
		Hysteresis		20		°C
SD pull-down current	I_{SD}			60		µA
SD voltage (respective to V_{IN})	V_{SD-IN}	V_{IN} = 12V, V_{IN} - V_{SD}		5.3		V

Notes:

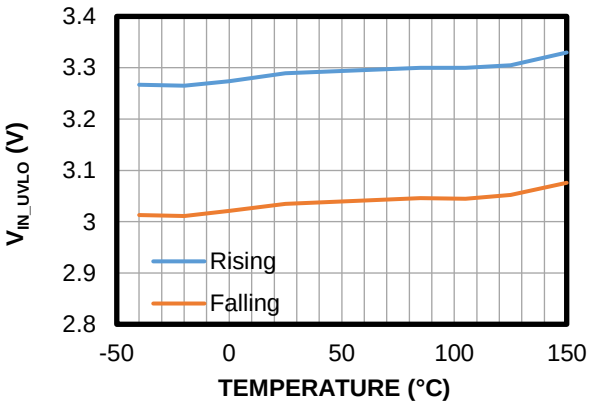
9) Matching is defined as the difference between the maximum current and minimum current, divided by 2 times the average current.
10) Guaranteed by design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

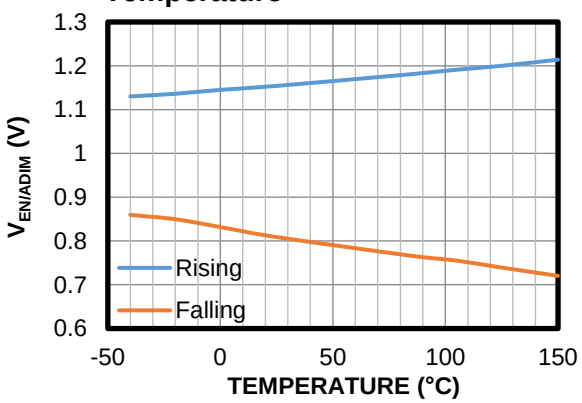
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, unless otherwise noted.

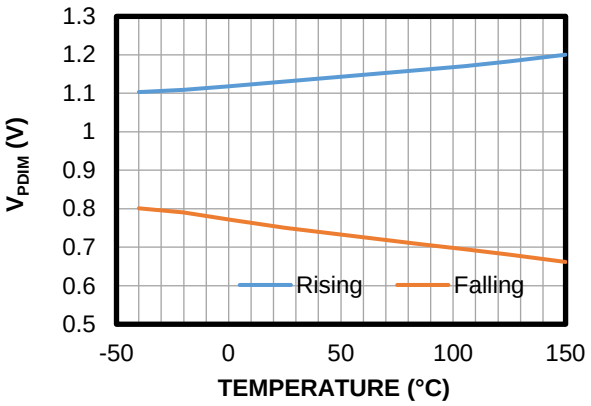
V_{IN} UVLO Threshold vs. Temperature



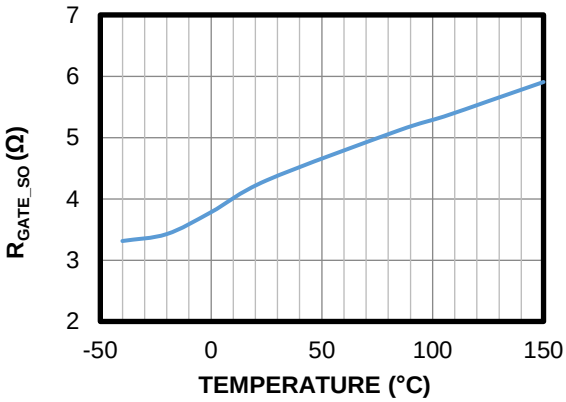
EN/ADIM Threshold vs. Temperature



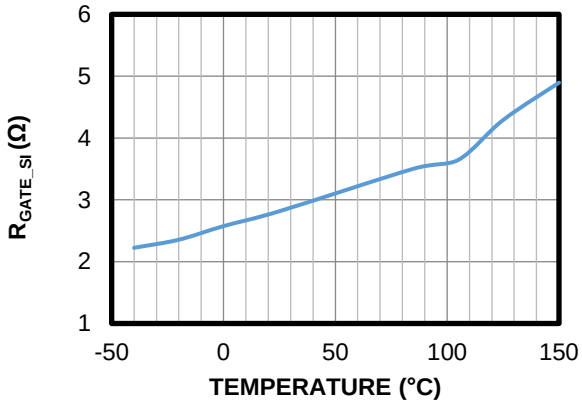
PDIM Threshold vs. Temperature



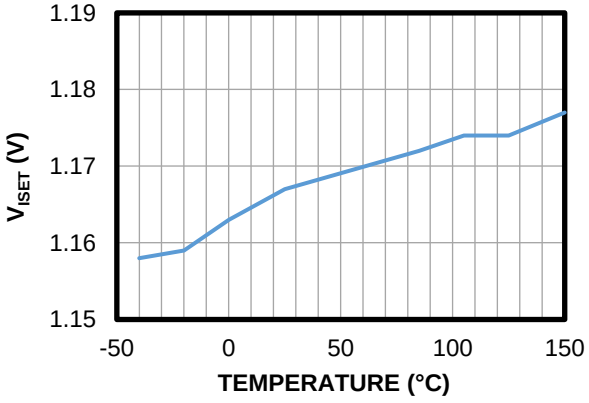
Gate Driver Source Impedance (R_{GATE_SO}) vs. Temperature



Gate Driver Sink Impedance (R_{GATE_SI}) vs. Temperature



ISET Voltage vs. Temperature

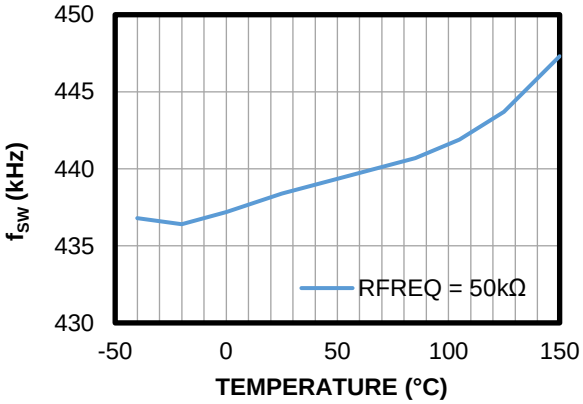


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

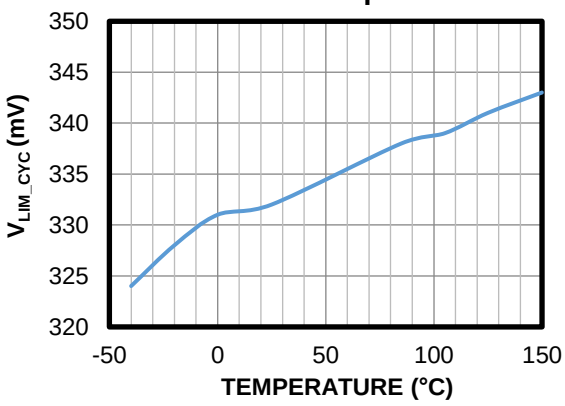
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +150°C, unless otherwise noted.

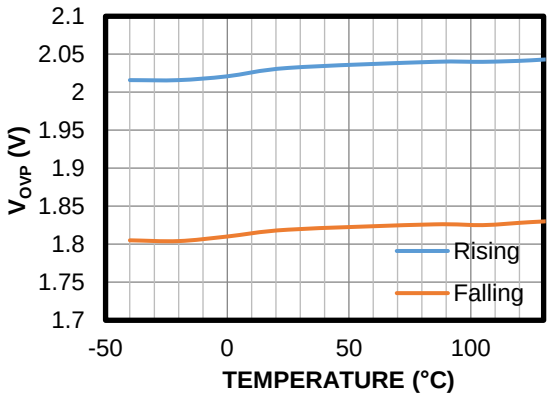
Switching Frequency vs. Temperature



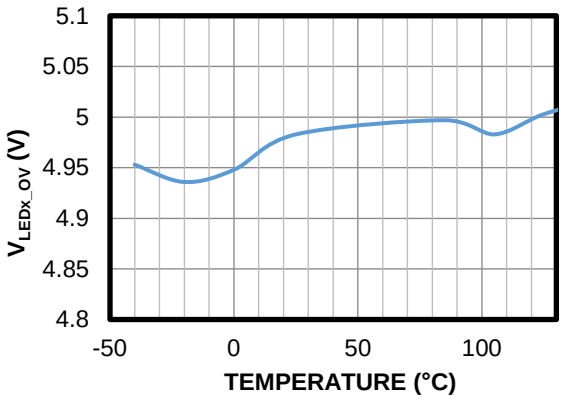
Cycle-by-Cycle Current Limit Threshold vs. Temperature



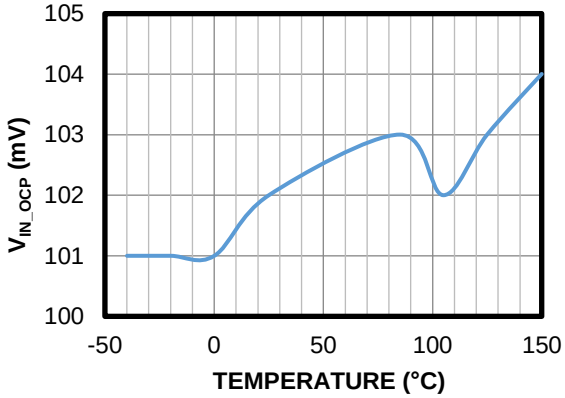
OVP Threshold vs. Temperature



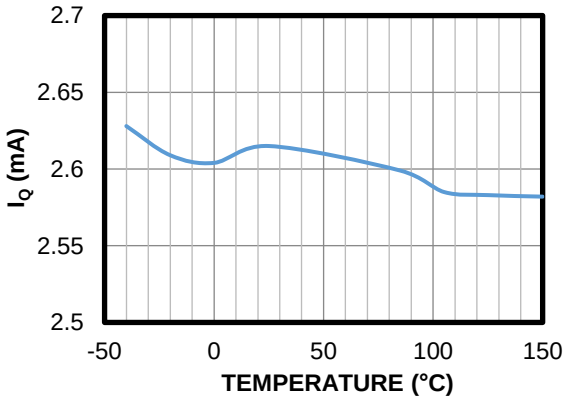
V_{LEDx} Over-Voltage Threshold vs. Temperature



I_{IN} OCP Threshold vs. Temperature



Quiescent Current vs. Temperature



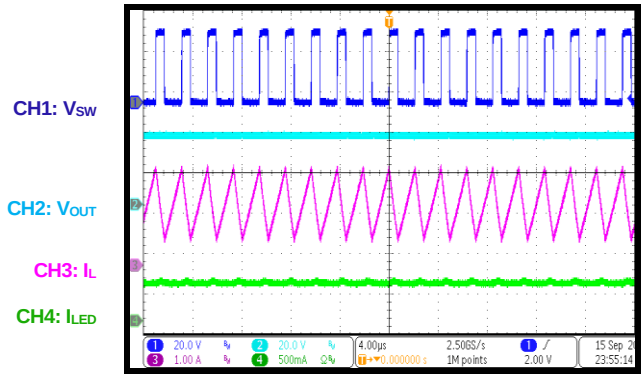
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, 4 strings, 12 LEDs in series, 120mA/string, L = 15µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted.

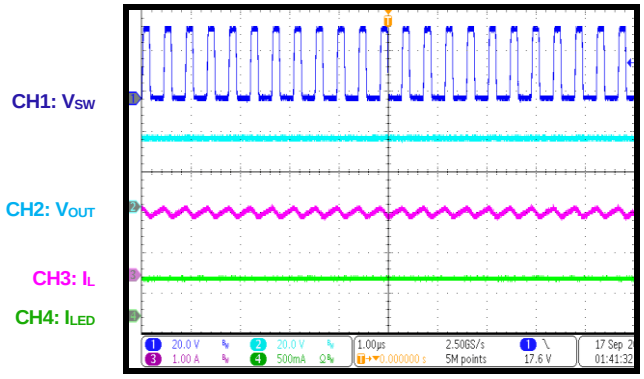
Steady State

f_{SW} = 440kHz

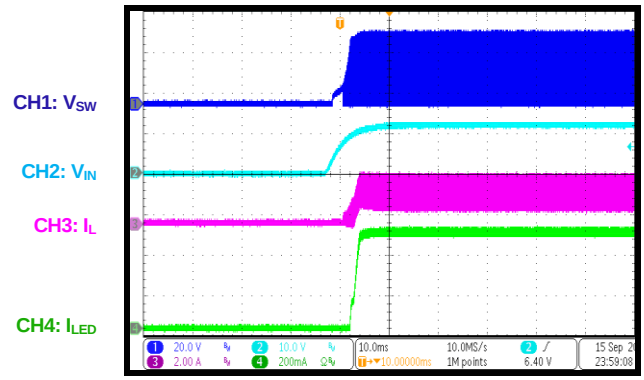


Steady State

f_{SW} = 2.2MHz

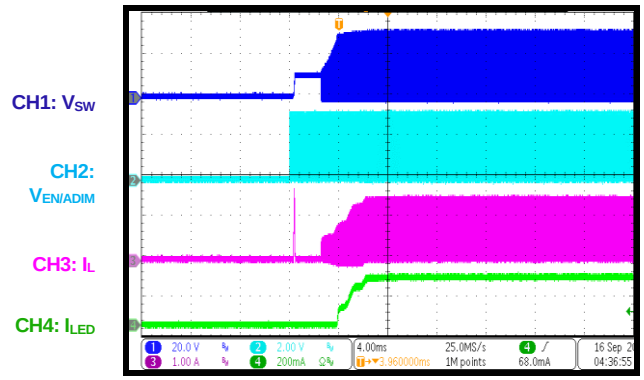


Start-Up through VIN



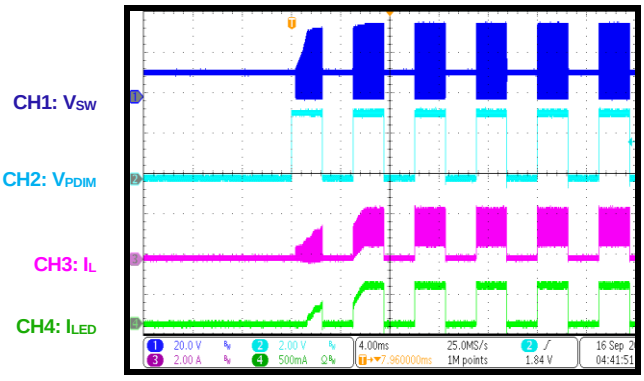
Start-Up through EN/ADIM

$f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 50%



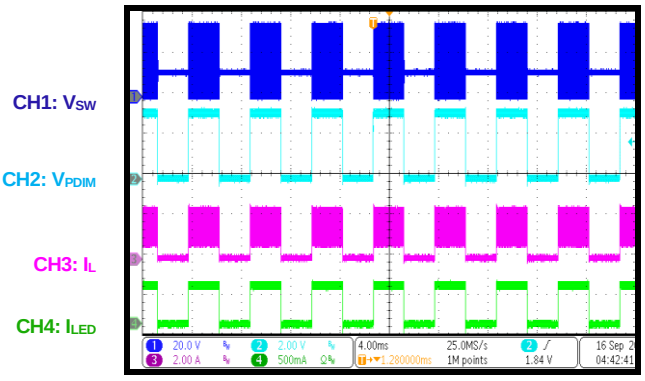
Start-Up through PDIM

f_{PDIM} = 200Hz, D_{PDIM} = 50%



PWM Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 50%



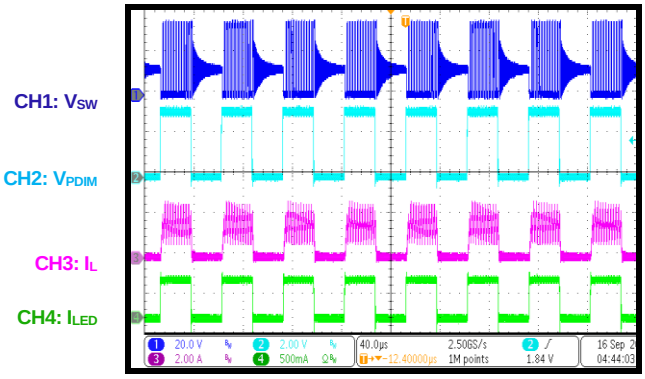
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, 4 strings, 12 LEDs in series, 120mA/string, L = 15µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted.

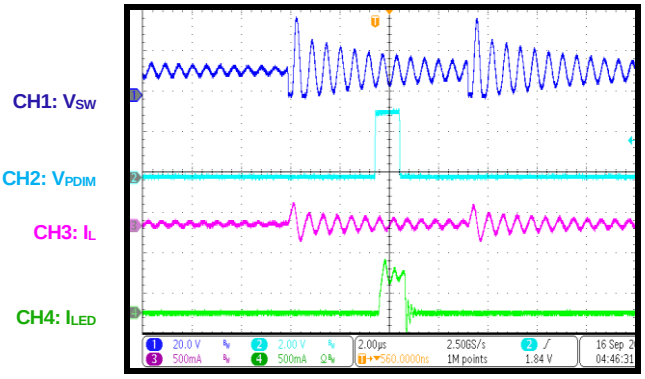
PWM Dimming

f_{PDIM} = 20kHz, D_{PDIM} = 50%



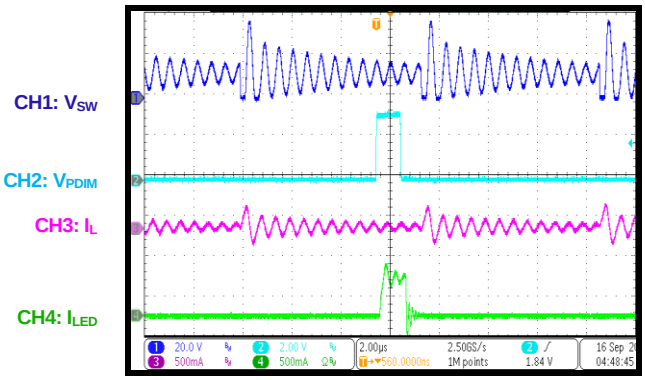
PWM Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 0.02%



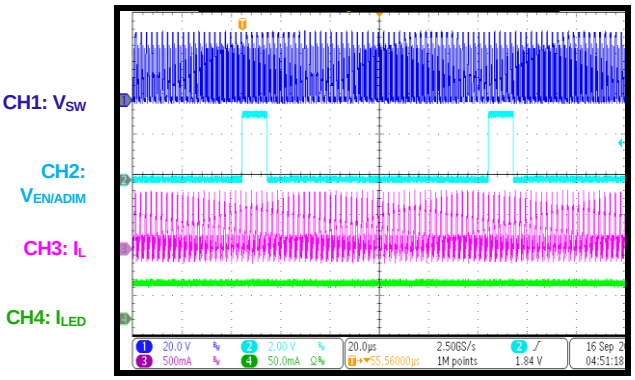
PWM Dimming

f_{PDIM} = 100Hz, D_{PDIM} = 0.01%



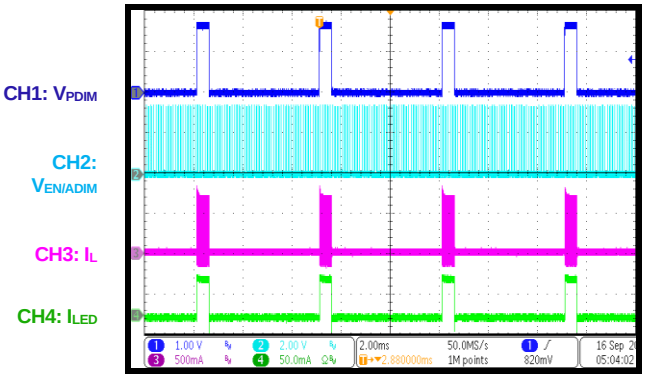
Analog Dimming

$f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 10%



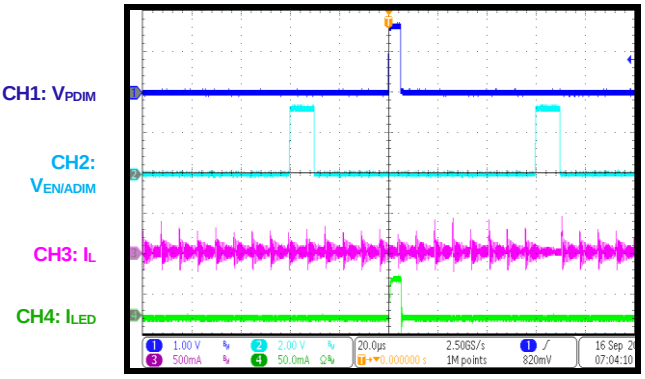
Both PWM Dimming and Analog Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 10%, $f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 10%



Both PWM Dimming and Analog Dimming

f_{PDIM} = 200Hz, D_{PDIM} = 0.1%, $f_{EN/ADIM}$ = 10kHz, $D_{EN/ADIM}$ = 10%



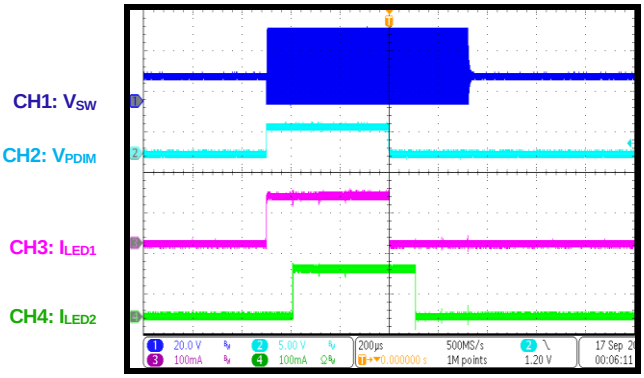
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

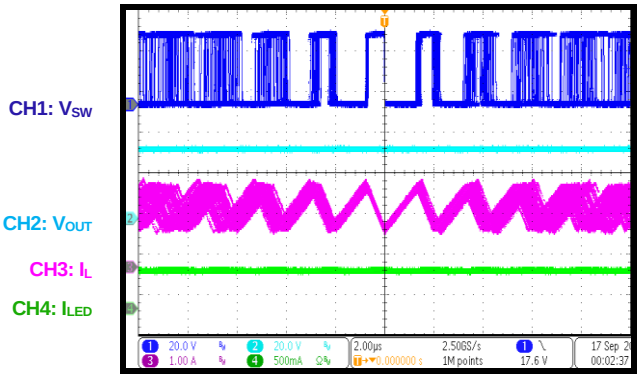
V_{IN} = 12V, 4 strings, 12 LEDs in series, 120mA/string, L = 15µH, f_{SW} = 440kHz, T_A = 25°C, unless otherwise noted.

PWM Dimming with 100µs Delay Time Function

f_{PDIM} = 200Hz, D_{PDIM} = 10%

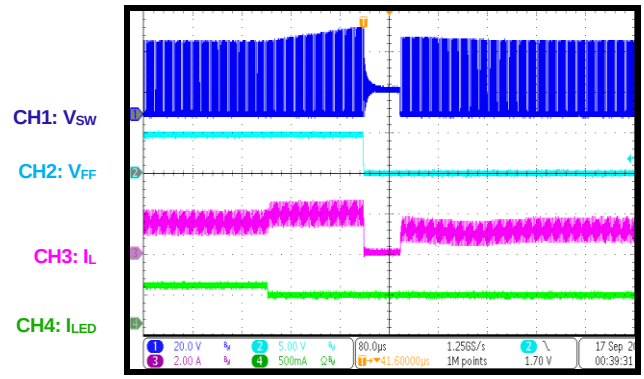


Frequency Spread Spectrum



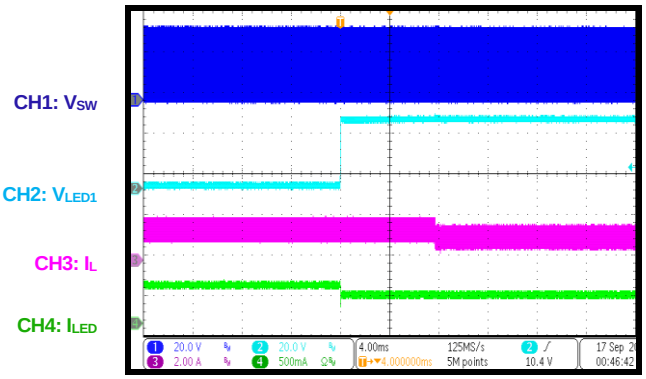
LED Open Protection

Open LED1 under normal operation



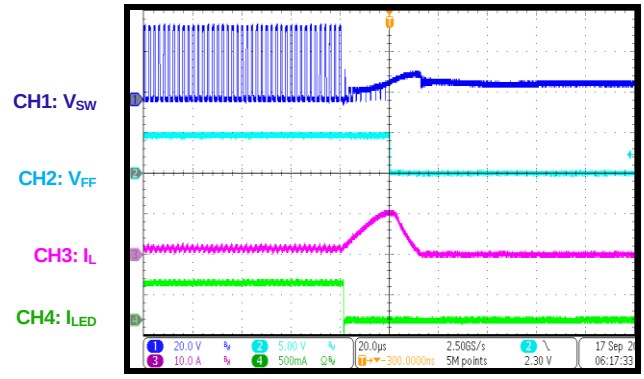
LED Short Protection

short LED1 under normal operation

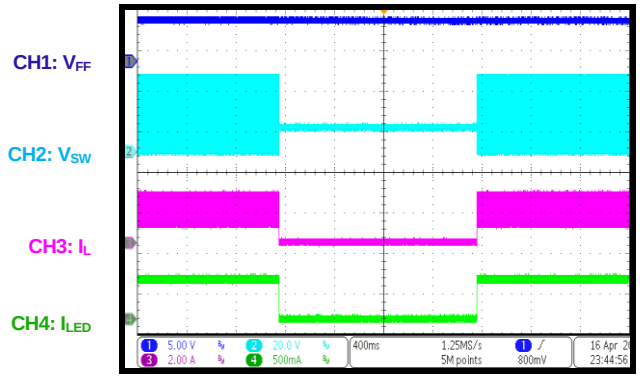


V_{OUT} Short-to-GND Protection

Set the input OCP threshold = 10A



Over-Temperature Protection



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

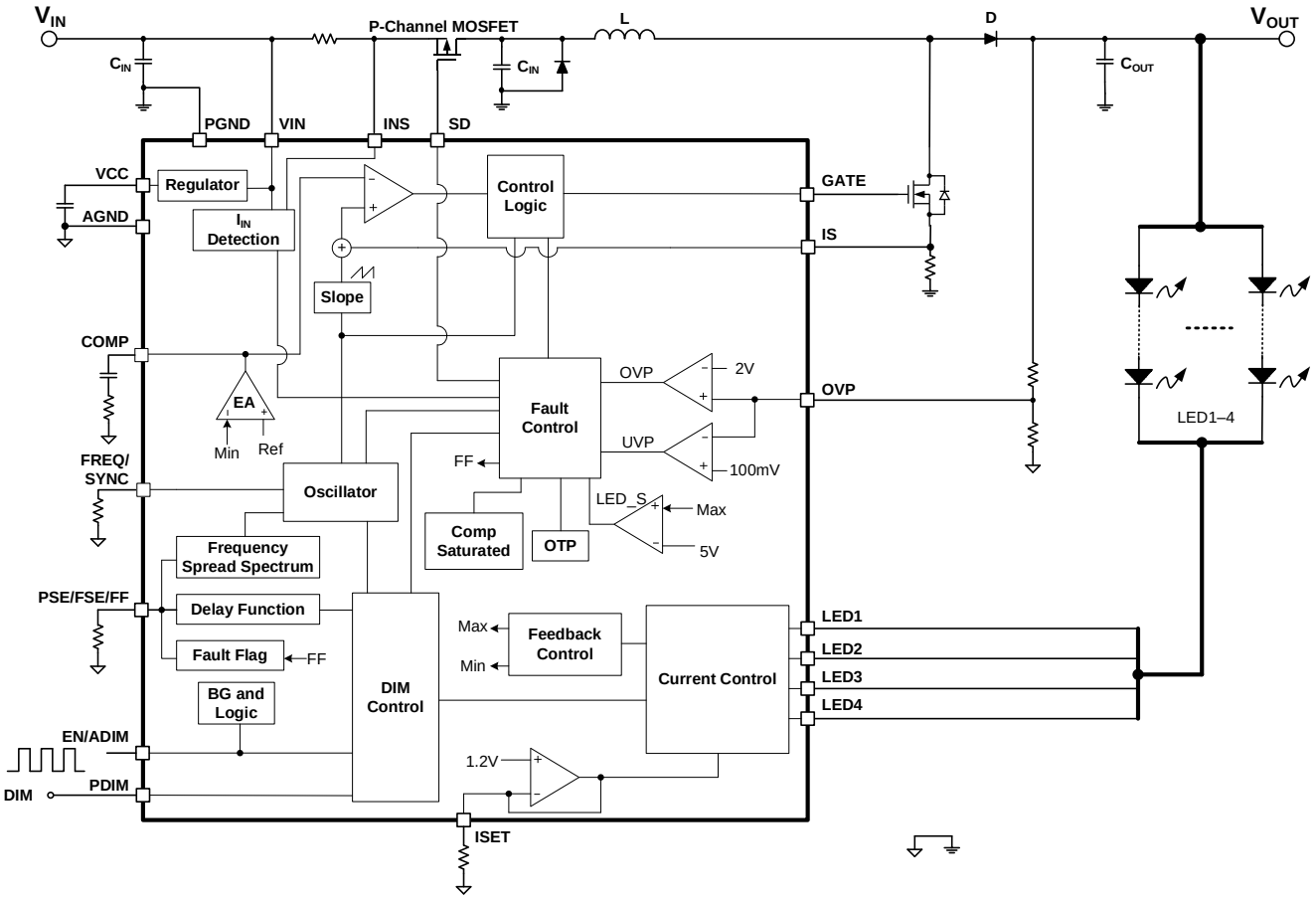


Figure 3: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

OPERATION

The MP3359C is a configurable, fixed-frequency, peak current control mode step-up controller with up to four channels of regulated current sources to drive an array of white LEDs (WLEDs).

Internal 5V Regulator

The MP3359C includes an internal linear regulator (VCC). When the input voltage (V_{IN}) exceeds 6V, this regulator provides a 5V power supply to the external MOSFET gate driver and the internal control circuitry. When the device shuts down, the VCC voltage (V_{CC}) drops to 0V. The device remains disabled until V_{CC} exceeds its under-voltage lockout (UVLO) threshold.

System Start-Up

Once enabled, the MP3359C checks the topology connection. The IC draws current from the SD pin to turn on the P-channel MOSFET if it is used. The device then monitors the OVP pin to see if the output is shorted to PGND. If the OVP pin's voltage (V_{OVP}) is below 100mV, the device is disabled and latches off. The MP3359C continues to check other safety limits (e.g. over-voltage protection (OVP)). If all protection tests pass, the IC starts boosting the step-up converter.

The recommended start-up sequence is listed below:

1. V_{IN}
2. EN/ADIM
3. Pulse-width modulation (PWM) dimming signal

Step-Up Converter

The MP3359C employs peak current control mode to regulate the output power (P_{OUT}). At the beginning of each switching cycle, the internal clock turns on the external N-channel MOSFET. During normal operation, the minimum turn-on time is about 100ns. A stabilizing ramp is added to the current-sense (CS) amplifier's output to prevent subharmonic oscillations when the duty cycle exceeds 50%. This result is fed into the PWM comparator. When the summed voltage reaches the error amplifier's (EA's) output, the external N-channel MOSFET turns off.

The internal EA's output voltage is an amplified signal of the difference between the reference voltage (V_{REF}) and the feedback (FB) voltage (V_{FB}). The converter automatically chooses the lowest active LEDx pin voltage (V_{LEDx}) to act as V_{FB} to provide a sufficient output voltage (V_{OUT}) for all the LED arrays.

If V_{FB} drops below V_{REF}, the EA's output increases. Then more current flows through the N-channel MOSFET, which increases the power delivered to the output. This forms a closed loop that regulates V_{OUT}.

Under light-load operation (e.g. when V_{OUT} is almost equal to V_{IN}), the converter runs in pulse-skip mode (PSM) with a fixed f_{SW}. In this mode, the MOSFET turns on for a minimum on time (t_{ON_MIN}), then the converter discharges power to its output for the remaining period. The MOSFET remains off until V_{OUT} requires another boost.

Ability to Disable LED4 if LED4 Is Unused

If LED4 is unused, connect it directly to the OVP pin. The MP3359C can disable the LED4 block and remove it from the boost loop. Then the PSE/FSE/FF pin can provide optimal performance for 3-string applications.

Dimming Control

The MP3359C provides analog and PWM dimming with two separate EN/ADIM and PDIM input pins. These dimming modes are described below.

Pulse-Width Modulation (PWM) Dimming Mode

When a PWM signal is applied to the PDIM pin, the LED current (I_{LED}) amplitude remains at the full-scale I_{LED}, and the I_{LED} duty cycle is the same as the input PWM signal duty cycle. The I_{LED} duty cycle follows the PWM input duty cycle, and the I_{LED} frequency is the same as the PWM input.

Analog Dimming Mode

The PWM input signal is connected to the EN/ADIM pin. The I_{LED} amplitude is equal to I_{SET} x D_{DIM}, where I_{SET} is the full-scale I_{LED}, and D_{DIM} is the duty of the input PWM signal. To improve analog dimming performance, a PWM signal above 5kHz is recommended.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

To ensure good performance with a small dimming ratio, the minimum V_{LEDx} rises to 1.2V when the dimming duty cycle is below 10%. Analog dimming supports a 200:1 dimming ratio.

Deep Dimming Ratio for PWM Dimming

When the PWM pin on time is shorter than 5µs, V_{OUT} is regulated to be 93% of V_{OVP} (see Figure 4).

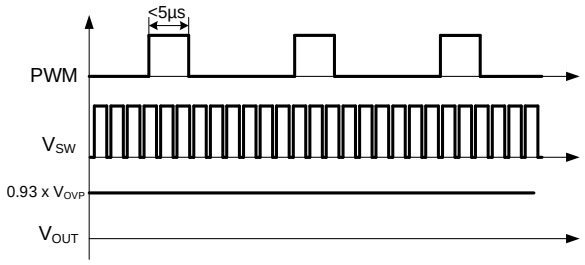


Figure 4: Deep Dimming Ratio for PWM Dimming

PSE/FSE/FF Pin

When V_{CC} exceeds its UVLO threshold, the PSE/FSE/FF pin sources a current (typically 32µA) to charge the resistor between the PSE/FSE/FF pin and AGND. The MP3359C detects the PSE/FSE/FF pin voltage to enable certain functions (see Table 1).

Table 1: PSE/FSE/FF Pin Function

PSE/FSE/FF Pin Voltage	Frequency Spread Spectrum	Delay Function
<1.13V	Disabled	Disabled
1.27V to 1.8V	Enabled	Disabled
2V to 2.55V	Disabled	Enabled
>2.85V	Enabled	Enabled

The PSE/FSE/FF pin must have a suitable voltage to match the microcontroller's (MCU's) logic level. After V_{CC} exceeds its UVLO threshold for a delay (typically 310µs), the MP3359C raises the PSE/FSE/FF pin voltage to be between 4.35V and 5.22V anytime V_{IN} exceeds 6V (see Figure 5).

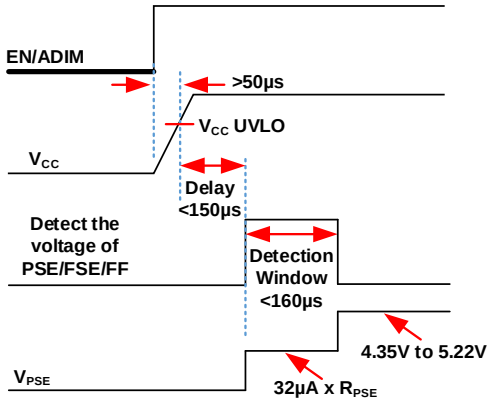


Figure 5: PSE/FSE/FF Pin Timing

Delay Time Function

To reduce inrush current and audible noise during PWM dimming, the MP3359C employs a delay time function. There is a 100µs delay time between the LED channels (see Figure 6).

When operating in delay time mode, the recommended I_{LED} pulse on time is ≥10µs.

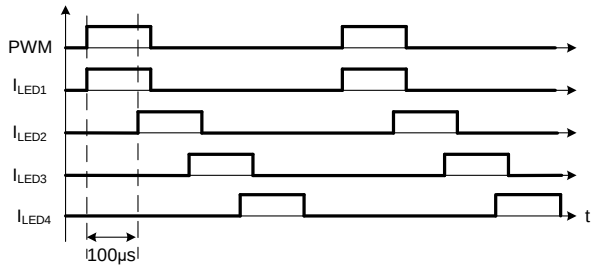


Figure 6: 100µs Delay Time with 4 Channels

Frequency Spread Spectrum (FSS)

The MP3359C uses switching frequency (f_{SW}) jitter (f_{JITTER}) to spread the f_{SW} spectrum. This reduces the spectrum spike around f_{SW} and its harmonic frequencies.

The frequency jitter range is ±10% of f_{SW}.

The modulation frequency is fixed at 6kHz.

Protections

The MP3359C provides LED open protection, LED short protection, LEDx short-to-GND protection, V_{OUT} short-to-GND protection, input over-current protection (OCP), cycle-by-cycle current limiting, and thermal protection. If any of the above protections are triggered (excluding cycle-by-cycle current limiting and thermal protection), PSE/FSE/FF is pulled to AGND. After the IC recovers from a protection, PSE/FSE/FF is pulled high again.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

LED Open Protection

LED open protection is achieved by detecting V_{OVP} and V_{LEDx}. If one string is open during normal operation, the respective V_{LEDx} drops low to PGND, and the IC keeps charging V_{OUT} until it reaches the over-voltage protection (OVP) threshold.

If OVP is triggered, the chip stops switching and marks off the fault string that has a V_{LEDx} below 100mV. The remaining LED strings force V_{OUT} back into normal regulation. The string with the largest voltage drop determines the V_{OUT} regulation value.

Every 500µs, the LEDx pin that was marked off turns on for 4µs to check whether the open fault has been removed.

If all used strings are open, the IC latches off and cannot recover until V_{IN} is reset or EN/ADIM is pulled low for >60ms and the device is turned on again.

LED Short Protection

The MP3359C monitors V_{LEDx} to check whether a short string fault has occurred. If one or more strings are shorted, the shorted LEDx pins tolerate the high voltage stress. If V_{LEDx} exceeds the short protection threshold, an internal counter starts counting.

If the fault condition lasts for 7.7ms (D_{PWM} = 100%), the fault string is marked off. Once a string is marked off, it disconnects from the V_{OUT} loop until the short fault is removed.

Every 500µs, the LEDx pin that was marked off turns on for 4µs to check whether the short fault has been removed.

If all the active LEDx pins' voltages exceed the threshold for 480ms (D_{PWM} = 100%), then all strings are marked off and the IC latches off.

If open LED condition occurs, LED short protection is disabled. This helps avoid mis-triggering LED short protection.

LEDx Short-to-GND Protection

If an LEDx pin is shorted to GND, the COMP voltage (V_{COMP}) increases and saturates. If COMP is saturated for 40ms, LEDx short-to-GND protection is triggered. PSE/FSE/FF is pulled low, and the SD pin is pulled high to turn off the external P-channel MOSFET. Then the IC latches off.

V_{OUT} Short-to-GND Protection

If V_{OUT} is shorted to PGND, V_{OUT} decreases. If V_{OVP} reaches its UVLO threshold and lasts for 10µs, V_{OUT} short-to-GND protection is triggered. SD is pulled high to turn off the external P-channel MOSFET, then V_{OUT} disconnects from V_{IN}, and the IC latches off.

Cycle-by-Cycle Current Limit

To prevent the internal or external components from exceeding the current stress rating, the IC features cycle-by-cycle current limit protection. If the current exceeds the current limit value, the IC stops switching until the next clock cycle.

Input Over-Current Protection (OCP)

To prevent the input current (I_{IN}) from exceeding the current stress rating, the INS pin detects the voltage across the input current-sense (CS) resistor (R_S) (see Figure 7). When the difference between V_{IN} and the INS voltage (V_{IN} - V_{INS}) reaches the protection threshold for 3µs, the P-channel MOSFET turns off and the MP3359C latches off.

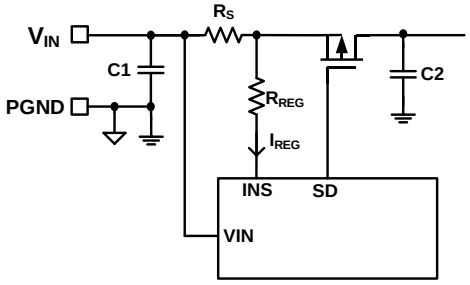


Figure 7: Typical VIN Current Detect Circuit

For flexibility when selecting R_S, the INS pin has a 20µA sink current capability. It is possible to add a resistor (R_{REG}) to make the difference between V_{IN} and V_{INS} equal to the summed voltage of (R_S + R_{REG}).

Thermal Shutdown

If the die's junction temperature (T_J) exceeds the upper threshold (T_{ST}), the IC shuts down. Once the temperature drops below the lower threshold, the IC recovers. The hysteresis is about 20°C.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the LED Current (I_{LED})

The LED current (I_{LED}) amplitude is set by an external resistor connected from ISET to GND. I_{LED} can be calculated with Equation (1):

$$I_{LED}(mA) = \frac{1200}{R_{ISET}(k\Omega)} \quad (1)$$

If R_{ISET} = 10kΩ, then I_{LED} is 120mA.

Setting the Switching Frequency (f_{SW})

f_{SW} can be configured via a resistor or an external clock.

When using an external resistor on FREQ/SYNC to configure f_{SW}, then f_{SW} can be estimated with Equation (2):

$$f_{SW}(kHz) = \frac{22000}{R_{FREQ}(k\Omega)} \quad (2)$$

If R_{FREQ} = 44.2kΩ, then f_{SW} is set to 500kHz.

There may be some deviation between the actual f_{SW} and the calculated value from Equation (2). R_{FREQ} = 50kΩ is recommended for a typical f_{SW} of 440kHz, and R_{FREQ} = 9.1kΩ is recommended for a typical f_{SW} of 2.2MHz.

To improve EMI, efficiency, and thermal performance, synchronize f_{SW} with an external clock. A ≥250kHz external clock frequency is recommended for the external SYNC SW function.

If using the external clock on the FREQ/SYNC pin, do not stop the clock during working, or the MP3359C may not operate normally.

Selecting the Input Capacitor

The input capacitor (C_{IN}) reduces the surge current drawn from the input supply and the switching noise from the device. To prevent the high-frequency switching current from passing through to the input, the C_{IN} impedance at f_{SW} should be less than the input source impedance. It is recommended to use ceramic capacitors with X5R or X7R dielectrics for their low ESR and small temperature coefficients. For most applications, a 10μF ceramic capacitor is sufficient.

Selecting the Inductor and External Current-Sense Resistor (R_{IS})

The MP3359C requires an inductor to supply a higher V_{OUT} while being driven by V_{IN}. A larger-value inductor results in less ripple current, lower peak inductor current ($I_{L(PEAK)}$), and less stress on the external N-channel MOSFET. However, a larger-value inductor also has a larger physical size, higher series resistance, and lower saturation current.

Choose an inductor that does not saturate under worst-case load conditions. Select the minimum inductance (L) to ensure that the boost converter works in continuous conduction mode (CCM) with high efficiency and good EMI performance.

Calculate the required inductance (L) with Equation (3):

$$L \geq \frac{\eta \times V_{OUT} \times D \times (1-D)^2}{2 \times f_{SW} \times I_{LOAD}} \quad (3)$$

Where V_{OUT} is the output voltage, f_{SW} is the switching frequency, I_{LOAD} is the LED load current, η is the efficiency, and D is the switching duty cycle.

D can be estimated with Equation (4):

$$D = 1 - \frac{V_{IN}}{V_{OUT}} \quad (4)$$

Where V_{IN} is the input voltage.

The switching current is used for peak current control mode. To avoid reaching the current limit, the voltage across the current-sensing resistor (R_{IS}) must be less than 70% of the current limit voltage (V_{LIM_CYC}) in the worst-case scenario. Calculate R_{IS} and $I_{L(PEAK)}$ with Equation (5) and Equation (6):

$$R_{IS} = \frac{0.7 \times V_{LIM_CYC}}{I_{L(PEAK)}} \quad (5)$$

$$I_{L(PEAK)} = \frac{V_{OUT} \times I_{LOAD}}{\eta \times V_{IN}} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times f_{SW} \times V_{OUT}} \quad (6)$$

Selecting the Power MOSFET

The MP3359C is capable of driving a wide variety of N-channel power MOSFETS. The critical MOSFET parameters are the maximum drain-to-source voltage ($V_{DS(MAX)}$), maximum current ($I_{D(MAX)}$), on resistance ($R_{DS(ON)}$), gate-

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

source charge (Q_{GS}), gate-drain charge (Q_{GD}), and total gate charge (Q_G).

Ideally, the off-state voltage across the MOSFET is equal to V_{OUT}. Considering the voltage spike when the MOSFET turns off, $V_{DS(MAX)}$ should be greater than 1.5 times V_{OUT}.

The maximum current through the power MOSFET occurs at the minimum V_{IN} and the maximum output power (P_{OUT}). The maximum RMS current ($I_{RMS(MAX)}$) through the MOSFET is calculated with Equation (7) and Equation (8):

$$I_{RMS(MAX)} = I_{IN(MAX)} \times \sqrt{D_{MAX}} \quad (7)$$

$$D_{MAX} \approx \frac{V_{OUT} - V_{IN(MIN)}}{V_{OUT}} \quad (8)$$

The MOSFET's current rating should be greater than 2 x $I_{RMS(MAX)}$.

The MOSFET's $R_{DS(ON)}$ determines the conduction loss, which is calculated with Equation (9):

$$P_{COND} = I_{RMS}{}^2 \times R_{DS(ON)} \times k \quad (9)$$

Where *k* is the MOSFET's temperature coefficient.

The switching loss is related to Q_{GD} and Q_{GS}, which determine the commutation time. Q_{GS1} is the charge between the threshold voltage and the plateau voltage when a driver charges the gate, which can be read in the V_{GS} vs. Q_G chart in the MOSFET datasheet. Q_{GD} is the charge during the plateau voltage. These two parameters are required to estimate the turn-on and turn-off losses, and can be calculated with Equation (10):

$$P_{SW} = \frac{Q_{GS1} \times R_G}{V_{DR} - V_{TH}} \times V_{DS} \times I_{IN} \times f_{SW} + \frac{Q_{GD} \times R_G}{V_{DR} - V_{PLT}} \times V_{DS} \times I_{IN} \times f_{SW} \quad (10)$$

Where V_{TH} is the threshold voltage, V_{PLT} is the plateau voltage, V_{DS} is the drain-source voltage, and R_G is the gate resistance.

Calculating the switching loss is the most difficult part of loss estimation. The formula above provides a simplified equation. For more accurate estimates, the equation becomes much more complex.

The total gate charge (Q_G) is used to calculate the gate drive loss, and can be calculated with Equation (11):

$$P_{DR} = Q_G \times V_{DR} \times f_{SW} \quad (11)$$

Where V_{DR} is the drive voltage.

Selecting the Output Capacitor

The output capacitor (C_{OUT}) keeps the V_{OUT} ripple (ΔV_{OUT}) small and ensures feedback (FB) loop stability. The C_{OUT} impedance must be low at f_{SW}. Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics. For most applications, a 10µF ceramic capacitor is sufficient.

Setting the Over-Voltage Protection (OVP)

Open-string protection is achieved by detecting the OVP pin's voltage (V_{OVP}). In some cases, an LED string failure results in the FB voltage (V_{FB}) always being 0V. If the MP3359C continues boosting V_{OUT} higher and higher and V_{OUT} reaches the configured OVP threshold, then OVP is triggered.

To ensure that the chip functions properly, an appropriate OVP threshold is required. The recommended threshold is about 1.2 times the maximum V_{OUT} for normal operation. The OVP threshold is set by a resistor divider from V_{OUT} to the OVP pin and the OVP pin to AGND. The OVP threshold (V_{OVP}) can be calculated with Equation (12):

$$V_{OVP} = 2(V) \times (1 + \frac{R_{HIGH}}{R_{LOW}}) \quad (12)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PCB Layout Guidelines

Efficient PCB layout is critical to reduce EMI noise and achieve stable operation. For the best results, refer to Figure 8 and follow the guidelines below:

1. The high-frequency switching current flows through the loop between the N-channel MOSFET (M2), output diode (D1), output capacitors (C4 and C5), PGND, and the external current-sense resistor (R_{IS}). Keep this loop as short as possible to reduce noise and EMI.
2. Internally connect the IC's exposed pad to the AGND pin, and refer all logic signals to AGND.
3. Externally connect PGND to AGND, routing PGND away from the logic signals.
4. Place the ceramic capacitors for the VIN pin and VCC pin as close to the IC as possible.

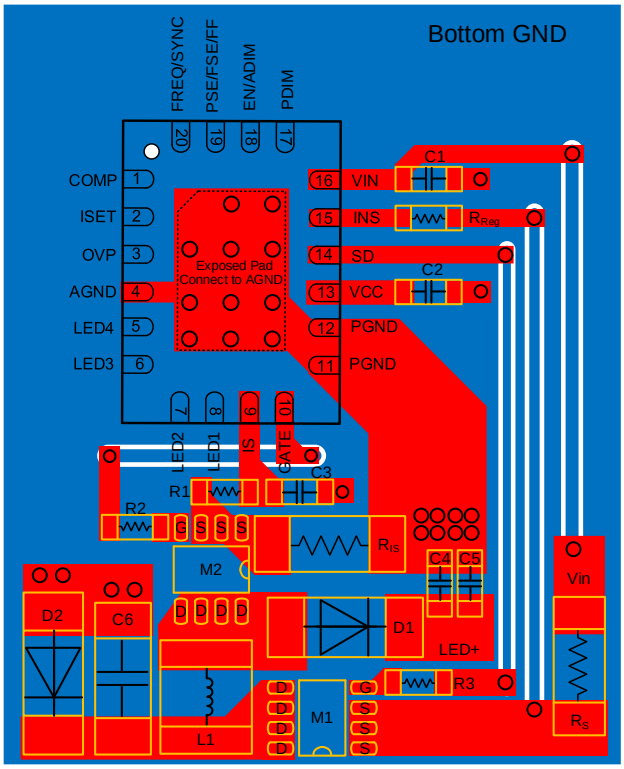


Figure 8: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

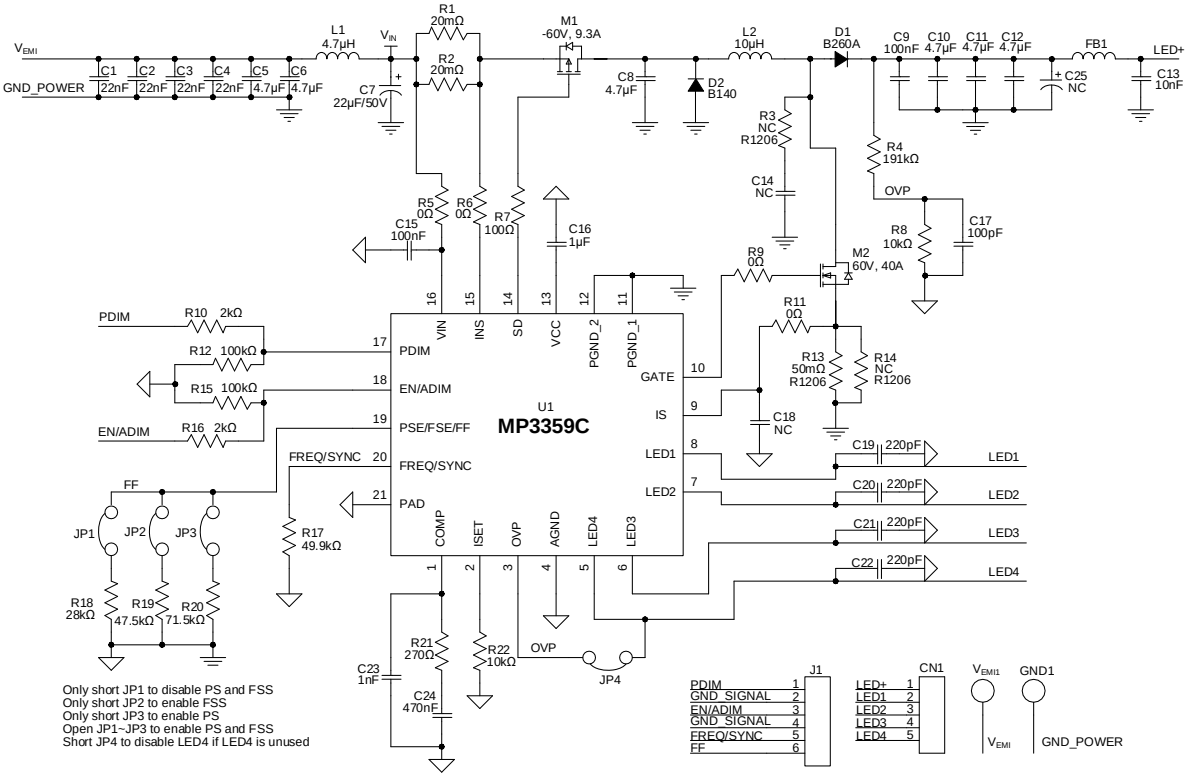


Figure 9: Typical Application Circuit (Boost)

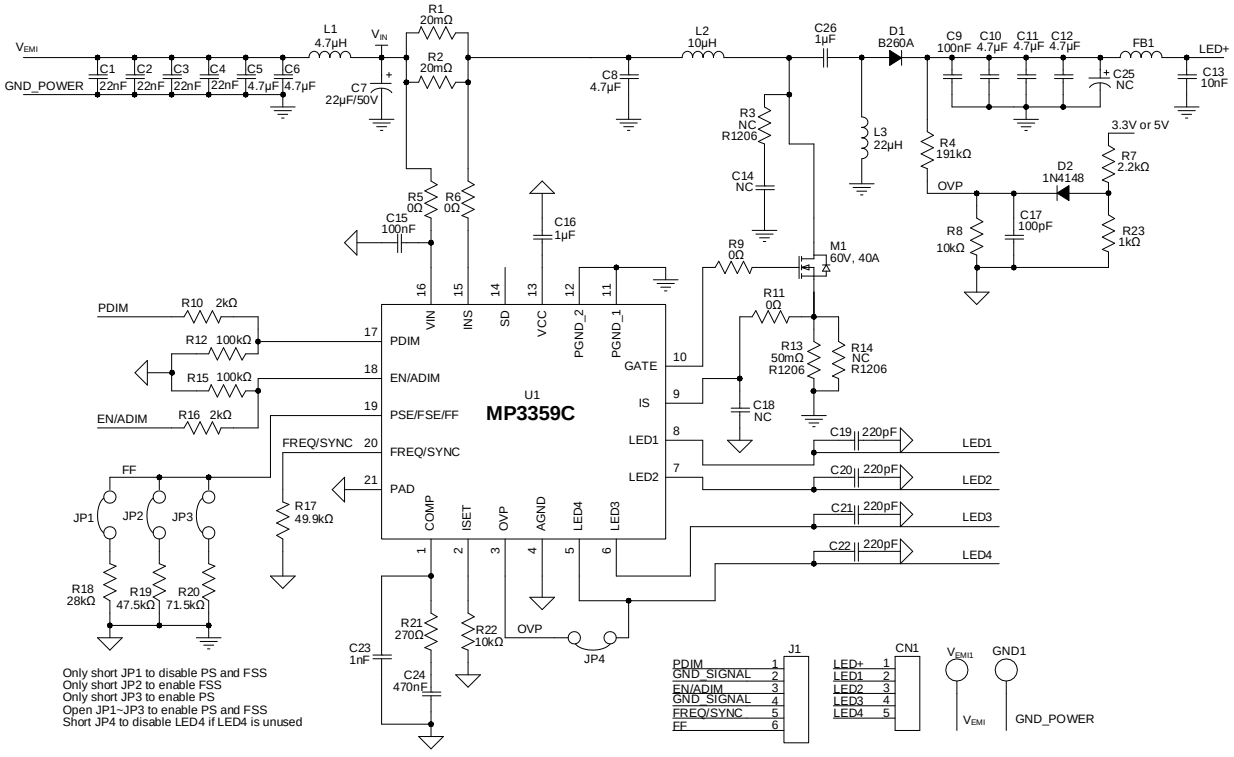
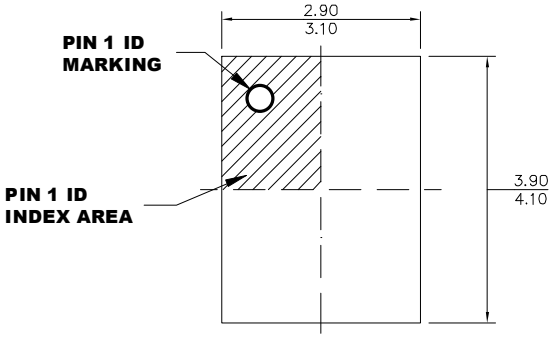


Figure 10: Typical Application Circuit (SEPIC)

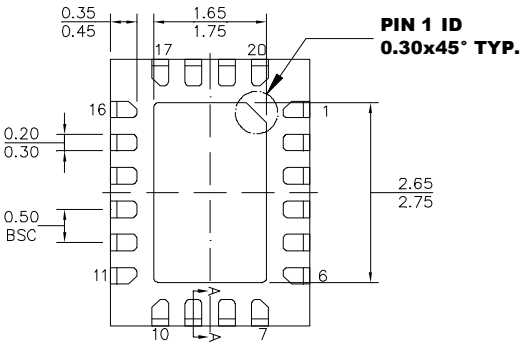
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

PACKAGE INFORMATION

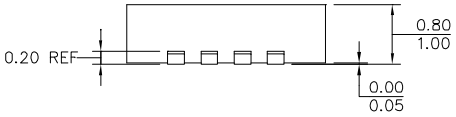
QFN-20 (3mmx4mm)
Wettable Flank



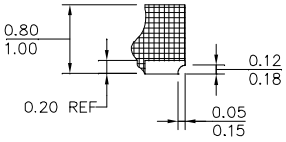
TOP VIEW



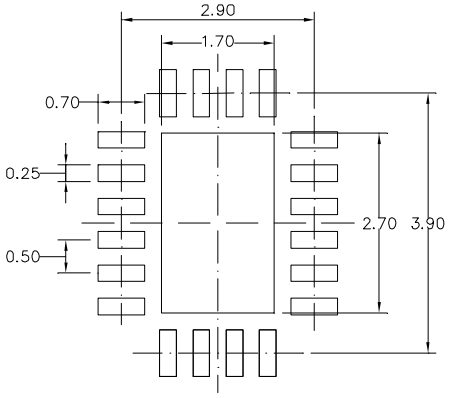
BOTTOM VIEW



SIDE VIEW



SECTION A-A



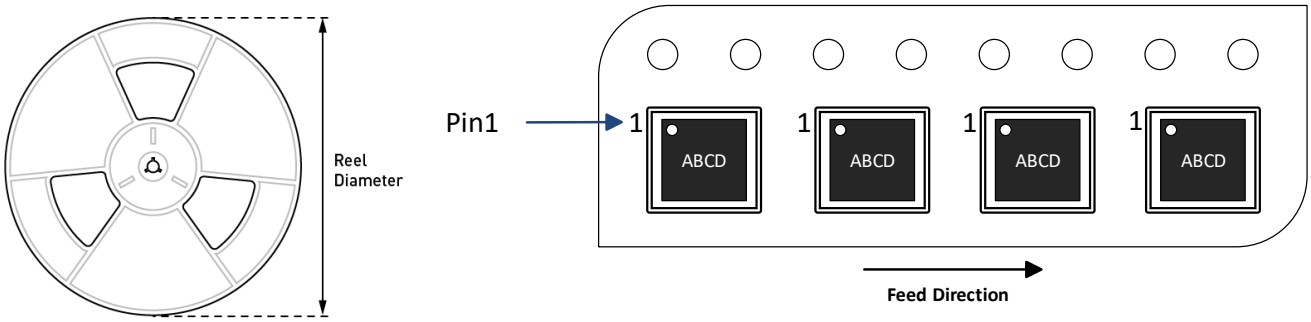
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3359CGLE-Z	QFN-20 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/23/2025	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2025 MPS. All Rights Reserved.