MP5461

Dual Input, 4-Switch Integrated Buck-Boost Converter with Input ORing and Selection

DESCRIPTION

The MP5461 is a dual input, 4-switch, integrated buck-boost converter. It is capable of regulating the output voltage from 4.2V to 5.5V VIN1 and 2.5V to 5.5V VIN2. The VIN1 can support up to 22V input voltage but is not functional after >5.75V.

The MP5461 has two auto-ORing switches from VIN1 and VIN2 to achieve a stable input for the buck-boost converter. The two sets of ORing MOSFETs are integrated. If one channel power source falls, the fast turn-off protection minimizes the reverse current.

The buck-boost converter can operate from an input voltage above, equal to, or below the output voltage. It uses current-mode control with 1.8MHz fixed PWM frequency to optimize stability and transient response. In a light-load condition, it enters PFM mode to get high light-load efficiency. Integrated MOSFETs minimize the solution size while maintaining high efficiency.

Fault protection includes VIN1 OVP shutdown, output hiccup current limiting, and thermal shutdown.

The MP5461 is available in a tiny CSP-12 (1.4mmx1.8mm) package.

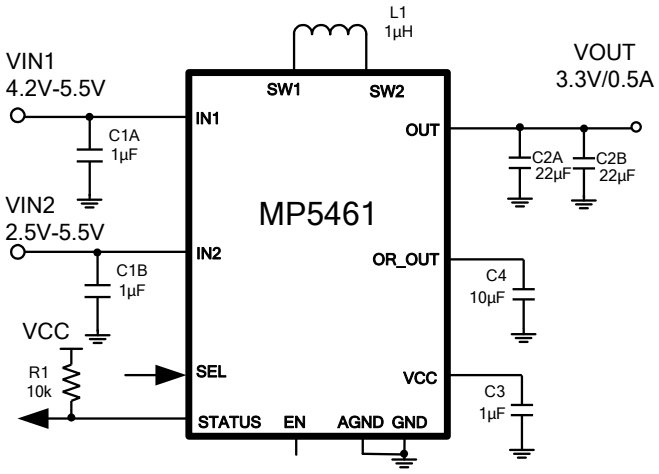
FEATURES

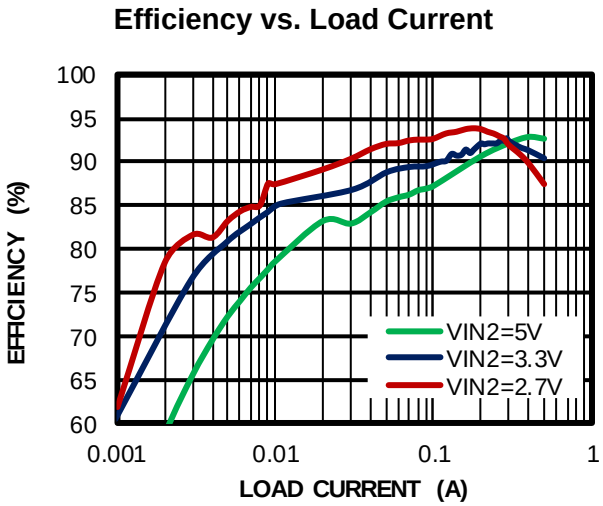
- Dual Input ORing Switches:
  - 4.2V to 5.5V Input Voltage Range for VIN1
  - Supports 22V Voltage Stress for VIN1
  - 5.75V OVP Shutdown for VIN1
  - 2.5V to 5.5V Input Voltage Range for VIN2
  - Fast Reverse Block within 2µs
  - 1A Current Capability for Each Channel
  - Soft-Start Control
  - Fast SCP (Short-Circuit Protection) on OR_OUT
  - Power-Path Selection Input
  - Power-Path Status Indication
- Buck-Boost Converter
  - 1.8MHz Switching Frequency for CCM
  - 3.3V Fixed Output Voltage
  - 500mA Continuous Output Current
  - 1ms Soft-Start Time
  - Auto PFM/PWM Mode
  - Output Over-Voltage Protection
  - Hiccup Over-Current Protection
- 1µA Shutdown Current
- 200µA Quiescent Current
- Active Low System EN Pin
- EN to OR_OUT Start-Up Delay 300µs
- Over-Temperature Shutdown
- Available in a Wafer Level Chip Scale Packaging: CSP-12(1.4mmx1.8mm)

APPLICATIONS

- USB-C Cable
- V_{CONN} Powered USB Device

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5461GC	CSP-12 (1.4mmx1.8mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5461GC–Z).

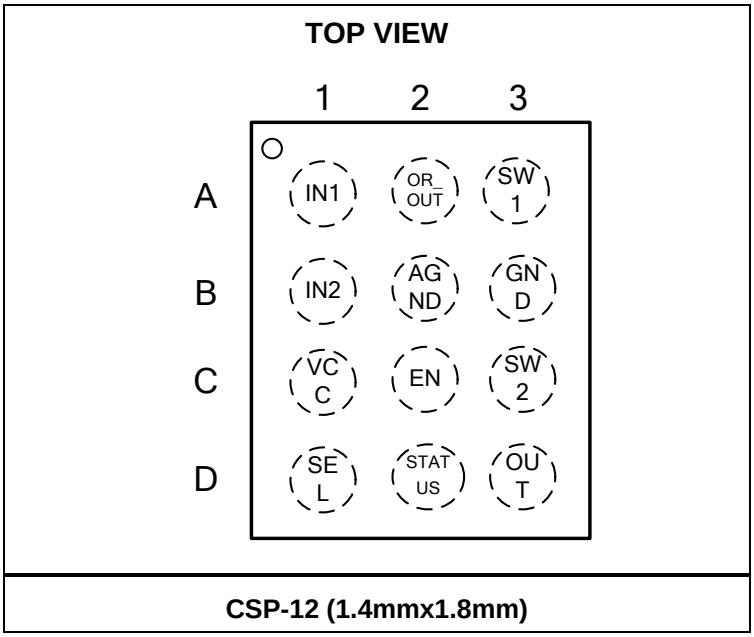
TOP MARKING

JGY

LLL

JG: Product code of MP5461GC
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



CSP-12 (1.4mmx1.8mm)

PIN FUNCTIONS

CSP-12 Pin #	Name	Description
A1	IN1	**VIN1 supply voltage.** The MP5461 operates from a 4.2V to 5.5V VIN1 voltage and supports a 22V input voltage, but it is not functional >5.75V. CIN1 prevents large voltage spikes at the input. Place CIN1 as close to the IC as possible.
A2	OR_OUT	**IN1, IN2 ORing output.** Also functions as the buck-boost input pin. Use a 10µF or larger capacitor for decoupling.
A3	SW1	**Switch1.** The first half-bridge switch node is connected to SW1. Connect an inductor between SW1 and SW2.
B1	IN2	**VIN2 supply voltage.** The MP5461 operates from a 2.5V to 5.5V VIN2 voltage. CIN2 prevents large voltage spikes at the input. Place CIN2 as close to the IC as possible.
B2	AGND	**Analog ground.** Connect AGND to VCC capacitor's GND node by a Kelvin sense trace.
B3	GND	**Power ground.** Reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect to GND with copper traces and vias.
C1	VCC	**Internal 5V LDO regulator output.** Decouple with a 1µF capacitor.
C2	EN	**On/off control for entire chip.** EN is active low. Drive EN high to turn off the chip. Drive EN low or float to turn on the device. It has an internal 600kΩ pull-down resistor to ground.
C3	SW2	**Switch2.** The internal second half-bridge switch node is connected to SW2. Connect an inductor between SW1 and SW2.
D1	SEL	**Power path select input.** If SEL=Low or is floated, VIN1 is selected; If SEL=High, VIN2 is selected. The MP5461 will auto select the available power path if only one supply is available. It has an internal 600kΩ pull-down resistor to ground.
D2	STATUS	**Status indication.** Open drain output. Indicates if the VIN1 or VIN2 channel is selected. Refer to the truth table.
D3	OUT	**Output pin.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN1}) .....-0.3V to +24V
V_{SW1}.....
–0.3V (-5V for <10ns) to V_{OR_OUT} + 0.3V(10V for <10ns)
V_{SW2}.....
–0.3V (-5V for <10ns) to V_{OUT} + 0.3V (10V for <10ns)
V_{EN}, V_{SEL},V_{STATUS} .....–0.3V to +5.5V
All Other Pins.....–0.3V to +6V
Continuous Power Dissipation (TA = +25°C) (2)
CSP-12 (1.4mmx1.8mm) 1.14W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Operation Input Voltage VIN1.....4.2V to 5.5V
Operation Input Voltage VIN2.....2.5V to 5.5V
Output Current 500mA
Operating Junction Temp. (TJ). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

CSP-12 (1.4mmx1.8mm)..... 110 ..... 12... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB. The value of θJA given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = 5V, V_{IN2}=5V, V_{EN} = 0V, T_J = -40°C to +125°C(5), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (Shutdown)	I_{IN1}	V_{EN}=5V, VIN1=5V, VIN2=float, T_J = +25°C		1	5	μA
	I_{IN2}	V_{EN}=5V, VIN1=float, VIN2=5V, T_J = +25°C		1	5	μA
Supply current (Quiescent)	I_{Q1}	V_{EN}=0V, VIN1=5V, VIN2=float, No switching, T_J = -40°C to +85°C		210	260	μA
	I_{Q2}	V_{EN}=0V, VIN1=float, VIN2=5V, No switching, T_J = -40°C to +85°C		185	230	μA
EN logic high input	V_{EN_H}	Disable Part	1.2			V
EN logic low input	V_{EN_L}	Enable Part			0.4	V
EN to ground resistance	R_{EN}			600		kΩ
Thermal shutdown(6)	T_{STD}			150		°C
Thermal hysteresis(6)	T_{HYS}			20		°C
VCC regulator	V_{CC}	VIN1=5.5V	4.5	5	5.5	V
VCC load regulation	V_{CC_RG}	I_{CC}=0-5mA		3	5	%
Dual Input ORing Switches						
V_{IN1} under-voltage lockout threshold rising	$IN1UV_{Vth}$		3.6	3.9	4.15	V
V_{IN1} under-voltage lockout threshold hysteresis	$IN1UV_{HYS}$			400		mV
V_{IN2} under-voltage lockout threshold rising	$IN2UV_{Vth}$		2.05	2.25	2.45	V
V_{IN2} under-voltage lockout threshold hysteresis	$IN2UV_{HYS}$			150		mV
EN to OR_OUT startup delay	t_{EN_DLY1}	EN=0 to OR_OUT>90%, IN1=5V, IN2=0		300		μs
	t_{EN_DLY2}	IN2=5V, IN1=0		300		μs
Input over-voltage rising	V_{OVP_R}	IN1 only	5.51	5.75	6.1	V
OVP recovery threshold	V_{OVP_F}	IN1 only		5.5		V
Switch1 on resistance	R_{DSON1}	VCC=5V		160		mΩ
Switch2 on resistance	R_{DSON2}	VCC=5V		90		mΩ
IN1 to OR_OUT regulation voltage	V_{REG1}	Io=1mA, Io=100mA	5	40	100	mV
IN2 to OR_OUT regulation voltage	V_{REG2}	Io=1mA, Io=100mA	5	40	100	mV
Reverse voltage turn-off response time(7)	t_{RV}			2		μs
SEL logic high input	V_{SEL_H}	VIN2 is selected	1.2			V
SEL logic low input	V_{SEL_L}	VIN1 is selected			0.4	V
SEL to ground resistance	R_{SEL}			600		kΩ
STATUS pin leakage	I_{STA_LKG}	Pull-up with 5V			1	μA
STATUS low voltage	V_{STA_Low}	Sink 1mA			50	mV

ELECTRICAL CHARACTERISTICS

V_{IN1} = 5V, V_{IN2}=5V, V_{EN} = 0V, T_J = -40°C to +125°C(5), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATUS delay	T_{STA_DEG}	Rising edge		25		µs
		Falling edge		55		
Buck-Boost						
Output voltage	V_{OUT}		-1.5%	3.3	+1.5%	V
Output over-voltage protection	$V_{OUT\_OVP\_R}$		110%	115%	120%	V_{OUT}
Output OVP recovery	$V_{OUT\_OVP\_F}$			105%		V_{OUT}
OVP discharge resistance	R_{DIS}			1		kΩ
Oscillator frequency	Fs		1.45	1.8	2.15	MHz
Steady state current limit	I_{LIM}	VOUT=0V	1.65	2.5	3.35	A
SWD valley current limit(7)				-1.5		A
PMOS on resistance	$R_{DS(on)-P}$	SWA, SWD, 3.3Vin, 3.3Vout		90		mΩ
NMOS on resistance	$R_{DS(on)-N}$	SWB, SWC, 3.3Vin, 3.3Vout		80		mΩ
Soft-start time	Tss	0-100%Vout		1		ms

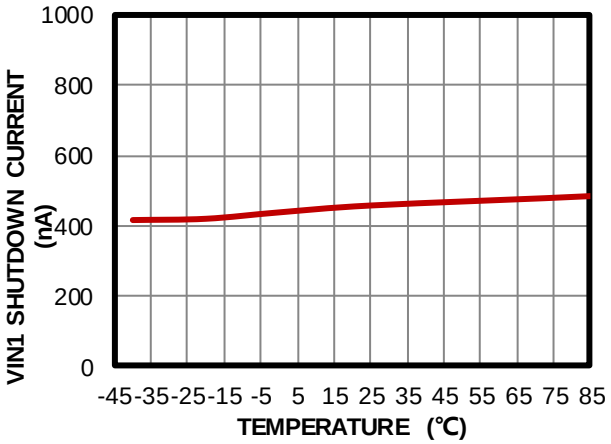
NOTE:

5) All min/max parameters are tested at T_J=25°C. Limits over temperature are guaranteed by design, characterization and correlation.
6) Guaranteed by design.
7) Guaranteed by engineering sample characterization.

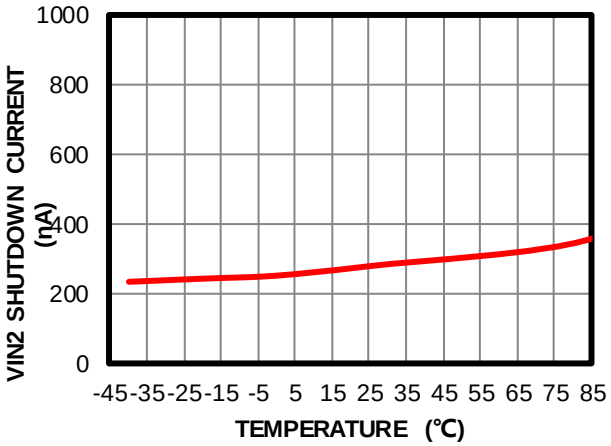
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 5V, V_{IN2} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

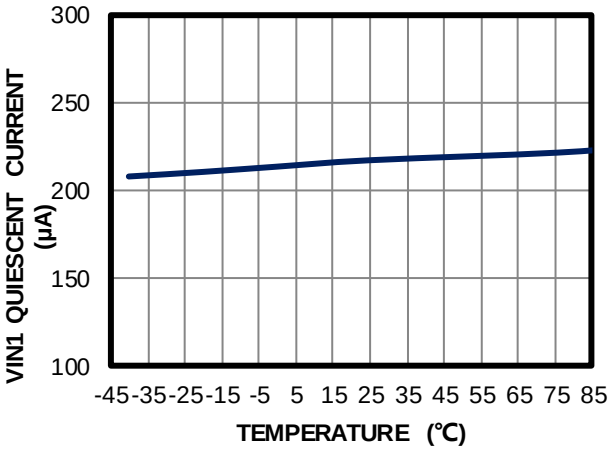
VIN1 Shutdown Current vs. Temperature, V_{IN1} = 5V



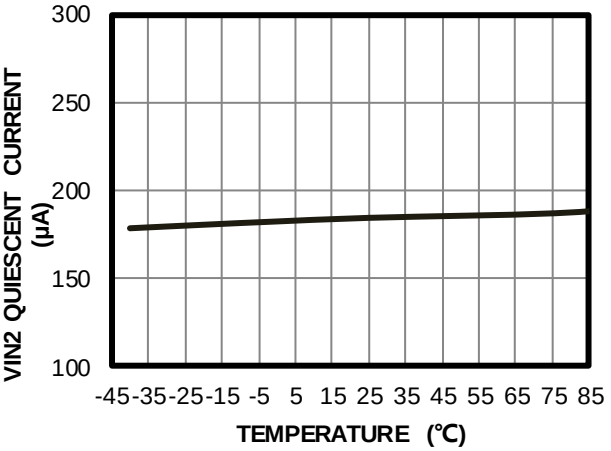
VIN2 Shutdown Current vs. Temperature, V_{IN2} = 5V



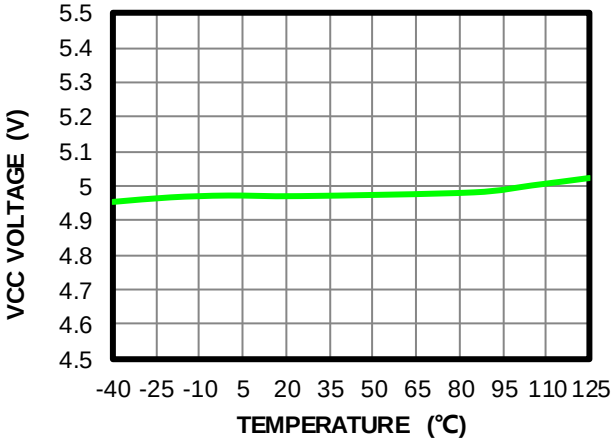
VIN1 Quiescent Current vs. Temperature, V_{IN1} = 5V



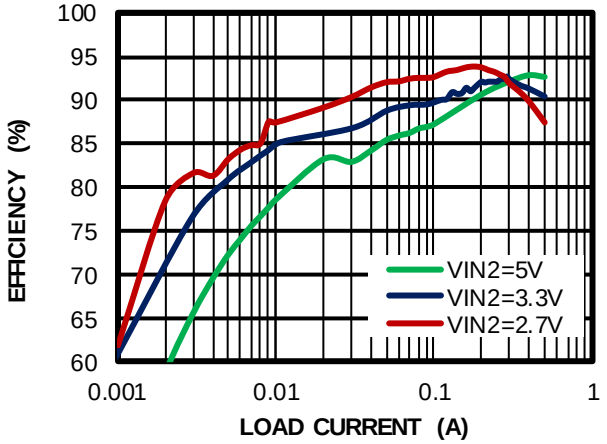
VIN2 Quiescent Current vs. Temperature, V_{IN2} = 5V



VCC Voltage vs. Temperature



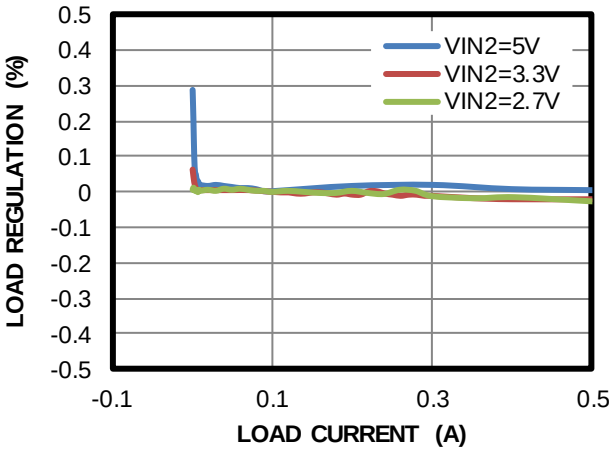
Efficiency vs. Load Current



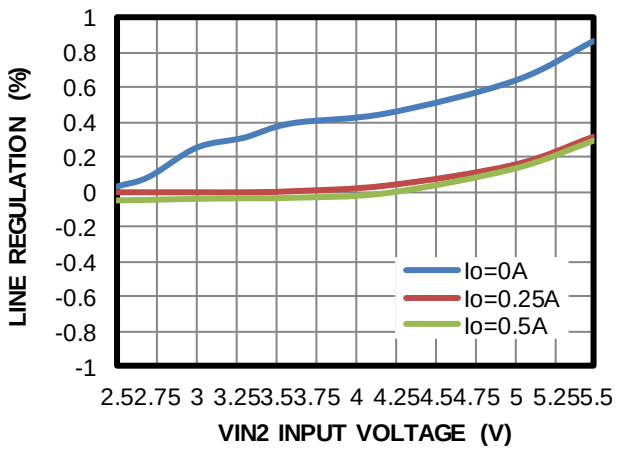
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 5V, V_{IN2} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

Load Regulation



Line Regulation

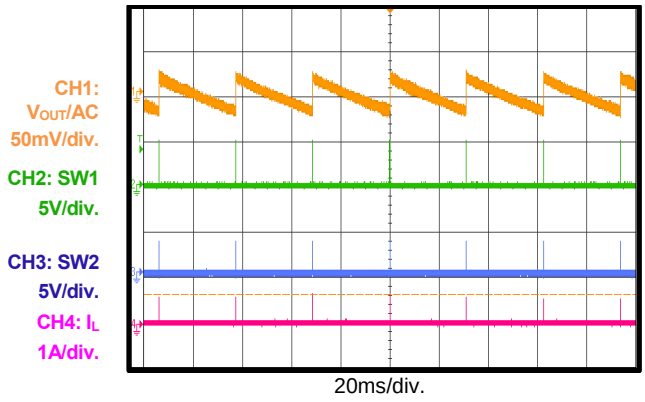


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 5V, V_{IN2} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

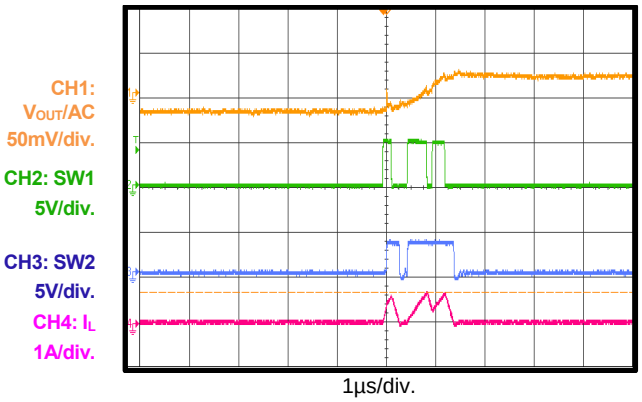
Output Ripple

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0A



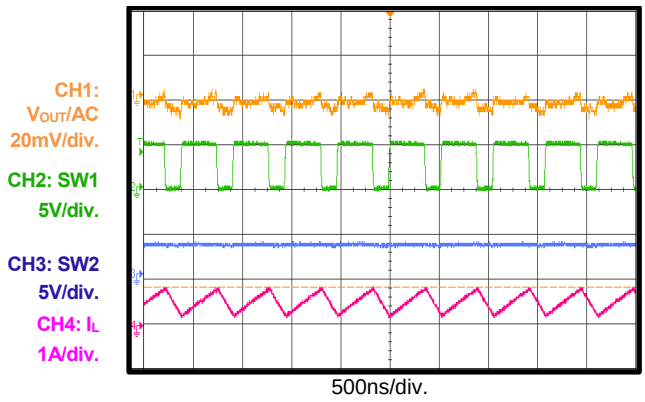
Output Ripple

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0A



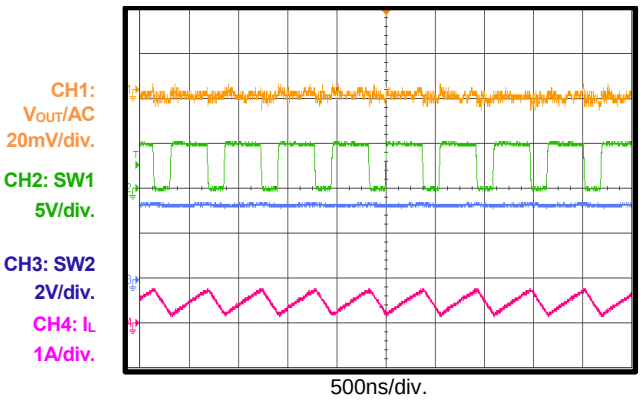
Output Ripple

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A



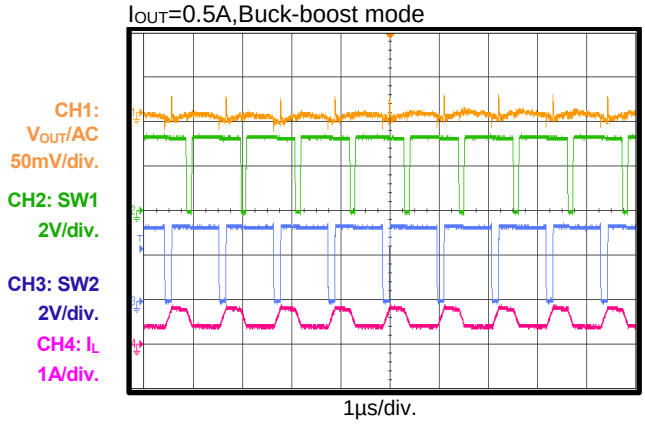
Output Ripple

V_{IN2}=5V, V_{IN1}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A



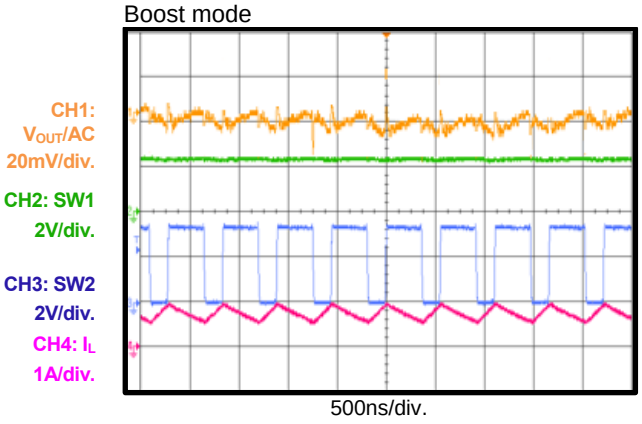
Output Ripple

V_{IN2}=3.3V, V_{IN1}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A,Buck-boost mode



Output Ripple

V_{IN2}=2.5V, V_{IN1}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A, Boost mode

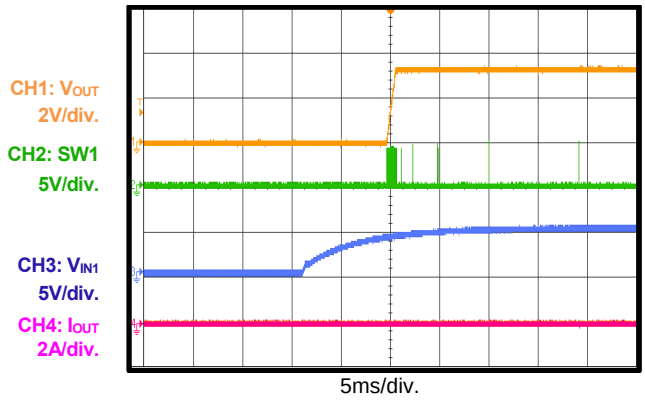


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 5V, V_{IN2} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

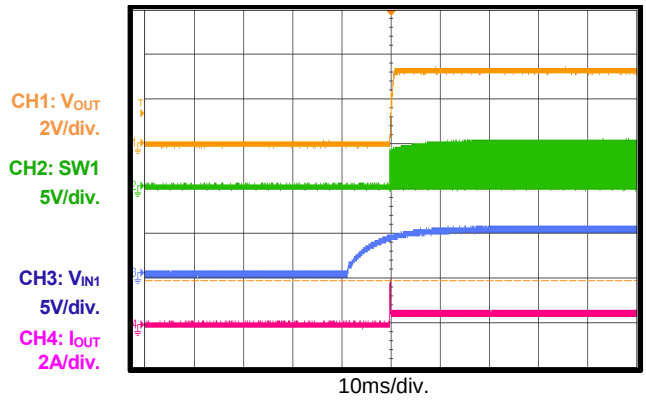
Power Start-Up

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0A



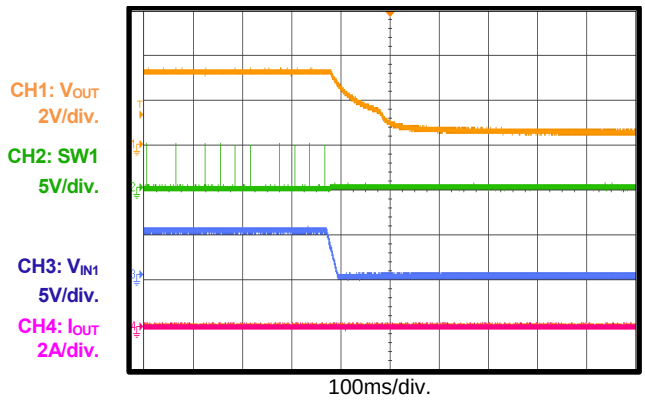
Power Start-Up

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A



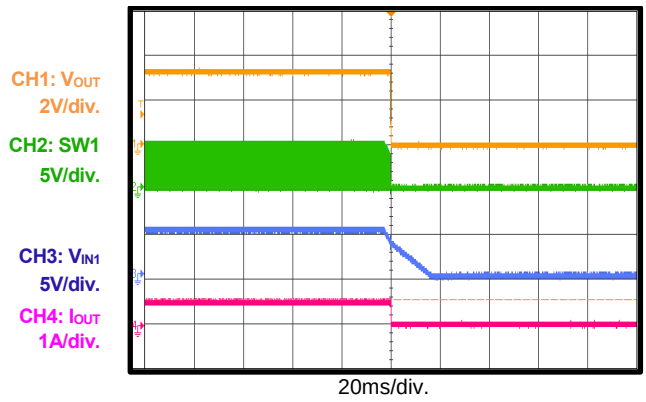
Power Shutdown

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0A



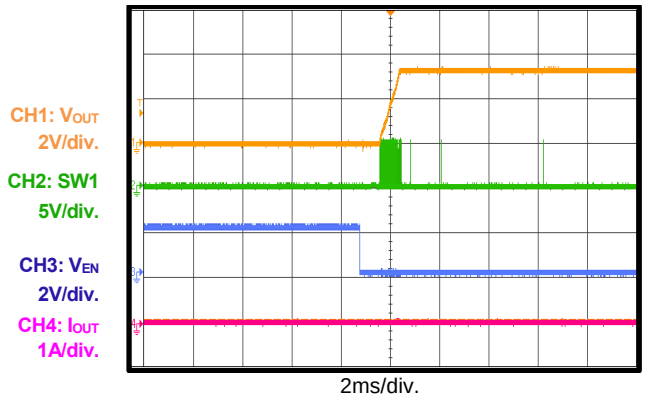
Power Shutdown

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A



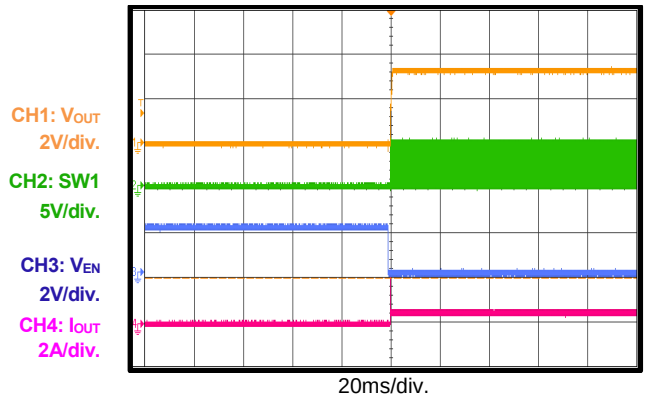
EN Start-Up

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0A



EN Start-Up

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A

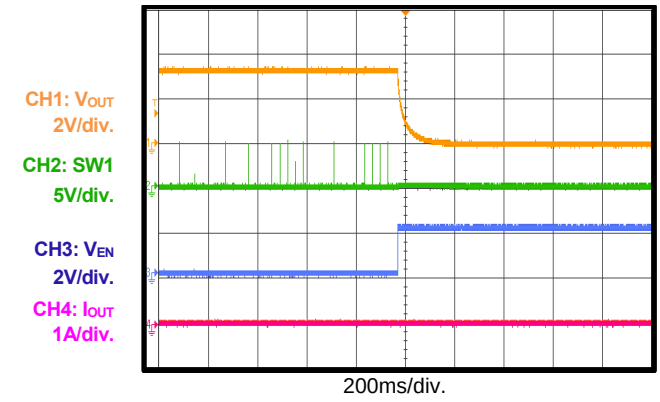


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 5V, V_{IN2} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

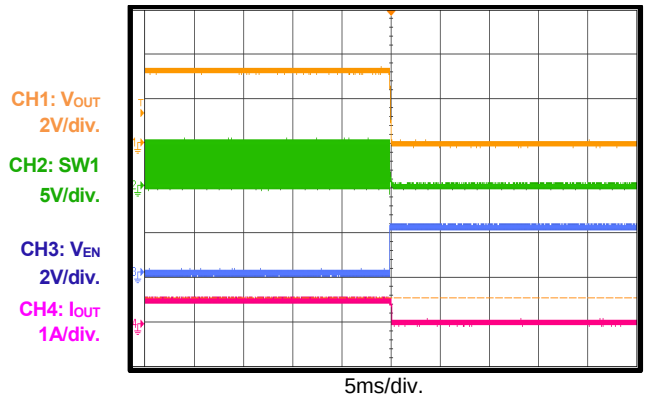
EN Shutdown

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0A



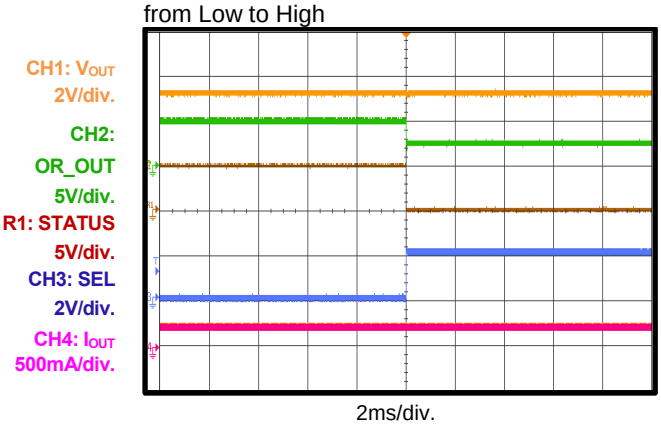
EN Shutdown

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0.5A



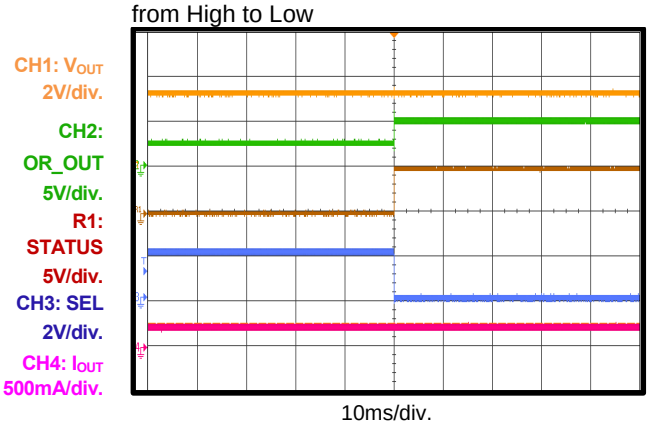
Input Voltage Selection by SEL Pin

V_{IN1}=5V, V_{IN2}=2.5V,V_{OUT}=3.3V, I_{OUT}=0.2A, SEL from Low to High



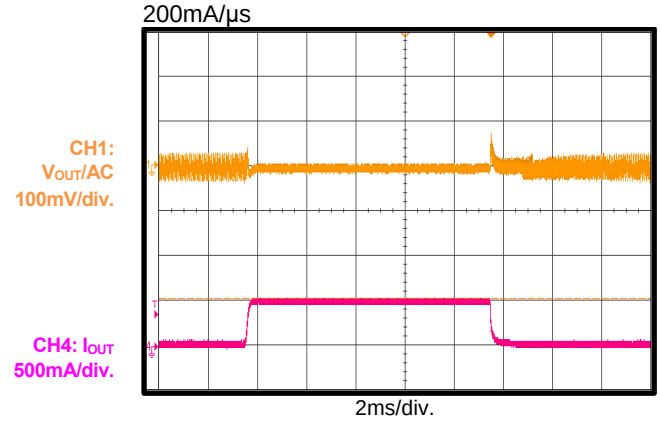
Input Voltage Selection by SEL Pin

V_{IN1}=5V, V_{IN2}=2.5V,V_{OUT}=3.3V, I_{OUT}=0.2A, SEL from High to Low



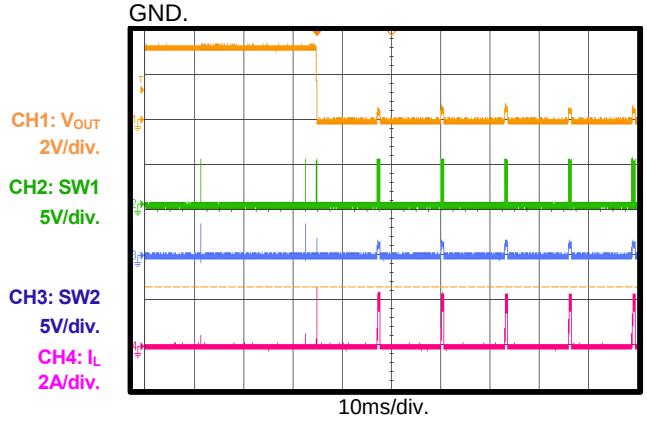
Load Transient

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, I_{OUT}=0A-0.5A, 200mA/µs



SCP Entry

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, short output to GND.

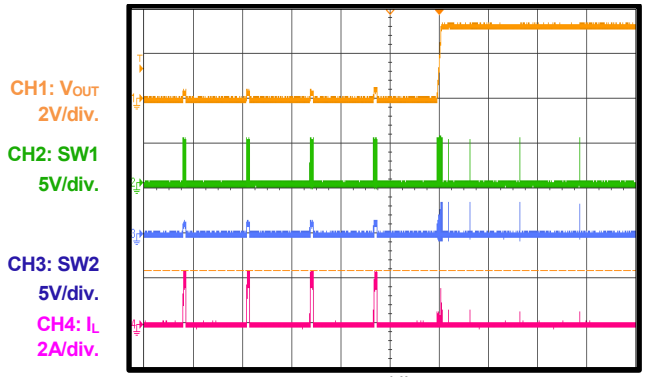


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 5V, V_{IN2} = 5V, V_{OUT} = 3.3V, L =1µH, T_A = 25°C, unless otherwise noted.

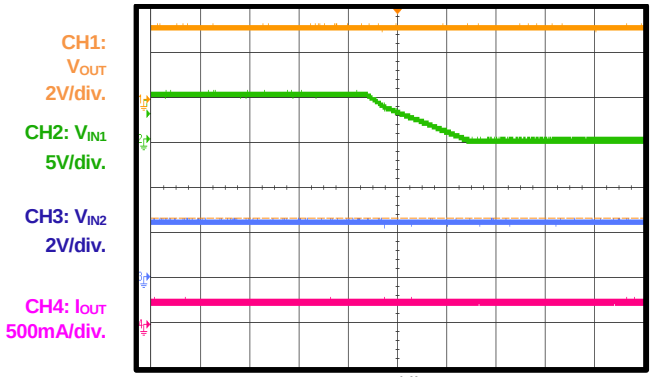
SCP Recovery

V_{IN1}=5V, V_{IN2}=Float, V_{OUT}=3.3V, short output to GND



Line Transient

V_{IN1}=5V, V_{IN2}=2.5V, I_{OUT}=0.25A, input voltage from VIN1 to VIN2



BLOCK DIAGRAM

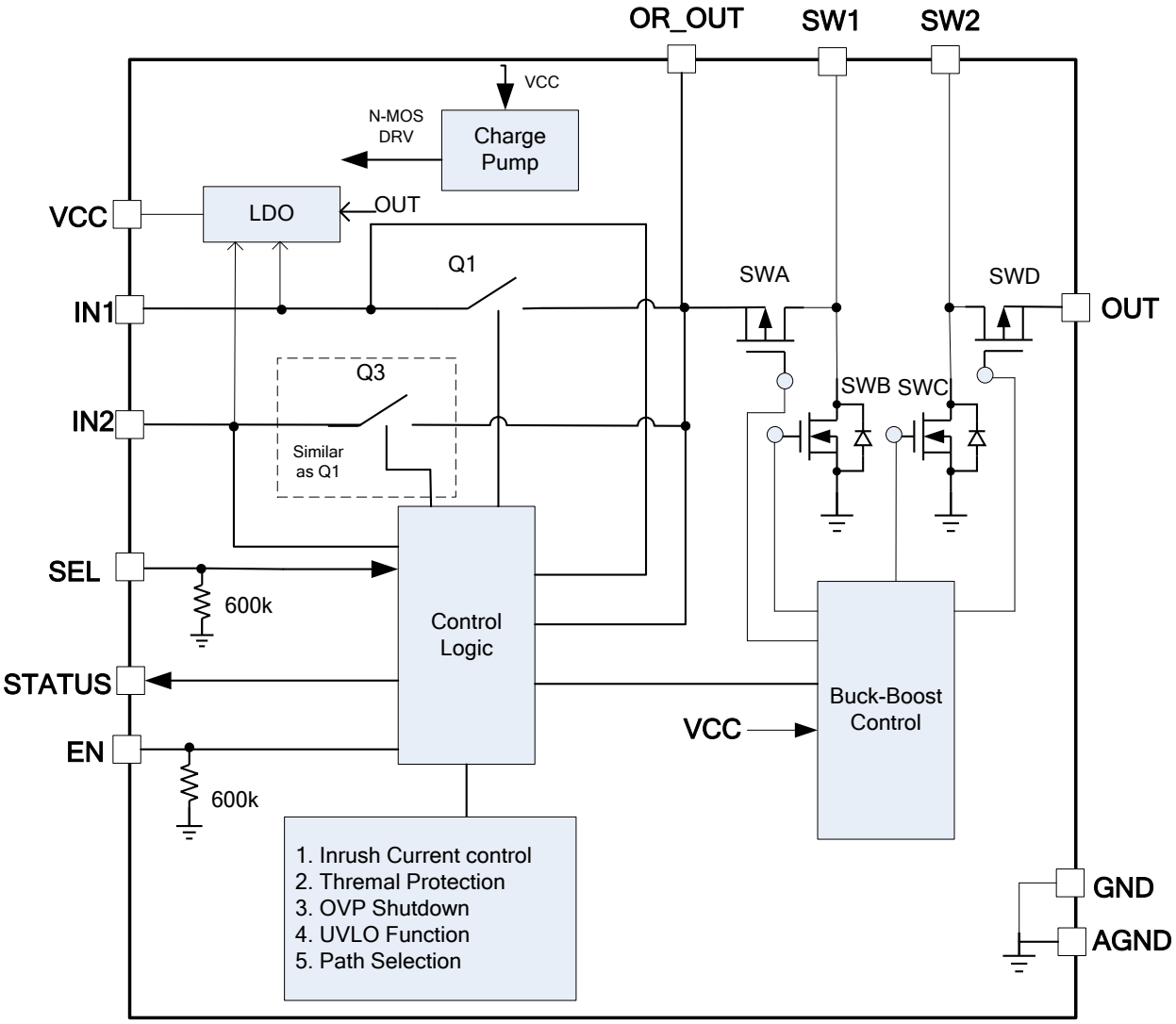
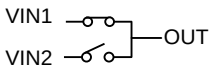
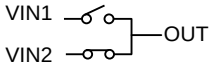
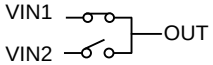
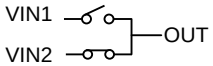
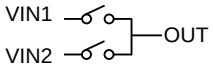


Figure 1. Functional Block Diagram

Table 1: Truth Table of SEL and STATUS Logic

VIN1	VIN2	SEL Input (SEL="low or float" selects VIN1 SEL="high" selects VIN2)	Power path	ORing Output	STATUS (Open drain output. Open drain: VIN1 is selected; or VIN1/2 N/A Low: VIN2 is selected)
4.2V-5.5V	2.5V-5.5V	"0", Select VIN1		OUT=VIN1	Open drain
		"1", Select VIN2		OUT=VIN2	0
4.2V-5.5V	Not available or <2.5V	"0", Select VIN1		OUT=VIN1	Open drain
		"1", Select VIN2			Open drain
Not available or <4.2V or >5.75V	2.5V-5.5V	"0", Select VIN1		OUT=VIN2	0
		"1", Select VIN2			0
>5.75V or Not available or <4.2V	Not available or <2.5V	"0", Select VIN1		OUT=0	Open drain
		"1", Select VIN2			

OPERATION

The MP5461 is a dual input, high-efficiency, buck-boost converter that provides regulated output voltage above, equal to, or below the input voltage.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is used to protect the device from operating at an insufficient supply voltage. The MP5461 UVLO circuit monitors the IN1 and IN2 voltage. During start-up, either IN1 or IN2 must rise higher than $V_{IN-UVLO}$ to enable the IC.

EN

EN is the system on/off control input. It's an active low input. EN has an internal weak pull-down resistor. Pull EN low or float to enable the MP5461. Pull EN high to disable the MP5461.

VCC Power Supply

When EN is active, IN1 and IN2 charges the VCC. IN1 is a high voltage pin; there is a LDO from IN1 to VCC. An ORing block will determine using the IN1 LDO output or IN2 to supply VCC. All internal circuits of the MP5461 are supplied by VCC. VCC only needs to be decoupled with a ceramic capacitor less than 1µF. After the system starts up, VCC is powered by the higher value of IN1, IN2, or VOUT internally.

Dual Input - IN1 and IN2

IN1 is a high voltage input pin, which can support up to 22V voltage, but the part will be in input over-voltage shutdown mode when IN1>5.75V.

IN2 is a low voltage input pin, which supports 5.5V maximum operation voltage.

OR_OUT is the output of the IN1 and IN2 ORing. The two sets of ORing MOSFETs (IN1 to OR_OUT, IN2 to OR_OUT) are integrated. The MP5461 employs soft-start control for both IN1 or IN2 to OR_OUT start-up.

If the power source for one channel drops, the fast turn-off protection minimizes the reverse current.

SEL is the power path selection input. Applying low voltage or floating SEL can select the IN1 to OR_OUT power path. Applying a high voltage on SEL can select the IN2 to OR_OUT power path.

If only one power input is available, the MP5461 will auto use that power input to supply OR_OUT. For additional details on the SEL input state, refer to Table 1.

Power Path Indication – STATUS

STATUS is an open drain output. It indicates if the VIN1 or VIN2 channel is selected. When VIN1 is selected, or there is no power supply at VIN1 and VIN2, STATUS is an open drain output; when VIN2 is selected, STATUS is pulled low. Refer to the truth table.

Buck - Boost Operation

The output voltage is sensed via an internal resistor divider from the output to ground. The voltage difference between the VOUT feedback voltage and the internal reference is amplified by the error amplifier to generate a control signal (V_{C-Buck}). By comparing V_{C-Buck} with the internal current ramp signal (the sensed SWA's current with slope compensation) through the buck comparator, a pulse-width modulation (PWM) control signal for the buck leg (SWA, SWB) is generated.

Another control signal ($V_{C-Boost}$) is derived from V_{C-Buck} through the level shift. Similarly, $V_{C-Boost}$ is compared with the same ramp signal through the boost comparator and generates a PWM control signal for the boost leg (SWC, SWD). The switch topology for the buck-boost converter is shown in Figure 2.

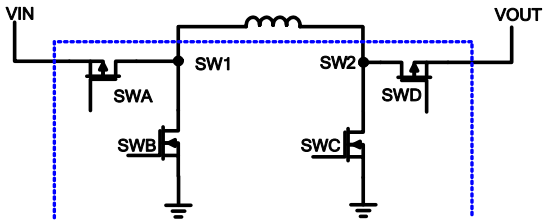


Figure 2: Buck-Boost Switch Topology

Buck Region (VIN > VOUT)

When the input voltage is significantly higher than the output voltage, the converter can deliver energy to the load within SWA's maximum duty cycle by switching SWA and SWB. The converter operates in buck mode. In this condition, SWD remains on and SWC remains off. V_{C-Buck} compares the current ramp signal and generates a PWM output. Therefore, SWA/SWB is pulse-width modulated to produce the required duty cycle and eventually supports the output voltage.

Buck-Boost Region (VIN ≈ VOUT)

When VIN is close to VOUT, the converter is unable to provide enough energy to the load due to SWA's maximum duty cycle, so the current ramp signal cannot trigger V_{C-Buck} in the first cycle, and SWA remains on with a 100% duty cycle. If SWB is not turned on in the first cycle, boost begins working in the second cycle (SWC switches in the second cycle), and an offset voltage is added to the current ramp signal to allow it to reach V_{C-Buck}. SWC turns off when the current ramp signal intersects with $V_{C-Boost}$ in the second cycle, and SWD conducts the inductor current when SWC is off. This is called boost operation.

SWA turns off when the current ramp signal intersects with V_{C-Buck} in the second cycle, and SWB turns on to conduct the inductor current after SWA turns off. This is called buck operation.

If SWB turns on in the second cycle, the boost operation (SWC on) is disabled in the following cycle. If SWA continues to conduct with 100% duty in the second cycle, boost operation is also enabled in the following duty cycle. SWA/SWB and SWC/SWD switch during this condition simultaneously. This is called buck-boost mode.

Boost Region (VIN < VOUT)

When the input voltage is significantly lower than the output voltage, the control voltage (V_{C-Buck}) is always higher than the current ramp signal. The offset voltage is added to the current signal, so SWB cannot turn on in all cycles. The boost operation (SWC on) is enabled in every cycle based on the logic, so only SWC and SWD switch. This is called boost mode. In this condition, SWC/SWD is pulse-width modulated to produce the required duty cycle and eventually support the output regulation voltage.

Internal Soft Start (SS)

When EN is active and OR_OUT is above the UVLO rising threshold, the MP5461 buck-boost starts up with a soft-start function. The internal soft-start (SS) signal ramps up and controls the feedback reference voltage.

OCP/SCP

The MP5461 employs peak current limits through switch A current sensing. The current limit is 2.5A (typical).

In an overload or short-circuit condition, VOUT drops due to the steady-state switching current limit. If VOUT drops below 60% of its normal output, the MP5461 stops switching and recovers after ~12ms with hiccup mode protection. After the switching stops in hiccup protection, the internal soft-start signal is clamped to V_{FB} + 0.3V, where V_{FB} is the divided voltage from the residual VOUT. This is used to make the soft start-up smooth when the MP5461 recovers from hiccup protection.

During the soft-start time, the MP5461 blanks during hiccup protection. After the soft-start time is finished, if VOUT is still lower than 60% of the normal voltage, the MP5461 resumes hiccup mode. If VOUT rises above 60% of the normal value, the MP5461 enters normal operation.

OVP

The MP5461 employs output over-voltage protection. A fast comparator will sense the output voltage condition. Once it's triggered, the MP5461 will stop switching, and a 1k internal resistor will be switched on to discharge the output.

APPLICATION INFORMATION

Component Selection

Selecting the Inductor

As a buck-boost topology circuit, the inductor must support buck application with the maximum input voltage and boost application with the minimum input voltage. Two critical inductance values can be calculated according to the buck and boost mode current ripple using equation (1) and equation (2).

$$L_{MIN-BUCK} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times F_{REQ} \times \Delta I_L} \quad (1)$$

$$L_{MIN-BOOST} = \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{V_{OUT} \times F_{REQ} \times \Delta I_L} \quad (2)$$

Where:

F_{REQ} is the switching frequency

ΔI_L is the peak-to-peak inductor current ripple. As a rule of thumb, the peak-to-peak ripple can be set at 0.2A to 1A to achieve better balance of the BOM cost, output ripple, and efficiency. The minimum inductor value for application should be the highest value between the results from equation (1) and equation (2).

In addition to the inductance value, the inductor must support peak current based on equation (3) and equation (4) to avoid saturation.

$$I_{PEAK-BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{2 \times V_{IN(MAX)} \times F_{REQ} \times L} \quad (3)$$

$$I_{PEAK-BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN(MIN)}} + \frac{V_{IN(MIN)} \times (V_{OUT} - V_{IN(MIN)})}{2 \times V_{OUT} \times F_{REQ} \times L} \quad (4)$$

Where η is the estimated efficiency of the MP5461.

Choose a proper inductor to make sure the inductor current won't trigger a peak current limit and valley current limit.

Input and Output Capacitor Selection

It is recommended to use ceramic capacitors with low ESR as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation.

Minimum values of 1μF for input 1, and 1μF for input 2 as well as 2x22μF for output capacitors are needed to achieve optimal performance.

The input and output capacitors must be placed as close to the device as possible.

PC Board Layout (8)

Efficient PCB layout is critical for standard operation and thermal dissipation. Refer to Figure 3 and the PCB layout guidelines below to ensure an effective layout design:

1) Place the OR_OUT capacitor and VOUT capacitor as close as possible to the OR_OUT and OUT pin as possible.

2) Use a large ground plane directly connected to GND. Add lots of GND vias to connect Cout's GND node and OR_OUT capacitor's GND.

3) Connect AGND to VCC capacitor's GND node by a Kelvin sense trace.

4) Place the VCC decoupling capacitor as close as possible to VCC.

Notes:

(8) The recommended layout is based on the typical application circuit on the next page (see Figure 4).

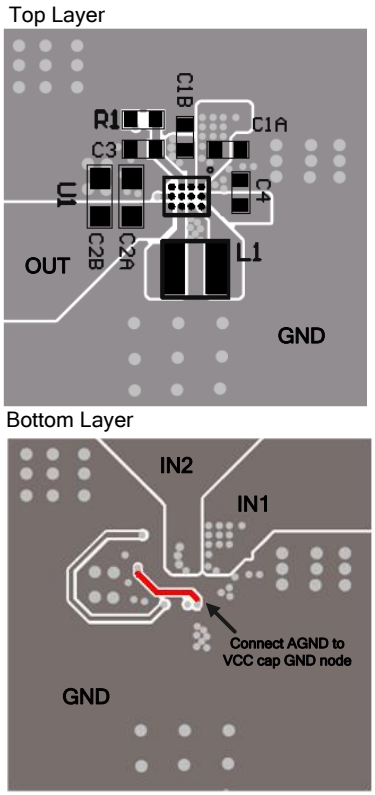


Figure 3: PC Board Layout

TYPICAL APPLICATION CIRCUITS

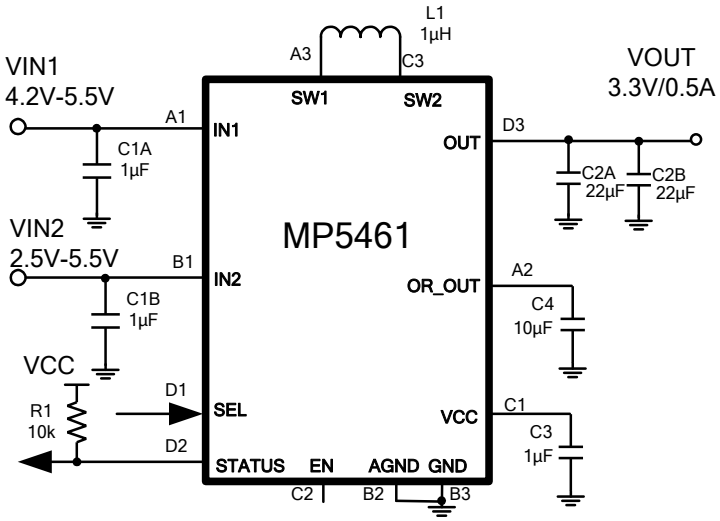
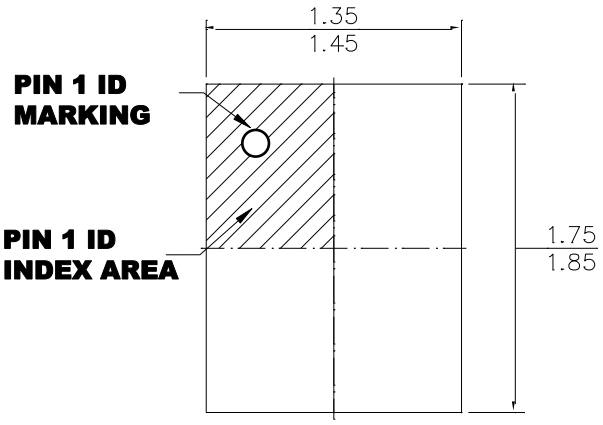


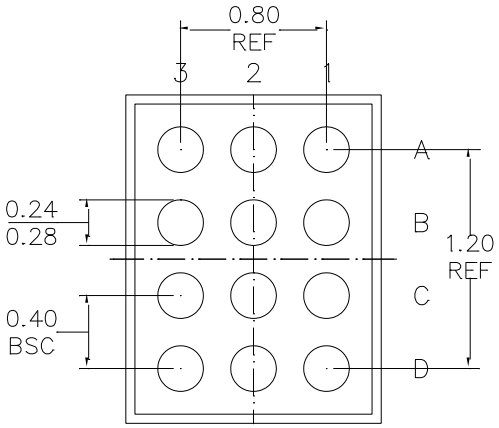
Figure 4: Typical application circuit with fixed 3.3V output voltage

PACKAGE INFORMATION

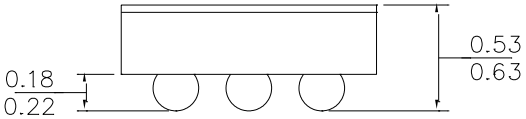
CSP-12 (1.4mmx1.8mm)



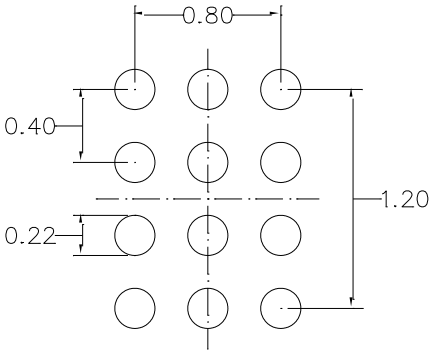
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.