MP5505

7V, 4A, High-Efficiency Energy Storage and Management Unit

The Future of Analog IC Technology

DESCRIPTION

MP5505 is a lossless energy storage and management unit targeted at the solid-state and hard-disk drive applications. Its highly-integrated input-current limit and energy storage and release management makes the system solution very compact.

The internal input-current–limit block with dv/dt control prevents inrush current during system start up. The bus voltage start-up slew rate is programmable. It also includes a Power-On-Reset function for hot-swapping. MPS's patented energy storage and release management control circuit minimizes the storage capacitor requirement. It pumps the input voltage to a higher storage voltage and releases the energy over a hold-up time to the system in the case of an input outage. The storage voltage and the release voltage are both programmable for different system applications.

The MP5505 requires a minimal number of readily-available standard external components, and is available in a 20-pin QFN (3mm×4mm) package.

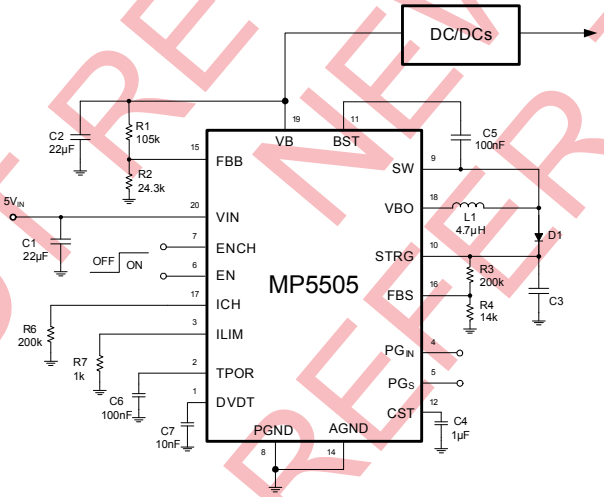
FEATURES

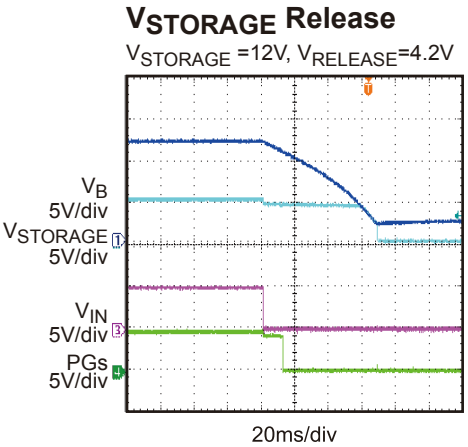
- Wide 2.7V-to-7V Operating Input Range
- Input Current Limiter with Integrated 60mΩ MOSFET
- Up to 4.5A Input Current Limit
- Reverse Current Protection
- 6V Bus Clamping Voltage
- Power-On-Reset
- Adjustable dv/dt Slew Rate for Bus Voltage Start-Up
- Internal 30mΩ Disconnect Switch
- Internal 70mΩ and 60mΩ Power Switches for Energy Storage and Release Management Circuits
- Thermal Protection
- EN and Power-Good Indicators
- Available in a QFN20 (3mm×4mm) Package

APPLICATIONS

- Solid-State Drives
- Hard-Disk Drives
- Power Back-up/Battery Hold-up Supplies

TYPICAL APPLICATION



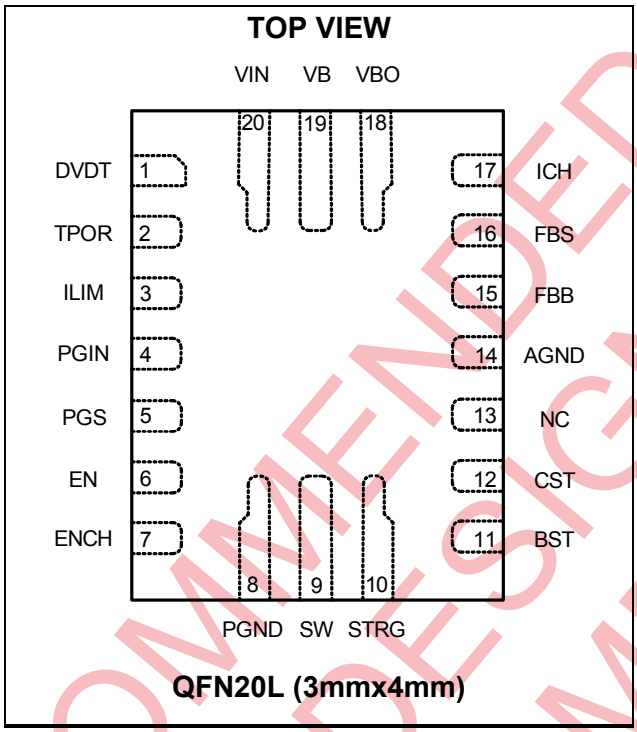


ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5505GL	QFN20L (3mmx4mm)	MP5505

* For Tape & Reel, add suffix –Z (e.g. MP5505GL–Z);

PACKAGE REFERENCE



QFN20L (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 8.0V
V_{STRG} ..... -0.3V to 35V
V_{SW} ..... -0.3V to V_{STRG}+0.3V
V_{BST} ..... -0.3V to V_{STRG}+6.5V
V_{CST} ..... -0.3V to 40V
All Other Pins ..... –0.3V to 6.5 V
Continuous Power Dissipation (T_A = +25°C) (2) 2.6W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Operating Temperature ..... –40°C to +85°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 7V
Bus Voltage V_B ..... 2.7V to 6V
Storage Voltage V_{STRG} ..... V_{IN} to 30V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
QFN20 (3mmx4mm)	48	10 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage Range	V_{IN}		2.7		7	V
Supply Current (Shutdown)	I_S	V_{EN}=0V			2	μA
Supply Current (Quiescent)	I_Q	$V_{EN/EN1/EN2}$=2V, $V_{FB1/FB2}$=1V			2	mA
Thermal Shutdown (6)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (6)	T_{HYS}			30		°C
VIN Under Voltage Lockout Threshold Rising	$INUV_R$			2.5	2.7	V
VIN Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$		0.3	0.4	0.5	V
EN UVLO Threshold Rising	EN_R				1.2	V
EN UVLO Threshold Falling	EN_F		0.4			V
Current Limit FET ON Resistance	R_{DSON}	T_a=25°C		60	65	mΩ
Continuous Current Limit	I_{LIM}	R_{ILIM}=1.07kΩ		4.6		A
		R_{ILIM}=1.2kΩ		4.1		
		R_{ILIM}=1.4kΩ	-10%	3.7	10%	
Off State Leakage Current	I_{LEAK}	V_{IN}=6V, V_B=0V or V_B=6V, V_{IN}=0V			2	μA
Clamping Voltage	V_{CLAMP}	V_{IN}=7V	+10%	6	+10%	V
Rise Time (dv/dt)	τ_R	DVDT pin floating	0.5	0.9	1.5	ms
		$C_{dv/dt}$=10nF		10		
		$C_{dv/dt}$=100nF		100		
Internal RESET Delay Time	τ_D	TPOR pin floating		0.4		ms
		C_{TPOR}=100nF		100		
		C_{TPOR}=500nF		500		
Pre-charge current	$I_{CH\ PRE}$			130		mA
Charge Peak current @ Boost Mode	I_{CH}	ICH pin floating		500		mA
		R_{ICH}=100kΩ		400		
		R_{ICH}=200kΩ		200		
Boost Disconnect Switch R_{on}	R_{dison}			30	35	mΩ
Energy Management HS R_{on}	R_{Hon}			70		mΩ
Energy Management LS R_{on}	R_{Lon}			60		mΩ
Feedback Voltage	V_{FBB}, V_{FBS}		0.77	0.79	0.81	V
Feedback Current	I_{FBB}	V_{FB1}=V_{FB2}=0.79V			50	nA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5.0V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG_S High Threshold	$PG_{H\ S}$			0.95		V_{FBS}
PG_S Low Threshold	$PG_{L\ S}$			0.9		V_{FBS}
PG_S Delay	$PG_{D\ S}$			20		µs
PG_S Sink Current Capability	$V_{PG\ S}$	Sink 4mA			0.3	V
PG_S Leakage Current	$I_{PGS\ L}$	V_{PGS}=3.3V			120	nA
PG_{IN} High Threshold	$PG_{H\ IN}$			1.03		V_{FBS}
PG_{IN} Low Threshold	$PG_{L\ IN}$			1		V_{FBS}
PG_{IN} Delay	$PG_{D\ IN}$			4		µs
PG_{IN} Sink Current Capability	$V_{PG\ IN}$	Sink 4mA			0.3	V
PG_{IN} Leakage Current	$I_{PGIN\ L}$	V_{PGIN}=3.3V			120	nA
Buck-Mode Dumping-Current Limit	I_{DUMP}			5		A
Release-Buck Switching Frequency	f_{s_RLS}	V_{STRG} from 20V to 5V		500		kHz
VB Under-Voltage Lockout Threshold, Rising[5)]	$INUVB_R$		1.8	2.2	2.5	V
VB Under-Voltage Lockout Threshold, Hysteresis[5)]	$INUVB_{HYS}$		0.15	0.25	0.35	V

Notes:

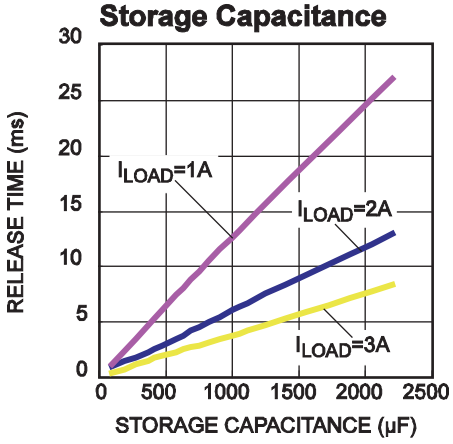
5) VB UVLO is applied to Energy Storage and Release Circuitry

6) Guaranteed by design.

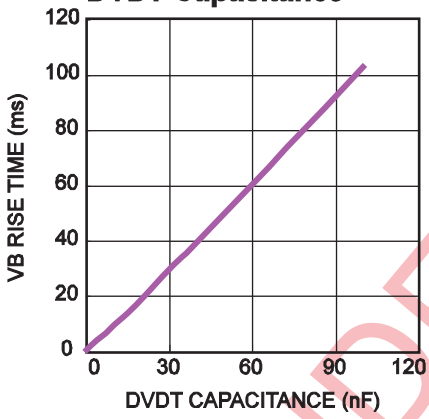
TYPICAL CHARACTERISTICS

V_{IN} = 5V, $V_{STORAGE}$ = 12V, $V_{RELEASE}$=4.2V, L = 4.7µH, T_A = 25°C, unless otherwise noted.

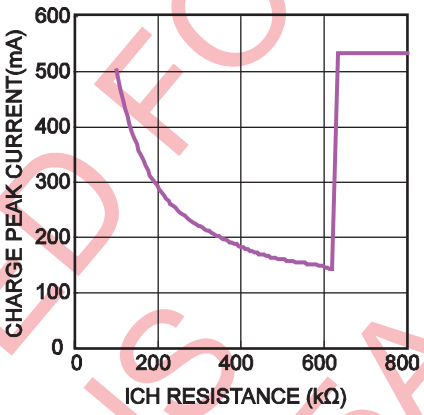
Release Time vs. Storage Capacitance



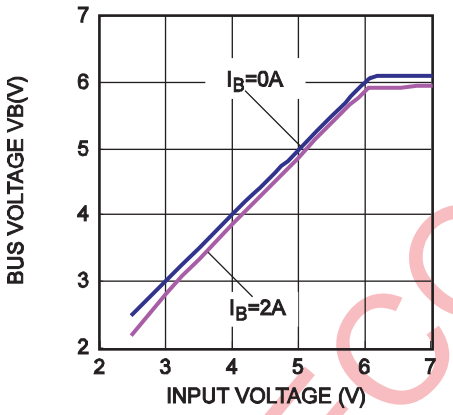
VB Rising Rate vs. DVDT Capacitance



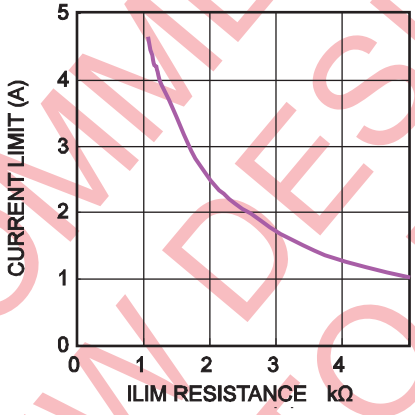
Boost Charge Peak Current vs. ICH Resistor



VB Bus Clamping Voltage



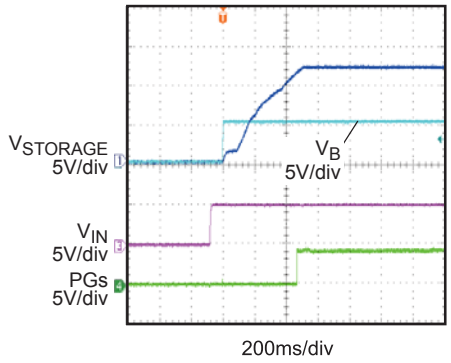
VIN to VB Current Limit



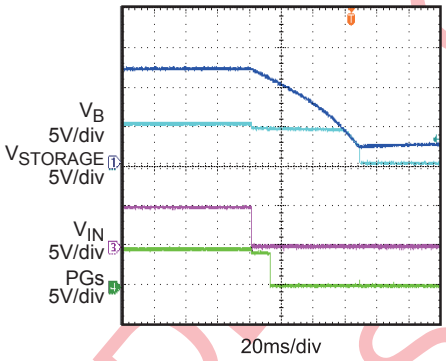
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 5V, $V_{STORAGE}$ = 12V, $V_{RELEASE}$=4.2V, L = 4.7μH, T_A = 25°C, unless otherwise noted.

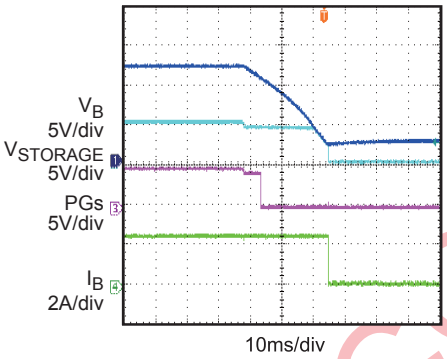
$V_{STORAGE}$ Charge



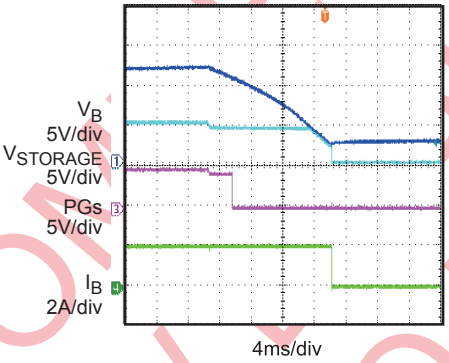
$V_{STORAGE}$ Release



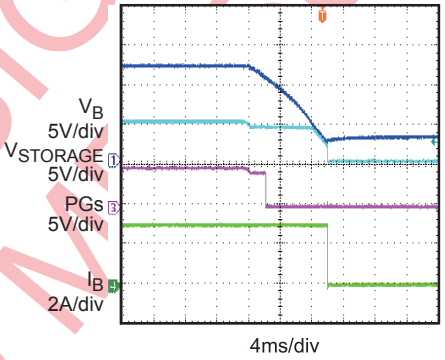
Release Time
Pb=5W, C Storage=2200μF



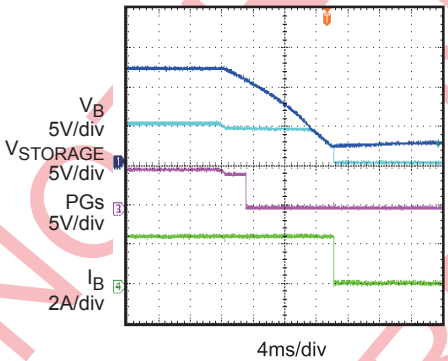
Release Time
Pb=8W, C Storage=2200μF



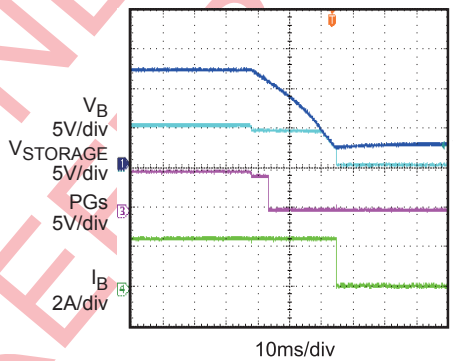
Release Time
Pb=12W, C Storage=2200μF



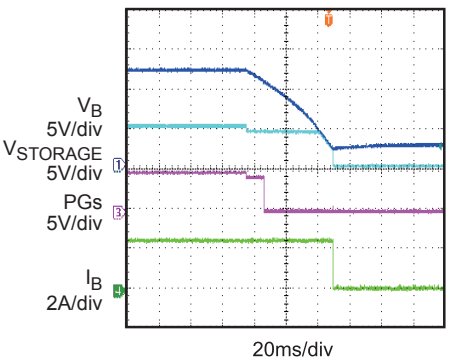
Release Time
Pb=5W, C Storage=1000μF



Release Time
Pb=5W, C Storage=2200μF



Release Time
Pb=5W, C Storage=4400μF



PIN FUNCTIONS

QFN20 (3×4mm) Pin #	Name	I/O	Description
1	DVDT	I	Slew rate control pin for VB voltage during start up. Connect a capacitor from this pin to GND to program different VB charge up slew rate. Leave it open for the default soft start time of around 0.9ms from 0V to VIN.
2	TPOR	I	Power-on-reset delay time for VB start up. When VIN and EN are ready and after this programmable delay time, VB starts to charge up. Connect a capacitor between this pin and GND to select different delay time. Leave it open for the default power-on-reset delay time of 0.4ms.
3	ILIM	I	Input current limit setting pin. Connect a resistor between this pin and GND to adjust the current limit of the input current limiter. This pin cannot be left open.
4	PG_{IN}	O	VB Power-Good Indicator. This pin is an open drain output. PG_{IN} goes HIGH if the FBB voltage exceeds $1.03\times V_{FBB}$ which is typically 0.813V. PG_{IN} goes LOW if the FBB voltage drops below $1.0\times V_{FBB}$ which is 0.79V.
5	PG_S	O	Storage Voltage Power-Good Indicator. This pin is an open drain output. PG_S goes HIGH if the FBS voltage exceeds $0.95\times V_{FBS}$ which is 0.75V. PG_S goes LOW if the FBS voltage drops below $0.9\times V_{FBS}$ which is 0.71V.
6	EN	I	ON/OFF control pin for MP5505. When EN is pulled low, all the functions of MP5505 will be disabled, for both input current limiter and charge/release circuitry. Make sure EN voltage is high during releasing.
7	ENCH	I	ON/OFF control pin for charge and release circuitry. When the ENCH is pulled down, the release circuitry is disable, note that ENCH needs to be keep high to achieve energy release.
8	PGND	I/O	Power ground.
9	SW	O	Switch output for the charge and release circuitry. Connect a small inductor between this pin and VBO pin.
10	STRG	O	Storage voltage pin. Connect appropriate storage capacitors for energy storage and release operation
11	BST	NC	Bootstrap pin for charge and release circuitry. The internal bi-directional switcher requires the bootstrap capacitor 100nF from this pin to SW pin to supply the high-side switch driver voltage during releasing.
12	CST	O	High side switch driving voltage storage pin. MP5505 can support energy even when storage voltage is close to the VB regulated voltage..
13	NC	NC	No Connect
14	AGND	I/O	IC Ground
15	FBB	I	Bus Voltage Feedback Sense. Sets the bus voltage release.
16	FBS	I	Storage Voltage Feedback Sense. Sets the storage voltage.
17	ICH	I	Boost-Mode Current Limit Adjustment Pin. This pin cannot be pulled to VCC or pulled to external voltage source.
18	VBO	O	Internal Boost. The input voltage after passing through input isolation FET.
19	VB	O	Internal Bus Voltage. Requires a 22μF-to-47μF ceramic capacitor as close to this pin as possible.
20	VIN	I	Input Supply Voltage. The MP5505 operates from an unregulated 2.7V-to-7V input. Place a 10μF-to-22μF ceramic capacitor as close to the pin as possible.

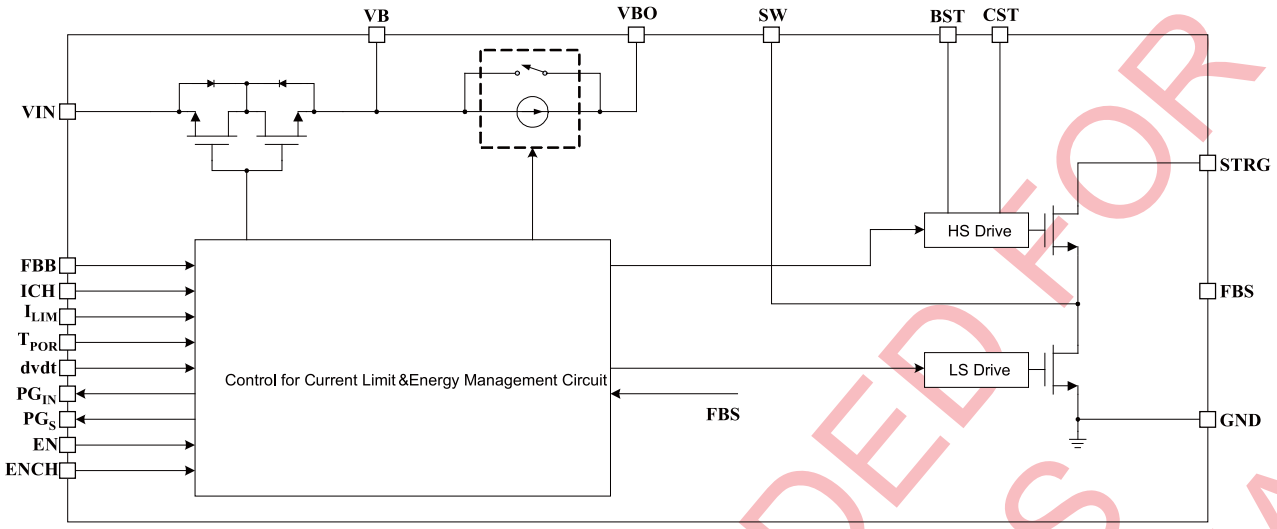


Figure 1: Functional Block Diagram

OPERATION

The MP5505 is an energy storage and management unit in a 3mm×4mm 20-pin QFN package. It provides very compact and efficient energy management solution for a typical solid-state–drive or hard-disk–drive application. MPS's patented lossless energy storage and release management circuits use a bi-directional Buck/Boost converter to achieve optimal energy transfer and provide the most cost-effective energy storage solution.

The integrated boost converter raises the energy-storage voltage level. The storage feedback resistor divider sets the storage voltage. When the input suddenly shuts down, the internal Buck converter transfers the energy from the storage capacitor to the bus and keep holds the bus voltage when the system consumes the energy from the storage capacitor. The buck converter can work in 100% duty cycle operation to fully deplete the stored energy.

Start-Up

When VIN starts up, the bus voltage VB is charged from 0 to nearly VIN. The VB rising slew rate is controlled by DVDT capacitance. This function avoids the input inrush current and provides protection to the whole system.

EHCH is used to enable the storage charge and release circuitry. When ENCH is already high before VB finishing DVDT process, the storage charge circuitry will work automatically when VIN is higher than UVLO which is 2.5V typically.

The storage charge circuitry operates in two modes: the pre-charge mode where the STRG voltage is charged to VB voltage by using a current source and the boost mode where the STRG voltage is charged to finally setting voltage. The pre-charge mode charges the STRG voltage up to nearly VB voltage by using almost constant current source. The current is around 130mA. When STRG voltage is close to VB, and VB voltage is higher than certain threshold where the corresponding FBB is higher than 0.813V, the boost mode initiates.

The boost mode charges the STRG voltage to the target voltage finally. Figure 2 shows the charging build-up process when ENCH is high before VB starts up.

It is strongly recommended for our customers to enable the ENCH after VB is well settled down which is shown in Figure 3. Because the release mode is triggered when FBB voltage is lower than 0.79V, although there is a 23mV hysteresis between boost mode and release mode, in some high current charge boost mode case which can be programmed by ICH, VB voltage might be pulled low back and wrongly enter the release mode. In order to avoid this, the ENCH pin is suggested to be enabled after VB settling down. Figure 3 shows the charging build-up process when ENCH is enabled after VB settles down.

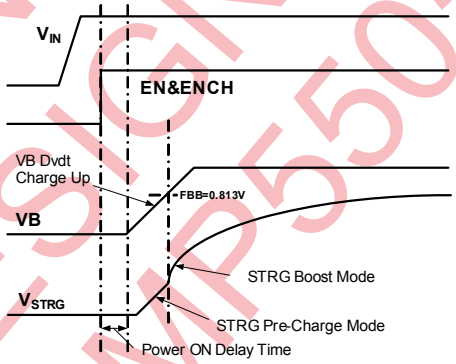


Figure 2: Charging Process

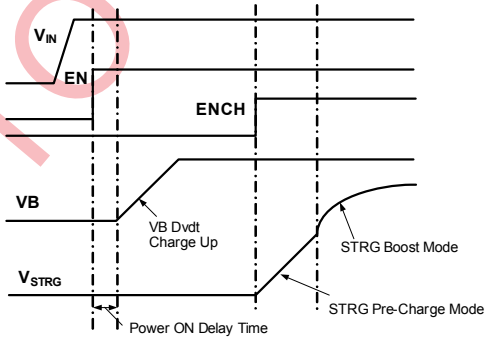


Figure.3 Charging Process when EN and ENCH Separated

Storage Voltage

After the start up period, the internal Boost converter automatically regulates the storage voltage to a set value. The MP5505 uses burst mode to minimize the converter's power loss. When the storage voltage drops below the set voltage, burst mode initiates and charges the storage capacitor. During the burst period, the current limit and the low-side MOSFET control the switch. When the power MOSFET turns on, the inductor current increases until it reaches its current limit. The boost current limit can be programmable by ICH resistor. By default, it is around 500mA. After hitting the current limit, the power MOSFET turns off for the set minimum OFF time. At the end of this minimum OFF time, if the feedback voltage remains below the 0.79V internal reference, the power MOSFET turns on again; otherwise the MP5505 waits until the voltage drops below the threshold before turning on the MOSFET.

Release

The MP5505 continuously monitors the input and bus voltages. Once the bus voltage drops below the selected release voltage (such as when losing input power), the internal boost converter stops charging and works in buck release mode. In buck mode, the part transfers energy from the high-voltage storage capacitor to the low-voltage bus capacitor. Determine the release voltage by selecting resistor values for the bus resistor divider. The buck release current can be as high as 4.5A.

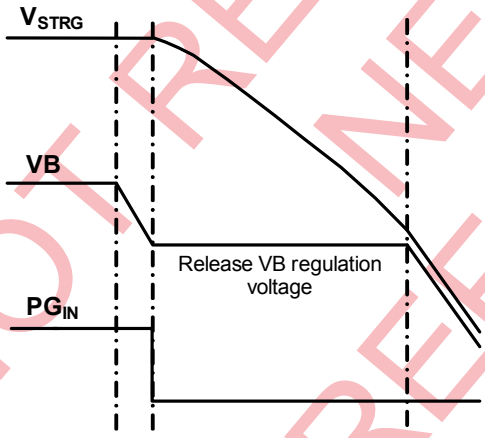


Figure 4: Release Times

The released Buck applies the fixed-frequency constant-on-time (COT) enables the fast transition between charge and release modes. The buck converter works at 100% duty cycle until the storage capacitor voltage approaches the bus voltage. Then the storage and bus voltages drop until they reach the DC-DC converter's UVLO, as shown in Figure 4.

Input-Current Limit

The input-current limiter carefully controls the input inrush current of the internal hot-swap MOSFET to prevent an inrush current from the input to the bus. A capacitor connected to dv/dt pin can set the soft-start time. Despite of the soft-start process, the ILIM pin can also limit the steady-state current. Connect a resistor between ILIM and GND to set the current limit.

Reverse-Current Protection

The hot-swapping circuit uses reverse-current protection to prevent the storage energy from transferring back to the input during energy released from storage capacitors to bus. The hot-swapping MOSFET turns on when input voltage exceeds the VIN UVLO threshold during start up, and turn off when input voltage falls below the bus voltage during release.

Start-Up Sequencing

Connect a capacitor across the DVDT pin to program the soft-start time. During soft-start, the energy storage capacitors charge. Very short dv/dt times can trigger the current-limit threshold. Select the DVDT capacitor based on the storage capacity.

Storage Power-Good Indicator, PG_S

When the voltage on the FBS pin (storage feedback) drops below $0.9\times V_{FBS}$, the MP5505 internally pulls the storage PGS pin LOW. When the FBS voltage is above $0.95\times V_{FBS}$, this pin goes HIGH.

Bus Power-Good Indicator, PG_{IN}

When the voltage on FBB pin (bus feedback) falls below $1.0\times V_{FBB}$, the MP5505 pulls PG_{IN} LOW to indicate releasing status. When MP5505 works in Boost mode, the PG_{IN} will be pulled high to indicate charging status.

APPLICATION INFORMATION

Setting the Storage Voltage

Set the storage voltage by choosing the external feedback resistors R1 and R2 shown in Figure 5.

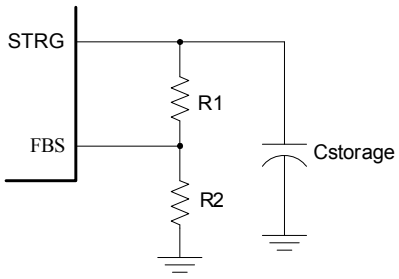


Figure 5: Storage Feedback Circuit

The storage voltage is determined by:

$$V_{STORAGE} = (1+\frac{R1}{R2}) \times V_{FBS}$$

Where V_{FBS} is 0.79V typically. R1 and R2 are not critical for normal operation. Select R1 and R2 higher than 10kΩ to account for the bleed current. For example, if R2 is 14kΩ, R1 is then:

$$R1 = \frac{14k\Omega \times (V_{STORAGE} - V_{FBS})}{V_{FBS}}$$

For a 12V storage voltage, R1 is 200kΩ.

Table 1 lists the recommended resistors for different storage voltages.

Table 1: Resistor Pairs for $V_{STORAGE}$

$V_{STORAGE}$(V)	R1 (kΩ)	R2 (kΩ)
8	127	14
12	200	14
20	340	14

Select Release Voltage and Input Capacitors

Select the release voltage by choosing the external feedback resistors R3 and R4 as shown in Figure 6.

Similarly, the release voltage is:

$$V_{RELEASE} = (1+\frac{R3}{R4}) \times V_{FBB}$$

V_{FBB} is also 0.79V typically. However, R3 and R4 not only determine the release voltage, but affect stability. Since the release buck mode works in COT mode, avoid small resistor values to ensure a sufficient voltage ramp. Generally, choose R3//R4≥20kΩ for stable performance with C_B=22μF. Table 2 lists the recommended resistor values for different release voltages.

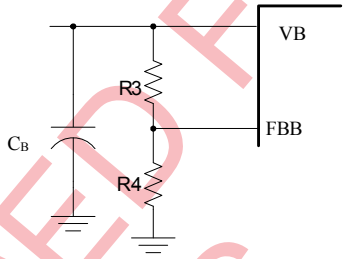


Figure 6: Release Feedback Circuit

Table 2: Resistor Pairs for $V_{RELEASE}$

$V_{RELEASE}$ (V)	R3 (kΩ)	R4 (kΩ)
4.2	105	24.3
2.9	107	40.2

Selecting the Storage Capacitor

The storage capacitor stores energy during normal operation and releases this energy to VIN when VIN loses input power. Use a general-purpose electrolytic capacitor or low profile POS capacitor for most applications.

Select a storage capacitor with a voltage rating that exceeds the targeted storage voltage. The stable voltage on the storage capacitor during normal operation allows for full capacitor utilization. Consider the capacitance reduce with the DC voltage offset when choosing the capacitors. Different capacitors have different capacitance derating performance. Choose capacitor with enough voltage rating to guarantee enough capacitance.

The required capacitance depends on the length of the "dying gasp" for a typically application. Assume the input release current is $I_{RELEASE}$ when input voltage is regulated at $V_{RELEASE}$ for the DC-DC converter, the storage is $V_{STORAGE}$, and the required dying gasp time is τ_{DASP}. The required storage capacitance is then:

$$C_S = \frac{2 \times V_{RELEASE} \times I_{RELEASE} \times \tau_{DASP}}{V_{STORAGE}^2 - V_{RELEASE}^2}$$

Consider of the power loss during releasing where the Buck converter can run up to 90% efficiency in most application, select storage capacitance to 1.1xCs to ensure enough releasing time. If $I_{RELEASE}$=1A, τ_{DASP}=20ms, $V_{STORAGE}$=12V, $V_{RELEASE}$=4.2V, then the required storage capacitance is 1500μF.

For typical applications using a 5V input supply, set the storage voltage above 10V to fully utilize the high-voltage energy and minimize the storage capacitance requirements. Generally, use the 16V POS capacitor or 25V electrolytic capacitors.

Selecting the External Diode

The external diode is strongly recommended for normal operation of charge mode where the boost converter works. The voltage rating should be higher than the storage voltage and the current rating should be high than the current programmed by ICH pin.

Setting the Input Hot-Swap Current Limit

Connect a resistor from ILIM to GND to set the current limit value. For example, a 1.2kΩ resistor sets the current limit to about 4.1A. Table 3 lists the recommended resistors for different current limit values.

Table 3: I_{LIM} vs. R_{LIM}

I_{LIM}(A)	R_{LIM} (kΩ)
4.6	1.07
4.1	1.2
3.7	1.4
1.6	3.2

Selecting Inductor

The inductor is necessary to supply constant current to the load. Since the Boost mode and Buck mode are sharing the same inductor, and generally the Buck mode current is higher, the inductor supporting at least the Buck mode releasing current is recommended.

Selecting the inductor based on Buck releasing mode. If the storage voltage is VS, the release voltage is VR, and Buck running at fixed 500kHz frequency. The inductance value can be calculated by:

$$L = \frac{V_R}{\Delta I_L \times F_{SW}} \times (1 - \frac{V_R}{V_S})$$

Where ΔI_L is the peak to peak inductor ripple current which can be set in the range of 30% to 40% of full releasing current.

The inductor should not saturate under the maximum inductor peak current.

Setting the Power-On Reset Delay Time

Connect a capacitor to the TPOR pin to set the power on reset delay time. Leave it floating for the default delay time of around 0.4ms. Table 4 lists the recommended capacitors for different delay times. In order to eliminate the power on reset delay, connect the TPOR pin directly to VIN.

Table 4: Reset Delay vs. Capacitor Value

τ_D (mS)	C_{TPOR} (nF)
100	100
500	500

Setting the Bus Voltage Rise Time

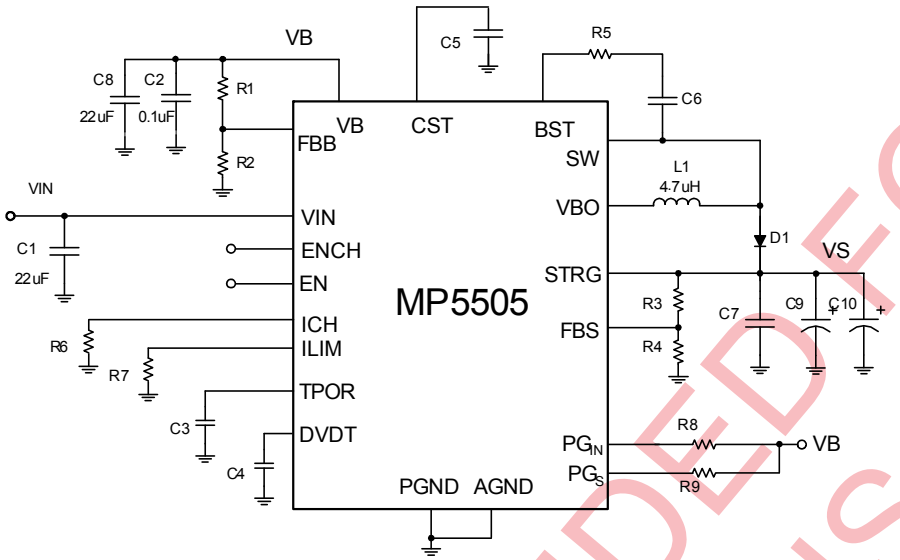
Connect a capacitor to the DVDT to set the bus voltage start-up slew rate and soft-start time. Leave it floating for the default soft start time of around 0.9ms from 0V to 5V. Table 5 lists the recommended capacitors for different soft-start times.

Table 5: Soft-Start vs. Capacitor Value

τ_R (mS)	$C_{dv/dt}$ (nF)
10	10
100	100

Layout Recommendation

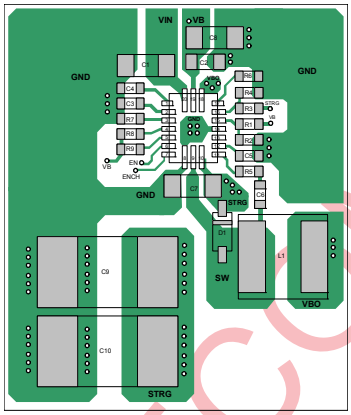
1) The high current paths (VIN, VB, VBO, SW, STRG, GND) should use short, wide and direct traces.
2) Put the decoupling capacitor across VB and GND as close as possible.
3) Put the decoupling capacitor across STRG and GND as close as possible.
4) Keep the switching node SW short and away from the feedback network.
5) The external feedback resistors should be placed next to FB pins.
6) Keep the BST voltage path (BST, C6, R5 and SW) as short as possible.
7) Four-layout is recommended to achieve better thermal performance and easily layout.



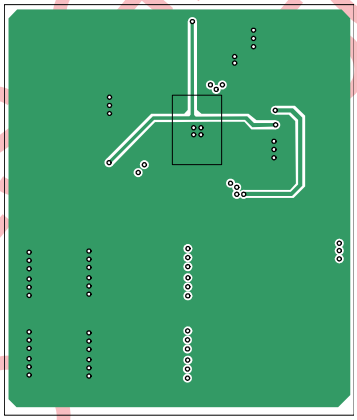
Schematic for Layout

Please take following figures as sampled layout (with four layers).

Top Layer:



Inner Layer 2:



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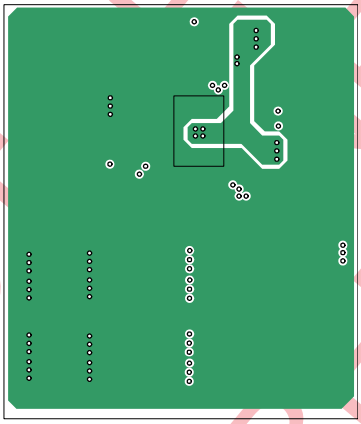


Bottom Layer:

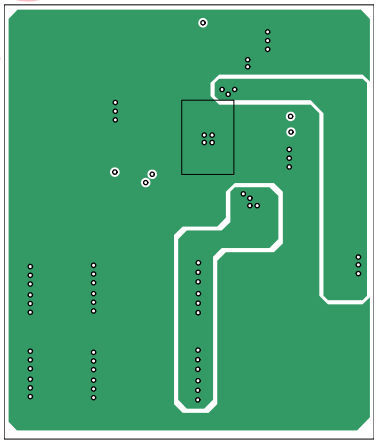


Figure 7: Layout Recommendation

Design Example

Below is a design example following the application guidelines for the specifications:

Table 6: Design Example

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	5	V
Charge Voltage	V_{STRG}	12	V
Regulated Bus Voltage at Pfail	V_{RLS}	4.2	V
Boost Mode Max Charge Current	I_{CHARGE}	0.5	A
Buck Mode Max Output Current at Pfail	$I_{RELEASE}$	4	A

The detailed application schematic is shown in Figure 8. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

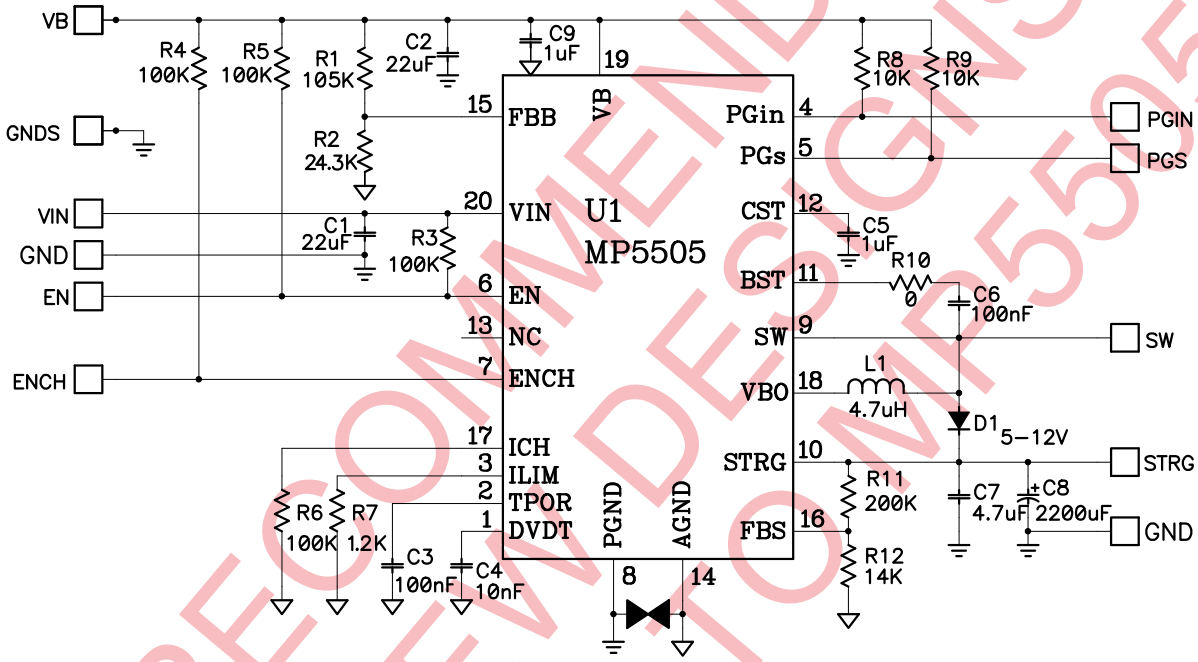
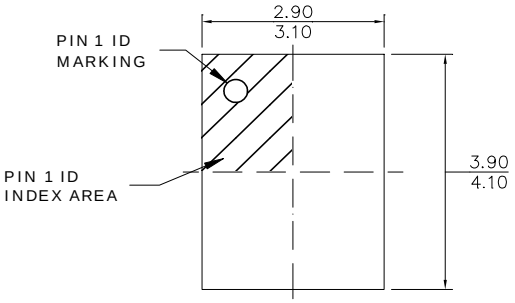


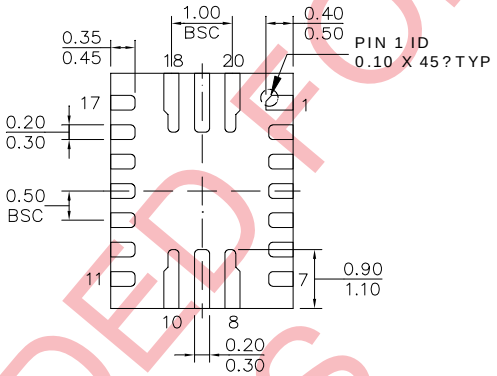
Figure 8: Detailed Application Schematic

PACKAGE INFORMATION

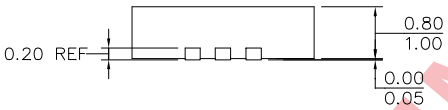
QFN20L (3mmx4mm)



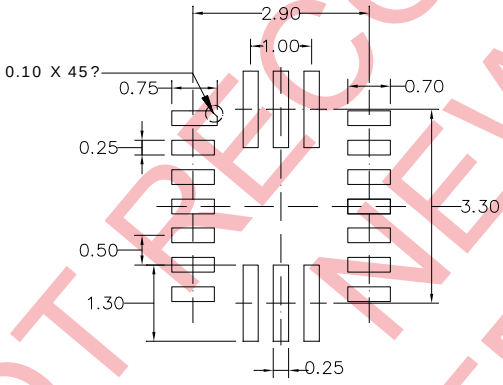
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.