MP8845C

5A High Efficient Synchronous Step-Down Switchers with I²C Interface

The Future of Analog IC Technology

DESCRIPTION

The MP8845C is a highly integrated and high frequency synchronous step-down switcher with I²C control interface. It is optimized to support up to 5A load current over an input supply range from 2.7V to 6V with excellent load and line regulation.

Constant frequency hysteretic control mode provides extremely fast transient response without loop compensation and easily achieves high efficiency under light load condition.

The output voltage level can be controlled, on-the fly through a 3.4Mbps I²C serial interface. Voltage range can be adjusted from 0.6V to 1.45V in 6.69mV steps. Voltage slew rate, switching frequency and power savings mode are also selectable through the I²C interface.

Fully protection features includes internal soft start, over current protection and over temperature protection.

The MP8845C requires a minimum number of readily available standard external components and is available in the compact WLCSP20-(1.70mmx2.10mm) package.

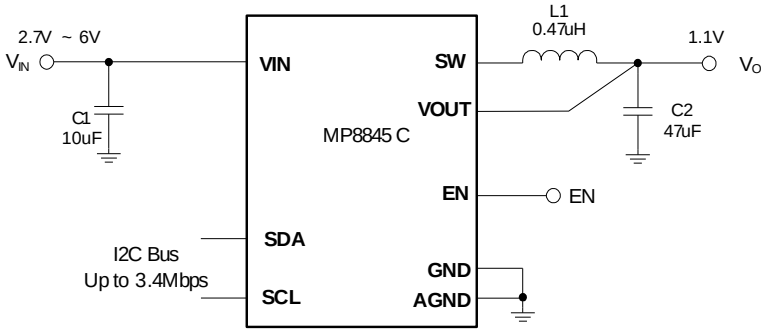
FEATURES

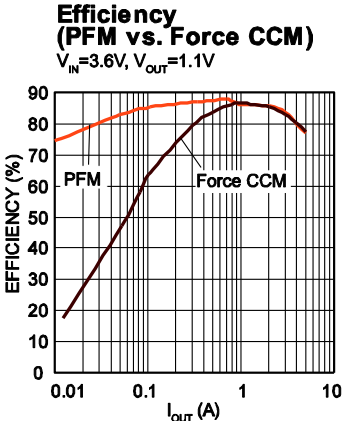
- 2.7V to 6V Input Voltage Range
- Up to 5A Load Current
- Internal 32mΩ High-Side, 17mΩ Low-Side Power MOSFETs
- Fixed Frequency Hysteretic Mode Control
- I²C Compatible Interface up to 3.4Mbps
- I²C Programmable Output Range from 0.6V to 1.45V in 6.69mV Steps
- Factory Adjustable Switching Frequency from 1MHz to 2.2MHz
- I²C Programmable Voltage Transition Slew Rate
- Power Saving Mode Selectable via I2C
- Internal Soft-Start
- Current Overload and Thermal Shutdown Protection
- Available in 20-ball WLCSP-1.70mmx2.10mm package

APPLICATIONS

- Processor Core Supply
- Micro Converter

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8845CGC	WLCSP-20(1.70mmx2.10mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP8845CGC–Z);

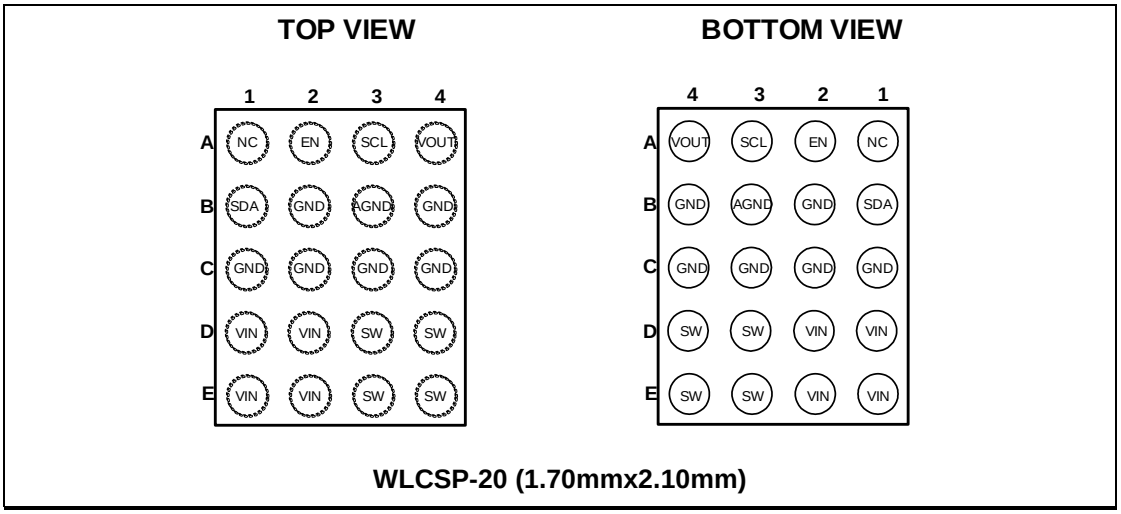
TOP MARKING

BRY

LLL

BR: product code of MP8845CGC
Y: year code
LLL: lot number

PACKAGE REFERENCE



WLCSP-20 (1.70mmx2.10mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} ..... -0.3V to 6.5 V
V_{SW} .....–0.3V(-2V<5ns) to V_{IN}+0.3 V (8V<5ns)
All Other Pins..... –0.3V to 6.5 V
Junction Temperature.....150°C
Lead Temperature .....260°C
Continuous Power Dissipation (T_A = +25°C) (2)
WLCSP-20(1.70mmx2.10mm) 1.31W
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.7V to 6V
Output Voltage V_{OUT}..... 0.6V to 1.45V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

WLCSP-20(1.70mmx2.10mm)	95	30	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C. The limit over temperature is guaranteed by characterization, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.7		6	V
Quiescent Current (5)	I_Q	Io=0A, switching, PWM mode		18		mA
Shut Down Current	I_S	V_{EN}=GND, V_{IN}=4.2V		10		μA
Internal Reference Voltage	V_{REF}	T_J=25°C	0.594	0.6	0.606	V
		T_J = -40°C to 125°C	0.588	0.6	0.612	
Lowest Output Voltage	V_{LOW}	Register = 00h, T_J=25°C	0.594	0.6	0.606	V
		T_J = -40°C to 125°C	0.588	0.6	0.612	
Highest Output Voltage	V_{HIGH}	Register = 7Fh, T_J=25°C	1.435	1.45	1.465	V
		T_J = -40°C to 125°C	1.421	1.45	1.479	
Output Voltage Step	V_{STEP}			6.69		mV
High Side Switch On Resistance	R_{HSON}			32		mΩ
Low Side Switch On Resistance	R_{LSON}			17		mΩ
UVLO Rising Threshold	V_{UVLOR}			2.45	2.7	V
UVLO Hysteretic	V_{UVLOHY}			200		mV
Switching Frequency Range	F_{SW}		1		2.2	MHz
Frequency Variation	F_{SW}			20%		
Minimum On Time (5)	T_{MINON}			60		ns
Switch Leakage	I_{SW}	V_{EN}=0V, V_{IN}=5V, V_{SW}=0V and 5V			1	uA
EN leakage Current	I_{EN}	V_{IN}=V_{EN}=4.2V			1	uA
EN pull down resistance	R_{EN}	V_{EN}=0V		1		MOhm
EN Logic Low Voltage	V_{ENH}				0.4	V
EN Logic High Voltage	V_{ENL}		1.8			V
High Side Switch Peak Current Limit (source)	I_{peak}		7.5	9	10.5	A
High Side Switch Valley Current Limit (5)	I_{valley}			5.8		A
Low Side Switch Current Limit (sink) (5)				-5		A
Soft-Start Time	T_{SS-ON}	From V_{EN} on to V_O rise to 90% target value		0.4		ms
Thermal Warning (5)				130		°C
Thermal Shutdown (5)				150		°C
DAC Resolution				7		Bits

Note:

5) Not production tested; guaranteed by design.

I/O LEVEL CHARACTERISTICS

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	0.3Vcc	-0.5	0.3Vcc	V
High-level input voltage	V_{IH}		0.7Vcc	Vcc+0.5	0.7Vcc	Vcc+0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	Vcc>2V	0.05Vcc	-	0.05Vcc	-	V
		Vcc<2V	0.1Vcc	-	0.1Vcc	-	
Low-level output voltage(Open drain) at 3mA sink current	V_{OL}	Vcc>2V	0	0.4	0	0.4	V
		Vcc<2V	0	0.2Vcc	0	0.2Vcc	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL=3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at Vcc level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{cs}	SCLH output levels between 0.3Vcc and 0.7Vcc	2	6	2	6	mA
Rise time of the SCLH or SCL signal	t_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	t_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of SDAH signal	t_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns

I/O LEVEL CHARACTERISTICS *(continued)*

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Fall time of SDAH signal	t_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O pin	I_i	Input voltage between 0.1Vcc and 0.9Vcc	-	10	-10	+10	uA
Capacitance for each I/O pin	C_i		-	10	-	10	pF

I2C PORT SIGNAL CHARACTERISTICS

Parameter	Symbol	Condition	Cb=100pF		Cb=400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated START condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time (repeated) START condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	t_{LOW}		160	-	1300	-	ns
High period of the SCL clock	t_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	t_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	t_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	t_{fDA}		10	80	20*0.1Cb	300	ns

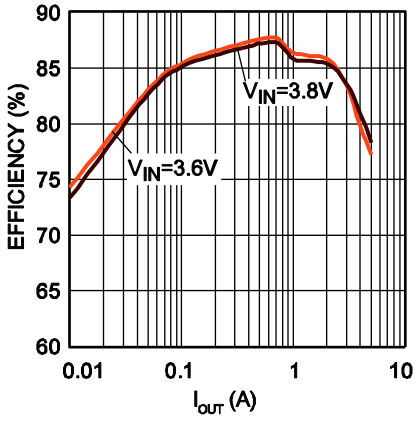
I2C PORT SIGNAL CHARACTERISTICS *(continued)*

Parameter	Symbol	Condition	Cb=100pF		Cb=400pF		Units
			Min	Max	Min	Max	
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for STOP condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a STOP and START condition	T_{BUF}		160	-	1300	-	ns
Data Valid Time	$T_{VD;DAT}$		-	160	-	900	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH+SDA line and SCLH+SCL line	-	400	-	400	pF
Noise margin at the LOW level	C_i	For each connected device	-	0.1Vcc	0.1Vcc	-	V
Noise margin at the HIGH level	V_{nH}	For each connected device	-	0.2Vcc	0.2Vcc	-	V

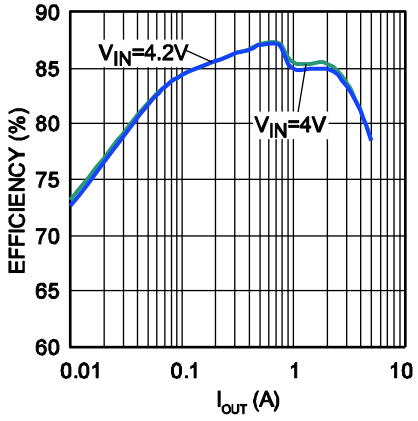
TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 1.1V, L = 0.47µH, C_{OUT}=2*22µF, T_A = 25°C, unless otherwise noted.

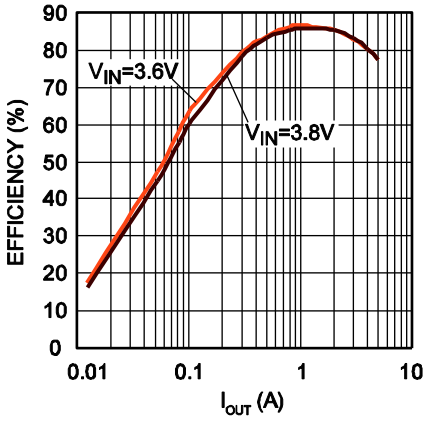
Efficiency
PFM



Efficiency
PFM



Efficiency
Force CCM



Efficiency
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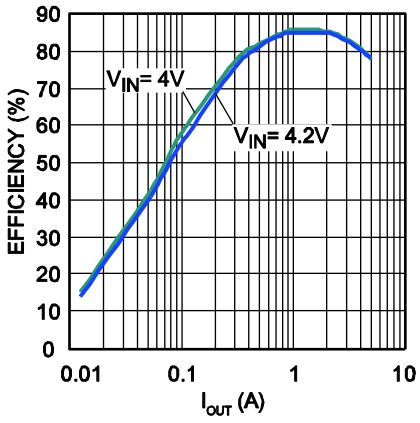
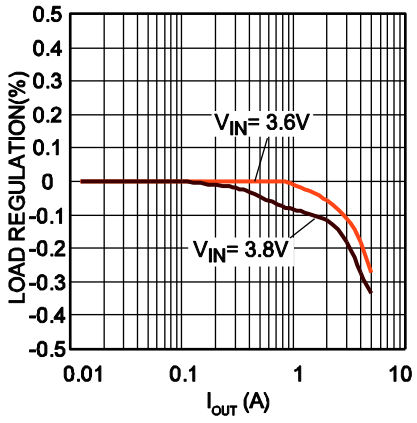
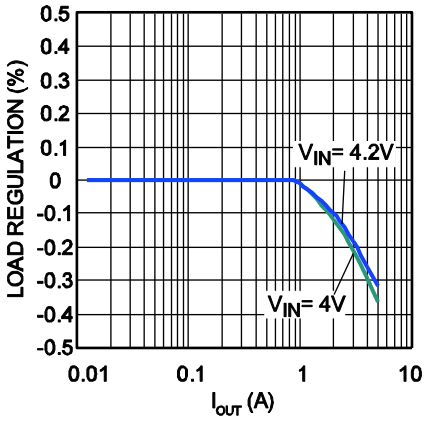


Load Regulation
Force CCM



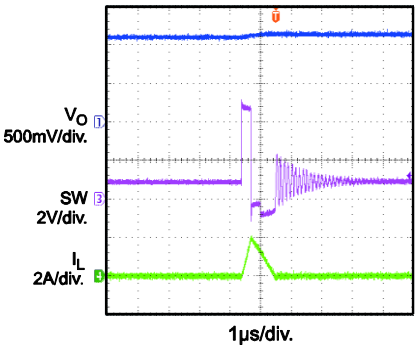
Load Regulation
Force CCM



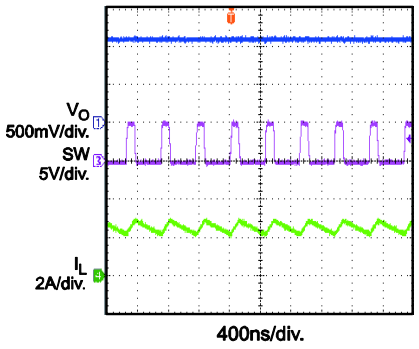
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.1V, L = 0.47µH, C_{OUT}=2*22µF, PFM, T_A = 25°C, unless otherwise noted.

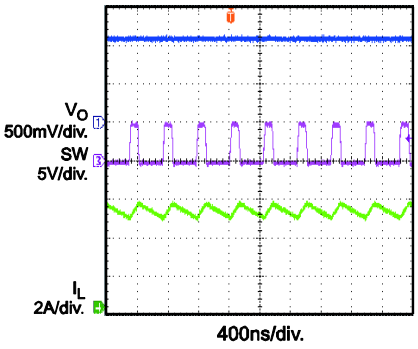
Steady State
I_{OUT} = 0A



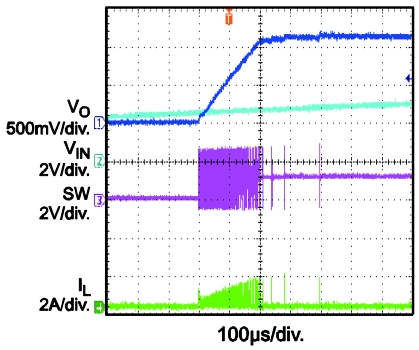
Steady State
I_{OUT} = 2.5A



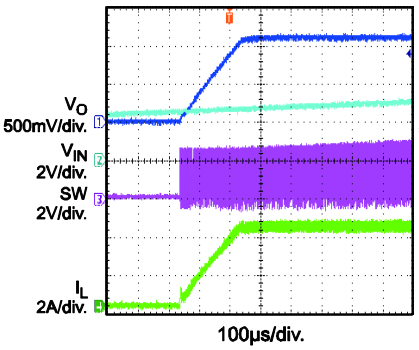
Output ripple
I_{OUT} = 5A



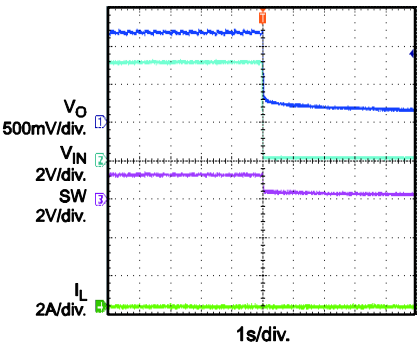
Vin power up without load
I_{OUT} = 0A



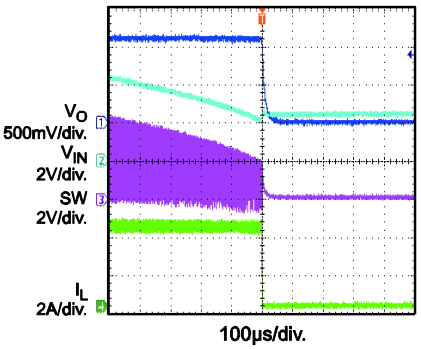
Vin power up full load
I_{OUT} = 5A



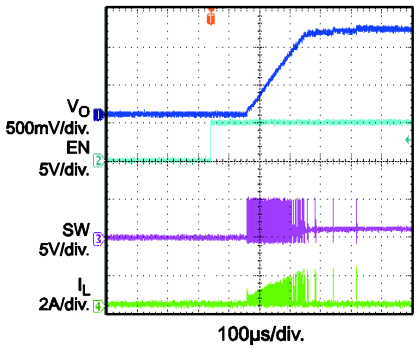
Vin power down without load
I_{OUT} = 0A



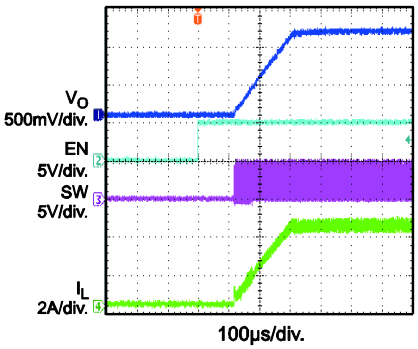
Vin power down full load
I_{OUT} = 5A



EN on without load
I_{OUT} = 0A



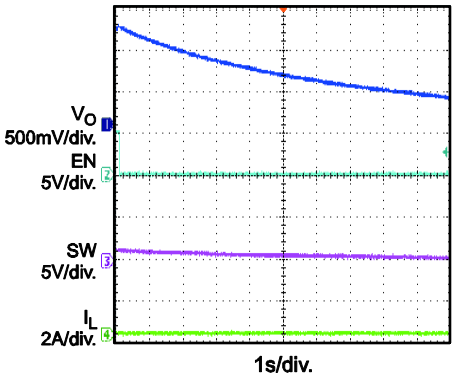
EN on with full load
I_{OUT} = 5A



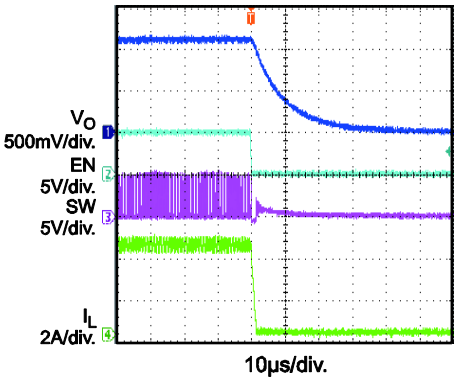
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.1V, L = 0.47µH, C_{OUT}=2*22µF, PFM, T_A = 25°C, unless otherwise noted.

EN down without load
I_{OUT} = 0A



EN down with full load
I_{OUT} = 5A



PIN FUNCTIONS

Package Pin #	Name	Description
A1	NC	Not Connect. Internal test use. Float it or connect to ground is ok.
A2	EN	ON and Off Control.
A3	SCL	I2C Serial Clock.
A4	VOUT	Output Voltage Sensing.
B1	SDA	I2C Serial Data.
B2, B4, C1-C4	GND	Power Ground.
B3	AGND	Analog Ground.
D1, D2, E1, E2	VIN	Input Supply Voltage.
D3, D4, E3, E4	SW	Switch Note.

REGISERS AND DESCRIPTION

Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	EN	Output reference						
01	SysCntlreg1	R/W	Switching frequency			Reserved	Reserved	Pglohi	Vinovp	Mode
02	SysCntlreg2	R/W	Reserved		Go	Out-dis	Reserved	Slew rate		
03	ID1	R	Vendor ID				Die id			
04	ID2	R	Reserved				Die rev			
05	Status	R	ILIM	UVLO	OVP	VoOV	VoUV	PGOOD	OTW	EN stat

Default Value of Register

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	1	1	0	0	1	0	1	1
01	SysCntlreg1	R/W	0	0	0	0	1	1	0	0
02	SysCntlreg2	R/W	0	0	0	0	0	0	0	1
03	ID1	R	0	0	0	1	0	0	0	1
04	ID2	R	0	0	0	0	0	0	0	0
05	Status	R	NA	NA	NA	NA	NA	NA	NA	NA

Register Description

1. Reg00 VSEL

NAME	BITS	DESCRIPTION
EN	D7	I2C controlled enable. When EN pin is low, the converter is off. When EN pin is high, the EN bit will take over
Output Reference	D[6:0]	Set output voltage from 0.6V to 1.45V as Table 1

Table 1— Output Voltage Chart

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
000 0000	0.6000	010 0000	0.8141	100 0000	1.0282	110 0000	1.2422
000 0001	0.6067	010 0001	0.8208	100 0001	1.0349	110 0001	1.2489
000 0010	0.6134	010 0010	0.8275	100 0010	1.0415	110 0010	1.2556
000 0011	0.6201	010 0011	0.8342	100 0011	1.0482	110 0011	1.2623
000 0100	0.6268	010 0100	0.8408	100 0100	1.0549	110 0100	1.2690
000 0101	0.6335	010 0101	0.8475	100 0101	1.0616	110 0101	1.2757
000 0110	0.6401	010 0110	0.8542	100 0110	1.0683	110 0110	1.2824
000 0111	0.6468	010 0111	0.8609	100 0111	1.0750	110 0111	1.2891
000 1000	0.6535	010 1000	0.8676	100 1000	1.0817	110 1000	1.2958
000 1001	0.6602	010 1001	0.8743	100 1001	1.0884	110 1001	1.3025
000 1010	0.6669	010 1010	0.8810	100 1010	1.0951	110 1010	1.3091
000 1011	0.6736	010 1011	0.8877	100 1011	1.1018	110 1011	1.3158
000 1100	0.6803	010 1100	0.8944	100 1100	1.1084	110 1100	1.3225
000 1101	0.6870	010 1101	0.9011	100 1101	1.1151	110 1101	1.3292
000 1110	0.6937	010 1110	0.9077	100 1110	1.1218	110 1110	1.3359
000 1111	0.7004	010 1111	0.9144	100 1111	1.1285	110 1111	1.3426
001 0000	0.7070	011 0000	0.9211	101 0000	1.1352	111 0000	1.3493
001 0001	0.7137	011 0001	0.9278	101 0001	1.1419	111 0001	1.3560
001 0010	0.7204	011 0010	0.9345	101 0010	1.1486	111 0010	1.3627
001 0011	0.7271	011 0011	0.9412	101 0011	1.1553	111 0011	1.3694
001 0100	0.7338	011 0100	0.9479	101 0100	1.1620	111 0100	1.3760
001 0101	0.7405	011 0101	0.9546	101 0101	1.1687	111 0101	1.3827

Table 1—Output Voltage Chart *(continued)*

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
001 0110	0.7472	011 0110	0.9613	101 0110	1.1753	111 0110	1.3894
001 0111	0.7539	011 0111	0.9680	101 0111	1.1820	111 0111	1.3961
001 1000	0.7606	011 1000	0.9746	101 1000	1.1887	111 1000	1.4028
001 1001	0.7673	011 1001	0.9813	101 1001	1.1954	111 1001	1.4095
001 1010	0.7739	011 1010	0.9880	101 1010	1.2021	111 1010	1.4162
001 1011	0.7806	011 1011	0.9947	101 1011	1.2088	111 1011	1.4229
001 1100	0.7873	011 1100	1.0014	101 1100	1.2155	111 1100	1.4296
001 1101	0.7940	011 1101	1.0081	101 1101	1.2222	111 1101	1.4363
001 1110	0.8007	011 1110	1.0148	101 1110	1.2289	111 1110	1.4429
001 1111	0.8074	011 1111	1.0215	101 1111	1.2356	111 1111	1.4496

2. Reg01 SysCntlreg1

NAME	BITS	DESCRIPTION			
Switching Frequency	D[7:5]	D[7:5]	Switching Frequency	D[7:5]	Switching Frequency
		000	2.2MHz (Default)	100	1.25MHz
		001	2MHz	101	1.11MHz
		010	1.67MHz	110	1MHz
		011	--	111	--
Reserved	D4	Reserved			
Reserved	D3	Reserved			
PG_LOHI	D2	A “0” here sets “PGOOD” to sense only a negative voltage excursion of VO from the reference. A high (default) will set “PGOOD” to detect both a positive and negative excursion of VO from the reference			
VIN_OVP	D1	A “1” disables the VIN OVP function. Converter will continue to operate. A low will turn-off the converter when Vin reaches Vin Max.			
Mode	D0	A “0” enables PFM mode, a high disables PFM mode.			

3. Reg02 SysCntlreg2

NAME	BITS	DESCRIPTION			
Reserved	D[7:6]	Reserved			
Go	D5	Writing to this bit starts a Vout transition regardless of its initial value			
Output Discharge	D4	A “0” disables the Output discharge, the output voltage just be discharged by load. A high enables internal pull down.			
Reserved	D3	Reserved			
Slew Rate	D[2:0]	D[2:0]	SLEW RATE	D[2:0]	SLEW RATE
		000	64 mV/μs	100	4 mV/μs
		001	32 mV/μs	101	2 mV/μs
		010	16 mV/μs	110	1 mV/μs
		011	8 mV/μs	111	0.5 mV/μs

4. Reg03 ID1

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	VENDOR ID
Die ID	D[3:0]	IC Type

5. Reg04 ID2

NAME	BITS	DESCRIPTION
Reserved	D[7:4]	RESERVED
Die Rev	D[3:0]	Die revision

6. Reg05 Status

NAME	BITS	DESCRIPTION
ILIM	D7	When bit is high, IC is in current limit
UVLO	D6	When bit is high Vin is less than the UVLO threshold
OVP	D5	When bit is high Vin is greater than the OVP threshold
VoOV	D4	When bit is high a voltage higher than 110% of regulation voltage is presented.
VoUV	D3	When bit is high a voltage lower than 90% of regulation voltage is presented.
PGOOD	D2	When bit is high, the output is in regulation; otherwise the output voltage is out of +/- 10% regulation window.
OTW	D1	When junction temperature is higher than 130^{o}C, the bit is high, otherwise is low.
En stat	D0	When bit is high the SMPS is enabled, when bit is low the SMPS is disabled.

Operation Status

CONIDTION	PG	REGULATION	LATCH-OFF	STATUS BIT
VIN Overvoltage	LOW	OFF	NO	OVP
VIN Under Voltage	LOW	OFF	N/A	UVLO
Thermal Warning	LOW	ON	NO	OTW
Thermal Shut Down	LOW	OFF	YES	N/A
Current Limit	HIGH	ON	NO	ILIM
Output Under voltage	LOW	OFF	YES	VoUV
Output Over Voltage (>110% of target output)	LOW	ON	NO	VoOV

FUNTIONAL DIAGRAM

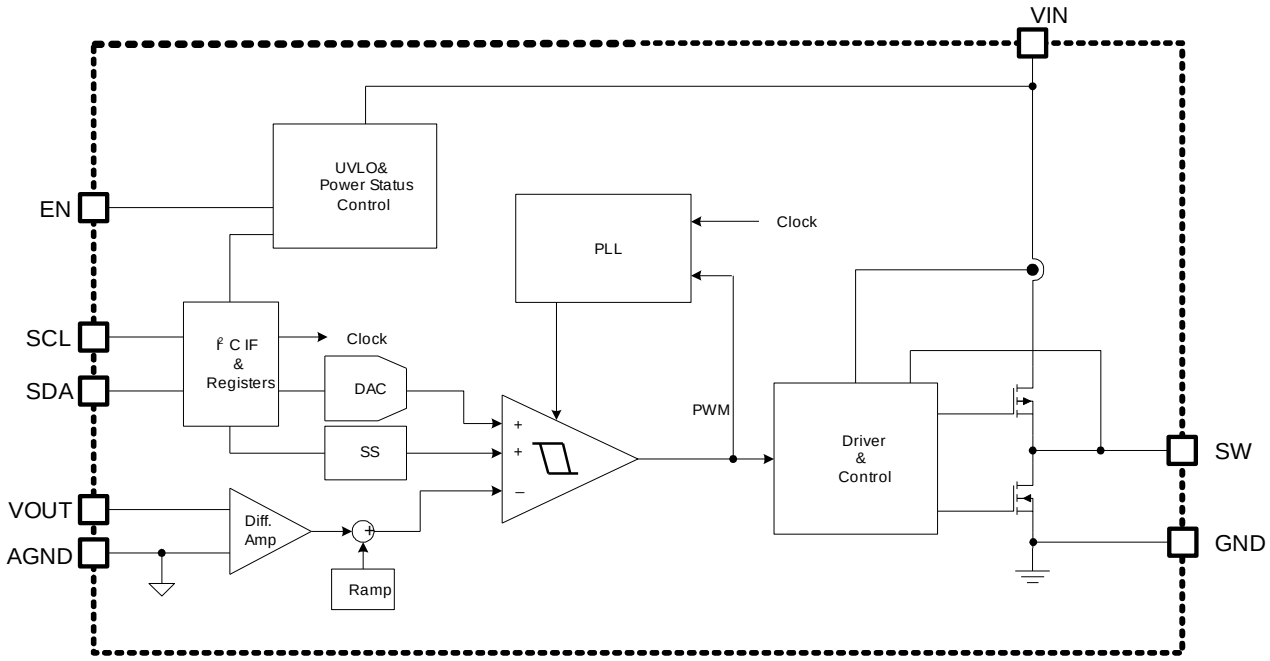


Figure 1—MP8845C Block Diagram

OPERATION

MP8845C is a low voltage 5A synchronous step-down converter with controllable I2C interface. It applies the MPS patented constant frequency hysteretic control to utilize the fast transient response of hysteretic control and keep the switching frequency to be constant. No compensation is needed which simplifies the design procedure.

MP8845C integrates an I2C compatible interface allowing transfers up to 3.4Mbps. This communication interface can be used for dynamic voltage scaling with voltage steps down to 6.69mV with the output voltage from 0.6V to 1.45V. The voltage transition slew rate can be controlled as well.

Fixed Frequency Hysteretic Control

Compare to fixed frequency PWM control, hysteretic control offers the advantage of simpler control loop and faster transient response. By using internal phase lock loop, MP8845C maintains a very good constant switching frequency across input and output voltage range.

To prevent inductor current run away during load transient, MP8845C fixes the minimum off time to be 100ns. However, this minimum off time limit will not affect operation of MP8845C in steady state in any way.

Light Load Operation

MP8845C can work in auto PFM mode or forced PWM mode with I2C control. In light load condition, MP8845C has an option to uses a proprietary control scheme to save power and improve efficiency. Instead of turning off the low side switch immediately when inductor current start to reverse, MP8845C gradually ramp down and regulates the low side switch current to a minimal level, thus avoids the ringing at switching node that always occurs in discontinuous conduction mode (DCM) operation.

Enable

When input voltage is greater than the under-voltage lockout threshold (UVLO), typically 2.45V, MP8845C can be enabled by pulling EN pin to higher than 1.8V. Pulling down to ground will disable MP8845C. Floating EN pin could also automatically keep device off.

Soft Start

MP8845C has built-in soft start that ramps up the output voltage in a controlled slew rate, avoiding start up inrush current and output voltage overshoot at startup. The soft start time is about 0.4ms.

Current Limit

MP8845C has a typical 9A current limit for the high side switch. When the high side switch hits current limit, MP8845C will expand the minimum off time till the current drops to 5.8A before the high side switch is turned on for the next switching cycle. This will prevent inductor current from continuing to build up which will result in damage of the components. If the load current continuous rise, it will pull down output voltage and trigger Vo under voltage protection. MP8845C will enter latch-off. Only re-cycle EN or Vin can revoke it.

Thermal Protection

MP8845C employs thermal shutdown by internally monitoring the junction temperature of the IC. If the junction temperature exceeds the thermal warning threshold which is around 130^{o}C, the OTW pin will be assert. If no action from the system responses, the junction temperature will keep rising until it exceeds the threshold of thermal shutdown (150^{o}C typically). After thermal shutdown, a new power start up cycle is needed to turn on MP8845C again.

I2C INTERFACE

MP8845C can communicate with core with I²C for smart design. MPS has a GUI control Interface is shown in figure 2. Its install process and usage can be found in another document "MP8845 Software Guide".

I²C Address

The I²C slave address of MP8845C is 0x38H / 0x39H internally. If need other slave address, please contact with factory.

Table 2—I²C Slave Address

Hex	A7	A6	A5	A4	A3	A2	A1	A0
W 0x38 **R 0x39**	0	0	1	1	1	0	0	R/W
Address	0x1C							

I²C Enable

Except MP8845C EN pin can start up and shutdown the convertor, the I²C Enable can also control the convertor. Reg00 VSEL D7 bit is I²C controlled enable. When writing D7=0, the convertor is off. When writing D7=1, the convertor is on. Both external EN and I2C EN can control the converter. Only when both EN is high, the converter works.

Output Voltage Select

MP8845C output voltage is I²C programmable. There is no need to set feedback resistors to get different output voltage. The default output voltage is 1.1V, but it can be set from 0.6V to 1.45V in 6.69mV Steps by I²C. The process of change output voltage is:

1. Write Go bit (Reg02 Syscntlreg2 [D5]) to 1. This action means output voltage can be set another value which is not default Vo voltage;
2. Write Output reference bit (Reg00 VSEL [D6 : D0]). The output voltage can be changed refer to Table 1. Output Voltage Chart.

Switching Frequency

The default switching frequency of MP8845C is 2.2MHz; however the frequency can also be changed based on the application. By writing Switching frequency bits (Reg01 SysCntlreg1 [D7:D5], switching frequency can be programmed for one of six possible value. Their corresponding data can be found in Table 1. Reg01.

PGOOD Configure

MP8845C has an option to uses PG_LOHI function. This function can be wrote Pglohi bit (Reg01 Syscntlreg1 [D2]). The default value is 1, "PGOOD" will sense both a positive and negative excursion of Vo from the reference. If writing this bit to 0, "PGOOD" only sense a negative voltage excursion of Vo from the reference.

Input Over Voltage Protection

MP8845C has an option to uses VIN_OVP function. This function can be wrote Vinovp bit (Reg01 Syscntlreg1 [D1]). The default value is 0, VIN OVP function is enabled. When Vin voltage is higher than 6.1V, the converter will be disabled. After Vin voltage recover to 5.8V, the converter will re-start. If Vinovp bit is set to 1, the Vin OVP will be disable. It will not stop converter even Vin voltage excess its safe range.

Forced CCM

The MP8845C has auto PFM mode and forced CCM. This function can be wrote Mode bit (Reg01 Syscntlreg1 [D0]). The default value is 0, auto PFM mode is selected. Consider smaller Vo ripple and regulation for full load range, forced CCM mode is recommended. Set this bit to 1 will disable the PFM mode.

Output Discharge

MP8845C has output discharge function. Write Out-dis bit (Reg02 SysCntlreg2 [D4]) can change the output discharge mode. The default value is 0 and just discharge the Vo by its load when EN is low. Writing D4=1 can enable the function, and then the output voltage can be discharged by internal pull down resistance.

Ouput Voltage Transition Slew Rate

When output voltage transits from a low to high voltage or from a high to low voltage, the transition slew rate can be different. There are eight possible values for selecting. Through writing the Slew rate bits (Reg02 Syscntlreg2 [D2:D0]), the transition slew rate can be set at one possible value based on the application. The internal reference will follow the set slew rate, but the output voltage slew rate is not always follow internal reference. Consider output capacitor and inductor, the actual output voltage slew rate should be a little slower.

I²C Register Hold On

MP8845C has special function that is I²C register hold on after EN pin change low. The updated register can be hold for later application condition even external EN pull low.

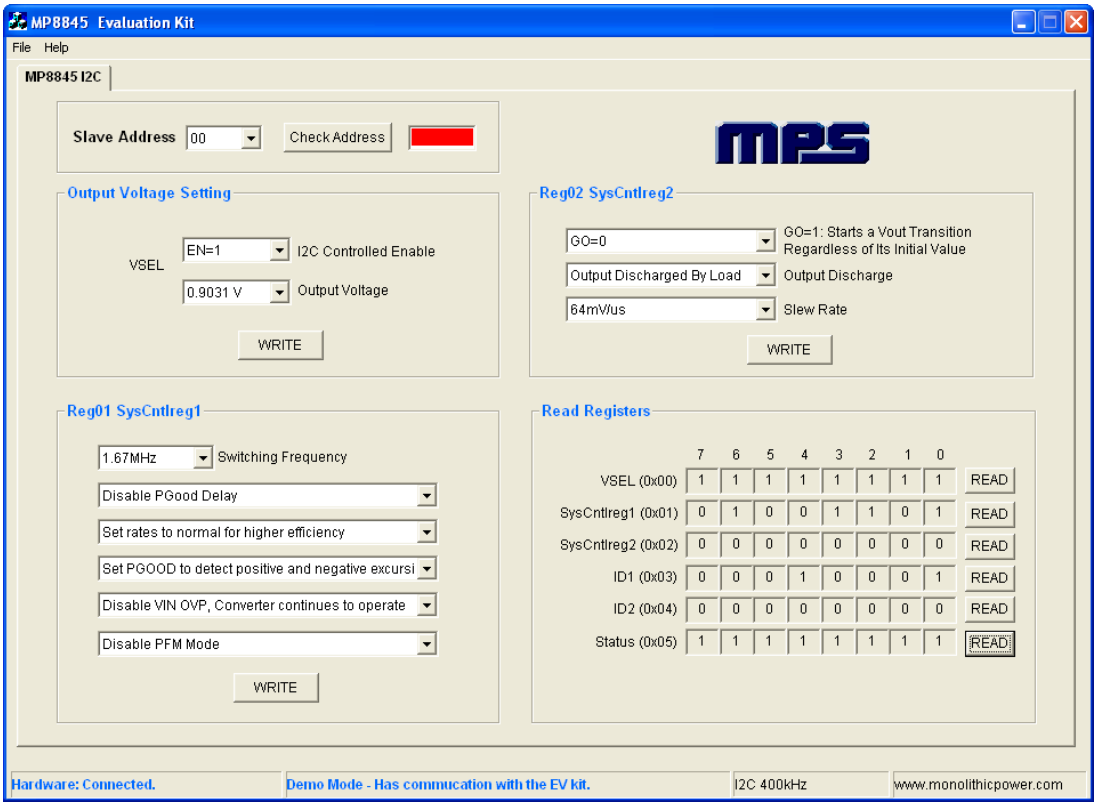


Figure 2—MP8845C control interface

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor is sufficient. For higher output voltage, 47µF may be needed for more stable system.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small and high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage.

Low ESR ceramic capacitors can be used with MP8845C to keep the output ripple low. Generally, 22µF output ceramic capacitor is enough for most of the cases. In higher output voltage condition, 47µF might be needed for a stable system. Larger output capacitor can get smaller output voltage ripple.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

Layout Recommendation of MP8845C

Proper layout of the switching power supplies is very important, and sometimes critical to make it work properly. Especially, for the high switching converter, if the layout is not carefully done, the regulator could show poor line or load regulation, stability issues.

For MP8845C, the high speed step-down regulator, the input capacitor should be placed as close as possible to the IC pins. As shown in Figure 6, the 0805 size ceramic capacitor is used, please make sure the two ends of the ceramic capacitor be directly connected to VIN pin and GND pin. A 0603 size decouple ceramic capacitor is strongly recommended here.

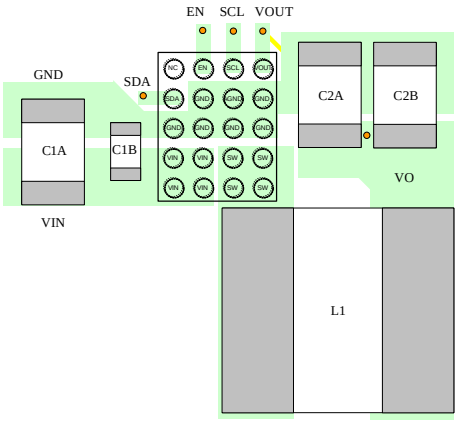


Figure 3—Recommend Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 3—Design Example

V_{IN}	5V
V_{OUT}	1.1V
I_{OUT}	5A

The detailed application schematic is shown in Figure 4. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS

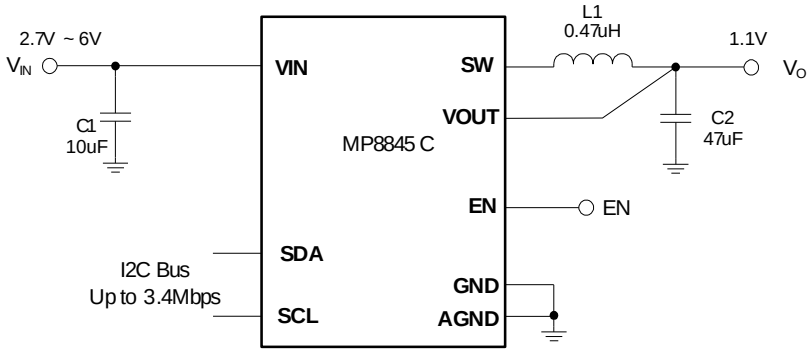
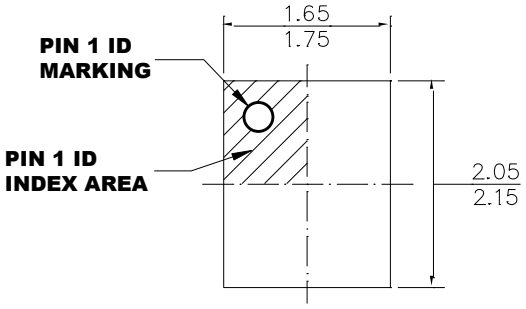


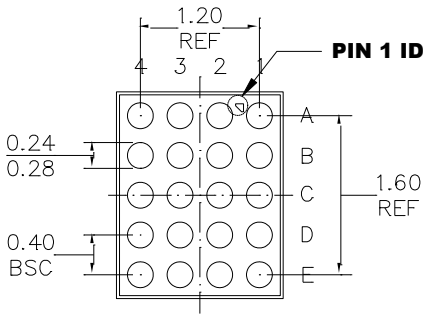
Figure 4—Application Circuit

PACKAGE INFORMATION

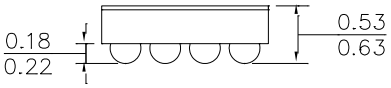
WLCSP-20 (1.70mmX2.10mm)



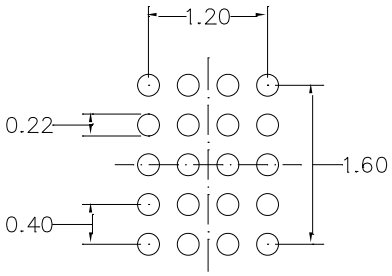
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) BALL COPLANARITY SHALL BE 0.05 MILLIMETER MAX.
3) JEDEC REFERENCE IS MO-211.
4) DRAWING IS NOT TO SCALE.