

## DESCRIPTION

The MP9148 is an internally-compensated, 1MHz fixed-frequency, dual PWM, synchronous, step-down regulator. The MP9148 operates from a 2.7V-to-6V input, generates an output voltage as low as 0.608V, and has a 45 $\mu$ A quiescent current that makes it ideal for powering portable equipment that runs on a single cell lithium-ion (Li+) battery.

The MP9148 integrates dual 100m $\Omega$  high-side switches and 40m $\Omega$  synchronous rectifiers for high efficiency without an external Schottky diode. Peak-current mode control and internal compensation limits the minimum number of readily-available external components.

Fault-condition protections include cycle-by-cycle current limiting and thermal shutdown.

The MP9148 is available in an 8-pin TSOT23-8 package.

## FEATURES

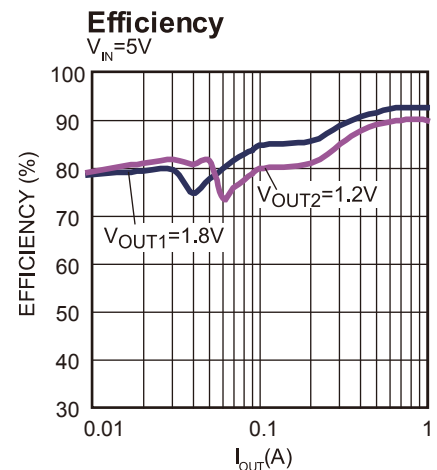
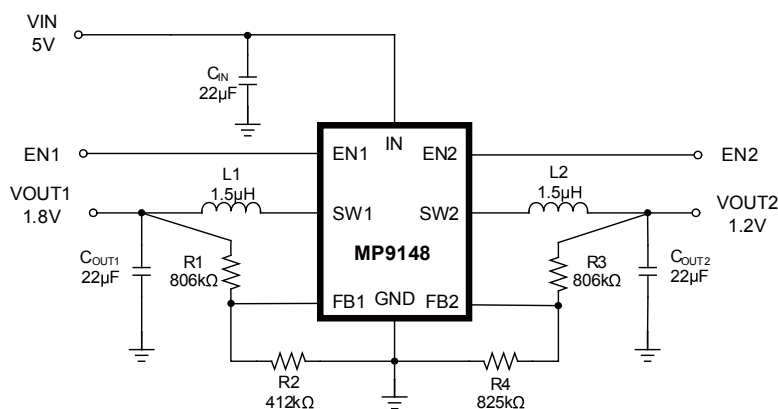
- Dual 1A-Output Current
- >93% Peak Efficiency
- >80% Light-Load Efficiency
- Wide 2.7V-to-6V Operating Input Range
- 100m $\Omega$  and 40m $\Omega$  Internal Power MOSFET
- 1MHz Fixed Switching Frequency
- Adjustable Output from 0.608V to VIN
- 180° Phase-Shifted Operation
- 100% Duty-Cycle Operation
- 45 $\mu$ A Quiescent Current
- Cycle-by-Cycle Over-Current Protection
- Short-Circuit Protection with Hiccup Mode
- Thermal Shutdown
- Available in an 8-pin TSOT23-8 Package

## APPLICATIONS

- Small/Handhold Devices
- DVD Drivers
- Portable Instruments
- Smartphones and Feature Phones
- Battery-Powered Devices

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## TYPICAL APPLICATION



### ORDERING INFORMATION

Part Number*	Package	Top Marking
MP9148GJ	TSOT23-8	See Below

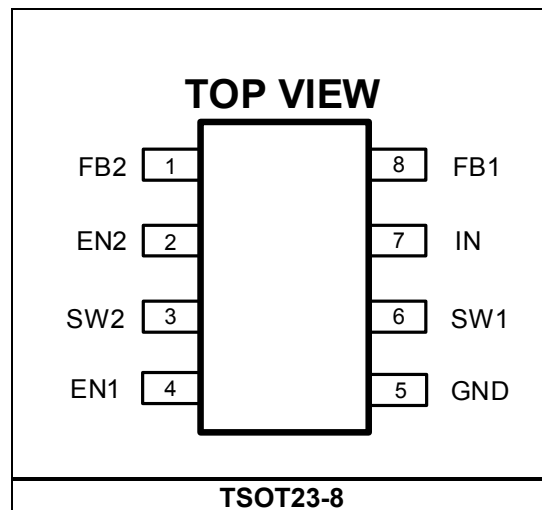
\* For Tape & Reel, add suffix -Z (e.g. MP9148GJ-Z);

### TOP MARKING

**| AKXY**

AKX: product code of MP9148GJ;  
Y: year code;

### PACKAGE REFERENCE



**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

Supply Voltage $V_{IN}$ .....	6.5V
$V_{SW}$ —0.3V (-3V for<10ns) to 6.5V (7.5V for<10ns)	
All Other Pins.....	-0.3V to +6.5 V
Junction Temperature.....	150°C
Lead Temperature.....	260°C
Continuous Power Dissipation ( $T_A = +25^\circ\text{C}$ ) <sup>(2)</sup>	
.....	1.25W

**Recommended Operating Conditions** <sup>(3)</sup>

Supply Voltage $V_{IN}$ .....	2.7V to 6V
Output Voltage $V_{OUT}$ .....	0.608V to 5.5V
Operating Junction Temp. ....	-40°C to +125°C

<b>Thermal Resistance</b> <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$
TSOT23-8 .....	100	55 °C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX)- $T_A$ )/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS <sup>(5)</sup>**
**V<sub>IN</sub> = V<sub>EN</sub> = 3.6V, T<sub>A</sub> = +25°C, unless otherwise noted.**

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Quiescent)	I <sub>Q</sub>	V <sub>IN</sub> =3.6V, V <sub>EN</sub> =2V, V <sub>FB</sub> = 0.65V	35	45	55	μA
Shutdown Current		V <sub>EN</sub> = 0V		0	1	μA
IN Under-Voltage Lockout Threshold		Rising edge	2.4	2.5	2.6	V
IN Under-Voltage Lockout Hysteresis				300		mV
Regulated FB Voltage	V <sub>FB</sub>	T <sub>A</sub> = +25°C	0.596	0.608	0.620	V
FB Input Current		V <sub>FB</sub> = 0.608V		±10	50	nA
EN, HIGH Threshold		-40°C ≤ T <sub>A</sub> ≤ +85°C	1.2			V
EN, LOW Threshold		-40°C ≤ T <sub>A</sub> ≤ +85°C			0.4	V
Internal Soft-Start Time	τ <sub>SS</sub>			0.5		ms
High-Side Switch, ON-Resistance	R <sub>DSON_P</sub>	V <sub>IN</sub> =5V		100		mΩ
Low-Side Switch, ON-Resistance	R <sub>DSON_N</sub>	V <sub>IN</sub> =5V		40		mΩ
SW Leakage Current		V <sub>EN</sub> = 0V; V <sub>IN</sub> = 6V V <sub>SW</sub> = 0V and 6V	-1	0	1	μA
High-Side Switch, Current Limit		Sourcing, D=40%		2.5		A
Oscillator Frequency		Both channels work in CCM	0.8	1	1.2	MHz
Phase Shift				180		degree
Minimum ON Time <sup>(6)</sup>	τ <sub>ON_MIN</sub>			90		ns
Minimum OFF Time	τ <sub>OFF_MIN</sub>			100		ns
Maximum Duty Cycle				100		%
Thermal Shutdown Threshold <sup>(6)</sup>		Hysteresis = 30°C		160		°C

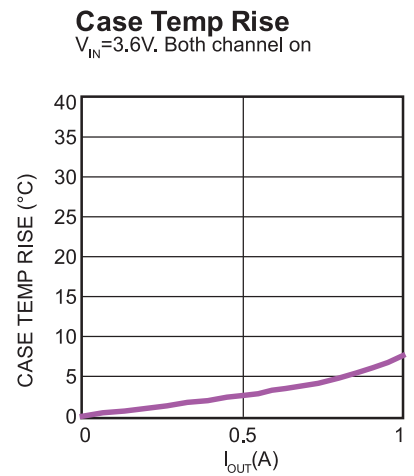
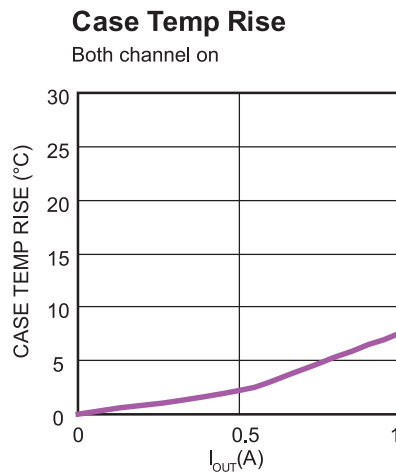
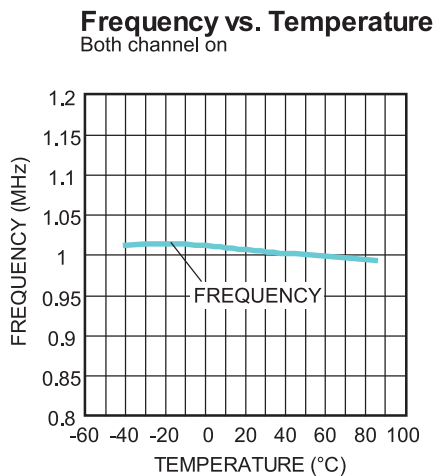
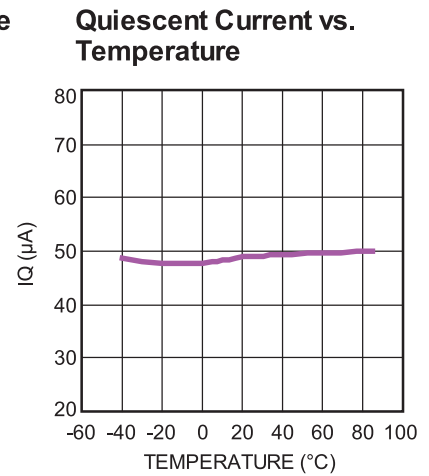
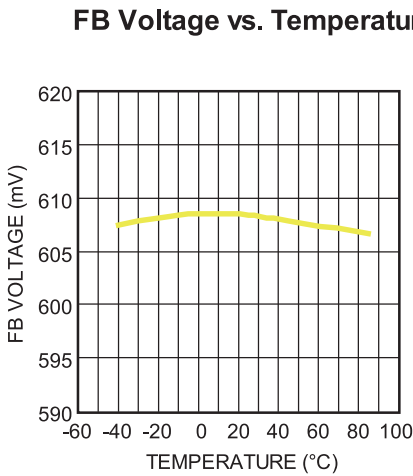
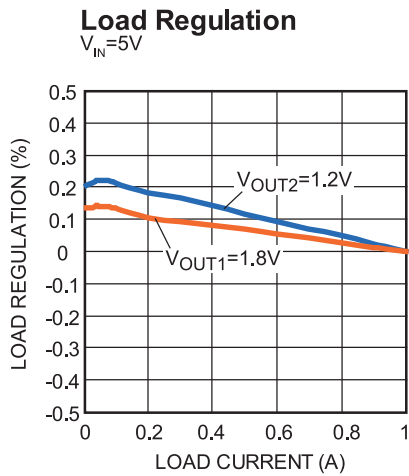
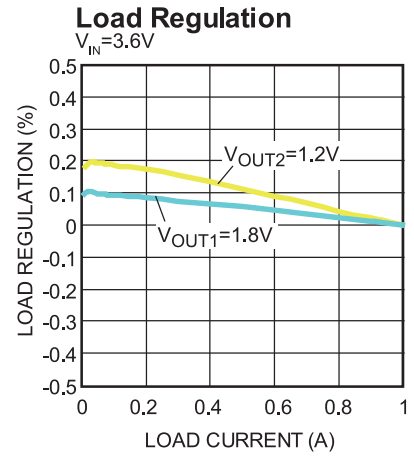
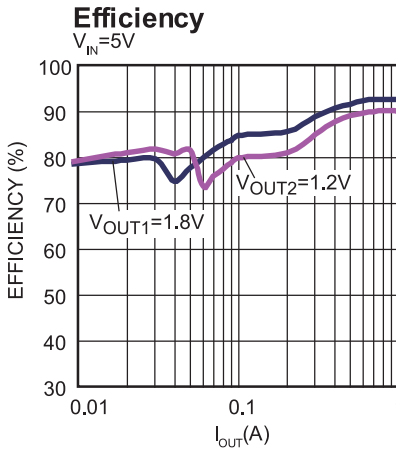
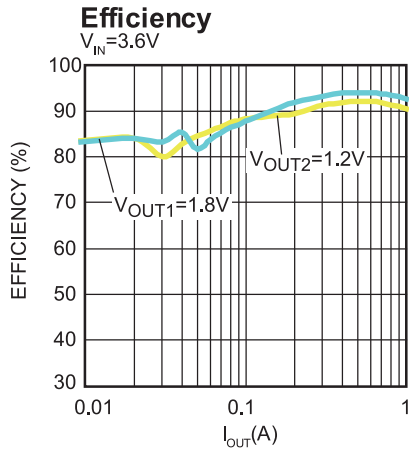
**Notes:**

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

6) Guarantee by design

## TYPICAL PERFORMANCE CHARACTERISTICS

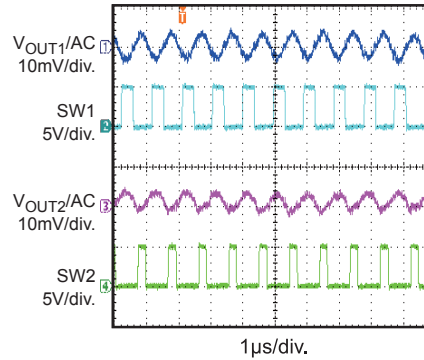
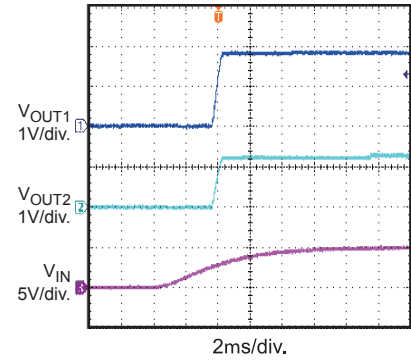
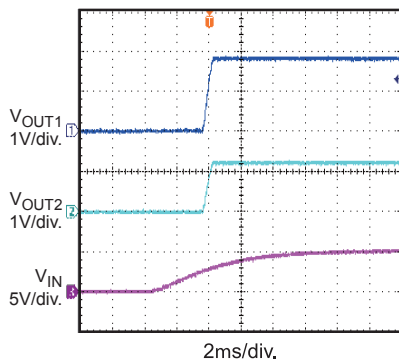
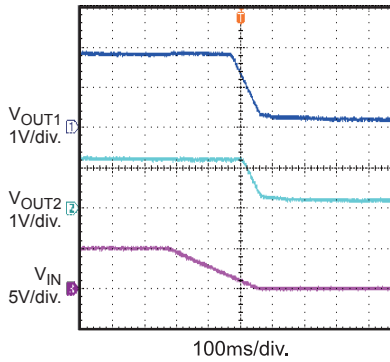
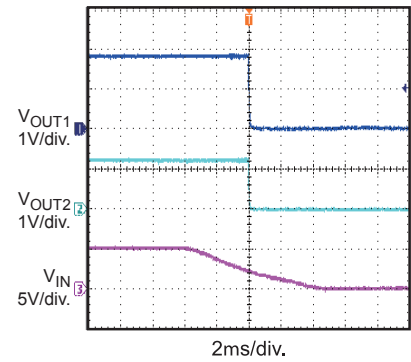
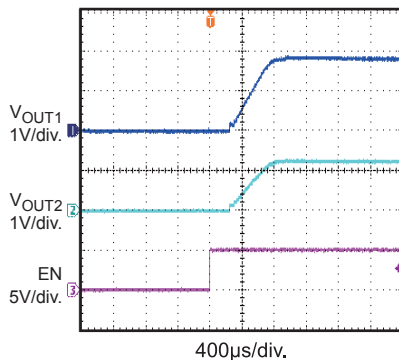
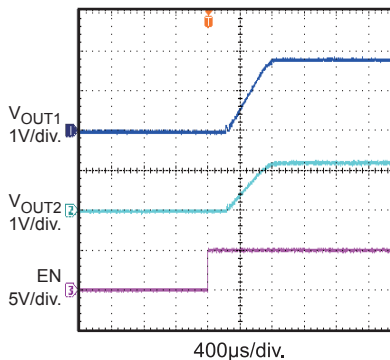
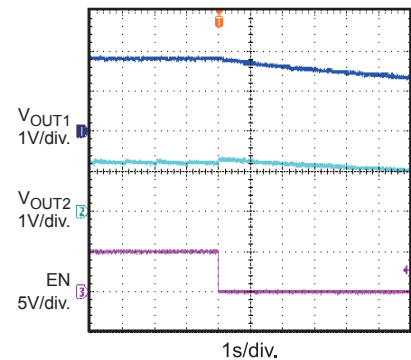
$V_{IN} = 5V$ ,  $V_{OUT1} = 1.8V$ ,  $V_{OUT2} = 1.2V$ ,  $L = 1.5\mu H$ ,  $C_{OUT1}=C_{OUT2}=22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

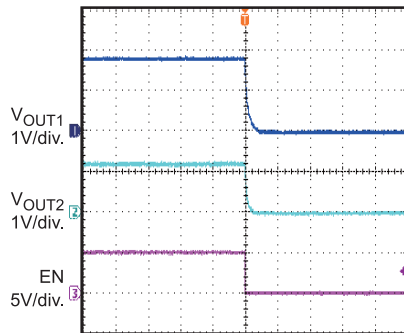
$V_{IN} = 5V$ ,  $V_{OUT1} = 1.8V$ ,  $V_{OUT2} = 1.2V$ ,  $L = 1.5\mu H$ ,  $C_{OUT1}=C_{OUT2}=22\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

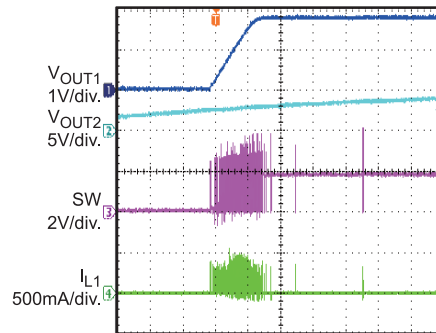
**Output Ripple**
 $I_{OUT1} = I_{OUT2} = 0A$ 

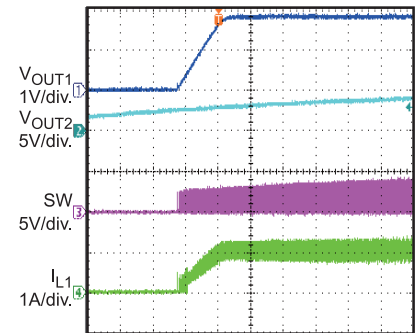
**Output Ripple**
 $I_{OUT1} = I_{OUT2} = 1A$ 

**Vin Power Up without Load**
 $I_{OUT1} = I_{OUT2} = 0A$ 

**Vin Power Up with Load**
 $I_{OUT1} = I_{OUT2} = 1A$ 

**Vin Power Down without Load**
 $I_{OUT1} = I_{OUT2} = 0A$ 

**Vin Power Down with Load**
 $I_{OUT1} = I_{OUT2} = 1A$ 

**EN On without Load**
 $I_{OUT1} = I_{OUT2} = 0A$ 

**EN On with Load**
 $I_{OUT1} = I_{OUT2} = 1A$ 

**EN Down without Load**
 $I_{OUT1} = I_{OUT2} = 0A$ 


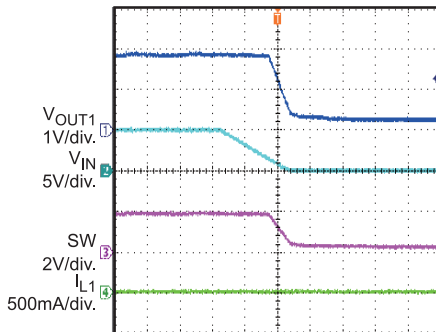
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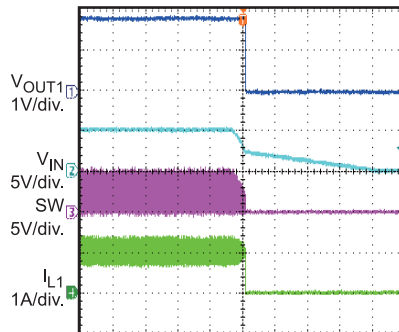
**EN Down with Load**
 $I_{OUT1} = I_{OUT2} = 1A$ 

 400 $\mu s$ /div.

**Vin Power On without Load**
 $I_{OUT1} = I_{OUT2} = 0A$ 

 400 $\mu s$ /div.

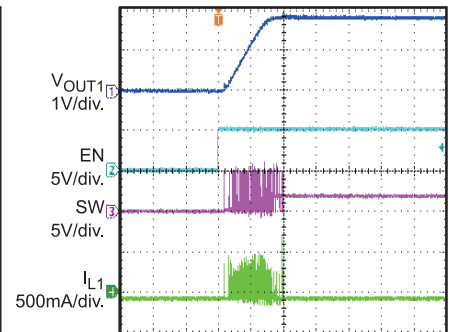
**Vin Power On**
 $I_{OUT1} = 1A$ ,  $I_{OUT2} = 0A$ 

 400 $\mu s$ /div.

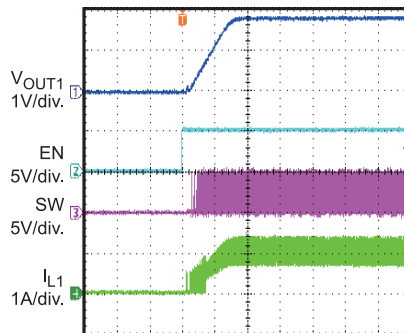
**Vin Power Down**
 $I_{OUT1} = I_{OUT2} = 0A$ 


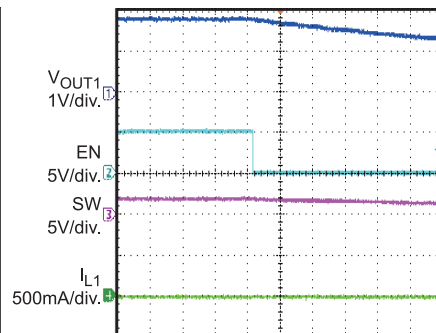
40ms/div.

**Vin Power Down**
 $I_{OUT1} = 1A$ ,  $I_{OUT2} = 0A$ 


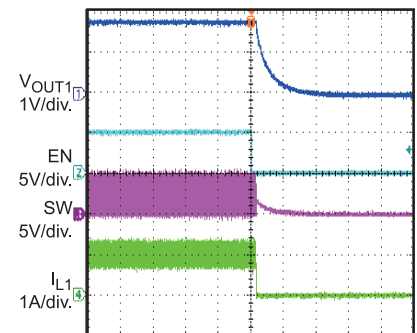
10ms/div.

**Enable On**
 $I_{OUT1} = I_{OUT2} = 0A$ 

 400 $\mu s$ /div.

**Enable On**
 $I_{OUT1} = 1A$ ,  $I_{OUT2} = 0A$ 

 400 $\mu s$ /div.

**Enable Down**
 $I_{OUT1} = I_{OUT2} = 0A$ 


1s/div.

**Enable Down**
 $I_{OUT1} = 1A$ ,  $I_{OUT2} = 0A$ 

 100 $\mu s$ /div.

## PIN FUNCTIONS

Package Pin #	Name	Description
1	FB2	Feedback 2. Error amplifier input. Connect to the tap of an external resistor divider between the output and GND. Sets the regulation voltage.
2	EN2	Channel 2 Enable. Buck.
3	SW2	Switch Node Connects to the channel 2 internal high-side and low-side power MOSFETs. Connects to the inductor.
4	EN1	Channel 1 Enable. Buck.
5	GND	Ground.
6	SW1	Switch Node Connects to the channel 1 internal high-side and low-side power MOSFETs. Connects to the inductor.
7	IN	Input Supply. Requires a decoupling capacitor to ground to reduce switching spikes.
8	FB1	Feedback 1. Error amplifier input. Connect to the tap of an external resistor divider between the output and GND. Sets the regulation voltage.



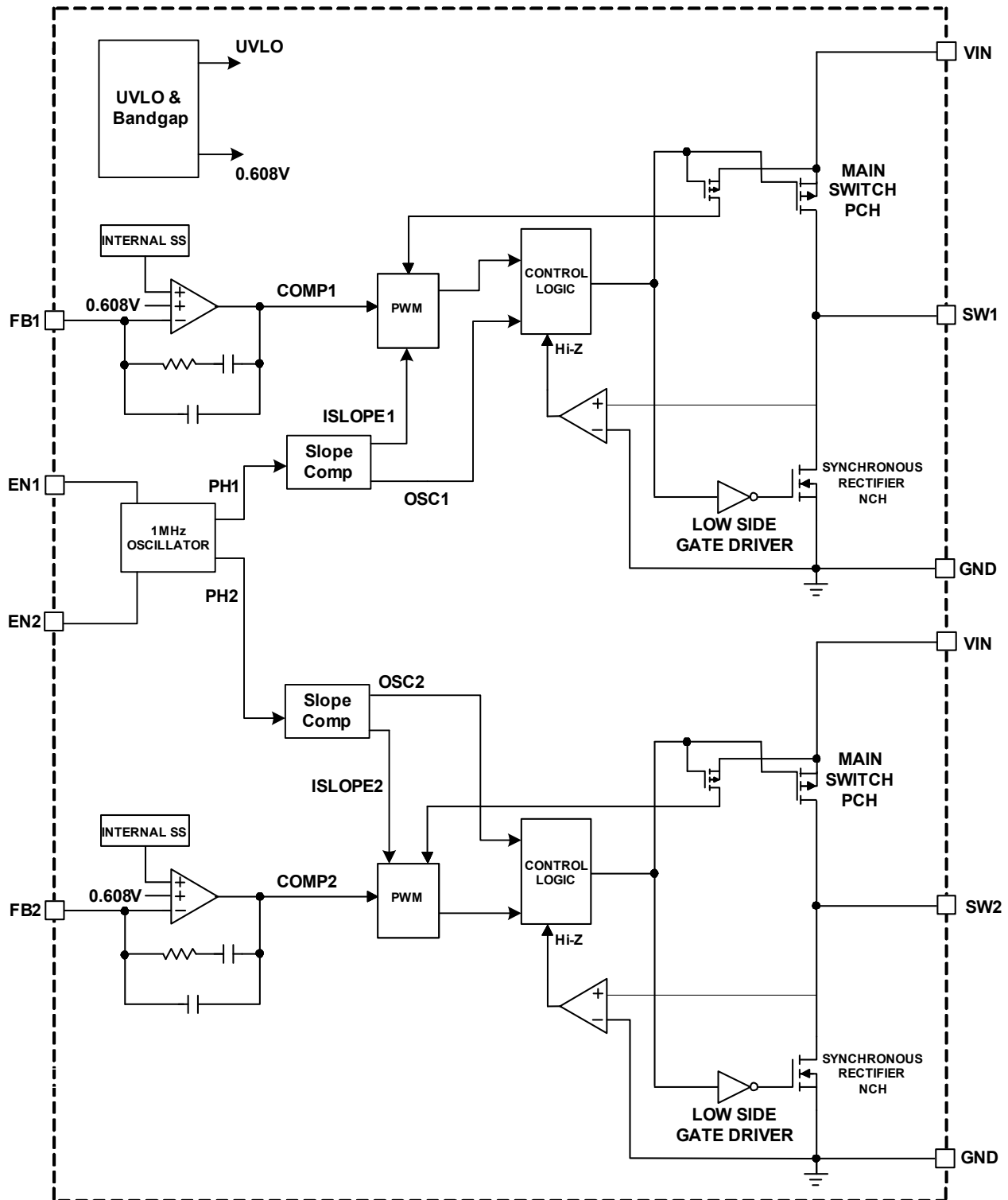


Figure 1: Functional Block Diagram

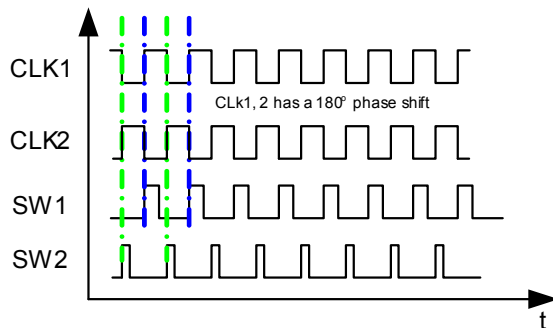
## OPERATION

MP9148 is a fully-integrated, dual-channel, synchronous, step-down converter. Both channels have peak-current modes with internal compensation for faster transient responses and cycle-by-cycle current limits.

MP9148 is optimized for low-voltage, portable applications where efficiency and small size are critical.

### 180° Phase-Shift

By default, the MP9148's two channels operate at a 180° phase-shift to reduce input current ripple: The smaller current ripple allows for a smaller input bypass capacitor. In CCM, two internal clocks control the switching: The high-side MOSFET turns on at the corresponding CLK's rising edge.



**Figure 2: Clock/Switching Timing**

However, the switching frequency for each channel falls when operating at low dropout, so the MP9148 operates at a default switching frequency of 1MHz with a fixed OFF time. After the input voltage recovers, switching for PWM mode resumes normally and synchronizes with the master oscillator for phase-shifted operation.

### Light-Load Operation

In light loads, the MP9148 uses a proprietary control scheme to save power and improve efficiency. The MP9148 will turn off the low side switch when inductor current starts to reverse. Then MP9148 works in discontinuous conduction mode (DCM) operation.

When either channel enters DCM or low-dropout operation, this channel will not be controlled by the internal 1MHz oscillator.

	Condition		Mode	
	CH1	CH2	CH1	CH2
1	Heavy Load		1MHz CCM	1MHz CCM, 0° Phase
2	Light Load		DCM	DCM
3	Low Dropout		Fixed OFF Time	Fixed OFF Time
4	Heavy Load	Light Load	0.95MHz CCM	DCM
5	Light Load	Heavy Load	DCM	0.95MHz CCM
6	Heavy Load	Low Dropout	0.95MHz CCM	Fixed OFF Time
7	Low Dropout	Heavy Load	Fixed OFF Time	0.95MHz CCM
8	Light Load	Low Dropout	DCM	Fixed OFF Time
9	Low Dropout	Light Load	Fixed OFF Time	DCM

### Soft Start

MP9148 has a built-in soft start that ramps up the output voltage at a controlled slew rate to start-up overshoot. The soft-start time is ~0.5ms.

### Current Limit and Short-Circuit Recovery

Each channel's high-side switch has a 2.5A (typ.) current limit. The MP9148 treats any current-limit condition that remains for 400us as a short and enter hiccup mode.

The MP9148 disables its output power stage in hiccup mode, and then slowly discharges the soft-start capacitor before initiating soft-start. If the short-circuit condition remains, the MP9148 repeats this operation till the short circuit disappears and output returns to the regulation level.

## APPLICATION INFORMATION

### COMPONENT SELECTION

#### Output Voltage

External resistor dividers connected to the FB pins set the output voltages. The feedback resistor connected to FB1 (R1) also sets the feedback loop bandwidth ( $f_c$ ).

$f_c$  does not exceed  $0.1 \times f_{sw}$ . When using a ceramic output capacitor ( $C_o$ ), set the range to 50kHz and 100kHz for optimal transient performance and good phase margin. When using an electrolytic capacitor, set the loop bandwidth no higher than 1/4 the ESR zero frequency ( $f_{ESR}$ ).  $f_{ESR}$  is:

$$f_{ESR} = \frac{1}{2\pi \cdot R_{ESR} \cdot C_o}$$

We suggest using a 600k to 800k resistor for R1 when  $C_o=22\mu F$ . R2 is then:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.608V} - 1}$$

**Table 1: Resistor Values vs. Output Voltage**

V <sub>OUT</sub>	R1	R2	L	C <sub>OUT</sub> (Ceramic)
1.2V	806kΩ	825kΩ	0.47μH-2.2μH	22μF
1.5V	806kΩ	549kΩ	0.47μH-2.2μH	22μF
1.8V	806kΩ	412kΩ	0.47μH-2.2μH	22μF
2.5V	806kΩ	261kΩ	1μH-4.7μH	22μF
3.3V	806kΩ	182kΩ	1μH-4.7μH	22μF

#### Inductor Selection

Use a 0.47μH-to-2.2μH inductor with a DC current rating of at least 1.25 times the maximum load current for most applications. For best efficiency, select an inductor with a DC resistance <20mΩ. See Table 2 for recommended inductors. For most designs, estimate the inductance value using the following equation:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{OSC}}$$

Where  $\Delta I_L$  is the inductor ripple current. Select an inductor ripple current equal to approximately 30% of the maximum load current, 1A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

**Table 2: Suggested Surface-Mount Inductors**

Vendor	Part Number	L (μH)	DCR (mΩ)	SC (A)	L x W x H (mm <sup>3</sup> )
<b>WURTH</b>					
	744777002	2.2	13	6	7.3×7.3×4.5
	744310200	2	14.2	6.5	7×6.9×3
<b>TDK</b>					
	RLF7030T-1R5N6R1-T	1.5	8	6.5	7.8×6.8×3.2

#### Input Capacitor

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. Select an input capacitor with a switching-frequency impedance that is less than the input source impedance to prevent high-frequency-switching current from passing to the input source. Use low-ESR ceramic capacitors with X5R or X7R dielectrics with small temperature coefficients. For most applications, a 22μF capacitor is sufficient.

#### Output Capacitor

The output capacitor limits the output voltage ripple and ensures a stable regulation loop. Select an output capacitor with low impedance at the switching frequency. Use ceramic capacitors with X5R or X7R dielectrics. Using an electrolytic capacitor may result in additional output voltage ripple, thermal issues, and requires additional care in selecting the feedback resistor (R1) due to the large ESR. The output ripple ( $\Delta V_{OUT}$ ) is approximately:

$$\Delta V_{OUT} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \cdot \left( ESR + \frac{1}{8 \cdot f_{OSC} \cdot C_o} \right)$$

#### Power Dissipation

IC power dissipation plays an important role in circuit design—not only because of efficiency concerns, but also because of the chip's thermal requirements. Several parameters influence power dissipation, such as:

- Conduction Loss (Cond)
- Dead Time (DT)

- Switching Loss (SW)
- MOSFET Driver Current (DR)
- Supply Current (S)

Based on these parameters, we can estimate the power loss as:

$$P_{LOSS} = P_{Cond} + P_{DT} + P_{SW} + P_{DR} + P_S$$

### Thermal Regulation

As previously discussed, changes in IC temperature change the electrical characteristics, especially when the temperature exceeds the IC's recommended operating range. Managing the IC's temperature requires additional considerations to ensure that the IC runs below the maximum-allowable temperature. While operating the IC within recommended electrical limits is a major component to maintaining proper thermal regulation, specific layout designs can improve the thermal profile while limiting costs to either efficiency or operating range.

For the MP9148, connect the ground pin on the package to a GND plane on top of the PCB to use this plane as a heat sink. Connect this GND plane to GND planes beneath the IC using vias to further improve heat dissipation. However, given that these GND planes can introduce unwanted EMI noise and occupy valuable PCB space, design the size and shape of these planes to match the thermal resistance requirement:

$$\theta_{SA} = \theta_{JA} - \theta_{JC}$$

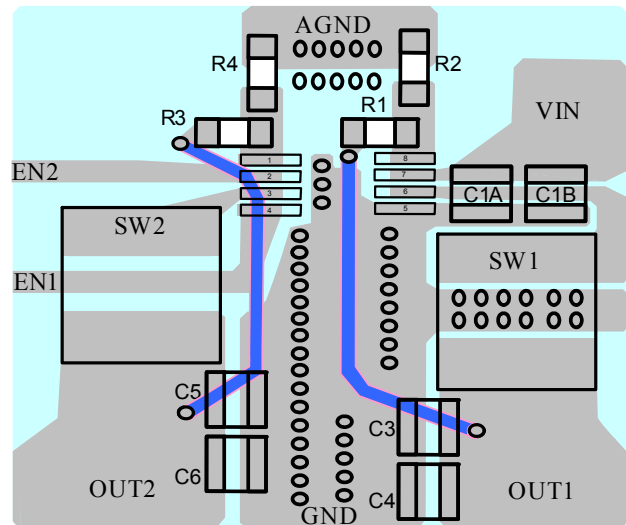
However, connecting the GND pin to a heat sink can not guarantee that the IC will not exceed its recommended temperature limits; for instance, if the ambient temperature exceeds the IC's temperature limits. If the ambient air temperature approaches the IC's temperature limit, options such as derating the IC so it operates using less power can help prevent thermal damage and unwanted electrical characteristics.

### PCB Layout

Proper layout of the switching power supplies is very important, and sometimes critical for proper function: poor layout design can result in poor line or load regulation and stability issues.

Place the high-current paths (GND, IN and SW) very close to the device with short, direct, and wide traces. Place the input capacitor as close as possible to the IN and GND pins. Place the

external feedback resistors next to the FB pin. Keep the switching node SW short and away from the feedback network. The circuit of below PCB layout is shown in Figure 4.



**Figure 3: Suggested PCB Layout**

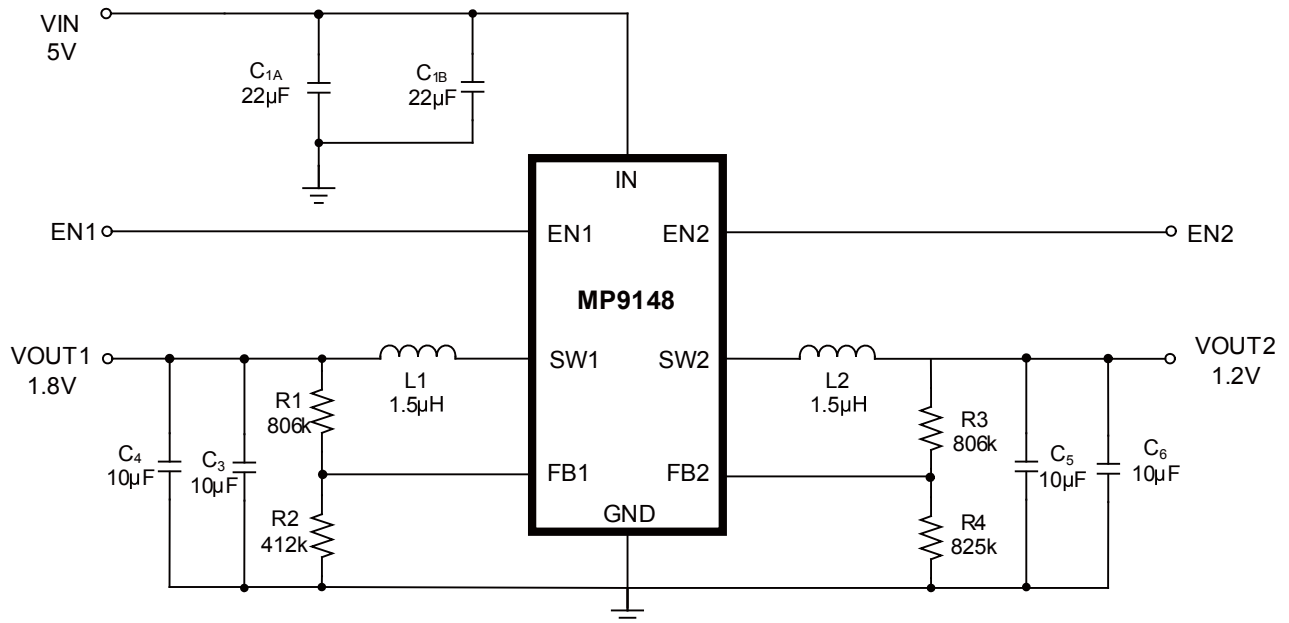
### Design Example

Below is a design example following the application guidelines for the specifications:

**Table 3: Design Example**

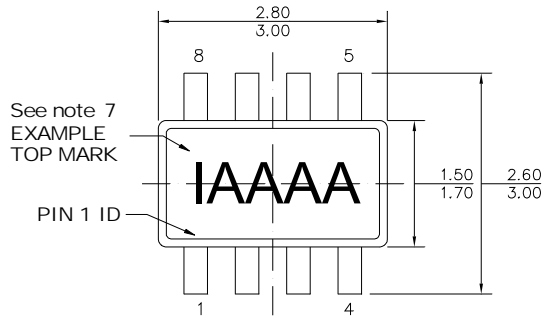
<b>VIN</b>	5V
<b>VOUT1</b>	1.8V
<b>VOUT2</b>	1.2V

The detailed application schematic is shown in Figure 1. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

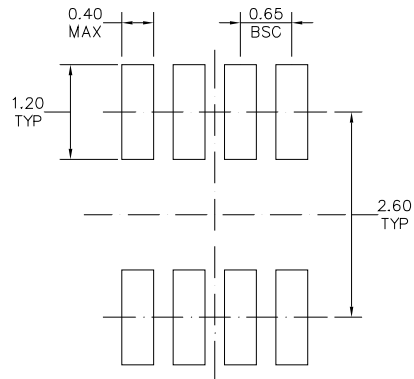
**TYPICAL APPLICATION CIRCUITS**

**Figure 4: Typical Application Circuit**

# PACKAGE INFORMATION

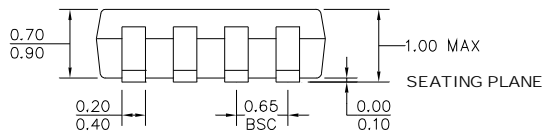
## TSOT23-8



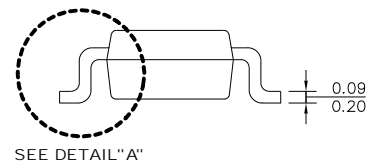
TOP VIEW



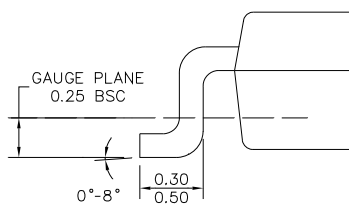
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO193, VARIATION BA
- 6) DRAWING IS NOT TO SCALE
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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