



The Future of Analog IC Technology®

MPQ2172

5.5V, 2A, 2.6MHz,
Synchronous, Step-Down Switcher
AEC-Q100 Qualified

DESCRIPTION

The MPQ2172 is a monolithic, step-down, switch-mode converter with integrated, internal, power MOSFETs. The MPQ2172 can achieve up to 2A of continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Full protection features include cycle-by-cycle current limiting and thermal shutdown.

The MPQ2172 is ideal for a wide range of applications, including automotive infotainment, clusters, telematics, and portable instruments.

The MPQ2172 requires only a minimal number of readily available, standard, external components and is available in a small TSOT23-8 package.

FEATURES

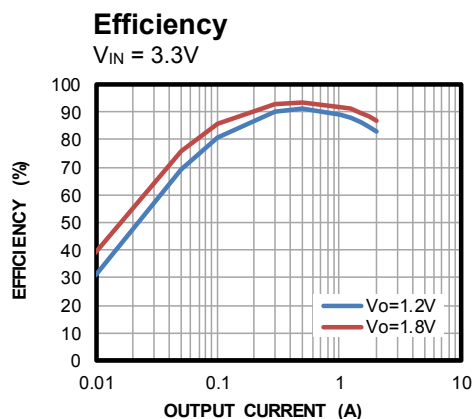
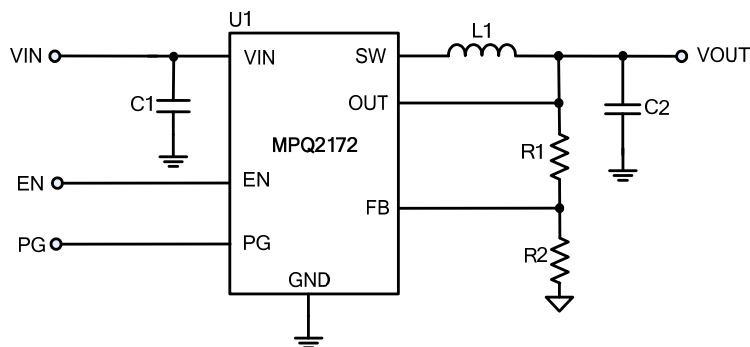
- Wide 2.5V to 5.5V Operating Input Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Up to 2A Output Current
- 80mΩ and 45mΩ Internal Power MOSFET Switches
- Default 2.6MHz Switching Frequency with 3.3V Input and 1.8V Output
- EN and Power Good for Power Sequencing
- Cycle-by-Cycle Over-Current Protection (OCP)
- Auto Discharge at Power-Off
- Short-Circuit Protection (SCP) with Hiccup Mode
- Stable with Low ESR Output Ceramic Capacitors
- Available in a TSOT23-8 Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Automotive Infotainment
- Automotive Clusters
- Automotive Telematics
- Low-Voltage I/O System Power
- Handheld/Battery-Powered Systems

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TYPICAL APPLICATION



ELECTRICAL CHARACTERISTICS

$V_{IN} = 5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted, typical values are at $T_J = +25^{\circ}C$.

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|--|---------------|---|------|------|------|------------|
| Quiescent current | I_Q | $V_{IN} = 5V$, $V_{EN} = 2V$, $V_{FB} = 0.63V$, no switching | | 520 | 720 | μA |
| Supply current (shutdown) | | $V_{EN} = 0V$ | | 0.1 | 35 | μA |
| Feedback voltage | V_{FB} | $T_J = +25^{\circ}C$ | 591 | 600 | 609 | mV |
| | | $T_J = -40^{\circ}C$ to $+125^{\circ}C$ | 588 | 600 | 612 | |
| Feedback current | I_{FB} | $V_{FB} = 0.63V$ | | 10 | 100 | nA |
| P-FET switch on resistance | R_{DSON_P} | | | 80 | 120 | m Ω |
| N-FET switch on resistance | R_{DSON_N} | | | 45 | 75 | m Ω |
| Switch leakage | | $V_{EN} = 0V$, $V_{IN} = 5V$, $V_{SW} = 0V$ and $5V$, $T_J = +25^{\circ}C$ | | 0.1 | 2 | μA |
| | | $V_{EN} = 0V$, $V_{IN} = 5V$, $V_{SW} = 0V$ and $5V$, $T_J = -40^{\circ}C$ to $+125^{\circ}C$ | | 0.1 | 35 | |
| P-FET current limit | | $T_J = +25^{\circ}C$ | 3.4 | 4.5 | 6 | A |
| On time | t_{ON} | $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$ | 135 | 150 | 180 | ns |
| | | $V_{IN} = 3.3V$, $V_{OUT} = 1.8V$ | 190 | 210 | 270 | |
| | | $V_{IN} = 5V$, $V_{OUT} = 1.2V$ | 95 | 110 | 130 | |
| | | $V_{IN} = 5V$, $V_{OUT} = 1.8V$ | 130 | 150 | 190 | |
| Switching frequency | f_s | $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$ | 1850 | 2400 | 2700 | kHz |
| | | $V_{IN} = 3.3V$, $V_{OUT} = 1.8V$ | 2000 | 2600 | 2800 | |
| | | $V_{IN} = 5V$, $V_{OUT} = 1.2V$ | 1850 | 2200 | 2500 | |
| | | $V_{IN} = 5V$, $V_{OUT} = 1.8V$ | 1850 | 2380 | 2700 | |
| Minimum off time | $t_{MIN-OFF}$ | $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$ | | 60 | 90 | ns |
| | | $V_{IN} = 3.3V$, $V_{OUT} = 1.8V$ | | | | |
| | | $V_{IN} = 5V$, $V_{OUT} = 1.2V$ | | 30 | 50 | ns |
| | | $V_{IN} = 5V$, $V_{OUT} = 1.8V$ | | | | |
| Soft-start time ⁽⁵⁾ | t_{SS-ON} | $V_{IN} = 3.6V$, $V_{OUT} = 1.5V$, 10% to 90% | 0.6 | 1.3 | 2.2 | ms |
| Soft-stop time ⁽⁵⁾ | t_{SS-OFF} | $V_{IN} = 3.6V$, $V_{OUT} = 1.5V$, 90% to 10% | 0.4 | 0.9 | 1.6 | ms |
| Power good upper trip threshold rising | PG_{H-R} | FB rising when PG turns to high voltage | 110 | 115 | 120 | % |
| Power good upper trip threshold falling | PG_{H-F} | FB falling when PG turns to high voltage | 105 | 110 | 115 | % |
| Power good upper trip hysteresis | PG_{H-Hys} | | | 5 | | % |
| Power good lower trip threshold rising | PG_{L-R} | FB rising when PG turns to high voltage | 85 | 90 | 95 | % |
| Power good lower trip threshold falling | PG_{L-F} | FB falling when PG turns to high voltage | 80 | 85 | 90 | % |
| Power good lower trip hysteresis | PG_{L-Hys} | | | 5 | | % |

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 5V, T_J = -40°C to +125°C, unless otherwise noted, typical values are at T_J = +25°C.

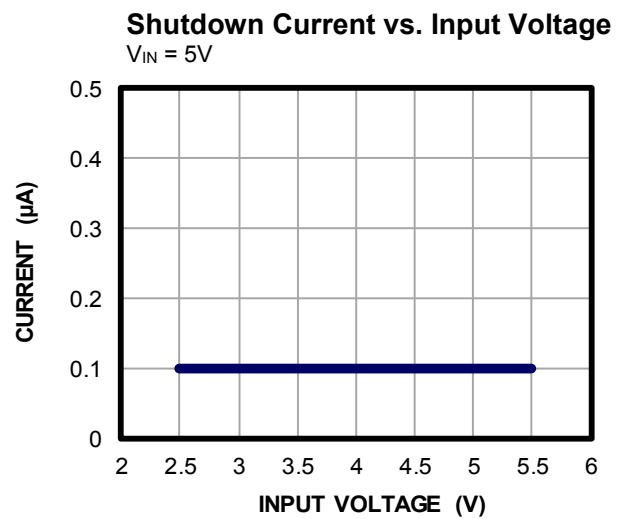
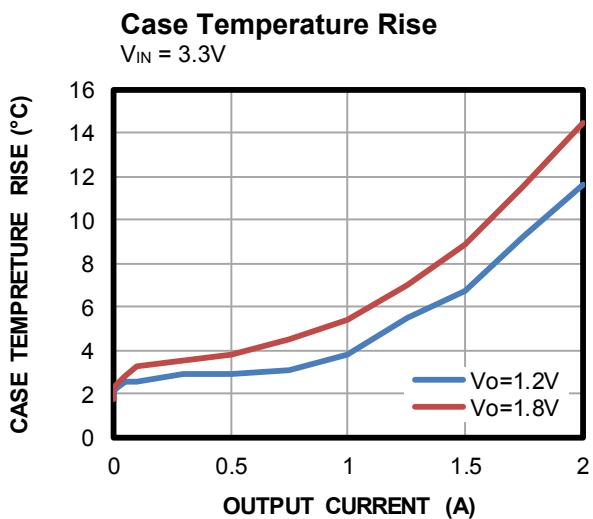
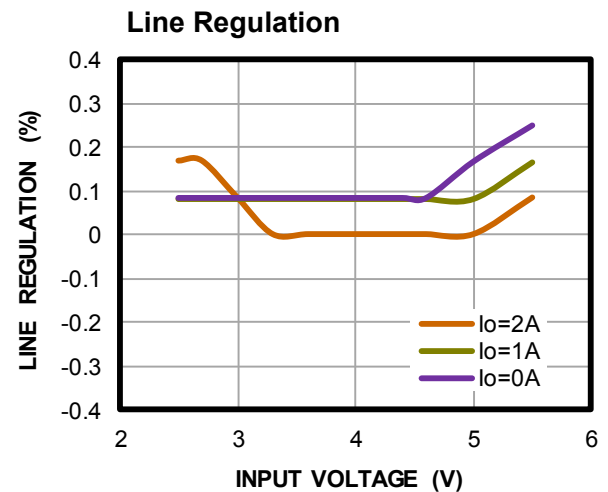
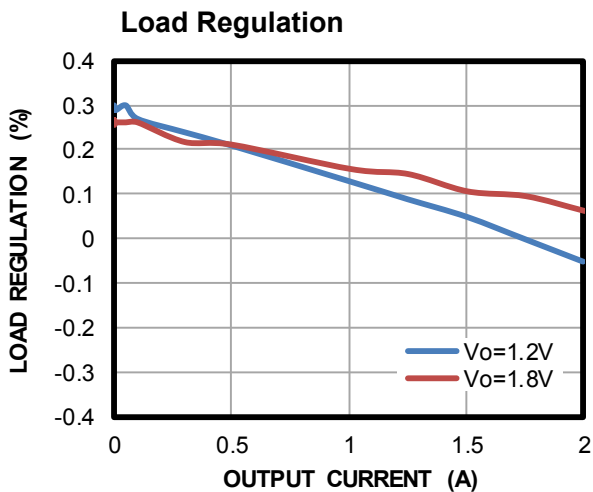
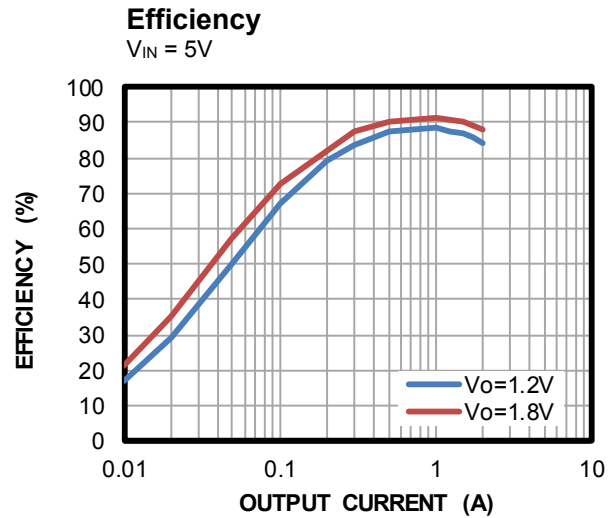
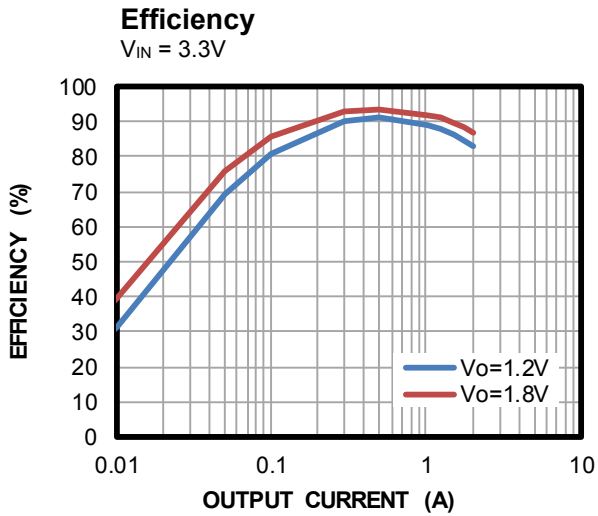
| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|--|-------------------|--|------|-----|-----|-------|
| Power good delay | P _{GD} | | 30 | 110 | 200 | μs |
| Power good sink current capability | V _{PG-L} | Sink 1mA | | 250 | 400 | mV |
| Power good logic high voltage | V _{PG-H} | V _{IN} = 5V, V _{FB} = 0.6V | 4.85 | | | V |
| Power good internal pull-up resistor | R _{PG} | | 200 | 500 | 800 | kΩ |
| Under-voltage lockout threshold rising | | | 2.0 | 2.2 | 2.4 | V |
| Under-voltage lockout threshold hysteresis | | | | 150 | | mV |
| EN input logic low voltage | | | | | 0.4 | V |
| EN input logic high voltage | | | 1.2 | | | V |
| EN input current | | V _{EN} = 0V | | 0.1 | 0.2 | μA |
| | | V _{EN} = 2V | | 2 | 4 | μA |
| Thermal shutdown ⁽⁵⁾ | | | | 170 | | °C |
| Thermal hysteresis ⁽⁵⁾ | | | | 30 | | °C |

NOTE:

5) Not tested in production. Guaranteed by design and characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

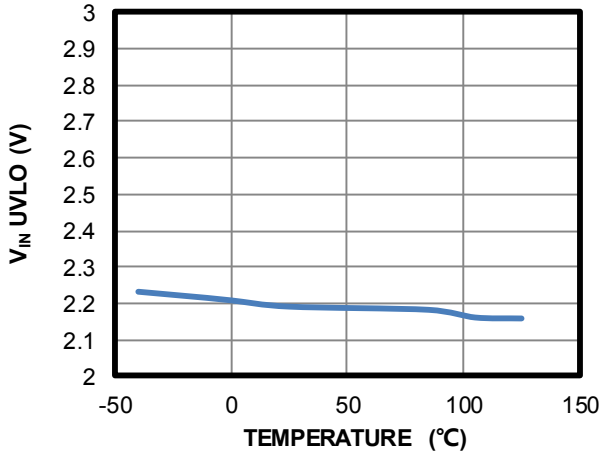
$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $L = 1\mu H$, $C_{OUT} = 22\mu F$, $T_A = +25^\circ C$, unless otherwise noted.



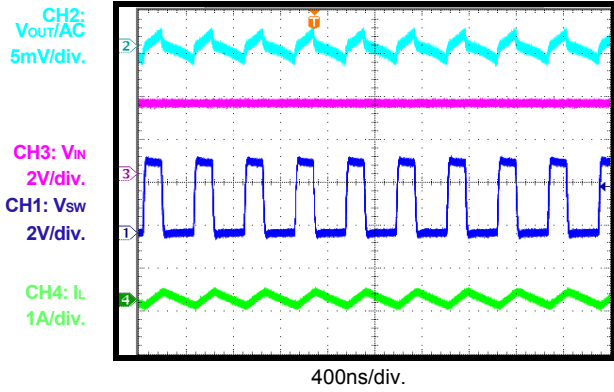
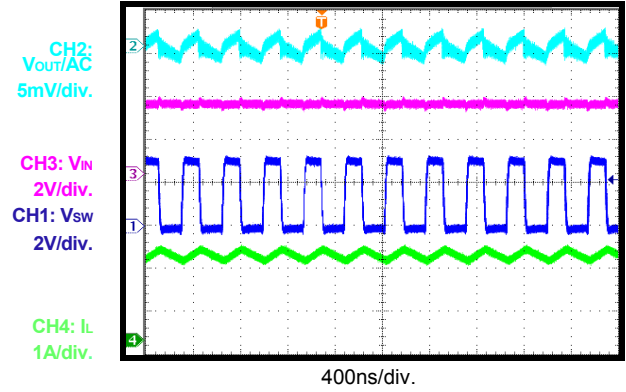
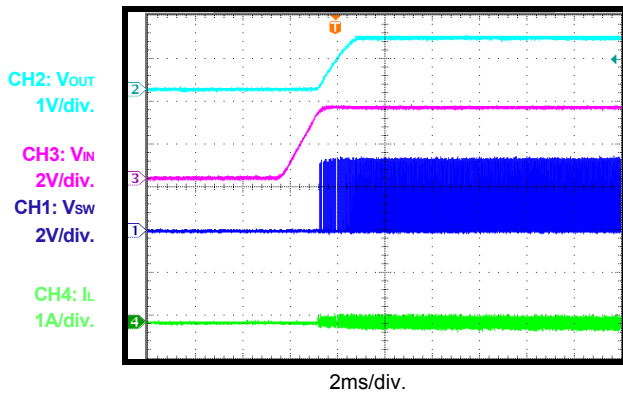
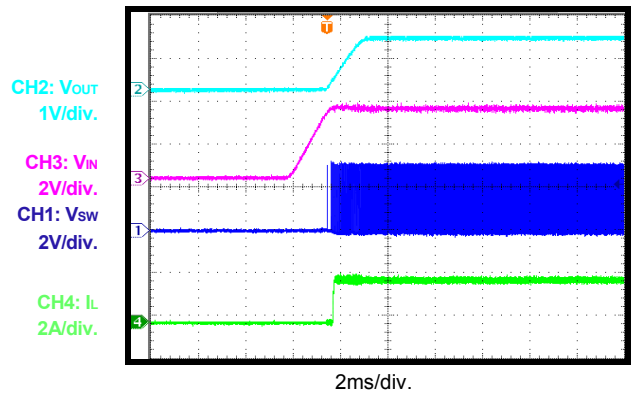
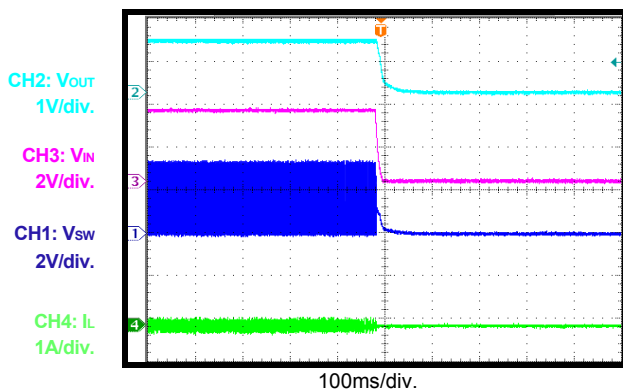
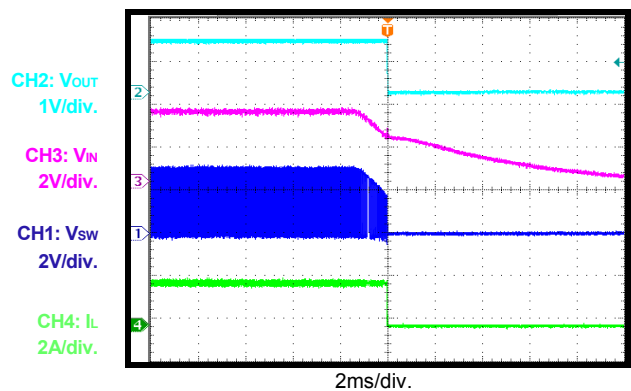
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $L = 1\mu H$, $C_{OUT} = 22\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

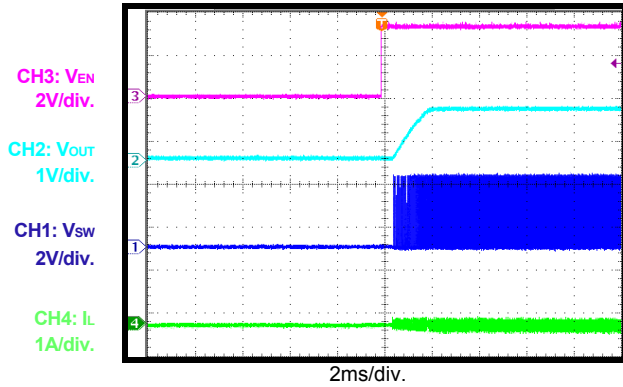
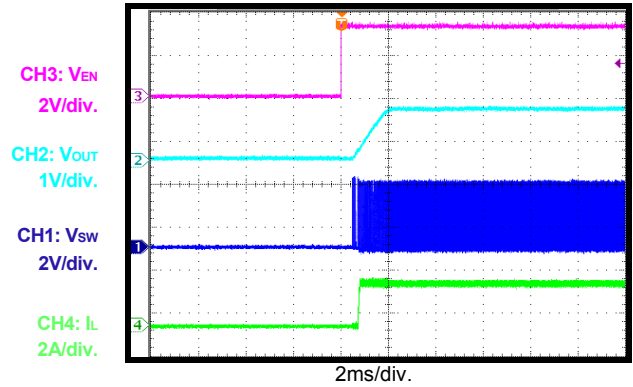
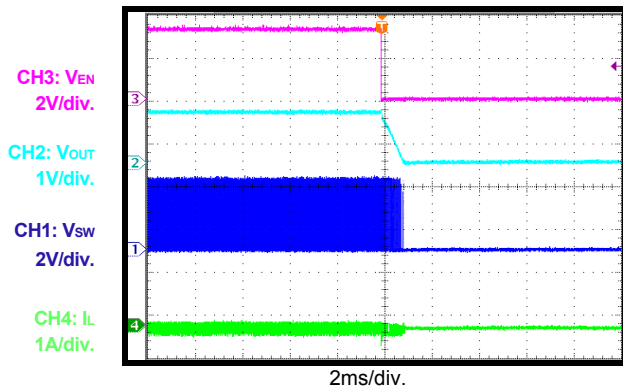
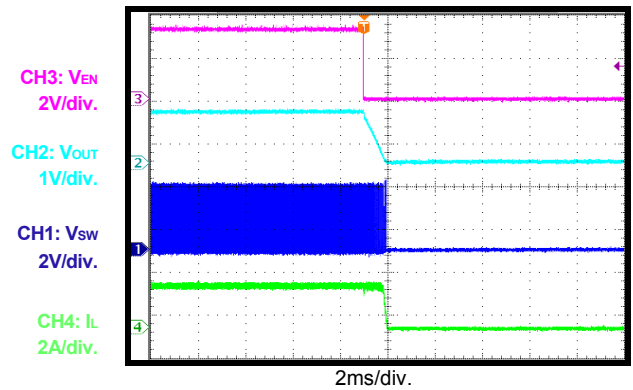
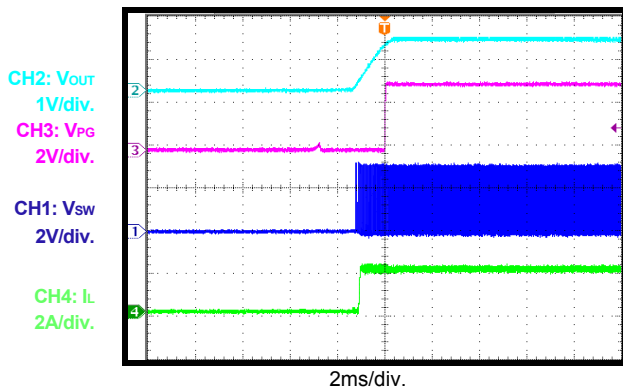
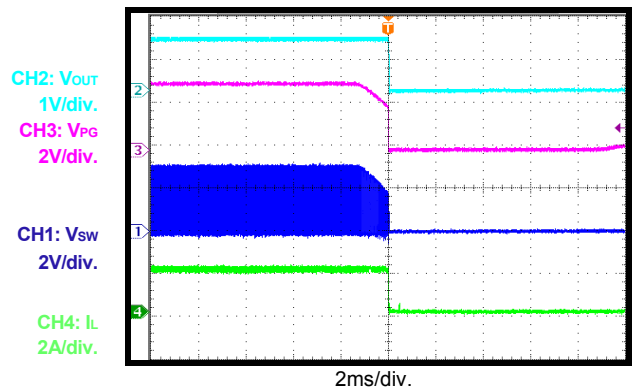
V_{IN} UVLO vs. Temperature



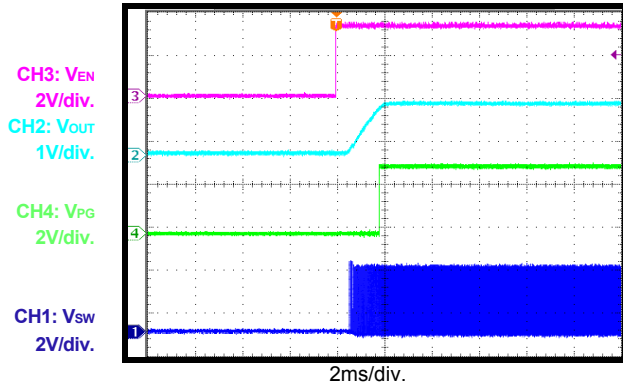
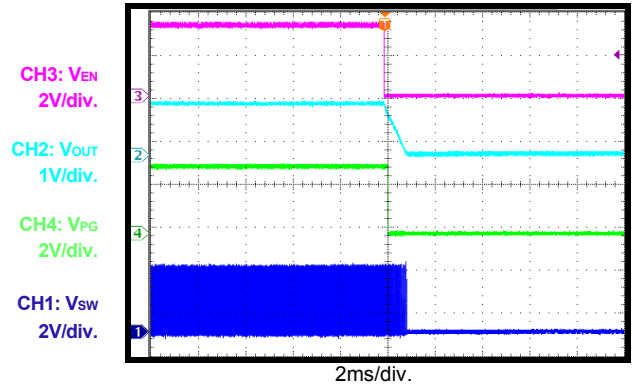
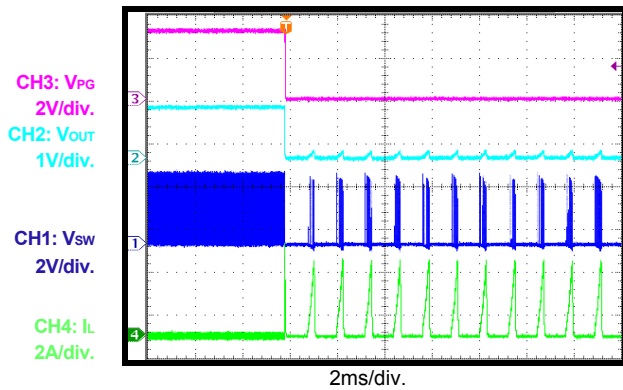
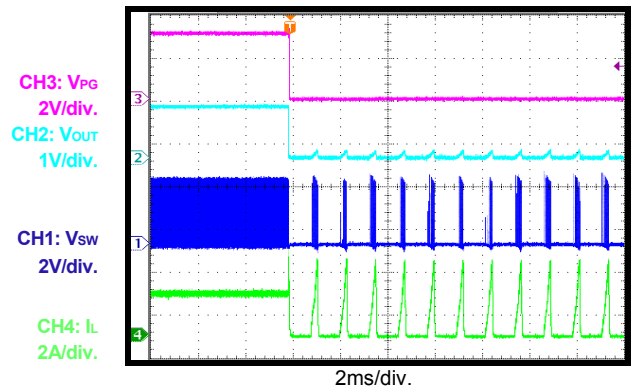
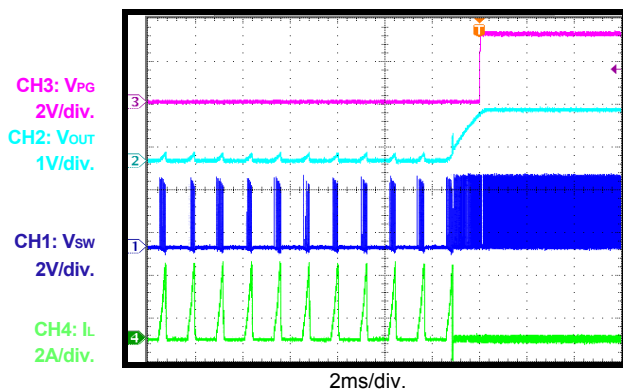
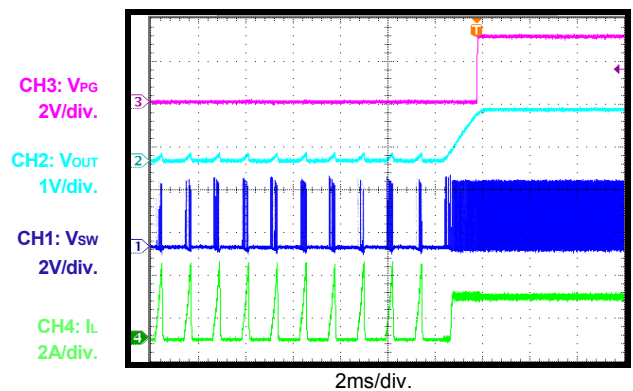
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $L = 1\mu H$, $C_{OUT} = 22\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

Output Ripple
 $I_{OUT} = 0A$

Output Ripple
 $I_{OUT} = 2A$

Start-Up through V_{IN}
 $I_{OUT} = 0A$

Start-Up through V_{IN}
 $I_{OUT} = 2A$

Shutdown through V_{IN}
 $I_{OUT} = 0A$

Shutdown through V_{IN}
 $I_{OUT} = 2A$


TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $L = 1\mu H$, $C_{OUT} = 22\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

Start-Up through EN
 $I_{OUT} = 0A$

Start-Up through EN
 $I_{OUT} = 2A$

Shutdown through EN
 $I_{OUT} = 0A$

Shutdown through EN
 $I_{OUT} = 2A$

PG in Start-Up through VIN
 $I_{OUT} = 2A$

PG in Shutdown through VIN
 $I_{OUT} = 2A$


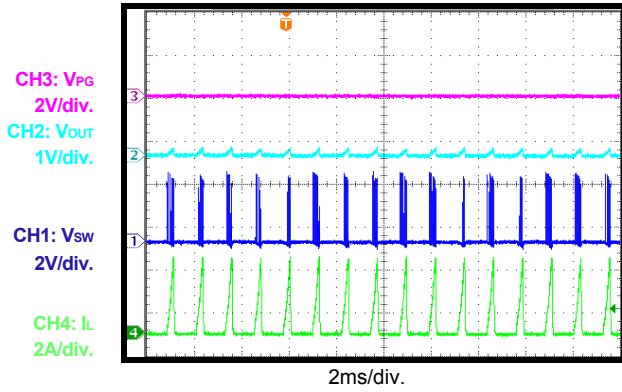
TYPICAL PERFORMANCE CHARACTERISTICS (continued)
 $V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $L = 1\mu H$, $C_{OUT} = 22\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

PG in Start-Up through EN
 $I_{OUT} = 2A$

PG in Shutdown through EN
 $I_{OUT} = 2A$

SCP Entry
 $I_{OUT} = 0A$

SCP Entry
 $I_{OUT} = 2A$

SCP Recovery
 $I_{OUT} = 0A$

SCP Recovery
 $I_{OUT} = 2A$


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

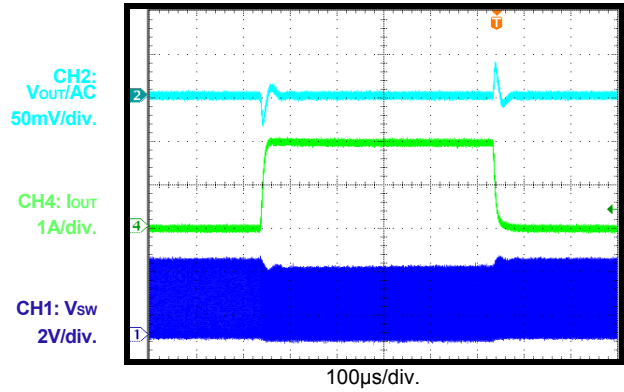
$V_{IN} = 3.3V$, $V_{OUT} = 1.2V$, $L = 1\mu H$, $C_{OUT} = 22\mu F$, $T_A = +25^\circ C$, unless otherwise noted.

SCP Steady State



Load Transient Response

$I_{OUT} = 0 - 2A$



PIN FUNCTIONS

| Package Pin # | Name | Description |
|---------------|------|---|
| 1 | PG | Power good indicator. The output of PG is an open drain that connects to VIN via an internal pull-up resistor. PG goes high if the output voltage is within $\pm 10\%$ of the nominal voltage. |
| 2 | VIN | Input supply. The MPQ2172 operates from a 2.5V to 5.5V input rail. A capacitor (C1) prevents large voltage spikes from appearing at the input. |
| 3 | SW | Switch output. SW is the output of the internal power switch. |
| 4 | PGND | Power ground. PGND is the reference ground of the power device and requires careful consideration during PCB layout. For best results, connect PGND with copper pours and vias. |
| 5 | OUT | Input sense. OUT is for the output voltage feedback. |
| 6 | AGND | Analog ground. AGND is the reference ground of the internal control circuit. |
| 7 | FB | Feedback. Connect FB to the tap of an external resistor divider from the output to AGND to set the output voltage. |
| 8 | EN | Enable. Pull EN high to enable the MPQ2172. Float EN or connect EN to ground to disable the MPQ2172. |

BLOCK DIAGRAM

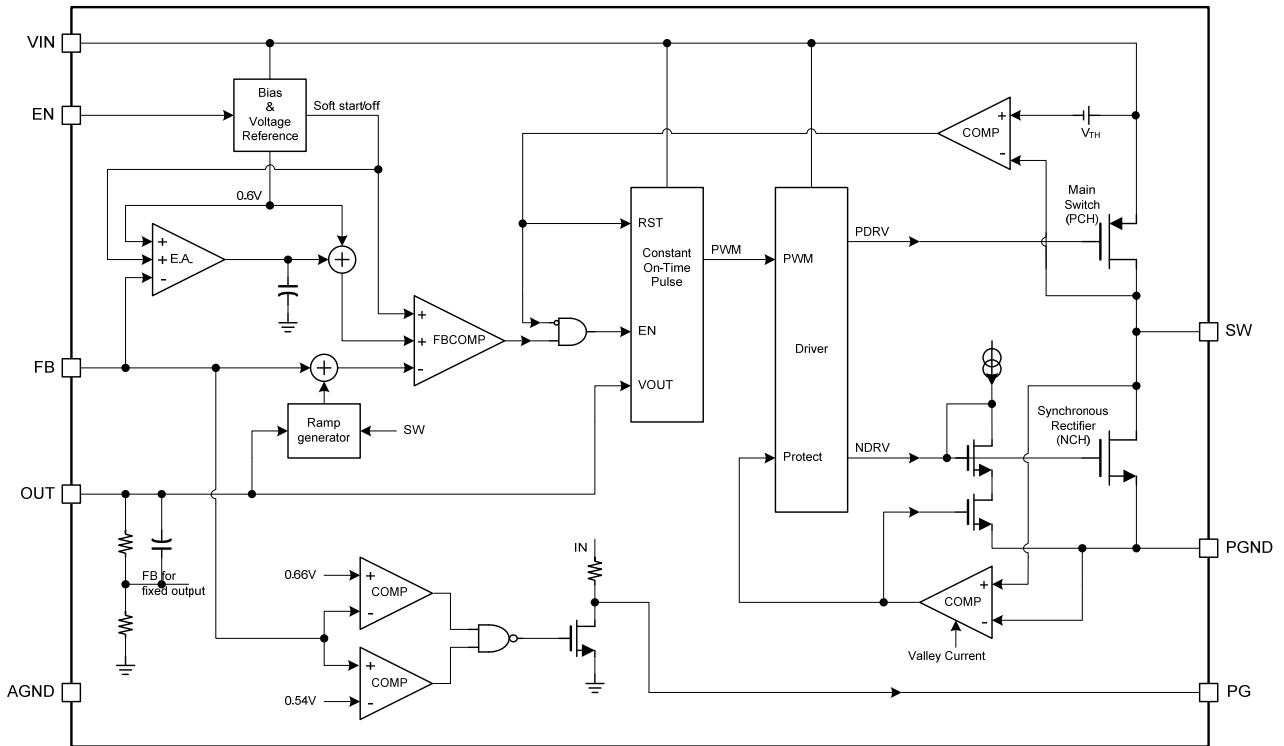


Figure 1: Functional Block Diagram

OPERATION

The MPQ2172 uses constant-on-time (COT) control with input voltage feed-forward to stabilize the switching frequency over its entire input range. The MPQ2172 achieves up to 2A of continuous output current from a 2.5V to 5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-On-Time (COT) Control

Compared to fixed-frequency pulse-width modulation (PWM) control, constant-on-time (COT) control offers a simpler control loop and faster transient response. By using input voltage feed-forward, the MPQ2172 maintains a nearly constant switching frequency across the entire input and output voltage range. The switching pulse on time can be estimated with Equation (1):

$$T_{on} = V_{OUT}/V_{IN} \times 0.385\mu s \quad (1)$$

For the specific value of the on time, refer to the EC table on page 3.

To prevent inductor current runaway during the load transient, the MPQ2172 implements a minimum off time in each cycle. This minimum off time limit does not affect the operation of the MPQ2172 in steady state in any way.

Enable (EN)

When the input voltage exceeds the under-voltage lockout (UVLO) threshold (typically 2.2V), the MPQ2172 is enabled by pulling the enable pin (EN) above 1.2V. Float EN or connect EN to ground to disable the MPQ2172. There is an internal 1M Ω resistor from EN to ground.

Soft-Start/Soft-Stop

The MPQ2172 has a built-in soft start that ramps up the output voltage at a constant slew rate to avoid overshooting during start-up. The soft-start time is about 1.3ms, typically. When disabled, the MPQ2172 ramps down the internal reference voltage to allow the load to discharge the output linearly.

Power Good (PG) Indicator

The MPQ2172 has an open drain with a 500k Ω pull-up resistor pin for power good indication (PG). When FB is within $\pm 10\%$ of the regulation voltage (0.6V), PG is pulled up to VIN by the internal resistor. If the FB voltage is outside the $\pm 10\%$ window, PG is pulled to ground by an internal MOSFET.

Current Limit

The MPQ2172 has a 4.5A current limit for the high-side switch (HS-FET). When the HS-FET reaches its current limit, the MPQ2172 enters hiccup mode until the current drops to prevent the inductor current from building and damaging the components.

Short Circuit and Recovery

The MPQ2172 enters short-circuit protection (SCP) mode when it reaches the current limit and attempts to recover from the short circuit with hiccup mode. In SCP, the MPQ2172 disables the output power stage, discharges a soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still remains after the soft start ends, the MPQ2172 repeats this operation until the short circuit is removed and the output rises back to the regulation level.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. The feedback resistor (R1) must account for both stability and dynamic response and therefore cannot be too large or too small. Choose R1 to be around 41.2kΩ. R2 can then be calculated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{out}}{0.6} - 1} \quad (2)$$

The feedback circuit is shown in Figure 2.

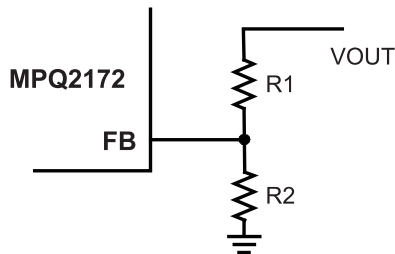


Figure 2: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

| V _{OUT} (V) | R1 (kΩ) | R2 (kΩ) |
|----------------------|-----------|-----------|
| 1.0 | 41.2 (1%) | 60.4 (1%) |
| 1.2 | 41.2 (1%) | 41.2 (1%) |
| 1.8 | 41.2 (1%) | 20.5 (1%) |
| 3.3 | 41.2 (1%) | 9.09 (1%) |

Selecting the Inductor

A 0.47 - 1.5μH inductor is recommended for most applications. For the highest efficiency, choose an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (3):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (3)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (4)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For higher output voltages, use a 47μF capacitor to improve system stability.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality, ceramic capacitor (0.1μF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to prevent excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the output DC voltage. Use low ESR, ceramic capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right) \quad (8)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Layout Guidelines

Proper layout of the switching power supplies is critical for stable operation. For high-frequency switching converters, a poor layout can lead to poor line or load regulation and stability issues. For best results, refer to Figure 3 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, SW) very close to the device using short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.
3. Place the external feedback resistors next to FB.
4. Keep the switching node SW short and away from the feedback network.

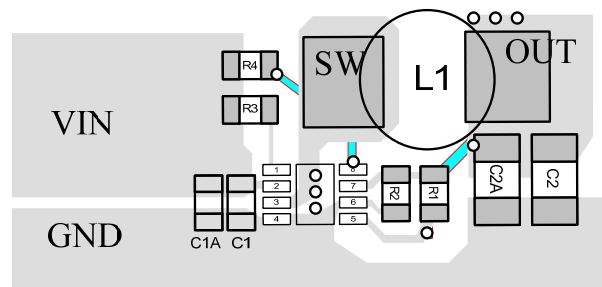


Figure 3: Layout Recommendation

TYPICAL APPLICATION CIRCUITS

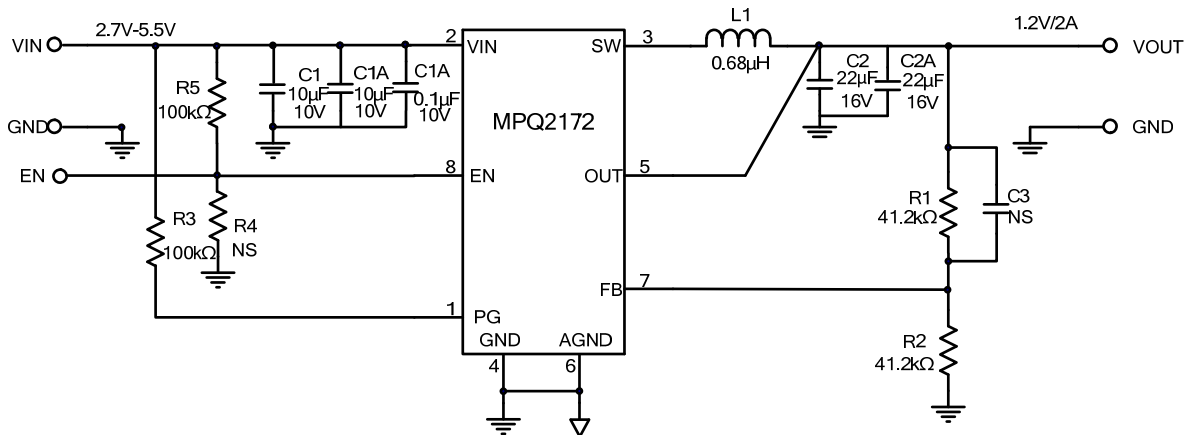


Figure 4: $V_{OUT} = 1.2V$ Typical Application Circuit

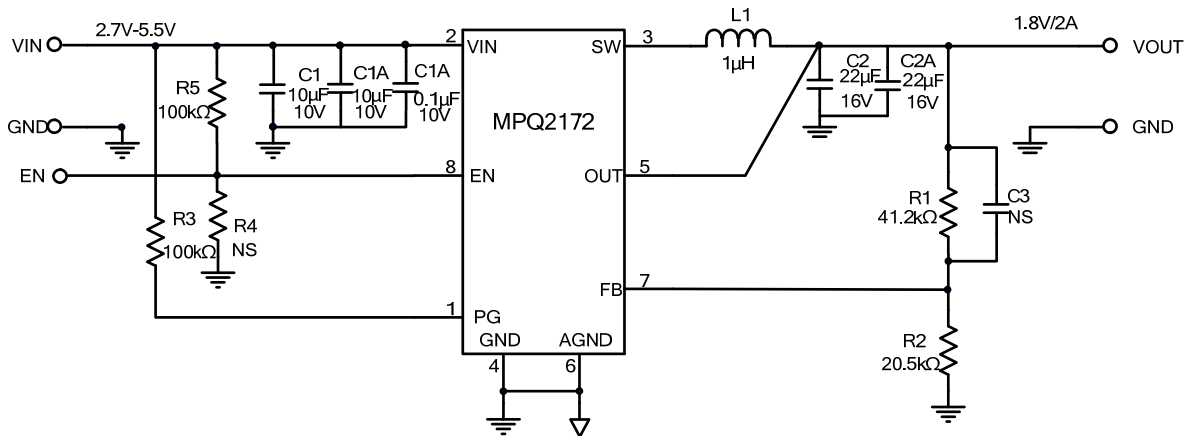
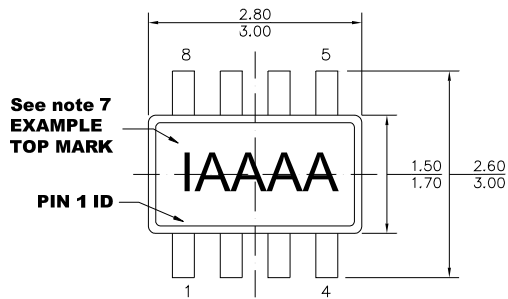


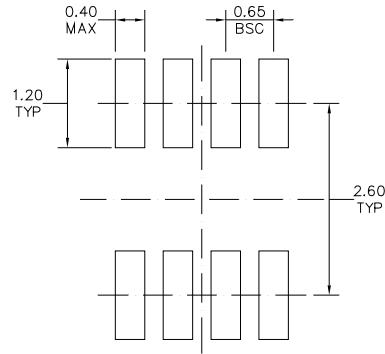
Figure 5: $V_{OUT} = 1.8V$ Typical Application Circuit

PACKAGE INFORMATION

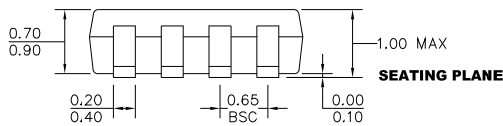
TSOT23-8



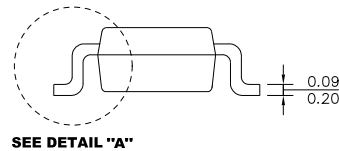
TOP VIEW



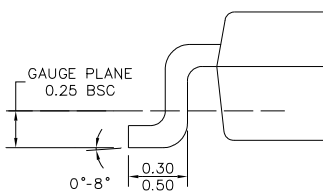
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-193, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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