MPQ70244FS

MPSafe™, ASIL-B, 18V, 4-Channel PMIC with 3 Bucks and 1 LDO, Enhanced PMBus Interface Logic, AEC-Q100 Qualified

DESCRIPTION

The MPQ70244FS is a power management IC (PMIC) solution integrating three high-efficiency step-down DC/DC converters and a low-noise low-dropout (LDO) regulator. Its dual-stage, 18V buck architecture maximizes efficiency for the 1.8V image sensor I/O rail in the CMOS sensor in high-resolution camera modules.

Constant-on-time (COT) control with phase-locked loop (PLL) provides a fast transient response time. During continuous conduction mode (CCM), the fixed 2.2MHz switching frequency (f_{SW}) greatly reduces external inductor and capacitor size.

The PMBus interface allows for application flexibility. The output voltage (V_{OUT}), power sequence, and protection thresholds can all be adjusted via the interface. Fault statuses can also be monitored. Protection features include under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown (TSD).

The MPQ70244FS features enhanced PMBus interface logic, which is recommended for systems using one of its own outputs as a pull-up for its PMBus interface.

The MPQ70244FS supports applications with a high automotive safety integrity level up to ASIL-B. Functional safety features include analog built-in self-testing (ABIST), diagnostics, and a PG output pin. The MPQ70244FS is developed under MPS' advanced MPSafe™ functional safety product development process, which has been independently certified to meet ISO 26262 guidelines.

The MPQ70244FS minimizes external component count and is available in a space-saving QFN-15 (2.5mmx3.5mm) package with wettable flanks. It is available in AEC-Q100 Grade 1.

FEATURES

- Designed for Automotive Cameras
  - Buck 1: 600mA with 3.5V to 18V Input
  - Buck 2: 600mA with 3.5V to 18V Input
  - Buck 3: 1A Buck with 2.5V to 4V Input
  - Low-Dropout (LDO) Regulator: 200mA for Large CMOS Sensors
  - Adjustable Output Voltage via Registers
  - PMBus Interface with Packet Error Checking (PEC)
  - Junction Temperature (T_J) Rating of -40°C to +150°C
  - Available in a QFN-15 (2.5mmx3.5mm) Package with Wettable Flanks
  - Available in AEC-Q100 Grade 1
- Optimized for EMC/EMI
  - 2.2MHz Fixed Switching Frequency (f_{SW})
  - Stepped Triangle Spread Spectrum with On/Off Function
  - Symmetric Input Capacitor for Reduced EMI
- Comprehensive Protection Features
  - Over-Voltage Protection (OVP)
  - Under-Voltage Protection (UVP)
  - Over-Current Protection (OCP)
  - Thermal Shutdown/Warning Protection
  - Power Good (PG) Output
- Functional Safety
  - Hardware Capable to ASIL-B
  - Integrated Analog Built-In Self-Testing (ABIST) and Reference Monitor
  - Documents Available to Aid ISO26262 System Design
  - Failure Modes Effects and Diagnostic Analysis (FMEDA)
  - Safety Manual

MPSafe Developed for Functional Safety Applications: ISO 26262 Compliant

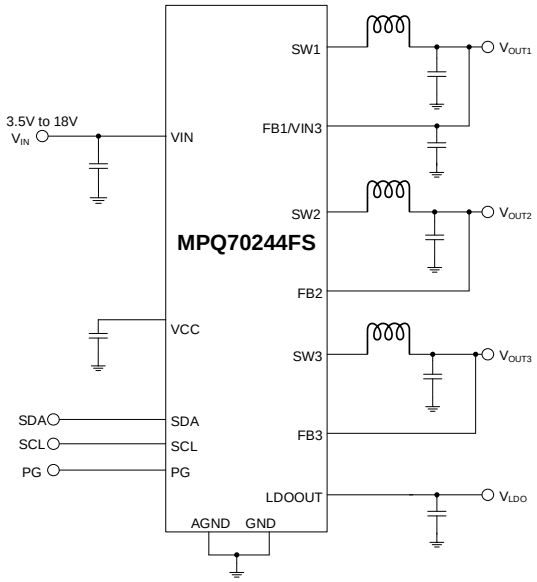
APPLICATIONS

- Automotive Camera Modules
- Space-Constrained Applications

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

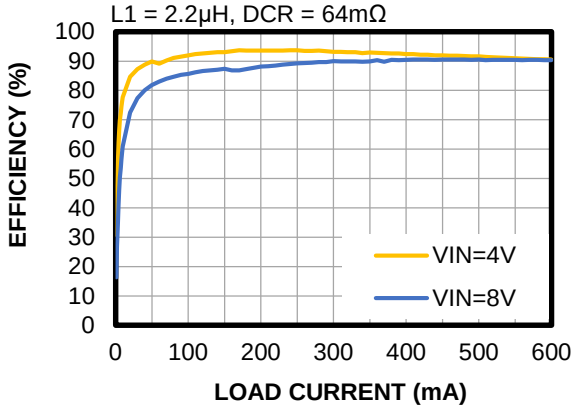
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION



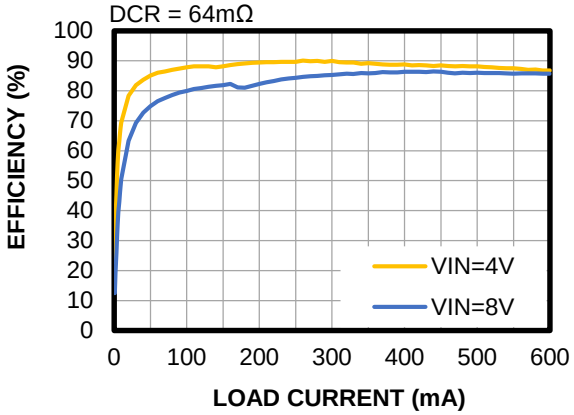
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, DCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



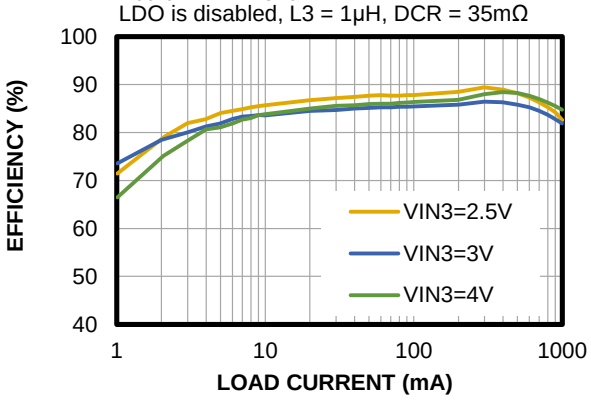
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, DCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, DCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating***
MPQ70244FSGRHE-xxxxAEC1**, ****	QFN-15 (2.5mmx3.5mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ70244FSGRHE-xxxxAEC1-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the OTP register. The default code is "0000". Contact an MPS FAE to create this unique number.

*** Moisture Sensitivity Level Rating

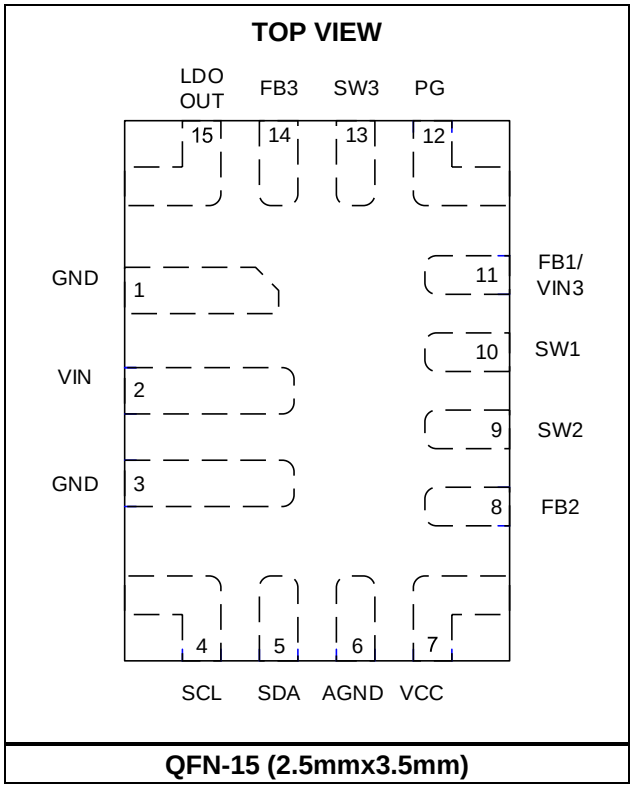
****Wettable flank

TOP MARKING

$\overline{\text{CCU}}$
YWW
LLL

CCU: Production code
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-15 (2.5mmx3.5mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 3	GND	**Power ground.** The two GND pins are connected internally. These pins should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
2	VIN	**Input supply voltage.** VIN supplies power to all the internal control circuitry and the power switch connected to SW1 and SW2. To minimize switching spikes, place a decoupling capacitor from VIN to ground, and close to VIN.
4	SCL	**PMBus interface clock pin.** Use an external pull-up resistor (e.g. 1.5kΩ) to connect the SCL pin to the external supply rail (e.g. 3.3V). Connect SCL to ground if it is not used.
5	SDA	**PMBus interface data pin.** Use an external pull-up resistor (e.g. 1.5kΩ) to connect the SDA pin to the external supply rail (e.g. 3.3V). Connect SDA to ground if it is not used.
6	AGND	**Analog ground.** AGND is the reference ground for the internal logic and signal circuit. AGND is internally connected to GND. AGND should be connected to GND in the PCB.
7	VCC	**Biased supply.** The VCC pin supplies power to the internal control circuit and gate drivers. Place a decoupling capacitor (recommended to be 4.7μF) from VCC to ground, placed as close as possible to VCC.
8	FB2	**Feedback for buck 2.** Connect the FB2 pin directly to buck converter 2's (buck 2) output. See the VOUT_COMMAND (21h on Page 1) section on page 55 for the V_{OUT2} setting.
9	SW2	**Buck 2 switch node.** The SW2 pin is the output of the internal power switch. Connect SW2 to an external inductor using a wide and short PCB trace.
10	SW1	**Buck 1 switch node.** The SW1 pin is the output of the internal power switch. Connect SW2 to an external inductor using a wide and short PCB trace.
11	FB1/VIN3	**Feedback for buck 1 and power source for buck 3 and the LDO.** Directly connect the FB1/VIN3 pin to buck converter 1's (buck 1) output. See the VOUT_COMMAND (21h on Page 0) section on page 43 for the V_{OUT1} setting. The FB1/VIN3 pin supplies power to buck converter 3 (buck 3) and the LDO. To minimize switching spikes, place a decoupling capacitor (recommended to be 0.1uF) from FB1/VIN3 to ground, placed as close as possible to FB1/VIN3.
12	PG	**Power good output.** The output of the PG pin is push-pull. The high output level can be configured to either 3.3V or 1.8V. Float the PG pin if it is not used.
13	SW3	**Buck 3 switch node.** The SW3 pin is the output of the internal power switch. Connect SW3 to an external inductor using a wide PCB trace.
14	FB3	**Feedback for Buck 3.** Directly connect the FB3 pin to buck 3's output. See the VOUT_COMMAND (21h on Page 2) section on page 59 for the V_{OUT3} setting.
15	LDOOUT	**LDO output pin.** See the VOUT_COMMAND (21h on Page 3) section on page 63 for the V_{LDOOUT} setting. A 2.2μF ceramic capacitor is recommended for the LDO output.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}…….. -0.3V to +21V
$V_{SW1/2}$……..-0.6V to V_{IN} + 0.3V
All other pins…… -0.3V to +6.25V
Continuous power dissipation (T_A = 25°C) (2) (6)
QFN-15 (2.5mmx3.5mm)…… 5.95W
Junction temperature (T_J) .....150°C
Lead temperature…….... ……...260°C
Storage temperature……..... -40°C to +150°C

ESD Ratings

Human body model (HBM).....Class 2 (3)
Charged-device model (CDM).....Class C2b (4)

Recommended Operating Conditions

Supply voltage (V_{IN})…… 3.5V to 18V
Buck 1 output voltage (V_{OUT1}).....2.5V to 4V
Buck 2 output voltage (V_{OUT2}).....0.6V to 3.75V
Buck 3 output voltage (V_{OUT3}).....0.6V to 2.55V
LDO output voltage (V_{LDOOUT}).....0.6V to 3.75V
Operating junction temp (T_J).... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-15 (2.5mmx3.5mm)		
JESD51-7	51	5 °C/W (5)
EVQ70244FS-RH-00A	21	1.7 °C/W (6)

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Per AEC-Q100-002.
4) Per AEC-Q100-011.
5) Measured on a JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application. The value of θ_{JC} shows the thermal resistance from junction-to-case bottom.
6) Measured on the MPS standard EVB for the MPQ70244FS, a 6.35cmx6.35cm, 2oz copper, 4-layer PCB. The value of θ_{JC} shows the thermal resistance from junction-to-case top.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Supply Voltage						
VIN quiescent current	I_Q	Disable all channels via the PMBus interface		1	2	mA
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	V_{IN_UVLO}		2.5	2.8	3.1	V
V_{IN} UVLO hysteresis	$V_{IN_UVLO_HYS}$			150		mV
V_{IN} starting level	V_{IN_START}	VIN_START[1:0] = 01	3.7	4	4.3	V
		VIN_START[1:0] = 10	4.7	5	5.3	
		VIN_START[1:0] = 11	5.7	6	6.3	
V_{IN} stopping level	V_{IN_STOP}	VIN_STOP[1:0] = 01	3.2	3.5	3.8	V
		VIN_STOP[1:0] = 10	4.2	4.5	4.8	
		VIN_STOP[1:0] = 11	5.2	5.5	5.8	
VCC regulation voltage	V_{CC}	C_{VCC} = 4.7µF	4.85	5.0	5.15	V
V_{CC} UVLO rising threshold	V_{CC_UVLO}		2.4	2.6	2.8	V
V_{CC} UVLO hysteresis	V_{CC_HYS}			200		mV
Oscillator						
Switching frequency	f_{SW}	FREQUENCY[0] = 0	1.9	2.2	2.5	MHz
		FREQUENCY[0] = 1	2.9	3.3	3.7	
Minimum on time(7)	t_{ON_MIN}			48		ns
Minimum off time(7)	t_{OFF_MIN}			40		ns
Buck Converter 1 (Buck 1)						
Buck 1 output voltage (V_{OUT1}) accuracy	V_{OUT1_ACC}	T_J = 25°C	-1		+1	%
			-1.5		+1.5	%
Buck 1 high-side (HS) switch on resistance	$R_{DS_HS_BUCK1}$			280	500	mΩ
Buck 1 low-side (LS) switch on resistance	$R_{DS_LS_BUCK1}$			150	250	mΩ
SW1 HS switch leakage current	$I_{ILEAK_HS_BUCK1}$			0.01	1.5	µA
SW1 LS switch leakage current	$I_{ILEAK_LS_BUCK1}$			12.5	25	µA
SW1 peak current limit	$I_{LIM0_HS_BUCK1}$	ILIM[0] = 0	800	1000	1250	mA
		ILIM[0] = 1	1000	1250	1650	mA
SW1 valley current limit	I_{VALLEY_BUCK1}	ILIM[0] = 0	650	850	1100	mA
		ILIM[0] = 1	800	1100	1400	mA
SW1 zero-current detection (ZCD) current	I_{ZCD_BUCK1}		-20	50	+150	mA
SW1 reverse current limit	I_{REV_BUCK1}		600			mA
V_{OUT1} feedback leakage	I_{FB_BUCK1}	V_{OUT1} = 4V, buck 3 and LDO disabled		35	80	µA
V_{OUT1} output discharge	I_{DIS_BUCK1}	V_{OUT1} = 0.3V	2			mA
Buck 1 soft-start range (7) (8)	t_{SS_BUCK1}	10% to 90% V_{OUT1}	0.5		2.25	ms
Buck1 soft-start accuracy (7)		V_{OUT1} = 3V	-10		+10	%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck Converter 2 (Buck 2)						
Buck 2 output voltage (V_{OUT2}) accuracy	V_{OUT2_ACC}	V_{OUT2} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT2} ≥ 1.25V	-1.5		+1.5	%
	V_{OUT2_ACC}	V_{OUT2} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT2} < 1.25V	-2		+2	%
Buck 2 HS switch on resistance	$R_{DS_HS_BUCK2}$			280	500	mΩ
Buck 2 LS switch on resistance	$R_{DS_LS_BUCK2}$			150	250	mΩ
SW2 HS switch leakage current	$I_{ILEAK_HS_BUCK2}$			0.01	1.5	µA
SW2 LS switch leakage current	$I_{ILEAK_LS_BUCK2}$			10	25	µA
SW2 peak current limit	$I_{LIM0_HS_BUCK2}$	ILIM[0] = 0	800	1000	1250	mA
		ILIM[0] = 1	1000	1250	1650	mA
SW2 valley current limit	I_{VALLEY_BUCK2}	ILIM[0] = 0	650	850	1100	mA
		ILIM[0] = 1	800	1100	1400	mA
SW2 ZCD current	I_{ZCD_BUCK2}		-20	50	+150	mA
SW2 reverse current limit	I_{REV_BUCK2}		600			mA
V_{OUT2} feedback leakage	I_{FB_BUCK2}	V_{OUT2} = 4V		30	45	µA
V_{OUT2} output discharge	I_{DIS_BUCK2}	V_{OUT2} = 0.3V	2			mA
Buck 2 soft-start range (7) (8)	t_{SS_BUCK2}	10% to 90% V_{OUT2}	0.5		2.25	ms
Buck2 soft-start accuracy(7)		V_{OUT2} = 1.8V	-10		+10	%
Buck 2 PG over-voltage (OV) rising threshold (9)	PG_{OVR0_BUCK2}	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	102	104	106	%
	PG_{OVR1_BUCK2}	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	104	106	108	%
Buck 2 PG OV falling threshold (9)	PG_{OVF0_BUCK2}	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	101.4	103.4	105.4	%
	PG_{OVF1_BUCK2}	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	103.4	105.4	107.4	%
Buck 2 PG OV threshold hysteresis (9)	$PG_{OV_HYS_BUCK2}$			0.6		%
Buck 2 PG under-voltage (UV) rising threshold (9)	PG_{UVR0_BUCK2}	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	95.1	97.1	99.1	%
	PG_{UVR1_BUCK2}	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	92.6	94.6	96.6	%
Buck 2 PG UV falling threshold (9)	PG_{UVF0_BUCK2}	PG_THRESHOLD[0] = 0, V_{OUT2} = 1.8V	94.5	96.5	98.5	%
	PG_{UVF1_BUCK2}	PG_THRESHOLD[0] = 1, V_{OUT2} = 1.8V	92	94	96	%
Buck 2 PG UV threshold hysteresis (9)	$PG_{UV_HYS_BUCK2}$			0.6		%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck Converter 3 (Buck 3)						
Buck 3 output voltage (V_{OUT3}) accuracy	V_{OUT3_ACC}	V_{OUT3} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT3} ≥ 1.25V	-1.5		+1.5	%
		V_{OUT3} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT3} < 1.25V	-2		+2	%
V_{OUT3} HS switch on resistance	$R_{DS_HS_BUCK3}$	V_{OUT1} = 4V		115	215	mΩ
V_{OUT3} LS switch on resistance	$R_{DS_LS_BUCK3}$	V_{OUT1} = 4V		50	120	mΩ
SW3 HS switch leakage current	$I_{ILEAK_HS_BUCK3}$			0.01	80	µA
SW3 LS switch leakage current	$I_{ILEAK_LS_BUCK3}$			0.01	10	µA
SW3 peak current limit	$I_{LIM0_HS_BUCK3}$	ILIM[0] = 0	1.4	1.65	1.9	A
		ILIM[0] = 1	1.7	2.1	2.5	A
SW3 valley current limit	I_{VALLEY_BUCK3}		1.2	1.7	2.2	A
SW3 ZCD current	I_{ZCD_BUCK3}		-50	60	+200	mA
SW3 reverse current limit	I_{REV_BUCK3}		0.6			A
V_{OUT3} feedback leakage	I_{FB_BUCK3}	V_{OUT3} = 2.7V		30	50	µA
V_{OUT3} output discharge	I_{DIS_BUCK3}	V_{OUT3} = 0.3V	2			mA
Buck 3 soft-start range (7) (8)	t_{SS_BUCK3}	10% to 90% V_{OUT3}	0.5		2.25	ms
Buck 3 soft-start accuracy(7)		V_{OUT1} = 3V, V_{OUT3} = 1.2V	-10		+10	%
Buck 3 PG OV rising threshold (9)	PG_{OVR0_BUCK3}	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	102	104	106	%
	PG_{OVR1_BUCK3}	PG_THRESHOLD[0] = 1, V_{OUT3} = 1.2V	104	106	108	%
Buck 3 PG OV falling threshold (9)	PG_{OVF0_BUCK3}	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	101.3	103.3	105.3	%
	PG_{OVF1_BUCK3}	PG_THRESHOLD[0] = 1, V_{OUT3} = 1.2V	103.3	105.3	107.3	%
Buck 3 PG OV threshold, hysteresis (9)	$PG_{OV_HYS_BUCK3}$			0.7		%
Buck 3 PG UV rising threshold (9)	PG_{UVR0_BUCK3}	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	95.1	97.1	99.1	%
	PG_{UVR1_BUCK3}	PG_THRESHOLD[0] = 1, V_{OUT3} = 1.2V	92.7	94.7	96.7	%
Buck 3 PG UV falling threshold (9)	PG_{UVF0_BUCK3}	PG_THRESHOLD[0] = 0, V_{OUT3} = 1.2V	94.4	96.4	98.4	%
	PG_{UVF1_BUCK3}	PG_THRESHOLD[0] = 1, V_{OUT3} = 1.2V	92	94	96	%
Buck 3 PG UV threshold hysteresis (9)	$PG_{UV_HYS_BUCK3}$			0.7		%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Low-Dropout (LDO) Regulator Output						
LDO accuracy	V_{OUT4_ACC}	V_{OUT4} ≥ 1.25V, T_J = 25°C	-1		+1	%
		V_{OUT4} ≥ 1.25V	-1.5		+1.5	%
		V_{OUT4} < 1.25V, T_J = 25°C	-1.5		+1.5	%
		V_{OUT4} < 1.25V	-2		+2	%
LDO power supply rejection ratio (PSRR) (7)	L_{DO_PSRR}	No input capacitor, C_{OUT} = 22µF,f = 2MHz, I_{LDO} = 100mA		50		dB
LDO dropout voltage	V_{DROP_LDO}	V_{IN3} = 3.2V, setting LDO output = 3.3V, I_{LDO} = 200mA		100	220	mV
LDO I_{LIMIT}	I_{LIM_LDO}	V_{IN3} = 3.0V, setting LDO output = 2.5V	280			mA
LDO output discharge	I_{DIS_LDO}	V_{LDO}=0.3V	2			mA
LDO soft-start time	t_{SS_LDO}	V_{OUT} = 10% to 90%, C_{OUT} = 4.7µF, V_{OUT} = 2.5V	50	130	200	µs
LDO line regulation	$L_{DO_LINE_REG}$	V_{IN3} = 2.7V to 4V.		0.02	0.1	% / V
LDO load regulation	$L_{DO_LOAD_REG}$	V_{IN3} = 3.3V, I_{OUT} from 10mA to 200mA		0.03	0.15	%
LDO noise (7)	V_{LDO_NOISE}	V_{IN3} = 3.7V, V_{LDO} = 3.3V, I_{LDO} = 200mA, buck 1 is not switching, buck 3 and buck 2 are disabled		105		μV_{RMS}
LDO PG OVP rising threshold (9)	PG_{OVR0_LDO}	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	102	104	106	%
	PG_{OVR1_LDO}	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	104	106	108	%
LDO PG OVP falling threshold (9)	PG_{OVF0_LDO}	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	101.4	103.4	105.4	%
	PG_{OVF1_LDO}	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	103.4	105.4	107.4	%
LDO PG OVP hysteresis (9)	$PG_{OV_HYS_LDO}$			0.6		%
LDO PG UVP rising threshold (9)	PG_{UVR0_LDO}	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	94.6	96.6	98.6	%
	PG_{UVR1_LDO}	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	92.6	94.6	96.6	%
LDO PG UVP falling threshold (9)	PG_{UVF0_LDO}	PG_THRESHOLD[0] = 0, V_{LDO} = 2.5V	94	96	98	%
	PG_{UVF1_LDO}	PG_THRESHOLD[0] = 1, V_{LDO} = 2.5V	92	94	96	%
LDO PG UVP hysteresis (9)	$PG_{UV_HYS_LDO}$			0.6		%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection						
Thermal warning (7)	T_{TW}		110	125	140	°C
Thermal warning hysteresis (7)	T_{TW_HYS}			20		°C
Thermal shutdown (7)	T_{SD}		155	170	185	°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			20		°C
Output Voltage Protection						
V_{OUT} OVP threshold (9)	V_{OUT_OV}	V_{OUT} > 1.25V	112	115	118	%
		V_{OUT} < 1.25V	110	115	120	%
V_{OUT} OV hysteresis (9)	$V_{OUT_OV_HYS}$	V_{OUT} > 1.25V	3.5	6	8.5	%
		V_{OUT} < 1.25V	2.5	6	10	%
V_{OUT} OVP threshold (9)	V_{OUT_UV}	V_{OUT} > 1.25V	72	75	78	%
		V_{OUT} < 1.25V	70	75	80	%
Hiccup time	t_{HIC}			1		ms
Reference Monitor						
Reference OVP threshold	V_{REF_OV}		102	103.3	104.6	%
Reference UVP threshold	V_{REF_UV}		95.4	96.7	98	%
Programming Options						
V_{OUT} range (7) (8)	V_{OUT1}		2.5		4.0	V
	V_{OUT2}		0.6		3.75	
	V_{OUT3}		0.6		2.55	
	LDO_{OUT}		0.6		3.75	
Start delay range (7) (8)	t_{START_DELAY}	D0h, bit[0] = 1'b0, 0.25ms/step	0		3.75	ms
		D0h, bit[0] = 1'b1, 2.5ms/step	0		37.5	ms
Start delay accuracy (7)		t_{START_DELAY} > 0ms	-10		+10	%
		t_{START_DELAY} = 0ms			200	µs
Stop delay range (7) (8)	t_{STOP_DELAY}	D0h, bit[0] = 1'b0, 0.25ms/step	0		3.75	ms
		D0h, bit[0] = 1'b1, 2.5ms/step	0		37.5	ms
Stop delay accuracy (7)		t_{STOP_DELAY} > 0ms	-10		+10	%
		t_{STOP_DELAY} = 0ms			200	µs
PG output voltage (7) (8)	V_{PG}	CCh, bit[3] = 1'b0	1.72	1.8	1.88	V
		CCh, bit[3] = 1'b1	3.16	3.3	3.44	V
PG de-assert delay time range (7) (8)	t_{PG_DLY}		0		10	ms
PG de-assert delay accuracy (7)		t_{PG_DLY} > 0ms	-10		+10	%
		t_{PG_DLY} = 0ms			200	µs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

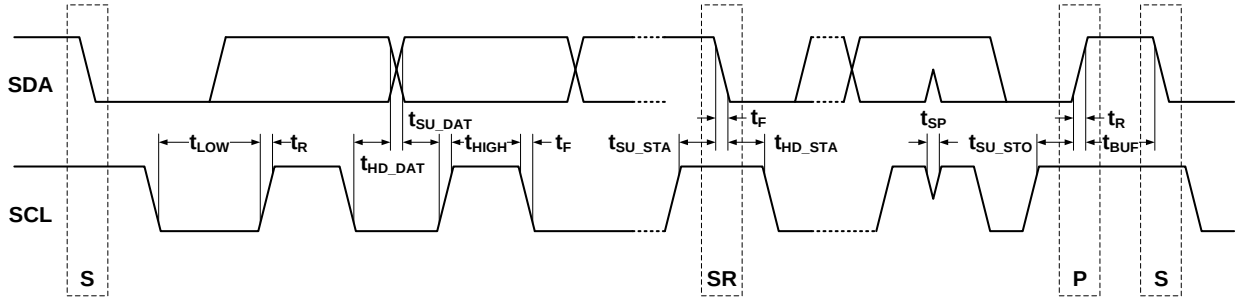
V_{IN} = 8V, T_J = -40°C to +150°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PMBus Interface (7)						
PMBus interface ready time	t_{PMB_R}	From V_{IN} > $V_{IN_UVLO_RISING}$ threshold to PMBus interface ready			12	ms
Input logic high	V_{IH}		1.6			V
Input logic low	V_{IL}				0.4	V
V_{OUT} logic low	V_{OUT_L}	SDA pin sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				1000	kHz
SCL high time	t_{HIGH}		260			ns
SCL low time	t_{LOW}		500			ns
Data set-up time	t_{SU_DAT}		50			ns
Data hold time	t_{HD_DAT}		0			ns
Set-up time for repeated start	t_{SU_STA}		260			ns
Hold time for (repeated) start	t_{HD_STA}		260			ns
Bus free time between a start and a stop command	t_{BUF}		500			ns
Set-up time for stop command	t_{SU_STO}		260			ns
Rising time of SCL and SDA	t_R				120	ns
Falling time of SCL and SDA	t_F	V_{DD} supplies the PMBus interface	20 x (V_{DD} / 5.5V)		120	ns
Pulse width of suppressed spike	t_{SP}				50	ns
Capacitance bus for each bus line	C_B				550	pF

Notes:

7) Guaranteed by design and bench characterization. Not tested in production.
8) Write to the relevant register to update this parameter.
9) The threshold is based on the nominal V_{OUT} of each output.

PMBUS INTERFACE TIMING DIAGRAM



S: Start Command
SR: Repeated Start Command
P: Stop Command

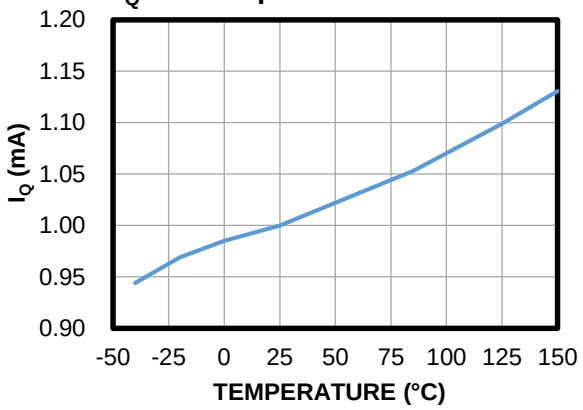
Figure 1: PMBus Interface Compatible Timing Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

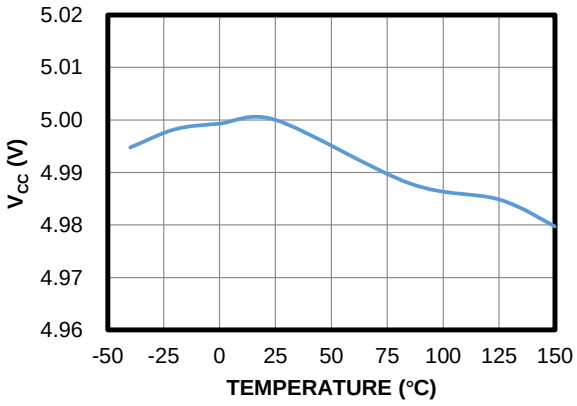
TYPICAL CHARACTERISTICS

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

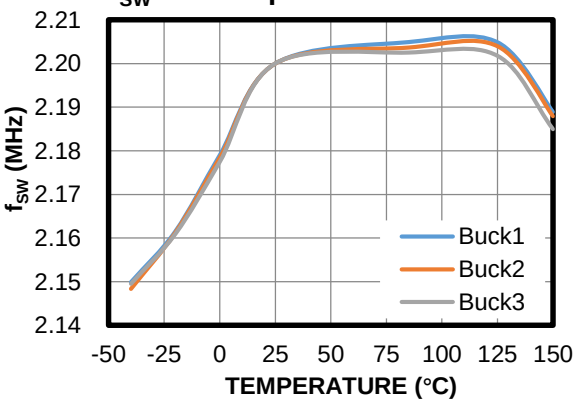
I_Q vs. Temperature



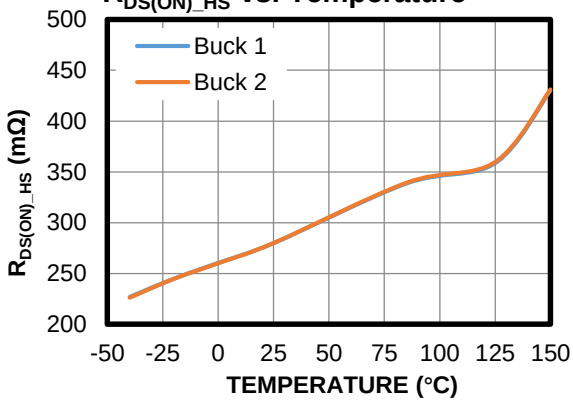
V_{CC} vs. Temperature



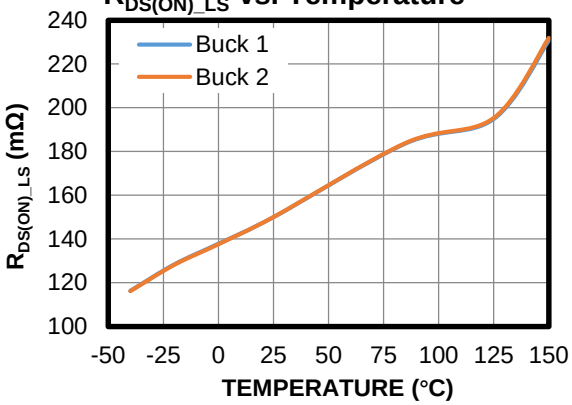
f_{SW} vs. Temperature



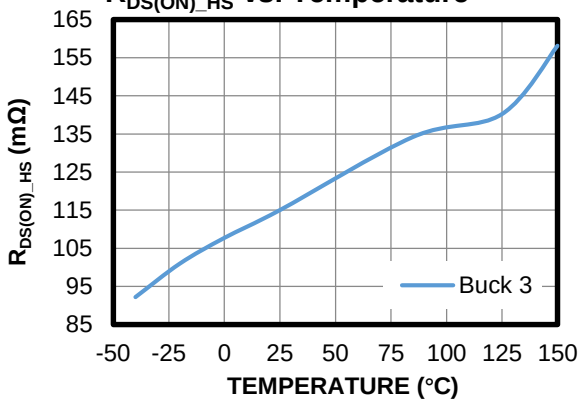
$R_{DS(ON)_HS}$ vs. Temperature



$R_{DS(ON)_LS}$ vs. Temperature



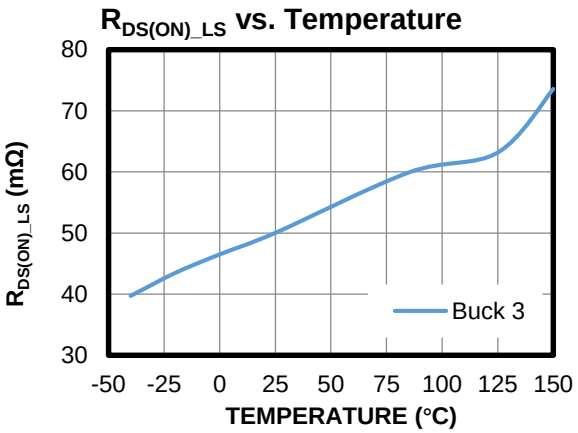
$R_{DS(ON)_HS}$ vs. Temperature

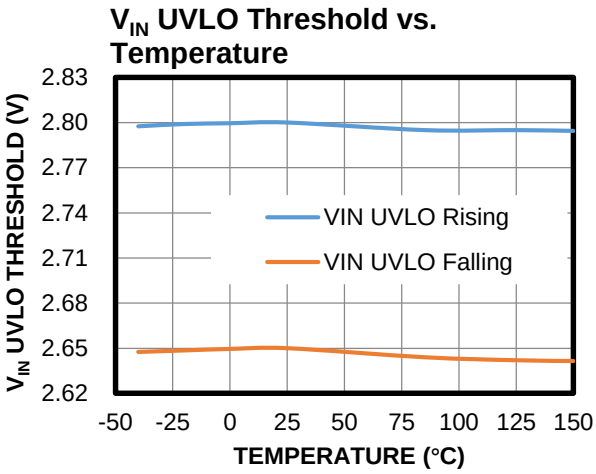


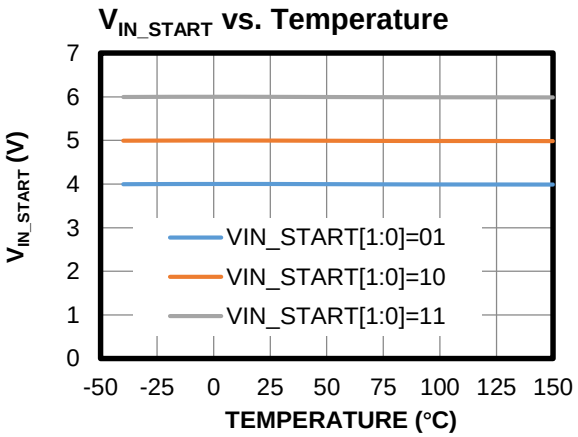
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

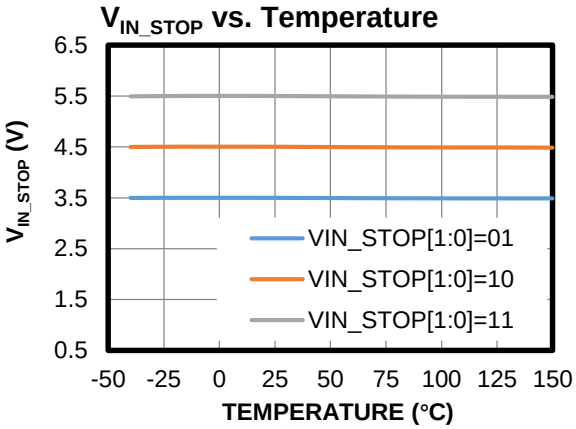
TYPICAL CHARACTERISTICS *(continued)*

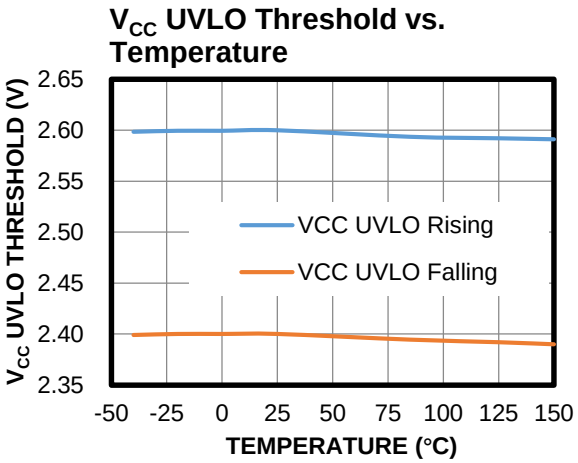
V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

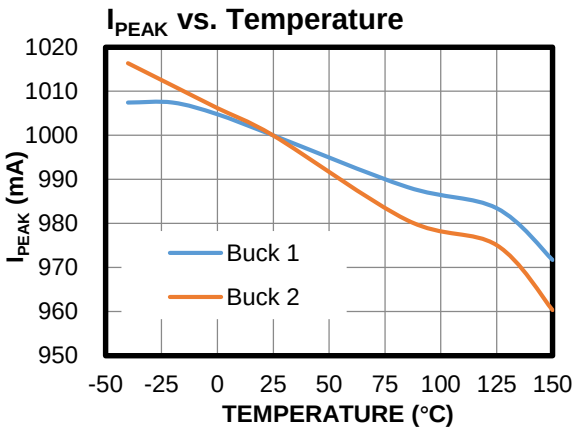










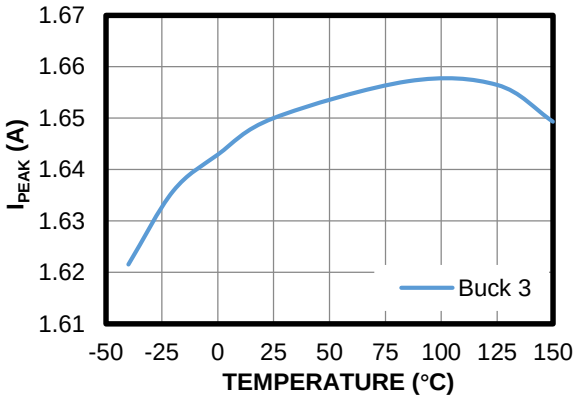


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

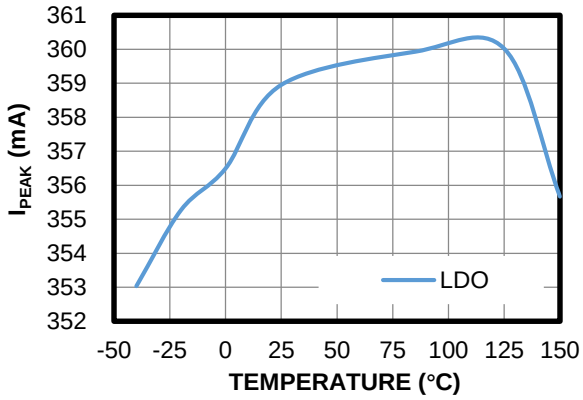
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

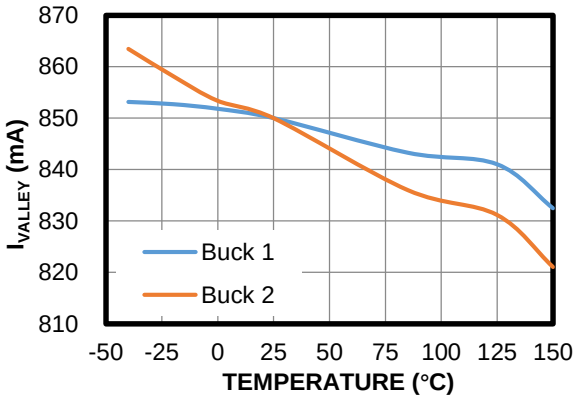
I_{PEAK} vs. Temperature



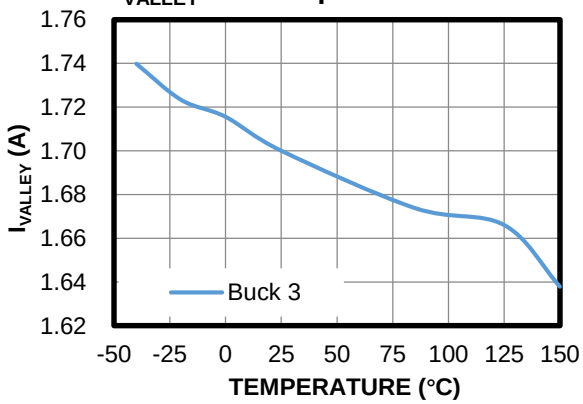
I_{PEAK} vs. Temperature



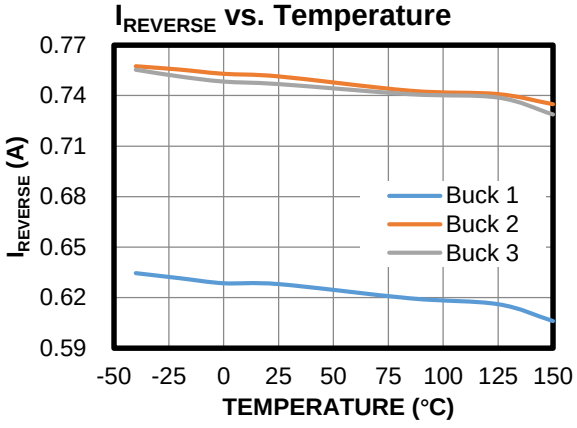
I_{VALLEY} vs. Temperature



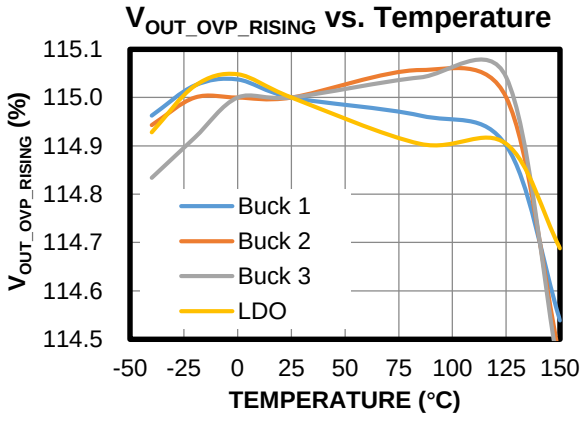
I_{VALLEY} vs. Temperature



$I_{REVERSE}$ vs. Temperature



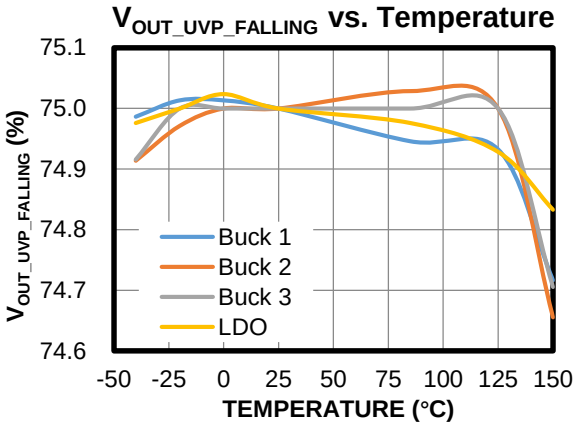
$V_{OUT_OVP_RISING}$ vs. Temperature

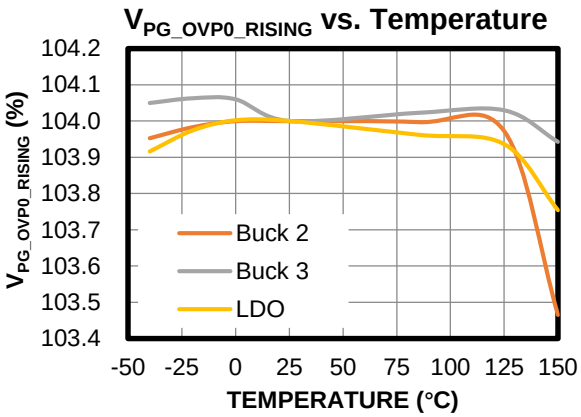


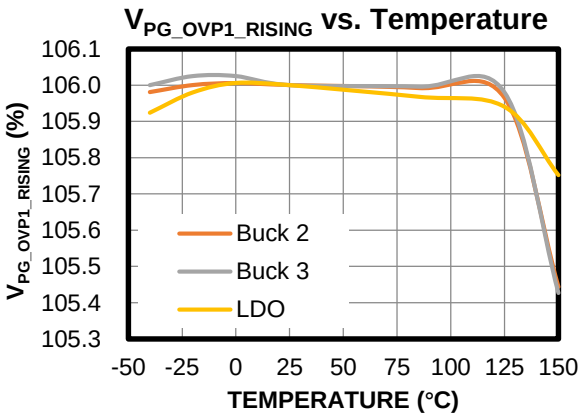
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

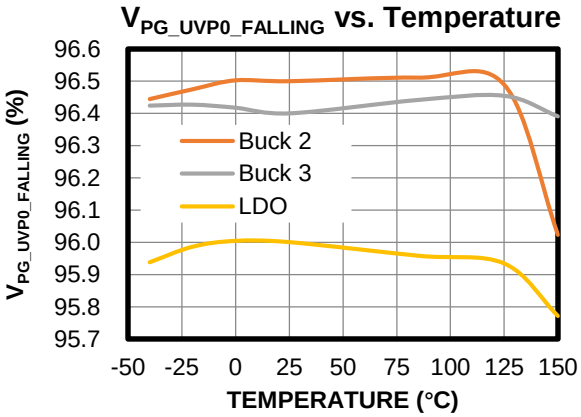
TYPICAL CHARACTERISTICS *(continued)*

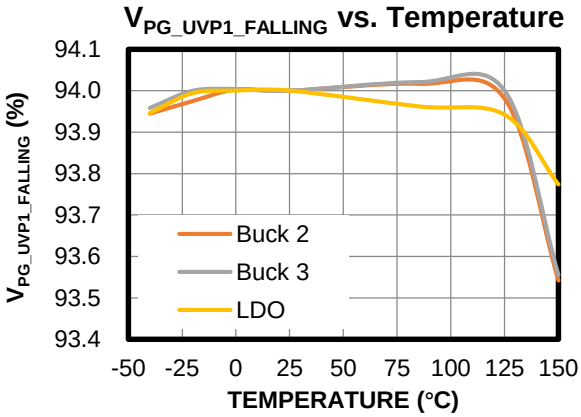
V_{IN} = 8V, T_A = -40°C to +150°C, unless otherwise noted.

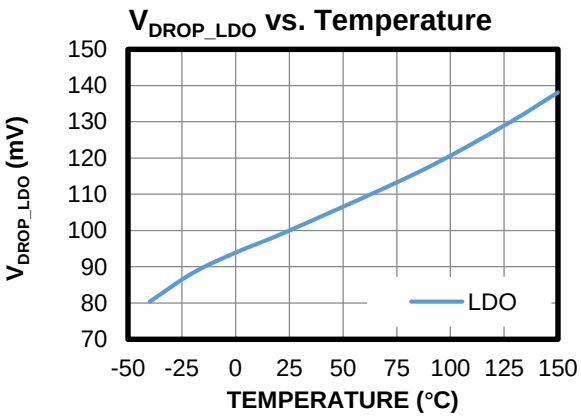












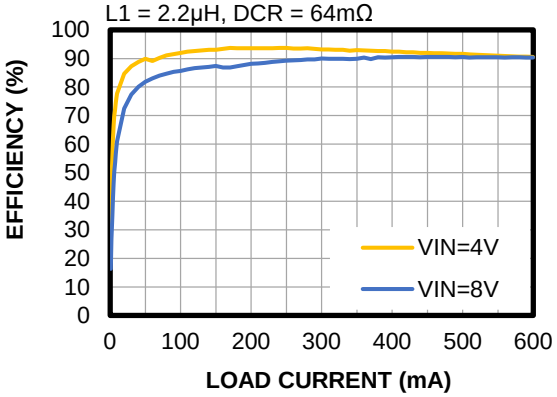
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

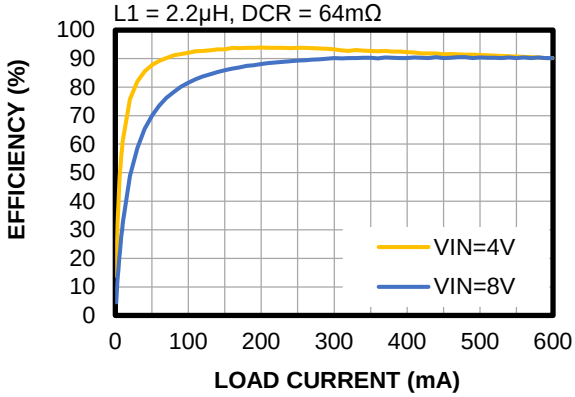
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, DCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



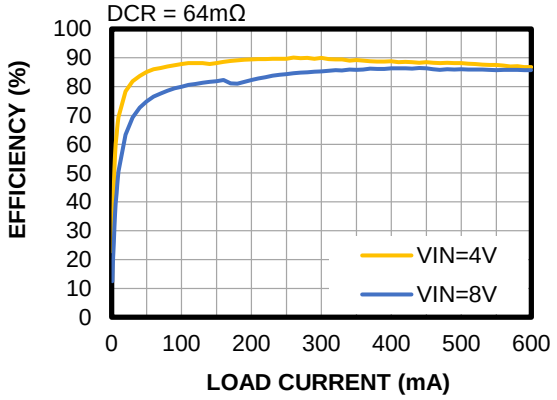
Efficiency vs. Load Current (Buck 1)

V_{OUT1} = 3V, f_{SW1} = 2.2MHz, FCCM, other channels are disabled, L1 = 2.2µH, DCR = 64mΩ



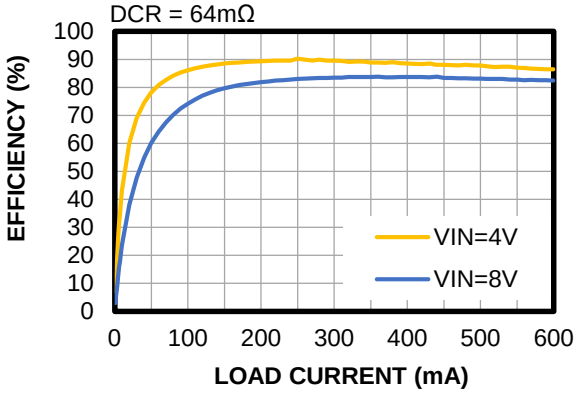
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, DCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



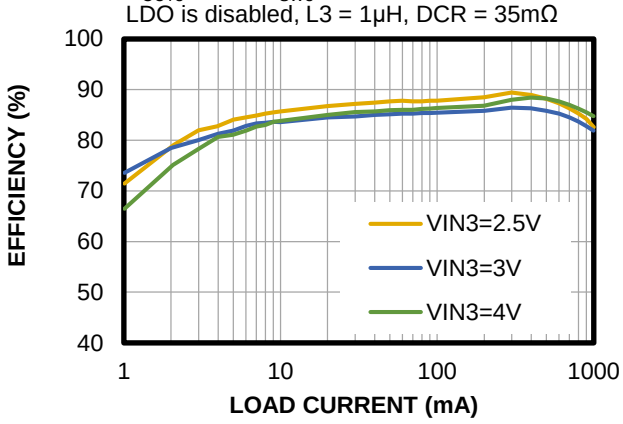
Efficiency vs. Load Current (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, FCCM, other channels are disabled, L2 = 2.2µH, DCR = 64mΩ



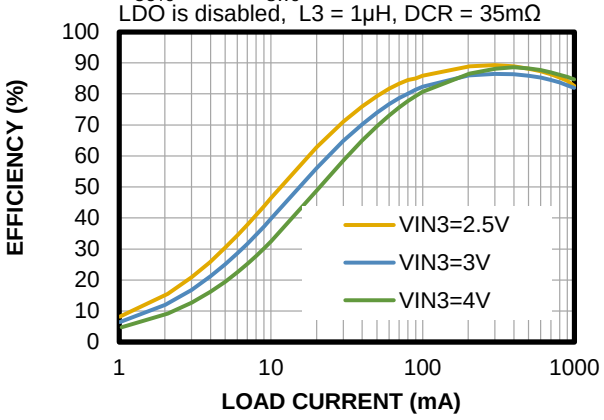
Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, DCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



Efficiency vs. Load Current (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, FCCM, LDO is disabled, L3 = 1µH, DCR = 35mΩ



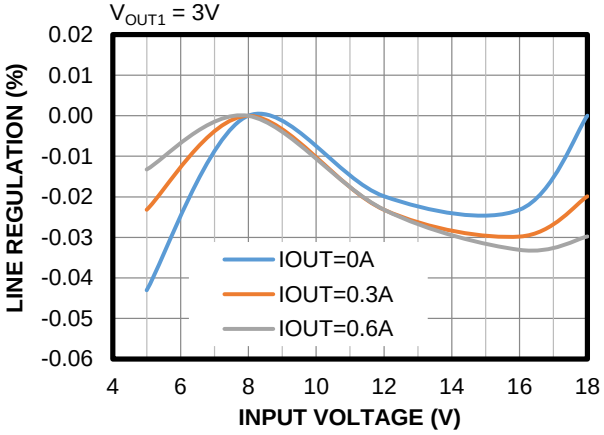
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

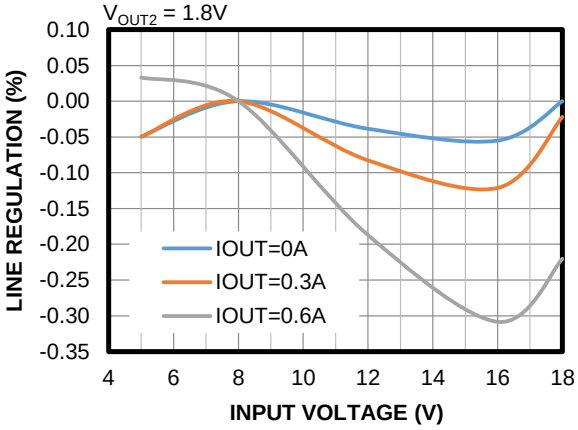
Line Regulation (Buck 1)

V_{OUT1} = 3V



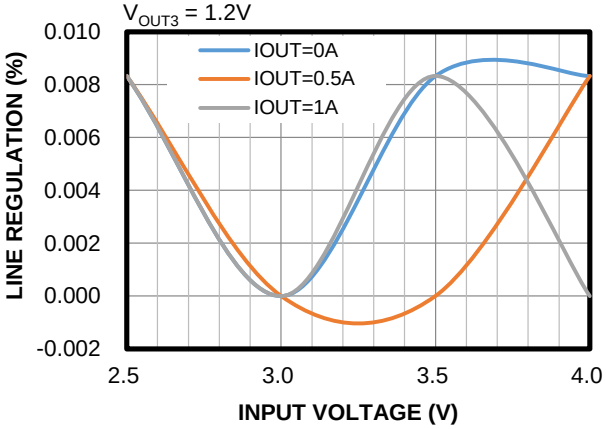
Line Regulation (Buck 2)

V_{OUT2} = 1.8V



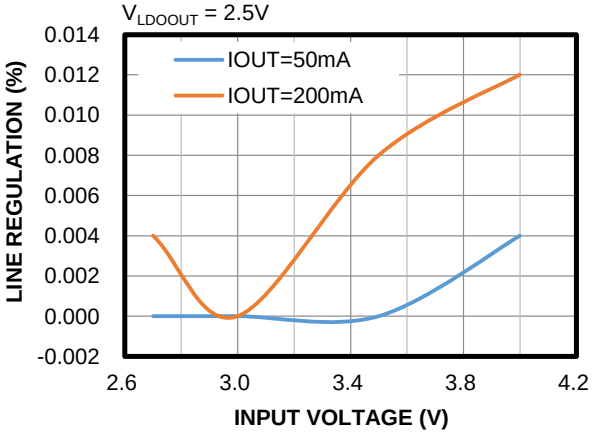
Line Regulation (Buck3)

V_{OUT3} = 1.2V



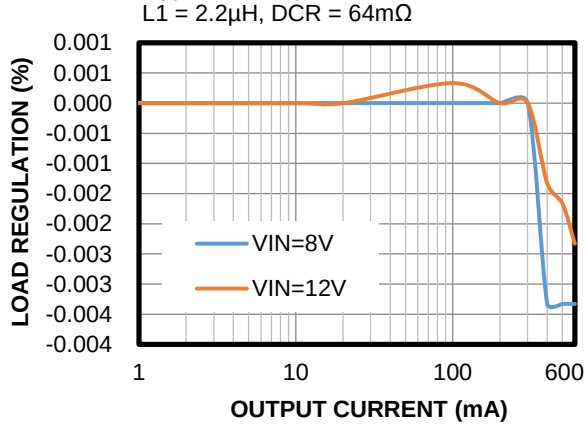
Line Regulation (LDO)

V_{LDOOUT} = 2.5V



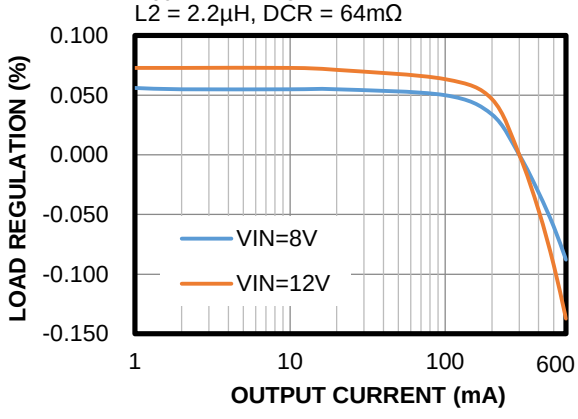
Load Regulation (Buck 1)

V_{OUT1} = 3.0V, f_{SW1} = 2.2MHz, FCCM,
L1 = 2.2µH, DCR = 64mΩ



Load Regulation (Buck 2)

V_{OUT2} = 1.8V, f_{SW2} = 2.2MHz, FCCM,
L2 = 2.2µH, DCR = 64mΩ



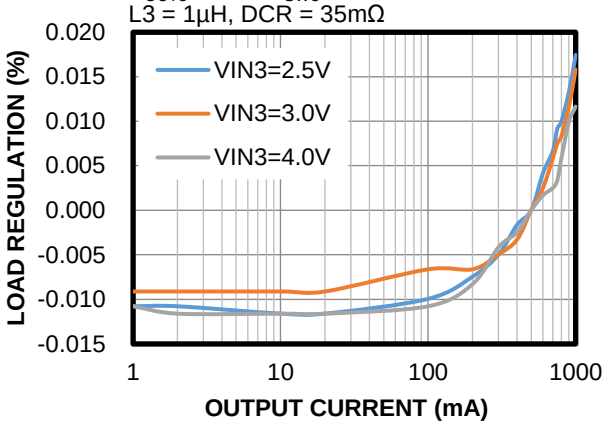
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

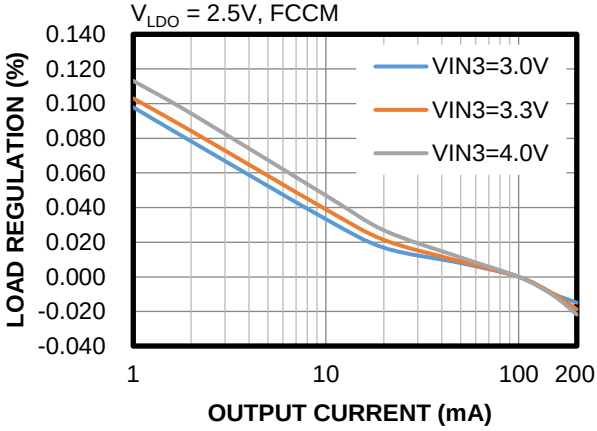
Load Regulation (Buck 3)

V_{OUT3} = 1.2V, f_{SW3} = 2.2MHz, FCCM, L3 = 1µH, DCR = 35mΩ



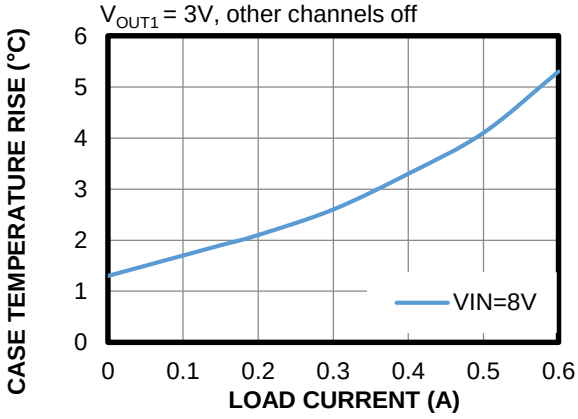
Load Regulation (LDO)

V_{LDO} = 2.5V, FCCM



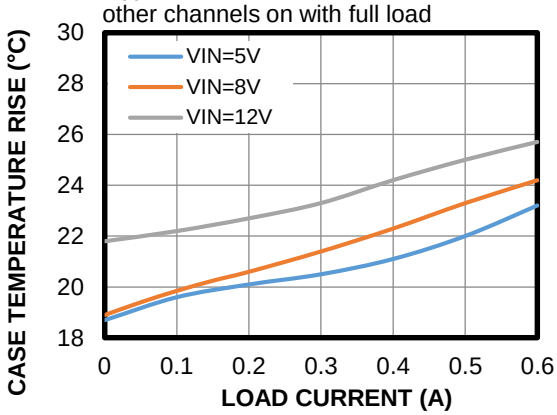
Case Temperature Rise (Buck 1)

V_{OUT1} = 3V, other channels off



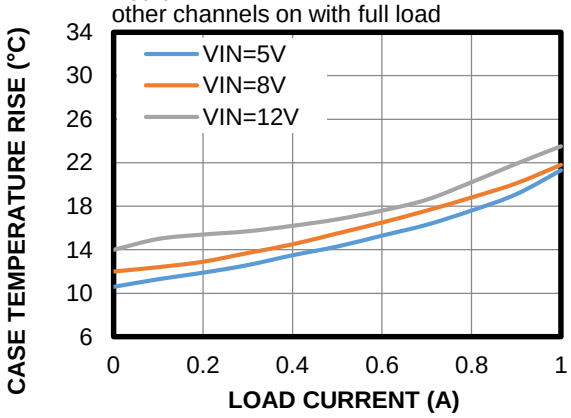
Case Temperature Rise (Buck 2)

V_{OUT2} = 1.8V, channel 1 on with no load, other channels on with full load



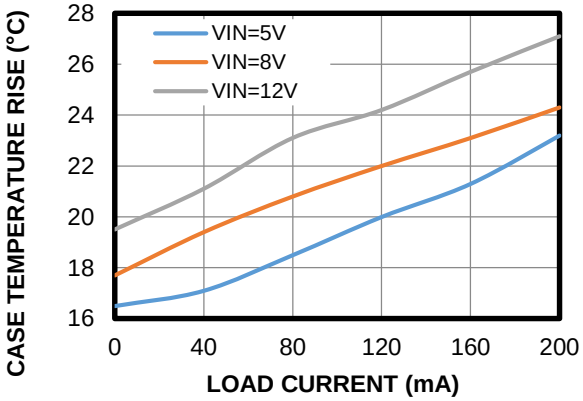
Case Temperature Rise (Buck 3)

V_{OUT3} = 1.2V, channel 1 on with no load, other channels on with full load



Case Temperature Rise (LDO)

V_{LDOOUT} = 2.5V, channel 1 on with no load, other channels on with full load



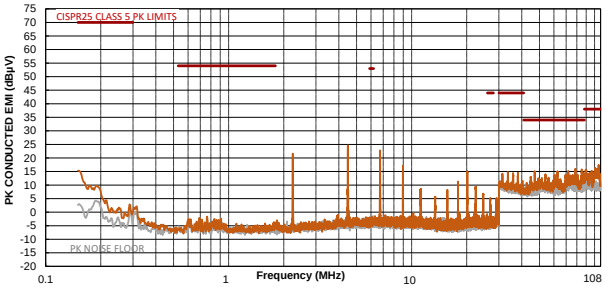
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (10)

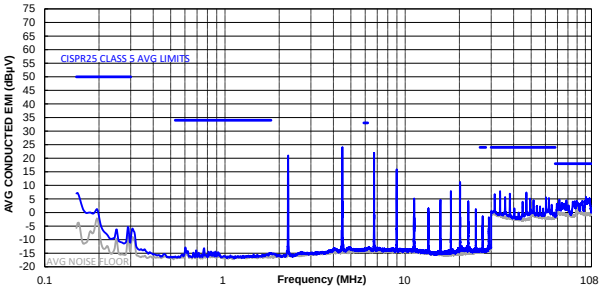
CISPR 25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



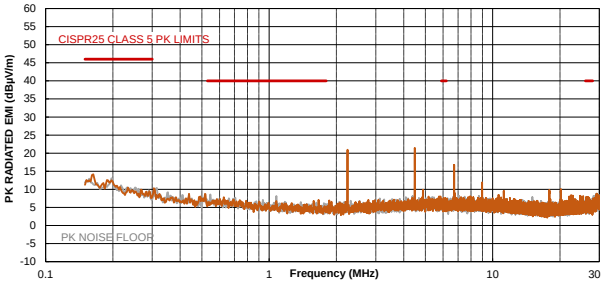
CISPR 25 Class 5 Average Conducted Emissions

150kHz to 108MHz



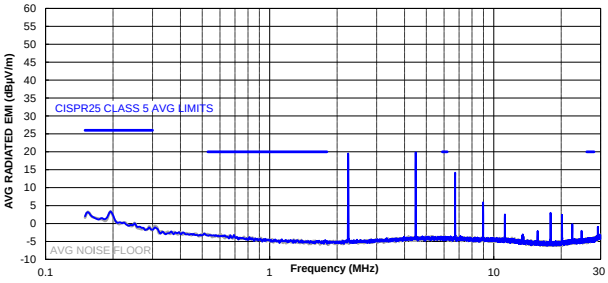
CISPR 25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



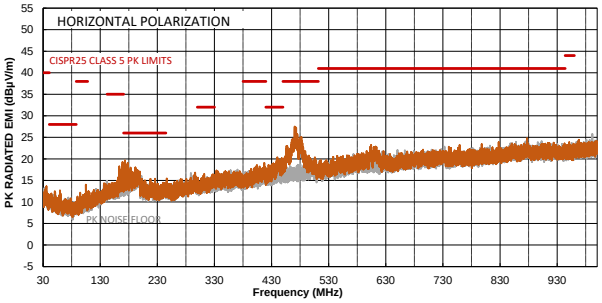
CISPR 25 Class 5 Average Radiated Emissions

150kHz to 30MHz



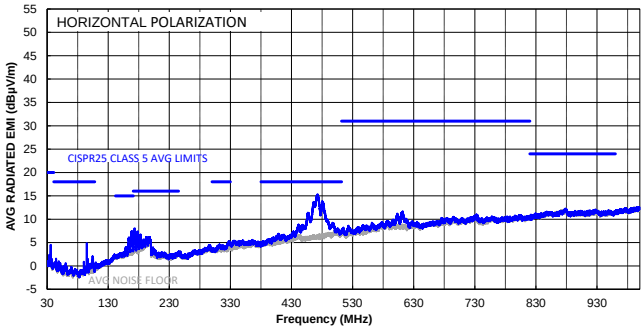
CISPR 25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 1GHz



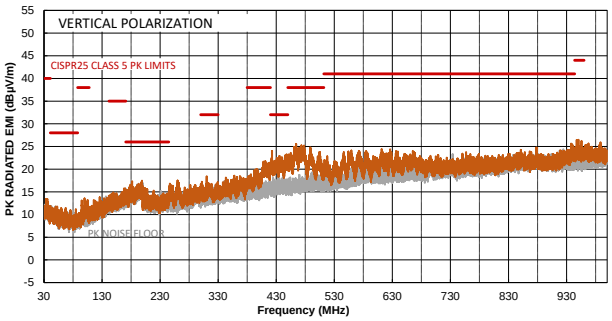
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted. (10)

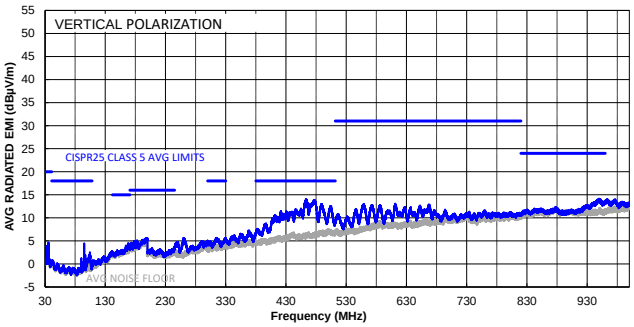
CISPR 25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR 25 Class 5 Average Radiated Emissions

Vertical, 30MHz-1GHz



Note:

10) The EMC test results are based on the typical application circuit with EMI filters and without frequency spread spectrum (FSS) function (see Figure 17 on page 78).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

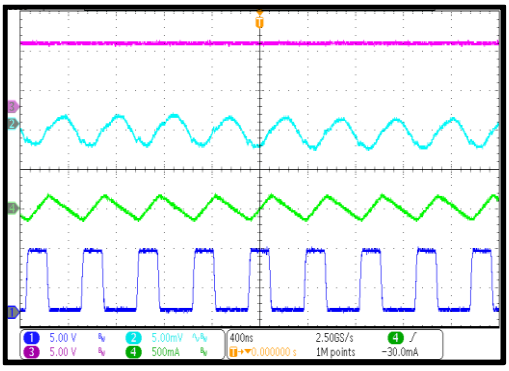
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

Steady State (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A

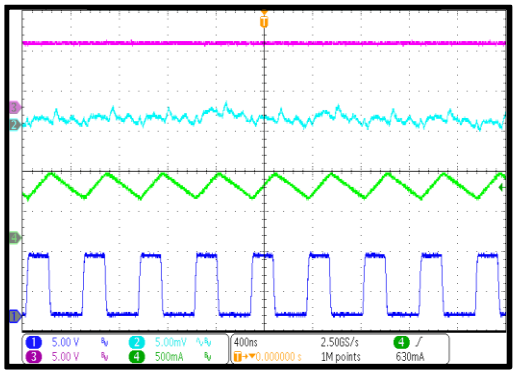
CH3: V_{IN}
CH2: V_{OUT1}/AC
CH4: I_{L1}
CH1: V_{SW1}



Steady State (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

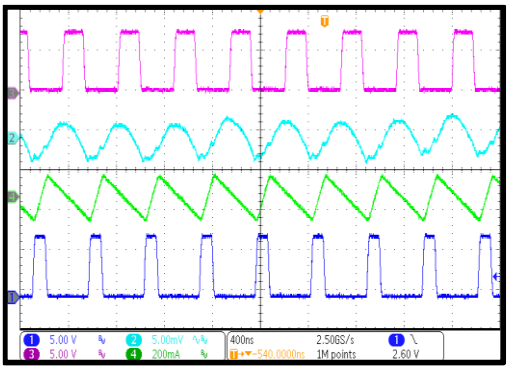
CH3: V_{IN}
CH2: V_{OUT1}/AC
CH4: I_{L1}
CH1: V_{SW1}



Steady State (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A

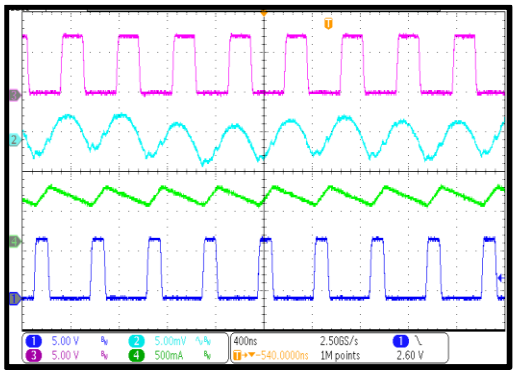
CH3: V_{SW1}
CH2: V_{OUT2}/AC
CH4: I_{L2}
CH1: V_{SW2}



Steady State (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

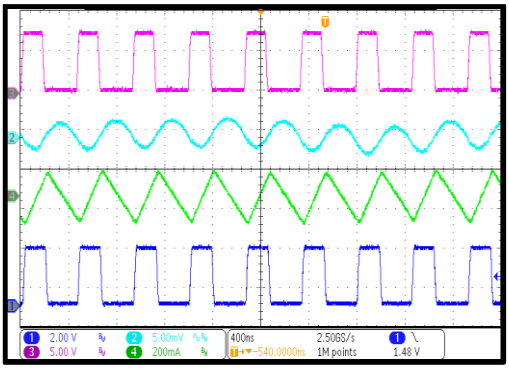
CH3: V_{SW1}
CH2: V_{OUT2}/AC
CH4: I_{L2}
CH1: V_{SW2}



Steady State (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A

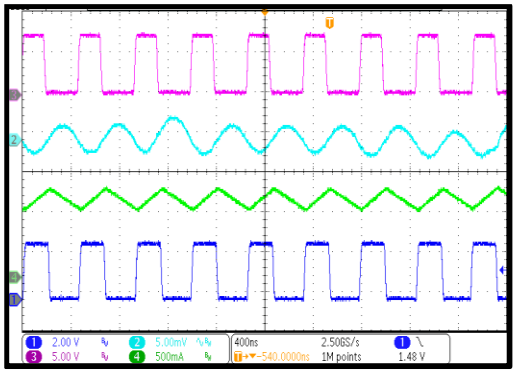
CH3: V_{SW1}
CH2: V_{OUT3}/AC
CH4: I_{L3}
CH1: V_{SW3}



Steady State (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA

CH3: V_{SW1}
CH2: V_{OUT3}/AC
CH4: I_{L3}
CH1: V_{SW3}



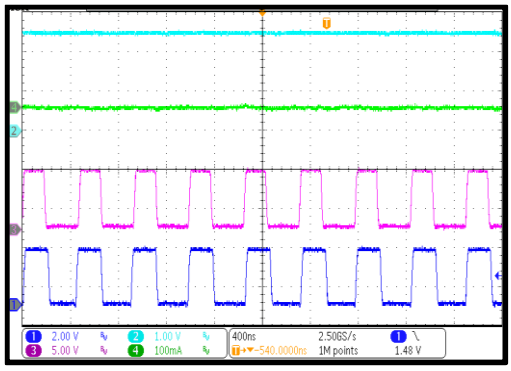
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

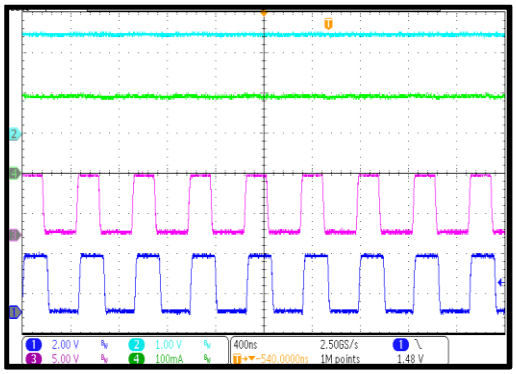
Steady State (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



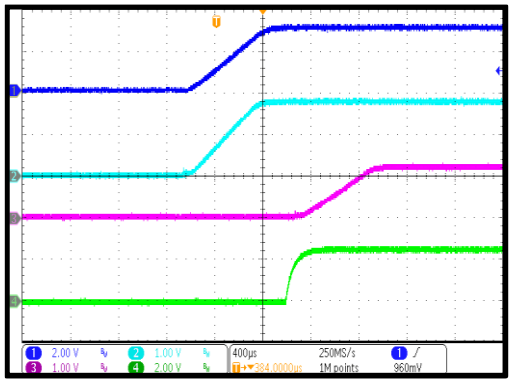
Steady State (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



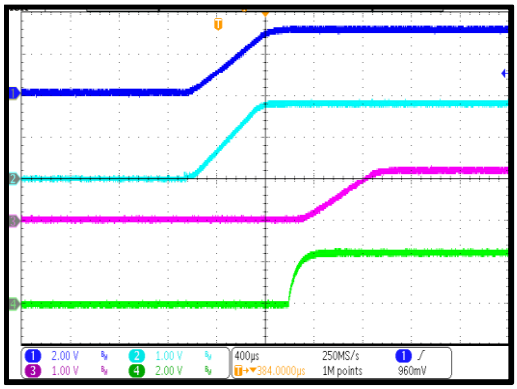
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



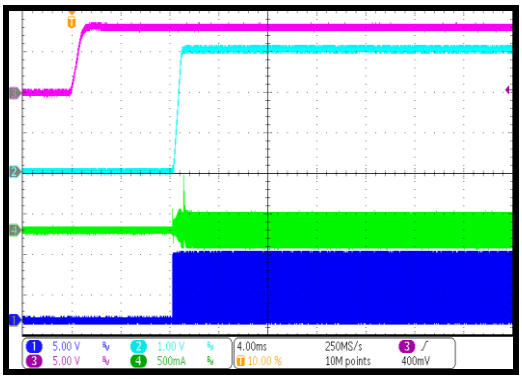
Start-Up through VIN (Start-Up Sequence)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



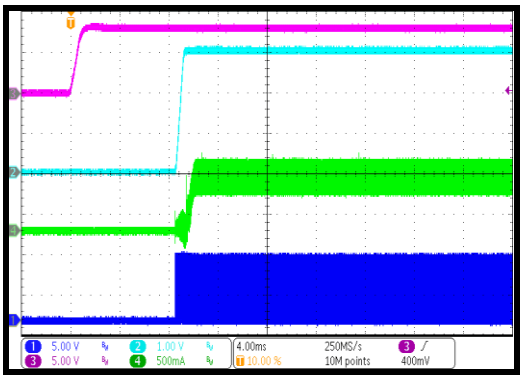
Start-Up through VIN (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



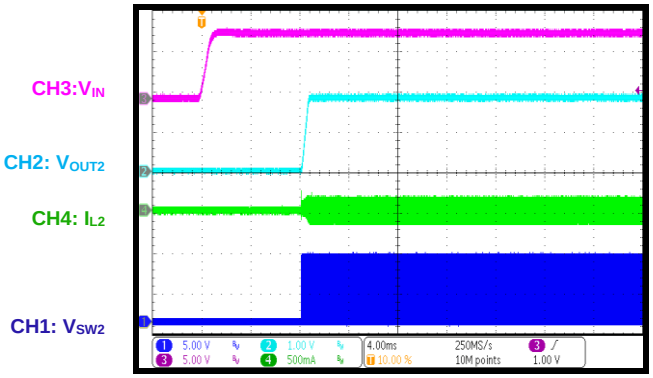
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

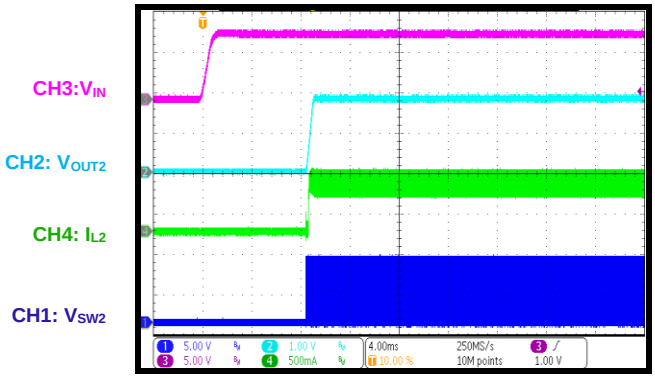
Start-Up through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



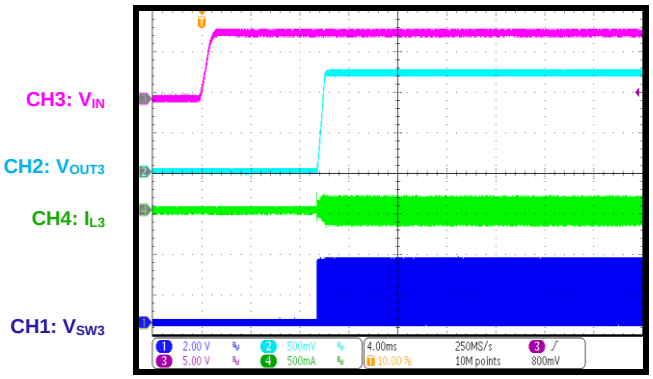
Start-Up through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



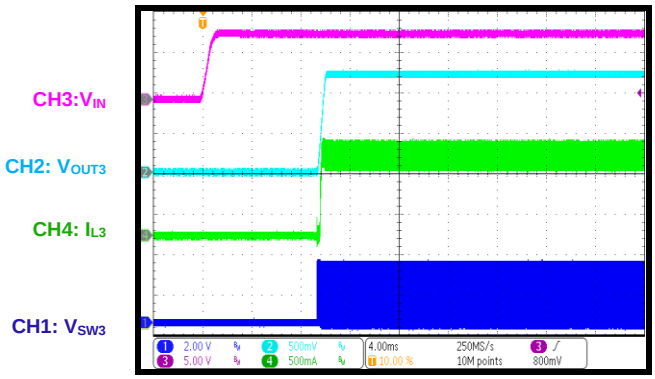
Start-Up through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



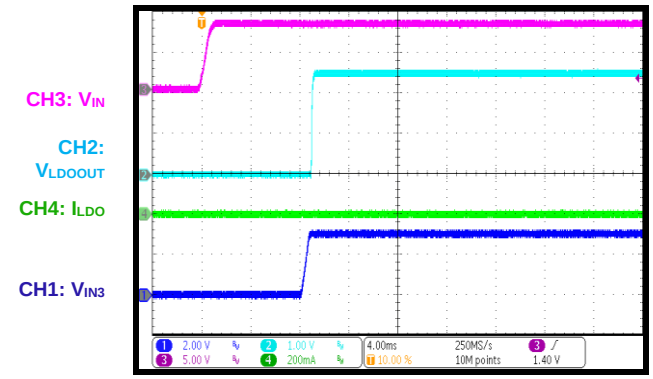
Start-Up through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



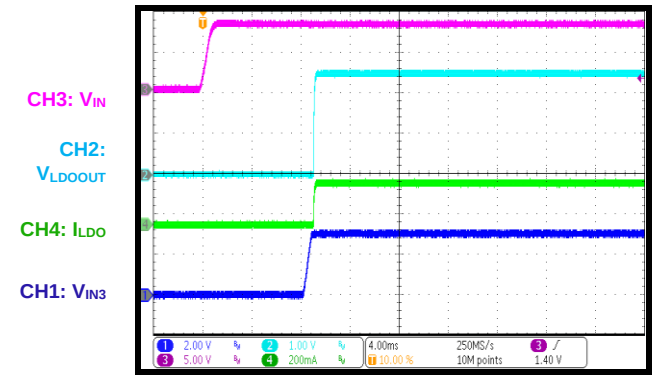
Start-Up through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Start-Up through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



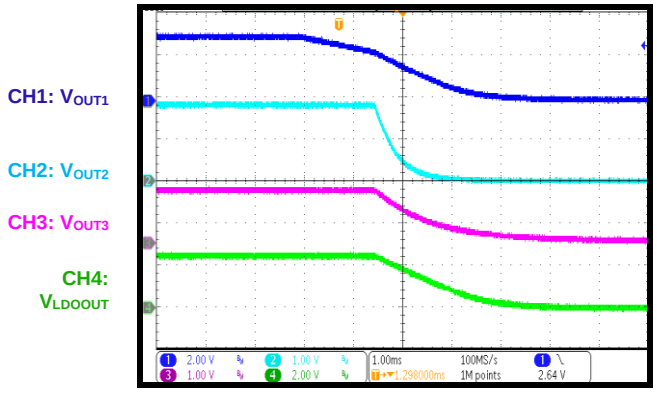
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

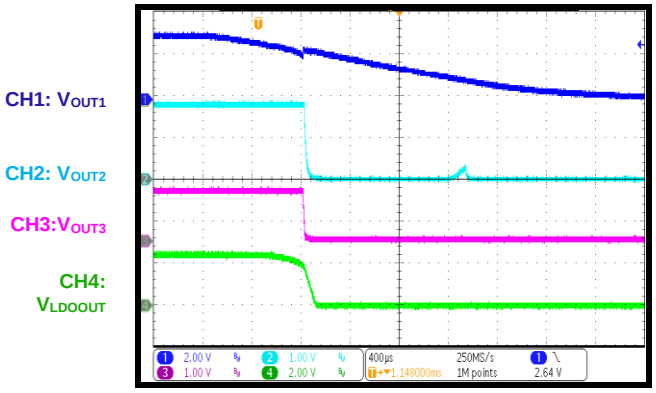
Shutdown through VIN

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



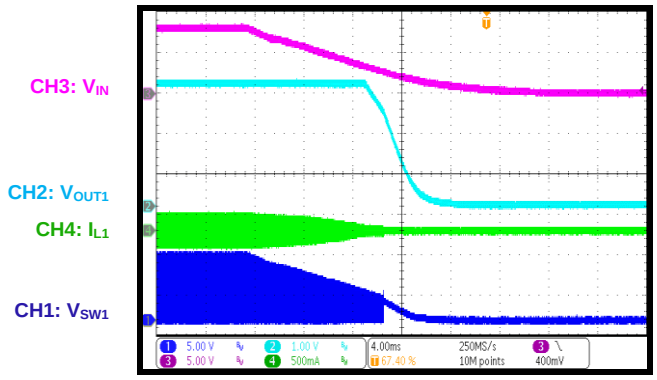
Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



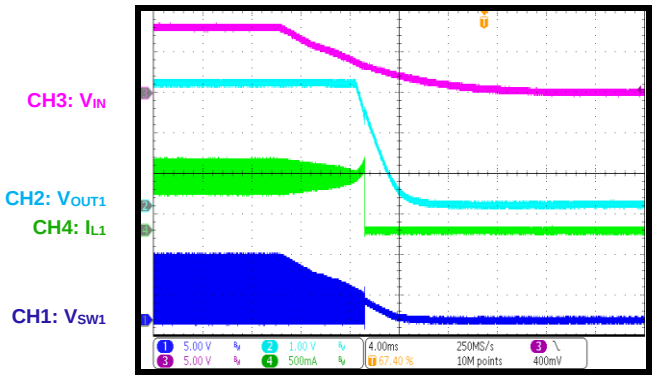
Shutdown through VIN (Buck 1)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



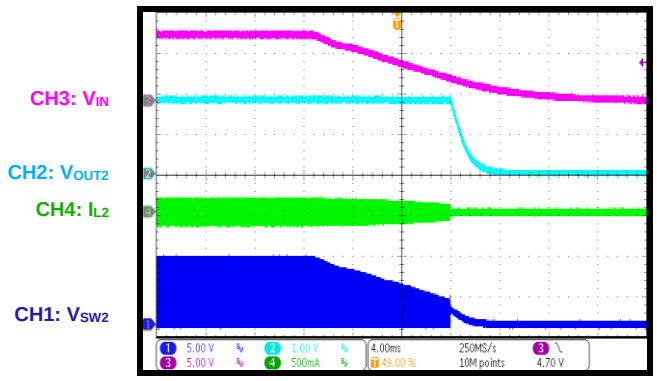
Shutdown through VIN (Buck 1)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



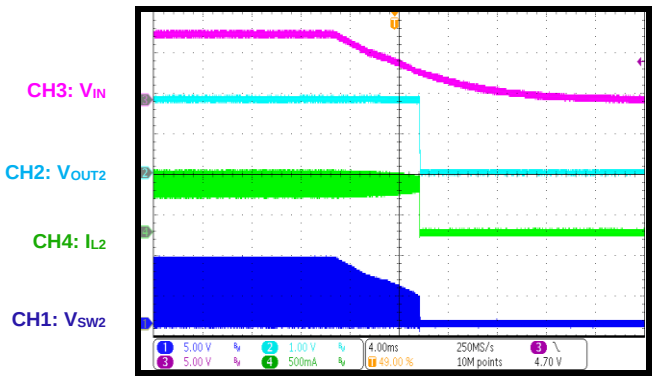
Shutdown through VIN (Buck 2)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



Shutdown through VIN (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



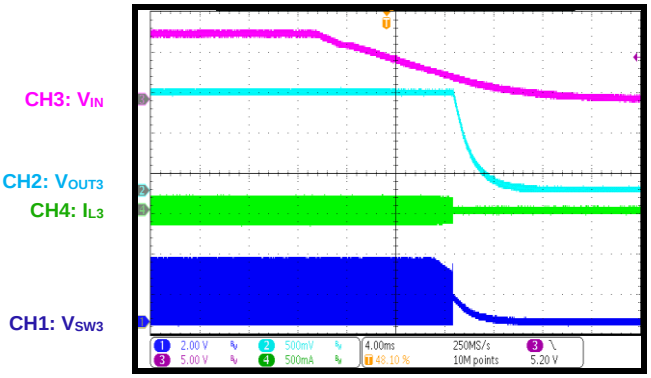
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

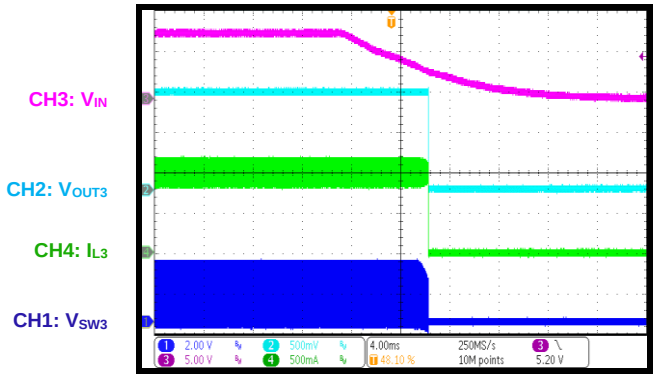
Shutdown through VIN (Buck 3)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



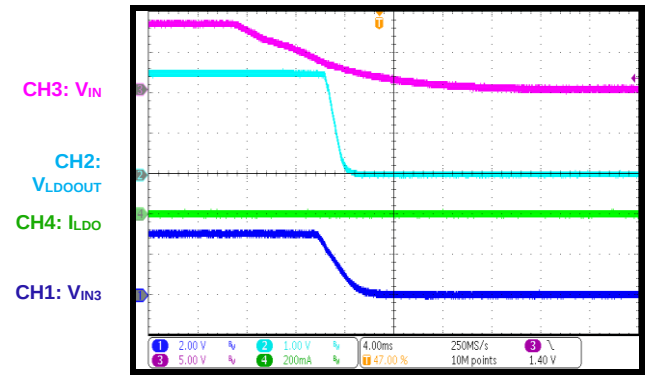
Shutdown through VIN (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



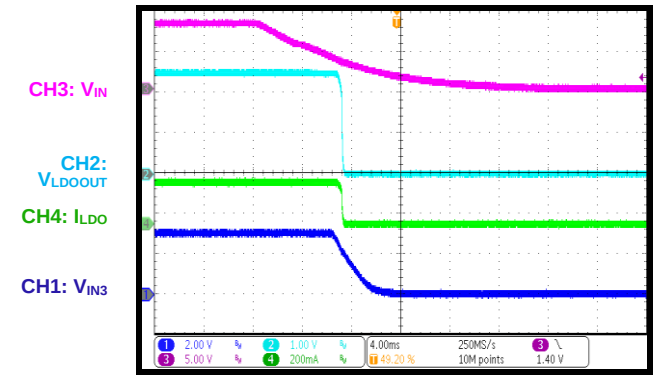
Shutdown through VIN (LDO)

I_{OUT1} = I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



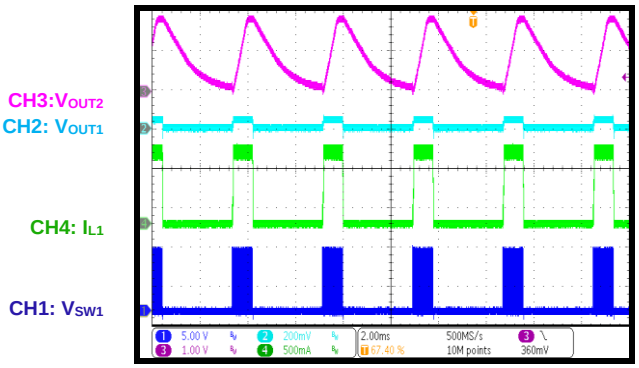
Shutdown through VIN (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



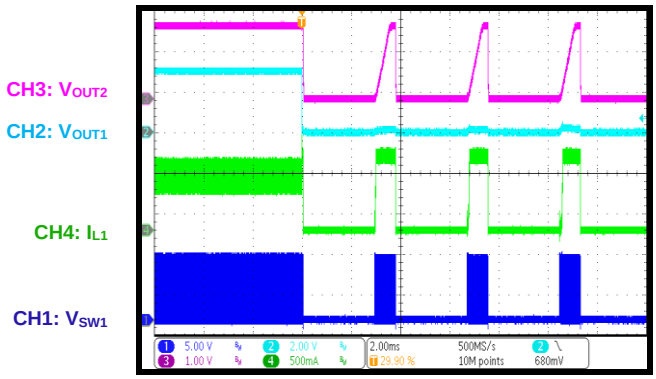
SCP Steady State (Buck 1)

Buck1 SCP, no SCP on other Channels



SCP Entry (Buck 1)

Buck1 SCP, no SCP on other Channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



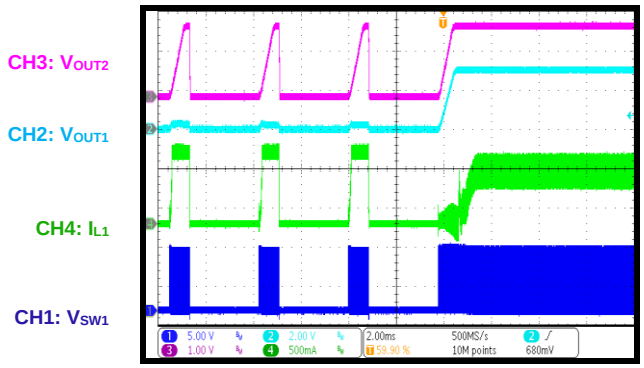
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

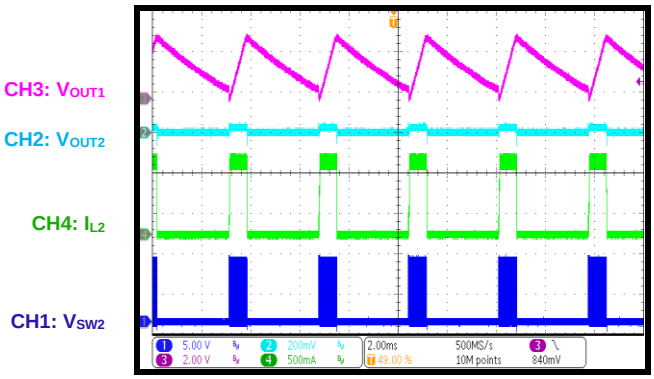
SCP Recovery (Buck 1)

Buck1 SCP, no SCP on other Channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



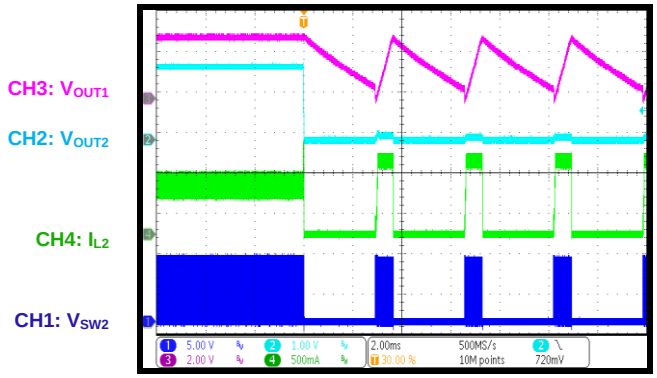
SCP Steady State (Buck 2)

Buck2 SCP, no SCP on other Channels



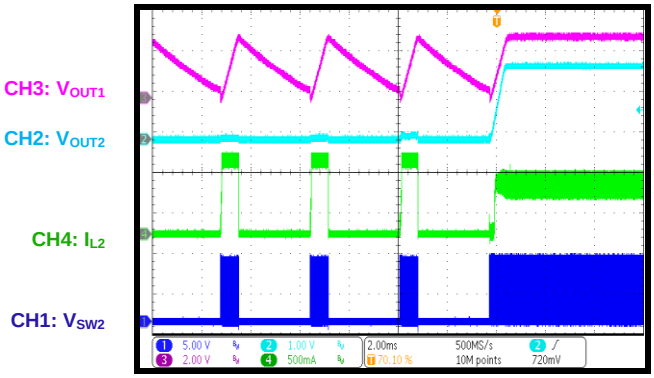
SCP Entry (Buck 2)

Buck2 SCP, no SCP on other Channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



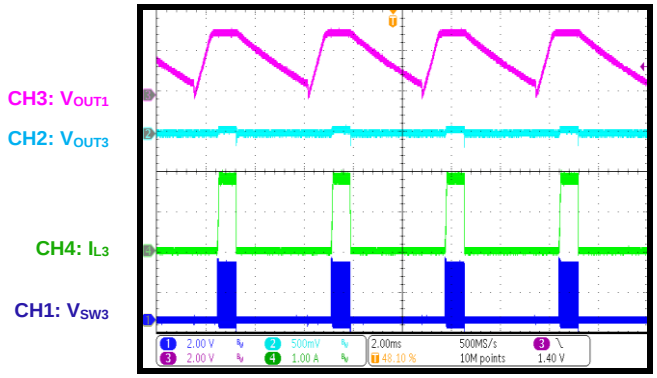
SCP Recovery (Buck 2)

Buck2 SCP, no SCP on other Channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



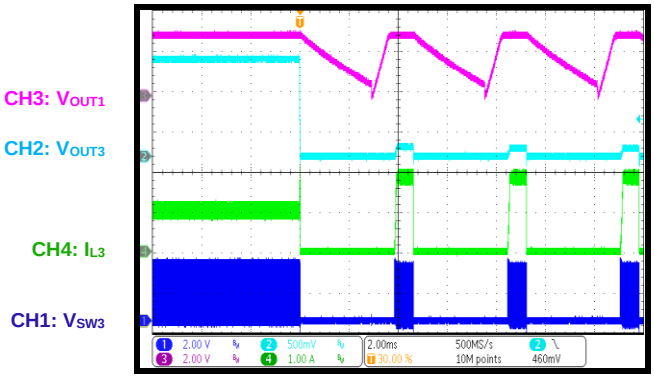
SCP Steady State (Buck 3)

Buck3 SCP, no SCP on other Channels



SCP Entry (Buck 3)

Buck3 SCP, no SCP on other Channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



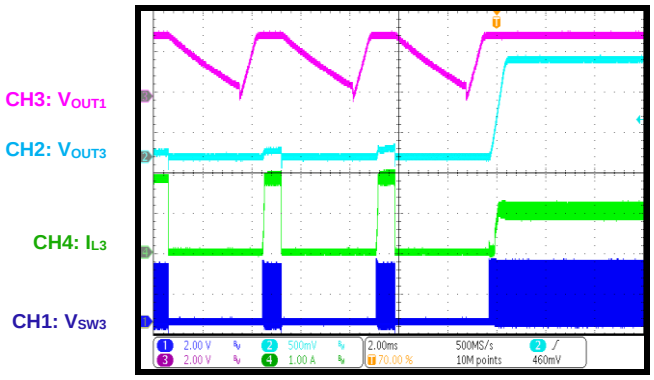
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

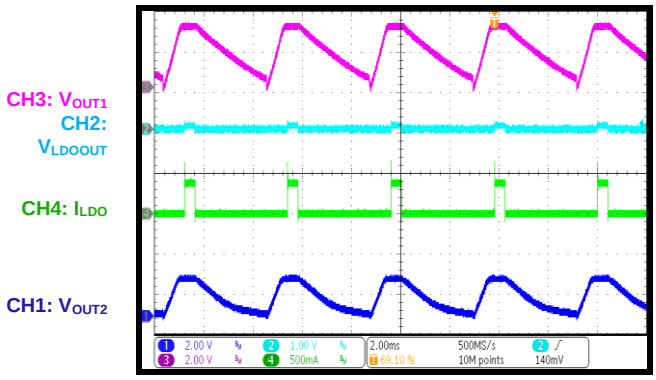
SCP Recovery (Buck 3)

Buck3 SCP, no SCP on other channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



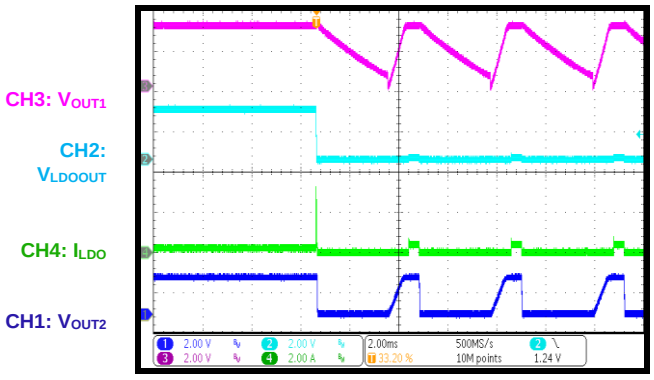
SCP Steady State (LDO)

LDO SCP, no SCP on other channels



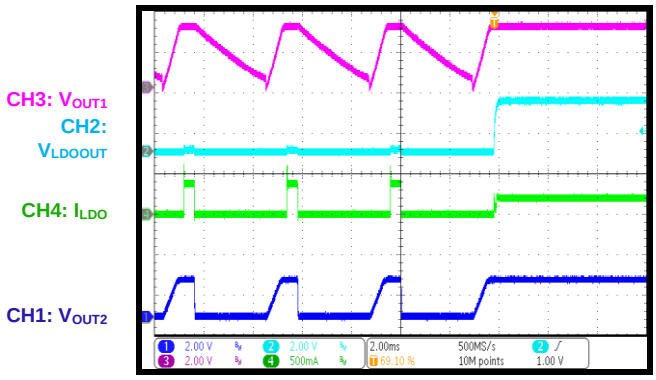
SCP Entry (LDO)

LDO SCP, no SCP on other channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



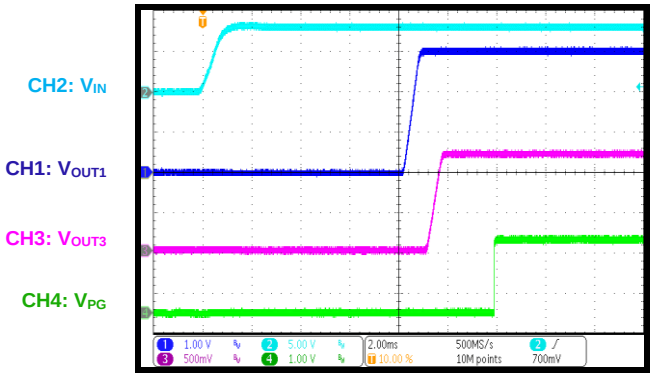
SCP Recovery (LDO)

LDO SCP, no SCP on other channels
I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



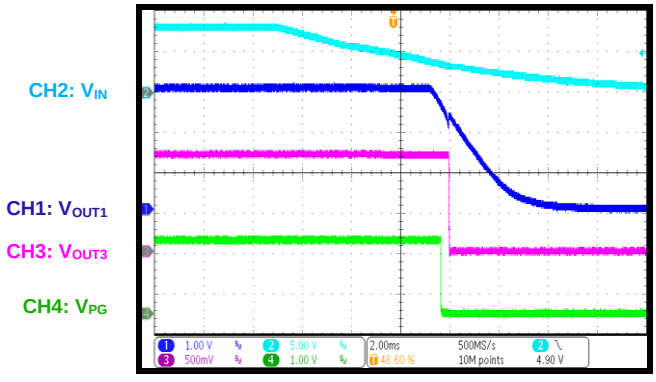
PG Start-Up through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



PG Shutdown through VIN

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A,
I_{LDO} = 200mA



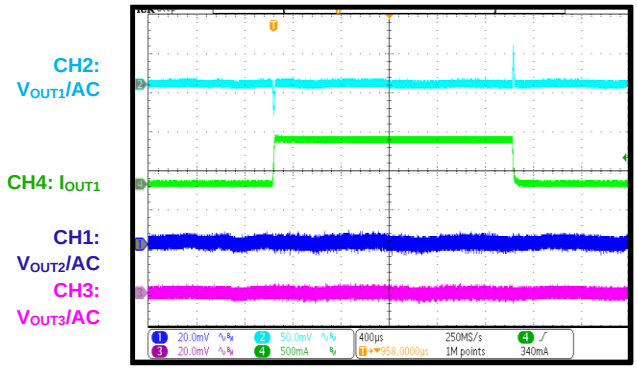
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 8V, V_{OUT1} = 3.0V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V, L1 = L2 = 2.2µH, L3 = 1µH, f_{SW1} = f_{SW2} = f_{SW3} = 2.2MHz, FCCM, T_A = 25°C, unless otherwise noted.

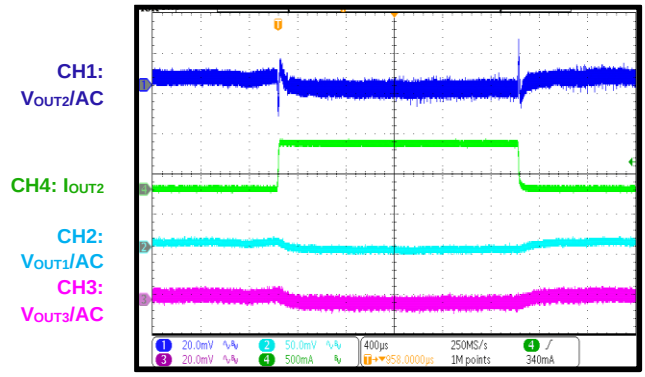
Load Transient Response (Buck 1)

I_{OUT1} = 0A to 600mA, I_{OUT2} = I_{OUT3} = I_{LDO} = 0A



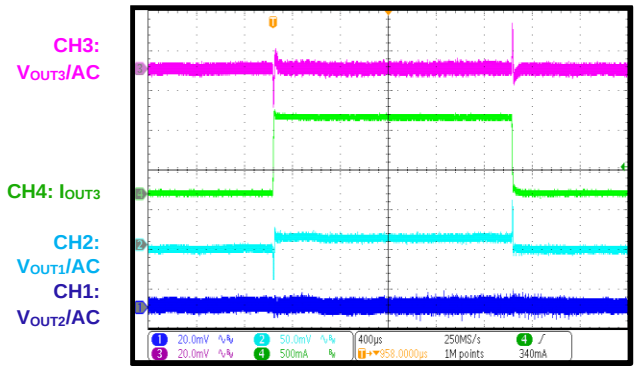
Load Transient Response (Buck 2)

I_{OUT1} = 0A, I_{OUT2} = 0A to 600mA, I_{OUT3} = 1A, I_{LDO} = 200mA



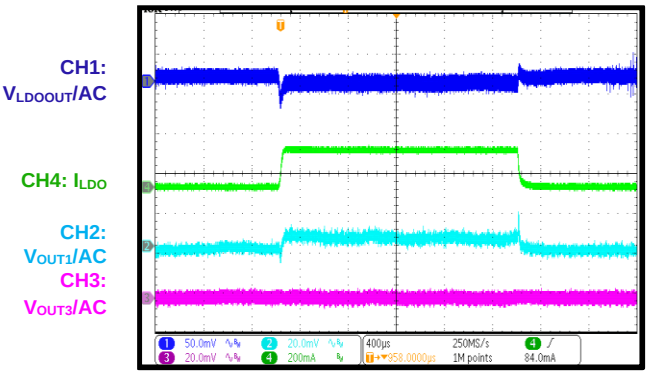
Load Transient Response (Buck 3)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 0A to 1A, I_{LDO} = 200mA



Load Transient Response (LDO)

I_{OUT1} = 0A, I_{OUT2} = 600mA, I_{OUT3} = 1A, I_{LDO} = 0A to 200mA



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

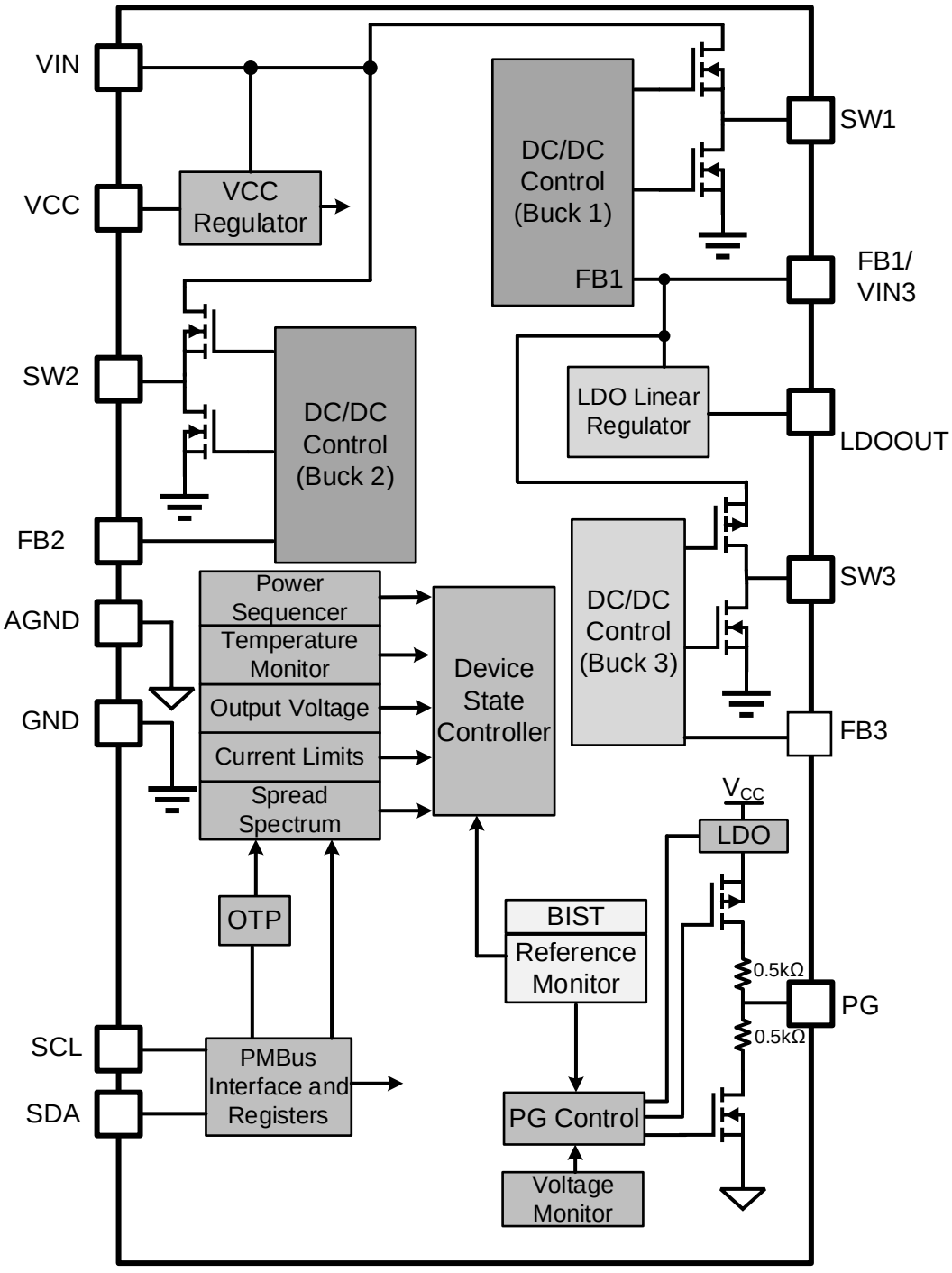
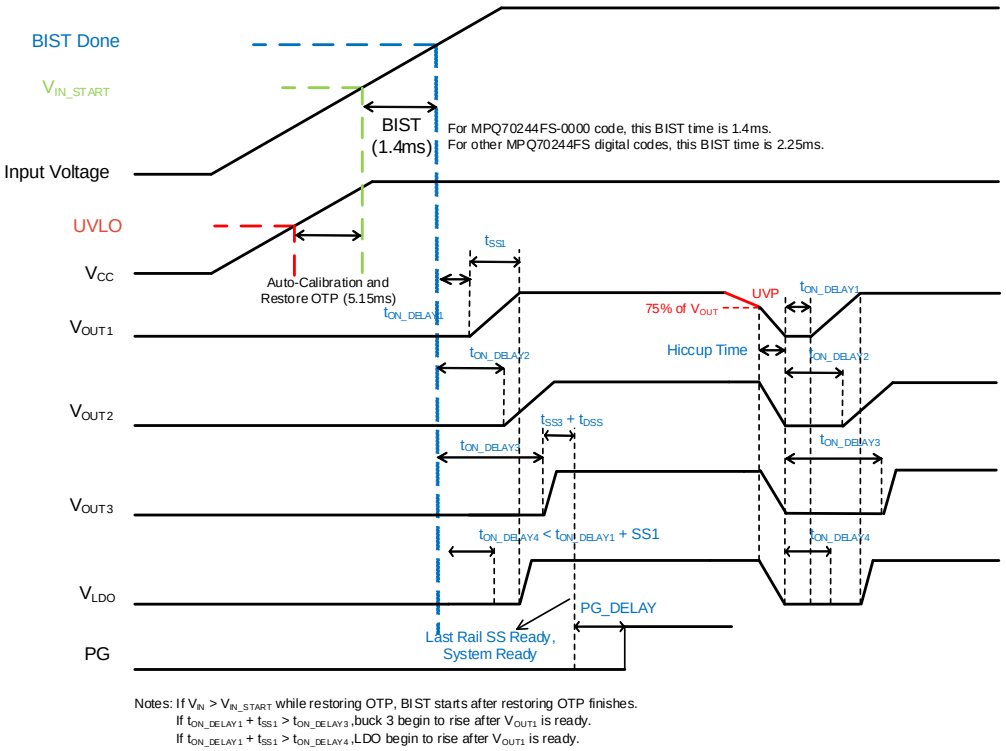


Figure 2: Functional Block Diagram

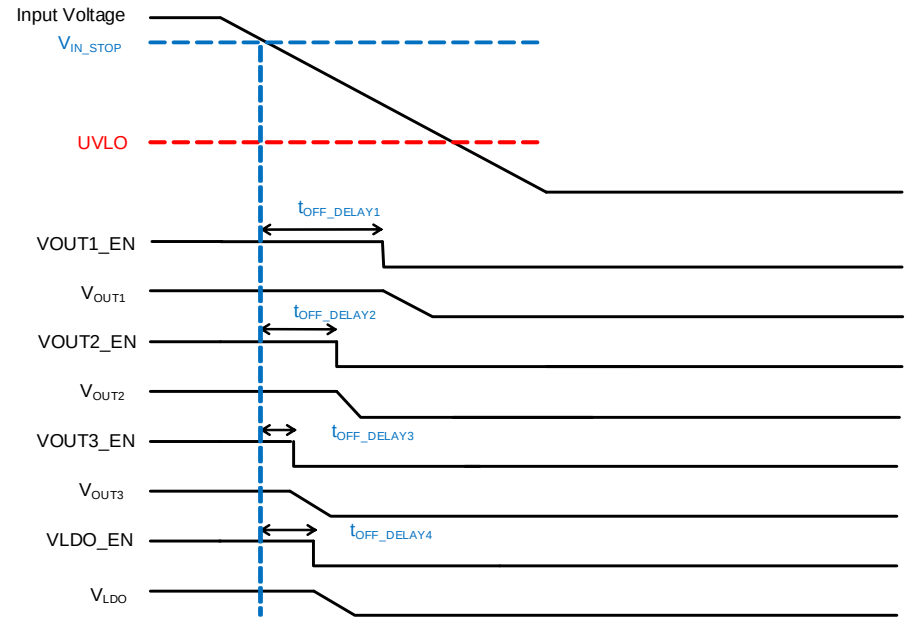
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

POWER-ON/OFF SEQUENCE



Notes: If $V_{IN} > V_{IN_START}$ while restoring OTP, BIST starts after restoring OTP finishes.
If $t_{ON_DELAY1} + t_{SS1} > t_{ON_DELAY3}$, buck 3 begin to rise after V_{OUT1} is ready.
If $t_{ON_DELAY1} + t_{SS1} > t_{ON_DELAY4}$, LDO begin to rise after V_{OUT1} is ready.

Figure 3: Power-On Sequence



Notes: The falling time depends on the load.
If the output discharge function is enabled, a pull-down resistor turns on after VOUTX_EN falls until UVLO.

Figure 4: Power-Off Sequence

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

OPERATION

The MPQ70244FS provides a complete power management solution for 8V automotive systems, such as satellite cameras. It integrates three high-frequency, synchronous, rectified, step-down switch-mode converters and a low-dropout (LDO) regulator. The MPQ70244FS greatly reduces PCB size due to its compact QFN-15 (2.5mmx3.5mm) package.

The PMBus interface provides an adjustable default output voltage (V_{OUT}), power-on sequence, and dynamic voltage scaling. It also provides powerful logic functions.

High-Efficiency Buck Converters

Buck converter 1 (buck 1), buck converter 2 (buck 2), and buck converter 3 (buck 3) are synchronous, step-down DC/DC converters that have built-in under-voltage lockout (UVLO), soft start (SS), compensation, and current-limit protection with hiccup mode. Fixed-frequency, constant-on-time (COT) control provides fast transient response. Both buck 1 and buck 2 are medium-voltage (MV) bucks, and their input is the input voltage (V_{IN}). Buck 3 is a low-voltage (LV) buck, and its input is buck 1's output.

Compared to fixed-frequency pulse-width modulation (PWM) control, constant-on-time (COT) control offers a simpler control loop and faster transient response. The internal clock's phase-locked loop (PLL) can ensure a fixed operating frequency. When the low-side MOSFET (LS-FET) turns on, it remains on for at least the high-side MOSFET (HS-FET) minimum off time (t_{OFF_MIN}). Then the HS-FET turns on when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}). After the HS-FET turns on for a calculated on time (t_{ON}), the LS-FET turns on.

The switching clock is phase-shifted from buck 1 to buck 2 during continuous conduction mode (CCM). Buck 1 is in phase with buck 3 during CCM.

LDOOUT

The MPQ70244FS supports an adjustable output and low-noise LDO output with over-voltage protection (OVP) and under-voltage protection (UVP). The LDO has an output that can be adjusted via the PMBus interface (from 0.6V to 3.75V, with 50mV/step). The LDO supports 200mA of output current (I_{LDO}) with over-current protection (OCP).

Power Supply and Under-Voltage Lockout (UVLO)

V_{IN} is the power supply for buck 1 and buck 2, as well as for the bias and internal logic blocks. V_{IN} generates the VCC voltage (V_{CC}) through a regulator, and V_{CC} supplies power to each internal module. FB1/VIN3 is the feedback of buck 1, as well as the power supply for buck 3 and LDOOUT. If buck 1 is disabled via the PMBus interface, the buck 3 and the LDO outputs shut down.

When V_{IN} is below its UVLO threshold and V_{CC} exceeds its UVLO threshold, the MPQ70244FS turns off all outputs (each channel turns off one by one according to the set shutdown sequence). If the output discharge function is enabled, the energy of the output capacitor (C_{OUT}) is released through the internal discharge path during shutdown. The MPQ70244FS reacts similarly to how it would if V_{IN} was below V_{IN_STOP}, but V_{CC} exceeds its UVLO threshold.

When V_{CC} is below its UVLO threshold, the MPQ70244FS turns off all outputs at the same time. During the shutdown process, the internal discharge path is not open, even if the output discharge function is enabled.

Internal Soft Start (SS)

The soft-start function is implemented to prevent the MPQ70244FS's V_{OUT} from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage (V_{REF}). At this point, V_{REF} is used by the error amplifier. The soft-start time (t_{SS}) for each buck can be adjusted. See the TON_RISE (61h on Pages 0, 1, and 2) section on page 44, page 55, and page 59, for more details. The LDO's soft-start time depends on the output capacitor and I_{OUT} during start-up. See Equation (8) on page 75 for more details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Light-Load Operation

The MPQ70244FS supports two light-load operation modes: continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

In DCM, the inductor current stays above 0A. After the HS-FET turns on for a calculated t_{ON}, the LS-FET turns on. The LS-FET stays on until I_L reaches the zero-current detection (ZCD) threshold. Then the LS-FET turns off and enters a high-impedance (Hi-Z) state. When V_{FB} drops below V_{REF}, the HS-FET turns on and stays on for the calculated t_{ON}.

In CCM, I_L can be negative, so the LS-FET stays on due to ZCD. After the HS-FET turns on for a calculated t_{ON}, the LS-FET turns on. When V_{FB} drops below V_{REF}, the HS-FET turns on and stays on for t_{ON}.

Output Discharge

To discharge the energy of C_{OUT} during the power-off sequence, there is an active discharge path from the bucks and the LDO output to ground. The discharge path turns on when the corresponding channel is disabled. It is recommended to fully discharge all the outputs before beginning a new start-up sequence.

Built-In Self-Testing (BIST) and Configuration Loading

The MPQ70244FS integrates several diagnostic features to improve system safety. If enabled, several built-in self-test (BIST) functions run in the BIST state before the power-on sequence begins. These functions are described below.

- PMBus interface protocol packet error checking (PEC): Data transferring through the PMBus interface includes a PEC code. The slave device rejects receiving data if the master device sends an incorrect PEC value (failure). PEC is an optional function that can be selected via the PMBus interface.
- Analog built in self-testing (ABIST): ABIST ensures that the OV, UV, and reference comparators operate normally. If any diagnostic function detects a failure during the power on state, the power good flag asserts and the corresponding fault bit is set to 1. Once the fault has been cleared, the device restarts all channels according to the power-on sequence. If any diagnostic functions detect a failure during the BIST state, the device restarts BIST at the ending of its current BIST, and the corresponding fault bit is set to 1.
- One-time programmable (OTP) memory cyclic redundancy check (CRC): During the power off state, and after the non-volatile memory (NVM) is read into the working registers, the CRC code is checked. If the CRC code does not match the previous CRC code, a memory fault is indicated. During the BIST state, the OTP CRC code is checked again. Load the data from the OTP for the CRC calculation. If the CRC code does not match the previous CRC code, a memory fault is indicated, and BIST restarts at the end of the current BIST. During the power on state, the PMIC can set a continuous OTP CRC check by writing 0x06 to the D9h register. If there is an OTP CRC failure, the PG pin is pulled low, and a memory fault is indicated.
- Memory CRC: The memory CRC code is checked using CRC-8 (polynomial: $x^8 + x^6 + x^3 + x^2 + 1$), which checks 224 bits, including the user page and trimming page. During power on, the MPQ70244FS can set a continuous memory CRC by writing 0x05 to the D9h register. If there is a memory CRC failure, PG pulls low, and a memory fault is indicated.
- Reference monitor: A second reference continuously monitors the main reference. If the main reference is out of its tolerance window, the PG flag asserts, and the reference fault bit is set to 1. If the reference returns to compliance and the fault register is cleared, the PG flag de-asserts.

Power Good (PG)

The PG pin is a push-pull output that pulls logic high when the device is powered on, all outputs are within the PG range, and no other faults occur. The high output level can be set to either 3.3V or 1.8V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PG asserts if any of the below events occur:

- Buck 1's output is out of its V_{OUT1} OVP/UVP threshold
- Buck 2's output is out of its PG range
- Buck 3's output is out of its PG range
- The LDO output is out of its PG range
- Thermal warning/shutdown
- The LDO enters its dropout region
- Over-current (OC) failure
- Reference check failure
- BIST failure
- PMBus interface communication failure
- PMBus interface CRC failure
- Register write check error
- $V_{IN} < V_{IN_STOP}$
- $V_{CC} < V_{CC_UVLO_FALLING}$

These errors force PG to pull down. If the error is removed, PG pulls up after a delay. The PG de-assertion delay time is configurable. If PG is pulled down because of shutdown events, wait until the error is gone, all channels have finished starting, and for the PG de-assertion time to finish before PG pulls up.

Certain events can be masked (see Table 1). The PG_MAPPING (C5h) register can determine whether PG is masked for these faults.

Table 1: Maskable Fault Types

Fault Type	PG Asserts?	
	PG Masked	PG Not Masked
BIST Failure	No	Yes
PMBus Interface Communication Failure	No	Yes
PMBus Interface CRC Failure	No	Yes
Reference check Failure	No	Yes

PG does not indicate the output for disabled channels. If SAFETY_CONFIG (CBh), bit[1] = 1, the MPQ70244FS shuts down when PG goes low.

Over-Voltage Protection (OVP)

If any buck's output or the LDO output exceeds the OVP threshold, all outputs shut down at the same time. The MPQ70244FS restarts BIST, and all outputs stay off for a hiccup time after BIST finishes. Then the normal start-up sequence starts again. If enabled, the output discharge function operates during the hiccup time.

Under-Voltage Protection (UVP)

If any buck's output or the LDO output falls below the UVP threshold, all outputs shut down at the same time. The MPQ70244FS restarts BIST, and all outputs stay off for a hiccup time after BIST finishes. Then the normal power up sequence starts again. If enabled, the output discharge function operates during the hiccup time.

Over-Current Protection (OCP)

For the three bucks, the MPQ70244FS provides a peak/valley current limit scheme designed to limit the peak/valley inductor current (I_L) to ensure that the switching currents remain within the device's capabilities during overload conditions or during an output short circuit.

When the HS-FET turns on, the device monitors the increased I_L through the relevant operating main power switch. Once the peak I_L exceeds the peak I_{LIMIT} threshold, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease I_L. The HS-FET does not turn on again until I_L falls below the valley I_{LIMIT} threshold. If I_L exceeds the peak I_{LIMIT} during the minimum t_{ON} (t_{ON_MIN}), the HS-FET does not turn off immediately, and it does not turn off until the end of t_{ON_MIN}.

If I_L does not fall below the valley I_{LIMIT} during the off time (the LS-FET turns on), or the peak I_L exceeds I_{LIMIT} during t_{ON} (HS-FET turns on) and lasts longer than the deglitch time, then an OC fault is recorded and OCP is activated.

For the LDO, an internal, fixed LDO I_{LIMIT} can ensure that the LDO's current remains within the device's capabilities during overload conditions or during an output short circuit.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

If any channel triggers an OC fault, all outputs shut down at the same time and stay off for the hiccup time. If enabled, the output discharge function operates during shutdown. Then the normal start-up sequence starts again with a configured turn-on delay. Bucks 1, 2, and 3 start according to the set t_{SS}, and the LDO determines the rising rate according to its load and capacitance. If no channel triggers OCP at the end of soft start, then the MPQ70244FS resumes normal operation.

Gate Drive Strength Control

To improve electromagnetic interference (EMI) performance, the MPQ70244FS has 4 options set via GATE_DRIVE_STRENGTH (CDh) to adjust the SW1 and SW2 slew rate by adjusting the gate drive ability. EMI can be improved with a slower SW1 and SW2 slew rate, though this is a tradeoff that reduces efficiency.

Frequency Spread Spectrum (FSS)

To further optimize EMI performance, the MPQ70244FS features frequency spread spectrum (FSS) (see Figure 5).

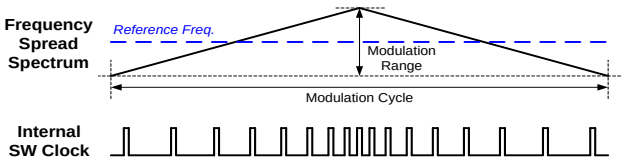


Figure 5: Frequency Spread Spectrum

The reference frequency and frequency spread spectrum modulation range can be set via the PMBus interface. Once frequency spread spectrum is enabled, the triangular frequency modulation mode varies the switching frequency between a maximum and minimum value that is related to the reference value.

See the FREQUENCY_DITHER (C4h) section on page 48 for more information.

Thermal Warning and Shutdown

PG asserts low and a thermal warning (TWN) fault is recorded if the silicon die temperature exceeds its upper threshold (about 125°C). PG de-asserts when the temperature drops below its lower threshold (about 105°C). If needed, contact an MPS FAE to configure PG so that it does not pull low when a TWN fault occurs.

Thermal shutdown is implemented to protect the chip from thermal runaway. If the silicon die temperature exceeds its upper threshold (about 170°C), the device and power MOSFETs shut down. If the temperature drops below its lower threshold (about 150°C), the thermal shutdown condition is removed, and the chip is enabled again.

One-Time Programmable (OTP) Memory

The MPQ70244FS provides an OTP memory function to set custom default parameters.

MPS provides a GUI (Virtual Bench Pro 4.0) and PMBus interface tool (EVKT-USBI2C-02) to configure the MPQ70244FS during the development process. Contact an MPS FAE to configure in application.

Only the MPQ70244FS-0000 code can be configured via the OTP once. Other codes cannot be configured via the OTP. The OTP can be written once via the STORE_USER_ALL (15h) command. See the STORE_USER_ALL (15h) section on page 43 for more details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

POWER CONTROL

Figure 6 shows several states of the MPQ70244FS and the transition conditions between each state. The state machine's statuses are described below.

No Supply

The PMIC has a UVLO detection circuit. If V_{CC} is below its UVLO rising threshold, all of the MPQ70244FS's functions are disabled.

Power Off

All power rails turn off. When V_{CC} exceeds its rising UVLO threshold, the MPQ70244FS enters a power off state. The digital block is reset and the MPQ70244FS loads its OTP data in the register.

Built-In Self-Testing (BIST)

If V_{IN} exceeds V_{IN} start voltage (V_{IN_START}), the BIST is performed. BIST includes analog built-in self-testing (ABIST) and OTP CRC calculation. ABIST consists of a self-check for the PGOV, PGUV and reference monitor comparators. Buck 2, buck 3, and the LDO have the PGOV and PGUV comparators, Buck 1 does not have these comparators. After BIST is finished, the device enters the power on state once V_{IN} exceeds V_{IN_START}.

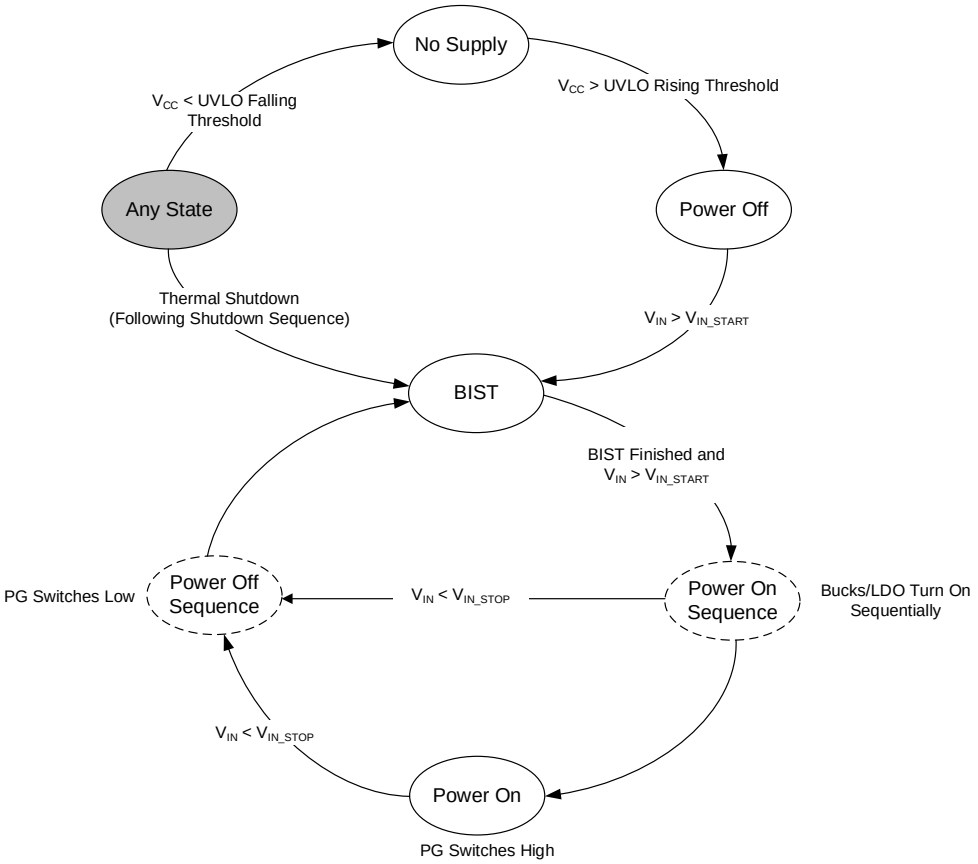


Figure 6: State Machine of the MPQ70244FS

Power-On Sequence

The start-up delay for the bucks and LDO can be configured via the OTP. Each output turns on after its configured delay. The bucks and the LDO turn on once their pre-configured on-time delay set by ON_DELAY (TON_OFF_DELAY (CFh), bits[7:4]) finishes. Buck 3 and the LDO must wait until buck 1 rises to its nominal output, then they begin to start up after a delay time. Figure 7 on page 36 shows a diagram of the correct start-up sequence.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

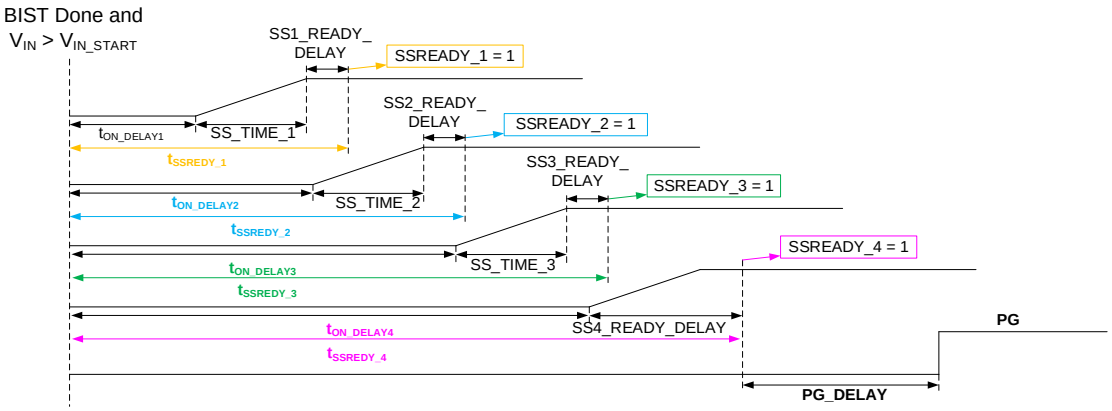


Figure 7: Power-On Sequence Diagram

Power On

In this stage, the bucks and LDO are on. The power good (PG) pin switches high while the outputs are within their defined thresholds.

Power-Off Sequence

The device enters this sequence when it detects that V_{IN} is below V_{IN_STOP} in a power-on state, or during the power-on sequence period. The bucks and LDO turn off once the pre-configured OFF_DELAY bits elapse for that output (see Figure 8). If a shutdown event occurs, the bucks and LDO turn off at the same time.

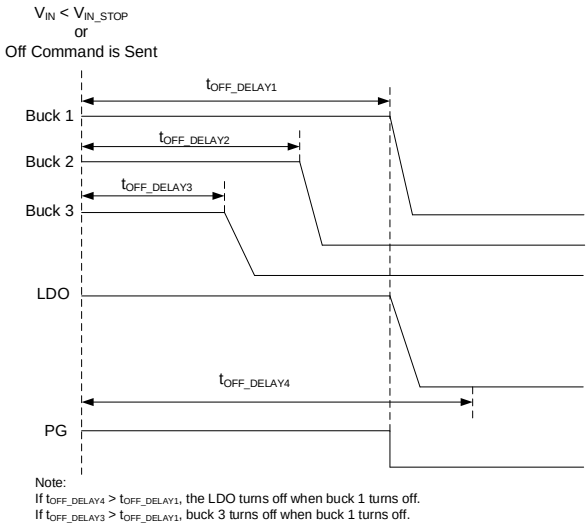


Figure 8: Power-Off Sequence Diagram

Shutdown Event

If the device detects a shutdown condition, it shuts down all channels at the same time and changes the current state. Table 2 shows certain shutdown events.

Table 2: Shutdown Event

Fault Type	Result
V_{CC} < UVLO falling threshold	Enter no supply state
V_{IN} < UVLO falling threshold and V_{CC} > UVLO falling threshold	Wait V_{IN} > V_{IN_START} again
Thermal shutdown	Enter BIST state
ABIST fault during BIST	Enter BIST state
OTP CRC fault during BIST	Enter BIST state
Memory CRC fault	Enter BIST state
V_{OUT} over-voltage (OV) fault	Enter BIST state
V_{OUT} under-voltage (UV) fault	Enter BIST state
Over-current (OC) fault	Enter BIST state
Reference fault	Enter BIST state

If PG_REACTION = 1, there are additional shutdown events when PG goes low (see Table 3).

Table 3: Additional Shutdown Events

Fault Type	Result
V_{OUT} PGOV Fault	Enter BIST state
V_{OUT} PGUV Fault	Enter BIST state
PMBus Interface Communication Error	Enter BIST state
PMBus Interface CRC Failure	Enter BIST state
Thermal Warning	Enter BIST state
LDO Enters the Dropout Range	Enter BIST state

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PMBUS INTERFACE

PMBus Interface Description

The PMBus interface is an open-standard, power management protocol that defines a means of communication with power conversion and other devices. The digital bus is a 2-wire, bidirectional serial interface, consisting of a serial data line (SDA) and a serial clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. Connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence.

The MPQ70244FS works as a slave-only device that supports standard mode (100kbps), fast mode (400kbps), and fast mode plus (1Mbps) bidirectional data transfer, adding flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be instantaneously controlled via the PMBus interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 9).

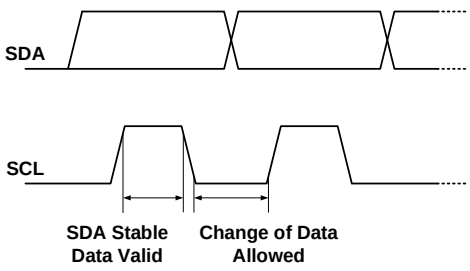


Figure 9: Bit Transfer

Start and Stop Commands

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the PMBus interface transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 10).

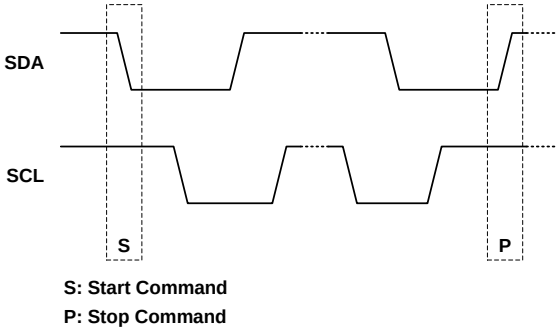


Figure 10: Start and Stop Command

Start and stop commands are always generated by the master. The bus is considered busy after the salve address command. The bus is considered free again after a certain time after the stop command. The bus stays busy if a repeated start is generated instead of a stop command. The start and repeated start commands are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the ACK clock pulse. The receiver must pull down the SDA line during the ACK clock pulse, so that it remains stable low during the high period of the clock pulse.

Figure 11 shows the data transfer format. After the start command, a slave address is sent. This address is 7 bits long followed by an eighth bit, which is a data direction bit (R/W). A “0” indicates a transmission (write), while a “1” indicates a request for data (read). A data transfer is terminated by a stop command, which is generated by the master. However, if the master still wishes to communicate on the bus, it can generate a repeated start command and address another slave without first generating a stop command.

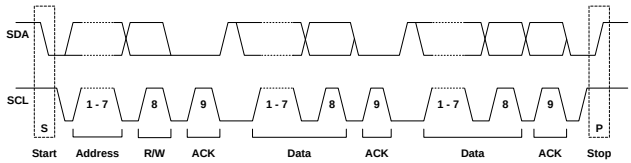


Figure 11: A Complete Data Transfer

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Packet Error Checking (PEC)

The PEC mechanism is employed to improve communication reliability and robustness. When applicable, PEC is implemented by appending a packet error code after the data of each message transfer. The PEC is a CRC-8 error-checking byte (where $C(x) = x^8 + x^2 + x^1 + 1$), calculated on all the message bytes (including addresses and read/write bits). The PEC is appended to the message by the device that supplied the last data byte.

If an incorrect PEC is received, a communication fault is triggered, and the PG flag asserts until the fault register is cleared.

PMBus Interface Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults, which are listed below:

- Sending too little data
- Reading too little data
- The host sends too many bytes
- The host reads too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

The communication failure is recorded in the STATUS_CML (7Eh) register.

Read/Write Sequence

All PMBus interface commands are supported by the MPQ70244FS. Figure 12 shows the read/write (R/W) sequence without PEC. Figure 13 on page 38 shows the read/write sequence with PEC. There are five commands that can be implemented with or without PEC:

1. Send command only
2. Write byte
3. Write word
4. Read byte
5. Read word

If the master sends a write command to a read-only register, the MPQ70244FS performs the same action as it would if the host has sent too many bytes. If the master sends a read command from a write-only register, the MPQ70244FS performs the same action as it would if the host read too many bytes.

Chip Address

The MPQ70244FS supports 16 addresses, which can be set via the ADDRESS (D3h) register. The default 7-bit address is 03h.

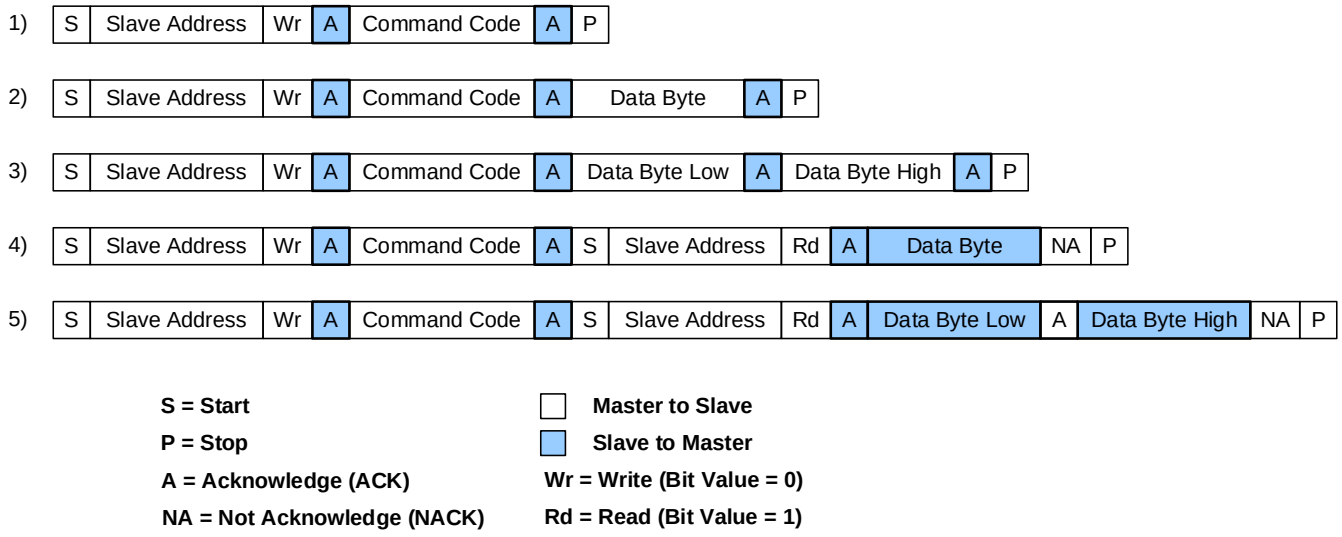


Figure 12: Read/Write Sequence without PEC

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

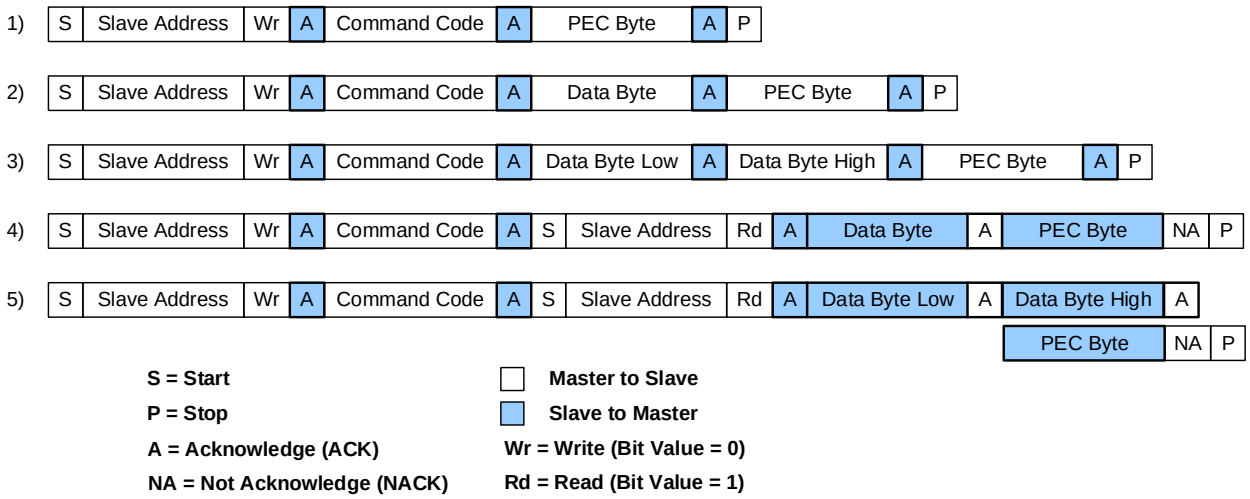


Figure 13: Read/Write Sequence with PEC

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER MAP

Command Code (11)	Command Name	Type	Bytes	Page 0 (Rail 1)	Page 1 (Rail 2)	Page 2 (Rail 3)	Page 3 (Rail 4)	Page FF (All Rails) (12)
00h	PAGE	R/W	1	✓	✓	✓	✓	✓ (13)
01h	OPERATION	R/W	1	✓	✓	✓	✓	✓
03h	CLEAR_FAULTS	Send	0	✓	-	-	-	✓
10h	WRITE_PROTECT	R/W	1	✓	-	-	-	✓
15h	STORE_USER_ALL	Send	0	✓	-	-	-	✓
16h	RESTORE_USER_ALL	Send	0	✓	-	-	-	✓
19h	CAPABILITY	R	1	✓	-	-	-	-
20h	VOUT_MODE	R	1	✓	-	-	-	-
21h	VOUT_COMMAND	R/W	2	✓	✓	✓	✓	✓
61h	TON_RISE	R/W	2	✓	✓	✓	-	✓
78h	STATUS_BYTE	R	1	✓	✓	✓	✓	-
79h	STATUS_WORD	R	2	✓	✓	✓	✓	-
7Ah	STATUS_VOUT	R	1	✓	✓	✓	✓	-
7Bh	STATUS_IOUT	R	1	✓	✓	✓	✓	-
7Dh	STATUS_ TEMPERATURE	R	1	✓	-	-	-	-
7Eh	STATUS_CML	R	1	✓	-	-	-	-
80h	STATUS_MFR_ SPECIFIC	R	1	✓	-	-	-	-
C4h	FREQ_DITHER	R/W	1	✓	-	-	-	✓
C5h	PG_MAPPING	R/W	1	✓	-	-	-	✓
CBh	SAFETY_CONFIG	R/W	1	✓	-	-	-	✓
CCh	PG_CONFIG	R/W	1	✓	-	-	-	✓
CDh	GATE_DRIVE_ STRENGTH	R/W	1	✓	-	-	-	✓
CEh	LIGHT_LOAD	R/W	1	✓	-	-	-	✓
CFh	TON_OFF_DELAY	R/W	1	✓	✓	✓	✓	✓
D0h	TON_OFF_SCALE	R/W	1	✓	-	-	-	✓
D1h	FREQUENCY_ILIM_ SCALE	R/W	1	✓	-	-	-	✓
D2h	VIN_START_STOP	R/W	1	✓	-	-	-	✓
D3h	ADDRESS	R/W	1	✓	-	-	-	✓

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REGISTER MAP *(continued)*

Command Code (11)	Command Name	Type	Bytes	Page 0 (Rail 1)	Page 1 (Rail 2)	Page 2 (Rail 3)	Page 3 (Rail 4)	Page FF (All Rails) (12)
D4h	CONFIGURATION_ CODE	R	1	✓	-	-	-	-
D5h	MEMORY_CRC	R	1	✓	-	-	-	-
D6h	LATEST_PEC	R	1	✓	-	-	-	-
D7h	REGISTER_CRC	R	1	✓	-	-	-	-
D9h	MFR_OTP_MEM_ CHK	R/W	1	✓	-	-	-	✓
DAh	MFR_OTP_MEM_ STATUS	R	2	✓	-	-	-	-

Notes:

11) Only registers in this table are supported to read or write
12) Read commands are invalid, but write commands are valid.
13) Read and write commands are valid.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PAGE 0 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 0 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 0 configures buck 1's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	Enables buck 1's output. 1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page 0 clears any fault bits in the following status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), STATUS_CML (7Eh), and STATUS_MFR_SPECIFIC (80h).

This command is write-only. There is no data byte for this command. If a CLEAR FAULTS command is sent with any data, the MPQ70244FS does not perform the clear command and reports a communication error (COM_ERROR).

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command on Page 0 controls writing to the converter. The intent of this command is to provide protection against accidental changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	8'b10000000: Disable all writes except to the WRITE_PROTECT command 8'b 01000000: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 8'b 00100000: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 8'b 00000000: Enable writes to all commands. Others: Ineffective input

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

STORE_USER_ALL (15h)

The STORE_USER_ALL command on Page 0 instructs the MPQ70244FS to copy the contents from the operating memory to the matching locations in the OTP, excluding the trim registers. This process occurs when the MPQ70244FS receives a STORE_USER_ALL command from the PMBus interface.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command on Page 0 instructs the MPQ70244FS to copy the contents from the OTP and overwrite the matching locations in the operating memory, excluding the trim registers. Any items in the OTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the MPQ70244FS is operating. However, the MPQ70244FS may be unresponsive during the operation with unpredictable or undesirable results.

This command is write-only. There is no data byte for this command.

CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command on Page 0 provides 1 byte to return the key PMBus interface features that the MPQ70244FS can support.

Bits	Access	Bit Name	Description
7	R	PACKET_ERR_ CHECKING	1’b1: Packet error checking (PEC) is supported Others: Ineffective input
6:5	R	MAX_BUS_SPEED	2’b10: The maximum supported bus speed is 1MHz Others: Ineffective input
4	R	SMBALERT#	1’b0: The device does not have a SMBALERT# pin and does not support the SMBus alert response protocol Others: Ineffective input
3	R	NUMERIC_FORMAT	1’b0: Numeric data is in Linear11, ULinear16, SLinear16, or direct format Others: Ineffective input
2	R	AVSBUS_SUPPORT	1’b0: The AVSBus is not supported Others: Ineffective input
1:0	R	RESERVED	Reserved.

VOUT_MODE (20h)

Format: Unsigned binary

The VOUT_MODE command on Page 0 commands and reads the output voltage mode. The 3MSB are used to determine the data format (only direct format is supported by the MPQ70244FS).

Bits	Access	Bit Name	Description
7:0	R	VOUT_MODE	8’b01000000: Direct mode. The coefficients are m = 2, R = 1, and b = -1.2 Others: Ineffective input

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 0 sets buck 1’s output voltage (V_{OUT1}).

Bits	Access	Bit Name	Description
15:4	R/W	RESERVED	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

3:0	R/W	VOUT_CMD	V_{OUT1} can be calculated with the following equation: V_{OUT1} = VOUT_CMD x 100mV + 2.5V V_{OUT1} ranges between 2.5V to 4V. 100mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 0 sets buck 1's soft-start time.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	Buck 1's soft-start time can be calculated with the following equation: Soft Start = (TON_RISE + 2) x 0.25ms This time ranges between 0.5ms and 2.25ms.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 0 returns the value of certain flags that indicate the state of the MPQ70244FS.

Bits	Access	Bit Name	Description
7	R	BUSY	Indicates whether a busy fault has been detected. This bit is set to 1 if a write command is sent through the PMBus interface by the host during the MPQ70244FS's OTP process. A busy fault cannot pull PG low. 1'b0: No busy fault has occurred 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	Returns buck 1's current status. 1'b0: Device is on 1'b1: Device is off
5	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on buck 1. This bit is set to 1 if buck 1 experiences a V_{OUT} OV event. This bit is same as STATUS_VOUT (7Ah), bit[8]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
4	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on buck 1. This bit is set to 1 if buck 1 experiences an I_{OUT} OC event. This bit is same as STATUS_WORD (79h), bit[14] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	R	RESERVED	Reserved.
2	R	TEMPERATURE	Indicates whether a temperature fault or warning has occurred. This bit is set to 1 when a thermal warning or thermal shutdown is detected. See the detailed fault information in the STATUS_TEMPERATURE (7Dh) section on page 46. 1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	Indicates whether a communication fault has occurred. See the detailed fault information in the STATUS_CML (7Eh) section on page 46. 1'b0: No communication fault has occurred 1'b1: A communication fault has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

0	R	RESERVED	Reserved.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 0 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	Indicates whether buck 1's V_{OUT} is within the normal operation window. This bit is set to 1 if a buck 1 V_{OUT} OV or UV fault is detected. See the detailed fault information in the STATUS_VOUT (7Ah) section below. 1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	Indicates the status of buck 1's output current (I_{OUT}). This bit is set to 1 if an output OC fault is detected on buck 1. This bit is same as STATUS_BYTE (78h), bit[4] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No I_{OUT} fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	Indicates whether a manufacturer-specific fault has been detected, such as a reference fault, ABIST fault, memory CRC fault, and OTP related fault. See STATUS_MFR_SPECIFIC (80h), bits[4:1] on page 47 for the detailed fault information. 1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	If the MPQ70244FS detects that the LDO has entered dropout mode or V_{OUT1} exceeds the V_{OUT} OV / UV threshold range, this bit is set to 1. When the LDO exits dropout mode, this bit is reset to 0 automatically. 1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 0 returns the value of flags that indicate the device's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on buck 1. This bit is set to 1 when buck 1 experiences a V_{OUT} OV event. This bit is the same as STATUS_BYTE (78h), bit[5]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	Indicates whether an under-voltage (UV) fault has occurred on buck 1. This bit is set to 1 if buck 1 experiences a V_{OUT} UV event. 1'b0: No output UV fault has occurred 1'b1: An output UV fault has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 0 returns the value of flags indicating the device's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on buck 1. This bit is set to 1 if buck 1 experiences an I_{OUT} OC event. This bit is the same as STATUS_BYTE (78h), bit[4] and STATUS_WORD (79h), bit[14]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

STATUS_TEMPERATURE (7Dh)

Format: Unsigned binary

The STATUS_TEMPERATURE command on Page 0 returns the value of flags that indicate the device's temperature fault status.

Bits	Access	Bit Name	Description
7	R	TEMP_OT_FAULT	Indicates whether the die junction temperature exceeds the thermal shutdown (TSD) threshold. This bit is set to 1 when an over-temperature (OT) fault is detected. 1'b0: No OT fault has occurred 1'b1: An OT fault has occurred
6	R	TEMP_OT_WARNING	Indicates whether the die junction temperature exceeds the thermal warning (TWN) threshold. This bit is set to 1 when an OT warning is detected. 1'b0: No OT warning has occurred 1'b1: An OT warning has occurred
5:0	R	RESERVED	Reserved.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command on Page 0 returns the value of flags that indicate the device's communication fault status.

Bits	Access	Bit Name	Description
7	R	INVALID_CMD	If the host sends any write/read command to an undefined register address in the MPQ70244FS, this bit is set to 1. 1'b0: No invalid or unsupported commands have been received 1'b1: An invalid or unsupported command has been received
6	R	INVALID_DATA	If the host sends a write command to CAPABILITY (19h), MEMORY_CRC (D5h), LATEST_PEC (D6h), REGISTER_CRC (D7h), MFR_OTP_MEM_STATUS (DAh), or a protected register by WRITE PROTECTION (10h), an invalid write error is detected and this bit is set to 1. 1'b0: No invalid or unsupported data has been received 1'b1: Invalid or unsupported data has been received

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

5	R	PEC_ERROR	If host sends a write command with incorrect PEC value when PEC function is optional, a PEC error is detected and then this bit is set to 1. 1'b0: The PEC has not failed 1'b1: The PEC has failed
4	R	CRC_ERROR	MPQ70244FS checks OTP contents by CRC check during restore OTP process. This bit is set to 1 if the OTP CRC has failed. 1'b0: The CRC has not failed 1'b1: The CRC has failed
3:2	R	RESERVED	Reserved.
1	R	COM_ERROR	If any of the three errors below are detected, this bit is set to 1. Long error: A long error is detected when host sends a write/read command with 2-byte data to the register that only supports 1 byte. Start error: A start error is detected if the host sends a start signal within the time during which a slave address, command address or data, or PEC value is sent. Stop error: A stop error is detected if host sends a stop signal within the time during which a slave address, command address or data, or PEC value is sent. 1'b0: No communication error has occurred 1'b1: A communication fault has occurred (START err, STOP err, LONG err)
0	R	RESERVED	Reserved.

STATUS_MFR_SPECIFIC (80h)

Format: Unsigned binary

The STATUS_MFR_SPECIFIC command on Page 0 returns the value of flags indicating the device's fault status.

Bits	Access	Bit Name	Description
7	R	RESERVED	Reserved.
6	R	PGOV_FAULT	Indicates whether V_{OUT2} PG OV, V_{OUT3} PG OV, or V_{LDOOUT} PG OV has been detected. 1'b0: No PG OV fault has occurred 1'b1: A PG OV fault has occurred
5	R	PGUV_FAULT	Indicates whether V_{OUT2} PG UV, V_{OUT3} PG UV, or V_{LDOOUT} PG UV has been detected. If the LDO's input voltage is below the LDO's set output voltage, this bit is also set to 1. 1'b0: No PG UV fault has occurred 1'b1: A PG UV fault has occurred
4	R	REFERENCE_FAULT	Indicates whether a reference fault has occurred. If the main reference is not within the normal range (typically 96.7% to 103.3% of the auxiliary reference), this bit is set to 1. 1'b0: No reference fault has occurred 1'b1: A reference fault has occurred
3	R	OTP_CRC_IND_ FAULT	Indicates whether an OTP CRC or OTP indicator fault has occurred. See the detail fault information in the MFR_OTP_MEM_STATUS (DAh), bits[1:0] section on page 53. 1'b0: No OTP CRC or OTP indicator fault has occurred 1'b1: An OTP CRC or OTP indicator fault has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

2	R	MEM_CRC_FAULT	Indicates whether a memory CRC fault has occurred. See the detailed fault information in the MFR_OTP_MEM_STATUS (DAh), bit[2] section on page 53. 1'b0: No memory CRC fault has occurred 1'b1: A memory CRC fault has occurred
1	R	ABIST_FAULT	Indicates whether an ABIST fault has occurred. If the PGOV or PGUV comparators cannot operate normally, this bit is set to 1. 1'b0: No ABIST fault has occurred 1'b1: An ABIST fault has occurred
0	R	BIST_DONE	Indicates the built-in self-testing (BIST) state. 1'b0: BIST has not started 1'b1: BIST has started

FREQUENCY_DITHER (C4h)

Format: Unsigned binary

The FREQUENCY_DITHER command on Page 0 configures the frequency spread spectrum parameters.

Bits	Access	Bit Name	Description
7	R/W	FSS_EN	Enables frequency spread spectrum control. 1'b0: Disabled 1'b1: Enabled
6:5	R/W	RESERVED	Reserved.
4	R/W	SSM_RAN	Sets the spread spectrum modulation range. 1'b0: ±5% spread spectrum modulation range 1'b1: ±10% spread spectrum modulation range
3:1	R/W	RESERVED	Reserved.
0	R/W	SSM_FRE	Sets the spread spectrum modulation frequency. 1'b0: 4.5kHz spread spectrum modulation frequency 1'b1: 9kHz spread spectrum modulation frequency

PG_MAPPING (C5h)

Format: Unsigned binary

The PG_MAPPING command on Page 0 configures PG mapping for certain faults.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PM_CML_PG#_ MAPPING	Sets the PG mapping for PMBus interface communication failures. If this bit is set to 1, PG does not pull low while these faults occur, including 7Eh, bit[1], 7Eh, bits[7:6], and DAh, bits[9:6]. 1'b0: A communication failure causes PG to go low and register assertion 1'b1: A communication failure causes register assertion only
2	R/W	PM_CRC_PG#_ MAPPING	Sets the PG mapping for the PMBus interface CRC faults. If this bit is set to 1, PG does not pull low if a PEC fault (7Eh, bit[5]) occurs. 1'b0: A CRC failure causes PG to go low and register assertion 1'b1: A CRC failure causes register assertion only

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

1	R/W	REF_FAULT_PG#_ MAPPING	Sets the PG mapping for reference failures. If this bit is set to 1, PG does not pull low if a reference check fault (80h, bit[4]) occurs. 1'b0: A reference/internal rail failure causes PG to go low and register assertion 1'b1: A reference/internal rail failure causes register assertion only
0	R/W	BIST_FAULT_ PG#_MAPPING	Sets the PG mapping for built-in self-testing (BIST) failures. If this bit is set to 1, PG does not pull low while these faults occur, including 80h, bits[3:1], DAh, bits[5:0], and DAh, bit[10]. 1'b0: A BIST failure causes PG to go low and register assertion 1'b1: A BIST failure causes register assertion only

SAFETY_CONFIG (CBh)

Format: Unsigned binary

The SAFETY_CONFIG command on Page 0 configures safety functions.

Bits	Access	Bit Name	Description
7:5	R/W	RESERVED	Reserved.
4	R/W	OV_PROTECT_EN	Enables output over voltage protection (OVP). 1'b0: Disabled 1'b1: Enabled
3	R/W	UV_PROTECT_EN	Enables output under voltage protection (UVP). 1'b0: Disabled 1'b1: Enabled
2	R/W	BIST_EN	Enables built-in self-testing (BIST). 1'b0: Disabled 1'b1: Enabled
1	R/W	PG_REACTION	Sets the device's reaction if a PG-low fault occurs. If this bit is set to 1, PG-low faults cause the MPQ70244FS to shut down and enter a BIST state. If this bit is set to 0, PG-low faults only pull the PG signal low. The PG-low faults include a PGUV fault, PGOV fault, thermal warning, LDO entering its dropout region, PEC error, register write check error, and PMBus communication error. 1'b0: A PG low fault does not move to device to a safe state 1'b1: A PG low fault causes safe state (all outputs off)
0	R/W	PEC_REQ	Indicates whether a PEC function is required. If PEC is disabled, the host does not need to send a PEC value during the write command, and the MPQ70244FS does not return the PEC value during the read command. If PEC is optional, the host can choose to send a PEC value during a write command, and the MPQ70244FS sends a PEC value during a read command. 1'b0: PEC is disabled 1'b1: PEC is optional

PG_CONFIG (CCh)

Format: Unsigned binary

The PG_CONFIG command on Page 0 configures the PG parameters.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

3	R/W	PG_OUT	Sets the PG output voltage. 1'b0: 1.8V 1'b1: 3.3V
2:1	R/W	PG_DELAY	Sets the PG de-assertion delay. 2'b00: Immediate 2'b01: 2ms 2'b10: 5ms 2'b11: 10ms
0	R/W	PG_THRESHOLD	Sets the PG threshold. 1'b0: ±4% 1'b1: ±6%

GATE_DRIVE STRENGTH (CDh)

Format: Unsigned binary

The GATE_DRIVE STRENGTH command on Page 0 configures the drive strength for buck 1 and buck 2's low-/high-side gate.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	GATE_STR	Sets the drive strength for buck 1 and buck 2's low-/high-side gate. 2'b00: Low gate drive strength 2'b01: Medium low gate drive strength 2'b10: Medium high gate drive strength 2'b11: High gate drive strength

LIGHT_LOAD (CEh)

Format: Unsigned binary

The LIGHT_LOAD command on Page 0 configures the light-load operation mode and enables the output discharge function.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	OUT_DIS	Enables the output discharge function for all channels. 1'b0: Output discharge disabled 1'b1: Output discharge enabled
0	R/W	LIGHT_MODE	Sets the light-load operation mode for the three buck converters. 1'b0: Continuous conduction mode (CCM) 1'b1: Discontinuous conduction mode (DCM)

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 0 configures the turn-off and turn-on time.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.

TON_OFF_SCALE (D0h)

Format: Unsigned binary

The TON_OFF_SCALE command on Page 0 configures the scale for the turn-off and turn-on time.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	DELAY_SCALE	Sets the delay scale. 1'b0: Scale = 0.25ms. The delay ranges between 0ms and 3.75ms 1'b1: Scale = 2.5ms. The delay ranges between 0ms and 37.5ms

FREQUENCY_ILIM_SCALE (D1h)

Format: Unsigned binary

The FREQUENCY_ILIM_SCALE command on Page 0 configures the switching frequency and current limit for buck 1, buck 2, and buck 3.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	FREQUENCY	Sets the switching frequency for buck 1, buck 2, and buck 3. 1'b0: 2.2MHz 1'b1: 3.3MHz
0	R/W	ILIM	Sets the peak current limit scale of all 3 bucks and only valley current limit scale for buck 1 and buck 2. 1'b0: 100% 1'b1: 125%

VIN_START_STOP (D2h)

Format: Unsigned binary

The VIN_START_STOP command on Page 0 configures the start voltage for VIN (V_{IN_START}) and stop voltage for VIN (V_{IN_STOP}).

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:2	R/W	VIN_START	Sets V_{IN_START}. 2'b00: UVLO threshold 2'b01: 4V 2'b10: 5V 2'b11: 6V
1:0	R/W	VIN_STOP	Sets V_{IN_STOP}. 2'b00: UVLO threshold 2'b01: 3.5V 2'b10: 4.5V 2'b11: 5.5V

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

ADDRESS (D3h)

Format: Unsigned binary

The ADDRESS command on Page 0 sets the PMBus interface communication address.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:0	R/W	ADDRESS	Sets the 4 bits of the PMBus interface address.

CONFIGURATION_CODE (D4h)

Format: Unsigned binary

The CONFIGURATION_CODE command on Page 0 returns information regarding the configuration code.

Bits	Access	Bit Name	Description
7:4	R	RESERVED	Reserved.
3:0	R	CONFIG_CODE	Sets the OTP configuration code at shipment.

OTP_CRC (D5h)

Format: Unsigned binary

The OTP_CRC command on Page 0 stores the CRC code for all of the MTP.

Bits	Access	Bit Name	Description
7:0	R	OTP_CRC	Stores the CRC code for all of the MTP. This value is checked at start-up and after writing.

LATEST_PEC (D6h)

Format: Unsigned binary

The LATEST_PEC command on Page 0 stores the latest calculated packet error code from the previous write transition.

Bits	Access	Bit Name	Description
7:0	R	LATEST_PEC	Stores the latest calculated packet error code from the previous write transition.

REGISTER_CRC (D7h)

Format: Unsigned binary

The REGISTER_CRC command on Page 0 stores the CRC code for all of the registers.

Bits	Access	Bit Name	Description
7:0	R	REGISTER_CRC	Stores the CRC code for all of the registers.

MFR_OTP_MEM_CHK (D9h)

Format: Unsigned binary

The MFR_OTP_MEM_CHK command on Page 0 configures the memory and OTP check.

Bits	Access	Bit Name	Description
7:3	R/W	RESERVED	Reserved.
2	R/W	MFR_OTP_MEM_CHK	Selects the memory and OTP check mode. 1’b0: Check once after OTP_CHK_EN and MEM_CHK_EN generate a rising edge 1’b1: Continuously check after OTP_CHK_EN and MEM_CHK_EN are set to 1

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

1	R/W	MFR_OTP_CRC_CHK_EN	Enables an OTP CRC check. 1'b0: Disabled 1'b1: Enabled
0	R/W	MFR_MEM_CRC_CHK_EN	Enables a memory CRC check. 1'b0: Disabled 1'b1: Enabled

MFR_OTP_MEM_STATUS (DAh)

Format: Unsigned binary

The MFR_OTP_MEM_STATUS command on Page 0 returns the value of certain flags that indicate the device's fault status.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Reserved.
9	R	PAGE3_WRITE_CHK_ERR	Indicates whether the data written to the register on Page 3 is the same as what the host sent. A write-check error occurs when the written data is inconsistent with the sent data. 1'b0: No Page 3 write-check error has occurred 1'b1: A Page 3 write-check error has occurred
8	R	PAGE2_WRITE_CHK_ERR	Indicates whether the data written to the register on Page 2 is the same as what the host sent. A write-check error occurs when the written data is inconsistent with the sent data. 1'b0: No Page 2 write-check error has occurred 1'b1: A Page 2 write-check error has occurred
7	R	PAGE1_WRITE_CHK_ERR	Indicates whether the data written to the register on Page 1 is the same as what the host sent. A write-check error occurs when the written data is inconsistent with the sent data. 1'b0: No Page 1-write check error has occurred 1'b1: A Page 1-write check error has occurred
6	R	PAGE0_WRITE_CHK_ERR	Indicates whether the data written to the register on Page 0 is the same as what the host sent. A write-check error occurs when the written data is inconsistent with the sent data. 1'b0: No Page 0 write-check error has occurred 1'b1: A Page 0 write-check error has occurred
5	R	STRUP_OTP_CRC_ERR	Indicates whether the CRC performed on the OTP loaded during start-up process passes. 1'b0: No start-up load OTP CRC error has occurred 1'b1: A start-up load OTP CRC error has occurred
4	R	STRUP_OTP_IND_ERR	Indicates whether the OTP is incorrectly programmed during the start-up process. There is an internal 6-bit OTP_IND_FLAG that indicates the OTP usage status with 3 valid values. OTP_IND_FLAG = 6'b000000 (both the trim page and user page in the OTP are not configured) OTP_IND_FLAG = 6'b001111 (only the trim page in the OTP is configured) OTP_IND_FLAG = 6'b111111 (both the trim page and user page in the OTP are configured) This bit is set to 1 when any value other than the three values above are detected. 1'b0: No start-up load OTP indicator error has occurred 1'b1: A start-up load OTP indicator error has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

3	R	STORE_OTP_ERR	Indicates whether the contents were successfully copied from the operating memory to the matching location in the OTP. 1'b0: No store OTP failure has occurred 1'b1: A store OTP failure has occurred
2	R	BIST_CHK_MEM_ CRC_ERR	Indicates whether a BIST memory CRC error has occurred. This bit is set to 1 if a memory CRC failed in the BIST state or power on state (if enabled). 1'b0: No BIST check memory CRC error has occurred 1'b1: A BIST check memory CRC error has occurred
1	R	BIST_CHK_OTP_ CRC_ERR	Indicates whether a BIST OTP CRC error has occurred. This bit is set to 1 if an OTP CRC failed in the BIST state or power on state (if enabled). 1'b0: No BIST check OTP CRC error has occurred 1'b1: A BIST check OTP CRC error has occurred
0	R	BIST_CHK_MEM_ IND_ERR	Indicates whether the OTP is incorrectly configured during the OTP CRC check process. See DAh, bit[4] on page 53 for the detailed OTP indication information. 1'b0: No BIST check OTP indicator error has occurred 1'b1: A BIST check OTP indicator error has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PAGE 1 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 1 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 1 configures buck 2's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	Enables buck 2's output. 1'b0: The output is off 1'b1: The output is on
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 1 sets buck 2's output voltage (V_{OUT2}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT2} can be calculated with the following equation: V_{OUT2} = Bits[5:0] x 50mV + 0.6V V_{OUT2} can range between 0.6V and 3.75V. 50mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 1 sets buck 2's soft-start time.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	Buck 2's soft-start time can be calculated with the following equation: Soft Start = (TON_RISE + 2) x 0.25ms This time ranges between 0.5ms and 2.25ms.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 1 returns the value of flags that indicate the state of the MPQ70244FS.

Bits	Access	Bit Name	Description
7	R	BUSY	Indicates whether a busy fault has been detected. This bit is set to 1 if a write command is sent through the PMBus interface by the host during the MPQ70244FS's OTP process. A busy fault cannot pull PG low. 1'b0: No busy fault has occurred 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	Returns buck 2's current status. 1'b0: Device is on 1'b1: Device is off
5	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on buck 2. This bit is set to 1 if buck 2 experiences a V_{OUT} OV event. This bit is the same as STATUS_VOUT (7Ah), bit[8]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
4	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on buck 2. This bit is set to 1 if buck 2 experiences an I_{OUT} OC event. This bit is the same as STATUS_WORD (79h), bit[14] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	R	RESERVED	Reserved.
2	R	TEMPERATURE	Indicates whether a temperature fault or warning has occurred. This bit is set to 1 when a thermal warning or thermal shutdown is detected. See the detailed fault information in the STATUS_TEMPERATURE (7Dh on Page 0) section on page 46. 1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	Indicates whether a communication fault has occurred. See the detailed fault information in the STATUS_CML (7Eh on Page 0) section on page 46. 1'b0: No communication fault has occurred 1'b1: A communication fault has occurred
0	R	RESERVED	Reserved.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 1 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	Indicates whether buck 2's V_{OUT} is within the normal operation window. This bit is set to 1 if a buck 2 V_{OUT} OV or UV fault is detected. See the detailed fault information in the STATUS_VOUT (7Ah) section on page 57. 1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

14	R	IOUT_OC_FAULT	Indicates the status of buck 2's output current (I_{OUT}). This bit is set to 1 if an output OC fault is detected on buck 1. This bit is the same as STATUS_BYTE (78h), bit[4] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No I_{OUT} fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	Indicates whether a manufacturer-specific fault has been detected, such as a reference fault, ABIST fault, memory CRC fault, and OTP related fault. See STATUS_MFR_SPECIFIC (80h), bits[4:1] on page 47 for the detailed fault information. 1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	Indicates whether buck 2's output voltage is within the PG window. This bit is set to 1 when buck 2's V_{OUT} is out of PG range. 1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 1 returns the value of flags that indicate buck 2's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on buck 2. This bit is set to 1 when buck 2 experiences a V_{OUT} OV event. This bit is the same as STATUS_BYTE (78h), bit[5]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	Indicates whether an under-voltage (UV) fault has occurred on buck 2. This bit is set to 1 if buck 2 experiences a V_{OUT} UV event. 1'b0: No output UV fault has occurred 1'b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 1 returns the value of flags indicating buck 2's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on buck 2. This bit is set to 1 if buck 2 experiences an I_{OUT} OC event. This bit is the same as STATUS_BYTE (78h), bit[4] and STATUS_WORD (79h), bit[14]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 1 configures the turn-off and turn-on time for buck 2.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PAGE 2 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 2 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 2 configures buck 3's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	Enables buck 3's output. 1'b1: The output is on 1'b0: The output is off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 2 sets buck 3's output voltage (V_{OUT3}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{OUT3} can be calculated with the following equation: V_{OUT3} = VOUT_CMD x 50mV + 0.6V V_{OUT3} ranges between 0.6V and 2.55V. This value is clamped to 2.55V when V_{OUT3} is set to exceed 2.55V. 50mV/step.

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page 2 sets buck 3's soft-start time.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	Buck 3's soft-start time can be calculated with the following equation: Soft Start = (TON_RISE + 2) x 0.25ms This time ranges between 0.5ms and 2.25ms.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 2 returns the value of flags that indicate the state of the MPQ70244FS.

Bits	Access	Bit Name	Description
7	R	BUSY	Indicates whether a busy fault has been detected. This bit is set to 1 if a write command is sent through the PMBus interface by the host during the MPQ70244FS's OTP process. A busy fault cannot pull PG low. 1'b0: No busy fault has occurred 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	Returns buck 3's current status. 1'b0: Device is on 1'b1: Device is off
5	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on buck 3. This bit is set to 1 if buck 3 experiences a V_{OUT} OV event. This bit is the same as STATUS_VOUT (7Ah), bit[8]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
4	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on buck 3. This bit is set to 1 if buck 3 experiences an I_{OUT} OC event. This bit is the same as STATUS_WORD (79h), bit[14] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	R	RESERVED	Reserved.
2	R	TEMPERATURE	Indicates whether a temperature fault or warning has occurred. This bit is set to 1 when a thermal warning or thermal shutdown is detected. See the detailed fault information in the STATUS_TEMPERATURE (7Dh on Page 0) section on page 46. 1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	Indicates whether a communication fault has occurred. See the detailed fault information in the STATUS_CML (7Eh on Page 0) section on page 46. 1'b0: No communication fault has occurred 1'b1: A communication fault has occurred
0	R	RESERVED	Reserved.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 2 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	Indicates whether buck 3's V_{OUT} is within the normal operation window. This bit is set to 1 if a buck 3 V_{OUT} OV or UV fault is detected. See the detailed fault information in the STATUS_VOUT (7Ah) section on page 61. 1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

14	R	IOUT_OC_FAULT	Indicates the status of buck 3's output current (I_{OUT}). This bit is set to 1 if an output OC fault is detected on buck 3. This bit is the same as STATUS_BYTE (78h), bit[4] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No I_{OUT} fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	Indicates whether a manufacturer-specific fault has been detected, such as a reference fault, ABIST fault, memory CRC fault, and OTP related fault. See STATUS_MFR_SPECIFIC (80h on Page 0), bits[4:1] on page 47 for the detailed fault information. 1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred
11	R	PGOOD	Indicates whether buck 3's output voltage is within the PG window. This bit is set to 1 when buck 3's V_{OUT} is out of the PG range. 1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 2 returns the value of flags that indicate buck 3's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on buck 3. This bit is set to 1 when buck 3 experiences a V_{OUT} OV event. This bit is the same as STATUS_BYTE (78h), bit[5]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	Indicates whether an under-voltage (UV) fault has occurred on buck 3. This bit is set to 1 if buck 3 experiences a V_{OUT} UV event. 1'b0: No output UV fault has occurred 1'b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 2 returns the value of flags indicating buck 3's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on buck 3. This bit is set to 1 if buck 3 experiences an I_{OUT} OC event. This bit is the same as STATUS_BYTE (78h), bit[4] and STATUS_WORD (79h), bit[14]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 2 configures the turn-off and turn-on time for buck 3.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PAGE 3 REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page 3 provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page 3 configures LDO's output on/off state.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	Enables the LDO's output. 1'b1: Output on 1'b0: Output off
6:0	R/W	RESERVED	Reserved.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page 3 sets the LDO's output voltage (V_{LDOOUT}).

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	V_{LDOOUT} can be calculated with the following equation: V_{LDOOUT} = VOUT_CMD x 50mV + 0.6V V_{LDOOUT} ranges between 0.6V and 3.75V. 50mV/step.

STATUS_BYTE (78h)

Format: Unsigned binary

The STATUS_BYTE command on Page 3 returns the value of flags that indicate the state of the MPQ70244FS.

Bits	Access	Bit Name	Description
7	R	BUSY	Indicates whether a busy fault has been detected. This bit is set to 1 if a write command is sent through the PMBus interface by the host during the MPQ70244FS's OTP process. A busy fault cannot pull PG low. 1'b0: No busy fault has occurred 1'b1: A fault was declared because the device was busy and unable to respond
6	R	OFF	Returns the LDO's status. 1'b0: Device is on 1'b1: Device is off

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

5	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on the LDO. This bit is set to 1 if the LDO experiences a V_{OUT} OV event. This bit is the same as STATUS_VOUT (7Ah), bit[8]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
4	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on the LDO. This bit is set to 1 if the LDO experiences an I_{OUT} OC event. This bit is the same as STATUS_WORD (79h), bit[14] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
3	R	RESERVED	Reserved.
2	R	TEMPERATURE	Indicates whether a temperature fault or warning has occurred. This bit is set to 1 when a thermal warning or thermal shutdown is detected. See the detailed fault information in the STATUS_TEMPERATURE (7Dh on Page 0) section on page 46. 1'b0: No temperature fault or warning has occurred 1'b1: A temperature fault or warning has occurred
1	R	CML	Indicates whether a communication fault has occurred. See the detailed fault information in the STATUS_CML (7Eh on Page 0) section on page 46. 1'b0: No communication fault has occurred 1'b1: A communication fault has occurred
0	R	RESERVED	Reserved.

STATUS_WORD (79h)

Format: Unsigned binary

The STATUS_WORD command on Page 3 returns 2 bytes of information with a summary of the device's fault/warning conditions. The higher bytes return more detailed information of the fault conditions. The lower bytes are the same as what is returned by register STATUS_BYTE (78h).

Bits	Access	Bit Name	Description
15	R	VOUT_FAULT	Indicates whether the LDO's V_{OUT} is within the normal operation window. This bit is set to 1 if an LDO V_{OUT} OV or UV fault is detected. See the detailed fault information in the STATUS_VOUT (7Ah) section on page 65. 1'b0: No V_{OUT} fault has occurred 1'b1: An V_{OUT} fault has occurred
14	R	IOUT_OC_FAULT	Indicates the status of the LDO's output current (I_{OUT}). This bit is set to 1 if an output OC fault is detected on the LDO. This bit is the same as STATUS_BYTE (78h), bit[4] and STATUS_IOUT (7Bh), bit[7]. 1'b0: No I_{OUT} fault has occurred 1'b1: An I_{OUT} fault has occurred
13	R	RESERVED	Reserved.
12	R	MANUFAC_FAULT	Indicates whether a manufacturer-specific fault has been detected, such as a reference fault, ABIST fault, memory CRC fault, and OTP related fault. See STATUS_MFR_SPECIFIC (80h on Page 0), bits[4:1] on page 47 for the detailed fault information. 1'b0: No manufacturer-specific fault has occurred 1'b1: A manufacturer-specific fault has occurred

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

11	R	PGOOD	Indicates whether the LDO's output voltage is within PG window. This bit is set to 1 when the LDO's V_{OUT} is out of PG range. 1'b0: PG is high 1'b1: PG is low
10:8	R	RESERVED	Reserved.
7:0	R	STATUS_BYTE	The same as STATUS BYTE (78h).

STATUS_VOUT (7Ah)

Format: Unsigned binary

The STATUS_VOUT command on Page 3 returns the value of flags that indicate the LDO's V_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	VOUT_OV_FAULT	Indicates whether an over-voltage (OV) fault has occurred on the LDO. This bit is set to 1 when the LDO experiences a V_{OUT} OV event. This bit is the same as STATUS_BYTE (78h), bit[5]. 1'b0: No output OV fault has occurred 1'b1: An output OV fault has occurred
6:5	R	RESERVED	Reserved.
4	R	VOUT_UV_FAULT	Indicates whether an under-voltage (UV) fault has occurred on the LDO. This bit is set to 1 if the LDO experiences a V_{OUT} UV event. 1'b0: No output UV fault has occurred 1'b1: An output UV fault has occurred
3:0	R	RESERVED	Reserved.

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command on Page 3 returns the value of flags indicating the LDO's I_{OUT} fault status.

Bits	Access	Bit Name	Description
7	R	IOUT_OC_FAULT	Indicates whether an output over-current (OC) fault has occurred on the LDO. This bit is set to 1 if the LDO experiences an I_{OUT} OC event. This bit is the same as STATUS_BYTE (78h), bit[4] and STATUS_WORD (79h), bit[14]. 1'b0: No output OC fault has occurred 1'b1: An output OC fault has occurred
6:0	R	RESERVED	Reserved.

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page 3 configures the turn-off and turn-on time for the LDO.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PAGE FF REGISTER MAP

PAGE (00h)

Format: Unsigned binary

The PAGE command on Page FF provides the ability to configure, control, and monitor all outputs through only one physical address. All subsequent commands that allow for multi-page actions are applied to the corresponding regulators selected by the PAGE (00h) command.

Bits	Access	Bit Name	Description
7:0	R/W	PAGE	8'b00000000: V_{OUT1} (Page 0) 8'b00000001: V_{OUT2} (Page 1) 8'b00000002: V_{OUT3} (Page 2) 8'b00000003: LDO (Page 3) 8'b11111111: All rails (Page FF) Others: Ineffective input

OPERATION (01h)

Format: Unsigned binary

The OPERATION command on Page FF configures all output on/off states.

Bits	Access	Bit Name	Description
7	R/W	OPERATION	Enables all rails' outputs at the same time. 1'b1: Output on 1'b0: Output off
6:0	R/W	RESERVED	Reserved.

CLEAR_FAULTS (03h)

The CLEAR_FAULTS command on Page FF clears any fault bits in the following status registers: STATUS_BYTE (78h), STATUS_WORD (79h), STATUS_VOUT (7Ah), STATUS_IOUT (7Bh), STATUS_INPUT (7Ch), STATUS_TEMPERATURE (7Dh), STATUS_CML (7Eh), and STATUS_MFR_SPECIFIC (80h).

This command is write-only. There is no data byte for this command. If the CLEAR FAULTS command is sent with any data, the MPQ70244FS does not perform a clear command and reports a communication error (COM_ERROR).

WRITE_PROTECT (10h)

Format: Unsigned binary

The WRITE_PROTECT command on Page FF controls writing to the converter. The intent of this command is to provide protection against accidental changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:0	R/W	WRITE_PROTECT	8'b10000000: Disable all writes except to the WRITE_PROTECT command 8'b 01000000: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 8'b 00100000: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands 8'b 00000000: Enable writes to all commands. Others: Ineffective input

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the MPQ70244FS to copy the contents of the operating memory to the matching locations in the OTP, excluding the internal trim registers. This process begins once the MPQ70244FS receives a STORE_USER_ALL command from the PMBus interface.

This command is write-only. There is no data byte for this command.

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command on Page FF instructs the MPQ70244FS to copy the contents from the OTP and overwrite the matching locations in the operating memory, excluding the trim registers. Any items in the OTP that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the MPQ70244FS is operating. However, the MPQ70244FS may be unresponsive during this operation, with unpredictable or undesirable results.

This command is write-only. There is no data byte for this command.

VOUT_COMMAND (21h)

Format: Unsigned binary

The VOUT_COMMAND command on Page FF sets the MPQ70244FS's output voltages.

Bits	Access	Bit Name	Description
15:6	R/W	RESERVED	Reserved.
5:0	R/W	VOUT_CMD	All channels' VOUT_CMD are set to same value while the MPQ70244FS is in Page FF. Each output voltage can be calculated with its unique formula below. V_{OUT1} = Bits[3:0] of this command x 100mV + 2.5V. 2.5V to 4V. 100mV/step V_{OUT2} = Bits[5:0] of this command x 50mV + 0.6V. 0.6V to 3.75V. 50mV/step V_{OUT3} = Bits[5:0] of this command x 50mV + 0.6V. 0.6V to 2.55V (is clamped to 2.55V when V_{OUT3} is set to exceed 2.55V). 50mV/step V_{LDOOUT} = Bits[5:0] of this command x 50mV + 0.6V, 0.6V to 3.75V. 50mV/step

TON_RISE (61h)

Format: Unsigned binary

The TON_RISE command on Page FF sets the MPQ70244FS's soft-start time for buck 1, buck 2, and buck 3. This command cannot be used for the LDO rail.

Bits	Access	Bit Name	Description
15:3	R/W	RESERVED	Reserved.
2:0	R/W	TON_RISE	Sets the soft start time for buck 1, buck 2, and buck 3, which can be calculated with the following equation: Soft Start = (TON_RISE + 2) x 0.25ms This time ranges between 0.5ms and 2.25ms.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FREQUENCY_DITHER (C4h)

Format: Unsigned binary

The FREQUENCY_DITHER command on Page FF configures the frequency spread spectrum parameters.

Bits	Access	Bit Name	Description
7	R/W	FSS_EN	Enables frequency spread spectrum control. 1'b0: Disabled 1'b1: Enabled
6:5	R/W	RESERVED	Reserved.
4	R/W	SSM_RAN	Sets the spread spectrum modulation range. 1'b0: ±5% spread spectrum modulation range 1'b1: ±10% spread spectrum modulation range
3:1	R/W	RESERVED	Reserved.
0	R/W	SSM_FRE	Sets the spread spectrum modulation frequency. 1'b0: 4.5kHz spread spectrum modulation frequency 1'b1: 9kHz spread spectrum modulation frequency

PG_MAPPING (C5h)

Format: Unsigned binary

The PG_MAPPING command on Page FF configures PG mapping for certain faults.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PM_CML_PG#_ MAPPING	Sets the PG mapping for PMBus interface communication failures. If this bit is set to 1, PG does not pull low while these faults occur, including 7Eh, bit[1], 7Eh, bits[7:6], and DAh, bits[9:6]. 1'b0: A communication failure causes PG to go low and register assertion 1'b1: A communication failure causes register assertion only
2	R/W	PM_CRC_PG#_ MAPPING	Sets the PG mapping for the PMBus interface CRC faults. If this bit is set to 1, PG does not pull low if a PEC fault (7Eh, bit[5]) occurs. 1'b0: A CRC failure causes PG to go low and register assertion 1'b1: A CRC failure causes register assertion only
1	R/W	REF_FAULT_PG#_ MAPPING	Sets the PG mapping for reference failures. If this bit is set to 1, PG does not pull low if a reference check fault (80h, bit[4]) occurs. 1'b0: A reference/internal rail failure causes PG to go low and register assertion 1'b1: A reference/internal rail failure causes register assertion only
0	R/W	BIST_FAULT_PG#_ MAPPING	Sets the PG mapping for built-in self-testing (BIST) failures. If this bit is set to 1, PG does not pull low while these faults occur, including 80h, bits[3:1], DAh, bits[5:0], and DAh, bit[10]. 1'b0: A BIST failure causes PG to go low and register assertion 1'b1: A BIST failure causes register assertion only

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

SAFETY_CONFIG (CBh)

Format: Unsigned binary

The SAFETY_CONFIG command on Page FF configures safety functions.

Bits	Access	Bit Name	Description
7:5	R/W	RESERVED	Reserved.
4	R/W	OV_PROTECT_EN	Enables output over voltage protection (OVP). 1'b0: Disabled 1'b1: Enabled
3	R/W	UV_PROTECT_EN	Enables output under voltage protection (UVP). 1'b0: Disabled 1'b1: Enabled
2	R/W	BIST_EN	Enables built-in self-testing (BIST). 1'b0: Disabled 1'b1: Enabled
1	R/W	PG_REACTION	Sets the device's reaction if a PG-low fault occurs. If this bit is set to 1, PG-low faults cause the MPQ70244FS to shut down and enter a BIST state. If this bit is set to 0, PG-low faults only pull the PG signal low. The PG-low faults include a PGUV fault, PGOV fault, thermal warning, LDO entering its dropout region, PEC error, register write check error, and PMBus communication error. 1'b0: A PG low fault does not move to device to a safe state 1'b1: A PG low fault causes safe state (all outputs off)
0	R/W	PEC_REQ	Indicates whether a PEC function is required. If PEC is disabled, the host does not need to send a PEC value during the write command, and the MPQ70244FS does not return the PEC value during the read command. If PEC is optional, the host can choose to send a PEC value during a write command, and the MPQ70244FS sends a PEC value during a read command. 1'b0: PEC is disabled 1'b1: PEC is optional

PG_CONFIG (CCh)

Format: Unsigned binary

The PG_CONFIG command on Page FF configures the PG parameters.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3	R/W	PG_OUT	Sets the PG output voltage. 1'b0: 1.8V 1'b1: 3.3V
2:1	R/W	PG_DELAY	Sets the PG de-assertion delay. 2'b00: Immediate 2'b01: 2ms 2'b10: 5ms 2'b11: 10ms
0	R/W	PG_THRESHOLD	Sets the PG threshold. 1'b0: ±4% 1'b1: ±6%

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

GATE_DRIVE STRENGTH (CDh)

Format: Unsigned binary

The GATE_DRIVE STRENGTH command on Page FF configures the drive strength for buck 1 and buck 2's low-/high-side gate.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1:0	R/W	GATE_STR	Sets the drive strength for buck 1 and buck 2's low-/high-side gate. 2'b00: Low gate drive strength 2'b01: Medium-low gate drive strength 2'b10: Medium-high gate drive strength 2'b11: High gate drive strength

LIGHT_LOAD (CEh)

Format: Unsigned binary

The LIGHT_LOAD command on Page FF configures the light-load operation mode and enables the output discharge function.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	OUT_DIS	Enables output discharge function for all channels. 1'b0: Output discharge disabled 1'b1: Output discharge enabled
0	R/W	LIGHT_MODE	Sets the light-load operation mode for all three buck converters. 1'b0: Continuous conduction mode (CCM) 1'b1: Discontinuous conduction mode (DCM)

TON_OFF_DELAY (CFh)

Format: Unsigned binary

The TON_OFF_DELAY command on Page FF configures the turn-off and turn-on time for all channels.

Bits	Access	Bit Name	Description
7:4	R/W	ON_DELAY	Sets the turn-on delay, calculated with the following equation: Turn-On Delay = ON_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.
3:0	R/W	OFF_DELAY	Sets the turn-off delay, calculated with the following equation: Turn-Off Delay = OFF_DELAY x DELAY_SCALE Where DELAY_SCALE can be set by the TON_OFF_SCALE (D0h) register.

TON_OFF_SCALE (D0h)

Format: Unsigned binary

The TON_OFF_SCALE command on Page FF configures the scale of the turn-off and turn-on time.

Bits	Access	Bit Name	Description
7:1	R/W	RESERVED	Reserved.
0	R/W	DELAY_SCALE	Sets the delay scale. 1'b0: Scale = 0.25ms. The delay ranges between 0ms and 3.75ms 1'b1: Scale = 2.5ms. The delay ranges between 0ms and 37.5ms

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

FREQUENCY_ILIM_SCALE (D1h)

Format: Unsigned binary

The FREQUENCY_ILIM_SCALE command on Page FF configures the switching frequency and current limit for buck 1, buck 2, and buck 3.

Bits	Access	Bit Name	Description
7:2	R/W	RESERVED	Reserved.
1	R/W	FREQUENCY	Sets the switching frequency for buck 1, buck 2, and buck 3. 1'b0: 2.2MHz 1'b1: 3.3MHz
0	R/W	ILIM	Sets the peak current limit scale of all three bucks and the valley current limit scale for buck 1 and buck 2. 1'b0: 100% 1'b1: 125%

VIN_START_STOP (D2h)

Format: Unsigned binary

The VIN_START_STOP command on Page FF configures the start voltage for VIN (V_{IN_START}) and stop voltage for VIN (V_{IN_STOP}).

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:2	R/W	VIN_START	Sets V_{IN_START}. 2'b00: UVLO threshold 2'b01: 4V 2'b10: 5V 2'b11: 6V
1:0	R/W	IN_STOP	Sets V_{IN_STOP}. 2'b00: UVLO threshold 2'b01: 3.5V 2'b10: 4.5V 2'b11: 5.5V

ADDRESS (D3h)

Format: Unsigned binary

The ADDRESS command on Page FF sets the PMBus interface communication address.

Bits	Access	Bit Name	Description
7:4	R/W	RESERVED	Reserved.
3:0	R/W	ADDRESS	Sets the 4 bits of the PMBus interface address.

MFR_OTP_MEM_CHK (D9h)

Format: Unsigned binary

The MFR_OTP_MEM_CHK command on Page FF configures the memory and OTP check.

Bits	Access	Bit Name	Description
7:3	R/W	RESERVED	Reserved.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

2	R/W	MFR_OTP_MEM_CHK	Selects the memory and OTP check mode. 1'b0: Check once after OTP_CHK_EN and MEM_CHK_EN generate a rising edge 1'b1: Continuously check after OTP_CHK_EN and MEM_CHK_EN are set to 1
1	R/W	MFR_OTP_CRC_ CHK_EN	Enables an OTP CRC check. 1'b0: Disabled 1'b1: Enabled
0	R/W	MFR_MEM_CRC_ CHK_EN	Enables a memory CRC check. 1'b0: Disabled 1'b1: Enabled

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

APPLICATION INFORMATION

Figure 14 shows the MPQ70244FS's typical application circuit.

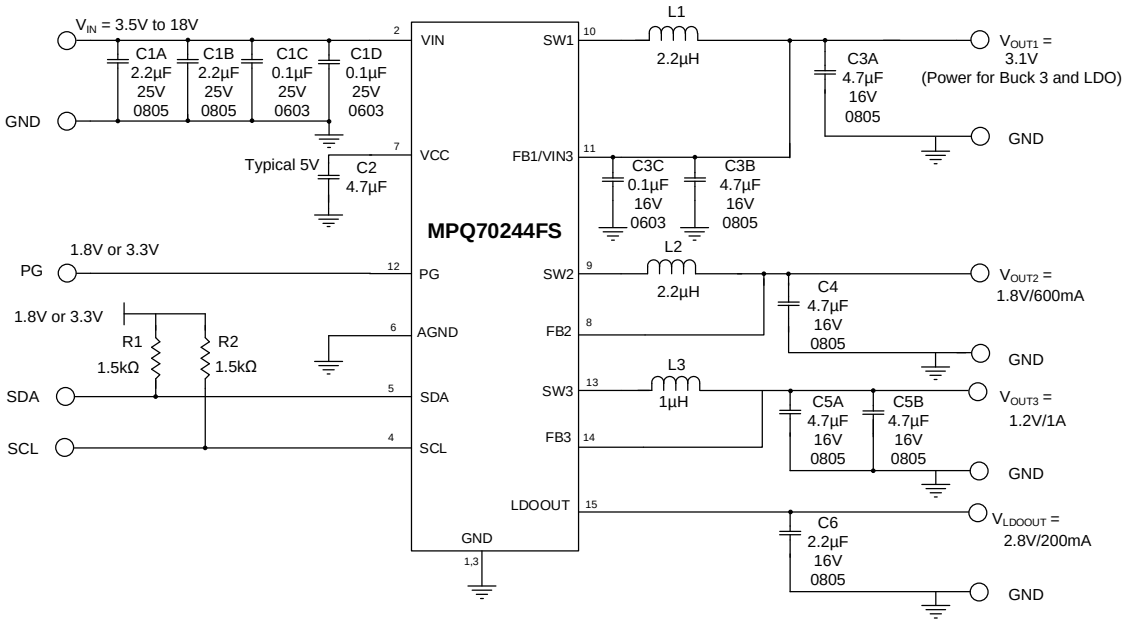


Figure 14: Typical Application Circuit (V_{OUT1} = 3.1V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.8V)

Table 4: Design Guide Index

Pin #	Pin Name	Component	Design Guide Index
14	FB3	-	Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
2	VIN	C1A, C1B, C1C, C1D	Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11)
11	FB1/VIN3	C3B, C3C	Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11) Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
9	SW2	L2, C4	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15) Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
10	SW1	L1, C3A	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15) Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
13	SW3	L3, C5A, C5B	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15) Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)
15	LDOOUT	C6	Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15)
7	VCC	C2	Internal VCC (VCC, Pin 7)
4	SCL	-	PMBus Interface (SCL, Pin 4; SDA, Pin 5)
5	SDA	-	PMBus Interface (SCL, Pin 4; SDA, Pin 5)
8	FB2	-	Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)
12	PG	-	Power Good Indicator (PG, Pin 12)
1, 3	GND	-	GND Connection (GND, Pins 1 and 3; AGND, Pin 6)
6	AGND	-	GND Connection (GND, Pins 1 and 3; AGND, Pin 6)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

Setting the Output Voltage (FB1, Pin 11; FB2, Pin 8; FB3, Pin 14)

The OTP command VOUT_COMMAND (21h on Page 0, Page 1, Page 2, Page 3, and Page FF) sets the output voltages. Write to the VOUT_CMD bits to set the output voltages, or write to VOUT_COMMAND (21h on Page FF) to set every output voltage.

The different V_{OUT} values for buck 1, buck 2, buck 3, and the LDO can be calculated with Equation (1), Equation (2), Equation (3), and Equation (4), respectively:

$$V_{OUT1}(V) = VOUT_CMD[3:0] \times 0.1 + 2.5 \quad (1)$$

$$V_{OUT2}(V) = VOUT_CMD[5:0] \times 0.05 + 0.6 \quad (2)$$

$$V_{OUT3}(V) = VOUT_CMD[5:0] \times 0.05 + 0.6 \quad (3)$$

$$V_{LDOOUT}(V) = VOUT_CMD[5:0] \times 0.05 + 0.6 \quad (4)$$

Selecting the Input Capacitors (VIN, Pin 2; VIN3, Pin 11)

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

It is strongly recommended to use another lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place this capacitor as close to VIN and GND as possible.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (5):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (5)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (6):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive input voltage ripple. The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

Selecting the Output Capacitors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13; LDOOUT, Pin 15)

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For the best results, use low-ESR capacitors to keep the output voltage ripple low. The buck regulator's output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (8)$$

Where L is the inductance, and R_{ESR} is the output capacitor's equivalent series resistance (ESR).

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (10)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ70244FS can be optimized for a wide range of capacitances and ESR values.

The LDO is specifically designed to work with a standard ceramic output capacitor to save space and improve performance.

The LDO charges the output capacitor during the start-up stage, and the charge current is equal to the LDO current limit subtracted by the LDO load current. There is an internal under-voltage blanking time with a minimum of 385µs, and the output capacitor must be fully charged during this period.

For example, if there is a constant 200mA load during start-up and the LDO voltage is set to 2.8V, the output capacitor should be below 6.9µF to be fully charged. A 2.2µF ceramic capacitor (e.g. GRM21BR71C225KA12L, 16V, X7R) is recommended for most applications.

A higher output capacitance is possible if the load current during the start-up stage is kept sufficiently low. The maximum effective output capacitance can be estimated with Equation (11):

$$C_{MAX} = (I_{LIM_MIN} - I_{LOAD}) \times BT / V_{LDO} \quad (11)$$

Where I_{LIM_MIN} = 280mA, and BT = 385µs.

For example, if the load current is a constant 10mA during start-up and the LDO voltage is set to 2.8V, the maximum allowed effective capacitance is (0.27A / 2.8V x 385µs), which is about 37µF.

Selecting the Inductors (SW2, Pin 9; SW1, Pin 10; SW3, Pin 13)

For most applications, it is recommended to use a 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance can be calculated with Equation (12):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (13):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

Internal VCC (VCC, Pin 7)

The VCC capacitor (C2) should be between 1µF and 10µF. Generally, a 2.2µF or 4.7µF ceramic capacitor is recommended.

Most of the internal circuitry is powered by the internal 5V VCC regulator. This regulator uses VIN as its input and operates across the full V_{IN} range. When V_{IN} exceeds 5V, V_{CC} is in full regulation. When V_{IN} drops below 5V, the V_{CC} output degrades.

PMBus Interface (SCL, Pin 4; SDA, Pin 5)

The MPQ70244FS works as a slave-only device, which supports up to 1000kbps of bidirectional data transfer in fast mode, adding flexibility to the power supply solution. See the PMBus Interface section on page 37 for details.

The SCL and SDA lines are externally pulled to a stable voltage (e.g. 3.3V) with a resistor (e.g. 1.5kΩ).

Power Good Indicator (PG, Pin 12)

The PG pin integrates an internal, push-pull structure, so no external components are required.

GND Connection (GND, Pins 1 and 3; AGND, Pin 6)

See the PCB Layout Guidelines section on page 67 for more details.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

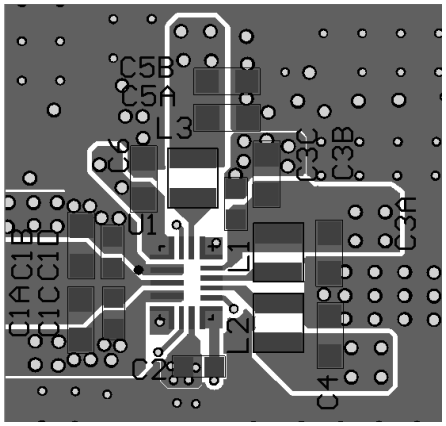
PCB Layout Guidelines (14)

Efficient PCB layout, especially for input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 15 and follow the guidelines below:

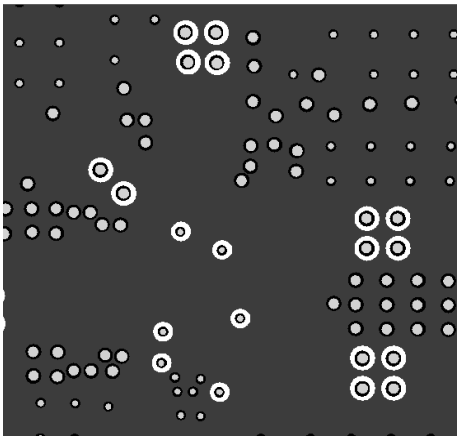
1. Place the symmetric input capacitors as close to VIN and GND as possible.
2. Use a large ground plane to connect to GND directly.
3. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
4. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN, VIN3, and GND as possible to minimize high-frequency noise.
5. Keep the connection between the input capacitor and VIN as short and wide as possible.
6. Place the VCC capacitor as close to VCC and AGND as possible.
7. Route SW away from sensitive analog areas, such as FB.
8. Ensure that the trace between FB and the output is as short as possible.
9. Use multiple vias to connect the power planes to the internal layers.

Note:

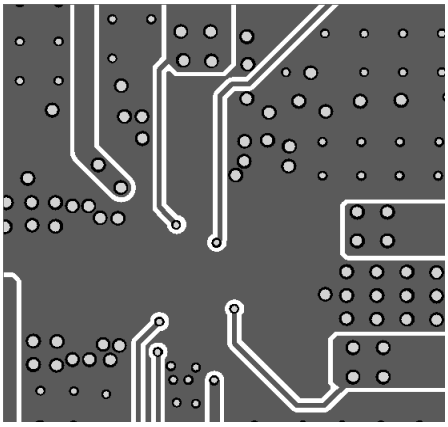
14) The recommended PCB layout is based on Figure 15.



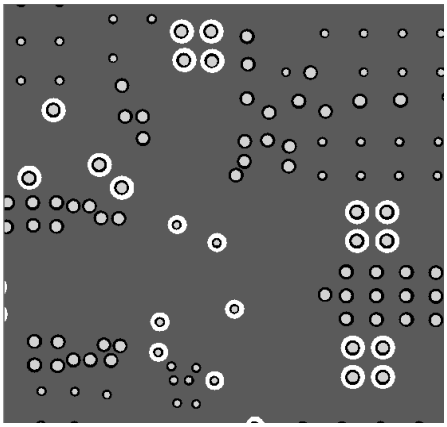
Top Layer



Inner Layer 1



Inner Layer 2



Bottom Layer

Figure 15: Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

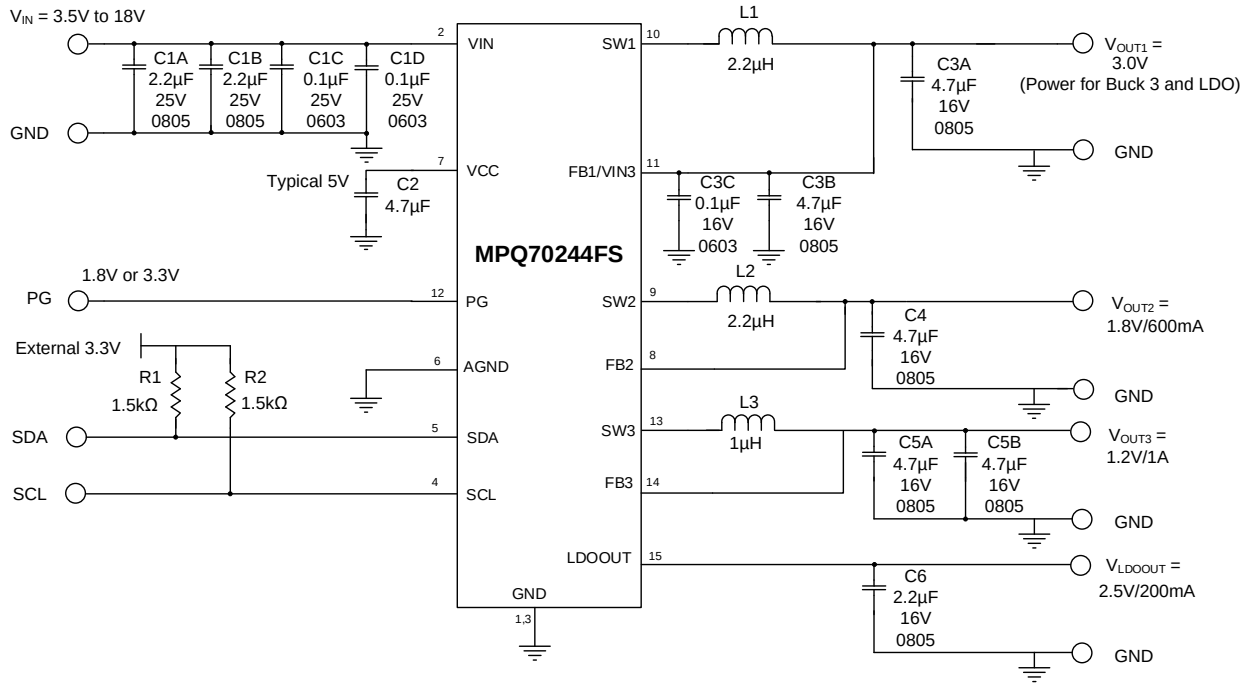


Figure 16: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V)

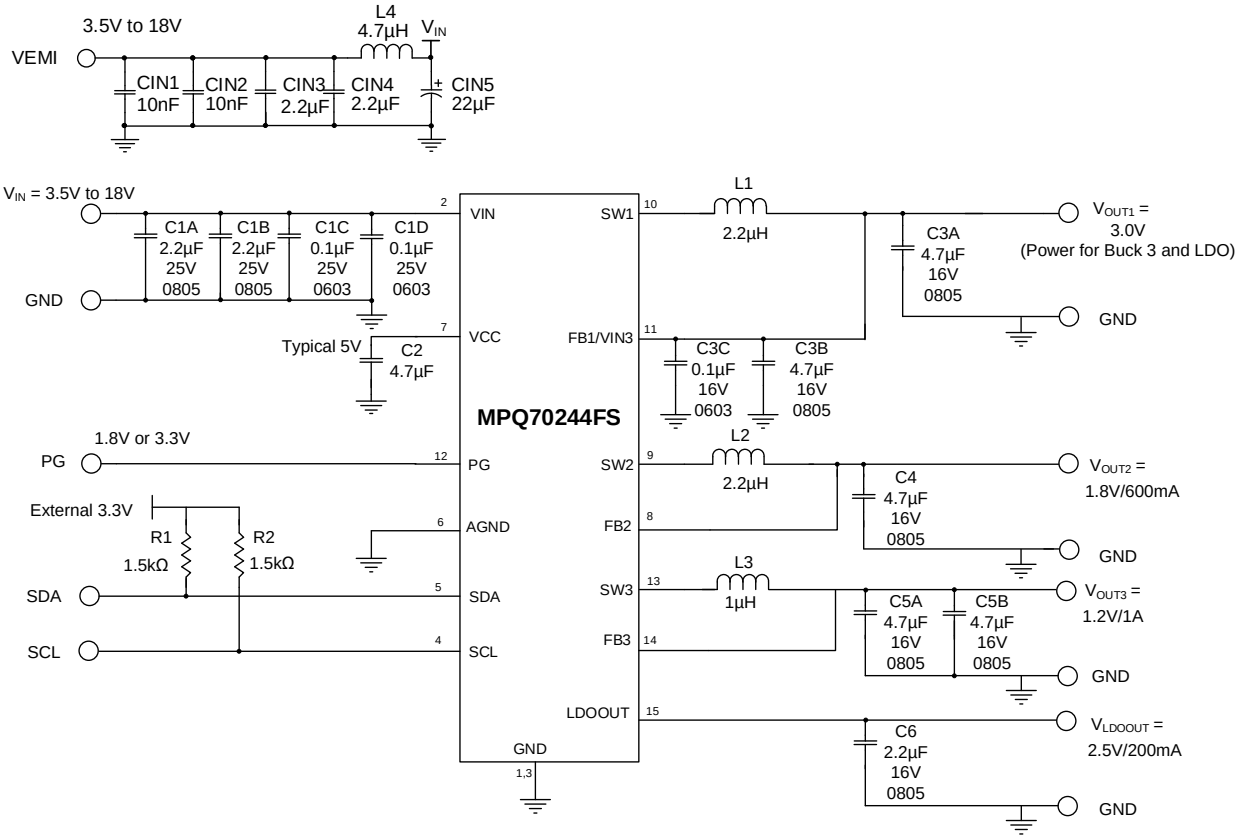


Figure 17: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V with EMI Filters)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS *(continued)*

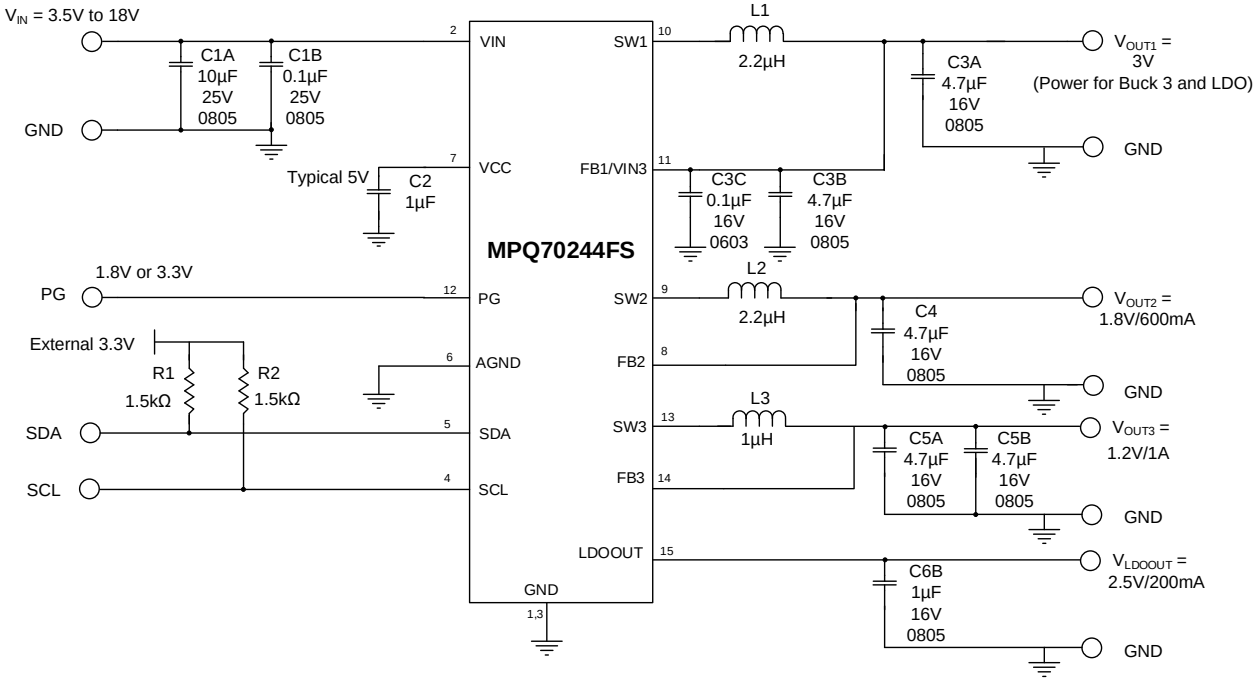
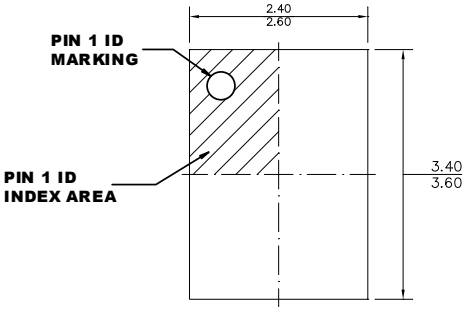


Figure 18: Typical Application Circuit (V_{OUT1} = 3V, V_{OUT2} = 1.8V, V_{OUT3} = 1.2V, V_{LDOOUT} = 2.5V with Minimal External Components)

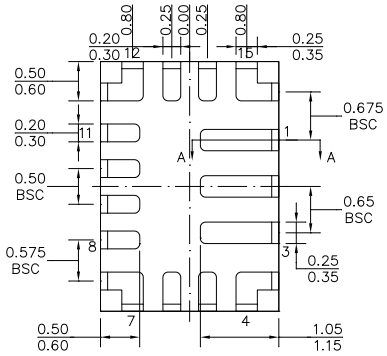
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

PACKAGE INFORMATION

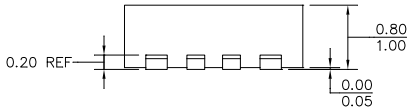
QFN-15 (2.5mmx3.5mm)
Wettable Flank



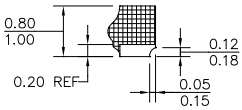
TOP VIEW



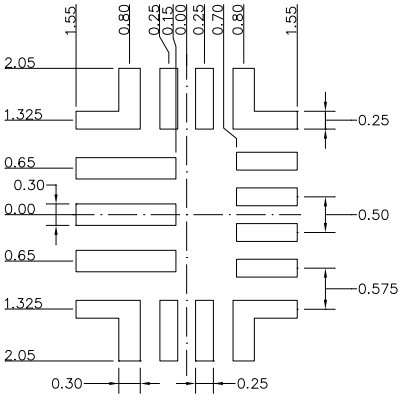
BOTTOM VIEW



SIDE VIEW



SECTION A-A



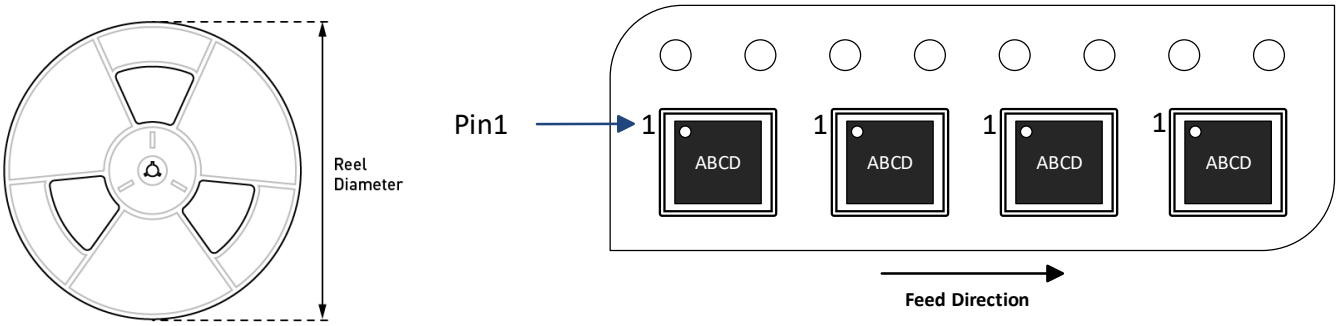
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ70244FSGRHE-xxxxAEC1-Z	QFN-15 (2.5mmx3.5mm)	5000	N/A	N/A	13in	12mm	8mm

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/30/2024	Initial Release	-

Notice: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2024 MPS. All Rights Reserved.