MPQ8623

16V, 6A, High Efficiency, Synchronous, Step-Down Converter with Adjustable Current Limit

The Future of Analog IC Technology

DESCRIPTION

The MPQ8623 is a fully integrated, high-frequency, synchronous, buck converter. The MPQ8623 offers a very compact solution that achieves up to 6A of output current with excellent load and line regulation over a wide input supply range. The MPQ8623 operates at high efficiency over a wide output current load range.

The MPQ8623 adopts an internally compensated constant-on-time (COT) control that provides fast transient response and eases loop stabilization.

The operating frequency can be set to 600kHz, 1100kHz, or 2000kHz easily with MODE configuration, allowing the MPQ8623 frequency to remain constant regardless of the input and output voltages.

The output voltage start-up ramp is controlled by an internal 1.5ms timer, which can be increased by adding a capacitor on TRK/REF. An open-drain power good (PGOOD) signal indicates if the output is within its nominal voltage range. PGOOD is clamped to around 0.7V with an external pull-up voltage when the input supply fails to power the MPQ8623.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPQ8623 requires a minimal number of readily available, standard, external components and is available in a QFN-14 (2mmx3mm) package.

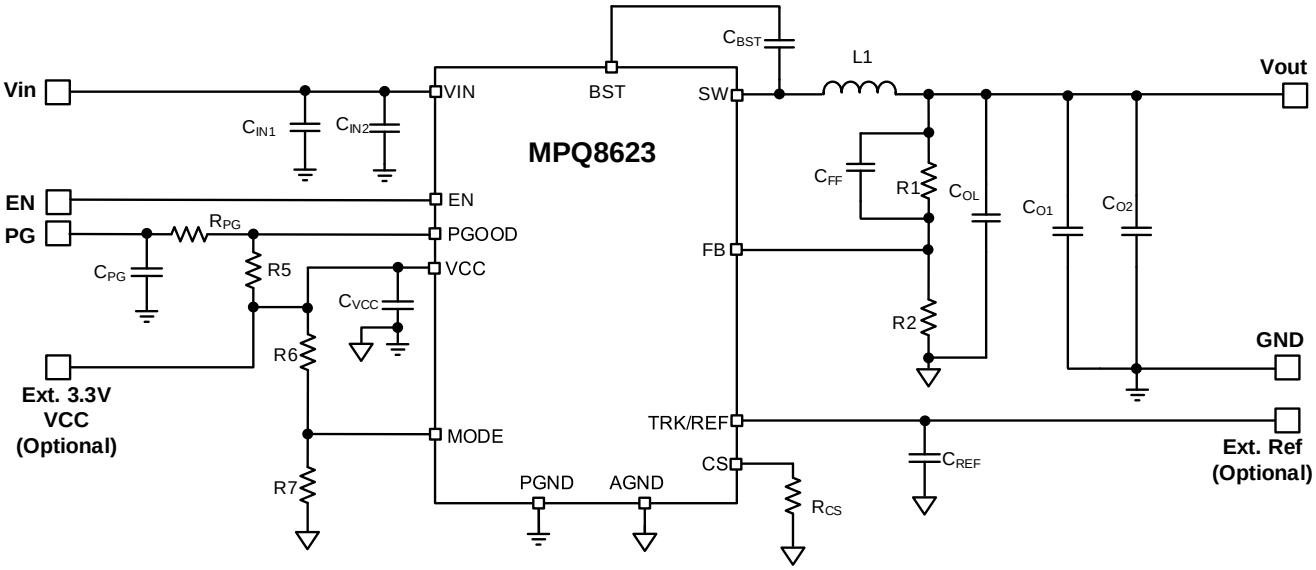
FEATURES

- Wide Input Voltage Range
  - 2.85V to 16V with External 3.3V VCC Bias
  - 4V to 16V with Internal VCC Bias or External 3.3V VCC Bias
- 6A Output Current
- Programmable Accurate Current Limit Level
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive Constant-On-Time (COT) for Ultrafast Transient Response
- Stable with Zero ESR Output Capacitor
- 0.5% Reference Voltage Over 0°C to +70°C Junction Temperature Range
- 1% Reference Voltage Over -40°C to +125°C Junction Temperature Range
- Selectable Forced CCM or Pulse-Skip Operation
- Excellent Load Regulation
- Output Voltage Tracking
- Output Voltage Discharge
- PGOOD Active Clamped at Low Level during Power Failure
- Programmable Soft-Start Time from 1.5ms and Up
- Pre-Bias Start-Up
- Selectable Switching Frequency from 600kHz, 1100kHz, and 2000kHz
- Latch-Off for OCP, OVP, UVP, OTP, and UVLO
- Output Adjustable from 0.9V to 0.9 x VIN Up to 6V Max
- Available in a QFN-14 (2mmx3mm) Package

APPLICATIONS

- Telecom and Networking Systems
- Servers, Cloud-Computing, Storage
- Base Stations
- General Purpose Point-of-Load (PoL)
- 12V Distribution Power Systems
- High-end TV
- Game Consoles and Graphic Cards

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ8623GD	QFN-14 (2mmx3mm)	*See Below*

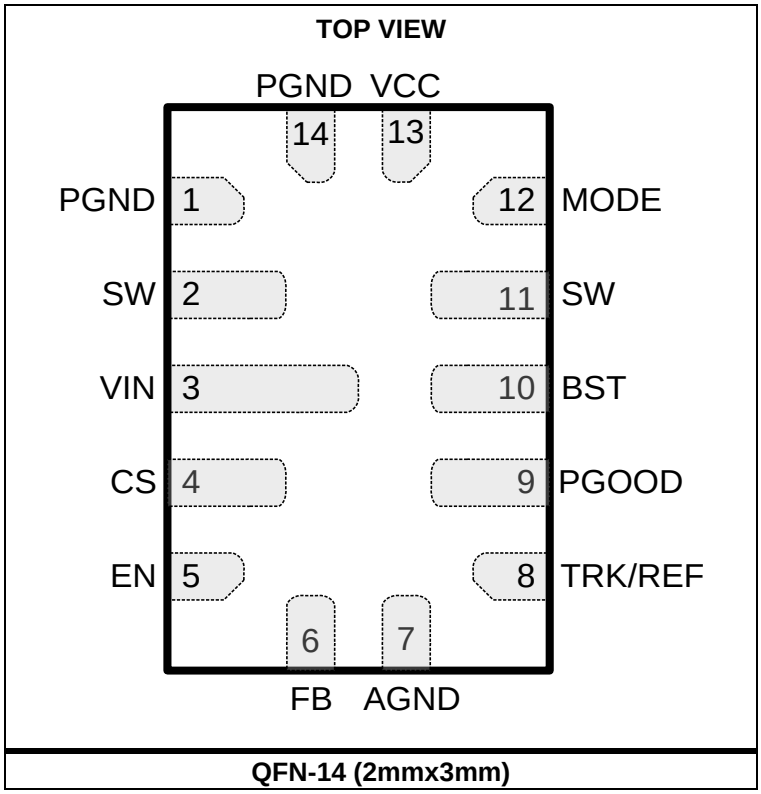
* For Tape & Reel, add suffix –Z (e.g. MPQ8623GD–Z)

TOP MARKING

ARM
YWW
LLL

ARM: Product code of MPQ8623GD
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (2mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 18V
V_{IN} - V_{SW} (DC) ..... -0.3V to +18.3V
V_{IN} - V_{SW} (25ns) ..... -5V to +28V
V_{SW} (DC) ..... -0.3V to +18.3V
V_{SW} (25ns) (2) ..... -5V to +25V
V_{BST} 22.3V
V_{BST} - V_{SW} (25ns) (2) 5V
VCC, EN 4.5V
All other pins ..... -0.3V to 4.3V
Junction temperature ..... 170°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +170°C

Recommended Operating Conditions (3)

Supply voltage (VIN) ..... 4V to 16V
Output voltage (V_{OUT}) ..... 0.9V to 6V
External VCC bias (V_{CC_EXT}) ..... 3.12V to 3.6V
Maximum output current (I_{OUT_MAX}) 6A
Maximum output current limit (I_{OC_MAX}) 8A
Maximum peak inductor current (I_{L_PEAK}) 10A
EN voltage (V_{EN}) 3.6V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance(4) θ_{JB} θ_{JC_TOP}

QNF-14 (2mmx3mm)	6.8	17.4	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) Measured by using a differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point.
   θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

VIN = 12V, T_J = -40°C to 125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VIN Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		0	10	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
HS on-state resistance	$R_{DS\_ON\_HS}$	V_{EN} = 2V @ 25°C		22.6		mΩ
LS on-state resistance	$R_{DS\_ON\_LS}$	V_{EN} = 2V @ 25°C		8.1		mΩ
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS}/I_{OUT}	I_{OUT} ≥ 2A	36	40	44	μA/A
Low-side negative current limit	$I_{LIM\_NEG\_10}$			-8		A
Negative current limit time-out (5)	t_{NCL_Timer}			80		ns
Timer						
Switching frequency (6)	f_{SW}	V_{OUT}=1V	530	660	790	kHz
		V_{OUT}=1V	935	1100	1265	kHz
		V_{OUT}=3.3V	1870	2200	2530	kHz
Minimum on time (5)	T_{ON_MIN}				50	ns
Minimum off time (5)	T_{OFF_MIN}	V_{FB} = 1000mV			180	ns
Over-Voltage (OVP) and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft Start (SS)						
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	891	900	909	mV
		T_J = 0°C to +70°C	895	900	905	mV
TRK/REF sourcing current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		15		μA
TRK/REF sinking current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 1V		6		μA
Soft-start time	t_{SS}	C_{TRACK} = 1nF	1	1.5		ms
Error Amplifier (EA)						
Error amplifier offset	V_{OS}		-3	0	3	mV
Feedback current	I_{FB}	V_{FB} = REF		50	100	nA
Enable (EN)						
Enable input rising threshold	VIH_{EN}		1.17	1.22	1.27	V
Enable hysteresis	$V_{EN\text{-}HYS}$			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge FET	R_{ON_DISCH}			80		Ω
VIN UVLO						
VIN under-voltage lockout threshold rising	$VIN_{Vth\text{-}Rise}$	VCC = 3.3V	2.25	2.55	2.85	V
VIN under-voltage lockout threshold falling	$VIN_{Vth\text{-}Fall}$		1.7	2	2.3	V

ELECTRICAL CHARACTERISTICS *(continued)*

VIN = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC under-voltage lockout threshold rising	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold falling	VCC_{Vth_Fall}		2.35	2.5	2.65	V
VCC output voltage	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		I_{CC} = 25mA		0.5		%
Power Good (PGOOD)						
Power good high threshold	$PG_{Vth\_Hi\_Rise}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{Vth\_Lo\_Rise}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth\_Lo\_Fall}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low-to-high delay	PG_{Td}	T_J = 25°C	0.7	1	1.3	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.5	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3V			3	µA
Power good low-level output voltage	V_{OL_100}	VIN = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor		650	850	mV
	V_{OL_10}	VIN = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor		800	1000	
Thermal Protection (OTP)						
OTP shutdown (5)	T_{SD}		150	160		°C
OTP shutdown hysteresis (5)	T_{SD_Hys}			20		°C

NOTES:

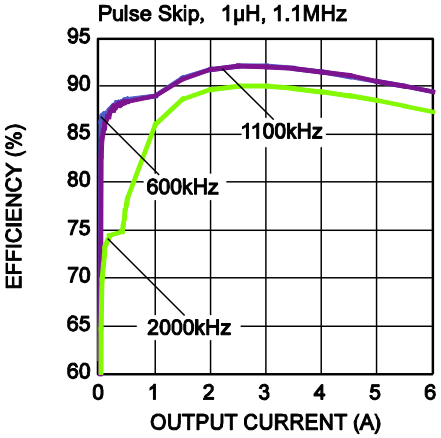
5) Specified by design and characterization. Not production tested.
6) Specified by design.

TYPICAL PERFORMANCE CHARACTERISTICS

VIN = 12V, V_{OUT} = 1.8V, L = 1µH, T_A = +25°C, unless otherwise noted.

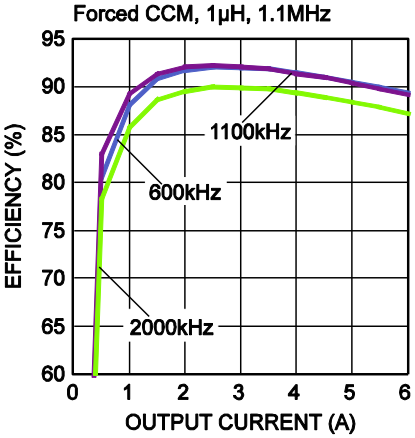
Efficiency (12V to 1.8V)

Pulse Skip, 1µH, 1.1MHz

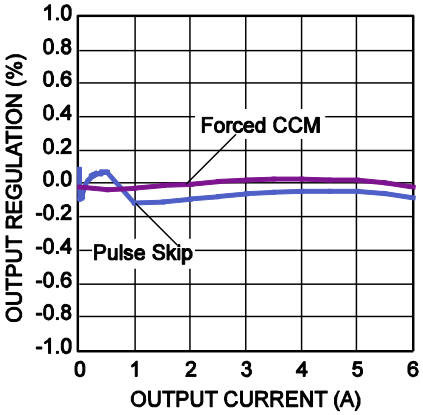


Efficiency (12V to 1.8V)

Forced CCM, 1µH, 1.1MHz

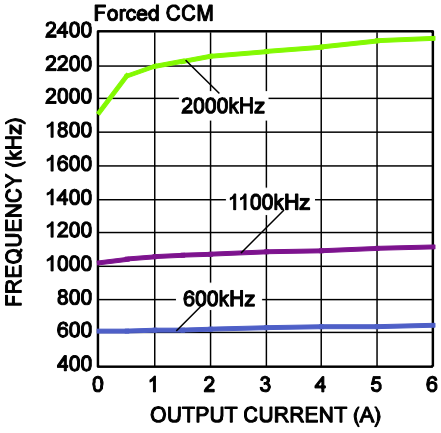


Load Regulation



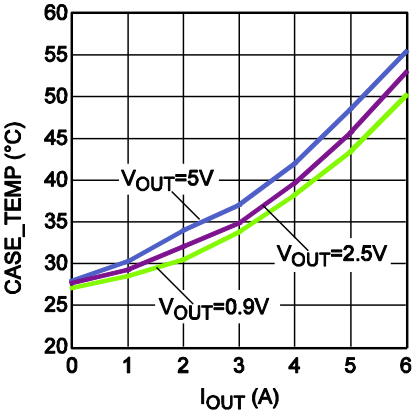
Switching Frequency vs. Output Current

Forced CCM



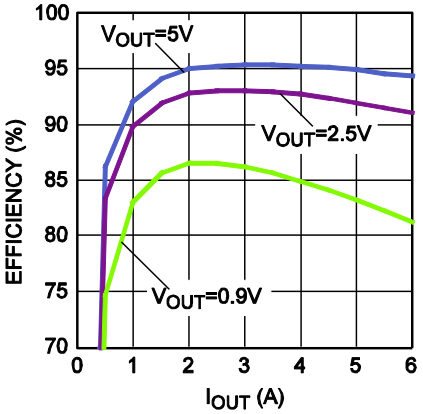
Thermal Results

1.1MHz, No Air-flow



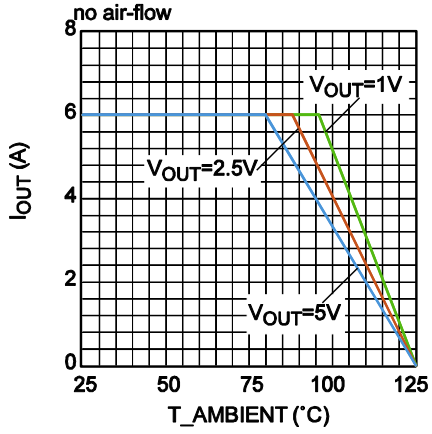
Efficiency

1.1MHz



Thermal Derating

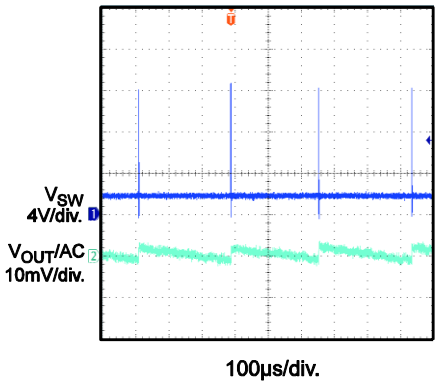
V_{IN}=12V, f_s=1.1MHz, T_J=125°C, no air-flow



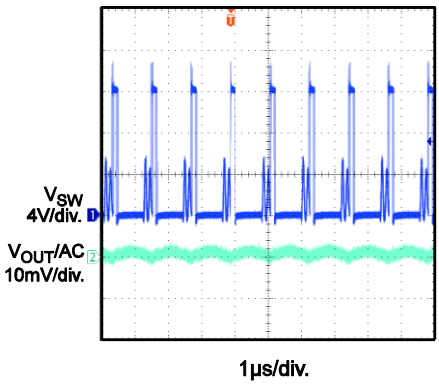
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1.8V, L = 1µH, T_A = +25°C, unless otherwise noted.

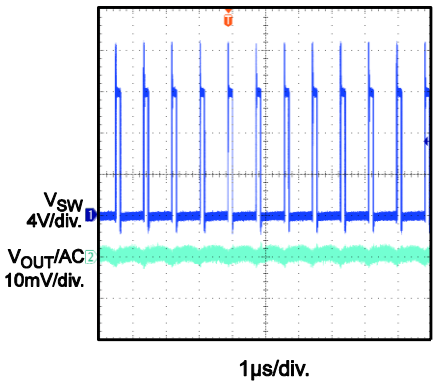
Steady State
I_{OUT}= 0A, Pulse Skip



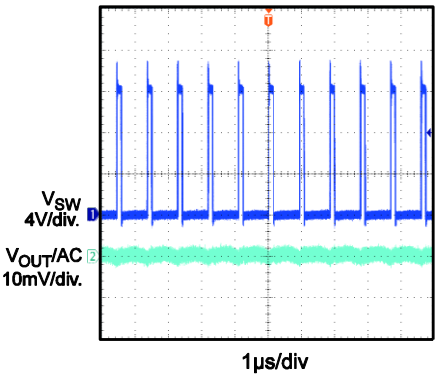
Steady State
I_{OUT} = 0.5A, Pulse Skip



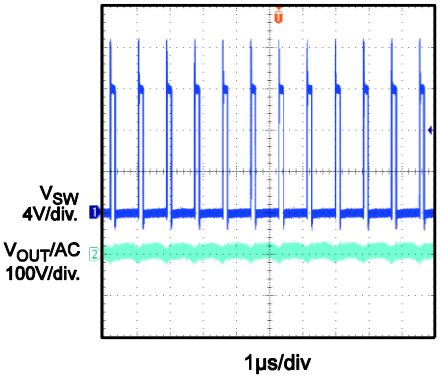
Steady State
I_{OUT} = 6A, Pulse Skip



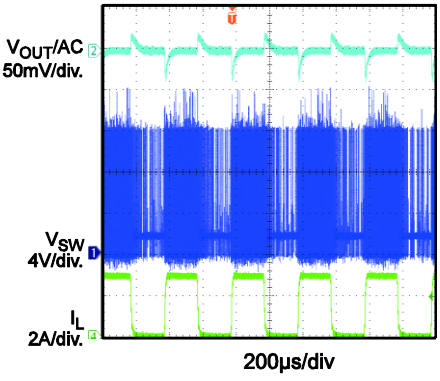
Steady State
I_{OUT} = 0A, Forced CCM



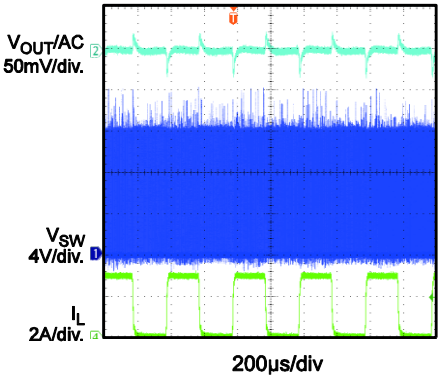
Steady State
I_{OUT} = 6A, Forced CCM



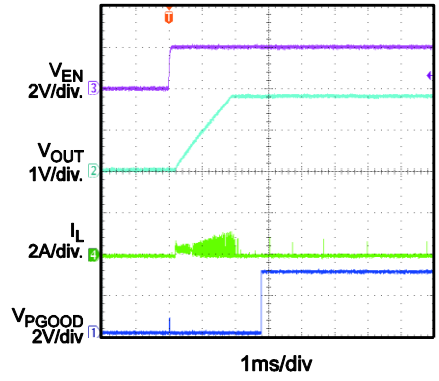
Load Transient
I_{OUT} = 0A-3A, Pulse Skip



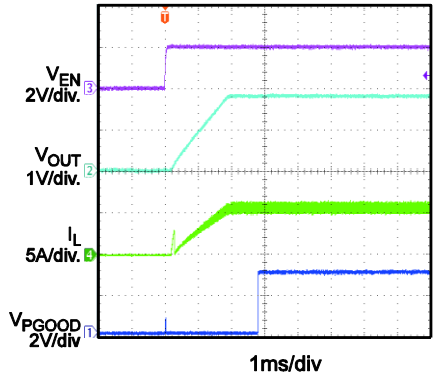
Load Transient
I_{OUT} = 0A-3A, Forced CCM



Power-Up through EN
I_{OUT}= 0A, Pulse Skip



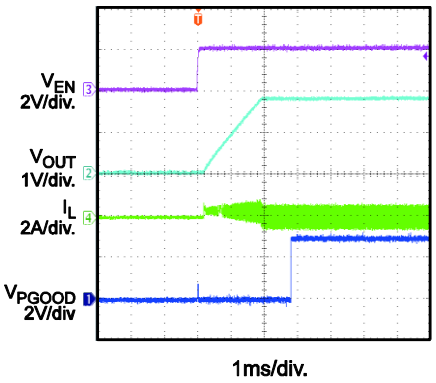
Power-Up through EN
I_{OUT}= 6A, Pulse Skip



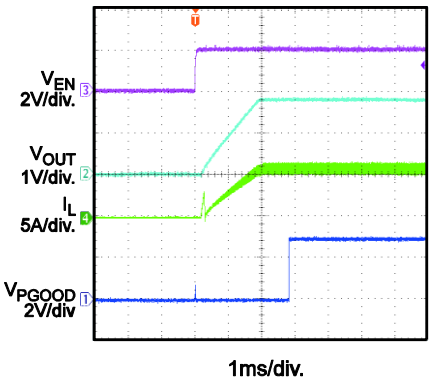
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1.8V, L = 1µH, T_A = +25°C, unless otherwise noted.

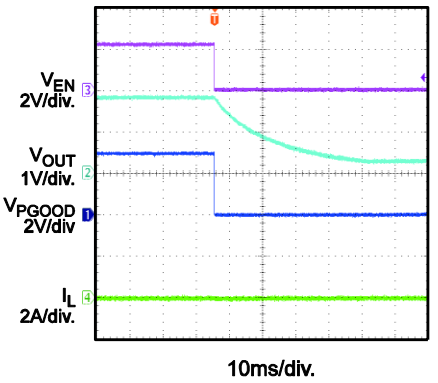
Power-Up through EN
I_{OUT} = 0A, Forced CCM



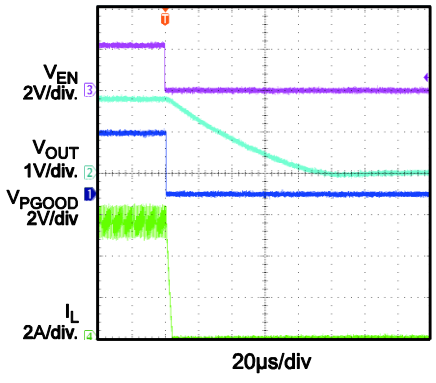
Power-Up through EN
I_{OUT} = 6A, Forced CCM



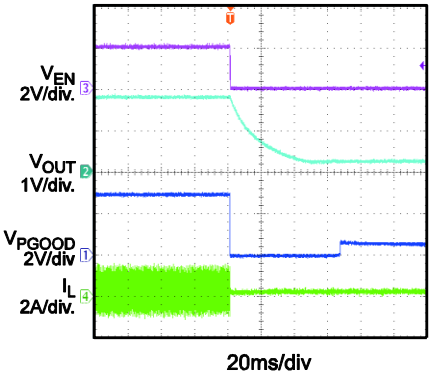
Power-Down through EN
I_{OUT} = 0A, Pulse Skip



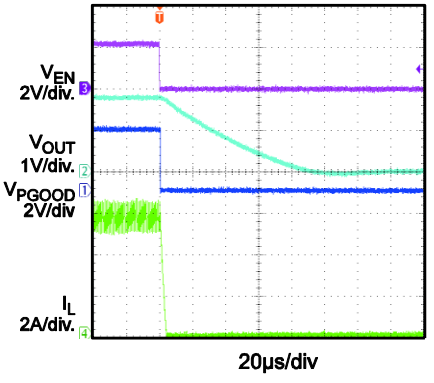
Power-Down through EN
I_{OUT} = 6A, Pulse Skip



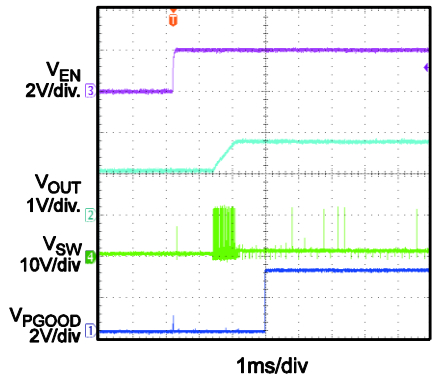
Power-Down through EN
I_{OUT} = 0A, Forced CCM



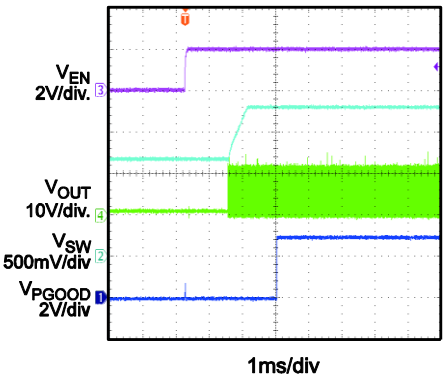
Power-Down through EN
I_{OUT} = 6A, Forced CCM



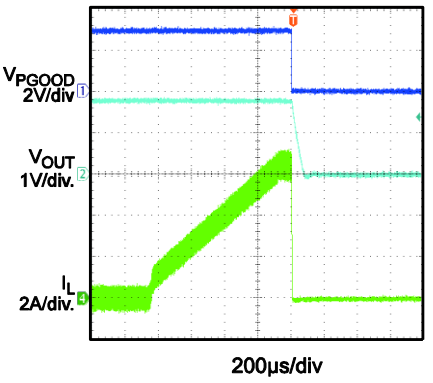
Pre-Bias Start-Up
Pulse Skip



Pre-Bias Start-Up
Forced CCM



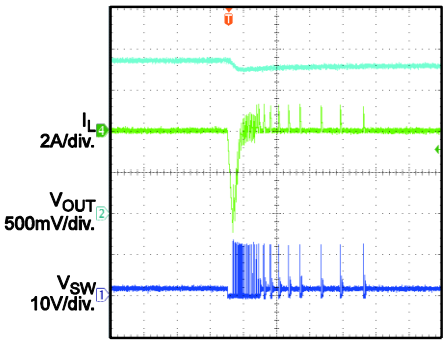
Over-Current Protection



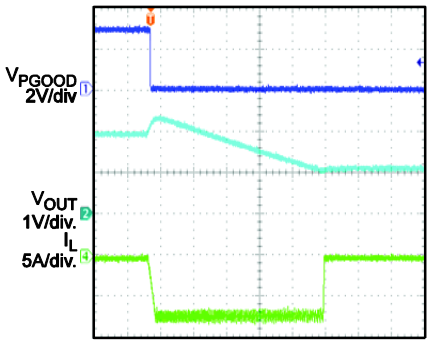
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VIN = 12V, V_{OUT} = 1.8V, L = 1µH, T_A = +25°C, unless otherwise noted.

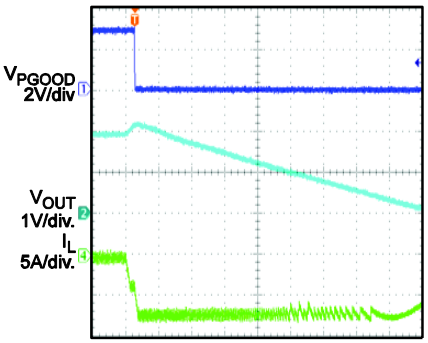
OSM Operation
Pulse Skip Mode



Over-Voltage Protection
Pulse Skip Mode



Over-Voltage Protection
Forced CCM



PIN FUNCTIONS

PIN #	Name	Description
1, 14	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during PCB layout. Connect using wide PCB traces.
2, 11	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Connect using wide PCB traces.
3	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed to decouple the input rail. Connect using wide PCB traces.
4	CS	**Current limit.** Connect a resistor to ground to set the current limit trip point. See Table 2 for additional details.
5	EN	**Enable.** EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
6	FB	**Feedback.** An external resistor divider from the output to AGND tapped to FB sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
7	AGND	**Analog ground.** Select AGND as the control circuit reference point.
8	TRK/REF	**External tracking voltage input.** The output voltage tracks this input signal. Decouple TRK/REF with a ceramic capacitor as close to it as possible. Ceramic capacitors with X7R or X5R grade dielectrics are recommended for their stable temperature characteristics. The capacitance of this capacitor determines the soft-start time. See Equation 2 and 3 for additional details.
9	PGOOD	**Power good output.** PGOOD is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate a logic high signal if the output voltage is within regulation. There is a delay of about 1ms from the time FB $\geqslant$ 92.5% and PGOOD pulling high.
10	BST	**Bootstrap.** Connect a capacitor between SW and BS to form a floating supply across the high-side switch driver.
12	MODE	**Operation mode selection.** Program MODE to select CCM, pulse-skip mode, and the operating switching frequency. See Table 1 for additional details.
13	VCC	**Internal 3V LDO output.** The driver and control circuits are powered from the VCC voltage. Decouple VCC with a minimum 1µF ceramic capacitor as close to it as possible. Ceramic capacitors with X7R or X5R grade dielectrics are recommended for their stable temperature characteristics.

BLOCK DIAGRAM

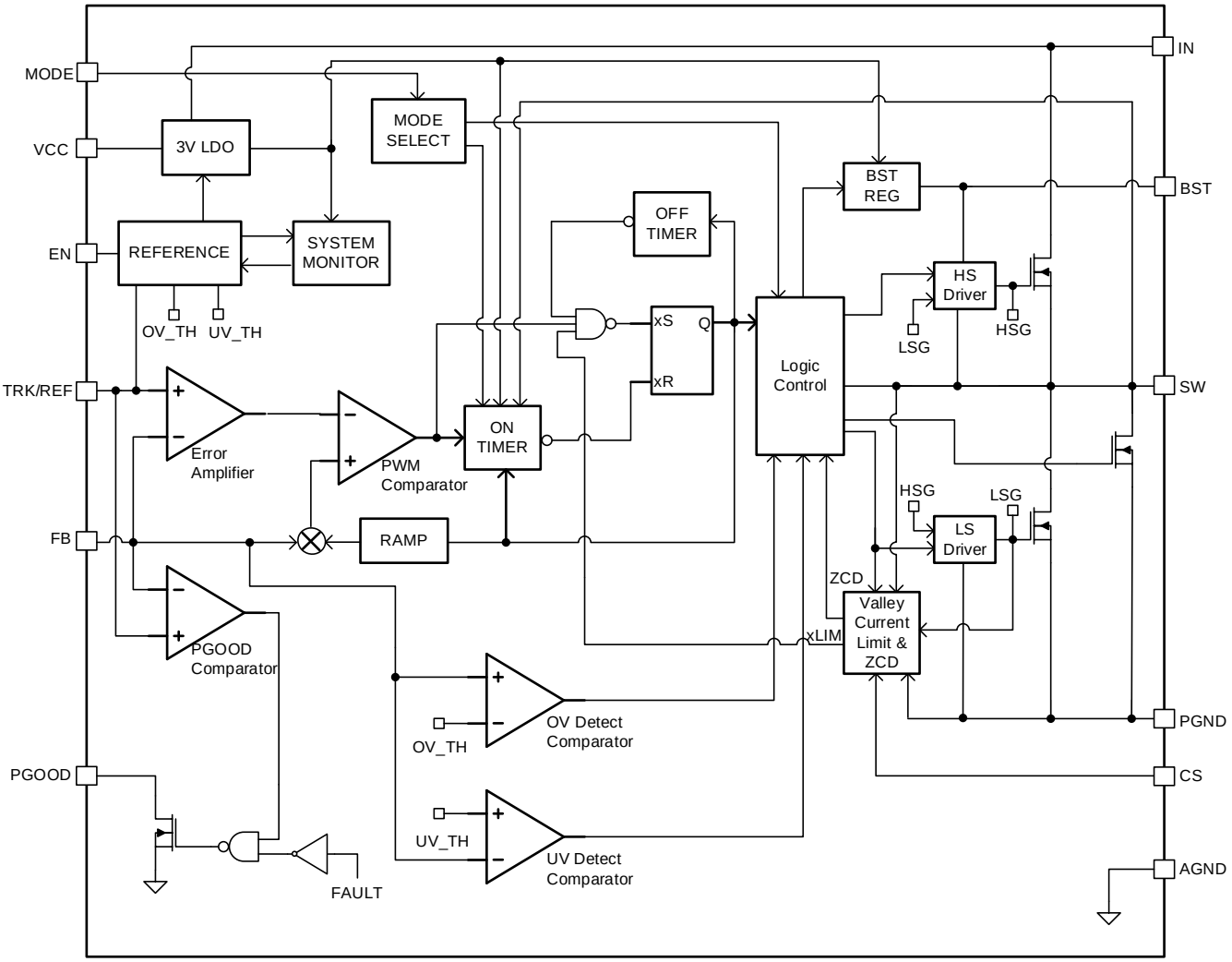


Figure 1: Functional Block Diagram

OPERATION

CONSTANT-ON-TIME (COT) Control

The MPQ8623 employs constant-on-time (COT) control to achieve fast load transient response. Figure 2 shows the details of the control stage of the MPQ8623.

The operational amplifier (AMP) corrects any error voltage between FB and VREF. The MPQ8623 can use AMP to provide excellent load regulation over the entire load range whether it is operating in forced continuous conduction mode (CCM) or pulse-skip mode.

The dedicated VSNS pin helps provide the feature of the differential output voltage remote sense. The pair of the remote sense trace should be kept at a low impedance to achieve the best performance.

The MPQ8623 has internal RAMP compensation to support low ESR MLCC output capacitor solutions. The adaptive internal RAMP is optimized so that the MPQ8623 is stable in the entire operating input/output voltage range with proper design of the output L/C filter.

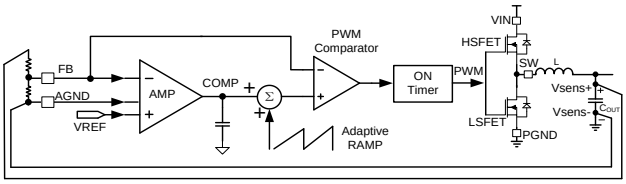


Figure 2: COT Control

PWM Operation

Figure 3 shows how the pulse-width modulation (PWM) signal is generated. AMP corrects any error between FB and REF and generates a fairly smooth DC voltage (COMP). The internal RAMP is superimposed onto COMP. The superimposed COMP is compared with the FB signal. Whenever FB drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) is turned on and remains on for a fixed turn-on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off. The HS-FET turns on again when FB drops below the superimposed COMP. By repeating this operation, the MPQ8623 regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time (shoot-through). In order to avoid a shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

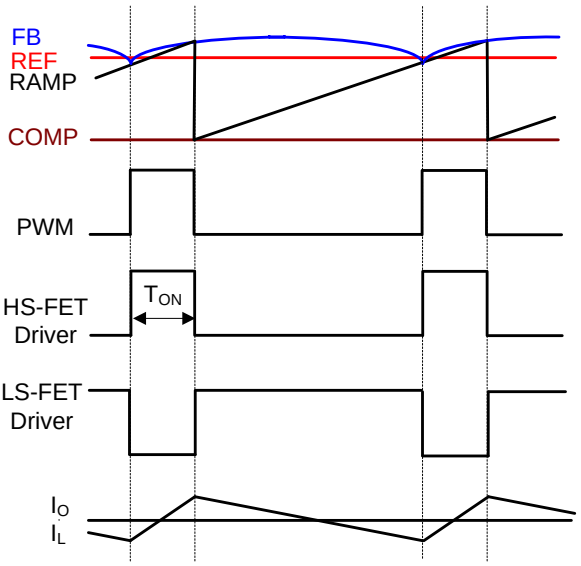


Figure 3: Heavy-Load Operation (PWM)

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps (see Figure 3). The MPQ8623 can also be configured to operate in forced CCM operation when the output current is low. See the Mode Selection section on page 14 for details.

In CCM operation, the switching frequency is fairly constant (PWM mode), so the output ripple remains almost constant throughout the entire load range.

Pulse-Skip Operation

At light-load condition, the MPQ8623 can be configured to work in pulse-skip mode to optimize efficiency. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MPQ8623 transitions from CCM to pulse-skip mode if the MPQ8623 is configured in this way. See the Mode Selection section on page 14 for details.

Figure 4 shows pulse-skip mode operation at light-load condition. When FB drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse-skip mode operation, FB does not reach the superimposed COMP when the inductor current approaches zero. The LS-FET driver turns into tri-state (high-Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. Therefore, the output capacitors discharge slowly to PGND through the LS-FET. At light-load condition, the HS-FET is not turned on as frequently in pulse-skip mode as it is in forced CCM. As a result, the efficiency in pulse-skip mode is improved greatly compared to that in forced CCM operation.

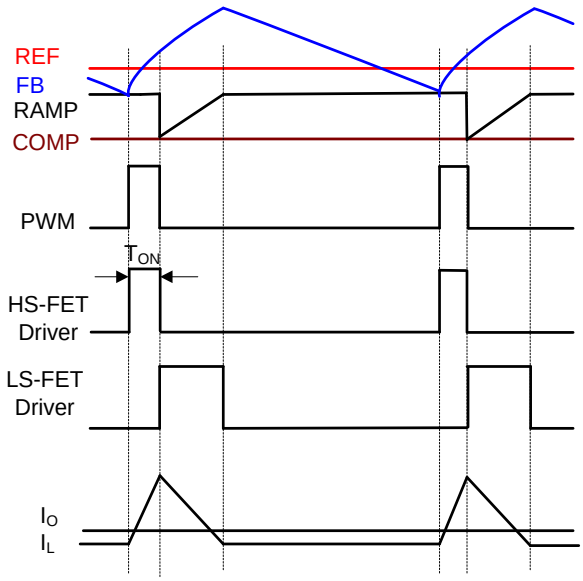


Figure 4: Pulse Skip in Light Load

As the output current increases from the light-load condition, the time period the current modulator regulates in becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches critical levels when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Where F_{SW} is the switching frequency.

The MPQ8623 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MPQ8623 can be configured to operate in forced CCM even in light-load condition (see Table 1).

Mode Selection

The MPQ8623 provides both forced CCM operation and pulse-skip operation in light-load condition. The MPQ8623 has three options for switching frequency. Selecting the operation mode under light-load condition and the switching frequency is done by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: Mode Selection

MODE	Light-Load Mode	Switching Frequency
AGND	Forced CCM	1100kHz
30.1kΩ (±20%) to AGND	Forced CCM	2000kHz
60.4kΩ (±20%) to AGND	Forced CCM	600kHz
121kΩ (±20%) to AGND	Pulse skip	600kHz
243kΩ (±20%) to AGND	Pulse skip	2000kHz
VCC	Pulse skip	1100Hz

Soft Start (SS)

The minimum soft-start time is limited to 1.5ms. This can be increased by choosing the capacitance between TRK/REF and AGND. A minimum value of 3.3nF for this capacitor is always required to stabilize the reference voltage.

The capacitance of this capacitor can be determined with Equation (2) and Equation (3):

$$C_{REF}(nF) = 3.3 \sim 17 \quad (t_{SS} = 1.5ms) \quad (2)$$

$$C_{REF}(nF) = \frac{t_{ss}(ms) \times 10\mu A}{0.9V} \quad (t_{SS} > 1.5ms) \quad (3)$$

Output Voltage Tracking and Reference

The MPQ8623 provides an analog input pin (TRK/REF) to track another power supply or accept an external reference voltage. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MPQ8623 output voltage. The FB voltage follows this external voltage signal exactly, and the soft-start settings are ignored. The TRK/REF input signal can be in the range of 0.3V to 1.4V. During the initial start-up, the TRK/REF must reach 900mV or above first to ensure proper operation. Afterward, TRK/REF can be set to any value between 0.3V and 1.4V.

Pre-Bias Start-Up

The MPQ8623 has been designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the TRK/REF capacitor exceeds the sensed output voltage at FB. Before the TRK/REF voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop in the pre-biased level is negligible.

Output Voltage Discharge

When the MPQ8623 is disabled through EN, the output voltage discharge mode is enabled. This causes both the HS-FET and the LS-FET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once the FB voltage drops below 10%*REF, the discharge FET is turned off.

Current Sense and Over-Current Protection (OCP)

The MPQ8623 features an on-die current sense and a programmable positive current limit threshold. The current limit is active when the MPQ8623 is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, the V_{CS} voltage is proportional to the SW current cycle-by-cycle. The HS-FET is only allowed to turn on when the V_{CS} voltage is below the internal OCP voltage threshold (V_{OCP}) during the LS-FET on state to limit the SW valley current cycle-by-cycle.

Calculate the current limit threshold setting from R_{CS} with Equation (4):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_s})} \quad (4)$$

Where V_{OCP} = 1.2V, G_{CS} = 40μA/A, and I_{LIM} is the desired output current limit.

If the MPQ8623 detects an over-current condition for 31 consecutive cycles, or if FB drops below the under-voltage protection (UVP) threshold, it latches off. A power recycling of VCC or EN is needed to enable the part again.

There is some offset for the low current limit threshold setting. Refer to Table 2 for a more accurate setting.

Table 2: Threshold Setting

L_{LIM_DC} (A)	R_{CS} (KΩ)
8	3.83
7.5	4.02
7	4.32
6.5	4.64
6	4.87
5.5	5.49
5	5.9
4.5	6.49
4	7.15

Negative Inductor Current Limit

When the LS-FET detects a -8A current, the MPQ8623 turns off the LS-FET for 200ns to limit the negative current.

Output Sinking Mode (OSM)

The MPQ8623 employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When the FB voltage is higher than 105%*REF but is below the OVP threshold, OSM is triggered. During OSM operation, the LS-FET remains on until it reaches the -4A negative current limit. The LS-FET is then turned off momentarily for 80ns and is turned on again. The MPQ8623 repeats this operation until FB drops below 102%*REF. The MPQ8623 exits OSM after 15 consecutive cycles of forced CCM.

Over-Voltage Protection (OVP)

The MPQ8623 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides latch-off OVP mode.

If the FB voltage exceeds 116% of the REF voltage, the MPQ8623 enters latch-off OVP mode. The HS-FET latches off and PGOOD latches low until the power of VCC or EN are recycled. Meanwhile, the LS-FET remains on until it reaches the low-side negative current limit (NOCP). The LS-FET is then turned off momentarily for 80ns and is turned on again. The MPQ8623 repeats this operation to bring down the output voltage. When the FB voltage drops below 50% of the REF voltage, the LS-FET is turned off for pulse-skip mode and continues turning on for forced CCM operation. If FB rises back to more than 116% of the REF voltage, the LS-FET turns on again with NOCP until FB drops back below 50% of the REF voltage. The power of EN or VIN must be recycled to clear the OVP fault. The OVP function is enabled after TRK/REF reaches 900mV.

Over-Temperature Protection (OTP)

The MPQ8623 has over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off.

This is a latch-off protection. The power of VCC or EN must be recycled to enable the MPQ8623 again.

Output Voltage Setting and Remote Output Voltage Sensing

First, choose a value for R1. Then R2 can be determined with Equation (5):

$$R_2(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_1(k\Omega) \quad (5)$$

Where V_{REF} = 900mV.

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is recommended to be in parallel with R1. R1 and C_{FF} add an extra zero to the system, which improves loop response. R1 and C_{FF} are selected so that the zero formed by R1 and C_{FF} is located around 5kHz to 40kHz. f_Z can be determined with Equation (6):

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}} \quad (6)$$

Power Good (PGOOD)

The MPQ8623 has a power good (PGOOD) output. PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source less than 3.6V through a pull-up resistor (10kΩ, typically). After applying the input voltage and EN is high, the MOSFET turns on, so PGOOD is pulled to GND before TRK/REF is ready. After the FB voltage reaches 92.5% of the REF voltage, PGOOD is pulled high after a 0.8ms delay.

When the FB voltage drops to 80% of the REF voltage or exceeds 116% of the nominal REF voltage, PGOOD is latched low. PGOOD can only be pulled high again after a new SS.

If the input supply fails to power the MPQ8623, PGOOD is clamped low, even though PGOOD is tied to an external DC source through a pull-up resistor. The relationship between the PGOOD voltage and the pull-up current is shown in Figure 5.

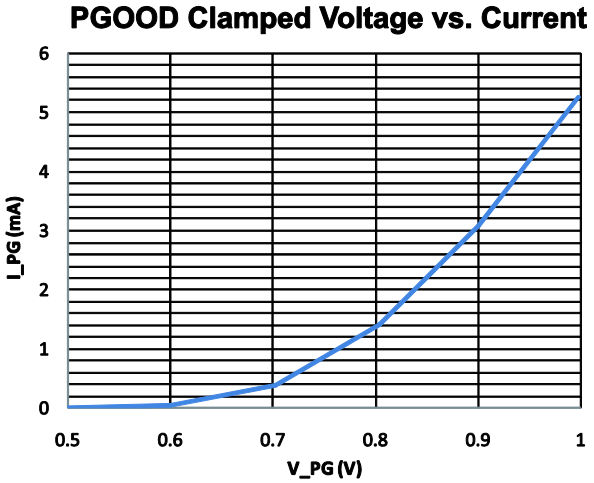


Figure 5: PGOOD Clamped Voltage vs. Pull-Up Current

Enable (EN) Configuration

The MPQ8623 turns on when EN goes high and turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MPQ8623.

The MPQ8623 provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage at which the MPQ8623 is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible UVLO bouncing during power-up and power-down. The resistor divider values can be determined with Equation (7):

$$V_{IN\_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (7)$$

Where VIH_{EN} = 1.22V, typically.

R_{UP} and R_{DOWN} should be chosen so that V_{EN} does not exceed 3.6V when VIN reaches the maximum value.

EN can also be connected to VIN directly through a pull-up resistor (R_{UP}). R_{UP} should be chosen so that the maximum current going to EN is 50μA. R_{UP} can be calculated with Equation (8):

$$R_{UP}(k\Omega) = \frac{VIN_{MAX}(V)}{0.05(mA)} \quad (8)$$

Enable (EN) Thresholds

The MPQ8623 has two EN thresholds. One is the LDO EN rising threshold, and the other is the EN input rising threshold. During power-up, once EN reaches the LDO EN rising threshold (typically 0.7V), the internal LDO is enabled, and V_{CC} starts to increase. Once EN reaches the EN input rising threshold, the device is enabled and starts to switch.

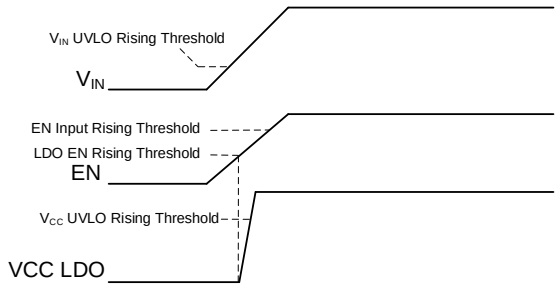


Figure 6: Power-Up Sequence with Internal LDO and Two EN Thresholds

Power Sequence with External VCC Bias

The MPQ8623 supports using an external 3.3V VCC bias (see Figure 7). When the external VCC bias is used, it is recommended to apply the external VCC bias before the V_{IN} UVLO rising threshold or LDO EN rising threshold is reached. If the external VCC bias is applied after the V_{IN} UVLO rising threshold and LDO EN rising threshold are reached, the LDO must output and provide power to the load, which is supposed to be supplied by the external VCC.

Depending on the load condition of the external VCC, the LDO might be overloaded until the external VCC bias is applied. It is recommended to power off the external VCC bias after the V_{IN} UVLO falling threshold or LDO EN falling threshold is reached.

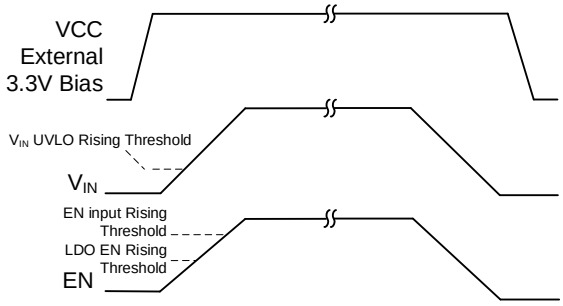


Figure 7: Power-Up Sequence with External VCC Bias

APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range. The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (9):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (9)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, shown in Equation (10):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (10)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirements.

Estimate the input voltage ripple with Equation (11):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The worst-case condition occurs at VIN = $2V_{OUT}$, with Equation (12):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (12)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAPs. Estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (13)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (14)$$

The ESR dominates the switching frequency impedance for POSCAPs. For simplification, the output ripple can be approximated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (15)$$

Inductor

The inductor supplies a constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical size, a higher series resistance, and a lower saturation current. Generally, select an inductor value that allows the inductor peak-to-peak ripple current to be 30% to 40% of the maximum switch current limit. Also design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value with Equation (16):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (17):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (17)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best performance, refer to Figure 8 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MPQ8623.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. Place as many PGND vias as possible as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the BST capacitor as close to BST and SW as possible.
8. Use traces with a width of 20mil or wider to route the path.
9. Use a 0.1µF to 1µF bootstrap capacitor.
10. Place the REF capacitor close to TRK/REF to AGND.
11. Do not place vias on the VB trace.
12. Use a 10Ω to 49.9Ω resistor for R_{PG} and a 1nF capacitor for C_{PG}.
13. Use a 1nF capacitor for C_{OL}.

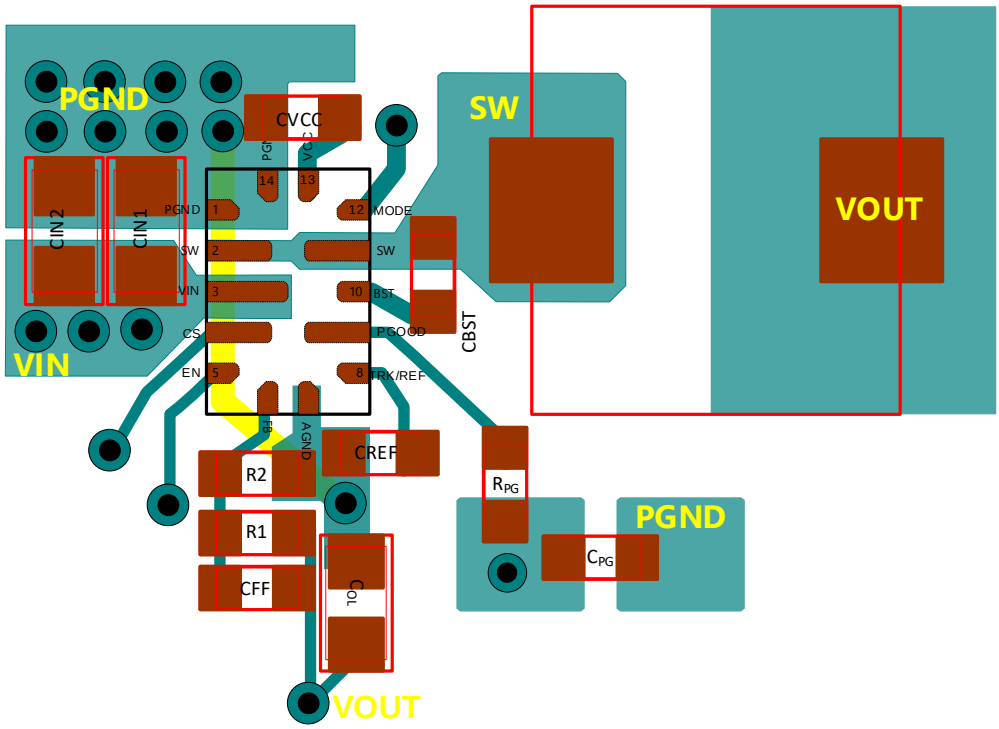
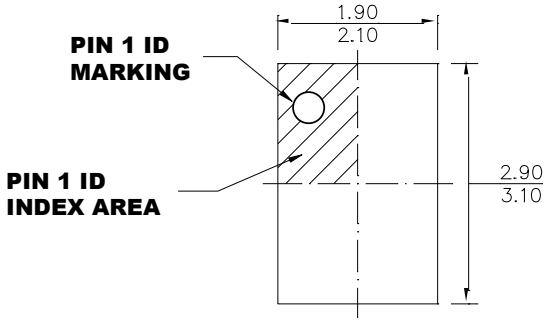


Figure 8: Example of PCB Layout (Placement & Top Layer PCB)

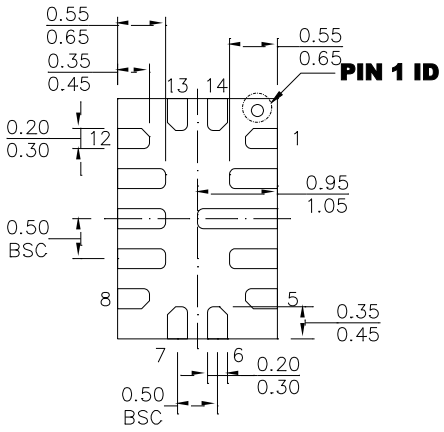
NOTE: Via size is 20/10mils.

PACKAGE INFORMATION

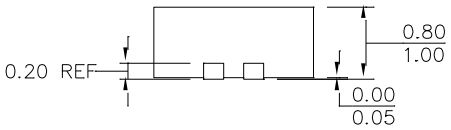
QFN-14 (2mmx3mm)



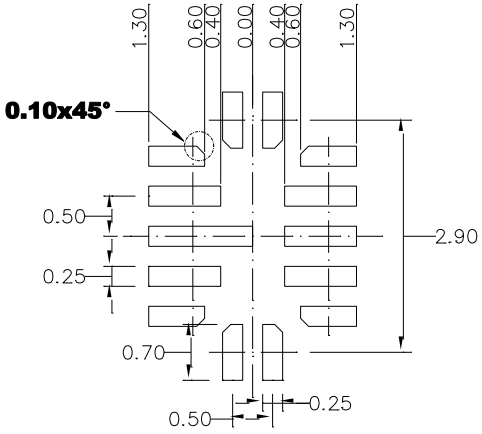
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN1,5,8 AND PIN12 HAVE THE SAME SHAPE.
2) LAND PATTERNS OF PIN2,4,9,10 AND PIN11 HAVE THE SAME SHAPE.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/27/2017	Initial Release	-
1.01	9/5/2018	Added more application to the Applications section	1
		Added the HS on-state resistance and LS on-state resistance parameters to the Electrical Characteristics section	5
		Added OTP shutdown hysteresis to the Electrical Characteristics section	6
		Added Table 2	15
		Deleted the Typical Application Circuit section	20
1.1	3/26/2024	Updated Typical Application Circuit (designs to VIN, PGOOD, VCC, MODE, and VOUT): • Removed CIN; added C_{IN1} and C_{IN2} • Added R_{PG}, C_{PG}, and R5 • Added R6 • Added R7 • Removed COUT; added C_{OL}, C_{O1}, and C_{O2}	2
		Updated the Absolute Maximum Ratings section: • Deleted: V_{SW} (DC), V_{SW} (25ns), VSW (25ns), VBST • Added: V_{IN} - V_{SW} (DC), V_{IN} - V_{SW} (25ns), V_{SW} (DC), V_{SW} (25ns), V_{BST}, V_{BST} - V_{SW} (25ns) • Deleted from Recommended Operating Conditions: V_{IN} (DC) – V_{SW} (DC), V_{SW} (DC) • Updated Thermal Resistance (6) to Thermal Resistance (4) • Deleted Notes 4 and 5; Note 6 became Note 4	4
		Updated Notes 7 and 8 to Notes 5 and 6, respectively	5–6
		Update Functional Block Diagram • Changed SW connection	12
		• Updated the fz range from “20~60kHz” to “5kHz to 40kHz” in Output Voltage Setting and Remote Output Voltage Sensing section • Added “After applying the input voltage and EN is high,” to the Power Good (PGOOD) section	16
		• Added the Enable (EN) Thresholds and Power Sequence with External VCC Bias sections • Added Figure 6 and Figure 7	17
		Updated the PCB Layout Guidelines section: • Added step 11: “Do not place vias on the VB trace.” • Added step 12: “Use a 10Ω to 49.9Ω resistor for R_{PG} and a 1nF capacitor for C_{PG}." • Added step 13: “Use a 1nF to 100nF capacitor for C_{OL}.” • Updated Figure 6 to Figure 8 and made changes	19