NB682

28V, 3A, Low IQ, Wide Output Synchronous Buck Converter with 2-Bit VID

NOT RECOMMENDED FOR NEW DESIGNS, REFER TO NB695

DESCRIPTION

The NB682 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with 2-Bit VID, especially designed for IMVP8 applications—VCCIO, PRIMCORE, V1.0A, EDRAM, and EOPIO, as well as other POLs (1.8V/2.5V/3.3V). It offers a very compact solution to achieve a 3A continuous output current and a 4A peak output current over a wide input supply range.

The NB682 operates at high efficiency over a wide output current load range based on MPS proprietary switching loss reduction technology and internal low Ron power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

NB682 provides both a low-power mode for power-loss saving during the low-power state and ultrasonic mode to avoid audible noise.

Full protection features include OC Limit, OVP, UVP, and thermal shutdown (TSD).

The converter requires a minimum number of external components and is available in a QFN-13 2mm x 3mm package.

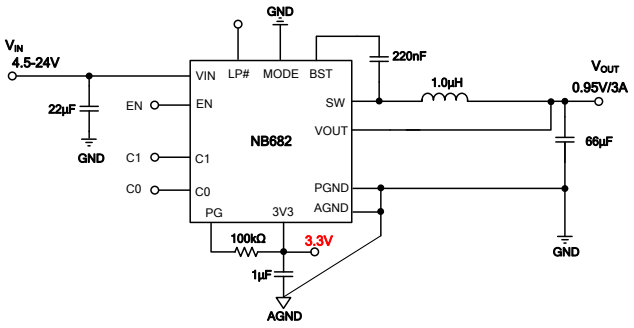
FEATURES

- Wide 4.5V to 28V Operating Input Range
- VCCIO/PRIMCORE/EDRAM/EOPIO/V1.0A/ 1.8V/2.5V/3.3V Compatible for IMVP8
- Wide Output Adjustable by 2-Bit VID
- Low-Power Mode
- 25µA Low Quiescent Current
- 3A Continuous Output Current
- 4A Peak Output Current
- Selectable Ultrasonic Mode
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- Stable with POSCAP and Ceramic Capacitors
- 1% Reference Voltage
- Internal Soft Start
- Output Discharge
- UVP, OVP, OCL, and Thermal Shutdown
- Latch-Off Re-Set via EN or Power Cycle
- Lead and Halogen-Free, RoHS Compliant
- Available in a QFN-13 2mm x 3mm Package

APPLICATIONS

- Laptop Computers/Tablet PCs
- Networking Systems
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
NB682GD	QFN-13 (2mm x 3mm)	*See Below*

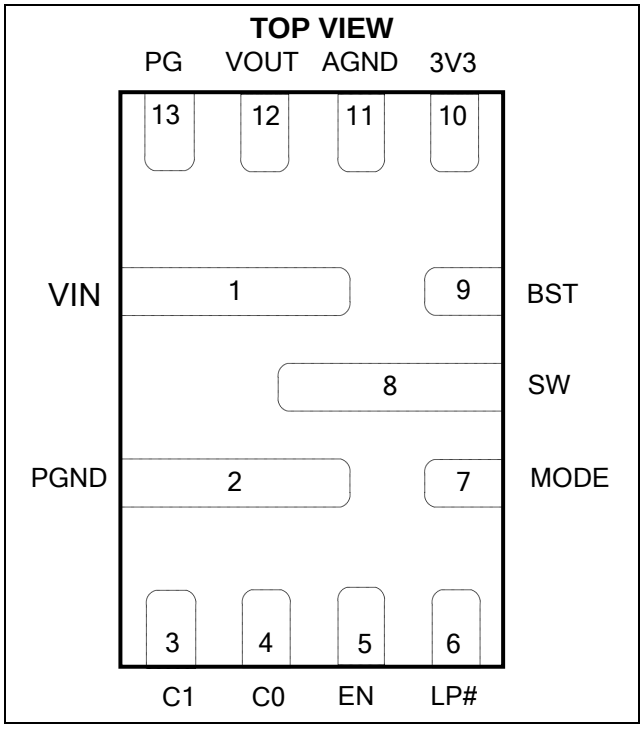
* For Tape & Reel, add suffix –Z (e.g. NB682GD–Z)

TOP MARKING

ANJY
LLL

ANJ: Product code of NB682GD
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 28V
V_{SW}(DC) ..... -1V to 26V
V_{SW} (25ns) ..... -3.6V to 28V
V_{BST} ..... V_{SW} + 4.5V
I_{EN} 100µA
All other pins ..... -0.3V to +4.5V
Continuous power dissipation (T_A = +25°C)(2)
QFN-13 2mm x 3mm 1.8W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.5V to 24V
Supply voltage (V_{CC}) ..... 3.15V to 3.5V
Enable current (I_{EN}) 50µA
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN (2mm x 3mm)	70	15	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, 3V3 = 3.3V, T_J = 25°C, LP# = 1, C1 = 1, C0 = 0, Mode = 0, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
3V3 supply current in normal mode	I_{3V3}	V_{EN} = 3.3V, $V_{LP\#}$ = 3.3V, V_{OUT} = 1V		150		μA
3V3 supply current in LP# mode	$I_{3V3\_LP\#}$	V_{EN} = 3.3V, $V_{LP\#}$ = 0		30		μA
3V3 shutdown current	I_{3V3_SDN}	V_{EN} = 0V			1	μA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}			36		mΩ
Low-side switch on resistance	LS_{RDS-ON}			13		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side valley current limit	I_{LIMIT_LS}		3.5	4	4.5	A
Switching Frequency and Minimum Off Timer						
Switching frequency(5)	F_S	Default		750		kHz
Constant on timer	Ton	V_{IN} = 5V, V_{OUT} = 1.0V	220	290	350	ns
Minimum on time(5)	T_{ON_Min}			50		ns
Minimum off time(5)	T_{OFF_Min}			250		ns
Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}	V_{FB}	120%	130%	135%	V_{REF}
UVP-1 threshold	V_{UVP}	V_{FB}	70%	75%	80%	V_{REF}
UVP-1 hold off timer(5)	T_{OC}	V_{OUT} = 60% V_{REF}		64		μs
UVP-2 threshold	V_{UVP}	V_{FB}	45%	50%	55%	V_{REF}
Reference and Soft Start						
Internal reference voltage	V_{REF}, MODE=0	LP# = 0(5)		0		mV
		LP# = 1, C1 = 0, C0 = 0		850		mV
		LP# = 1, C1 = 0, C0 = 1		875		mV
		LP# = 1, C1 = 1, C0 = 0	940	950	960	mV
		LP# = 1, C1 = 1, C0 = 1		975		mV
	V_{REF}, MODE=Float	LP# = 0		700		mV
		LP# = 1, C1 = 0, C0 = 0		850		mV
		LP# = 1, C1 = 0, C0 = 1		900		mV
		LP# = 1, C1 = 1, C0 = 0		950		mV
		LP# = 1, C1 = 1, C0 = 1		1000		mV
	V_{REF}, MODE=100k	LP# = 0(5)		0		mV
		LP# = 1, C1 = 0, C0 = 0		800		mV
		LP# = 1, C1 = 0, C0 = 1		950		mV
		LP# = 1, C1 = 1, C0 = 0	990	1000	1010	mV
		LP# = 1, C1 = 1, C0 = 1		1050		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, 3V3 = 3.3V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Internal reference voltage	V_{REF}, **MODE=150k**	LP# = 0, C1 = 0, C0 = 0		1590		mV
		LP# = 0, C1 = 0, C0 = 1		1990		mV
		LP# = 0, C1 = 1, C0 = 0		2380		mV
		LP# = 0, C1 = 1, C0 = 1		3300		mV
		LP# = 1, C1 = 0, C0 = 0		1200		mV
		LP# = 1, C1 = 0, C0 = 1		1500		mV
		LP# = 1, C1 = 1, C0 = 0		1800		mV
		LP# = 1, C1 = 1, C0 = 1		2500		mV
Soft-start time	T_{SS}	En to PG up	1.0	1.3	1.5	ms
VID change slew rate	SR_{VID}	MODE = float	5		10	mV/µs
		MODE = 100k	25		35	mV/µs
		MODE = 0	10		20	mV/µs
VID change timer (EOPIO) (5)	T_{VID_EOPIO}	MODE = 100k			10	µs
LP# exit timer(5)	$T_{LP\#\_exit}$	MODE = float			45	µs
		MODE = 0/100k			240	µs
MODE						
Mode source current	I_{MODE}		9	10	11.6	µA
Enable and UVLO						
EN UVLO rising threshold	$V_{EN\_H\_UVLO}$		1.1	1.2	1.3	V
EN hysteresis	V_{EN_HYS}			100		mV
EN high limit @ USM	$V_{EN\_H\_USM}$				1.7	V
EN low limit @ normal(5)	$V_{EN\_L\_Normal}$		2.3			V
Enable input current	I_{EN}	V_{EN} = 3.3V		5		µA
		V_{EN} = 0V		0		
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.8	3.0	3.13	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			200		mV
VIN under-voltage lockout threshold rising	VIN_{VTH}			4.2	4.4	V
VIN under-voltage lockout threshold hysteresis	VIN_{HYS}			300		mV
LP# , C1, C0 Logic						
Rising threshold	V_{LH}		0.39	0.6	0.79	V
Hysteresis	V_{LHYS}			100		mV
Input current	I_{LIN}	$V_{LP\#,C1,C0}$ = 3.3V			1	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, 3V3 = 3.3V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good						
PG when V_{OUT} risng (good)	$PG_{\_Rising(GOOD)}$	V_{FB} rising, percentage of V_{REF}		95		
PG when V_{OUT} falling (fault)	$PG_{\_Falling(Fault)}$	V_{FB} falling, percentage of V_{REF}		90		
PG when V_{OUT} rising (fault)	$PG_{\_Rising(Fault)}$	V_{FB} rising, percentage of V_{REF}		115		
PG when V_{OUT} falling (good)	$PG_{\_Falling(GOOD)}$	V_{FB} falling, percentage of V_{REF}		105		
Power good low to high delay	PG_{Td}			2	7	µs
EN low to power good low delay	$PG_{Td\_EN\ low}$				1	µs
PG sink-current capability	V_{PG}	Sink 4mA			0.4	V
Thermal Protection						
Thermal shutdown(5)	T_{SD}			145		°C
Thermal shutdown hysteresis(5)	T_{SD_HYS}			25		°C

NOTE:

5) Guaranteed by design.

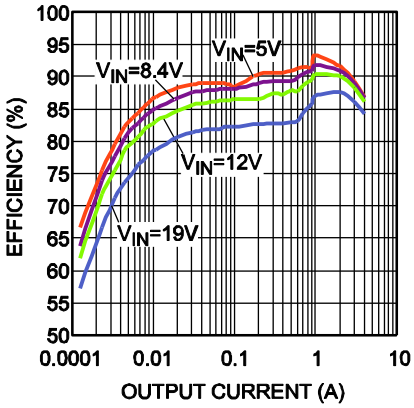
PIN FUNCTIONS

PIN #	Name	Description
1	VIN	**Supply voltage input**. The NB681 operates from a +4.5V to +24V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection with at least two layers for the input trace.
2	PGND	**Power ground**. Use wide PCB traces and multiple vias to make the connection.
3-4	C1, C0	**2-bit VID control input**. Set C1 and C0 with MODE to get different voltage references for different rails. C1 and C0 are pulled high internally.
5	EN	**Enable.** Drive EN high to turn on the buck regulator; drive EN low to turn off the buck regulator. (There is an internal 800kΩ pull-down resistor.) EN determines USM. If EN is within 1.3V-1.7V, it is in USM. If EN >2.3 V, it is in normal mode. For normal operation, it is recommended that EN rising finishes in < 1ms.
6	LP#	**Low-power mode control signal.** Pull LP# high during normal operation. Pull LP# low to enter low-power mode. Usually, LP# is controlled by the SLP#S0 of the system. LP# is pulled high internally.
7	MODE	**Selects VCCIO/PRIMCORE/EDRAM/EOPIO/V1.0A.** Also, MODE selects other POLs (like 1.8V/2.5V/3.3V for IMVP8 applications **with external 1% resistors**)**.**
8	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is connected to VIN when the HS-FET is on; SW is connected to PGND when the LS-FET is on. Use wide and short PCB traces to make the connection. SW is noisy, so keep sensitive traces away from SW.
9	BST	**Bootstrap.** A > 100nF capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
10	3V3	**External 3V3 VCC input for control and driver**. Place a 1µF decoupling capacitor close to 3V3 and AGND.
11	AGND	**Signal logic ground.** Make a Kelvin connection to PGND near the VCC capacitor. AGND can be applied as a remote sense ground with proper setting.
12	VOUT	**Output sense input.** Connect the VOUT to the remote output capacitor with good GND decoupling. Keep the VOUT trace away from SW or other noisy nodes. It is recommended to use a >20mil trace for the VOUT sense.
13	PG	**Power good output**. PG is an open-drain signal. PG is high if the output voltage is higher than 95% of the nominal voltage or lower than 105% of the nominal voltage.

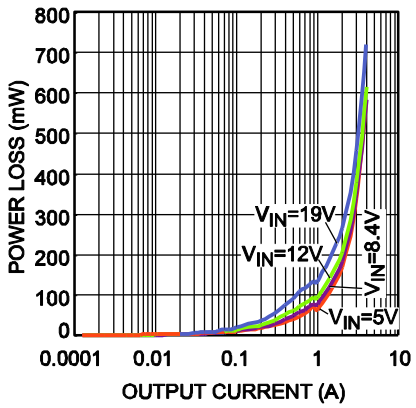
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 1.0µH/10mΩ, R_{mode} = 100kΩ, LP# = C1 = 1, C0 = 0, R_{bst} = 0, T_J = +25°C, C_{OUT} = 22µF*3 unless otherwise noted.

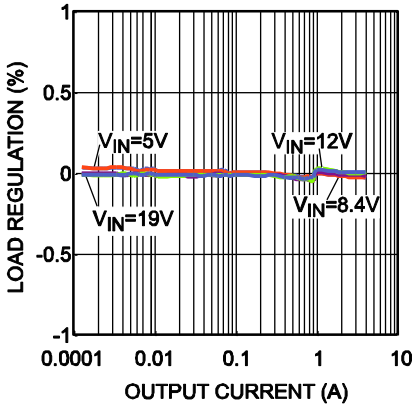
Efficiency vs. Load Current



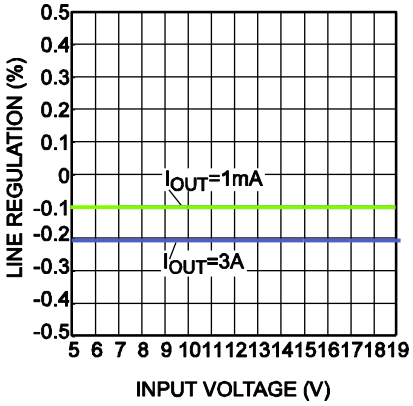
Power Loss



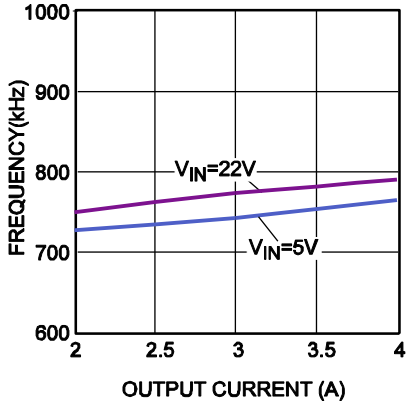
Load Regulation



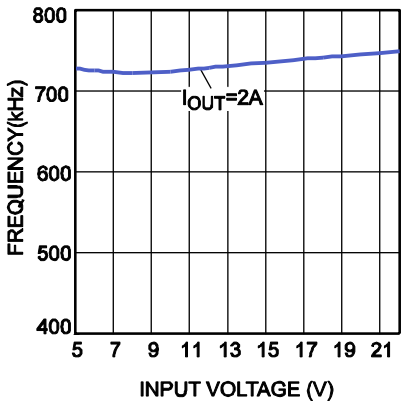
Line Regulation



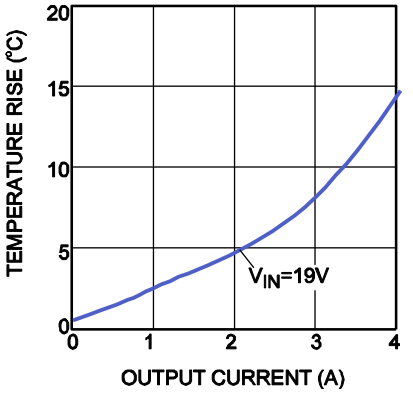
Switch Frequency vs. Output Current



Switch Frequency vs. Input Voltage



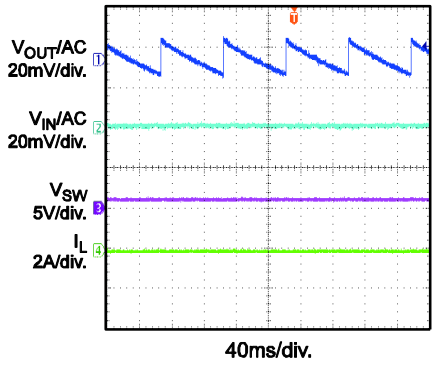
Temperature Rise vs. Load Current



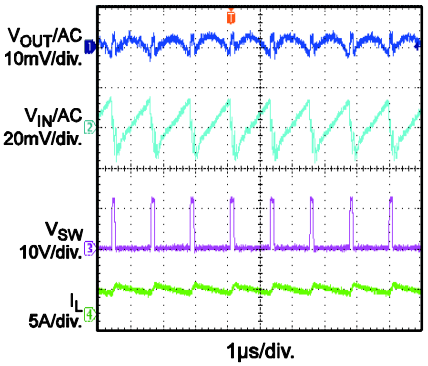
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 1.0µH/10mΩ, R_{mode} = 100kΩ, LP# = C1 = 1, C0 = 0, R_{bst} = 0, T_J = +25°C, C_{OUT} = 22µF*3 unless otherwise noted.

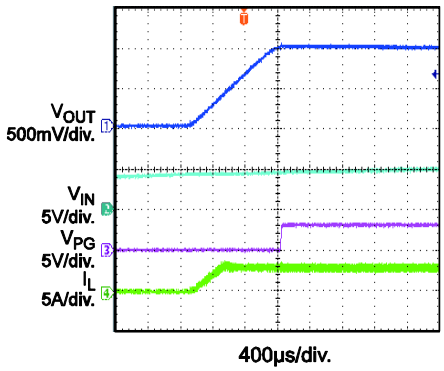
Input/Output Voltage Ripple
I_{OUT} = 0A



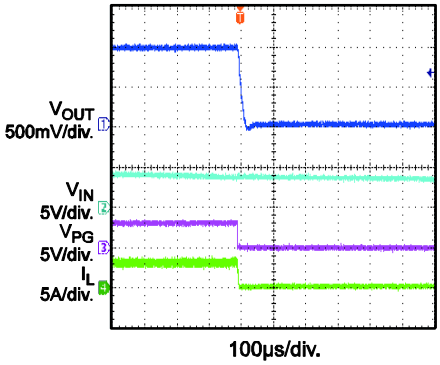
Input/Output Voltage Ripple
I_{OUT} = 3A



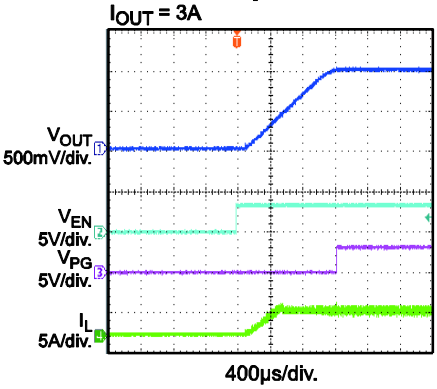
Power Good through V_{IN} Start-Up
I_{OUT} = 3A



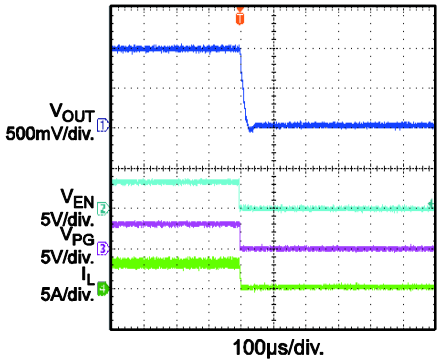
Power Good through V_{IN} Shutdown
I_{OUT} = 3A



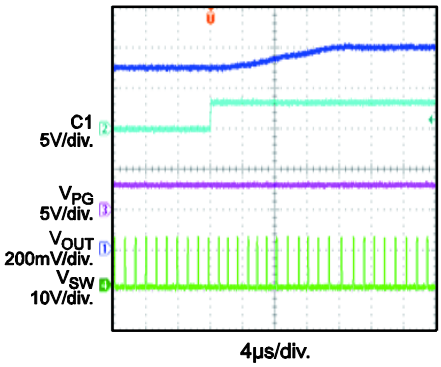
Power Good through EN Start-Up
I_{OUT} = 3A



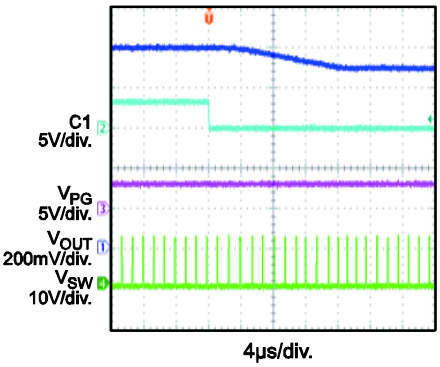
Power Good through EN Shutdown
I_{OUT} = 3A



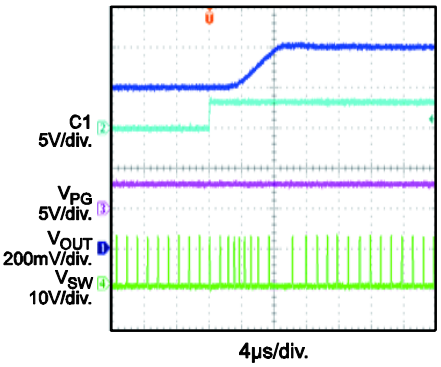
VID Transient
I_{OUT}=1A, C0=1, C1=0 to 1,
R_{MODE}=Float (VCCPRIMCORE)
V_{OUT}=0.9V-1V



VID Transient
I_{OUT}=1A, C0=1, C1=1 to 0,
R_{MODE}=Float (VCCPRIMCORE)
V_{OUT}=1V-0.9V



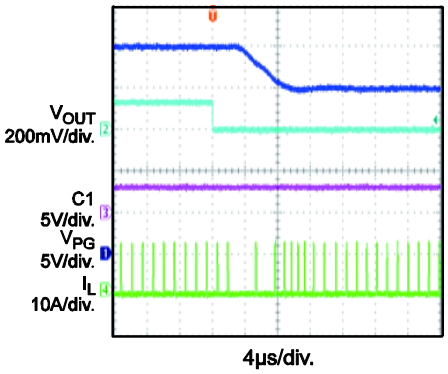
VID Transient
I_{OUT}=1A, C0=0, C1=0 to 1,
R_{MODE}=100k (EOPIO)
V_{OUT}=0.8V-1V



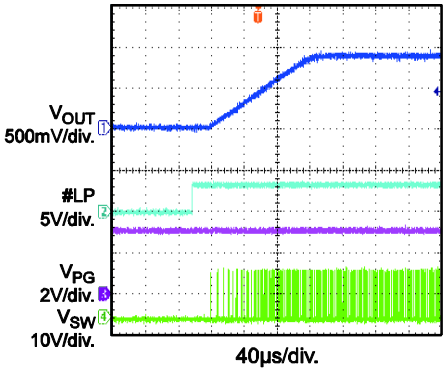
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 1.0µH/10mΩ, R_{mode} = 100kΩ, LP# = C1 = 1, C0 = 0, R_{bst} = 0, T_J = +25°C, C_{OUT} = 22µF*3 unless otherwise noted.

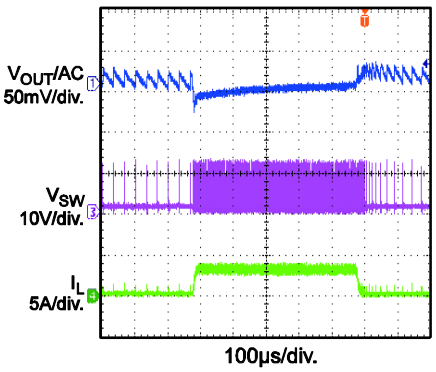
VID Transient
I_{OUT}=1A, C0=0, C1=1 to 0,
R_{MODE}=100k (EOPIO)
V_{OUT}=1V-0.8V



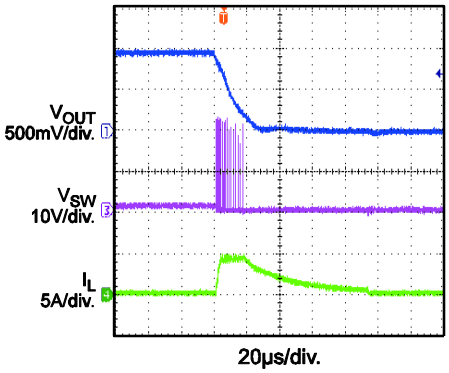
LP# Transient
I_{OUT}=3A, C1=1, C0=1,
LP#=0-1, R_{MODE}=0 (VCCIO)
V_{OUT}=0V-1V



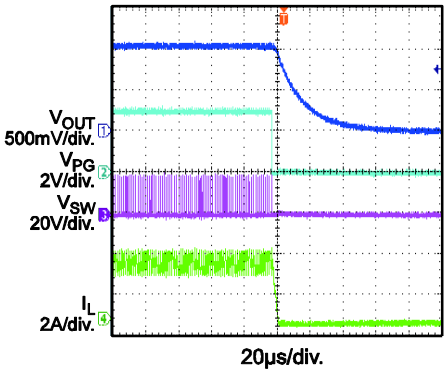
Load Transient
V_{IN}=12V, L=1.0µH, C_{OUT}=66µF,
I_{OUT}=0A-3A @1.6A/µs



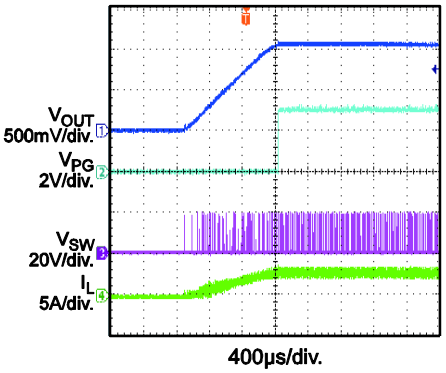
Short-Circuit Protection
V_{IN}=22V



Thermal Shutdown
V_{IN}=19V, I_{OUT}=3A



Thermal Recovery
V_{IN}=19V, I_{OUT}=3A



FUNCTIONAL BLOCK DIAGRAM

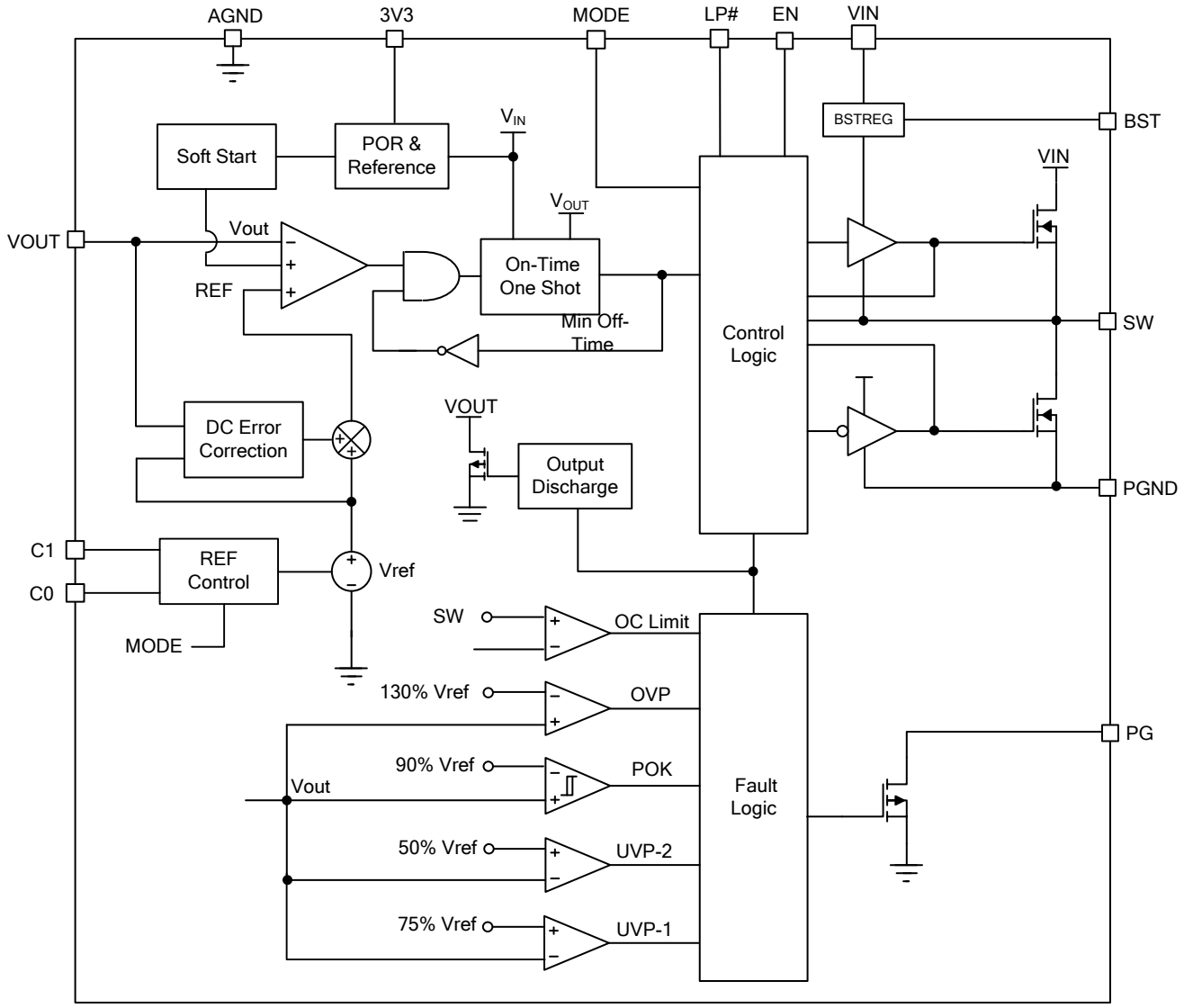


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The NB682 is a fully integrated, synchronous, rectified, step-down, switch-mode converter especially designed for IMVP8 applications—VCCIO, PRIMCORE, V1.0A, EDRAM, and EOPIO, as well as other POLs (1.8V/2.5V/3.3V). Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET turns off. The HS-FET turns on again once V_{FB} drops below V_{REF}. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize the conduction loss. There will be a dead short between the input and GND if both the HS-FET and the LS-FET are turned on at the same time (shoot-through). In order to avoid shoot-through, a dead-time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

Internal compensation is applied for COT control to enable more efficient, stable operation. Even when ceramic capacitors are used as output capacitors, the internal compensation improves the jitter performance without affecting the line or load regulation.

CCM Operation

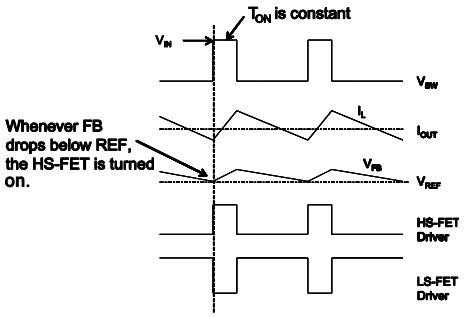


Figure 2: CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the next period.

In CCM operation, the switching frequency is fairly constant (PWM mode).

DCM Operation

The inductor current decreases when the load decreases. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on timer. See Equation (1). When the HS-FET is turned off, the LS-FET turns on until the inductor current reaches zero. In DCM operation, V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver enters tri-state (high Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. This causes the output capacitors to discharge slowly to GND through the LS-FET. As a result, the efficiency during a light-load condition is improved greatly. During a light-load condition, the HS-FET is not turned on as frequently as it is during a heavy-load condition (skip mode).

During a light-load or no-load condition, the output drops very slowly, and the NB682 reduces the switching frequency gradually, achieving high efficiency at light load.

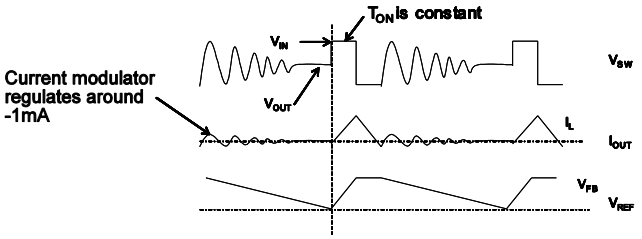


Figure 3: Light-Load Operation

As the output current increases from the light-load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned on more frequently. This causes the switching frequency to increase accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined using Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. After the output current exceeds the critical level, the switching frequency stays fairly constant over the output current range.

DC Auto-Tune Loop

NB682 applies a DC auto-tune loop to balance the DC error between V_{FB} and V_{REF}. The DC auto-tune loop adjusts the comparator input REF to make V_{FB} always follow V_{REF}; this loop is very slow, so it improves the load and line regulation without affecting transient performance. The relationship between V_{FB}, V_{REF}, and REF is shown in Figure 4.

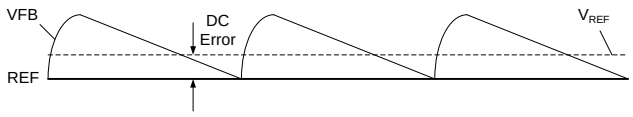


Figure 4: DC Auto-Tune Loop Operation

VCCIO/PRIMCORE/EDRAM/EOPIO/V1.0A MODE Selection

NB682 combines mode selection to support different rails in IMVP8 applications, including VCCIO, PRIMCORE, EDRAM, EOPIO, and V1.0A. These rails have a different VID, as well as a different voltage, in LPM, VID slew rate, and other features. By selecting a different resistor from MODE to GND, the NB682 can be applied in different rails with the proper features. Table 1 shows the resistor setting on MODE to enter different rails.

Table 1: Mode Selection for Different Rails

MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float (or >230K)
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

Low-Power Mode

To reduce the power loss at light load, the NB682 enters low-power mode. Once LP# is set to low, the NB682 decays to the LPM target value. With the assertion of LP# (when VR enters LPM), the NB682 behaves in the following manner:

- PG remains high for power good logic.
- VR stops switching (except the Primcore Mode).
- The output decays into the load (discharge circuitry is off) and decays to the LPM target.

Once LP# is pulled high, the NB682 exits LPM by ramping up V_{OUT} (with the appropriate delay and slew rate) to make sure the output is ready in time (e.g. 240µs), including the delay time (see Figure 5).

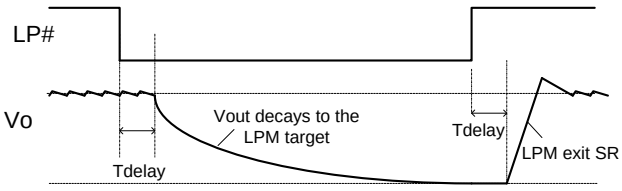


Figure 5: LPM Voltage Transition and Timing

The LPM target value, slew rate, and PG state for different rails are listed in Table 2.

Table 2: Intel LPM Specification for Each Rail

	PRIMCORE	VCCIO	EDRAM/ EOPIO	OTHER
LPM Target (V)	0.7	0	0	0
LPM Enter	Decay	Decay	Decay	Decay
LPM Exit Timer (µs)	45	240	240	240
PG during LPM	High	High	High	High

Control Bit Definitions (LP#, VID)

The control bit definitions, including LP# and VIDx for different rails, are shown in Table 3. It should be noted that C1, C0, and LP# are NOT allowed to change on-the-fly when the part is working in Other Modes.

Table 3 : Control Bit Logic

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM _CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others **Fixed design only** **Not allowed for changing on-the-fly**	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

Configuring EN Control

EN is used to enable or disable the whole chip. Pull EN high to turn on the regulator; pull EN low to turn off the regulator. It is recommended that EN rises from 0V to above 2.3V in less than 1ms. Note that there is an internal 800KΩ pull-down resistor on EN.

Also, EN works together with PG and the LP# signal to control the output (see Table 4).

Table 4 : EN/LP# Control

EN	LP#	Output	PG
0	0	0V, Off	Low
0	1	0V, Off	Low
1	0	Normal turn on and fall to LP# target value after PG+1ms	Active when the output reaches nominal voltage Keep high when LP# = 0
1	1	High	Stays active after SS

Soft Start (SS)

The NB682 employs a soft-start (SS) mechanism to ensure a smooth output during power-up. When EN becomes high, the internal reference voltage ramps up gradually; this causes the output voltage to ramp up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and the part enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the internal FB node.

Power Good (PG)

The NB682 has power good (PG) output used to indicate whether the output voltage of the buck regulator is ready. PG is an open drain of the MOSFET. PG should be connected to 3V3 (or another voltage source) through a resistor (e.g. 100k). After the input voltage is applied, the MOSFET is turned on so that PG is pulled to GND before SS is ready. After the FB voltage reaches 95% of V_{REF}, PG is pulled high in less than 10μs. When the FB voltage drops to 90% of V_{REF} (or rises higher than 115% of V_{REF}), PG is pulled low.

Note that when LP# goes low, PG stays high for the power good logic.

Start-Up and Shutdown Sequence

Figure 6 shows the start-up and shutdown sequence, including LP# and PG. During start-up, PG goes high immediately when V_{OUT} reaches its normal range. LP# mode is blanked until PG+1ms. This means the NB682 is NOT able to enter LP# mode during the start-up period+1ms. V_{OUT} decays to the target LPM

setting when LP# pulls low. V_{OUT} is able to ramp up to the normal value in the Intel required timing. PG pulls low immediately after EN becomes low.

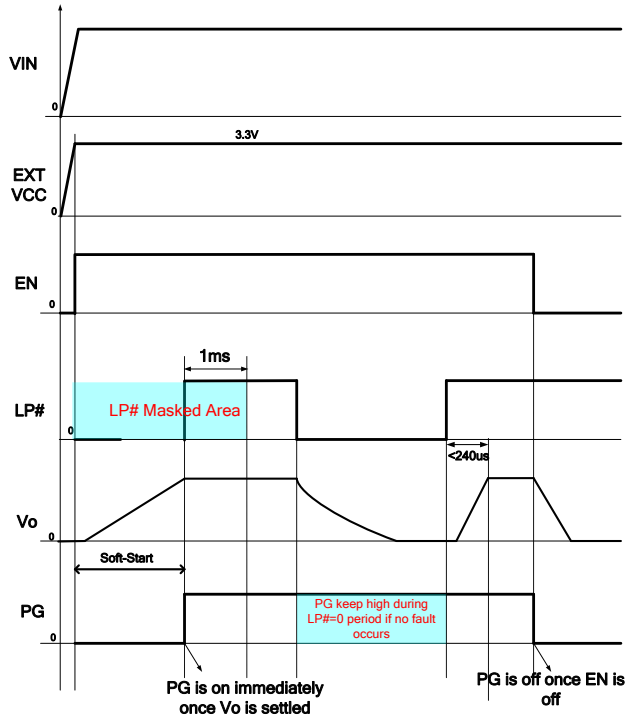


Figure 6: Power Sequence and EN/PG Logic

Ultra-Sonic Mode

Ultra-sonic mode (USM) is designed to keep the switching frequency above an audible frequency area during light-load or no-load conditions. Once the part detects that both the HS-FET and the LS-FET are off (for about 32µs), it will force PWM to its initial $T_{ON,}$ so the switching frequency will be out of audio range. To avoid V_{OUT} becoming too high, it will reduce T_{ON} to control V_{OUT}. If the part's FB is still too high after reducing T_{ON} to its minimum value, the output discharge function will be activated (keeping V_{OUT} within a reasonable range). USM is selected by the voltage threshold on EN (see Table 5). To enter USM, set EN by two resistor dividers (e.g. two 100kΩ, resistor dividers from 3.3V logic to get 1.65V).

Table 5: USM Selection

Mode	Voltage on EN
USM	1.3V < EN < 1.7V
Normal Operation	2.3V < EN < 3.5V

Over-Current Protection (OCP)

NB682 has cycle-by-cycle over-current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the Rds(on) of the LS-FET as a current-sensing element. If the magnitude of the current is above the current-limit threshold, the PWM is NOT allowed to initiate a new cycle, even if FB is lower than REF. Figure 7 shows the detailed operation of the valley current limit.

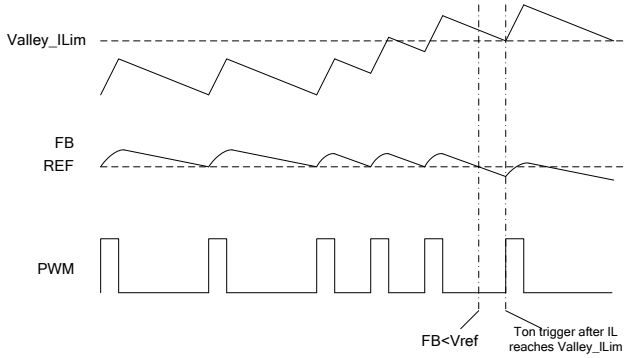


Figure 7: Valley Current Limit (OCL) Operation

Since the comparison is done during the LS on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (Ioc) can be calculated with Equation (2):

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

The OCL itself only limits the inductor current and does NOT latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up crossing the under-voltage protection (UVP) threshold and latch off. Fault latching can be re-set by EN going low, the power-cycling of VIN, or VCC.

Over/Under-Voltage Protection (OVP/UVP)

NB682 monitors the output voltage to detect over and under voltage. When the feedback voltage becomes higher than 130% of the reference voltage, the OVP comparator output goes high, and the circuit latches (as the HS-FET driver turns off, and the LS-FET driver turns on), acting as a -2A current source.

To protect the part from damage, there is an absolute 3.9V OVP on VOUT. Once V_{OUT} reaches this value, it latches off. The LS-FET will act the same at 130% OVP. This OVP is active even in LP# mode.

When the feedback voltage becomes lower than 75% of the V_{REF}, the UVP-1 comparator output goes high. The part latches if the FB voltage remains in this condition for about 64µs (which latches the HS-FET off and the LS-FET on); the LS-FET remains on until the inductor current goes to zero. During this period, the valley current limit controls the inductor current. When the feedback voltage drops below 60% of V_{REF}, the UVP-2 comparator output goes high, and the part latches off directly. After the comparator and logic delay, the HS-FET latches off and the LS-FET latches on. The LS-FET remains on until the inductor current goes to zero. Also, fault latching can be re-set by EN going low, the power-cycling of VIN, or VCC.

UVLO Protection

The NB682 has two under-voltage lockout protections (UVLO): a 3.0V VCC UVLO and a 4.2V VIN UVLO. The part starts up only when both the VCC and VIN exceed their own UVLO. The device shuts down when either the VCC voltage is lower than the UVLO falling threshold voltage (2.8V, typically), or VIN is lower than the 3.9V VIN falling threshold. Both UVLO protections are non-latch off.

Thermal Shutdown (TSD)

Thermal shutdown is employed in the NB682. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (145ºC, typically), the converter shuts off. This is a non-latch protection. There is about a 25ºC hysteresis. Once the junction temperature drops to about 120ºC, it initiates a new SS.

Output Discharge

NB682 discharges the output when EN is low, or the controller is turned off by the protection functions (UVP, OVP, UVLO, and thermal shutdown). The part discharges outputs using an internal 3Ω MOSFET.

Remote Sense

For NB682 where the remote sense is required, AGND acts as a remote sen-, which is connected to the remote ground of the output caps. VOUT acts as a remote sen+. A VCC capacitor connected between 3V3 and AGND is still required and must be placed close to the IC. Figure 9 shows a SCH with a remote sense connection. For additional remote sense details, refer to AN086.

APPLICATION INFORMATION

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore it requires a capacitor to supply the AC current while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple-current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (3) and Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specifications. The input voltage ripple can be estimated using Equation (5) and Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (6)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (7)$$

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The maximum output capacitor limitation should be considered in the design application for a small soft-start time period. If the output capacitor value is too high, the output voltage will NOT reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (10):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (10)$$

Where, I_{LIM_AVG} is the average start-up current during a soft-start period. It can be equivalent to the current limit value. T_{ss} is the soft-start time.

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will lead to a lower output ripple voltage. However, a larger value inductor will be larger physically, have a higher series resistance, and/or a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 50% of the maximum output current; keep the peak inductor current below the maximum switch current limit. The inductance value can be calculated with Equation (11):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

Where, ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current (including a short current). Choosing Isat > 4A for the NB682 is recommended.

PCB Layout Guidelines

Efficient PCB layout is critical for optimum performance of the IC. For additional information, refer to AN087. For best results, refer to Figure 8 and follow the guidelines below:

1. Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces. **The PGND trace should be the 1st priority.**
2. Place the input capacitors as close to IN and GND as possible on the same layer as the IC.
3. 3. Place the decoupling capacitor as close to VCC and GND as possible. Keep the switching node (SW) short and away from the feedback network.
4. Keep the BST voltage path as short as possible (with a >25mil trace).
5. Connect the IN and GND pads with a large copper trace to achieve better thermal performance. Add several vias (with 10mil_drill/18mil_copper_width) close to the IN and GND pads to help thermal dissipation.
6. A 4-layer layout is recommended to achieve better thermal performance.
7. It is recommend to use >20mil trace for the vout sense for output discharge.

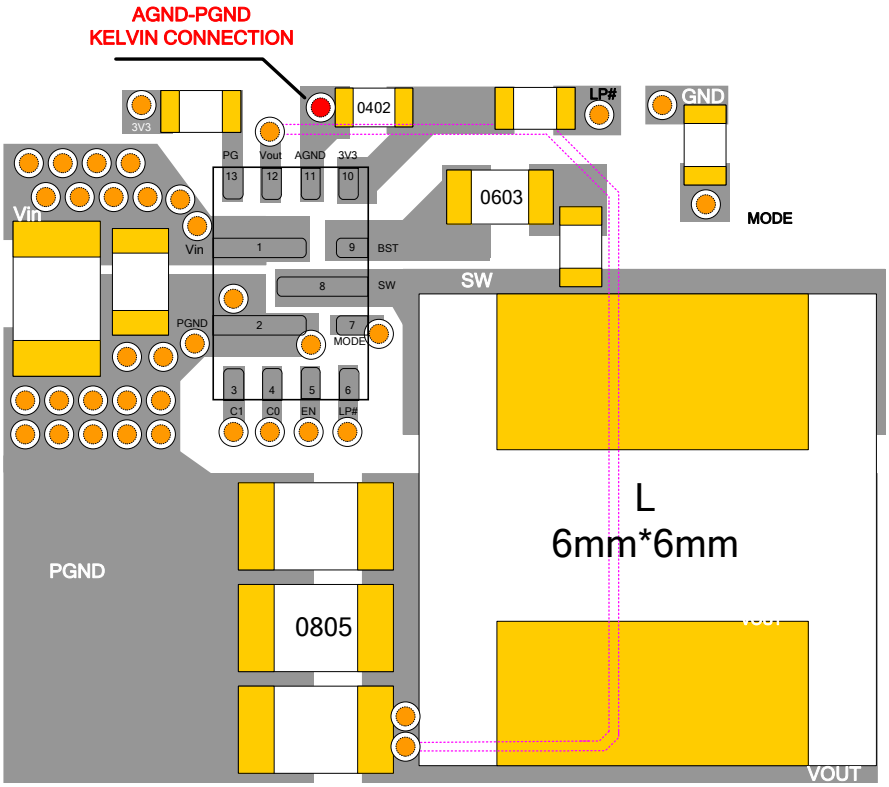


Figure 8: Recommended PCB Layout

Design Example

Table 6 shows design examples when ceramic capacitors are applied.

There is a resistor from an external 3.3V to 3V3 acting as the ripple noise filter of the 3.3V power supply. A resistor value from 0-5.1Ω (depending on the noise level) is recommended. A 0402 size resistor is sufficient. If the 3.3V voltage rises up with a SS > 100µs, a larger size resistor (e.g. 0603/0805) is needed.

Table 6: Design Example for Different Rails

V_{OUT} (V)	R_{Mode} (Ω)	Cout (F)	L (µH)
VCCIO	0	22µx3	0.68~1
PRIMCORE	Float	22µx3	0.68~1
EDRAM/ EOPIO/ V1.0A	100K	22µx3	0.68~1
Others-1.8V/2.5	150K	22µx4	1.0-1.5
Others-3.3V	150K	22µx4[6]	1.2-1.5

NOTE[6]:

If Vin is lower than 7V, apply a150µF POSCAP capacitor, considering the transient.

TYPICAL APPLICATION FOR DIFFERENT RAILS

VCCIO

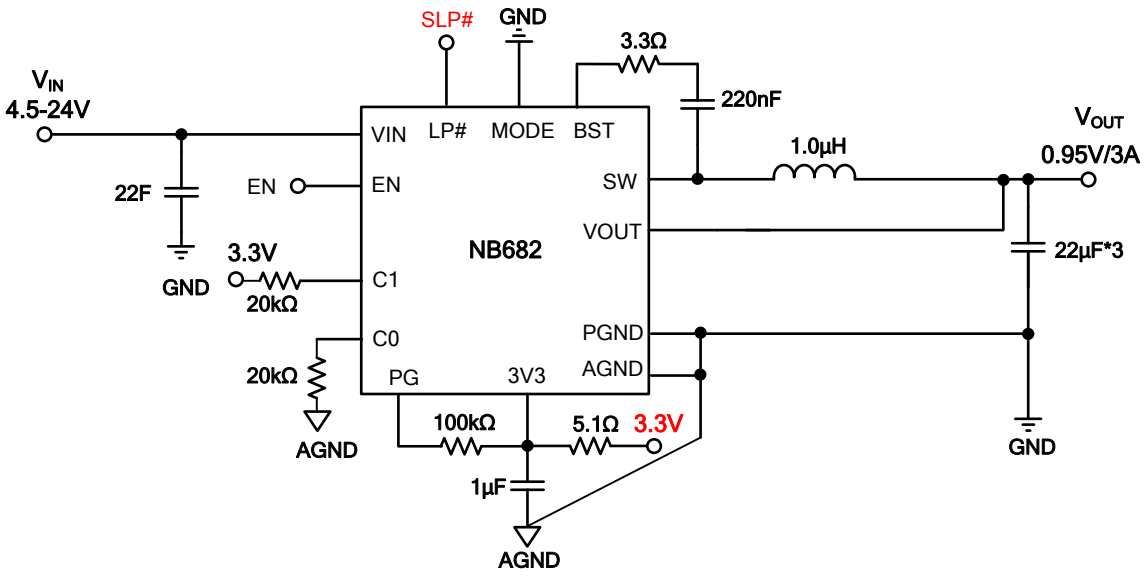


Figure 8.1: Typical Application Schematic for VCCIO, Default 0.95V (C1 and C0 can be Pulled High/Floating or Low Directly without a Resistor if V_{OUT} is Fixed)

PRIMCORE

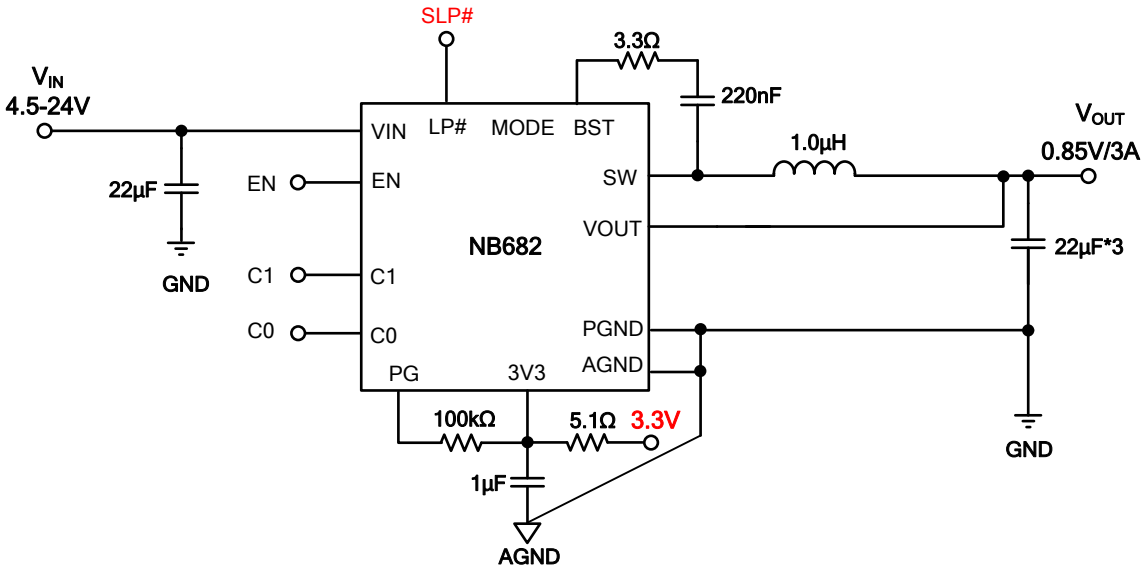


Figure 8.2: Typical Application Schematic for PRIMCORE, V_{OUT} Adjusted by VID

TYPICAL APPLICATION FOR DIFFERENT RAILS

EDRAM&V1.0A

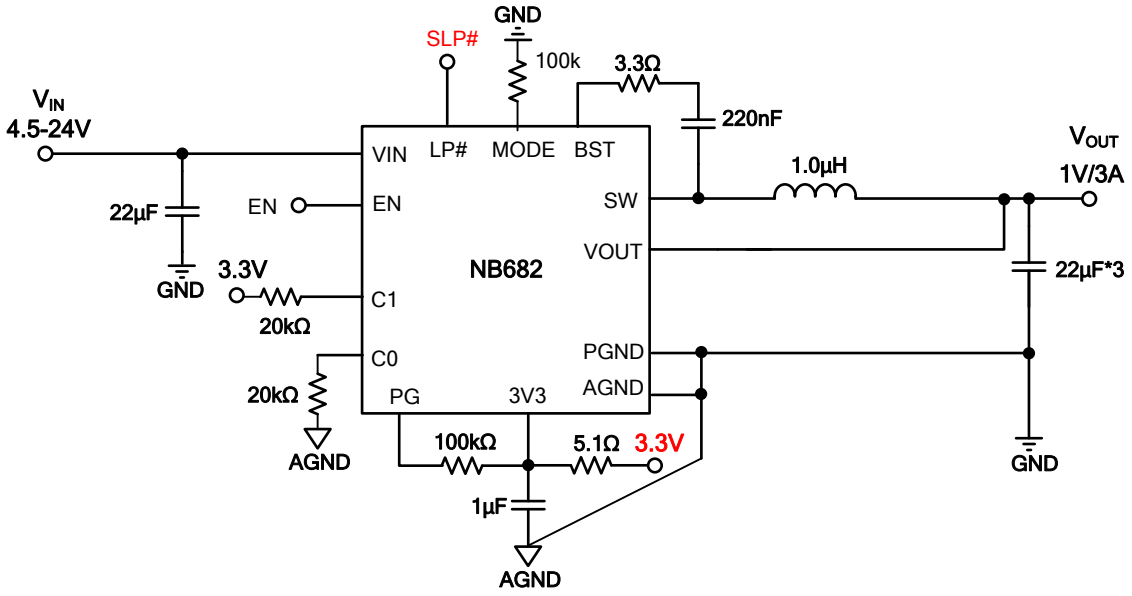


Figure 8.3: Typical Application Schematic for EDRAM and V1.0A, Default 1V, (C1 and C0 can be Pulled High/Floating or Low Directly without a Resistor if V_{OUT} is Fixed)

EOPIO

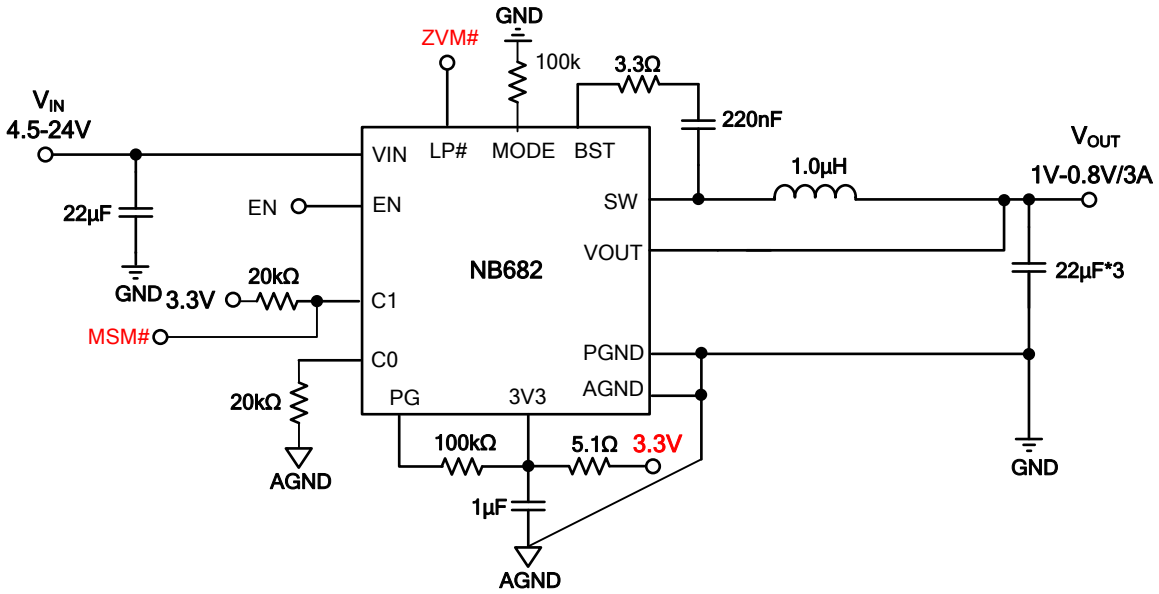


Figure 8.4: Typical Application Schematic for EOPIO

Others (1.8V)

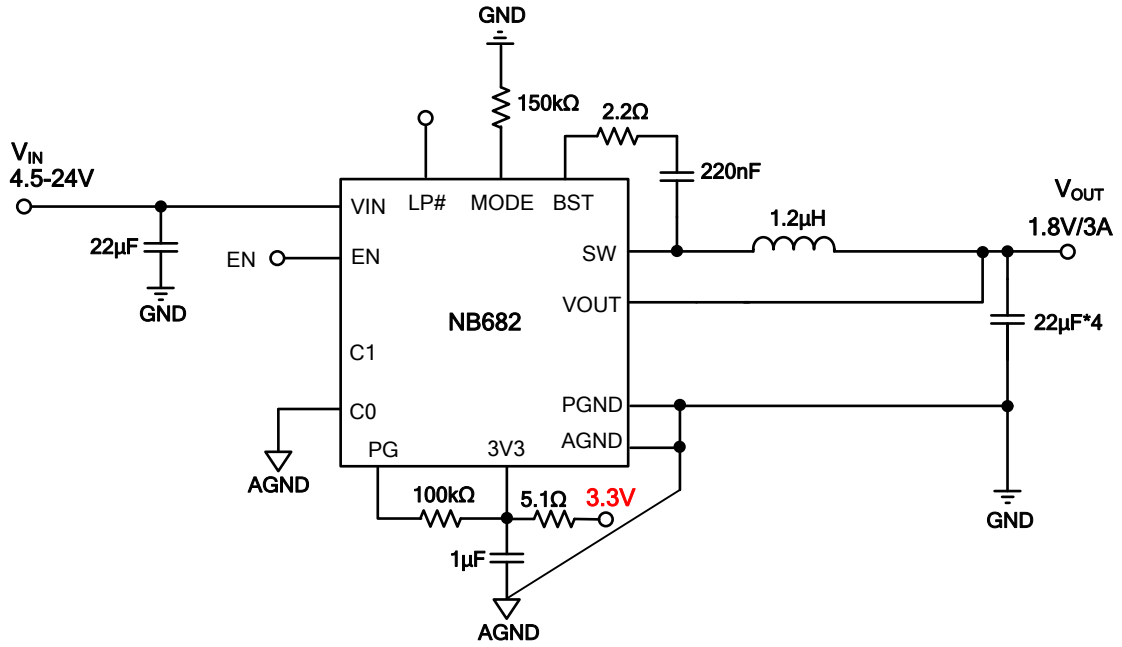


Figure 8.5: Typical Application Schematic for Others Mode (1.8V)

Others (2.5V)

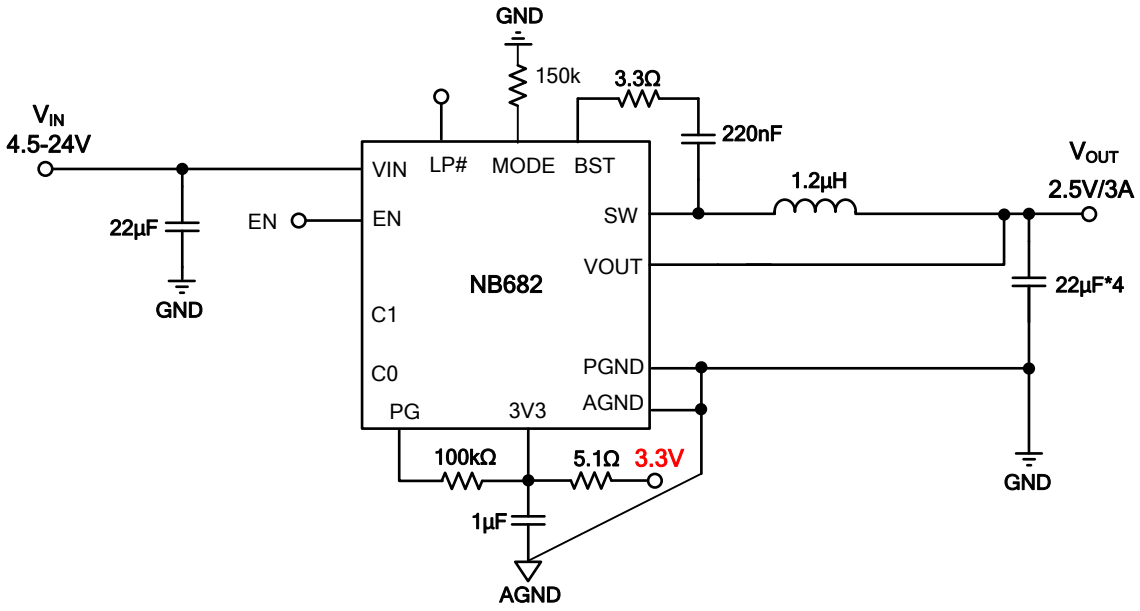


Figure 8.6: Typical Application Schematic for Others Mode (2.5V)

TYPICAL APPLICATION WITH REMOTE SENSE

Refer to AN086 for additional details on the remote sense application.

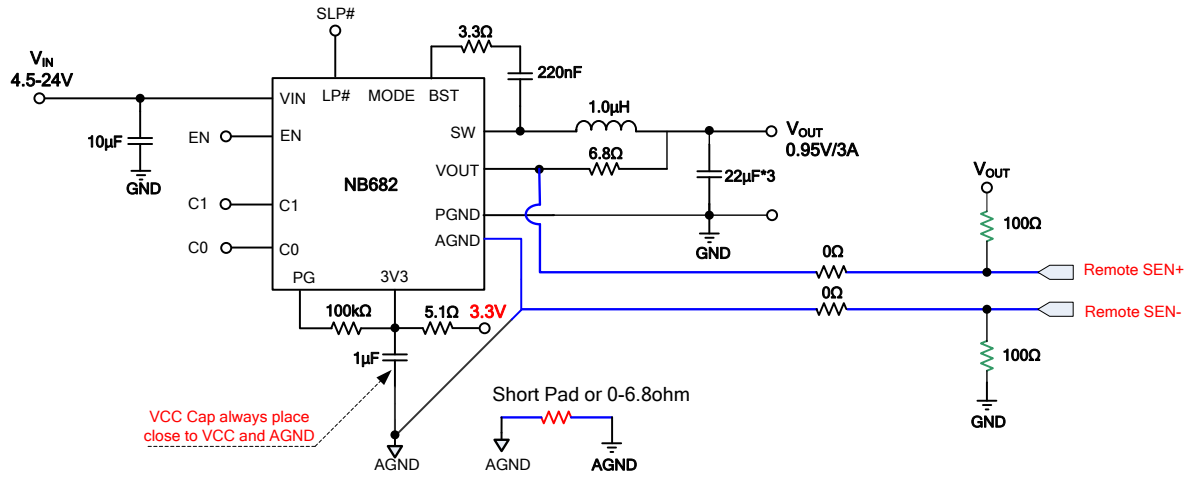


Figure 9: Typical Application Schematic for NB682 Remote Sense Application

NOTE1: Ultra-sonic mode is **NOT** effective if applied in this SCH, make sure EN rising finishes in 1ms.

TYPICAL APPLICATION WITH VOUT FROM VID TABLE

The two red resistors on VOUT act as feedback resistors to adjust VOUT to the proper value. It is recommended to choose the closest VID value (which is lower than the target VOUT) as V_{REF} if there are no other limitations. Figure 10 shows the typical SCH with the V_{OUT} setting at 1.1V.

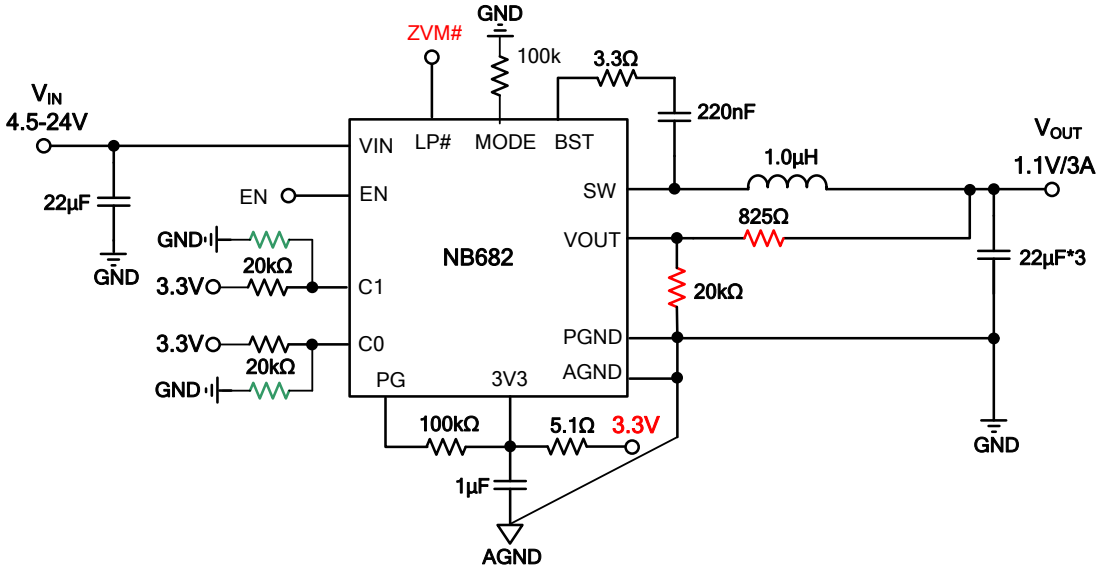


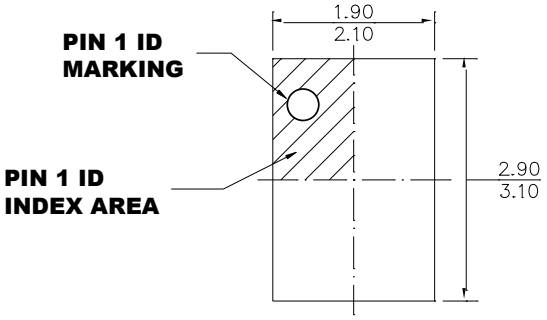
Figure 10: Typical Application Schematic for NB682 with V_{OUT} of the VID Table

NOTE 2: Ultra-sonic mode is **NOT** effective if applied in this SCH, make sure EN rising finishes in 1ms.

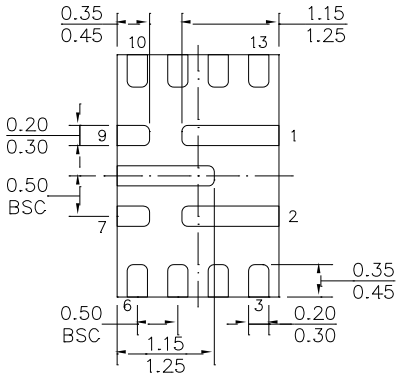
NOTE 3: It is **NOT** recommended to set V_{OUT} over 50% of the target V_{REF}.

PACKAGE INFORMATION

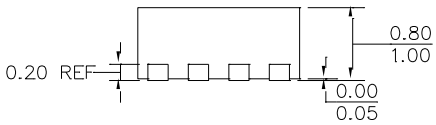
QFN-13 (2mm x 3mm)



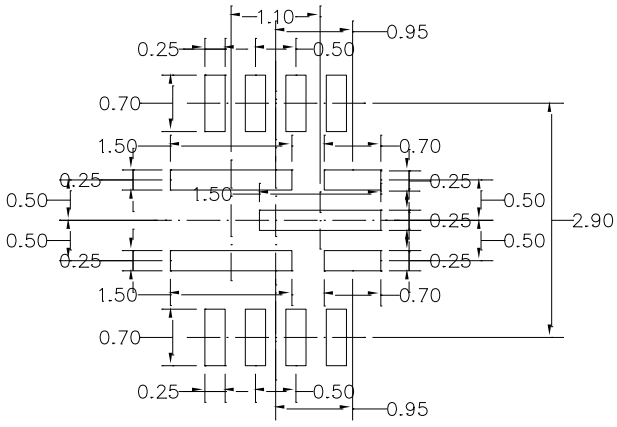
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.