EV3363-J-00A

Single String, 1.8V Vin-min, 36V Vout Boost LED Driver-Evaluation Board

DESCRIPTION

MP3363 is a fixed frequency converter ideal for low-to-high current Boost applications. The low 0.2V feedback voltage offers higher efficiency in white LED driver applications.

MP3363 regulates the output voltage up to 36V with efficiency as high as 95%. Current-mode regulation and external compensation components allow the MP3363 control loop to be optimized over a wide variety of input voltage.

MP3363 supports analog dimming and PWM dimming on same pin. The <2kHz input dimming frequency is for PWM dimming, >5kHz is for analog dimming.

Soft-start, cycle-by-cycle current limiting, and input under voltage lockout prevent overstressing or damage to sensitive external circuitry at startup and over load current conditions.

The MP3363 is available in a TSOT23-8 package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	1.8 – 36	V
Output Voltage	VLED	<40	V
LED String		1	string
LED Current	I_{LED}	40	mA

FEATURES

- Input Range of 1.8V to 36V
- 1A Peak Current Limit
- 0.5μA Shutdown Current
- Low 200mV Feedback Voltage
- Programmable Fsw 200kHz-2.2MHz
- Internal 100mΩ 40V Power Switch
- High Efficiency
- Analog and PWM Dimming
- Under Voltage Lockout Protection
- Open/Short LED Protection
- Short FB Protection
- Soft-Start Operation
- Thermal Shutdown
- TSOT23-8 Package

APPLICATIONS

- 2 AA Power Backlighting
- LCD Backlighting
- General Lighting

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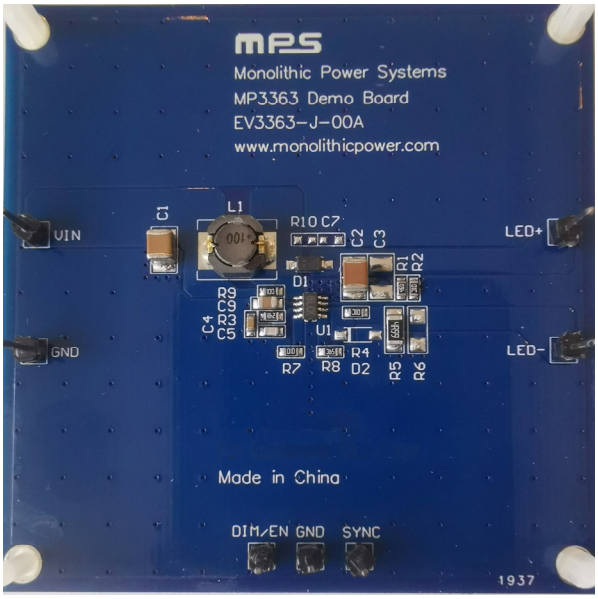
EVQ3362-J-00A EVALUATION BOARD



(L x W x H) 6.35cm x 6.35cm x 1.0cm

Board Number	MPS IC Number
EV3363-J-00A	MP3363GJ

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QUICK START GUIDE

1. Preset DC Power Supply output to 1.8V to 36V and turn off Power Supply.
2. Connect the positive terminal of Power Supply output to the VIN pin and the negative terminal to the GND pin.
3. Connect the LED load between “LED+” (anode of LED string) and “LED-“(cathode of LED string).
4. Turn on Power Supply.
5. Apply the Enable voltage to the EN/DIM pin and drive Enable high to turn on the chip. Apply the PWM signal to then EN/DIM pin for realizing the Dimming function(Fpwm>5kHz for Analog dimming, Fpwm<2kHz for PWM dimming).

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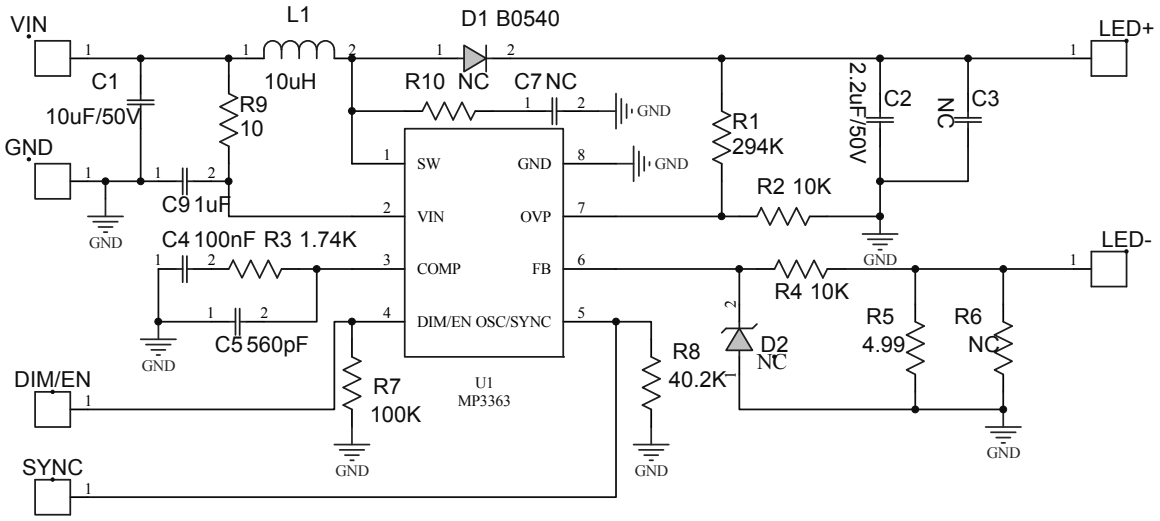
EVALUATION BOARD SCHEMATIC



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EVQ3362-J-00A BILL OF MATERIALS

RefDes	Value	Description	Package	Manufacturer	Manufactuer_P/N
C1	10μF	Ceramic Capacitor; 50V;X7R;1210;	1210	TDK	C3225X7R1H106M
C2	2.2μF	Ceramic Capacitor; 50V;X7R;1210;	1210	muRata	GJ8319R61H225K
C4	100nF	Ceramic Capacitor; 25V;X7R;0603;	0603	Wurth	8.85012E+11
C5	560pF	Ceramic Capacitor; 50V;X7R;0603;	0603	muRata	GRM1885C1H561JA01
C7,C3	NC				
C9	1μF	Ceramic Capacitor; 50V;X7R;0805;	0805	muRata	GRM21BR71H105KA12L
D1	B0540	40V/0.5A	SOD-123	Diodes	B0540W-7-F
D2	NC				
L1	10μH/1.14A	SUMIDA/CDRH3D16	SMD	TOKO	D63LCB-A921CY-100M=P3
R1	294k	Film Resistor;1%;	0603	Yageo	RC0603FR-07294KL
R2,R4	10k	Film Resistor;1%;	0603	Yageo	RC0603FR-0710KL
R3	1.74k	Film Resistor;1%;	0603	Yageo	RC0603FR-071K74RL
R5	4.99	Film Resistor;1%;	1206	Yageo	RC1206FR-074R99L
R6,R10	NC				
R7	100k	Film Resistor;1%;	0603	Yageo	RC0603FR-07100KL
R8	40.2k	Film Resistor;1%;	0603	Yageo	RC0603FR-0740K2L
R9	10	Film Resistor;5%;	0603	Yageo	RC0603JR-0710RL
VIN,GND, LED+,LED-, DIM/EN,SYNC		Connector			Connector: 2.54mm 排针
U1		MP3363			

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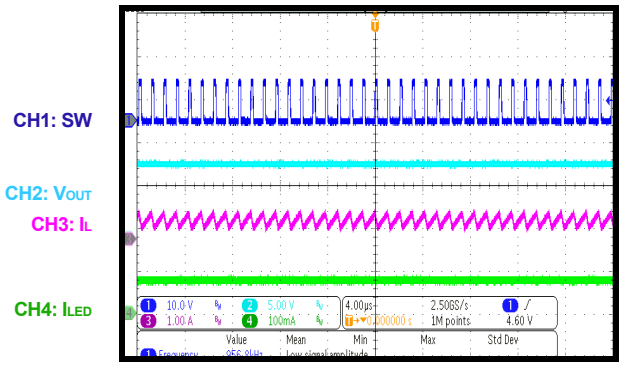
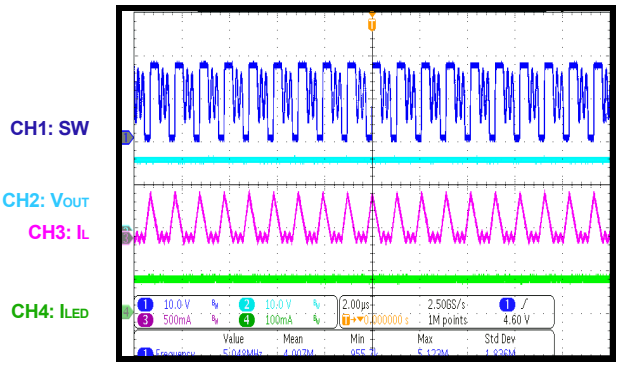
EVB TEST RESULTS

V_{IN}=10V, Load:10LEDs, I_{LED}=80mA, L=4.7uH, Ta=25°C, unless otherwise noted.

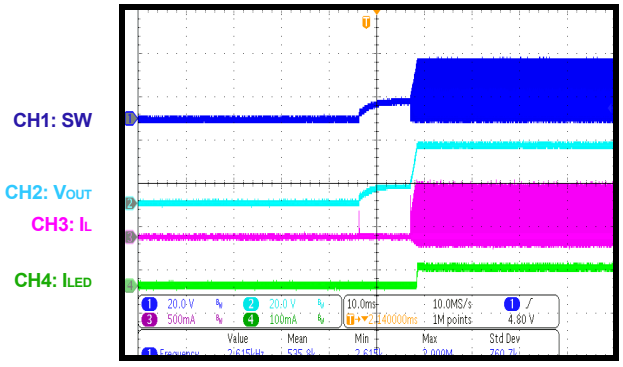
Steady State
V_{IN} = 1.8V, Load: 3LEDs



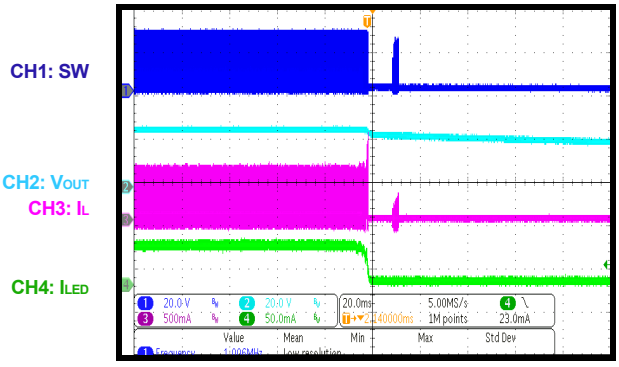
Steady State
Load: 6LEDs



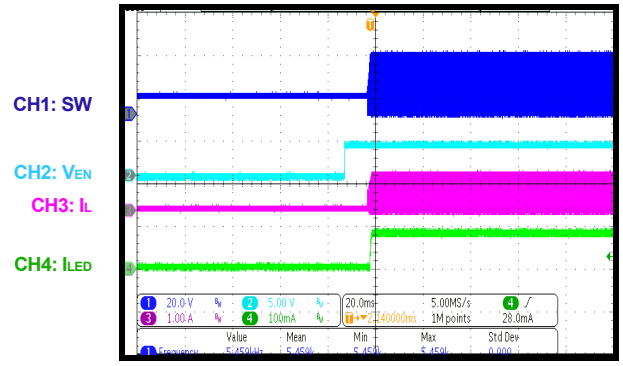
V_{IN} Power On



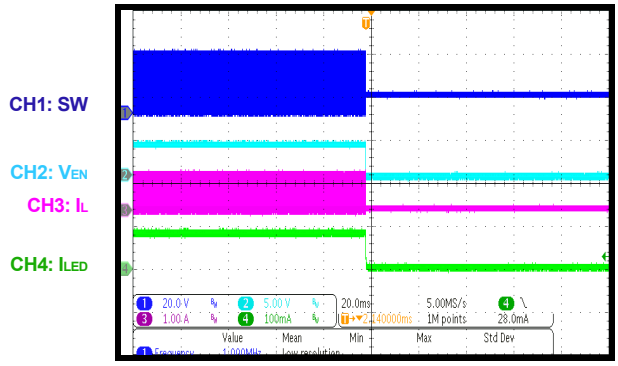
V_{IN} Power Off



V_{EN} On



V_{EN} Off



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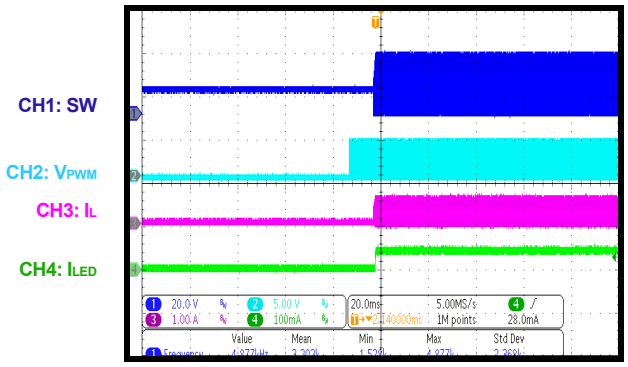
EVB TEST RESULTS *(continued)*

V_{IN}=10V, Load:10LEDs, I_{LED}=80mA, L=4.7uH, Ta=25°C, unless otherwise noted.

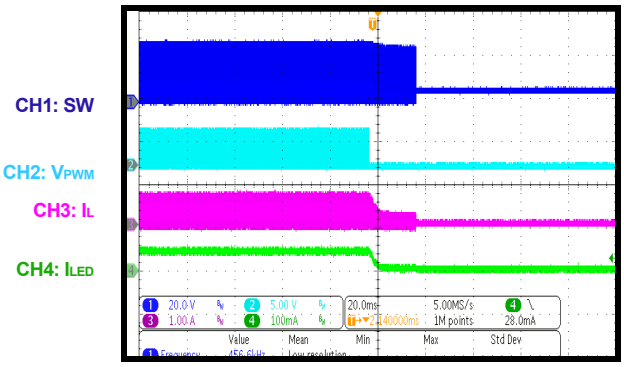
PWM Power On

F_{PWM} = 10kHz(D=0.5)



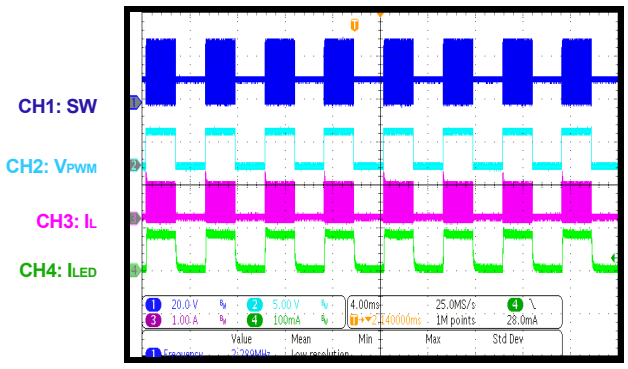
PWM Power Off

F_{PWM} = 10kHz(D=0.5)



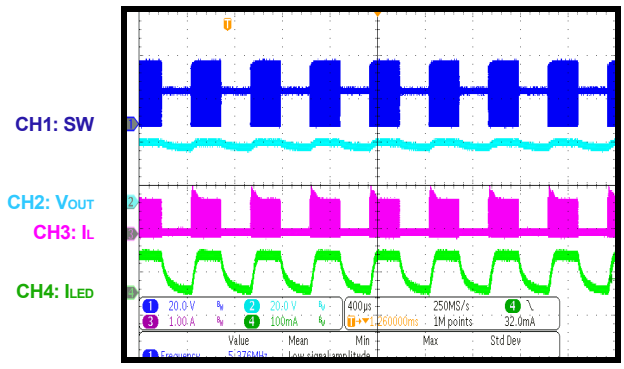
PWM Dimming

200Hz/D=0.5



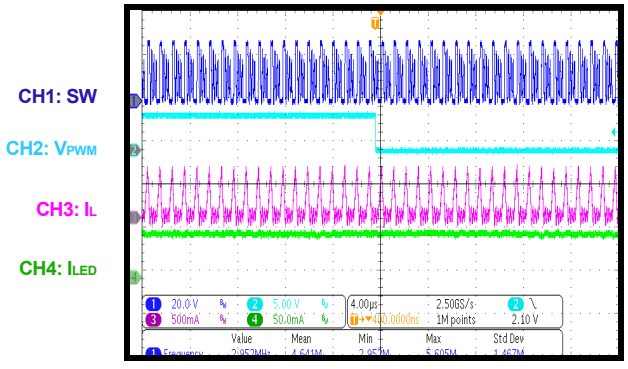
PWM Dimming

2kHz/D=0.5

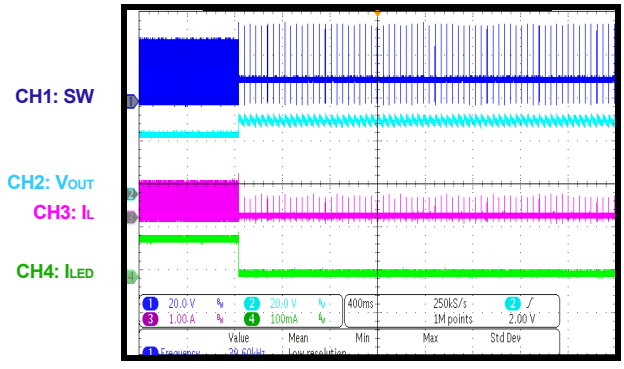


Analog Dimming

5kHz/D=0.5



OVP When Work Normal



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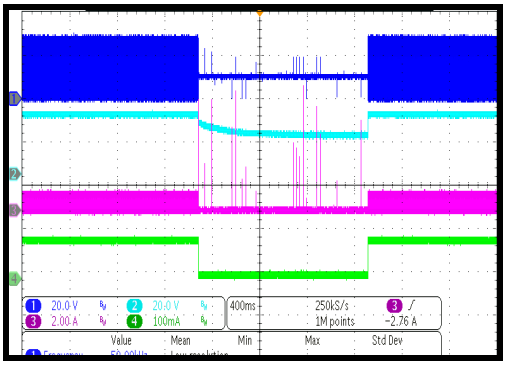
EVB TEST RESULTS *(continued)*

V_{IN}=10V, Load:10LEDs, I_{LED}=80mA, unless otherwise noted.

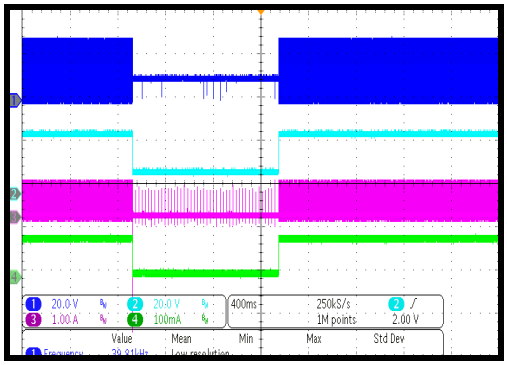
Short Inductor When Work Normal Then Recover

CH1: SW
CH2: VOUT
CH3: IL
CH4: ILED



Short Diode When Work Normal Then Recover

CH1: SW
CH2: VOUT
CH3: IL
CH4: ILED



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PRINTED CIRCUIT BOARD LAYOUT

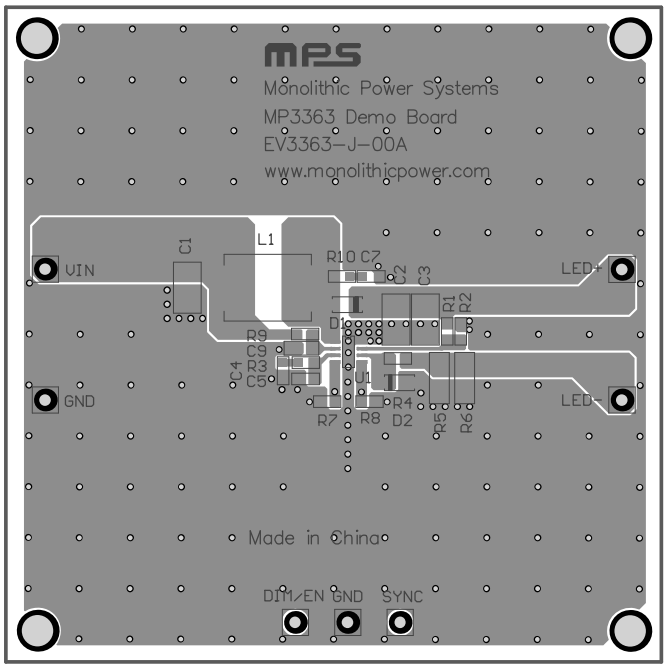

Figure 1: Top Layer

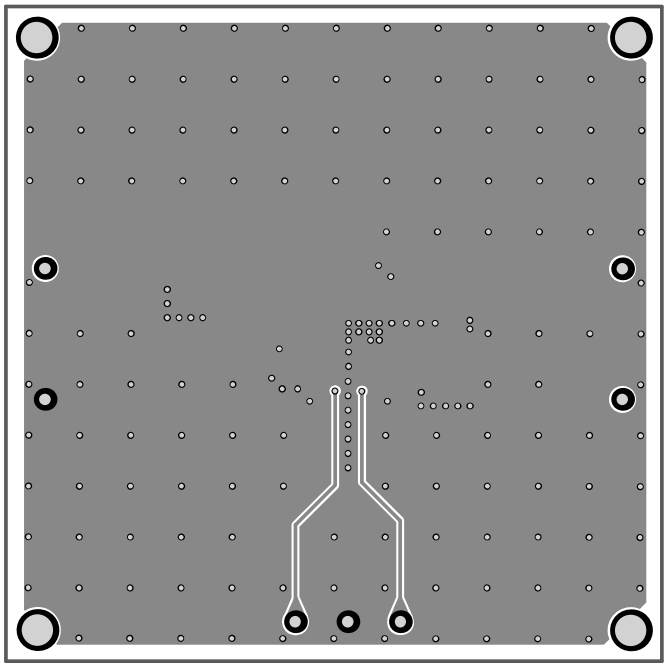

Figure 2: Bottom Layer

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