HR1001L

Enhanced LLC Controller with Adaptive Dead-Time Control

The Future of Analog IC Technology

DESCRIPTION

The HR1001L is an enhanced LLC controller that provides new, adaptive, dead-time adjustment (ADTA) and capacitive mode protection (CMP) features. The HR1001L is the OCP latch-off version of the HR1001B.

ADTA inserts a dead time between the two complimentary gate outputs automatically by keeping the outputs off while sensing the dV/dt current of the half-bridge switching node. ADTA features an easier design, lower EMI, and higher efficiency.

The HR1001L incorporates anti-capacitive mode protection, which prevents potentially destructive capacitive mode switching if the output is shorted or has a severe overload. This feature protects the MOSFET during abnormal conditions, making the converter robust.

The HR1001L has a programmable oscillator that sets both the maximum and minimum switching frequencies. It starts up at a programmed maximum switching frequency and decays until the control loop takes over to prevent excessive inrush current.

The HR1001L enters controlled burst mode at light loads to minimize the power consumption and tighten output regulation.

Full protection features include two-level over-current protection (OCP), external-latch shutdown, brown-in/brown-out, capacitive mode protection (CMP), and over-temperature protection (OTP).

FEATURES

- Two-Level Over-Current Protection (OCP): Frequency Shift and Latch-Off Mode
- Adaptive Dead-Time Adjustment (ADTA)
- Capacitive Mode Protection (CMP)
- 50% Duty Cycle, Variable Frequency Control for Resonant Half-Bridge Converter
- 600V High-Side Gate Driver with Integrated Bootstrap Diode with a High-Accuracy Oscillator of High dV/dt Immunity
- Operates up to 600kHz
- Latched to Disable Input for Easy Protection
- Remote On/Off Control and Brown-Out Protection through BO
- Programmable Burst Mode Operation at Light Load
- Non-Linear Soft Start for Monotonic Output Voltage Rise
- Available in a SOIC-16 Package

APPLICATIONS

- LCD and PDP TVs
- Desktop PCs and Servers
- Telecom SMPS
- AC/DC Adapter, Open-Frame SMPS
- Video Game Consoles
- Electronic Lighting Ballast

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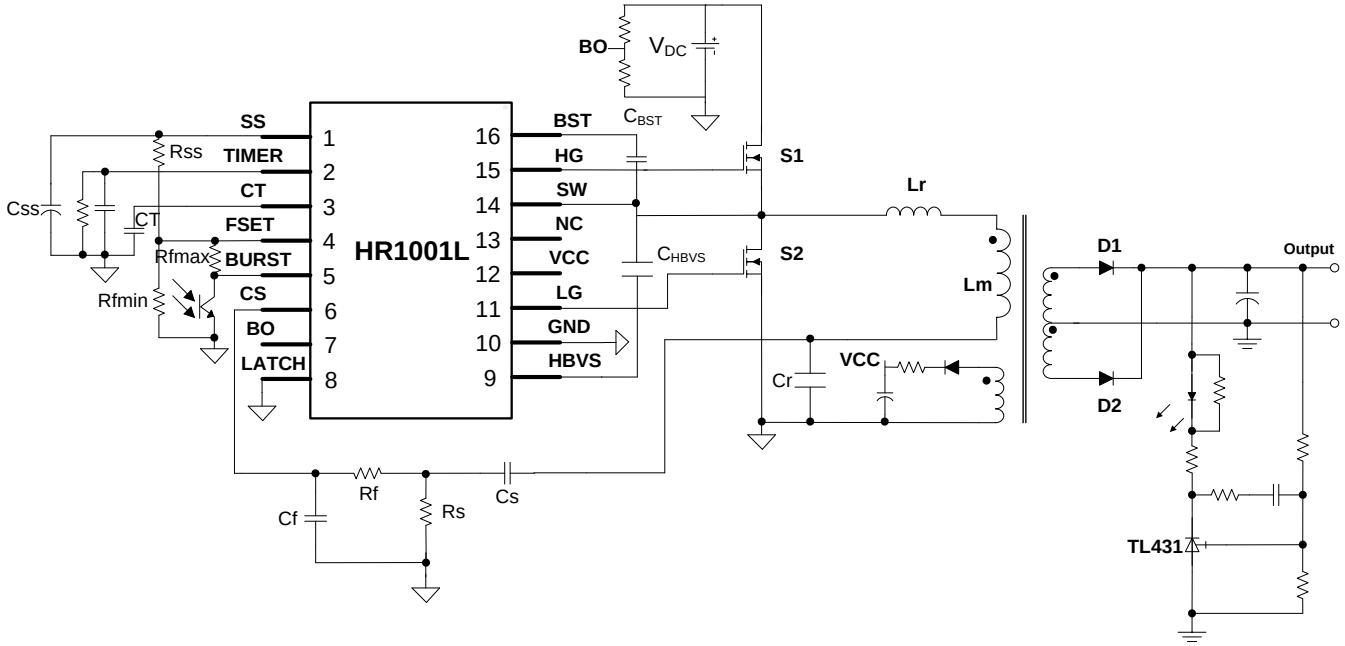
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
HR1001LGS	SOIC-16	*See Below*

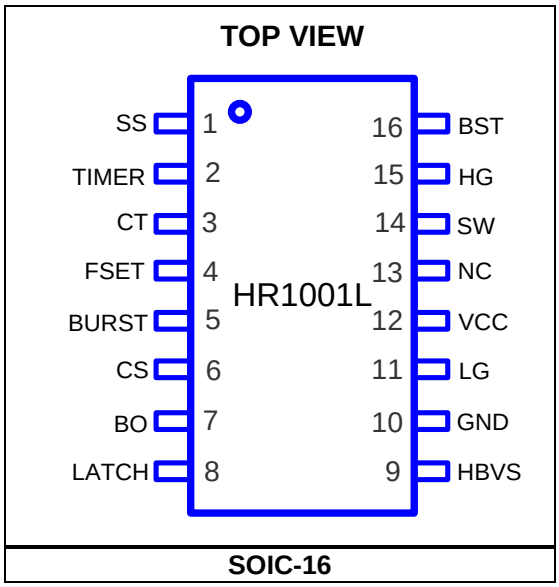
* For Tape & Reel, add suffix –Z (e.g. HR1001LGS–Z)

TOP MARKING

MPSYYWW
HR1001L
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
HR1001L: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



SOIC-16

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ABSOLUTE MAXIMUM RATINGS (1)

BST voltage.....……..... -0.3V to 618V
SW voltage ……..... ..... -3V to 600V
Max voltage slew rate of SW….. .....50V/ns
Supply voltage (VCC)…….. ..... Self-limited
Sink current of HBVS….. .....±65mA
Voltage on HBVS.....…. .....-0.3V to self-limit
Source current of FSET….....2mA
Voltage rating of LG……. .....-0.3V to V_{CC}
Voltage on CS.....…….....-3V to 6V
Other analog inputs and outputs..... -0.3V to 6V
Continuous power dissipation (T_A = +25°C)(2)
P_{IC} ……. 1.56W
Junction temperature….....150°C
Lead temperature ……....260°C
Storage temperature…….....-65°C to +150°C
ESD immunity……..BST, HG, SW passes HBM 2.5kV, other pins can pass HBM 4kV.

Recommended Operating Conditions (3)

Supply voltage (VCC)….. .....13V to 15.5V
Analog inputs and outputs.....-0.3V to 6V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

SOIC-16.....80.....35…… °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

VCC = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C~125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
IC Supply Voltage (VCC)						
VCC operating range			8.9		15.5	V
VCC high threshold, IC switch on	V_{CCH}		10.3	11	11.7	V
VCC low threshold, IC switch off	V_{CCL}		7.5	8.2	8.9	V
Hysteresis	V_{CC-hys}			2.8		V
VCC clamp voltage	$V_{CC-Clamp}$	I_{Clamp} = 1mA		16.5		V
IC Supply Current (VCC)						
Start-up current	$I_{start-up}$	Before the device turns on, VCC = VCC_H - 0.2V		250	320	μA
Quiescent current	I_Q	Device on, V_{Burst} < 1.23V, R_{FSET} =12k, F_{MIN} = 60kHz		1.2	1.5	mA
	I_{Q-f}	Device on, V_{Burst} < 1.23V, R_{FSET} = 3.57k, F_{BURST} = 200kHz		1.42	1.8	mA
Operating current	I_{CC-nor}	Device on V_{Burst} = V_{FSET}		3	5	mA
Residual consumption	I_{Fault}	VCC < 8.2V or V_{LATCH} > 1.85V or V_{CS} > 1.5V or V_{TIMER} > 3.5V or V_{BO} < 1.81V or V_{BO} > 5.5V or OTP	240	350	420	μA
High-Side Floating Gate Driver Supply (BST, SW)						
BST leakage current	I_{LK-BST}	V_{BST} = 600V, T_J = 25°C			12	μA
SW leakage current	I_{LK-SW}	V_{SW} = 582V, T_J = 25°C			12	μA
Current Sensing (CS)						
Input bias current	I_{CS}	V_{CS} = 0 to $V_{CSlatch}$			2	μA
Frequency shift threshold	V_{CS-OCR}		0.71	0.78	0.85	V
OCP threshold	V_{CS-OCP}		1.41	1.5	1.59	V
Current polarity comparator reference when HG turns off	V_{CSPR}		50	85	131	mV
Current polarity comparator reference when LG turns off	V_{CSNR}		-131	-85	-50	mV
Line Voltage Sensing (BO)						
Start-up threshold voltage	V_{BO-On}			2.30	2.4	V
Turn-off threshold voltage	V_{BO-Off}		1.72	1.81		V
Clamp level	$V_{BO-Clamp}$		5.1	5.5	5.9	V
Latch Function (LATCH)						
Input bias current (V_{LATCH} = 0 to V_{th})	I_{LATCH}				1	μA
LATCH threshold	V_{LATCH}		1.72	1.85	1.95	V

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C~125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillator						
Output duty cycle	D	T_J = 25°C	48	50	52	%
		T_J = -40~125°C	47	50	53	%
Oscillation frequency	f_{osc}	CT ≤ 150pF, R_{FSET} ≤ 2k			600	kHz
CT peak value	V_{CFp}			3.8		V
CT valley value	V_{CFv}			0.9		V
Voltage reference at FSET	V_{REF}		1.87	2	2.05	V
Dead time	DT_{MIN}	C_{HBVS} = 5pF, typically	180	235	290	ns
	DT_{MAX}			1		µs
	DT_{-float}	HBVS floating	250	350	450	ns
Timer for CMP	t_{CMP}			52		µs
Half-Bridge Voltage Sense (HBVS)						
Voltage clamp	$V_{HBVS-Clamp}$			7.6		V
Minimum voltage change rate that can be detected	dV_{min}/dt	C_{HBVS} = 5pF, typically			180	V/µs
Turn-on delay	T_d	Slope finish to turn-on delay		100		ns
Soft-Start Function (SS)						
Discharge resistance	R_d	$V_{CS} > V_{CS-OCR}$		130		Ω
Standby Function (BURST)						
Disable threshold	V_{Burst}		1.17	1.23	1.28	V
Hysteresis	$V_{Burst-hys}$			30	100	mV
Delayed Shutdown (TIMER)						
Charge current	I_{TIMER}	V_{TIMER} = 1V, V_{CS} = 0.85V, T_J = 25°C	80	130	180	µA
Threshold for forced operation at maximum frequency	$V_{TIMER-fmax}$		1.80	2	2.10	V
Shutdown threshold	$V_{TIMER-SD}$		3.2	3.5	3.7	V
Restart threshold	$V_{TIMER-R}$		0.21	0.28	0.35	V
Low-Side Gate Driver (LG, Referenced to GND)						
Peak source current(5)	$I_{sourcepk}$			0.75		A
Peak sink current(5)	I_{sinkpk}			0.87		A
Sourcing resistor	R_{source}	Isrc = 0.1A		4		Ω
Sinking resistor	R_{sink}	Isnk = 0.1A		2		Ω
Fall time	t_f			30		ns
Rise time	t_{LG-r}			30		ns
UVLO saturation		VCC = 0 to V_{CCH}, I_{sink} = 2mA			1	V

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ELECTRICAL CHARACTERISTICS *(continued)*

VCC = 13V, C_{HG} = C_{LG} = 1nF, CT = 470pF, R_{FSET} = 12kΩ, T_J = -40°C~125°C, min and max values are guaranteed by characterization, typical values are tested under 25°C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-Side Gate Driver (HG, Referenced to SW)						
Peak source current(5)	$I_{HG-source-pk}$			0.74		A
Peak sink current(5)	$I_{HG-sink-pk}$			0.87		A
Sourcing resistor	$R_{HG-source}$	Isrc = 0.01A		4		Ω
Sinking resistor	$R_{HG-sink}$	Isnk = 0.01A		2		Ω
Fall time	t_{HG-f}			30		ns
Rise time	t_{HG-r}			30		ns
Thermal Shutdown						
Thermal shutdown threshold(5)				150		°C
Thermal shutdown recovery threshold(5)				120		°C

NOTE:

5) Guaranteed by design.

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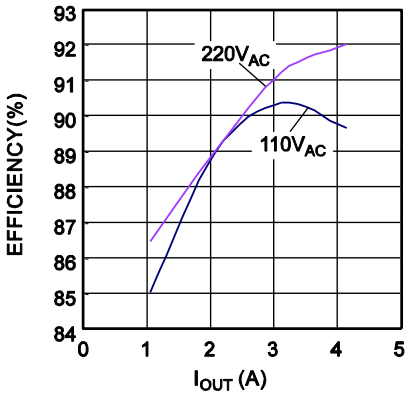
TYPICAL PERFORMANCE CHARACTERISTICS

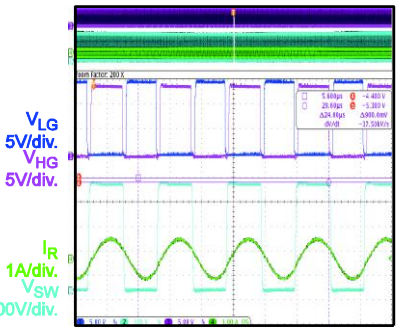
Performance waveforms are generated using the evaluation board built with the design example on page 22, V_{AC} = 120V, V_{OUT} = 24V, I_{OUT} = 4.16A, T_A = 25°C, unless otherwise noted.

Efficiency



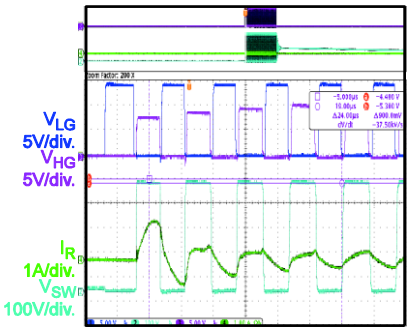
Steady State

V_{OUT}=24V, I_{OUT}=4.16A



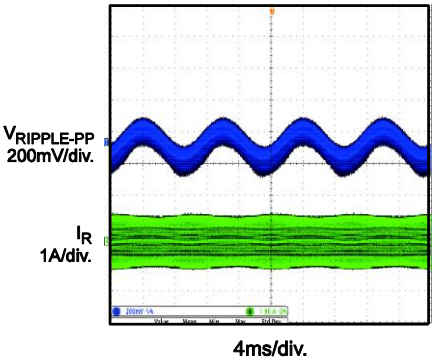
Steady State

V_{OUT}=24V, I_{OUT}=0A



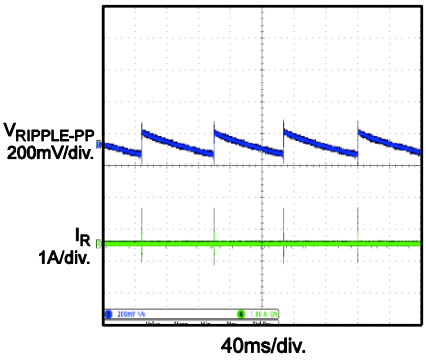
Steady State

V_{OUT}=24V, I_{OUT}=4.16A



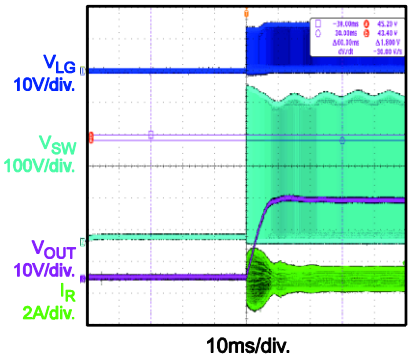
Steady State

V_{OUT}=24V, I_{OUT}=0A



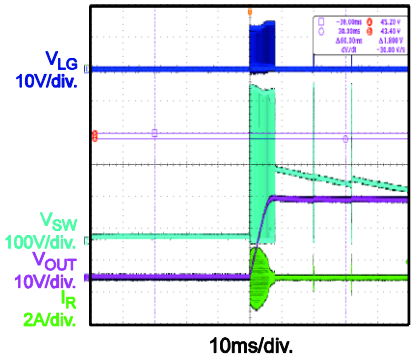
Start-Up

V_{OUT}=24V, I_{OUT}=4.16A



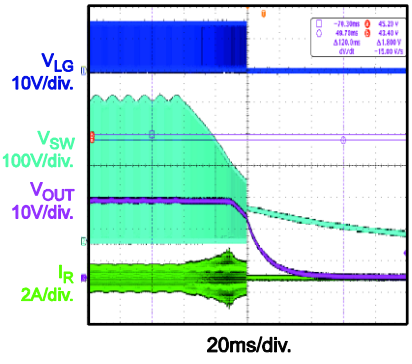
Start-Up

V_{OUT}=24V, I_{OUT}=0A



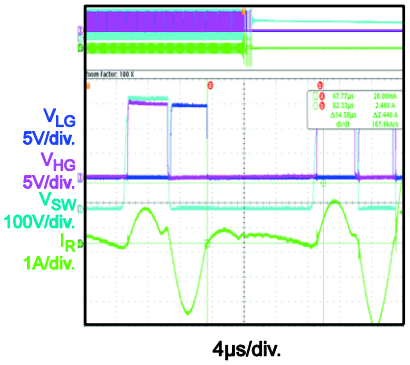
Shutdown

V_{OUT}=24V, I_{OUT}=4.16A



Capacitive-Mode Protection

V_{OUT} Short



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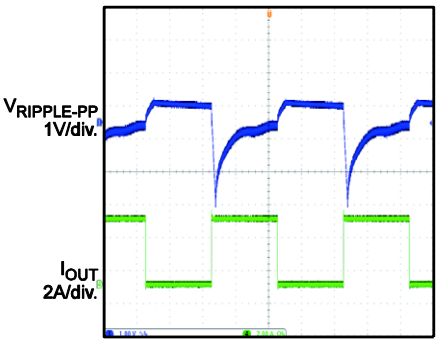
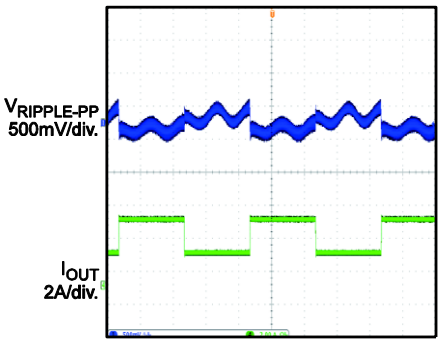
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are generated using the evaluation board built with the design example on page 22, V_{AC} = 120V, V_{OUT} = 24V, I_{OUT} = 4.16A, T_A = 25°C, unless otherwise noted.

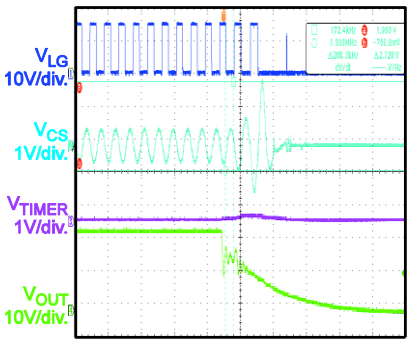
Transient
0A to 4.16A



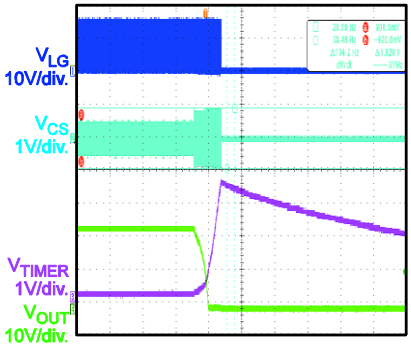
Transient
2.08A to 4.16A



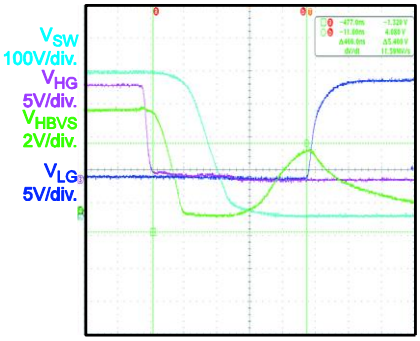
Short Circuit Protection
V_{CS} >1.5V, Latch Off



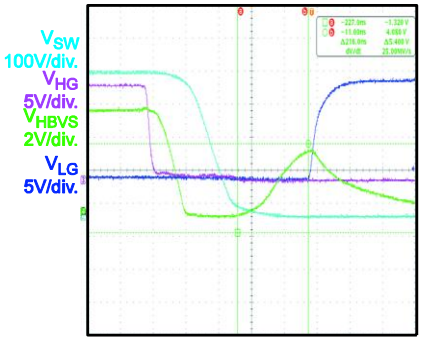
Over-Current Protection
0.8V <V_{CS} <1.5V, Latch Off



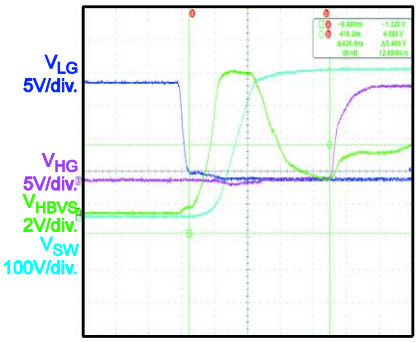
Dead Time when HG Turns Off



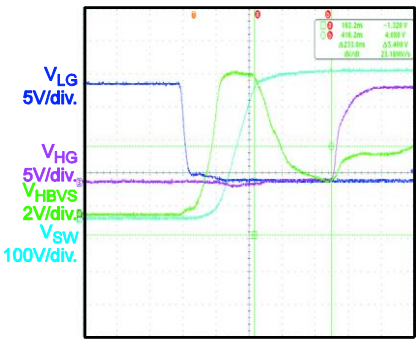
Delay Time when HG Turns Off



Dead Time when LG Turns Off



Delay Time when LG Turns Off



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PIN FUNCTIONS

Pin #	Name	Description
1	SS	**Soft start.** Connect an external capacitor from SS to GND and a resistor to FSET to set the maximum oscillator frequency and the time constant for the frequency shift during start-up. An internal switch discharges the capacitor when the chip turns off (VCC < UVLO, BO < 1.81V or > 5.5V, LATCH > 1.85V, CS > 1.5V, TIMER > 2V, thermal shutdown) to guarantee a soft start.
2	TIMER	**Period between over-current and shutdown.** Connect a capacitor and a resistor from TIMER to GND to set the maximum duration from an over-current condition before the IC stops switching. Whenever the voltage on CS exceeds 0.78V, an internal 130μA current source charges the capacitor. An external resistor discharges this capacitor slowly. If the voltage on TIMER reaches 2V, the soft-start capacitor discharges completely, raising its switching frequency to its maximum value. The 130μA current source remains on. When the voltage exceeds 3.5V, the IC stops switching and latches. The internal current source turns off, and the voltage decays. Two events are required for the IC to resume soft start: 1) the voltage on TIMER must drop below 0.28V; 2) VCC must drop below the UVLO threshold and rise up to the VCC high threshold.
3	CT	**Time set.** An internal current source programmed by an external network connected to FSET charges and discharges a capacitor connected to GND. This determines the converter's switching frequency.
4	FSET	**Switching frequency set.** FSET provides a precise 2V reference. A resistor connected from FSET to GND defines a current that sets the minimum oscillator frequency. Connect the phototransistor of an optocoupler to FSET through a resistor to close the feedback loop that modulates the oscillator frequency. This regulates the converter's output voltage. The value of this resistor sets the maximum operating frequency. An R-C series connected from FSET to GND sets the frequency shift at start-up to prevent excessive inrush energy.
5	BURST	**Burst mode operation threshold.** BURST senses the voltage related to the feedback control, which is compared to an internal reference (1.23V). When the voltage on BURST is lower than this reference, the IC enters an idle state and reduces its quiescent current. When the feedback drives BURST above 1.26V (30mV hysteresis), the chip resumes switching. There is no soft start. The burst function enables burst mode operation when the load falls below a programmed level that is determined by connecting an appropriate resistor to the optocoupler to FSET (see the Block Diagram on page 12). Connect BURST to FSET if burst mode is not used.
6	CS	**Current sense of the half-bridge.** CS uses a sense resistor or a capacitive divider to sense the primary-side current. CS has the following functions: • Over-current regulation: If the sensed voltage exceeds the 0.78V threshold, the soft-start capacitor on SS discharges internally. The frequency increases, limiting the power throughout. Under an output short circuit, this normally results in a near-constant peak primary current. TIMER limits the duration of this condition. • Over-current protection (OCP): If the primary-side current continues to rise despite the frequency increase, OCP enters latch mode when V_{CS} > 1.5V. This requires cycling the IC supply voltage to restart. The latch is removed once the voltage on VCC drops below the UVLO threshold. • Capacitive mode protection (CMP): Once LG turns off, CS is compared to the V_{CSNR} capacitive mode protection (CMP) threshold. If V_{CS} > V_{CSNR}, the HG gate is blocked from turning on until the slope is detected or the CMP timer is complete. When HG turns off, CS is compared to the V_{CSPR} CMP threshold. If Vcs < V_{CSPR}, the low-side gate is blocked from turning on until the slope is detected or the CMP timer is complete. If a capacitive mode status is detected, SS is not discharged immediately; there is a 1μs delay. After the blanking time delay, SS is discharged if the capacitive mode fault remains. This prevents the influence of CS noise effectively. Connect CS to GND if the CMP function is not used.

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PIN FUNCTIONS *(continued)*

Pin #	Name	Description
7	BO	**Input voltage sense and brown-in/brown-out protection.** If the voltage on BO is over 2.3V, the IC enables the gate driver. If the voltage on BO is below 1.81V, the IC is disabled.
8	LATCH	**IC latch off**. When the voltage on LATCH exceeds 1.85V, the IC shuts down and lowers its bias current to its pre-start-up level. LATCH is reset when the voltage on VCC is discharged below its UVLO threshold. Connect LATCH to GND if the function is not used.
9	HBVS	**Half-bridge dV/dt sense.** To detect the dV/dt of the half-bridge, a high-voltage capacitor is connected between SW and HBVS. The dV/dt current through HVBS is used to adjust the dead-time adaptively between the high-side gate and the low-side gate.
10	GND	**Ground.** GND is the current return for both the low-side gate driver and the IC bias. Connect all external ground connections with a trace to GND, one for signals and a second for pulsed current return.
11	LG	**Low-side gate driver output.** The driver is capable of a 0.8A of source/sink peak current to drive the lower MOSFET of the half-bridge. LG is pulled to GND during UVLO.
12	VCC	**Supply voltage.** VCC supplies both the IC bias and the low-side gate driver. Use a small bypass capacitor (e.g.: 0.1µF) to get a clean bias voltage for the IC signal.
13	NC	**High-voltage spacer.** No internal connection. NC isolates the high-voltage pin and eases compliance with safety regulations (creepage distance) on the PCB.
14	SW	**High-side switch source.** SW is the current return for the high-side gate drive current. SW requires careful layout to prevent large spikes below ground.
15	HG	**High-side floating gate driver output.** HG is capable of a 0.8A source/sink peak current to drive the upper MOSFET of the half-bridge. Connect an internal resistor to SW to ensure that HG does not float during UVLO.
16	BST	**Bias for floating voltage supply of the high-side gate driver.** Connect a bootstrap capacitor between BST and SW. This capacitor is charged by an internal bootstrap diode driven in phase with the low-side gate driver.

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BLOCK DIAGRAM

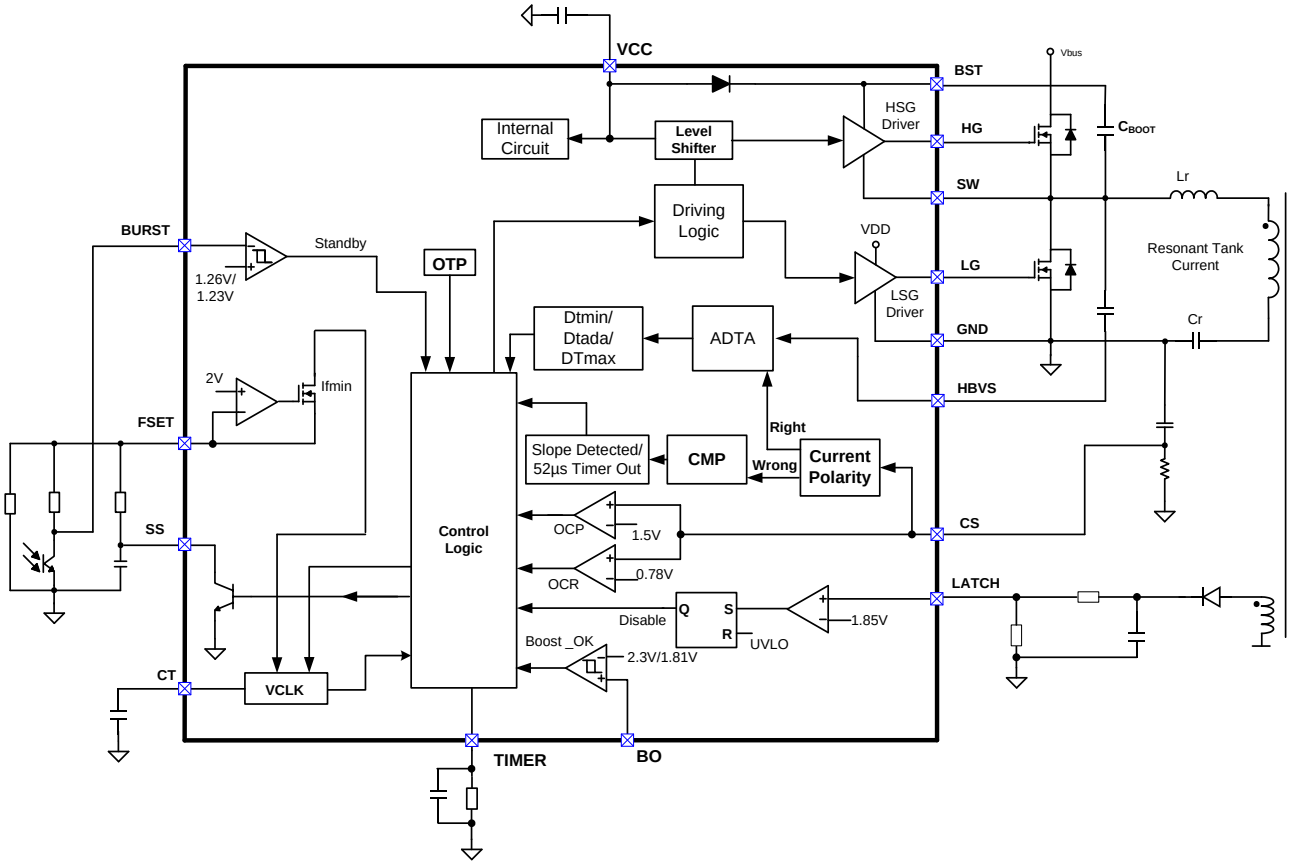

Figure 1: Functional Block Diagram

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APPLICATION INFORMATION

Oscillator

Figure 2 shows the oscillator block diagram. A modulated current charges and discharges the CT capacitor repeatedly between its peak valley thresholds, which determines the oscillator frequency.

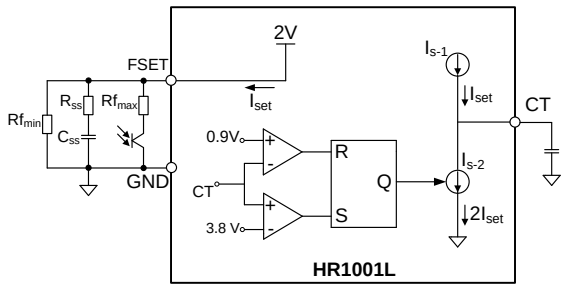

Figure 2: Oscillator Block Diagram

FSET sets the CT charging current, I_{SET} (I_{S-1}). When CT passes its peak threshold (3.8V), the filp-flop is set, and a discharging current source of twice the charge current is enabled. The difference between these two currents forces the charging and discharging of CT to be equal. When the voltage on the CT capacitor falls below its valley threshold (0.9 V), the flip-flop is reset and turns off the discharging current source. This starts a new switching cycle. Figure 3 shows the detailed waveform of the oscillator.

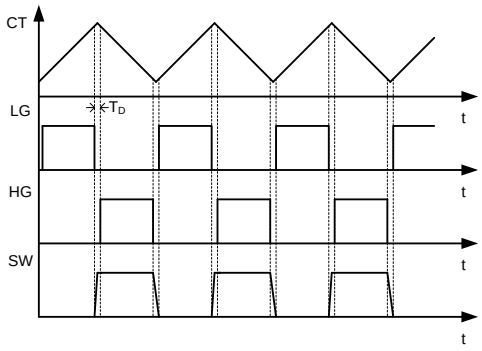

Figure 3: CT Waveform and Gate Signal

- An R-C network connected to FSET externally determines the normal switching frequency and the soft start switching frequency.

Rf_{min} from FSET to GND contributes to the maximum resistance of the external R-C network when the phototransistor does not conduct. This sets the FSET minimum source current, which defines the minimum switching frequency.

Under normal operation, the phototransistor adjusts the current flow through Rf_{max} to modulate the frequency for output voltage regulation. When the phototransistor is saturated, the current through Rf_{max} is at its maximum, which sets the frequency at its maximum.

An R-C in series connected between FSET and GND shifts the frequency at start-up. Please see the Soft-Start Operation section on page 14 for details.

Set the minimum and maximum frequencies with Equation (1) and Equation (2):

$$f_{min} = \frac{1}{3 \cdot CT \cdot Rf_{min}} \quad (1)$$

$$f_{max} = \frac{1}{3 \cdot CT \cdot (Rf_{min} \,||\, Rf_{max})} \quad (2)$$

Typically, the CT capacitance is between 0.1nF and 1nF. Calculate Rf_{min} and Rf_{max} with Equation (3) and Equation (4) :

$$Rf_{min} = \frac{1}{3 \cdot CT \cdot f_{min}} \quad (3)$$

$$Rf_{max} = \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1} \quad (4)$$

It is recommended to use a CT capacitor less than or equal to 330pF for best overall temperature performance.

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Soft-Start (SS) Operation

For the resonant half-bridge converter, the power delivered is inversely proportional to its switching frequency. To ensure that the converter starts or restarts with safe currents, the soft start forces a high initial switching frequency until the value is controlled by the closed loop.

The soft start is achieved using an external R-C series circuit (see Figure 4).

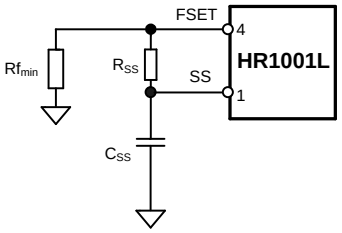

Figure 4: Soft-Start Block

When the IC starts up, the SS voltage is 0V, and the soft-start resistor (R_{SS}) is in parallel to Rf_{min}. Rf_{min} and R_{SS} determine the initial frequency, which can be calculated with Equation (5):

$$f_{start} = \frac{1}{3 \cdot CT \cdot (Rf_{min} || R_{ss})} \quad (5)$$

During start-up, C_{SS} charges until its voltage reaches the reference (2V) and the current through R_{SS} decays to zero. This period takes about $5x(R_{SS}xC_{SS})$ microseconds. During this period, the switching frequency change follows an exponential curve. Initially, the C_{SS} charge reduces the frequency relatively quickly, but the rate decreases gradually.

After the soft-start period, the switching frequency is dominated by the feedback loop to regulate the output voltage.

With the soft start, the current of the resonant tank increases gradually during start-up.

Select the soft-start R-C network with Equation (6) and Equation (7) :

$$R_{ss} = \frac{Rf_{min}}{\frac{f_{start}}{f_{min}} - 1} \quad (6)$$

$$C_{ss} = \frac{3 \cdot 10^{-3}}{R_{ss}} \quad (7)$$

Select an initial frequency (f_{start}) at least four times f_{min}. When selecting C_{SS}, there is a trade-off between the desired soft-start operation and the over-current protection (OCP) speed. See the Over-Current Protection section on page 17 for details.

Adaptive Dead-Time Adjustment (ADTA)

When operating in inductive mode, the soft switching of the power MOSFETs results in high efficiency of the resonant converter. A fixed dead time may result in hard switching at light load, especially when the magnetizing inductance (Lm) is too large. A dead time that is too long may lead to loss of the ZVS state. The current may change polarity during the dead time, which can result in capacitive mode switching. The adaptive dead-time control adjusts the dead time automatically by detecting the dV/dt of the half-bridge switching node (SW).

The HR1001L incorporates an intelligent adaptive dead-time adjustment (ADTA) logic circuit, which detects the dV/dt of SW and inserts a proper dead time automatically. For the external circuit, connect a capacitor (5pF, typically) between SW and HBVS to sense dV/dt. Figure 5 shows the simplified block diagram of ADTA. Figure 6 shows the operation waveform of ADTA.

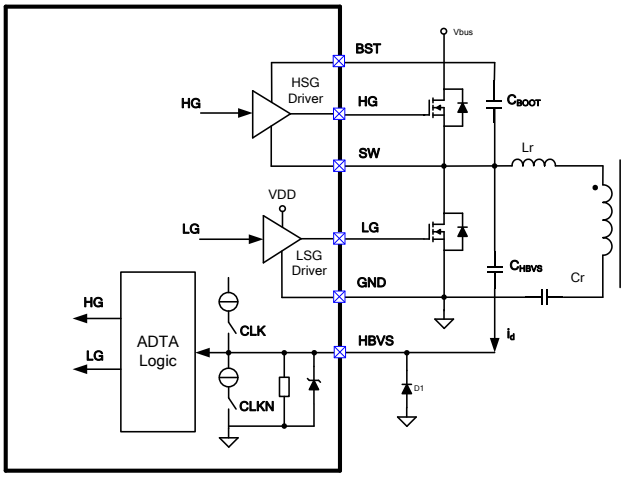

Figure 5: Block Diagram of ADTA

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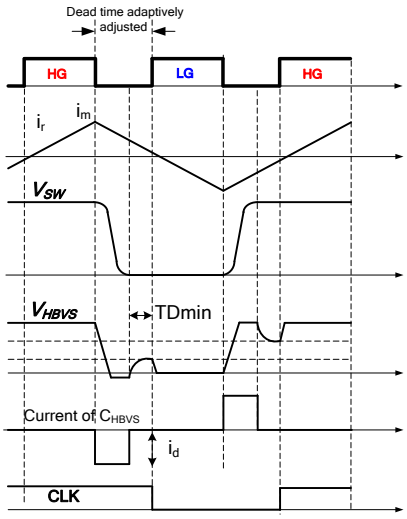

Figure 6: Operation Waveform of ADTA

When HG switches off, the SW voltage swings from high to low due to the resonant tank current (I_r). Accordingly, this negative dV/dt pulls current from HBVS via C_{HBVS}. If the dV/dt current is higher than the internal comparison current, the HBVS voltage (V_{HBVS}) is pulled down and clamped at zero. When SW stops slewing and the differential current stops, V_{HBVS} begins ramping up. LG turns on after a delay (minimum dead time). Dead time is defined as the duration between HG turning off and LG turning on.

When LG switches off, the SW voltage swings from low to high, and a positive dV/dt current is detected via C_{HBVS}. The dead time between LG turning off and HG turning on is maintained automatically by sensing the dV/dt current.

To avoid damaging HBVS, C_{HBVS} should be selected with careful consideration. Keep the dV/dt current below 65mA using Equation (8):

$$i_d = \left| C_{HBVS} \frac{dv}{dt} \right| < 65mA \quad (8)$$

If C_{HBVS} is too low to sense the dV/dt, the minimum voltage change rate (dV_{min}/dt) must be accounted for to design the proper C_{HBVS}.

First, calculate the peak magnetizing current (I_m) with Equation (9):

$$I_m = \frac{V_{in}}{8 \cdot L_m \cdot f_{max}} \quad (9)$$

Design C_{HBVS} using Equation (10):

$$C_{HBVS} > \frac{700\mu A}{I_m} \frac{C_{oss}}{2} \quad (10)$$

Where C_{oss} is the output capacitance when the drain-source voltage on the MOSFET is near zero volts (refer to the C_{oss} characteristics curve in the MOSFET's datasheet).

In a typical design, Lm = 870µH, V_{IN} = 450Vdc, and f_{max} = 140kHz, and C_{HBVS} is calculated at 4.5pF. 5pF is suitable for most MOSFETs.

Figure 7 illustrates a possible dead time by ADTA logic. Note that there are three kinds of dead time: minimum dead time (DT_{MIN}), maximum dead time (DT_{MAX}), and adjusted dead time (DT_{ADJ}), which is between DT_{MIN} and DT_{MAX}. ADTA logic sets DT_{MIN} = 235ns. When the SW transition time is smaller than DT_{MIN}, the logic does not let the gate turn on, which prevents a shoot-through between the low-side and high-side MOSFETs. A maximum dead time (DT_{MAX} = 1µs) forces the gate to turn on, preventing duty cycle losses or soft switching.

ADTA adjusts the dead time automatically and ensures zero-voltage switching (ZVS), which enables more flexibility in the MOSFET and Lm selection. ADTA also prevents hard switching if the design does not account for light load or no load carefully. At light load, the switching frequency goes high, and the magnetizing current goes low, risking hard switching that can lead to a thermal or reliability issue.

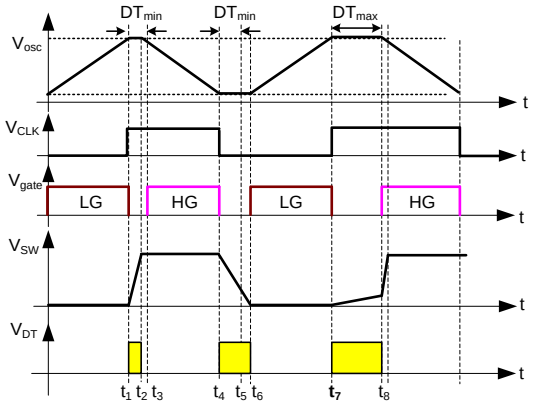

Figure 7: Dead Time in ADTA

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If HBVS is not connected, the internal circuit cannot detect the differential current from HBVS, so the dead time remains fixed at 350ns.

Figure 8 and Figure 9 show the waveforms of the dead time when HG turns off and when LG turns off respectively. ADTA logic inserts the dead time automatically according to the transition shape of SW.

If HBVS is pulled down too low by the negative current of C_{HBVS}, the dead time from HG turning off to LG turning on may be too long. To clamp HBVS at zero and ensure an optimum dead time, connect a Schottky diode (D1) (such as BAT54) on HBVS to GND.

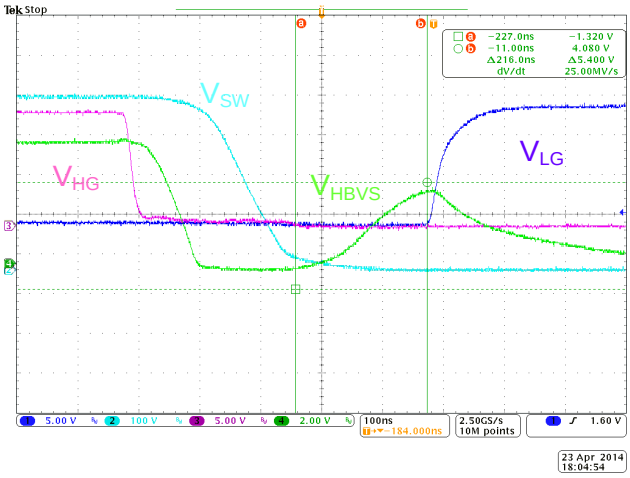

Figure 8: Dead Time at High-to-Low Transition

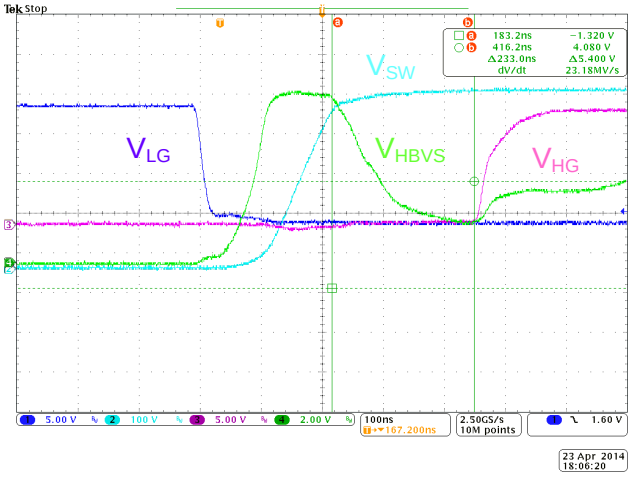

Figure 9: Dead Time at Low-to-High Transition

Capacitive Mode Protection (CMP)

When the resonant HB converter output is in overload or short circuit condition, it may cause the converter to run into a capacitive region. In capacitive mode, the voltage applied to the resonant tank causes the current of the resonant tank to lag. Under this condition, the body diode of one of the MOSFETs is conducting. The other MOSFET should not be turned on to avoid device failure. The functional block diagram of capacitive mode protection (CMP) is shown in Figure 10.

Figure 11 shows the operating current principle of CMP. CSPOS and CSNEG stand for the current polarity, which is generated by comparing the voltage on CS with the internal V_{CSNR} and V_{CSPR} voltage reference.

At t0, LG turns off. CSNEG is high, which means the current is in the correct direction and is operating in inductive mode.

At t1, HG turns off. CSPOS is high, which means the current is in the correct direction and is operating in inductive mode.

At t2, LG turns off for a second time. CSNEG is low, indicating that the current is in the wrong direction (the low-side MOSFET body diode is conducting), and the converter is operating in capacitive mode.

SW does not swing high until the current returns to the correct polarity. DT stays high and V_{OSC} is stopped, preventing the other MOSFET from turning on. This prevents capacitive switching.

At t3, the current returns to the correct polarity, and the other MOSFET turns on after the dV/dt current is detected.

Between t2 and t5, the correct current polarity cannot be detected, or there is so little current that SW is unable to be pulled up or down.

Eventually, the timer (52μs) for CMP expires, and the other MOSFET is forced to switch on (see Figure 11).

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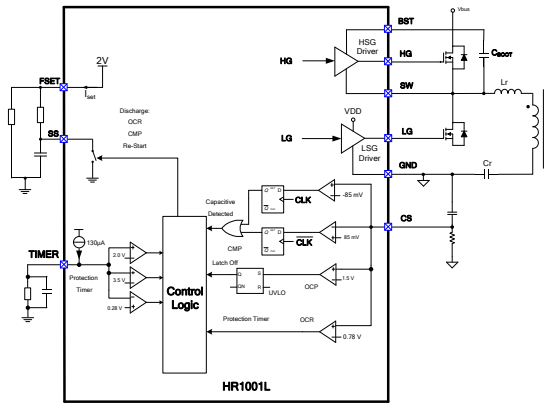

Figure 10: Block Diagram of CMP and OCP

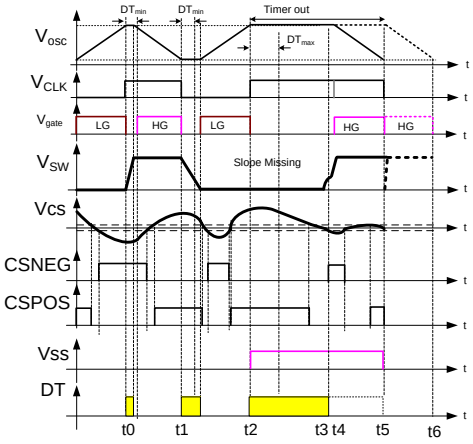

Figure 11: Operating Principle of CMP

When capacitive mode operation is detected, the V_{SS} control signal goes high, turning on an internal transistor to discharge C_{SS} (after a 1µs blanking delay). This causes the frequency to increase to a very high level quickly to limit the output power. The V_{SS} control is reset, and the soft start is activated when the first gate driver is switched off after CMP. The switching frequency decreases smoothly until the control loop takes over.

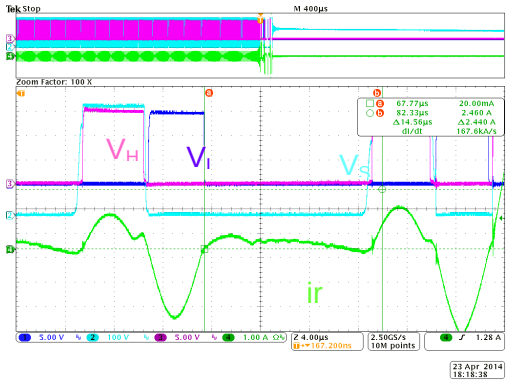

Figure 12: Capacitive Mode Protection Waveform

Figure 12 shows the CMP behavior when the output is shorted. The current polarity goes in the wrong direction when LG switches off. The CMP logic detects this capacitive mode immediately and prevents HG from turning on. This prevents destructive capacitive switching. Once the current (Ir) returns to the correct polarity, SW ramps up, dV/dt current is detected, and HG turns on at the ZVS state.

Over-Current Protection (OCP)

The HR1001L provides two levels of over-current protection (see Figure 13).

The first level of protection occurs when the voltage on CS (V_{CS}) exceeds 0.78V. Once this occurs, two actions take place. First, the internal transistor connected between SS and GND turns on for at least 10µs, which discharges C_{SS}. This creates a sharp increase in the oscillator frequency, reducing the energy transferred to the output. Second, an internal 130µA current source turns on to charge C_{TIMER}, ramping up the TIMER voltage. If V_{CS} drops below 0.78V before the voltage on TIMER (V_{TIMER}) reaches 2V, both the discharge of C_{SS} and the charge of C_{TIMER} are stopped. The converter resumes normal operation.

t_{OC} is the time for V_{TIMER} to rise from 0V to 2V. It is a delay time for over-current regulation. There is no simple relationship between t_{OC} and C_{TIMER}. Select C_{TIMER} based on experimental results. Based on experiments, C_{TIMER} may increase the operating time by 100ms. If V_{CS} is still larger than 0.78V after V_{TIMER} rises to 2V, C_{ss} is discharged completely. Simultaneously, the internal 130µA current source continues to charge C_{TIMER} until V_{TIMER} reaches 3.5V, then turns off all gate drivers and enters a latch-off mode. The latch is reset when the voltage on VCC is lower than the UVLO threshold.

Use Equation (11) to calculate the time it takes for V_{TIMER} to rise from 2V to 3.5V:

$$t_{OP} = 10^4 \cdot C_{TIMER} \quad (11)$$

Even if the latch is reset, the HR1001L will enter soft start again until V_{TIMER} decreases to 0.28V. Calculate this time period with Equation (12):

$$t_{OFF} = R_{TIMER} \cdot C_{TIMER} \cdot \ln\frac{3.5}{0.28} \approx 2.5 R_{TIMER} \cdot C_{TIMER} \quad (12)$$

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The second level of protection is triggered when V_{CS} rises to 1.5V. Typically, this condition occurs when V_{CS} continues to rise during a short circuit. The IC stops switching immediately and latches off until the voltage on VCC drops below the UVLO threshold.

The time sequence of OCP is shown in Figure 13. OCP limits the energy transferred from the primary side to the secondary side during an overload or short-circuit condition. Excessive power consumption due to high continuous currents can damage the secondary-side windings and rectifiers. When OCP is triggered, the converter enters a latched-off protection mode.

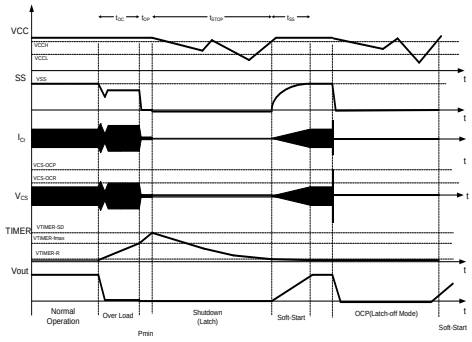

Figure 13: OCP Timing Sequence

Current Sensing

There are two current sensing methods: lossless current sensing and current sensing with a sense resistor.

Generally, a lossless current sensing solution is used in high-power applications (see Figure 14).

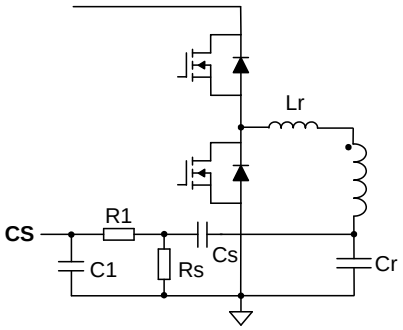

Figure 14: Current Sensing with a Lossless Network

Design the lossless current sensing network with Equation (13):

$$Cs \le \frac{Cr}{100} \quad (13)$$

Calculate R_S with Equation (14):

$$Rs < \frac{0.8}{I_{Crpk}} \cdot (1 + \frac{C_r}{C_S}) \quad (14)$$

Where I_{Crpk} is the peak current of the resonant tank at a low input voltage and full load, and can be calculated with Equation (15):

$$I_{Crpk} = \sqrt{(\frac{NV_O}{4L_m f_s})^2 + (\frac{I_O \pi}{2N})^2} \quad (15)$$

Where N is the turns ratio of the transformer, lo is the output current, Vo is the output voltage, f_S is the switching frequency, and L_m is the magnetizing inductance.

For capacitive mode detection in no-load or small-load condition, R_S should fulfill the condition in Equation (16):

$$R_S > \frac{85mV}{I_m}(1 + \frac{C_r}{C_S}) \quad (16)$$

In some conditions, especially when a large L_m is used, it is difficult to satisfy both Equation (14) and Equation (16). The IC will operate without CMP function at light load if it is not under the restriction of Equation (16). The R1 and C1 network is used to attenuate switching noise on CS. The time constant should be in the range of 100ns.

An alternate solution uses a sense resistor in series with the resonant tank (see Figure 15). This method is simple, but causes unnecessary power loss on the sense resistor.

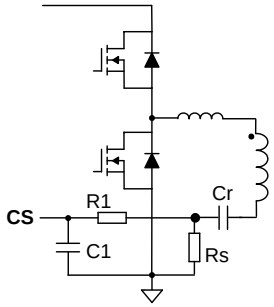

Figure 15: Current Sensing with a Sense Resistor

Design the sense resistor using Equation (17):

$$R_S = \frac{0.78}{I_{Crpk}} \quad (17)$$

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Input Voltage Sensing (BI/BO)

The HR1001L stops switching when the input voltage drops below a specified value and restarts when the input voltage returns to normal. This function guarantees that the resonant half-bridge converter always operates within the specified input-voltage range. The IC senses the voltage on BO (V_{BO}) through the tap of a resistor divider connected to the rectified AC voltage or the PFC output.

Figure 16 shows the line-sensing internal block diagram.

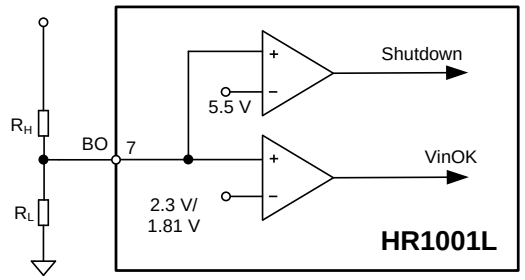

Figure 16: Input Voltage Sensing Block

If V_{BO} is higher than 2.3V, the IC provides the gate driver outputs. The IC does not stop the gate driver until V_{BO} drops below 1.81V.

For a minimum operation input voltage of the half-bridge (V_{IN-min}), select a value for R_H large enough to reduce power loss at no load. Then R_L can be calculated with Equation (18):

$$R_L = R_H \cdot \frac{1.81}{V_{IN-min} - 1.81} \quad (18)$$

For additional protection, the IC shuts down when V_{BO} exceeds the internal 5.5V clamp voltage. When V_{BO} is between 2.3V and 5.5V, the IC operates normally.

Burst Mode Operation

At light load or in the absence of a load, the maximum frequency limits the resonant half-bridge switching frequency. To control the output voltage and limit power consumption, the HR1001L enables compatible converters to operate in burst mode. This greatly reduces the average switching frequency, reducing the average residual magnetizing current and the associated losses.

Operating in burst mode requires setting up BURST. If the voltage on BURST (V_{BURST}) drops below 1.23V, the HR1001L shuts down HG and LG, only leaving the 2V reference voltage on FSET and SS to retain the previous state and minimize power consumption. When V_{BURST} exceeds 1.23V by over 30mV, the HR1001L resumes normal operation.

Based on the burst mode operation principle, BURST must be connected to the feedback loop. Figure 17 shows a typical circuit connecting BURST to the feedback signal for narrow input voltage range applications.

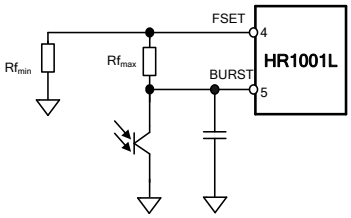

Figure 17: Burst Mode Operation Set-Up

In addition to setting the oscillator maximum frequency at start-up, Rf_{max} determines the maximum burst mode frequency. After determining f_{max}, calculate Rf_{max} with Equation (19):

$$Rf_{max} = \frac{3}{8} \cdot \frac{Rf_{min}}{\frac{f_{max}}{f_{min}} - 1} \quad (19)$$

f_{max} corresponds to a load point (P_{Burst}) where the peak current flow through the transformer is too low to cause audible noise.

The above burst mode introduction is based on a narrow input voltage range. The input voltage determines the switching frequency as well. This means that P_{Burst} has a large variance over the wide input voltage range. To stabilize P_{Burst} over the input range, use the circuit in Figure 18 to insert the input voltage signal into the feedback loop.

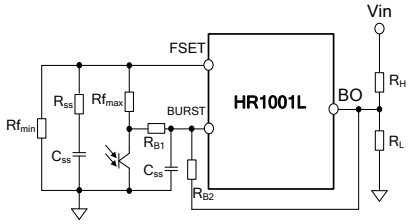

Figure 18: Burst Mode Operation Set-Up for a Wide Input Voltage Range

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R_{B1} and R_{B2} in Figure 18 correct against the wide input voltage range. Select both resistors based on experimental results. Note that the total resistance of R_{B1} and R_{B2} should be much larger than R_H to minimize the effect on V_{BO}. During burst mode operation when the load is lower than P_{Burst}, the switching frequency is clamped at the maximum frequency. The output voltage must rise over the setting value to increase the current flowing through the optocoupler. Therefore, the voltage on Rf_{max} rises due to the increased phototransistor current. Then V_{BURST} drops below 1.23V, triggering the gate signal off state. The current flows through the optocoupler decreases until the output voltage falls below the setting value, causing V_{BURST} to rise. When V_{BURST} exceeds 1.23V by over 30mV, the IC restarts to generate the gate signal. The IC operates in this mode under no load or light load to decrease the average power consumption.

Latch Operation

The HR1001L provides a simple latch-off function through LATCH. Applying an external voltage over 1.85V to HBVS causes the IC to enter a latched shutdown. After the IC is latched, its consumption drops. Resetting the IC requires dropping the VCC voltage below the UVLO threshold (see Figure 19).

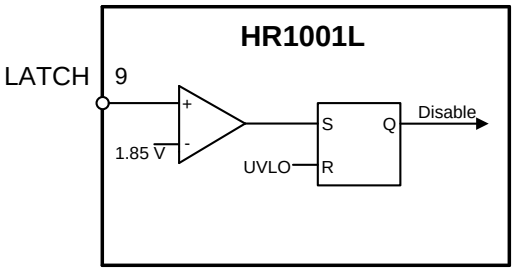

Figure 19: Latch Function Block

High-Side Gate Driver (HG)

The external BST capacitor provides energy to the high-side gate driver. An integrated bootstrap diode charges this capacitor through VCC. This diode simplifies the external driving circuit for the high-side switch, allowing the BST capacitor to charge when the low-side MOSFET is on (see Figure 20).

To provide enough gate driver power (considering the BST capacitor charge time), use a 100nF to 470nF capacitor for the BST capacitor.

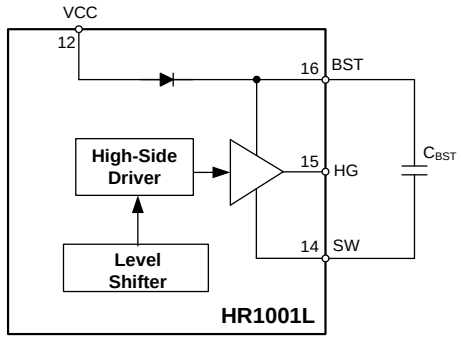

Figure 20: High-Side Gate Driver

Low-Side Gate Driver (LG)

LG provides the gate driver signal for the low-side MOSFET. The maximum voltage on LG is 16V. Under certain applications, a large voltage spike occurs on LG due to oscillations from the long-gate driver wire, the MOSFET parasitic capacitance, and the small gate driver resistor. This voltage spike is dangerous to LG, so a 15V Zener diode close to LG and GND is recommended (see Figure 21).

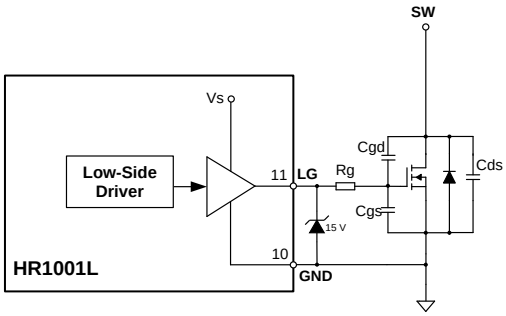

Figure 21: Low-Side Gate Driver

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Design Example

A 100W LED driver is designed with the specifications below (see Table 1).

Table 1: Design Example

Input AC voltage	90 - 305V_{AC}
Output voltage	24V
Output current	4.16A

Figure 22 shows the detailed application schematic. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section.

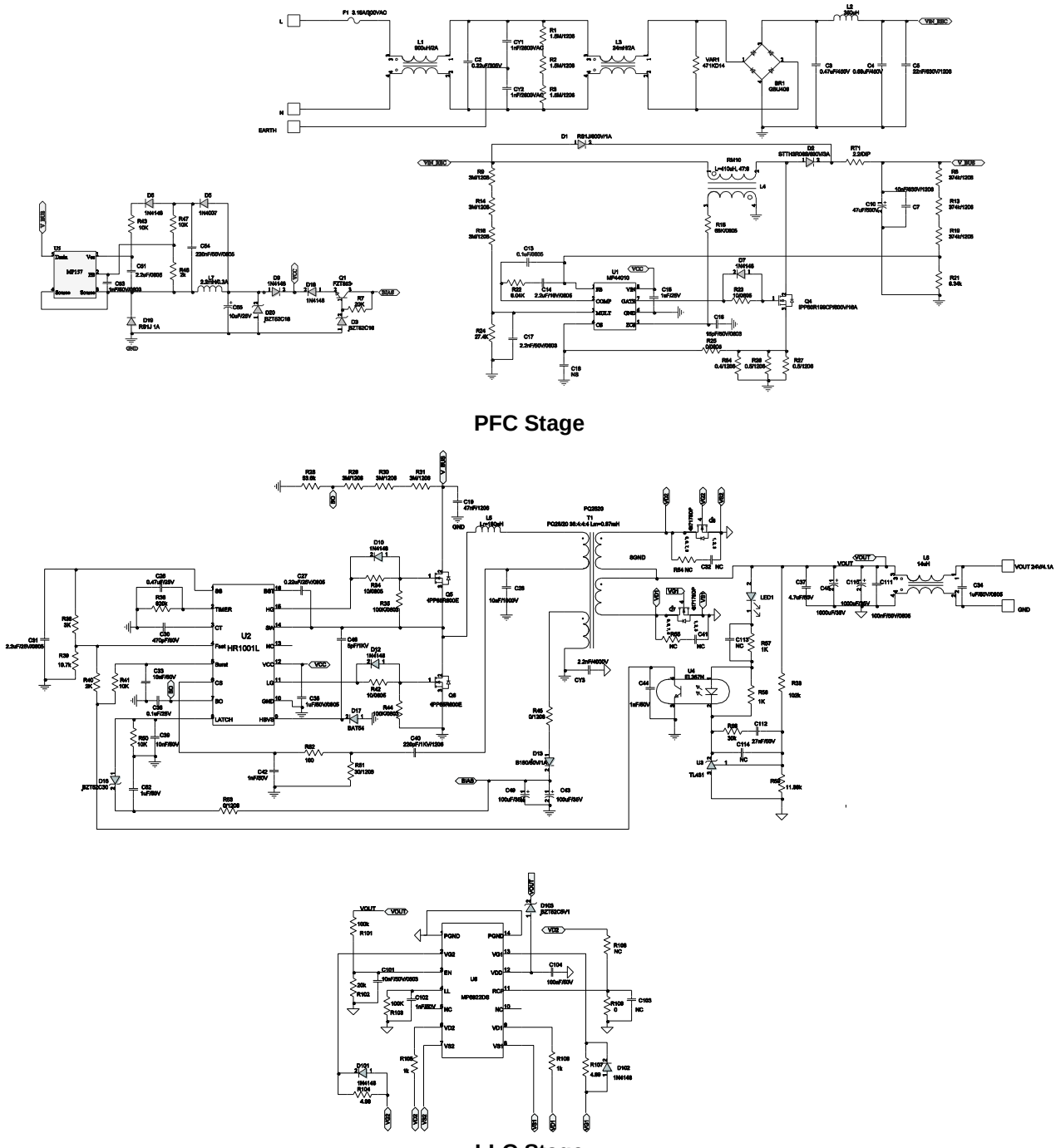

Figure 22: Design Example for a 24V/4.16A Output

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CONTROL FLOW CHART

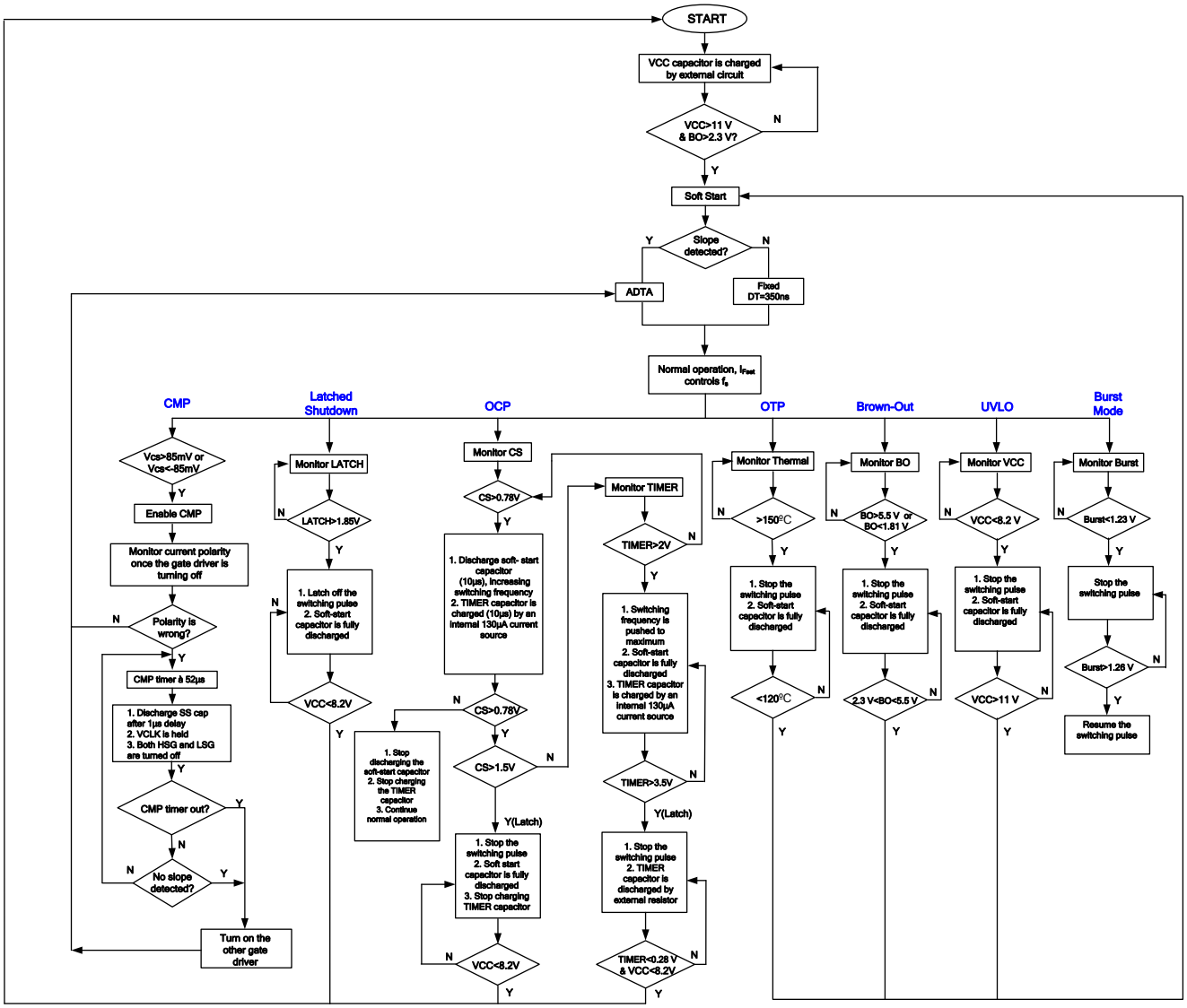

Figure 23: Control Flow Chart

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TYPICAL APPLICATION CIRCUIT

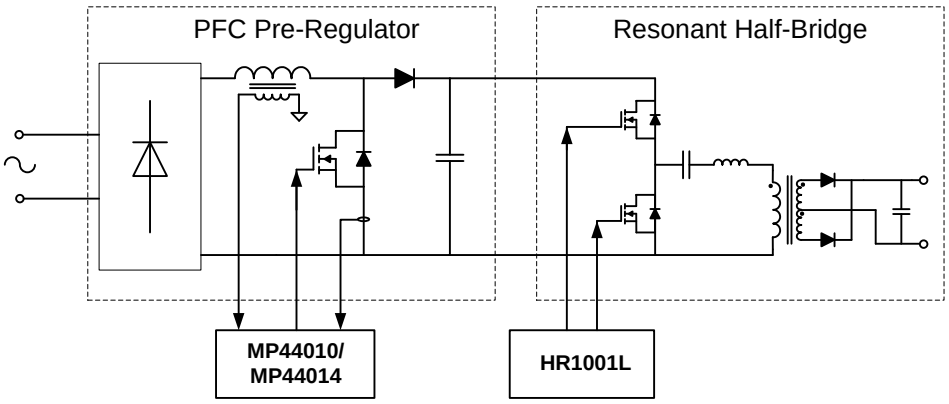

Figure 24: Application Circuit

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SYSTEM TIMING

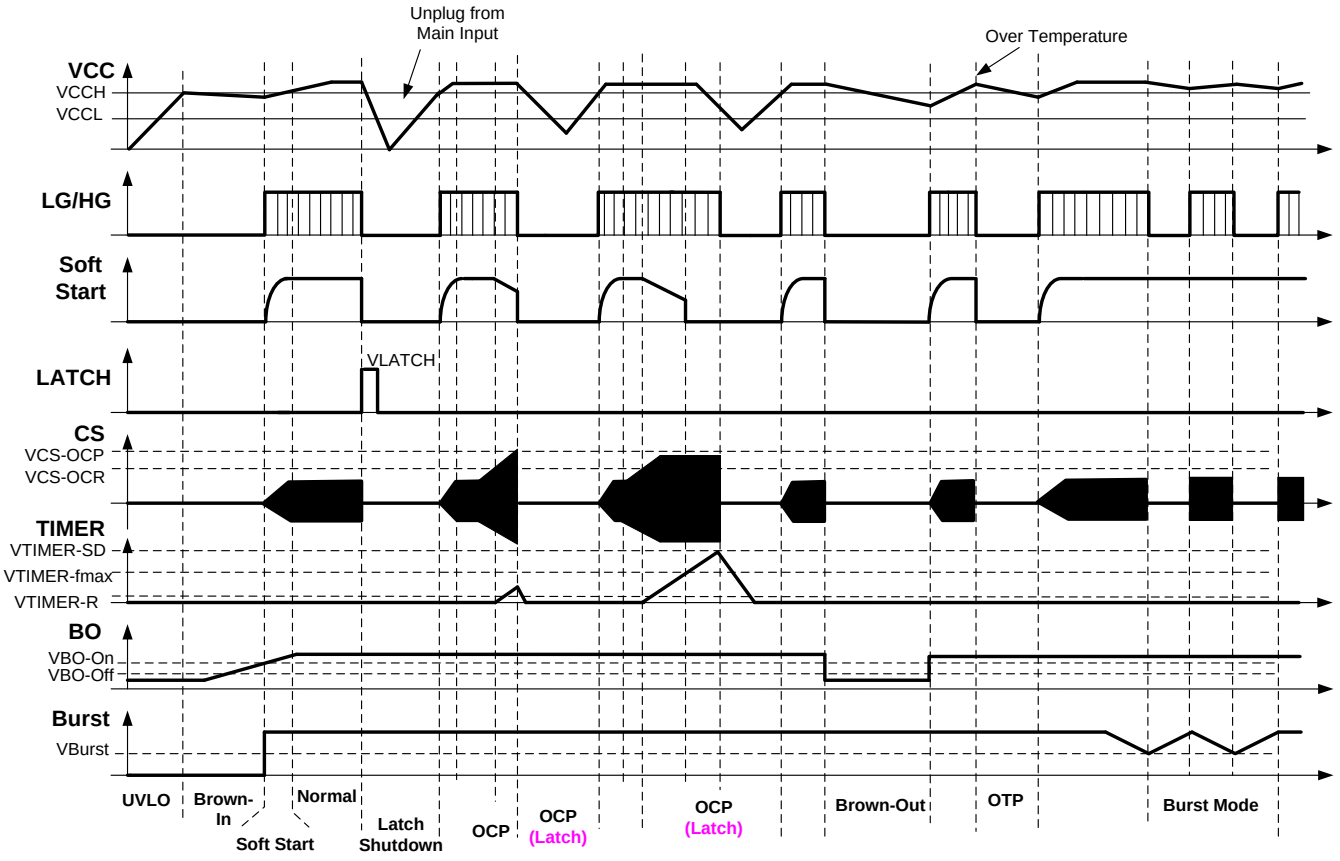

Figure 25: System Timing Diagram

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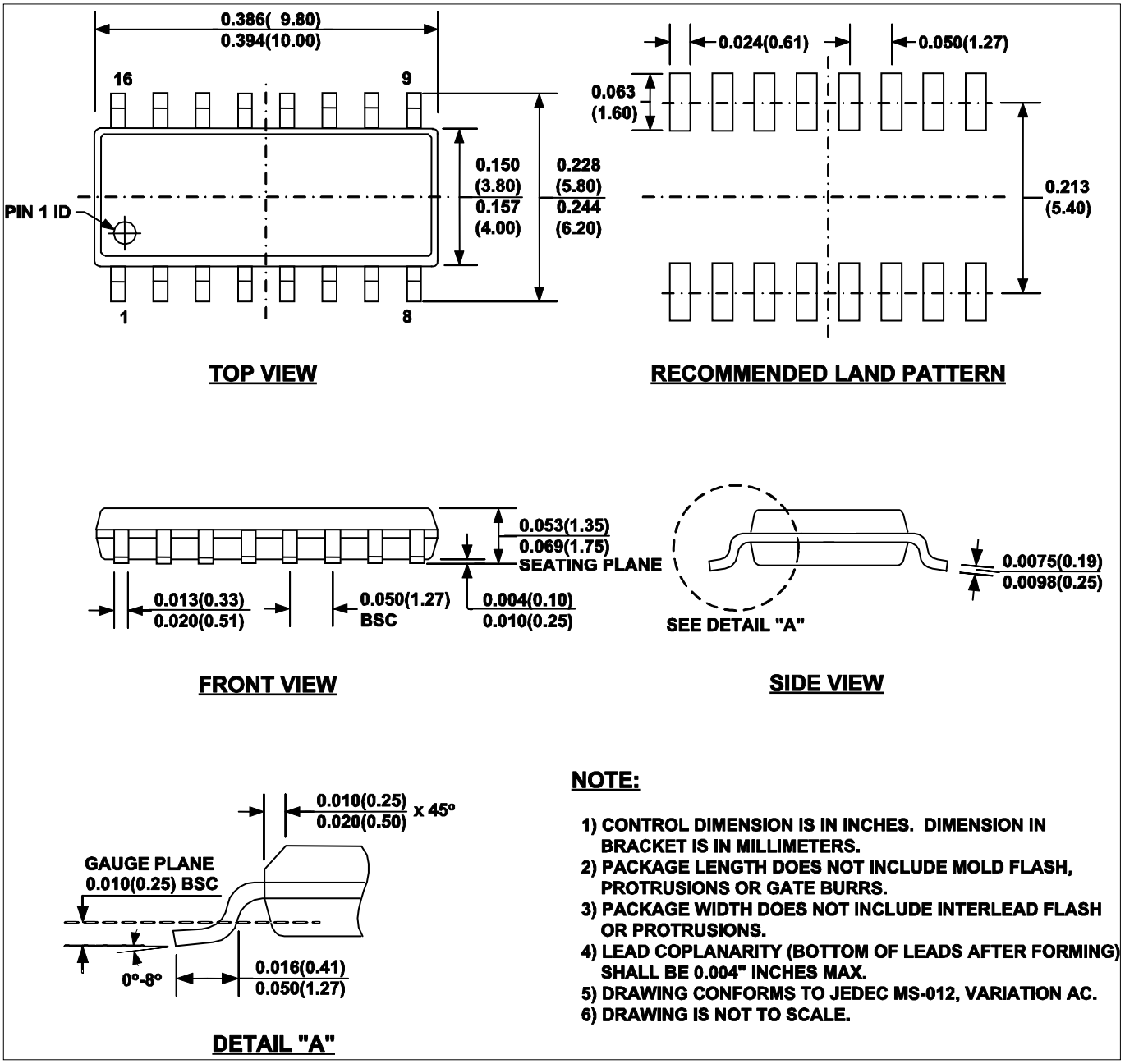
PACKAGE INFORMATION

SOIC-16



NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AC.
6) DRAWING IS NOT TO SCALE.

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