



# MID02W0303A

## 0.25W, 1.5kV<sub>DC</sub>/3kV<sub>DC</sub>, Regulated, Isolated DC/DC Converter

### DESCRIPTION

The MID02W0303A is a regulated, isolated DC/DC converter that can support 3V to 3.6V input voltage ( $V_{IN}$ ) applications across a  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature range. It has excellent load regulation, line regulation, and supports up to 0.25W of output power ( $P_{OUT}$ ).

The device integrates a power MOSFET, transformer, and feedback (FB) circuit all in one chip. The MID02W0303A is a small solution that provides high reliability compared to traditional isolated power modules.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), and OTP protection.

The MID02W0303A requires a minimal number of readily available, standard external components. It is available in a low-profile, wide body SOICW-16 package.

### FEATURES

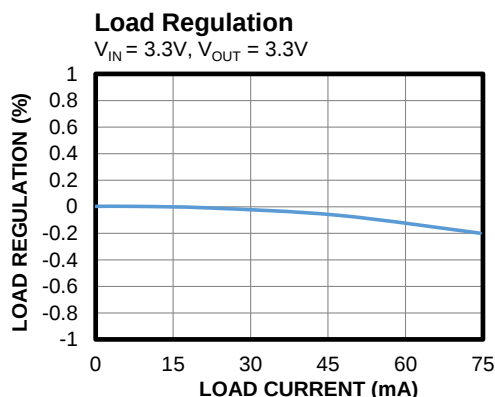
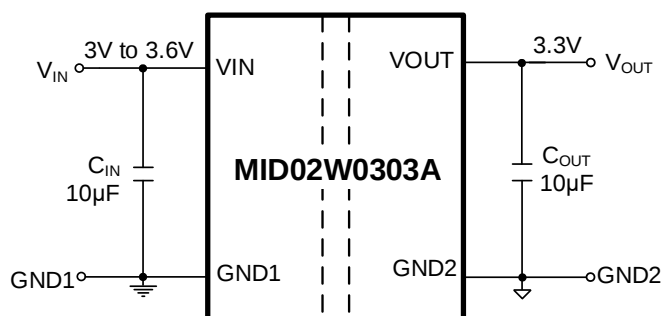
- 3V to 3.6V Operating Input Voltage ( $V_{IN}$ ) Range
- 1.5kV<sub>DC</sub> or 3kV<sub>DC</sub> Isolation Voltage
- Up to 0.25W Output Power ( $P_{OUT}$ )
- Max 50% Efficiency at Full Loads
- 0.2% Load Regulation
- 0.1% Line Regulation
- Excellent Transient Response
- Continuous Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Protection (OTP)
- Meets CISPR32 Class B Emissions
- UL1577 Certified
- CB Certified per IEC62368-1 3<sup>rd</sup> Edition
- $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Operating Temperature Range
- Available in an SOICW-16 Package

### APPLICATIONS

- Industrial Automation Systems
- Isolated Bias Power for Digital Isolators
- Isolated Bias Power for RS-485, RS-422, and CAN Interfaces
- Isolated Sensor Power Supplies
- Telecom and Network Devices (e.g. 5G RRU's, Industrial CPE, and Network Gateways)

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS", the MPS logo, and "Simple, Easy Solutions" are trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

### TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number        | Isolation Voltage   | Package  | Top Marking | MSL Rating |
|--------------------|---------------------|----------|-------------|------------|
| MID02W0303AGY-2R*  | 1.5kV <sub>DC</sub> | SOICW-16 | See Below   | 3          |
| MID02W0303AGY-3R** | 3kV <sub>DC</sub>   |          |             |            |

\* For Tape & Reel, add suffix -Z (e.g. MID02W0303AGY-2R-Z).

\*\* For Tape & Reel, add suffix -Z (e.g. MID02W0303AGY-3R-Z).

## TOP MARKING (MID02W0303AGY-2R)

MPS YYWW  
**02W0303A2**  
**LLLLLLLLLL**

MPS: MPS prefix

YY: Year code

WW: Week code

02W0303A2: First nine digits of the part number

LLLLLLLLLL: Lot number

## TOP MARKING (MID02W0303AGY-3R)

MPS YYWW  
**02W0303A3**  
**LLLLLLLLLL**

MPS: MPS prefix

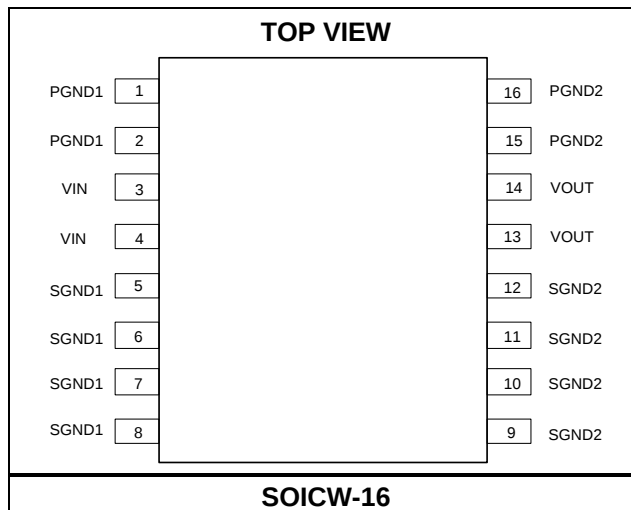
YY: Year code

WW: Week code

02W0303A3: First nine digits of the part number

LLLLLLLLLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #         | Name  | Description                                                                                                                                                                          |
|---------------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 2          | PGND1 | <b>Power ground side 1.</b> Connect the PGND1 pin using large copper traces and multiple vias to improve thermal performance.                                                        |
| 3, 4          | VIN   | <b>Power input.</b> Connect the VIN pin to a 3V to 3.6V power supply. Connect a 10 $\mu$ F capacitor and a 0.1 $\mu$ F capacitor between the VIN and PGND1 pins to stabilize the IC. |
| 5, 6, 7, 8    | SGND1 | <b>Signal ground side 1.</b> Connect the SGND1 and PGND1 pins using large copper traces to improve thermal performance.                                                              |
| 9, 10, 11, 12 | SGND2 | <b>Signal ground side 2.</b> Connect the SGND2 and PGND2 pins using a thin trace. Do not connect SGND2 using large copper traces, as this can increase EMI.                          |
| 13, 14        | VOUT  | <b>Power output.</b> Connect a 10 $\mu$ F capacitor and a 0.1 $\mu$ F capacitor between the VOUT and PGND2 pins to decrease the output voltage ( $V_{OUT}$ ) ripple and noise.       |
| 15, 16        | PGND2 | <b>Power ground side 2.</b> Do not connect the PGND2 pin using large copper traces, as this can increase EMI.                                                                        |

ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

VIN to PGND1 or SGND1 ..... -0.3V to +5V  
 VOUT to PGND2 or SGND2 ..... -0.3V to +5V  
 Continuous power dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>(2)</sup> <sup>(4)</sup>  
 ..... 2.65W  
 Junction temperature ..... 150 $^\circ\text{C}$   
 Lead temperature ..... 260 $^\circ\text{C}$   
 Storage temperature ..... -65 $^\circ\text{C}$  to +150 $^\circ\text{C}$

## ESD Ratings

Human body model (HBM) ..... 6000V  
 Charged device model (CDM) ..... 2000V

Recommended Operating Conditions <sup>(3)</sup>

Input voltage ( $V_{IN}$ ) ..... 3V to 3.6V  
 Output voltage ( $V_{OUT}$ ) ..... 3.3V  
 Operating junction temp ( $T_J$ ) .... -40 $^\circ\text{C}$  to +125 $^\circ\text{C}$

## Thermal Resistance

 $\theta_{JA}$   $\theta_{JC}$ 

EV02W0303A-3-Y-00A <sup>(4)</sup> ..... 47 ..... 11 .....  $^\circ\text{C/W}$   
 SOICW-16 <sup>(5)</sup> ..... 48 ..... 23 .....  $^\circ\text{C/W}$

## Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the converter to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on EV02W0303A-3-Y-00A (51mmx51mm), 1oz, 2-layer PCB.
- 5) The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 3.3V$ ,  $V_{OUT} = 3.3V$ ,  $T_J = -40^{\circ}C$  to  $125^{\circ}C$  <sup>(6)</sup>, typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                     | Symbol             | Condition                                                                                                 | Min  | Typ  | Max  | Units            |
|-----------------------------------------------|--------------------|-----------------------------------------------------------------------------------------------------------|------|------|------|------------------|
| Under-voltage lockout (UVLO) rising threshold | $V_{UVLO\_RISING}$ |                                                                                                           | 2.4  | 2.61 | 2.8  | V                |
| UVLO hysteresis                               | $V_{UVLO\_HYS}$    |                                                                                                           |      | 190  |      | mV               |
| Input current                                 | $I_{IN}$           | Load = 0A                                                                                                 |      | 7    |      | mA               |
|                                               |                    | Load = 75mA                                                                                               |      | 150  |      | mA               |
| Output voltage ( $V_{OUT}$ ) accuracy         | $V_{OUT\_ACC}$     | $V_{IN} = 3V$ to $3.6V$ , load = 0A, $T_J = 25^{\circ}C$                                                  | 3.25 | 3.3  | 3.35 | V                |
|                                               |                    | $V_{IN} = 3V$ to $3.6V$ , load = 0A, $T_J = -40^{\circ}C$ to $+125^{\circ}C$                              | 3.23 | 3.3  | 3.37 | V                |
| Load regulation                               |                    | Load = 0mA to 75mA                                                                                        |      | 0.2  | 1.5  | %                |
| Line regulation                               |                    | Load = 75mA, $V_{IN} = 3V$ to $3.6V$                                                                      |      | 0.1  | 1.2  | %                |
| Efficiency                                    |                    | Load = 75mA                                                                                               |      | 50   |      | %                |
| Ripple                                        |                    | Load = 0mA to 75mA, $T_A = 25^{\circ}C$                                                                   |      | 40   | 80   | mV               |
| Capacitive load                               |                    | With 45Ω resistance load                                                                                  | 330  |      |      | μF               |
| Isolation voltage (MID02W0303AGY-2R)          | $V_{ISO\_2R}$      | $V_{TEST} = V_{ISO}$ for 60s (qualification),<br>$V_{TEST} = 1.2 \times V_{ISO}$ for 1s (100% production) | 1.5  |      |      | kV <sub>DC</sub> |
| Isolation voltage (MID02W0303AGY-3R)          | $V_{ISO\_3R}$      | $V_{TEST} = V_{ISO}$ for 60s (qualification),<br>$V_{TEST} = 1.2 \times V_{ISO}$ for 1s (100% production) | 3    |      |      | kV <sub>DC</sub> |
| Thermal shutdown <sup>(7)</sup>               | $T_{SD}$           |                                                                                                           |      | 160  |      | $^{\circ}C$      |
| Thermal shutdown hysteresis <sup>(7)</sup>    | $T_{SD\_HYS}$      |                                                                                                           |      | 20   |      | $^{\circ}C$      |

## PACKAGE PARAMETERS

| Parameter                                  | Symbol    | Condition                                                                                                                         | Min | Typ | Max | Units |
|--------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-------|
| Minimum external air gap (clearance)       | $L_{IO1}$ |                                                                                                                                   |     | 8   |     | mm    |
| Minimum external tracking (creepage)       | $L_{IO2}$ |                                                                                                                                   |     | 8   |     | mm    |
| Input to output capacitance <sup>(7)</sup> | $C_{I-O}$ | Measure as a 2-terminal device, pin 1 to pin 8 are shorted together, pin 9 to pin 16 are shorted together, $f_{sw} = 1MHz$        |     | 7   |     | pF    |
| Input to output resistance <sup>(7)</sup>  | $R_{I-O}$ | Measure as a 2-terminal device, pin 1 to pin 8 are shorted together, pin 9 to pin 16 are shorted together, $V_{TEST} = 500V_{DC}$ | 50  |     |     | GΩ    |

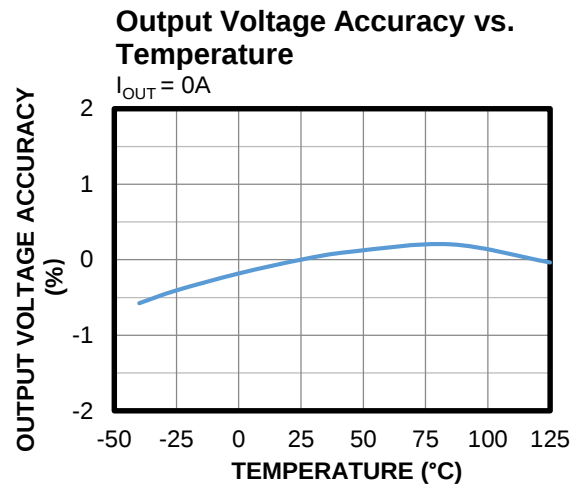
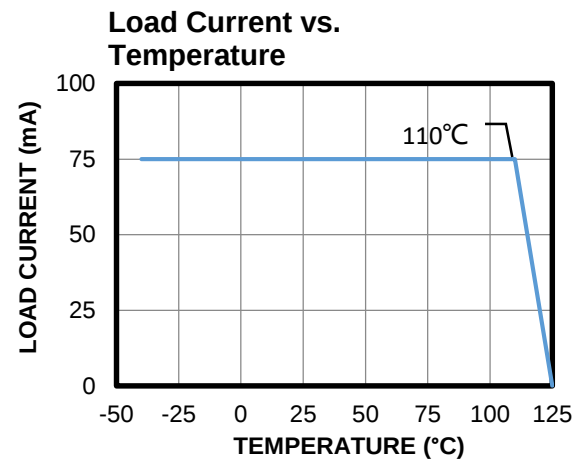
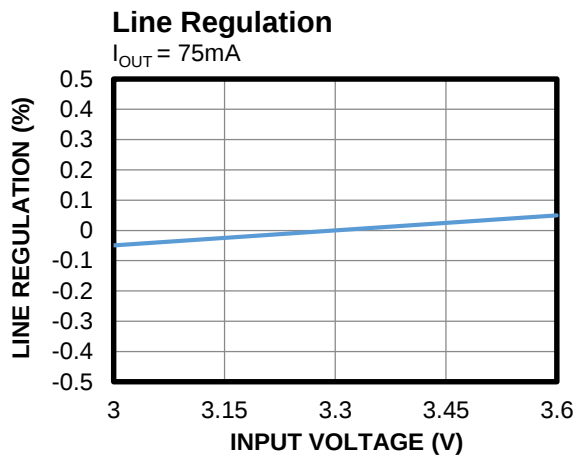
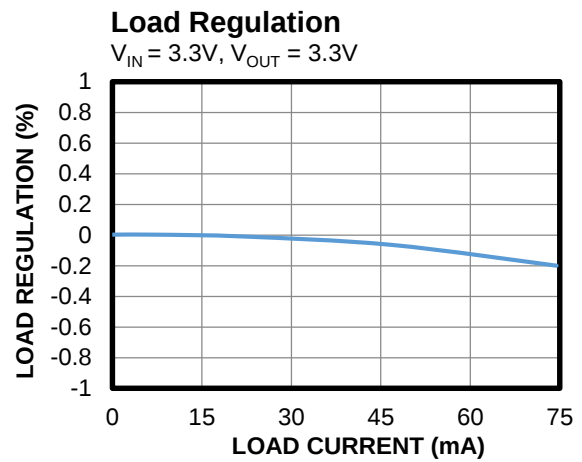
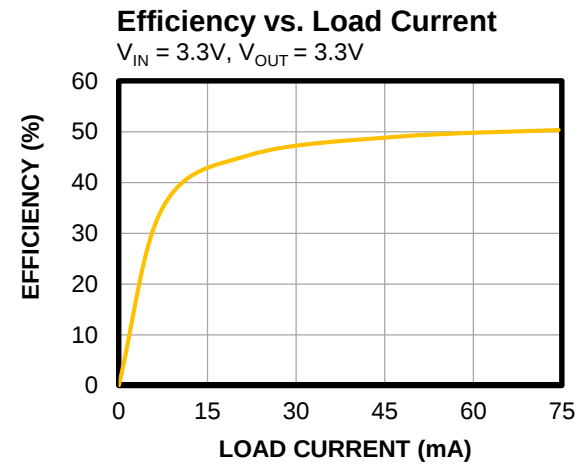
### Notes:

6) Guaranteed by over-temperature correlation. Not tested in production.

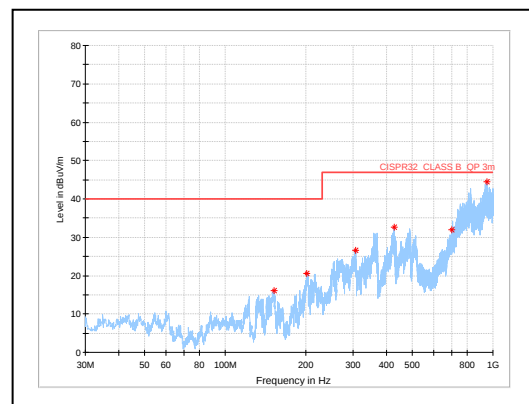
7) Guaranteed by sample characterization. Not tested in production.

# TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 3.3V$ ,  $V_{OUT} = 3.3V$ ,  $C_{IN} = C_{OUT} = 10\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.



**Radiated Emissions**  
30MHz to 1GHz, CISPR32 Class B <sup>(8)</sup>



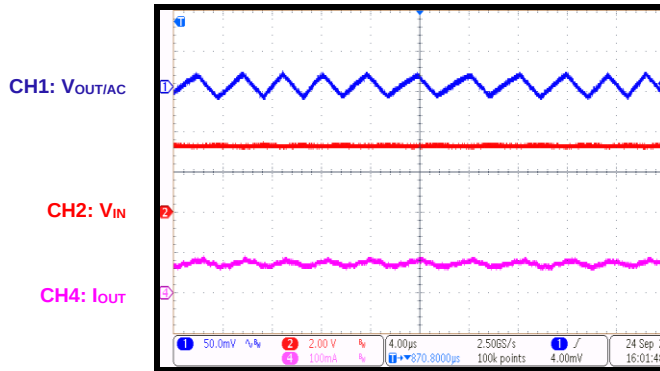
Note:

8) See Figure 2 on page 9 and Figure 3 on page 10 for details on the EMI circuit and PCB layout.

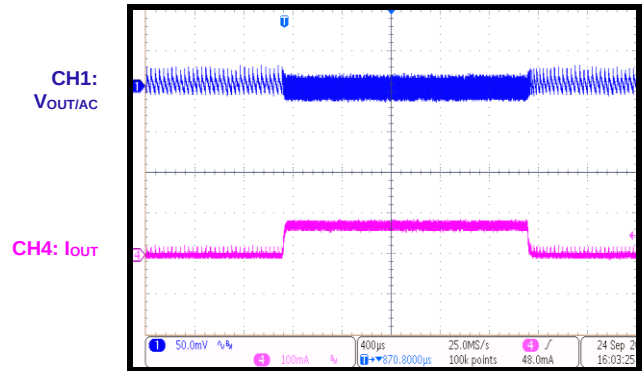
# TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board.  $V_{IN} = 3.3V$ ,  $V_{OUT} = 3.3V$ ,  $C_{IN} = C_{OUT} = 10\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

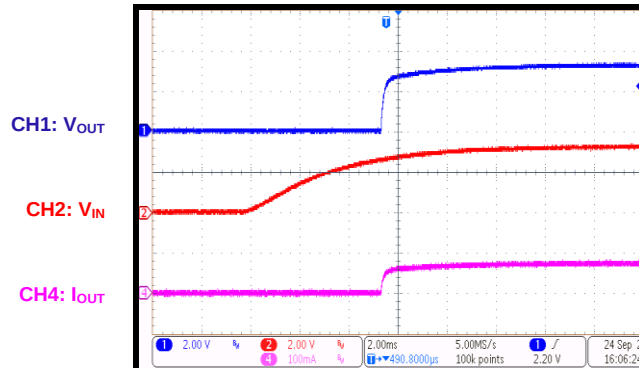
## $V_{OUT}$ Ripple

 $I_{OUT} = 75mA$ 


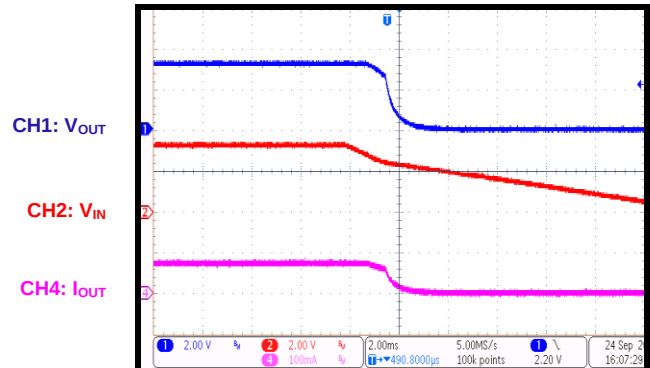
## Load Transient

 $I_{OUT} = 0mA$  to  $75mA$ 


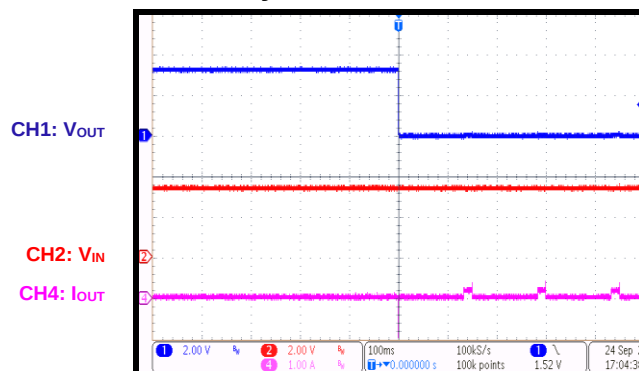
## Start-Up through $V_{IN}$

 $I_{OUT} = 75mA$ 


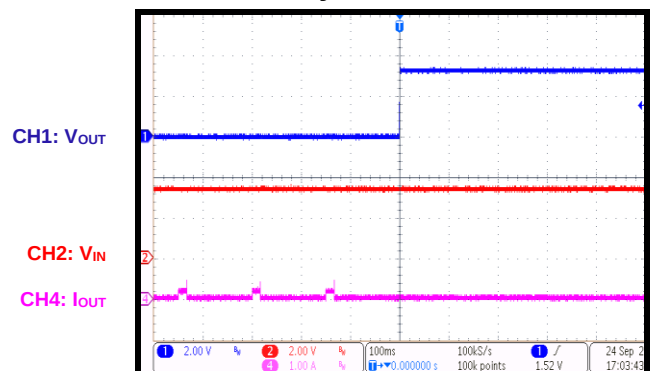
## Shutdown through $V_{IN}$

 $I_{OUT} = 75mA$ 


## SCP Entry



## SCP Recovery



# FUNCTIONAL BLOCK DIAGRAM

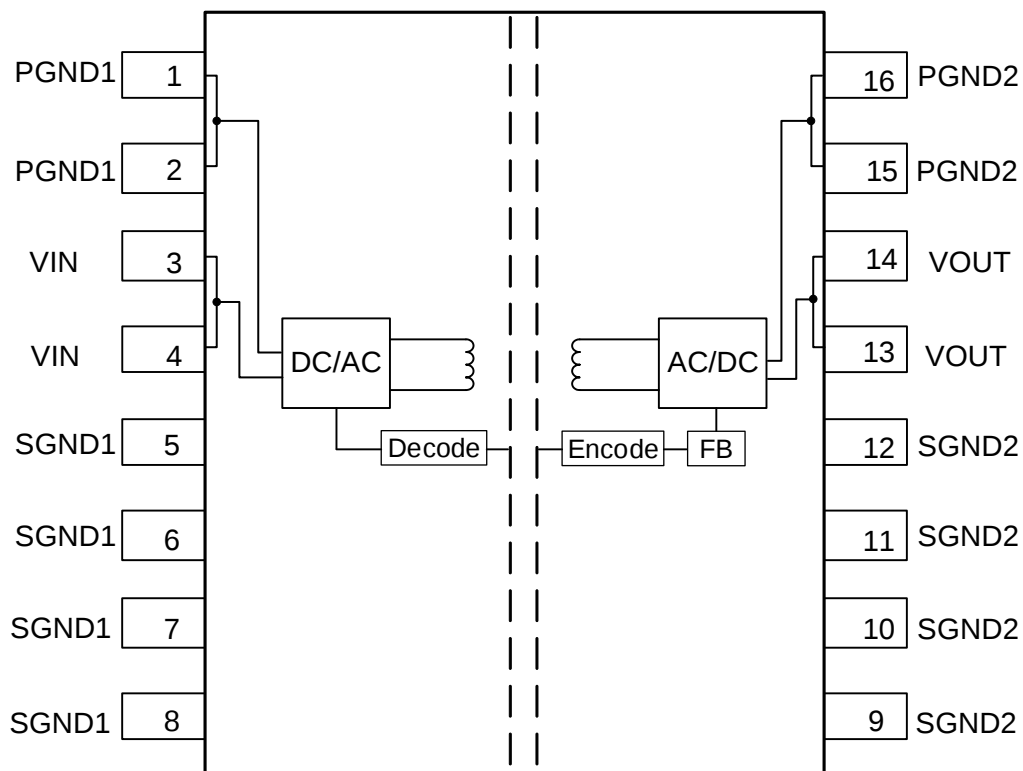


Figure 1: Functional Block Diagram

## OPERATION

The MID02W0303A is a regulated, isolated DC/DC converter that can support 3V to 3.6V input voltage ( $V_{IN}$ ) applications across a  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operating temperature range. It has excellent load regulation, line regulation, and supports up to 0.25W of output power ( $P_{OUT}$ ).

### Under-Voltage Lockout (UVLO) Protection

The MID02W0303A has input under-voltage lockout (UVLO) protection to ensure reliable  $P_{OUT}$ . The MID02W0303A starts up once  $V_{IN}$  exceeds the UVLO rising threshold. The device shuts down when  $V_{IN}$  drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. UVLO is a non-latch protection.

### Isolation Power Conversion

The MID02W0303A integrates a power MOSFET, transformer, and feedback (FB) circuit all in one chip, making it a high-performance, small-sized solution.

If  $V_{OUT}$  is below the target voltage, the IC starts switching to deliver power from  $V_{IN}$  to  $V_{OUT}$ . If  $V_{OUT}$  exceeds the target voltage, the device stops switching.

### Power Converter Soft Start (SS) and Short-Circuit Protection (SCP)

To avoid overshoot and inrush current during start-up, the MID02W0303A has built-in internal soft start (SS) that gradually ramps up the output current ( $I_{OUT}$ ).

The soft-start time ( $t_{SS}$ ) is internally set to about 15ms. If  $V_{OUT}$  does not exceed 2.61V after  $t_{SS}$  due to a short circuit or large capacitive load, the MID02W0303A enters in hiccup mode. The hiccup mode off time ( $t_{OFF}$ ) is about 150ms. After the hiccup mode  $t_{OFF}$ , the MID02W0303A initiates another SS. If the short circuit is removed, then the MID02W0303A resumes normal operation.

### Thermal Protection

The MID02W0303A monitors the IC temperature internally. If the die temperature exceeds  $160^{\circ}\text{C}$ , the driver outputs are disabled. Once the junction temperature ( $T_J$ ) drops to  $140^{\circ}\text{C}$ , the driver outputs are enabled again and the device resumes normal operation.

## APPLICATION INFORMATION

### Selecting the Input and Output Capacitors

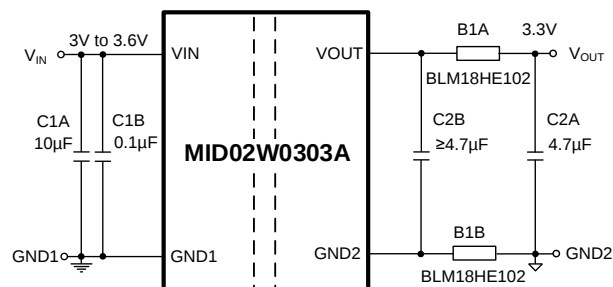
For stable operation, connect a decoupling capacitor between the VIN and PGND1 pins at the input side, and one between the VOUT and PGND2 pins at the output side. Place these decoupling capacitors as close to VIN and VOUT as possible.

### EMI Optimization

There are two main techniques used for PCB layout. Figure 2 and Figure 3 on page 10 show examples of layouts that are CISPR 32 Class B certified. The first technique to reduce EMI is to build a low-ESL Y-capacitor using a 4-layer PCB layout to filter high-frequency noise on the secondary side. The Y-capacitor is formed with the two overlapping middle layers. Mid-layer 1 is the PGND1 copper plane, which forms the Y-capacitor's top plate. Mid-layer 2 is the ground after the ferrite bead (GND2), which forms the Y-capacitor's bottom plate. More overlap in these layers provides a larger Y-capacitor value, which further reduces EMI. The second technique to reduce EMI is to use stitching vias

on the GND planes to suppress electromagnetic transmissions.

Aside from the two PCB layout techniques described above, a pair of ferrite beads are required to form a CLC structure filter (see Figure 2). Place this filter as close to VOUT and PGND2 as possible. The capacitor closest to the IC (C2B) should be  $\geq 4.7\mu\text{F}$  to ensure a stable output. Do not place large copper areas on the secondary side pins, as this can increase switching noise and EMI. Connect SGND2 and PGND2 using a thin trace.

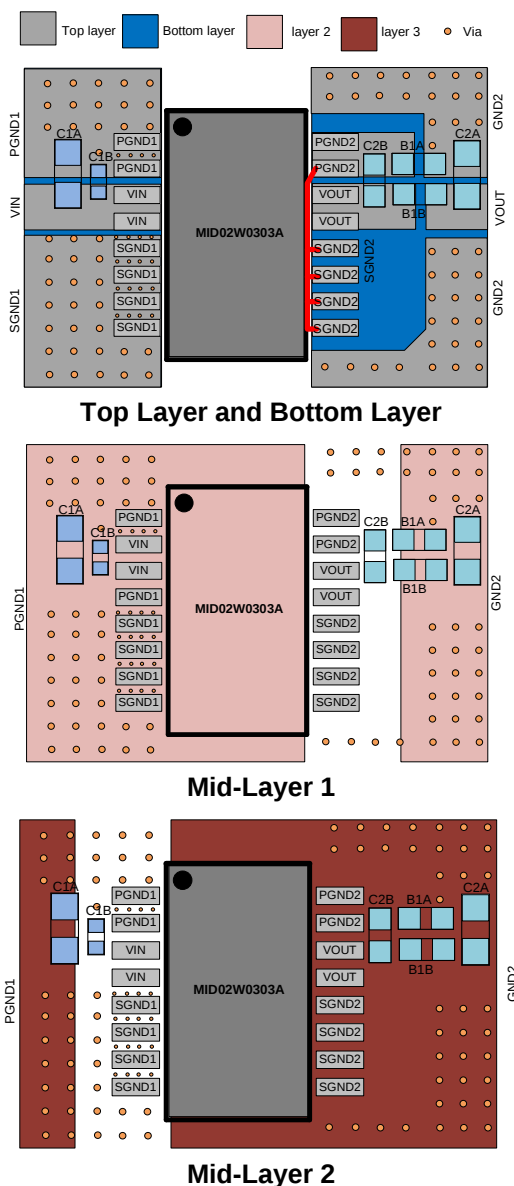


**Figure 2: Recommended EMI Schematic**

## PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. For safety, the primary side and secondary side should be physically separated. Ensure that the creepage/clearance meets the standards for the specified application.
2. To reduce output noise, minimize the loop area between VIN, the input capacitor, and PGND1, as well as VOUT, the output capacitor, and PGND2.
3. Place enough copper and vias around the IC's primary pin output to improve thermal performance.
4. Connect SGND1 and PGND1 using large copper traces and multiple vias to improve thermal dissipation.
5. Connect SGND2 and PGND2 using a thin trace (below the red trace in Figure 3) to reduce radiation.



**Figure 3: Recommended PCB Layout**

## TYPICAL APPLICATION CIRCUIT

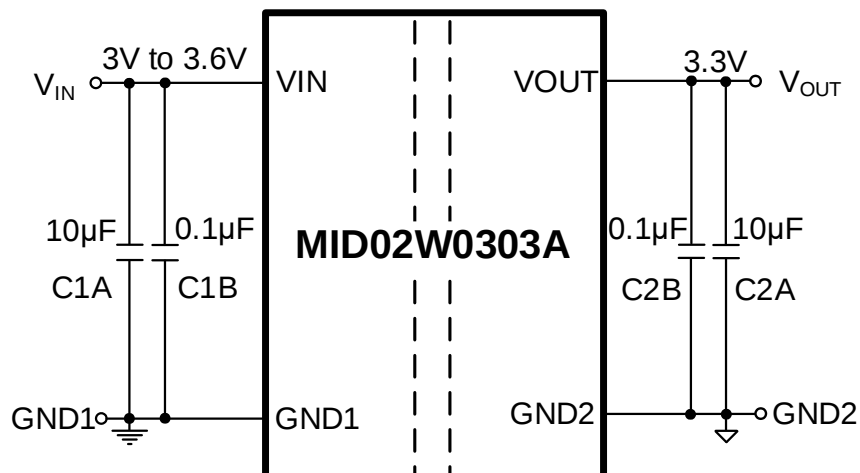
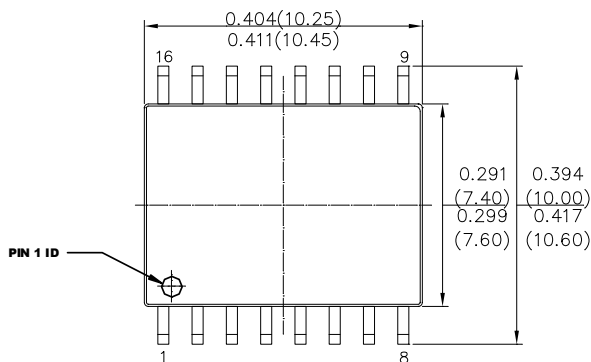


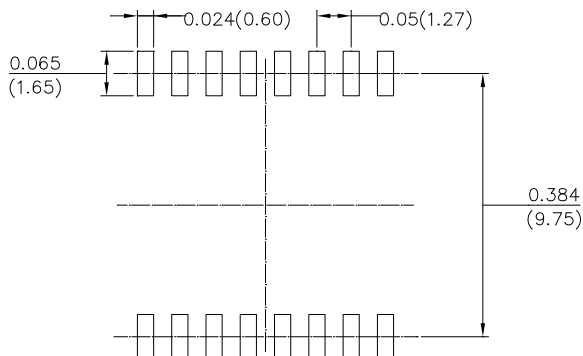
Figure 4: Typical Application Circuit

# PACKAGE INFORMATION

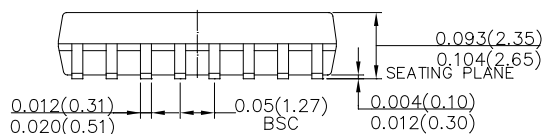
## SOICW-16



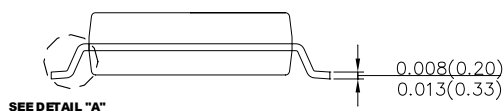
**TOP VIEW**



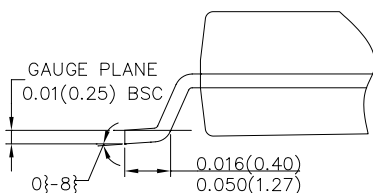
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**

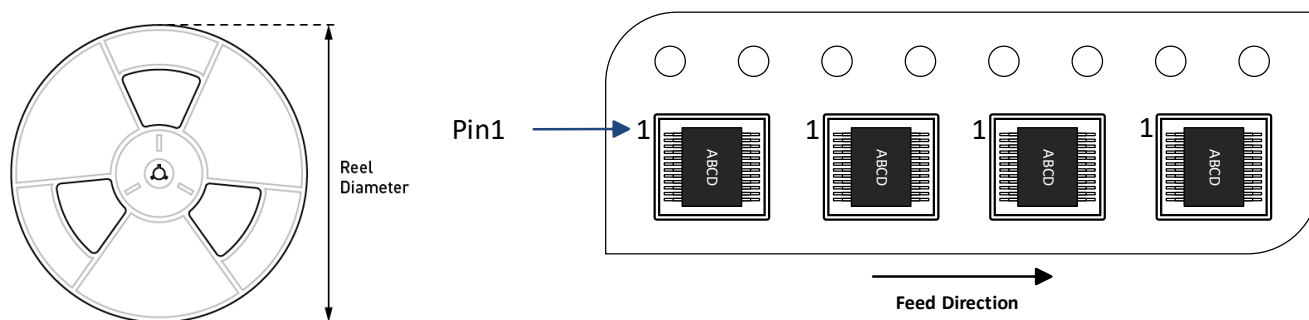


**DETAIL "A"**

### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION



| Part Number        | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|--------------------|---------------------|----------------|----------------|----------------|---------------|--------------------|--------------------|
| MID02W0303AGY-2R-Z | SOICW-16            | 1000           | 44             | N/A            | 13in          | 24mm               | 12mm               |
| MID02W0303AGY-3R-Z |                     |                |                |                |               |                    |                    |

## REVISION HISTORY

| Revision # | Revision Date | Description     | Pages Updated |
|------------|---------------|-----------------|---------------|
| 1.0        | 2/10/2023     | Initial Release | -             |

**Notice:** The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third-party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.