



MP2643

Integrated, 2A, Bidirectional Active Balancer

DESCRIPTION

The MP2643 is a highly integrated, bidirectional active balancer that provides up to 2A of charge redistribution among Li-ion, Li-polymer, or lithium iron phosphate batteries in a two-series battery pack. As an alternative to dissipating energy with passive balancing, the MP2643 efficiently moves charge between cells to minimize balancing time and heat generation. The device can also compensate for cell capacity mismatch to extend battery runtime.

By combining multiple MP2643 devices, active balancing can be scaled to any number of series cells, and charge can be redistributed to and from any cells within the pack.

The MP2643 can balance adjacent cells using two modes: buck-balance mode and boost-balance mode. In buck-balance mode, the MP2643 transfers energy from the upper cell (CU) to the lower cell (CL). In boost-balance mode, the MP2643 transfers energy from CL to CU.

To guarantee safe operation, the MP2643 provides CL and CU over-voltage protection (OVP), under-voltage protection (UVP), and thermal shutdown.

The MP2643 is available in a QFN-26 (4mmx4mm) package.

FEATURES

- Wide Operating Voltage Range Compatible with LiFePO4 Batteries:
 - 2.4V Minimum Cell Voltage
 - 4.35V Maximum Cell Voltage
- Low Quiescent Current (I_Q):
 - CU Pin: 12 μ A I_Q
 - CL Pin: 0.1 μ A I_Q
- Buck-Balance Mode:
 - Net Transfer Current to Lower Cell
 - Configurable between 0.5A and 2A
- Boost-Balance Mode:
 - Net Transfer Current to Upper Cell
 - Configurable between 0.5A and 2A
- Protections:
 - Thermal Shutdown
 - Internal CL Port Battery Reverse Leakage Blocking
 - Integrated CU Low Voltage Protection in Boost-Balance Mode
- Directly Powered from the Battery Cells
- Interleavable for Transfer across Many Cells
- Available in a QFN-26 (4mmx4mm) Package

APPLICATIONS

- Grid-Level Energy Storage Systems (ESS)
- Residential ESS
- Battery Backup Systems
- Material Handling Equipment

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TYPICAL APPLICATION

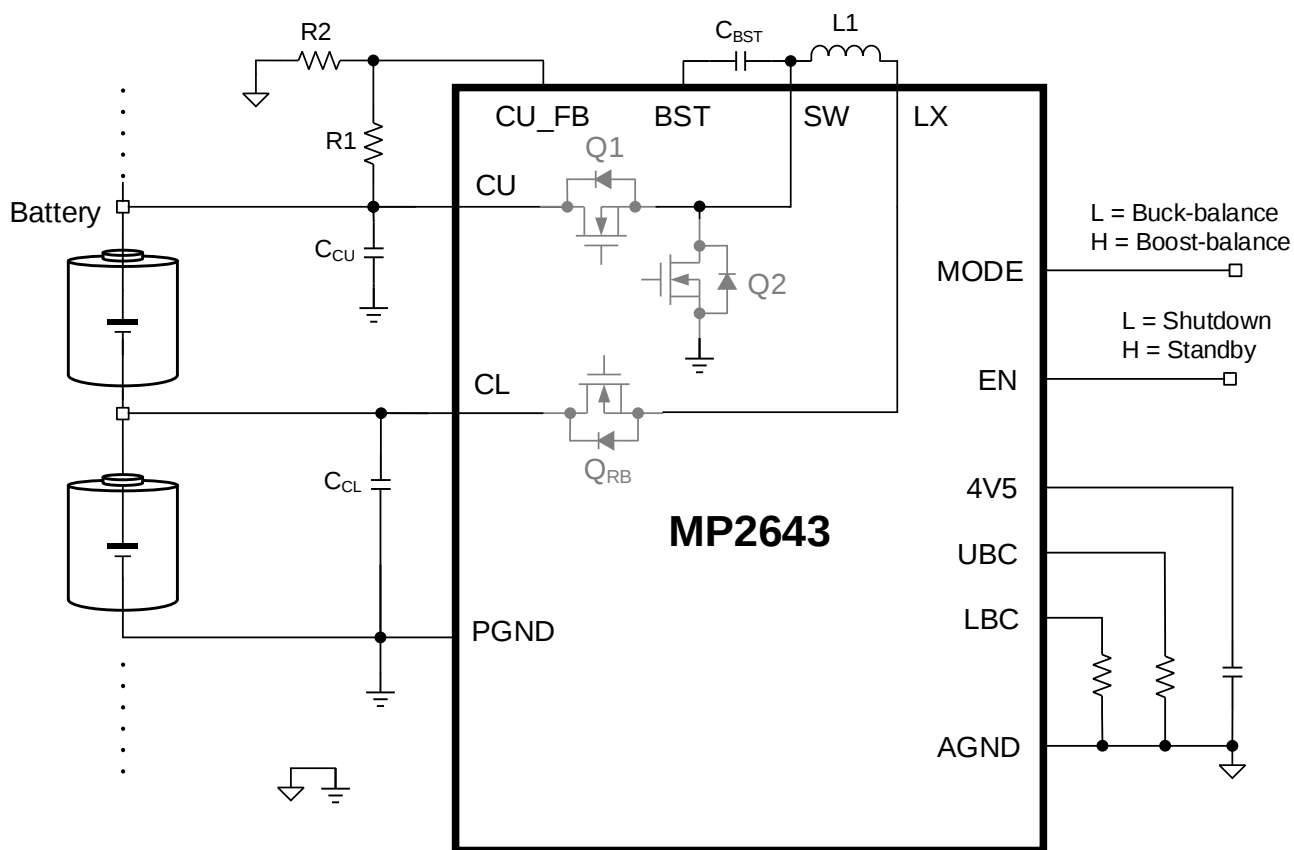


Table 1: Mode Selection for Cell Balancing

MODE Pin	Mode	Active SW	Topology
High	Boost-balance mode	Q2	Step-up
Low	Buck-balance mode	Q1	Step-down

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2643GR	QFN-26 (4mmx4mm)	See Below	1

* For Tape & Reel, add suffix -Z (e.g. MP2643GR-Z).

TOP MARKING

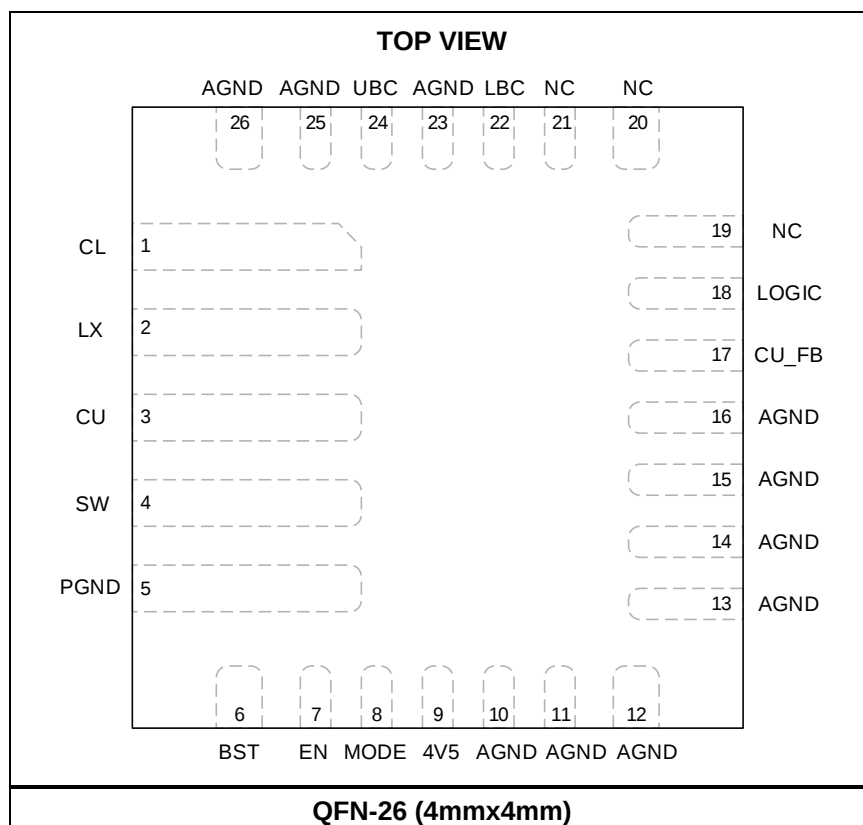
MPSYWW

MP2643

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2643: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	CL	Positive terminal of the lower battery cell. Connect the CL pin to the positive terminal of the lower battery cell in the two-series battery pack.
2	LX	Connection node between the inductor and the internal block switch.
3	CU	Positive terminal of the upper battery cell. Connect the CU pin to the positive terminal of the upper battery cell in the two-series battery pack.
4	SW	Switching node.
5	PGND	Power ground. Connect the PGND pin to the negative port of the lower cell battery.
6	BST	Bootstrap. Connect a BST capacitor (C_{BST}) between the BST pin and SW node.
7	EN	IC enable. The EN pin is low by default. If EN is pulled low, the IC is in sleep mode where the quiescent current (I_Q) at the CU and CL terminals are very small; the MODE state does not change the chip's sleep mode. If EN is pulled high, the IC is in standby mode, and the chip enters different modes depending on the MODE state.
8	MODE	Balance mode selection. Pull the MODE pin logic low to make the MP2643 work in buck-balance mode; pull MODE logic high to make the MP2643 work in boost-balance mode.
9	4V5	Internal circuit power supply. Bypass the 4V5 pin to AGND (pin 10) via a 1 μ F ceramic capacitor. 4V5 can be used for pull-up logic on the MP2643. This pin is not intended to carry other external loads. 4V5 outputs only when EN is high.
10, 11, 12, 13, 14, 15, 16, 23, 25, 26	AGND	Analog ground.
17	CU_FB	CU voltage feedback in boost-balance mode. Set the maximum CU pin voltage (V_{CU}) via resistor divider connected between the CU_FB and AGND pins.
18	LOGIC	Internal circuit power logic. Short the LOGIC pin directly to 4V5.
19, 20, 21	NC	Not connected. Float the NC pins.
22	LBC	Boost-balance current setting. Connect an external resistor between the LBC and AGND pins to configure the lower battery cell's balance current.
24	UBC	Buck-balance current setting. Connect an external resistor between the UBC and AGND pins to configure the upper battery cell's balance current.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

CU.....	-0.3V to +20V
SW	-0.3V (-2V for 50ns) to +20V
CL	-0.3V to +5.5V
BST to SW.....	-0.3V to +5.5V
All other pins to AGND.....	-0.3V to +5.5V
Continuous power dissipation	(T _A = 25°C) ⁽²⁾
.....	2.97W
Junction temperature (T _J)	150°C
Lead temperature (solder)	260°C
Storage temperature.....	-65°C to +150°C

ESD Ratings

Human body model (HBM)	2kV
Charged-device model (CDM)	2kV

Recommended Operating Conditions ⁽³⁾

CU to PGND.....	3.9V to 16V
CL to PGND	2.4V to 4.5V
Operating junction temp (T _J)	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
QFN-26 (4mmx4mm).....	42	9.... °C/W

Notes:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Internal Characteristics						
4V5 voltage	V _{4V5}	V _{CU} = 5V, V _{CL} = 2.1V	4.4	4.5	4.6	V
High-side (HS) N-channel MOSFET on resistance	R _{DS(ON)_Q1}	T _A = 25° C		17	35	mΩ
Low-side (LS) N-channel MOSFET on resistance	R _{DS(ON)_Q2}	T _A = 25°C		25	35	mΩ
Reverse blocking N-channel MOSFET on resistance	R _{DS(ON)_RB}	T _A = 25°C		12	15	mΩ
Peak current limit for HS N-channel MOSFET	I _{HS_PK}	Buck-balance mode, V _{CL} = 3V	6.7	8		A
Peak current limit for LS N-channel MOSFET	I _{LS_PK}	Boost-balance mode	7.6	9.2		A
Operating frequency	f _{SW}		900	1080	1200	kHz
Thermal shutdown threshold ⁽⁵⁾	T _{J_SHDN}			155		°C
Thermal shutdown hysteresis ⁽⁵⁾				18		°C
CU quiescent current		V _{CL} = 3.6V, V _{CU} = 7.2V, EN = low		12	15	μA
CL quiescent current		V _{CL} = 3.6V, V _{CU} = 7.2V, EN = low			0.4	μA
CU under-voltage lockout (UVLO) threshold	V _{CU_UVLO}	V _{CU} falling	3.5	3.8	4.1	V
CU UVLO threshold hysteresis		V _{CU} rising		300		mV
Buck-Balance Mode						
Buck-balance current range ⁽⁵⁾			0.5		2	A
Buck-balance current ⁽⁶⁾	I _{UBC}	R _{UBC} = 430kΩ	0.45	0.5	0.55	A
		R _{UBC} = 215kΩ	0.9	1	1.1	A
		R _{UBC} = 107kΩ	1.82	2	2.18	A
CL voltage limit	V _{CL_LIM}			4.35		V
CL over-voltage protection (OVP) threshold	V _{CL_OVP}			4.60	4.90	V
CL OVP recovery hysteresis				125	155	mV
Boost-Balance Mode						
CU voltage limit reference	V _{CU_LIM_REF}		1.18	1.2	1.22	V
CU voltage limit ^{(5) (6)}	V _{CU_LIM}	R1 = 2MΩ (1%), R2 = 402kΩ (1%)	6.93	7.17	7.41	V
CU voltage limit feedback input current	I _{FB_LKG}	Sink into the CU_FB pin			420	nA
CU OVP threshold reference	V _{CU_OVP_REFBST}	V _{CU_LIM} < 7V		1.41		V
		V _{CU_LIM} > 7V		1.35		V
CU OVP threshold reference hysteresis				32		mV

ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
CU OVP threshold ⁽⁵⁾ ⁽⁶⁾	V _{CU_OVP}	V _{CU_LIM} = 7.17V, V _{CU_OVP_REFBST} = 1.35V, R1 = 2MΩ (1%), R2 = 402kΩ (1%)	7.8	8.07	8.33	V
		V _{CU_LIM} = 6.78V, V _{CU_OVP_REFBST} = 1.41V, R1 = 2MΩ (1%), R2 = 430kΩ (1%)	7.7	7.97	8.23	V
CU OVP threshold hysteresis ⁽⁵⁾ ⁽⁶⁾		V _{CU_LIM} = 7.17V, R1 = 2MΩ (1%), R2 = 402kΩ (1%)		191		mV
		V _{CU_LIM} = 6.78V, R1 = 2MΩ (1%), R2 = 430kΩ (1%)		180		mV
Boost-balance current range ⁽⁵⁾			0.5		2	A
Boost-balance current ⁽⁶⁾	I _{LBC}	V _{CL} = 3.6V, V _{CU} = 7.2V, R _{LBC} = 536kΩ	0.46	0.5	0.54	A
		V _{CL} = 3.6V, V _{CU} = 7.2V, R _{LBC} = 267kΩ	0.92	1	1.08	A
		V _{CL} = 3.6V, V _{CU} = 7.2V, R _{LBC} = 133kΩ	1.85	2	2.15	A
Lower battery cell UVLO threshold	V _{CL_UVLO}	V _{CL} falling when boost-balance operating		2.1		V
		V _{CL} rising before boost-balance starts		2.4		V
Logic I/O Pin Characteristics						
EN and MODE input logic low voltage					0.4	V
EN and MODE input logic high voltage			1			V

Notes:

5) Guaranteed by design.

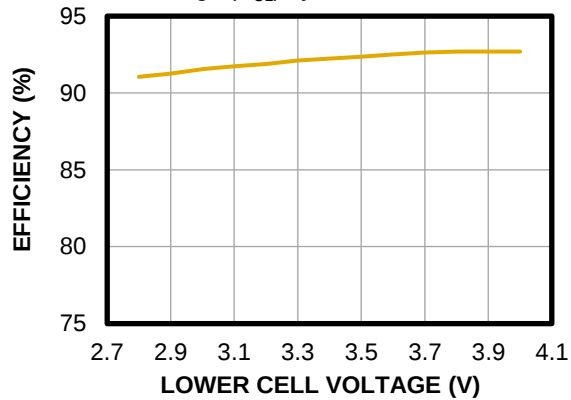
6) Calculated result. Not tested in production.

TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $C_{CL} = 22\mu\text{F}$, $C_{CU} = 22\mu\text{F}$, $L = 1.5\mu\text{H}$ (DCR = $10\text{m}\Omega$), $R_{UBC} = 107\text{k}\Omega$, $R_{LBC} = 130\text{k}\Omega$, unless otherwise noted.

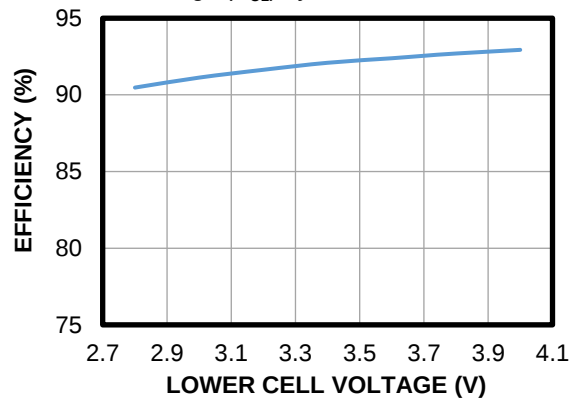
Buck-Balance Efficiency

The upper cell voltage exceeds the lower cell voltage (V_{CL}) by 0.2V



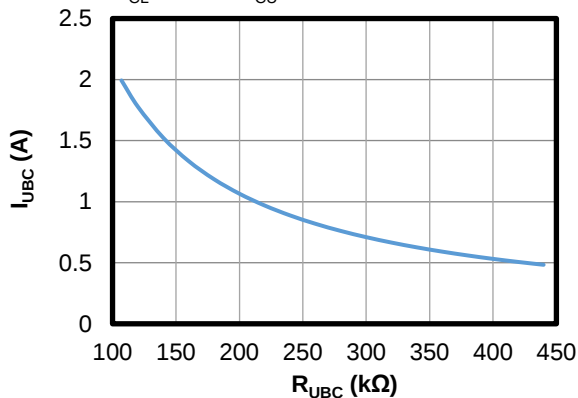
Boost-Balance Efficiency

The upper cell voltage is below the lower cell voltage (V_{CL}) by 0.2V



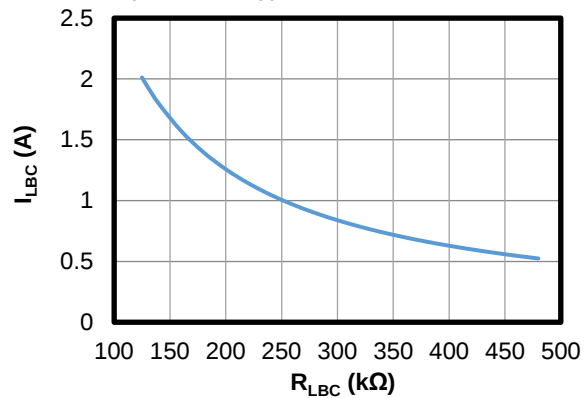
Buck-Balance Current

$V_{CL} = 3.3\text{V}$, $V_{CU} = 6.8\text{V}$



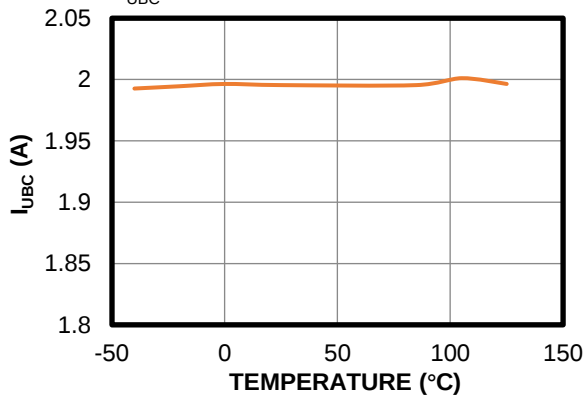
Boost-Balance Current

$V_{CL} = 3.3\text{V}$, $V_{CU} = 6.4\text{V}$



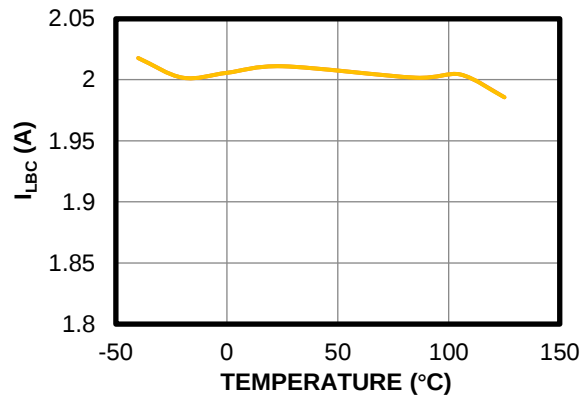
Buck-Balance Current vs. Temperature

$R_{UBC} = 107\text{k}\Omega$



Boost-Balance Current vs. Temperature

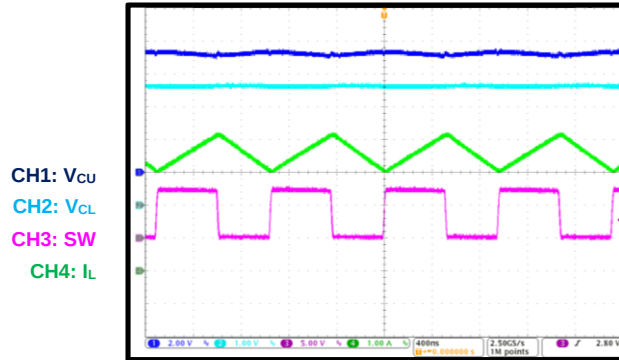
$R_{LBC} = 133\text{k}\Omega$, $V_{CL} = 3.6\text{V}$, $V_{CU} = 7.2\text{V}$



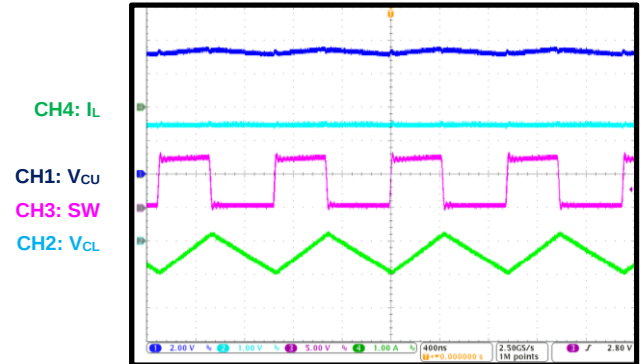
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CU} = 7.2V$, $V_{CL} = 3.6V$, $R_{UBC} = 107k\Omega$, $R_{LBC} = 107k\Omega$, $R_1 = 2M\Omega$, $R_2 = 392k\Omega$, $L = 1.5\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

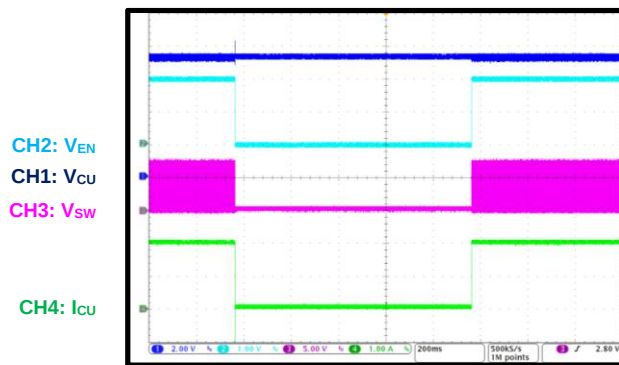
Buck-Balance Steady Operation



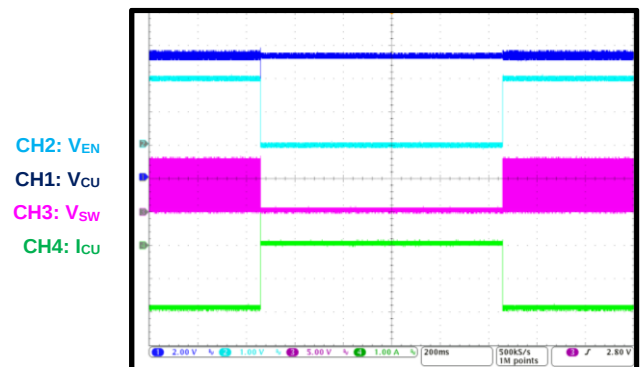
Boost-Balance Steady Operation



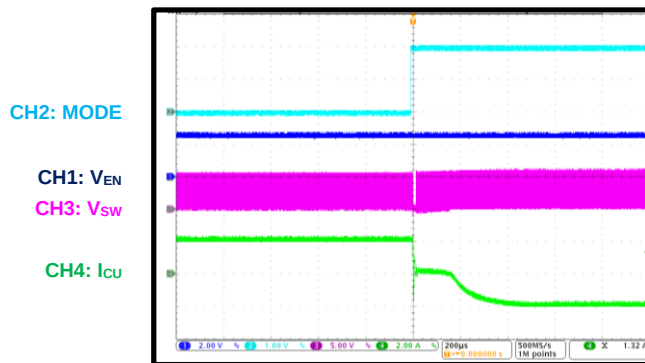
Buck-Balance Enable/Disable via EN



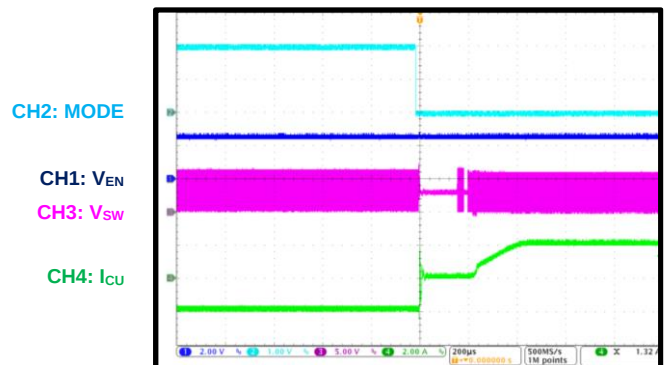
Boost-Balance Enable/Disable via EN



Transient from Buck-Balance to Boost-Balance via MODE



Transient from Boost-Balance to Buck-Balance via MODE



FUNCTIONAL BLOCK DIAGRAM

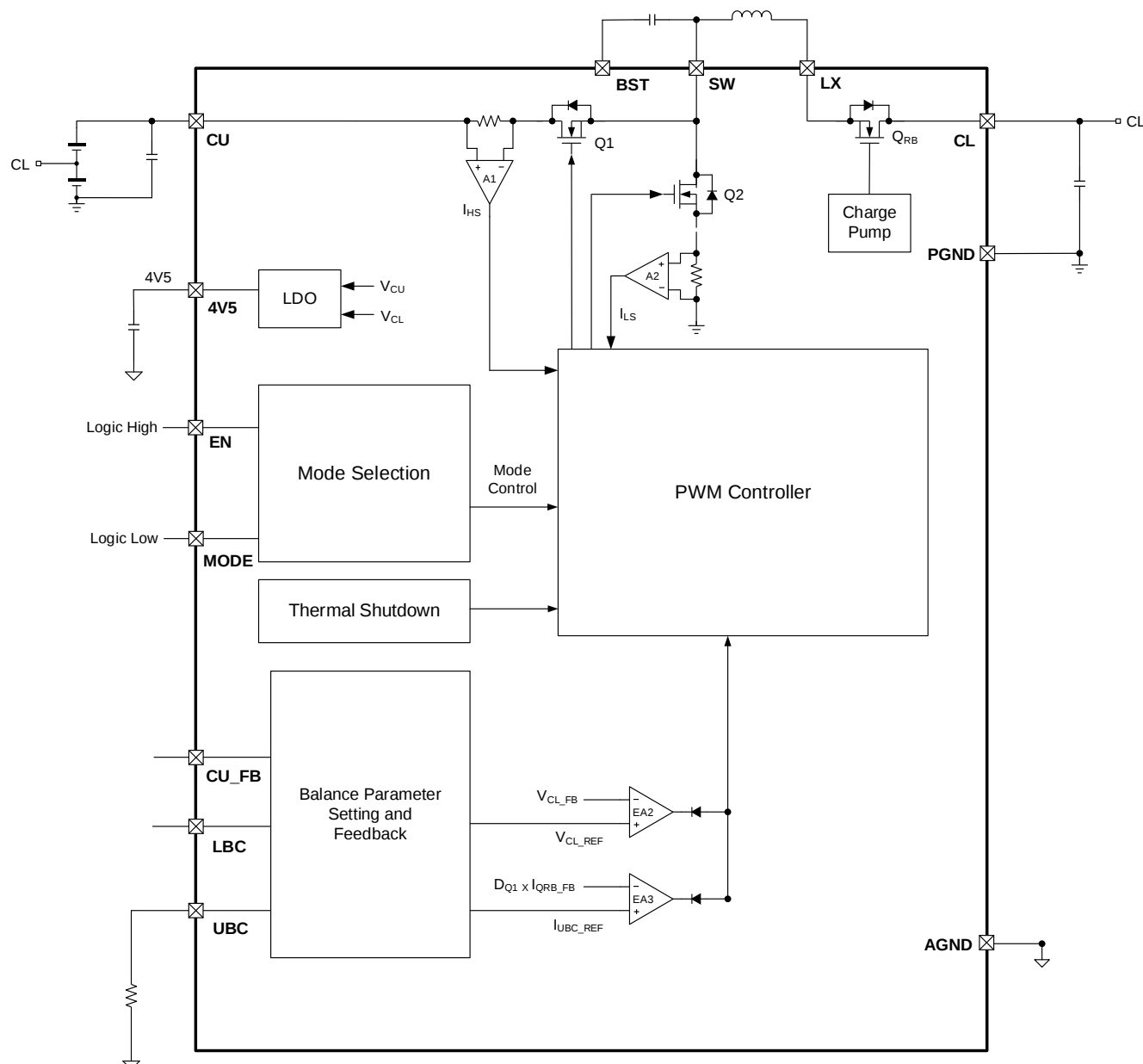


Figure 1: Functional Block Diagram for Buck-Balance

FUNCTIONAL BLOCK DIAGRAM (continued)

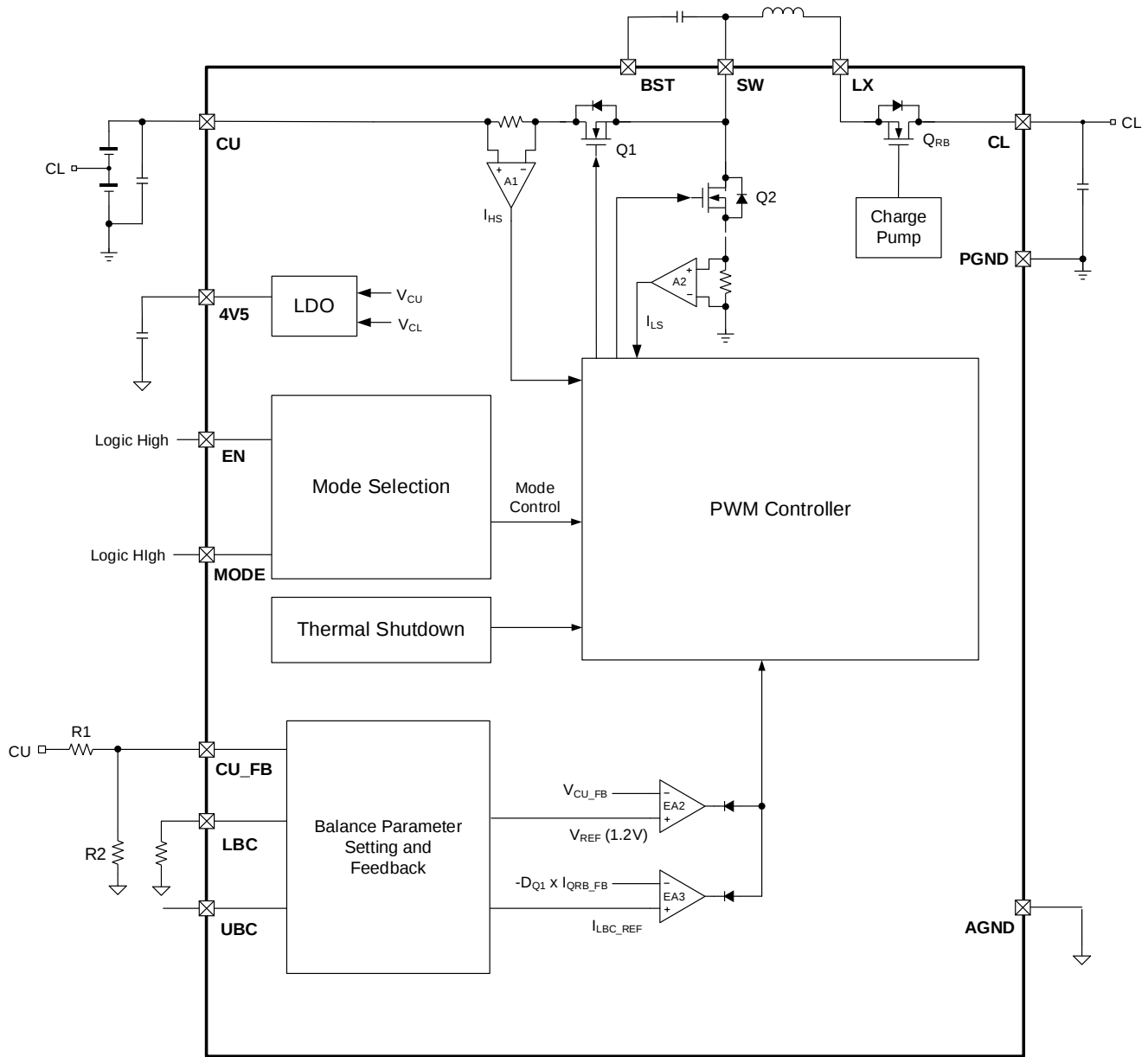


Figure 2: Functional Block Diagram for Boost-Balance

OPERATION

Introduction

The MP2643 is a highly integrated active balancer designed to transfer charge between two adjacent battery cells for the purpose of balancing the cells. By interleaving these devices, charge can be transferred across many cells in series.

Balance Direction Selection

Buck-balance mode transfers charge from the upper cell to the lower cell. In this mode, the MP2643 extracts power from both series cells and delivers this power to the lower cell. The net current delivered to the lower cell is about equal to the upper balancing current, which is also the buck-balance current (I_{UBC}) (see Figure 3).

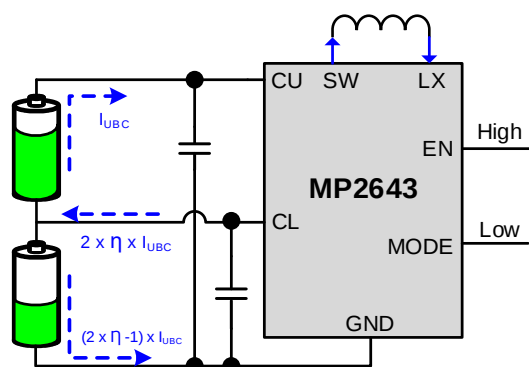


Figure 3: Buck-Balance Mode

The net current calculation assumes that both cell voltages are the same, meaning the net transfer current differs from I_{UBC} by only the buck converter efficiency (η).

Buck-balance is initiated when the part is enabled by pulling the EN pin high while the MODE pin is pulled low internally.

Boost-balance mode transfers charge from the lower cell to the upper cell. In this mode, the MP2643 extracts power from the lower cell and delivers this power to both series cells. The net current delivered to the upper cell is about equal to the lower balancing current, which is also the boost-balance current (I_{LBC}) (see Figure 4).

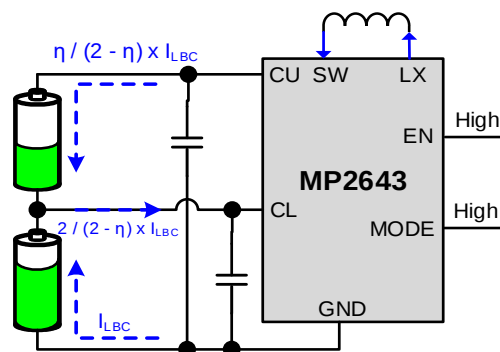


Figure 4: Boost-Balance Mode

The net current calculation assumes that both cell voltages are the same, meaning the net transfer current differs from I_{LBC} by only the boost converter efficiency (η).

Boost-balance is initiated when the part is enabled by pulling EN high while MODE is pulled high.

Internal Power Supply

The MP2643 provides a low-dropout (LDO) regulator (4V5) for the internal circuitry and the MOSFET driver. The LDO regulator only operates while the part is enabled (EN is high). Connect a 1 μ F ceramic capacitor between the 4V5 and AGND pins. 4V5 must be connected to the LOGIC pin, and it can pull up the MODE pin. Otherwise, it is not recommended to use the 4V5 pin for any external loads.

BUCK-BALANCE MODE

To enable buck-balance mode, pull EN high while MODE is low. Buck-balancing begins if the following conditions are met:

1. EN is high, and MODE is low
2. $19.5V > V_{CU} > V_{CU_UVLO}$
3. $V_{CU} > V_{CL} + 400mV$
4. $V_{CL} < V_{CL_OVP}$
5. No fault occurs

Buck-Balance Current Setting

I_{UBC} is configured via a resistor (R_{UBC}) connected between the UBC and AGND pins. I_{UBC} can be calculated with Equation (1):

$$I_{UBC} = \frac{640}{3 \times R_{UBC}} \quad (1)$$

Where I_{UBC} is in A, and R_{UBC} is in k Ω .

I_{UBC} should be limited to a maximum of 2A.

CL Voltage Limit Setting

The MP2643 includes a built-in lower cell voltage limit (V_{CL_LIM}) (4.35V). During buck-balancing, when the CL voltage (V_{CL}) rises to this limit, the MP2643 gradually reduces the balance current to avoid exceeding the voltage limit. If the lower cell voltage (V_{CL_OVP}) exceeds 4.6V, then the MP2643 suspends buck-balance immediately.

BOOST-BALANCE MODE

To enable boost-balance mode, pull EN high while MODE is high. Boost-balancing begins if the following conditions are met:

1. EN is high, and MODE is high
2. $V_{CU_OVP} > V_{CU} > V_{CU_UVLO}$
3. $V_{CL} > V_{CL_UVLO}$
4. No fault occurs

Boost-Balance Current Setting

In boost-balance mode, I_{LBC} is configured via an external resistor (R_{LBC}) connected from the LBC pin to AGND. I_{LBC} can be calculated with Equation (2):

$$I_{LBC} = \frac{V_{CU} - \eta \times V_{CL}}{\eta \times V_{CL}} \times \frac{640}{3 \times R_{LBC}} \quad (A) \quad (2)$$

Where R_{LBC} is in k Ω , η is the boost-balance efficiency, V_{CL} is the lower cell voltage (between CL and AGND), and V_{CU} is the voltage of both series cells (between CU and AGND). V_{CL} and V_{CU} are measured without balancing enabled.

To determine R_{LBC} , the boost-balance efficiency (η) must be estimated first, which depends on the cell voltage. Table 2 shows the efficiency selection.

Table 2: Boost-Balance Efficiency Selection

V_{CL} (V)	η
<3.65V	0.89
$\geq 3.65V$	0.91

Since I_{LBC} is dependent on V_{CL} and V_{CU} , any changes in V_{CL} and V_{CU} during boost-balance impact I_{LBC} .

I_{LBC} can be configured to a maximum of 2A.

CU Voltage Limit Setting in Boost-Balance Mode

The MP2643 provides a resistor-configurable voltage limit on V_{CU} (V_{CU_LIM} and V_{CU_OVP}). When V_{CU} reaches V_{CU_LIM} , the MP2643 holds the boost voltage by adjusting the boost regulator duty cycle. If V_{CU} exceeds V_{CU_OVP} , the MP2643 disables the boost balance and turns off the reverse block FET (Q_{RB}). When V_{CU} returns to a safe level, boost-balance restarts.

V_{CU_LIM} and V_{CU_OVP} are set by the voltage divider connected between the CU, CU_FB, and PGND pins. V_{CU_LIM} can be calculated with Equation (3):

$$V_{CU_LIM} = V_{CU_LIM_REF} \times \frac{R1+R2}{R2} \quad (V) \quad (3)$$

Where $V_{CU_LIM_REF}$ is the reference of V_{CU} (1.2V).

V_{CU_OVP} can be calculated with Equation (4):

$$V_{CU_OVP} = V_{CU_OVP_REFBST} \times \frac{R1+R2}{R2} \quad (V) \quad (4)$$

Where the CU over-voltage protection (OVP) threshold reference ($V_{CU_OVP_REFBST}$) is the reference of the output OVP threshold comparator, and its value depends on the V_{CU_LIM} setting (see $V_{CU_OVP_REFBST}$ in the Electrical Characteristics section on page 6).

APPLICATION INFORMATION

Setting the Buck-Balance Current

The MP2643's I_{UBC} can be configured between 0.5A and 2A via R_{UBC} connected between the UBC and AGND pins. By rewriting Equation (1) on page 13, R_{UBC} for a desired I_{UBC} can be calculated with Equation (5):

$$R_{UBC} = \frac{640}{3 \times I_{UBC}} (k\Omega) \quad (5)$$

Using this calculated R_{UBC} , the closest available resistance should be selected.

Determining the Buck-Balance Current Range

Consider an example where R_{UBC} is calculated for a target I_{UBC} , as well as the I_{UBC} minimum and maximum range based on ΔR and ΔI_{UBC} . If $V_{CU} = 7V$ and $V_{CL} = 3.6V$, using Equation (5), R_{UBC} for 2A is 106.6k Ω . Using a 1% resistor tolerance, the closest standard resistance is 107k Ω . With $\Delta I_{UBC} = 10\%$ and $\Delta R = 1\%$, Table 3 shows the I_{UBC} range between 1.78A and 2.22A, with a typical value at the target 2A.

Table 3: I_{UBC} Range When Setting I_{UBC_TYP}

Parameter	R_{UBC} (k Ω)	Typ I_{UBC} (A)	Min I_{UBC} (-10%) (A)	Max I_{UBC} (+10%) (A)
Typ R	107	2	1.8	2.2
Min R	105.93	2.014	1.813	2.215
Max R	108.07	1.974	1.777	2.171

Setting the Minimum and Maximum Buck-Balance Current

Once the resistance is selected, the minimum and maximum range of I_{UBC} can be estimated by considering the I_{UBC} tolerance (ΔI_{UBC}) and the resistor tolerance (ΔR). The MP2643's I_{UBC} tolerance (ΔI_{UBC}) is $\pm 10\%$.

Setting the Maximum Buck-Balance Current

To set the maximum I_{UBC} (I_{UBC_MAX}), the R_{UBC} accuracy and I_{UBC} tolerance must be considered. The minimum R_{UBC} (R_{UBC_MIN}) can be calculated with Equation (6):

$$R_{UBC_MIN} = \frac{640 \times (1 + \Delta I_{UBC})}{3 \times I_{UBC_MAX} \times (1 - \Delta R)} (k\Omega) \quad (6)$$

Select the closest standard resistance that either exceeds or is equal to R_{UBC_MIN} .

Determining the Maximum Buck-Balance Current

Consider an example where R_{UBC} is calculated for a target I_{UBC_MAX} to be 2A based on $\Delta R = \pm 1\%$ and $\Delta I_{UBC} = \pm 10\%$. R_{UBC_MIN} is 118.5k Ω according to Equation (6). The closest 1% standard resistance that either exceeds or is equal to R_{UBC_MIN} is 120k Ω . Table 4 shows the minimum I_{UBC} (I_{UBC_MIN}) and I_{UBC_MAX} , based on a 120k Ω 1% resistor, confirming that I_{UBC} does not exceed I_{UBC_MAX} (2A).

Table 4: I_{UBC} Range When Setting I_{UBC_MAX}

Parameter	R_{UBC} (k Ω)	Typ I_{UBC} (A)	Min I_{UBC} (-10%) (A)	Max I_{UBC} (+10%) (A)
Typ R	120	1.78	1.6	1.96
Min R	118.8	1.8	1.62	1.98
Max R	121.2	1.76	1.58	1.94

Setting the Minimum Buck-Balance Current

To set I_{UBC_MIN} , the maximum R_{UBC} (R_{UBC_MAX}) can be calculated with Equation (7):

$$R_{UBC_MAX} = \frac{640 \times (1 - \Delta I_{UBC})}{3 \times I_{UBC_MIN} \times (1 + \Delta R)} (k\Omega) \quad (7)$$

Select the closest standard resistance that is either below or equal to R_{UBC_MAX} .

Determining the Minimum Buck-Balance Current

Consider an example where R_{UBC} is calculated for a target I_{UBC_MIN} based on $\Delta R = \pm 1\%$ and $\Delta I_{UBC} = \pm 10\%$. Using Equation (7), R_{UBC_MAX} is 380k Ω . The closest 1% standard resistance that is below or equal to R_{UBC_MAX} is 374k Ω . Table 5 shows I_{UBC_MIN} and I_{UBC_MAX} , based on a 374k Ω 1% resistor, confirming that I_{UBC} does not drop below I_{UBC_MIN} (0.5A).

Table 5: I_{UBC} Range when Setting I_{UBC_MIN}

Parameter	R_{UBC} (k Ω)	Typ I_{UBC} (A)	Min I_{UBC} (-10%) (A)	Max I_{UBC} (+10%) (A)
Typ R	374	0.57	0.531	0.627
Min R	370.26	0.576	0.518	0.634
Max R	377.74	0.565	0.508	0.622

Setting the Boost-Balance Current

The MP2643's I_{LBC} can be configured between 0.5A and 2A via R_{LBC} , which is connected between the LBC and AGND pins. By rewriting Equation (2) on page 13, R_{LBC} can be calculated given a target I_{LBC} with Equation (8):

$$R_{LBC} = \frac{V_{CU} - \eta \times V_{CL}}{\eta \times V_{CL}} \times \frac{640}{3 \times I_{LBC}} (k\Omega) \quad (8)$$

Where η is the boost-balance efficiency, V_{CL} is the lower cell voltage (between CL and AGND), and V_{CU} is the voltage of both series cells (between CU and AGND).

Based on this calculated resistance, the closest available resistance should then be selected.

Setting the Minimum and Maximum Boost-Balance Current

For a given configuration, the minimum and maximum I_{LBC} can be estimated by considering the I_{LBC} tolerance (ΔI_{LBC}), R_{LBC} , tolerance (ΔR), and the variation in the cell voltages (V_{CU} and V_{CL}) during operation. The maximum I_{LBC} tolerance (ΔI_{LBC}) of the MP2643 is $\pm 10\%$.

Based on Equation (2) on page 13, I_{LBC_MAX} occurs at the point where the cell voltages are closest to being equal, and the minimum I_{LBC} (I_{LBC_MIN}) occurs at the point where the cell voltages have the largest difference. Therefore, the ratio of V_{CU} / V_{CL} for I_{LBC_MAX} and I_{LBC_MIN} can be estimated by using the voltage difference that initiates balancing, and the voltage difference that ends balancing. For example, if boost-balance mode is initiated when V_{CL} is 3.7V and V_{CU} is 7V, then V_{CU} / V_{CL} is 1.9. If boost-balance mode is finished when V_{CL} is 3.6V and V_{CU} is 7.2V, the V_{CU} / V_{CL} is 2.

Equation (8) for calculating R_{LBC} can be simplified with Equation (9):

$$R_{LBC} = \left(\frac{V_{CU}}{\eta \times V_{CL}} - 1 \right) \times \frac{640}{3 \times I_{LBC}} (k\Omega) \quad (9)$$

Determining the Boost-Balance Current Range

Consider an example where R_{LBC} for a target I_{LBC} balance current is 2A (typical), and the full I_{LBC}

range during the balancing process must be determined. If the cell voltages begin with $V_{CL} = 3.6V$ and $V_{CU} = 7V$, and end with $V_{CL} = 3.5V$ and $V_{CU} = 7V$, then η is 0.89 since V_{CL} is below 3.65V based on Table 2 on page 13.

Using Equation (9) combined with $V_{CU} / V_{CL} = 2$ (corresponding to the balance end point), the maximum I_{LBC} (I_{LBC_MAX}) can be calculated with Equation (10):

$$I_{LBC_MAX} = 1.247 \times \frac{640}{3 \times R_{LBC}} (A) \quad (10)$$

Using Equation (9) combined with $V_{CU} / V_{CL} = 1.94$ (corresponding to the balance begin point), the minimum I_{LBC} (I_{LBC_MIN}) can be calculated with Equation (11):

$$I_{LBC_MIN} = 1.185 \times \frac{640}{3 \times R_{LBC}} (A) \quad (11)$$

Using Equation (9) combined with the average $V_{CU} / V_{CL} = 1.97$, the typical I_{LBC} (I_{LBC_TYP}) can be calculated with Equation (12):

$$I_{LBC_TYP} = 1.216 \times \frac{640}{3 \times R_{LBC}} (A) \quad (12)$$

Equation (12) can be rewritten to calculate R_{LBC} for a typical I_{LBC} with Equation (13):

$$R_{LBC_TYP} = 1.216 \times \frac{640}{3 \times I_{LBC}} (k\Omega) \quad (13)$$

Using Equation (13), R_{LBC} is 129.7k Ω for a typical I_{LBC} of 2A. Using the 1% resistor tolerance ($\Delta R = 1\%$), the closest standard resistance is 130k Ω .

By using $R_{LBC} = 130k\Omega$, $\Delta I_{LBC} = 10\%$, and $\Delta R = 1\%$ for Equation (10), Equation (11), and Equation (12), I_{LBC} ranges between 1.73A and 2.27A during balancing operation.

Table 6: I_{LBC} Range when Setting I_{LBC_TYP}

Parameter	R_{LBC} (k Ω)	Typ I_{LBC} (A)	Min I_{LBC} (-10%) (A)	Max I_{LBC} (+10%) (A)
Typ R	130	2	1.75	2.25
Min R	128.7	2.02	1.77	2.27
Max R	131.3	1.97	1.73	2.23

Setting the Maximum Boost-Balance Current

I_{LBC_MAX} corresponds to the minimum R_{LBC} (R_{LBC_MIN}). As a result, R_{LBC_MIN} must be calculated first to ensure that I_{LBC} does not exceed the target maximum. R_{LBC_MIN} can be calculated by considering the I_{LBC} tolerance (ΔI_{LBC}) and resistor tolerance (ΔR). Based on Equation (9) on page 15, R_{LBC_MIN} (in k Ω) can be calculated with Equation (14):

$$R_{LBC_MIN} = \left(\frac{V_{CU}}{\eta \times V_{CL}} - 1 \right) \times \frac{640 \times (1 + \Delta I_{LBC})}{3 \times I_{LBC_MAX} \times (1 - \Delta R)} \quad (14)$$

Determining the Maximum Boost-Balance Current

Consider an example where R_{LBC_MIN} is calculated for a target I_{LBC_MAX} of 2A. If $\Delta R = \pm 1\%$, $\Delta I_{LBC} = \pm 10\%$, $V_{CL} = 3.6V$, and $V_{CU} = 7V$ at the beginning of balancing, then $V_{CL} = 3.5V$ and $V_{CU} = 7V$ at the end of balancing, and $\eta = 0.89$.

From Equation (14), R_{LBC_MIN} occurs at the point where the cell voltages are closest to being equal, which corresponds to the end of balancing. In this example, the cell voltages are equal at the end of balancing ($V_{CU} = 2 \times V_{CL}$). Entering these variables into Equation (14), R_{LBC_MIN} is calculated to be 147.8k Ω . This is the lowest resistance that ensures the target I_{LBC_MAX} . The closest standard resistance exceeding or equal to R_{LBC_MIN} is 150k Ω .

Table 7 shows the results from entering these variables into Equation (2) on page 13 and confirms that I_{LBC} remains below I_{LBC_MAX} (2A).

Table 7: I_{LBC} Range when Setting I_{LBC_MAX}

Parameter	R_{LBC} (k Ω)	Typ I_{LBC} (A)	Min I_{LBC} (-10%) (A)	Max I_{LBC} (+10%) (A)
Typ R	150	1.73	1.52	1.95
Min R	148.5	1.75	1.53	1.97
Max R	151.5	1.71	1.5	1.93

Setting the Minimum Boost-Balance Current

I_{LBC_MIN} corresponds to the maximum R_{LBC} (R_{LBC_MAX}). As a result, R_{LBC_MAX} must be calculated first to ensure that I_{LBC} does not drop below the target minimum. R_{LBC_MAX} can be calculated by considering the I_{LBC} tolerance (ΔI_{LBC}) and resistor tolerance (ΔR).

Based on Equation (9) on page 15, R_{LBC_MAX} (in k Ω) can be calculated with Equation (15):

$$R_{LBC_MAX} = \left(\frac{V_{CU}}{\eta \times V_{CL}} - 1 \right) \times \frac{640 \times (1 - \Delta I_{LBC})}{3 \times I_{LBC_MAX} \times (1 + \Delta R)} \quad (15)$$

Determining the Minimum Boost-Balance Current

Consider an example where R_{LBC_MAX} is calculated for a target I_{LBC_MIN} of 0.5A. If $\Delta R = \pm 1\%$, $\Delta I_{LBC} = \pm 10\%$, $V_{CL} = 3.6V$, and $V_{CU} = 7V$ at the beginning of balancing, then $V_{CL} = 3.5V$ and $V_{CU} = 7V$ at the end of balancing, and $\eta = 0.89$.

From Equation (15), R_{LBC_MAX} occurs at the point where the cell voltages have the largest difference, which corresponds to the beginning of balancing. In this example, there is a 200mV difference between the cell voltages at the beginning of balancing ($V_{CU} = 1.94 \times V_{CL}$). Entering these variables into Equation (15), R_{LBC_MAX} calculated to be 450.5k Ω . This is the highest resistance that ensures the target I_{LBC_MIN} . The closest standard resistance below or equal to R_{LBC_MAX} is 442k Ω .

Table 8 shows the results from entering these variables into Equation (2) on page 13 and confirms that I_{LBC} remains above I_{LBC_MIN} (0.5A).

Table 8: I_{LBC} Range when Setting I_{LBC_MIN}

Parameter	R_{LBC} (k Ω)	Typ I_{LBC} (A)	Min I_{LBC} (-10%) (A)	Max I_{LBC} (+10%) (A)
Typ R	442	0.587	0.515	0.662
Min R	437.5	0.593	0.52	0.669
Max R	446.4	0.581	0.509	0.655

Setting the CU Voltage Limit in Boost-Balance Mode

The MP2643 includes an upper cell voltage limit (V_{CU_LIM}) that can regulate V_{CU} during boost-balance mode. When V_{CU} reaches V_{CU_LIM} , the MP2643 holds the boost voltage by adjusting the boost regulator duty cycle, given V_{CU} does not exceed V_{CU_OVP} . Both are fixed at the same resistor setting.

V_{CU} is the combined voltage of both series cells. V_{CU_LIM} should be set to the target limit of the combined cells, and is set with a resistor divider as shown in Equation (3) on page 13.

Equation (3) can be rewritten to determine the resistance for a given V_{CU_LIM} with Equation (16):

$$R2 = \frac{R1 \times V_{CU_LIM_REF}}{V_{CU_LIM} - V_{CU_LIM_REF}} \text{ (k}\Omega\text{)} \quad (16)$$

A 2M Ω 1% resistor is recommended for R1.

Setting R2 for a Target CU Voltage Limit Reference

If Equation (3) on page 13 is used with $R1 = 2M\Omega$ and a target CU voltage limit reference (V_{CU_LIM}) of 7.17V, then R2 is 400k Ω .

The closest 1% standard resistance for R2 is 402k Ω . Based on Equation (3), the resulting V_{CU_LIM} is 7.17V and V_{CU_OVP} is 8.07V. When V_{CU} reaches 7.17V, the MP2643 holds the boost voltage by adjusting the boost regulator duty cycle. If V_{CU} exceeds 8.07V, the MP2643 disables boost-balance and turns off the Q_{RB} FET. When V_{CU} returns to a safe level, boost-balance restarts.

Selecting the Inductor

Selecting the inductor requires a tradeoff between cost, size, and efficiency. A lower inductance corresponds to a smaller size, but results in higher ripple currents, higher magnetic hysteretic losses, and requires more output

capacitances. The inductor ripple current (ΔI_L) is suggested to not exceed 30% of the maximum load current under the worst-cases conditions. For example, if I_{UBC} is set to 2A, the output current through the inductor is about 4A. (suppose duty is 50% and ignore the power loss), and then ΔI_L is generally set at 1.2A.

The MP2643 implements a peak current control mode architecture. For stable operation, the minimum recommended ripple current is 0.5A. Therefore, ΔI_L is between 0.5A and 30% of the maximum load current.

The inductance (L) can be calculated with Equation (17):

$$L = \frac{V_{CU} - V_{CL}}{\Delta I_L} \times \frac{V_{CL}}{V_{CU} \times f_{sw}} \text{ (}\mu\text{H)} \quad (17)$$

The inductor's peak current (I_{PEAK}) can be calculated with Equation (18)

$$I_{PEAK} = \frac{V_{CU}}{V_{CL}} \times I_{UBC} + \frac{1}{2} \times \Delta I_L \text{ (A)} \quad (18)$$

Where V_{CU} , V_{CL} , and f_{sw} are the two cells voltage in series, lower cell voltage, and switching frequency respectively.

Table 9 provides the inductance selection guide.

Table 9: Inductance Selection Guide

Inductance Selection							
Spec	Conditions	L_{MIN} (μ H)	L_{MAX} (μ H)	L (μ H)	Saturation Current (A) ⁽⁷⁾	DCR (m Ω)	Package
$V_{CU} = 6.2V$ $V_{CL} = 3V$ $I_{UBC} = 2A$	$\Delta I_L = \max(0.3 \times I_{UBC} / \text{duty}, 0.5A)$ $\Delta I_{L_MIN} = 0.5A$ $\Delta I_{L_MAX} = 1.24A$	1.31	3.26	2.2	>5.75	<50	Application Required

Note:

7) The saturation current of the inductor must exceed the inductor's maximum peak current with an additional 1A margin.

Selecting the CU Capacitor

The CU port is the converter's input during buck-balance, and the converter's output during boost-balance. The capacitor at CU (C_{CU}) absorbs the ripple current from the pulse-width modulation (PWM) converter.

In buck-balance mode, C_{CU} is the input capacitor of the converter. The input current ripple (I_{RIP_MAX}) can be calculated with Equation (19):

$$I_{RIP_MAX} = I_{UBC_MAX} \times \sqrt{(V_{CU_MAX} - V_{CL_MIN}) / V_{CL_MIN}} \quad (19)$$

In boost-balance mode, C_{CU} is the output capacitor of the converter. Maintain a small CU ripple (<0.5%) to ensure feedback loop stability.

If I_{UBC_MAX} is 2A, V_{CL_MIN} is 2.4V, and V_{CU_MAX} is 7.2V, then the maximum ripple current is 0.94A. Select the input capacitors to ensure that the temperature rise caused by the ripple current does not exceed 10°C. It is recommended to use 22 μ F ceramic capacitors with X5R or X7R dielectrics, as well as low-ESR and small temperature coefficients. A capacitor with a minimum 16V rating is recommended for a 7.2V input voltage (V_{IN}).

The input decoupling capacitor must be placed as close as possible to the CU and PGND pins.

Selecting the CL Capacitor

Select the CL capacitor (C_{CL}) based on the demand of the system current ripple.

C_{CL} is the converter's output capacitor during boost-balance and the converter's input capacitor during buck-balance. The V_{CL} ripple resistance (ΔR_{VCL}) can be calculated with Equation (20):

$$\Delta r_{VCL} = \frac{\Delta V_{CL}}{V_{CL}} = \frac{1 - V_{CL} / V_{CU}}{8 \times C_{CL} \times f_{SW}^2 \times L} \quad (20)$$

C_{CL} can be calculated with Equation (21):

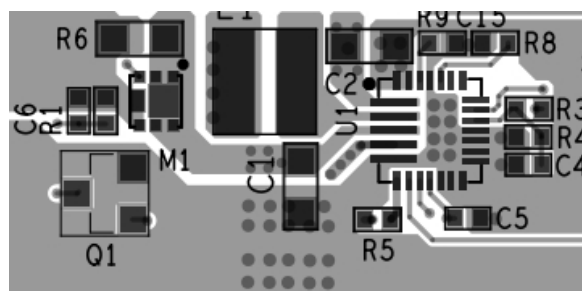
$$C_{CL} = \frac{1 - V_{CL_MIN} / V_{CU_LIM}}{8 \times \Delta r_{VCL_MIN} \times f_{SW}^2 \times L} \quad (21)$$

The capacitance is recommended to not be below 22 μ F, and rated for a minimum 10V voltage capacitor is sufficient.

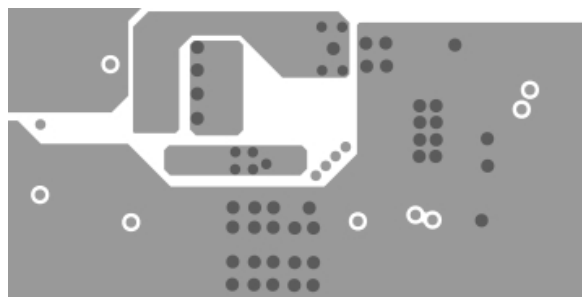
PCB Layout Guidelines

Efficiency PCB layout is critical for stable operation, especially to meet the specified noise and efficiency requirements. A 4-layer layout is strongly recommended. Additional layers may be required for multi-chip applications. For the best results, refer to Figure 5 and follow the guidelines below:

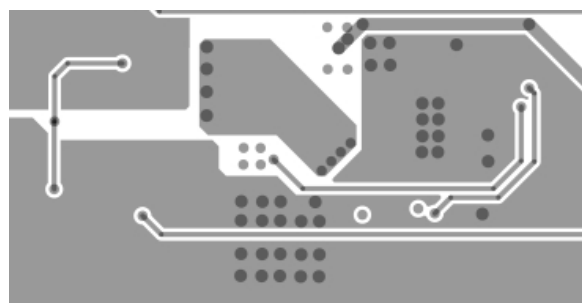
1. Route the loop of the power stages as short as possible.
2. Route the PGND copper for the CL and CU capacitors together using the shortest possible trace.
3. Place the PGND copper of the CL and CU capacitors as close as possible to the PGND pin and the IC's thermal pad using as much copper area as possible.
4. Place the CU and CL as close to the IC pins as possible.
5. Keep the switching node short, and route it away from all small control signals.
6. Place the BST capacitor (C_{BST}) between the SW and BST pins.
7. If there is a resistor in series with C_{BST} , make the RC route as short as possible, and place C_{BST} as close to the IC pin as possible.
8. Place the decoupling capacitors (e.g. VCC capacitor) as close to the IC pin as possible.
9. Connect the IC's power pins (CU, CL, and PGND) to as many copper planes as possible for improved thermal performance.



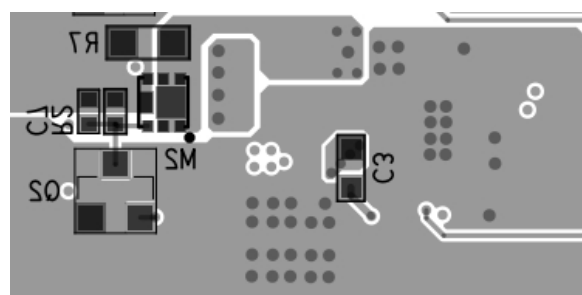
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

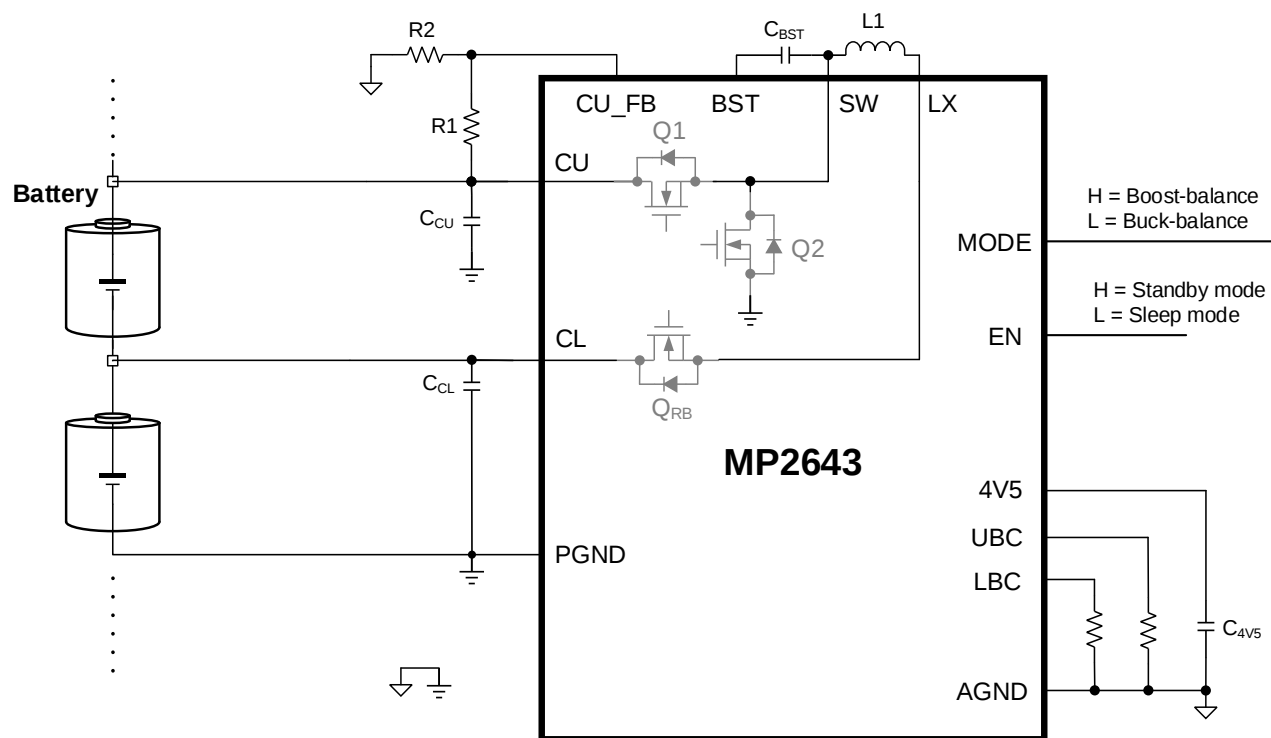


Figure 6: Typical Application Circuit

Table 10: Key BOM for the Typical Application Circuit

Qty	Ref	Value	Description	Package	Manufacturer
1	Ccu	22μF	Ceramic capacitor, 16V, X5R or X7R	0603	Any
1	Ccl	22μF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C4v5	1μF	Ceramic capacitor, 10V, X5R or X7R	0603	Any

TYPICAL APPLICATION CIRCUITS (continued)

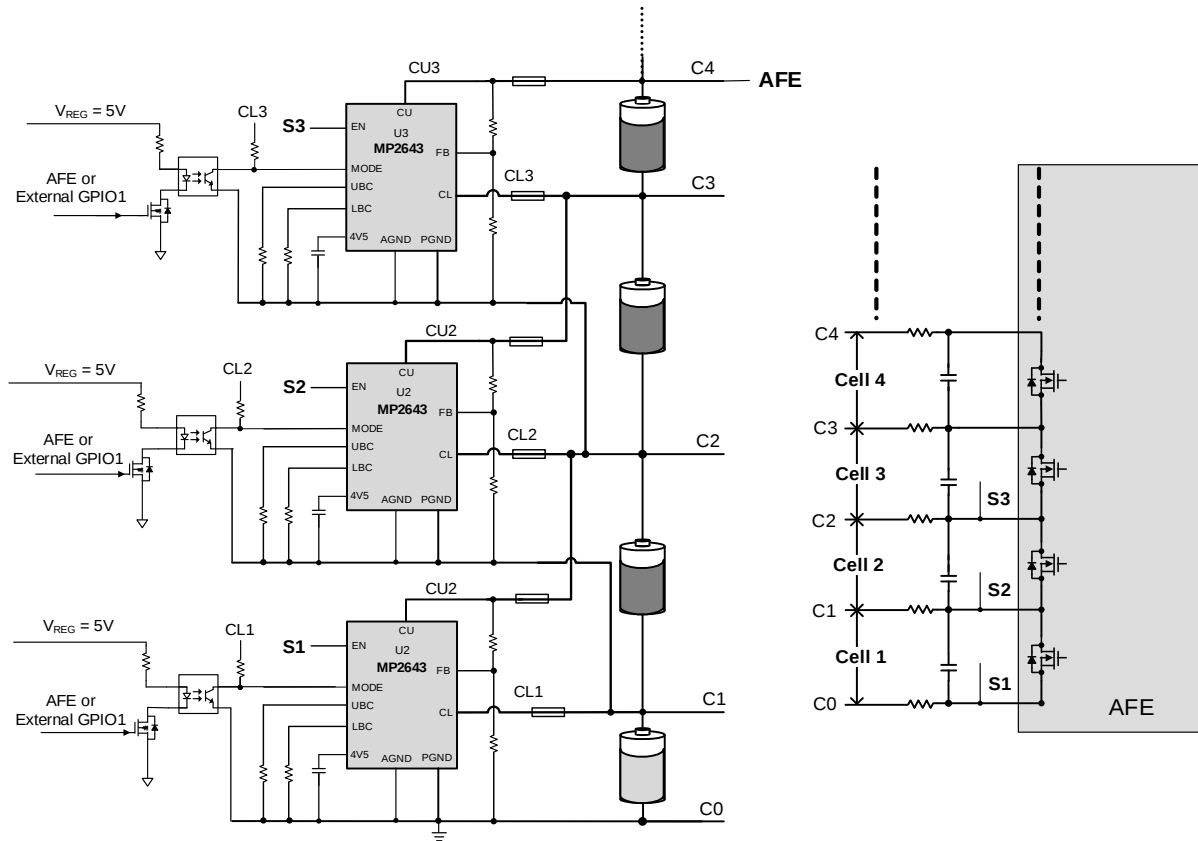
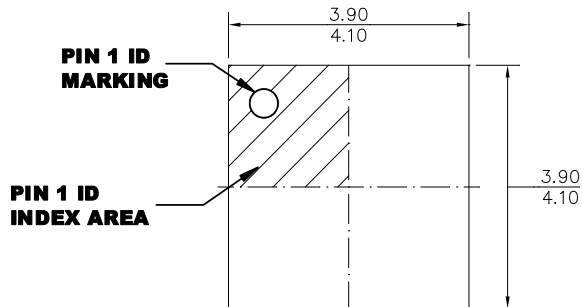


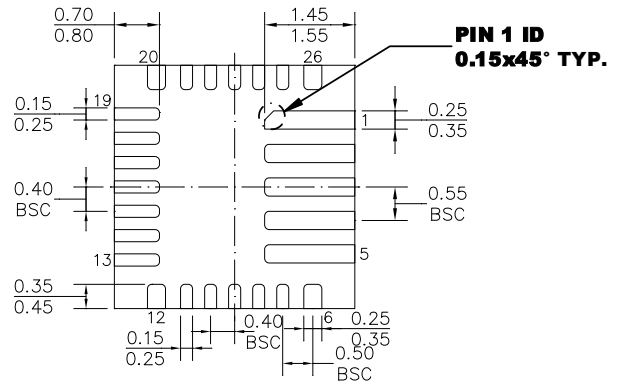
Figure 7: Typical Application Circuit in ESS

PACKAGE INFORMATION

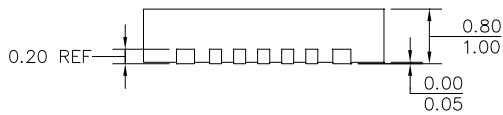
QFN-26 (4mmx4mm)



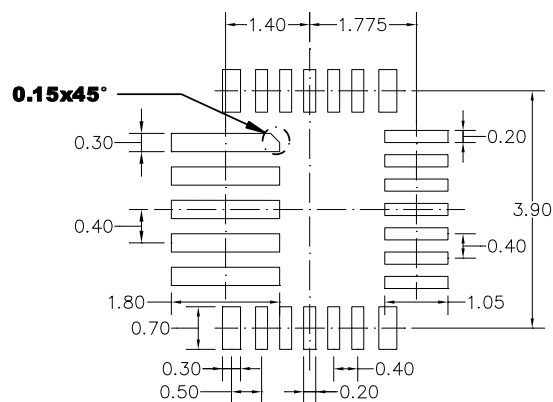
TOP VIEW



BOTTOM VIEW



SIDE VIEW

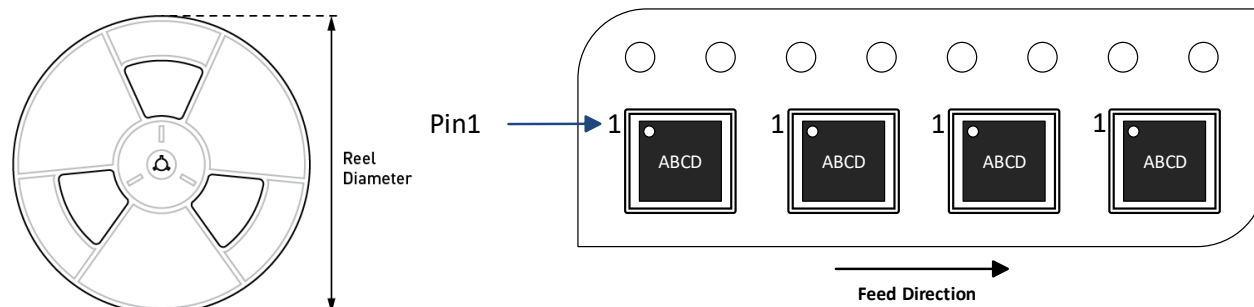


RECOMMENDED LAND PATTERN

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10
MILLIMETERS MAX.
3) DRAWING CONFORMS TO JEDEC MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2643GR-Z	QFN-26 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/21/2024	Initial Release	-

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