MP2770

I²C-Controlled, 6A, 1-Cell Switching Charger with Power Path Management and 3.65A Boost Output

DESCRIPTION

The MP2770 is a highly-integrated, flexible, switch-mode battery management device with system power path management. It is designed for single-cell Li-ion and Li-polymer batteries used in a wide range of portable applications.

The IC has an integrated IN to SYS pass-through path to send input voltage (V_{IN}) to the system even while charging is disabled.

When the input is present, the MP2770 operates in charge mode. The device detects the battery voltage (V_{BATT}) automatically and charges the battery with three phases: pre-charge, constant current fast charge, and constant voltage charge. The MP2770 manages the input and meets the system power demand priority with the integrated input current limit (I_{IN_LIMIT}) and V_{IN} regulation.

In the absence of the input source, the MP2770 can operate in boost mode to power the IN or SYS pin from the battery.

The charge and boost parameters (e.g. input clamp voltage, boost voltage (V_{BST}), current limit (I_{LIMIT}), I_{IN_LIMIT}, charging current, and charge full voltage) can be flexibly configured via the I²C interface.

Full safety features include output short-circuit protection (SCP), input over-voltage protection (OVP), battery under-voltage lockout (UVLO) protection, thermal shutdown, and battery temperature monitoring.

The MP2770 is available in a small QFN-18 (3mmx4mm) package.

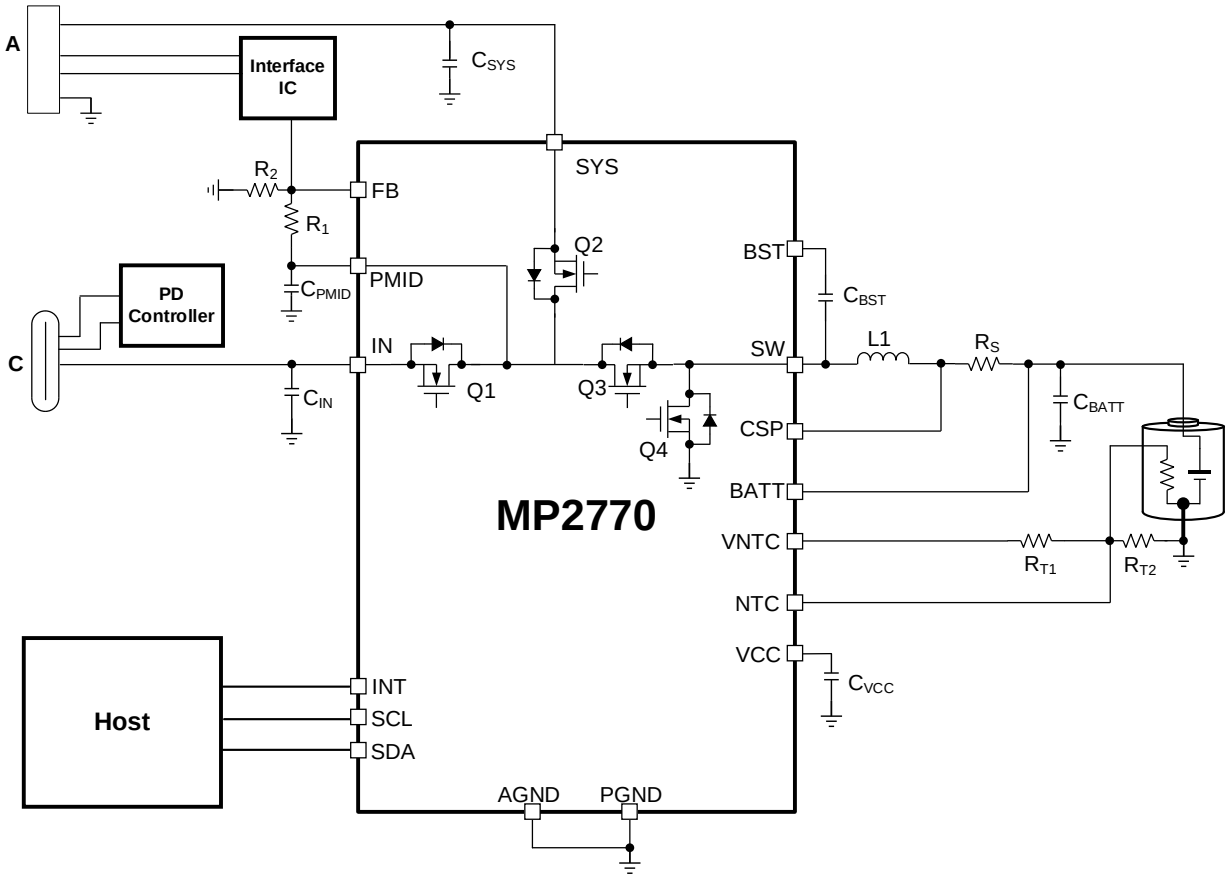
FEATURES

- 4V to 16V Operating Input Voltage (V_{IN}) Range
- Up to 20V Sustainable Voltage
- Up to 6A Configurable Charging Current
- 3.6V to 4.45V Configurable Charge Regulation Voltage with ±0.5% Accuracy
- Supports USB 2.0, USB 3.0, USB 3.1, USB 3.2, Type-C, and USB PD I_{IN_LIMIT} Settings
- Minimum V_{IN} Loop for Maximum Adapter Power Tracking
- Up to 22.5W Boost Output Power with a 3V Battery
- 4.3V to 16V V_{BST} with 20mV/Step
- 500mA to 3.65A I_{BOOST} with 50mA/Step
- Down to 12µA Battery Leakage in Standby Mode
- 5mΩ/10mΩ Battery Current-Sense Resistor
- Battery Discharge Current Limiting
- Up to 1.6x Overload Capability for 2ms
- Light-Load Detection and Output Plug-In Detection for the SYS Port
- Integrated 8-Bit ADC for Monitoring V_{IN}, V_{BATT}, V_{SYS}, V_{PMID}, I_{Q1}, I_{BATT}, I_{SYS}, and NTC
- I²C Interface for Real-Time Charge Parameter Configuration and Status Reporting
- Comprehensive Safety Features:
  - Charging Safety Timer
  - Watchdog Timer
  - Thermal Regulation and Shutdown
  - Customizable JEITA for Battery Temperature Monitoring
  - Cycle-by-Cycle OCP
  - SYS OCP and SCP
- Available in a Small QFN-18 (3mmx4mm) Package

APPLICATIONS

- Sub-Batteries
- USB Power Delivery (PD)
- Power Banks

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP2770GL-xxxx**	QFN-18 (3mmx4mm)	See below	1

* For Tape & Reel, add suffix -Z (e.g. MP2770GL-xxxx-Z).

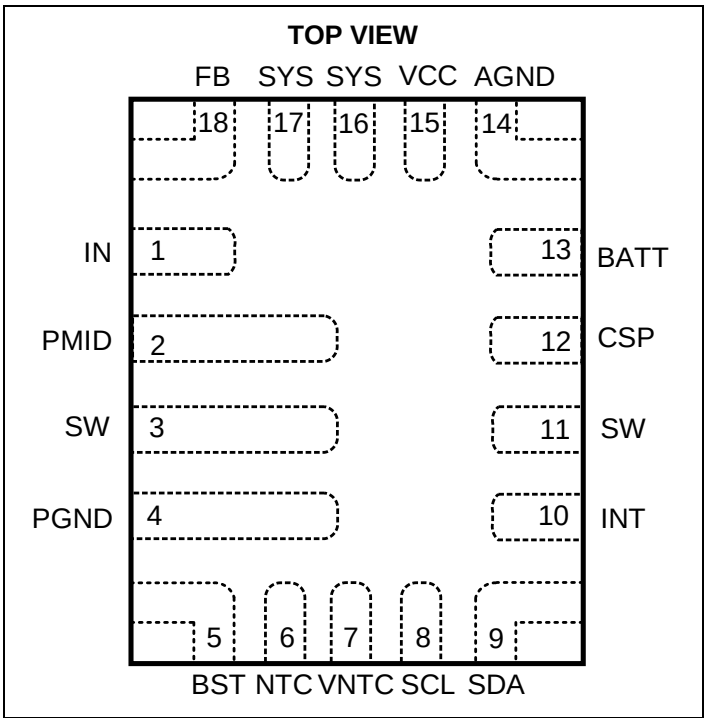
** "xxxx" is the configuration code identifier for the register settings. Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique configuration code. The factory default is "0000". This setting can be viewed in the I²C register map.

TOP MARKING

MPYW
2770
LLL

MP: MPS prefix
Y: Year code
W: Week code
2770: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-18 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	IN	Power	**IC input power supply.** Place a 22µF ceramic capacitor between the IN and PGND pins. Place this capacitor as close to the IC as possible. IN is also one of the boost outputs.
2	PMID	Power	**PMID.** Connect the PMID pin internally to the drains of reverse-blocking MOSFET and high-side MOSFET (HS-FET). Bypass PMID using two or three 22µF ceramic capacitors connected between the PMID and PGND pins. Place these capacitors as close to the IC as possible.
3, 11	SW	Power	**Output switching node.**
4	PGND	Power	**Power ground.**
5	BST	Power	**Bootstrap.** Connect a bootstrap capacitor (C_{BOOT}) between the BST and SW pins to form a floating supply across the power MOSFET driver to drive the power MOSFET's gate above the input voltage (V_{IN}). Place C_{BOOT} as close to the IC as possible.
6	NTC	I	**Temperature sense input.** Connect a negative temperature coefficient thermistor to the NTC pin. Configure the hot and cold temperature windows using a resistor divider connected from VNTC to NTC to AGND.
7	VNTC	O	**Reference voltage output to start up the NTC thermistor.**
8	SCL	I	**I²C interface clock.** Connect the SCL pin to the logic rail using a 10kΩ resistor.
9	SDA	I/O	**I²C interface data.** Connect the SDA pin to the logic rail using a 10kΩ resistor.
10	INT	O	**Open-drain interrupt output.** The INT pin sends the charging status and fault interrupt status to the host.
12	CSP	I	**Battery charge current-sense positive input.**
13	BATT	Power	**Positive battery terminal.** Connect a 22µF ceramic capacitor between the BATT and PGND pins.
14	AGND	Power	**Analog ground.**
15	VCC	Power	**Power supply for the internal circuitry.** Bypass the VCC pin to AGND using a 1µF ceramic capacitor.
16, 17	SYS	Power	**System power supply.** Connect a 22µF ceramic capacitor between the SYS and PGND pins.
18	FB	I	**Boost voltage feedback.**

ABSOLUTE MAXIMUM RATINGS (1)

IN, PMID, SYS to PGND..... -0.3V to +20V
SW to PGND..... -0.3V (-2V for 20ns) to +20V (24V for 20ns)
BST to PGND .....SW to SW + 5V
BATT to PGND .....-0.3V to +6V
All other pins to AGND.....-0.3V to +5V
Continuous power dissipation (T_A = 25°C) (2)..... 2.4W
Junction temperature..... 150°C
Lead temperature (solder) .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) 2kV
Charged device model (CDM)..... 2kV

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4V to 16V
Input current (I_{IN}).....Up to 3.5A
SYS current (I_{SYS}).....Up to 3.65A
Charge current (I_{CC}) .....Up to 6A
Battery voltage (V_{BATT}) .....Up to 4.5V
Operating junction temp (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-18 (3mmx4mm)	46.6	4.2	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on a JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Quiescent Current						
Battery current	I_{BATT}	V_{IN} is not present, standby mode, V_{BATT} = 4.2V, SYS plug-in detection is disabled, ADC is disabled		12	20	µA
		Boost mode, VBST[9:0] = 5V, I_{BST} = 0A, V_{BATT} = 4.2V, ADC is disabled		2		mA
Suspended input current	I_{IN_SUS}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT} + V_{HDRM}, standby mode, switching is disabled, SYS is floating			1	mA
Input current	I_{IN}	V_{IN} > V_{IN_UVLO}, V_{IN} > V_{BATT} + V_{HDRM}, charge mode, V_{BATT} = 4.3V			2	mA
Power Path						
Input voltage (V_{IN}) under-voltage lockout (UVLO) threshold	V_{IN_ULVO}	V_{IN} is falling	3	3.2	3.4	V
Input UVLO hysteresis				400		mV
Headroom voltage	V_{HDRM}	V_{IN} is rising, V_{IN} vs. V_{BATT}	250	350	450	mV
		V_{IN} is falling, V_{IN} vs. V_{BATT}	40	128	220	mV
V_{IN} over-voltage protection (OVP) threshold	V_{IN_OVP}	V_{IN} is rising, VINOVP[1:0] = 6.4V	6.15	6.4	6.65	V
		V_{IN} is rising, VINOVP[1:0] = 16.8V	16.4	16.8	17.2	V
V_{IN} OVP hysteresis				400		mV
VCC LDO output voltage	V_{CC}	V_{IN} = 5V, I_{VCC} = 10mA	3.55	3.65	3.75	V
V_{CC} UVLO threshold	V_{CC_UVLO}	V_{CC} is rising	2	2.2	2.4	V
V_{CC} UVLO hysteresis				100		mV
VIN to PMID MOSFET (Q1) on resistance	$R_{DS(ON)\_Q1}$			20		mΩ
PMID to SYS MOSFET (Q2) on resistance	$R_{DS(ON)\_Q2}$			20		mΩ
High-side MOSFET (HS-FET) (Q3) on resistance	$R_{DS(ON)\_Q3}$			10		mΩ
Low-side MOSFET (LS-FET) (Q4) on resistance	$R_{DS(ON)\_Q4}$			5		mΩ
HS-FET peak current limit (I_{LIMIT})	I_{PEAK_HS}	Constant current fast charge	9	10		A
		Pre-charge		4		A
LS-FET valley I_{LIMIT}	I_{VALLEY_LS}			7.4		A
LS-FET peak I_{LIMIT}	I_{PEAK_LS}	Boost mode, LS_PK = 1	10	12		A
Switching frequency	f_{SW}	FSW[1:0] = 600kHz	550	600	650	kHz
		FSW[1:0] = 1000kHz	900	1000	1100	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Charge Mode						
Battery regulation voltage	V_{BATT_REG}	VBATT_REG[2:0] = 4.2V	4.179	4.2	4.221	V
		VBATT_REG[2 :0] = 4.2V, T_A = 0°C to 70°C	4.179	4.2	4.221	V
		VBATT_REG[2:0] = 4.35V	4.328	4.35	4.375	V
		VBATT_REG[2:0] = 4.35V, T_A = 0°C to 70°C	4.328	4.35	4.375	V
Fast charge current	I_{CC}	ICC[5:0] = 0.5A, RSNS = 10mΩ	0.4	0.5	0.6	A
		ICC[5:0] = 0.5A, RSNS = 10mΩ, T_A = 0°C to 70°C	0.4	0.5	0.6	A
		ICC[5:0] = 2A, RSNS = 10mΩ	1.85	2	2.15	A
		ICC[5:0] = 2A, RSNS = 10mΩ, T_A = 0°C to 70°C	1.85	2	2.15	A
		ICC[5:0] = 3A, RSNS = 10mΩ	2.8	3	3.2	A
		ICC[5:0] = 3A, RSNS = 10mΩ, T_A = 0°C to 70°C	2.8	3	3.2	A
		ICC[5:0] = 5A, RSNS = 10mΩ	4.7	5	5.3	A
		ICC[5:0] = 5A, RSNS = 10mΩ, T_A = 0°C to 70°C	4.7	5	5.3	A
		ICC[5:0] = 3A, RSNS = 5mΩ	2.8	3	3.2	A
		ICC[5:0] = 3A, RSNS = 5mΩ, T_A = 0°C to 70°C	2.8	3	3.2	A
		ICC[5:0] = 5A, RSNS = 5mΩ	4.7	5	5.3	A
		ICC[5:0] = 5A, RSNS = 5mΩ, T_A = 0°C to 70°C	4.7	5	5.3	A
Charge Termination Current	I_{TERM}	ITERM[1:0] = 50mA, RSNS = 10mΩ, T_A = 0°C to 70°C	5	50	100	mA
		ITERM[1:0] = 100mA, RSNS = 10mΩ	50	100	150	mA
		ITERM[1:0] = 100mA, RSNS = 10mΩ, T_A = 0°C to 70°C	30	100	175	mA
		ITERM[1:0] = 100mA, RSNS = 5mΩ	50	100	150	mA
		ITERM[1:0] = 100mA, RSNS = 5mΩ, T_A = 0°C to 70°C	30	100	175	mA
Recharge threshold below V_{BATT_REG}	V_{RECH}	V_{BATT} falling, VBATT_REG = 4.2V		4.7		%
Battery pre-charge threshold	V_{BATT_PRE}	VBATT_PRE[1:0] = 3V, V_{BATT} rising	2.9	3	3.1	V
		VBATT_PRE[1:0] = 2.5V, V_{BATT} rising	2.4	2.5	2.6	V
Battery pre-charge hysteresis				200		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Pre-charge current	I_{PRE}	IPRE[1:0] = 50mA, V_{BATT} = 2.7V, RSNS = 10mΩ, T_A = 0°C to 70°C	5	50	110	mA
		IPRE[1:0] = 100mA, V_{BATT} = 2.7V, RSNS = 10mΩ	65	100	135	mA
		IPRE[1:0] = 100mA, V_{BATT} = 2.7V, RSNS = 10mΩ, T_A = 0°C to 70°C	55	100	160	mA
		IPRE[1:0] = 100mA, V_{BATT} = 2.7V, RSNS = 5mΩ	65	100	135	mA
		IPRE[1:0] = 100mA, V_{BATT} = 2.7V, RSNS = 5mΩ, T_A = 0°C to 70°C	55	100	160	mA
Termination deglitch time	t_{TERM_DGL}			200		ms
Recharge deglitch time	t_{RECH_DGL}			200		ms
Charging safety timer	t_{CHARGE}	CHG_TMR[1:0] = 11		20		hrs
Input Regulation						
Minimum V_{IN} regulation	V_{IN_MIN}	VIN_MIN[6:0] = 4.44V	4.31	4.44	4.57	V
		VIN_MIN[6:0] = 4.44V, T_A = 0°C to 70°C	4.305	4.44	4.575	V
		VIN_MIN[6:0] = 8.04V	7.8	8.04	8.28	V
		VIN_MIN[6:0] = 8.04V, T_A = 0°C to 70°C	7.75	8.04	8.285	V
		VIN_MIN[6:0] = 11.04V	10.7	11.04	11.37	V
		VIN_MIN[6:0] = 11.04V, T_A = 0°C to 70°C	10.695	11.04	11.375	V
Input I_{LIMIT}	I_{IN_LIMIT}	IIN_LIM[3:0] = 3A	2.5	2.7	3	A
		IIN_LIM[3:0] = 3A, T_A = 0°C to 70°C	2.5	2.7	3	A
		IIN_LIM[3:0] = 1.5A	1.25	1.35	1.5	A
		IIN_LIM[3:0] = 1.5A, T_A = 0°C to 70°C	1.25	1.35	1.5	A
		IIN_LIM[3:0] = 0.5A	0.4	0.45	0.5	A
		IIN_LIM[3:0] = 0.5A, T_A = 0°C to 70°C	0.4	0.45	0.5	A
Boost Mode						
Headroom voltage	V_{HDRM_BST}	V_{BATT} rising, V_{BST} vs. V_{BATT}	250	340	450	mV
		V_{BATT} falling, V_{BST} vs. V_{BATT}		140		mV
Boost voltage	V_{BST}	VBST[9:0] = 5V, I_{SYS} = 10mA, tested at the PMID pin	4.75	5	5.25	V
		VBST[9:0] = 9V, I_{SYS} = 10mA, tested at the PMID pin	8.55	9	9.45	V
		VBST[9:0] =12V, I_{SYS} = 10mA, tested at the PMID pin	11.4	12	12.6	V
		VBST[9:0] =15V, I_{SYS} = 10mA, tested at the PMID pin	14.25	15	15.75	V
Feedback (FB) voltage	V_{FB}	VBST_SET = 1, external FB setting	0.915	0.93	0.945	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Boost I_{LIMIT}	I_{BST_LIMIT}	IBST_LIM[5:0] = 3.6A	3.6	3.95	4.3	A
		IBST_LIM[5:0] = 3A	3	3.3	3.6	A
		IBST_LIM[5:0] = 2.25A	2.25	2.5	2.75	A
Battery voltage (V_{BATT}) UVLO threshold	V_{BATT_UVLO}	V_{BATT} is falling, BATT_UVLO = 0	2.4	2.5	2.6	V
		V_{BATT} is falling, BATT_UVLO = 1	2.6	2.7	2.8	V
		V_{BATT} is rising, BATT_UVLO = 0		2.9		V
		V_{BATT} is rising, BATT_UVLO = 1		3		V
Analog Control						
System no-load detection threshold	I_{BST_OFF}	NOLOAD_THR = 00	1	25	60	mA
		NOLOAD_THR = 01	75	100	125	mA
System plug-in detection threshold	V_{PLUG_IN}	V_{SYS} is falling	75	80	85	% of V_{BATT}
Protection						
Battery over-voltage protection (OVP) threshold	V_{BATT_OVP}	V_{BATT} = 4.2V	102.5	104	105.5	%
Battery OVP hysteresis				2		%
Boost OVP threshold	V_{BST_OVP}			115		% of VBST [9:0]
Boost OVP hysteresis				10		%
Highest boost OVP threshold	V_{BST_OVP2}			17.6		V
Highest boost OVP hysteresis				800		mV
Thermal regulation	T_{J_REG}	TJ_REG[1:0] = 120°C		120		°C
Thermal shutdown rising threshold	T_{SD}	T_J is rising		140		°C
Thermal shutdown hysteresis				20		°C
Battery Temperature Monitoring in Charge Mode						
VNTC Voltage	V_{VNTC}		1.273	1.28	1.287	V
NTC cold temperature rising threshold	V_{COLD}	VCOLD[1:0] = 72% of V_{VNTC}	71.3	72	72.7	% of V_{VNTC}
NTC cold temperature rising threshold hysteresis				1.4		% of V_{VNTC}
NTC cool temp rising threshold	V_{COOL}	VCOOL[1:0] = 67.2% of V_{VNTC}	66.5	67.2	67.9	% of V_{VNTC}
NTC cool temperature rising threshold hysteresis				1.4		% of V_{VNTC}
NTC warm temperature falling threshold	V_{WARM}	VWARM[1:0] = 44.1% of V_{VNTC}	43.4	44.1	44.8	% of V_{VNTC}
NTC warm temperature falling threshold hysteresis				1.4		% of V_{VNTC}

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
NTC hot temperature falling threshold	V_{HOT}	VHOT[1:0] = 34% of V_{VNTC}	33.3	34	34.7	% of V_{VNTC}
NTC hot temperature falling threshold hysteresis				1.4		% of V_{VNTC}
Battery Temperature Monitoring in Boost Mode						
NTC cold temperature rising threshold	V_{BATT_COLD}	VCOLD[1:0] = 72%	71.3	72	72.7	% of V_{VNTC}
NTC cold temperature rising threshold hysteresis				1.4		% of V_{VNTC}
NTC hot temperature falling threshold	V_{BATT_HOT}	VHOT[1:0] = 34%	33.3	34	34.7	% of V_{VNTC}
NTC hot temperature falling threshold hysteresis				1.4		% of V_{VNTC}
Analog-to-Digital Converter (ADC)						
Resolution	RES			8		bits
ADC V_{IN}	V_{IN_ADC}		0		20.4	V
V_{IN_ADC} least-significant bit (LSB)	$V_{IN\_ADC\_RES}$			80		mV
V_{IN_ADC} accuracy	$V_{IN\_ADC\_ACC}$			2		LSB
ADC SYS voltage	V_{SYS_ADC}		0		20.4	V
V_{SYS_ADC} LSB	$V_{SYS\_ADC\_RES}$			80		mV
V_{SYS_ADC} accuracy	$V_{SYS\_ADC\_ACC}$			2		LSB
ADC PMID voltage (V_{PMID})	V_{PMID_ADC}		0		20.4	V
V_{PMID_ADC} LSB	$V_{PMID\_ADC\_RES}$			80		mV
V_{PMID_ADC} accuracy	$V_{PMID\_ADC\_ACC}$			2		LSB
ADC V_{BATT}	V_{BATT_ADC}		0		5.1	V
V_{BATT_ADC} LSB	$V_{BATT\_ADC\_RES}$			20		mV
V_{BATT_ADC} accuracy	$V_{BATT\_ADC\_ACC}$			2		LSB
ADC I_{BATT}	I_{BATT_ADC}		0		10.23	A
I_{BATT_ADC} LSB	$I_{BATT\_ADC\_RES}$			40		mA
I_{BATT_ADC} accuracy	$I_{BATT\_ADC\_ACC}$			3		LSB
ADC Q1 current (I_{Q1})	I_{Q1_ADC}		0		5.1	A
I_{Q1_ADC} LSB	$I_{Q1\_ADC\_RES}$			20		mA
I_{Q1_ADC} accuracy	$I_{Q1\_ADC\_ACC}$			3		LSB
I_{Q1} accuracy	I_{Q1_ACC}			3		LSB

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{BATT} = 3.8V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SYS current	I_{SYS}		0		5.1	A
I_{SYS} LSB	I_{SYS_RES}			20		mA
I_{SYS} accuracy	I_{SYS_ACC}			3		LSB
NTC voltage	V_{NTC}		0		1280	mV
V_{NTC} LSB	V_{NTC_RES}			5		mV
V_{NTC} accuracy	V_{NTC_ACC}			2		LSB
I²C Interface (SDA and SCL)						
Input high threshold		V_{PU} = 1.8V, SDA and SCL	1.3			V
Input low threshold		V_{PU} = 1.8V, SDA and SCL			0.4	V
Output low threshold (5)		I_{SINK} = 5mA			0.4	V
I²C clock frequency	f_{SCL}				400	kHz
Watchdog timer	t_{WTD}	WD[1:0] = 40s		40		sec

Note:

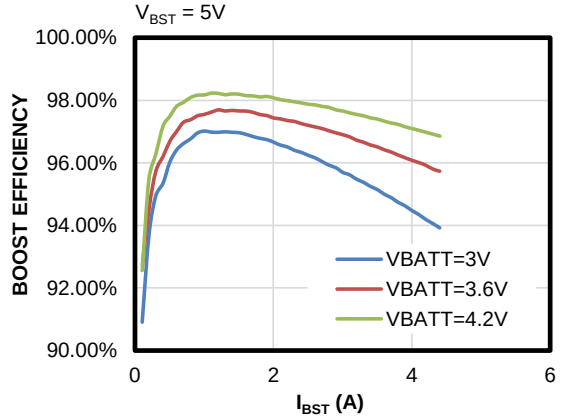
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS (6)

V_{IN} = 5V, C_{PMID} = 44µF, C_{IN} = 22µF, C_{SYS} = 22µF, C_{BATT} = 22µF, L = 2µH (DCR = 5.85mΩ), T_A = 25°C, unless otherwise noted.

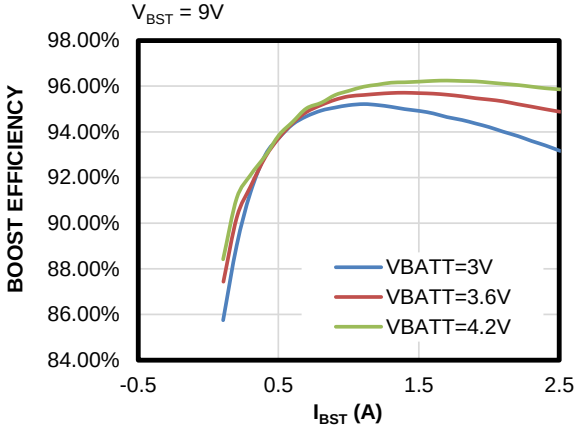
Boost Efficiency vs. Boost Current

V_{BST} = 5V



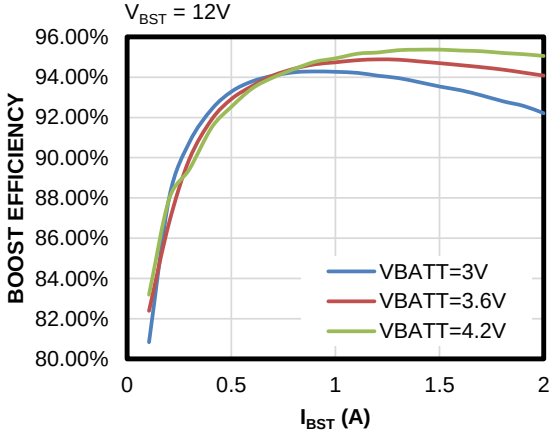
Boost Efficiency vs. Boost Current

V_{BST} = 9V



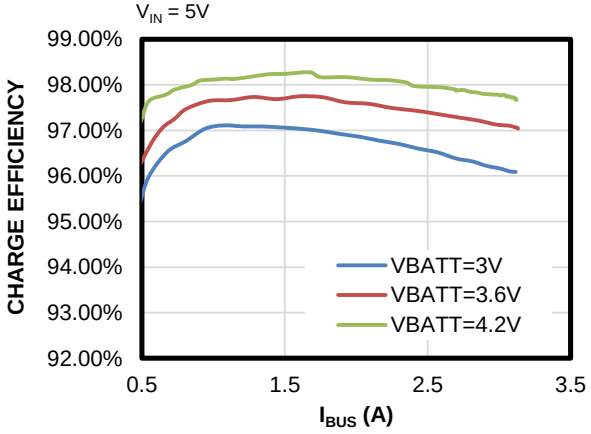
Boost Efficiency vs. Boost Current

V_{BST} = 12V



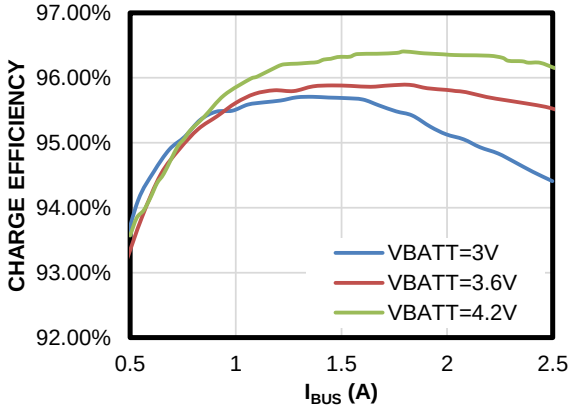
Charge Efficiency vs. Bus Current

V_{IN} = 5V



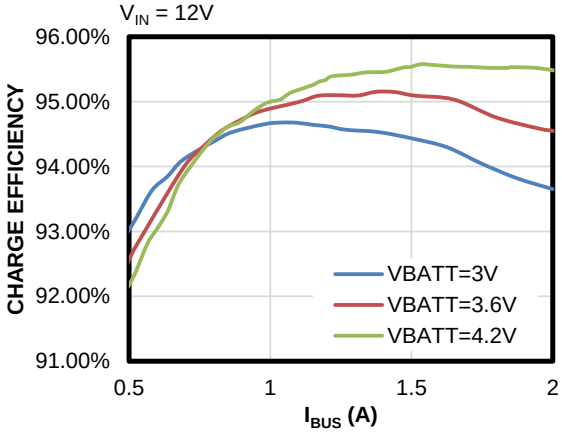
Charge Efficiency vs. Bus Current

V_{IN} = 9V



Charge Efficiency vs. Bus Current

V_{IN} = 12V



Note:

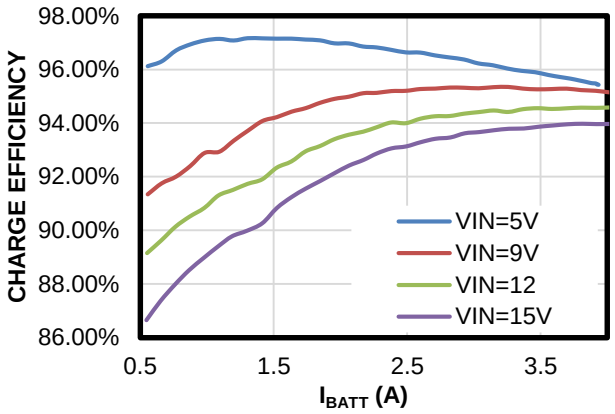
6) Efficiency is tested without the sense resistor (R_{SENSE}) and blocking MOSFET (Q1).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)* (7)

V_{IN} = 5V, C_{PMID} = 44µF, C_{IN} = 22µF, C_{SYS} = 22µF, C_{BATT} = 22µF, L = 2µH (DCR = 5.85mΩ), T_A = 25°C, unless otherwise noted.

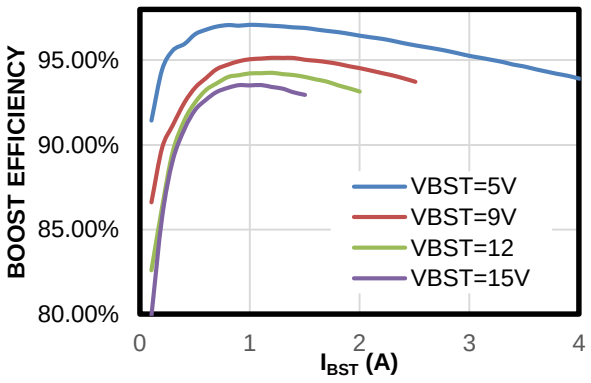
Charge Efficiency vs. Battery Current

V_{BATT} = 3.8V



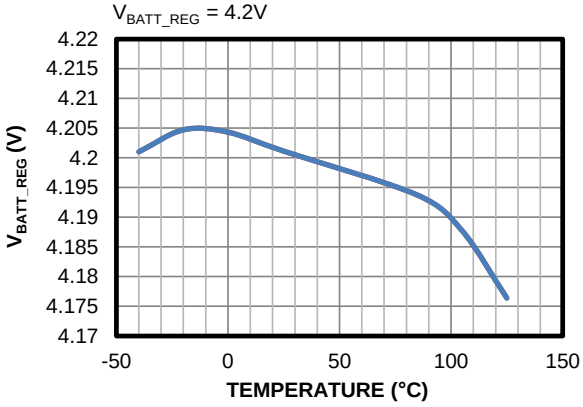
Boost Efficiency vs. Boost Current

V_{BATT} = 3.8V

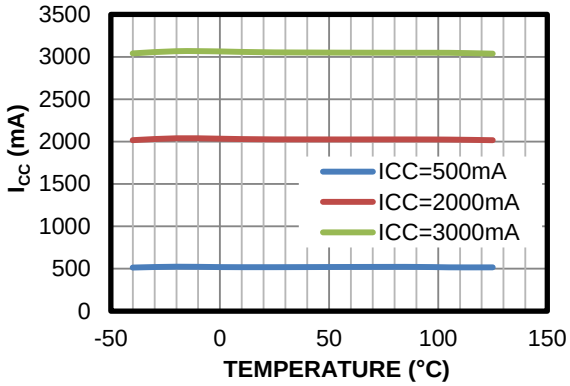


Battery Regulation Voltage vs. Temperature

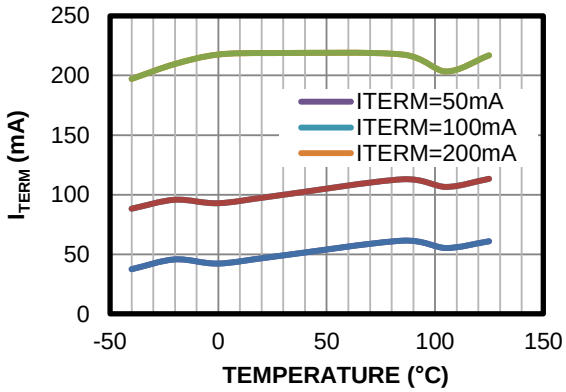
V_{BATT_REG} = 4.2V



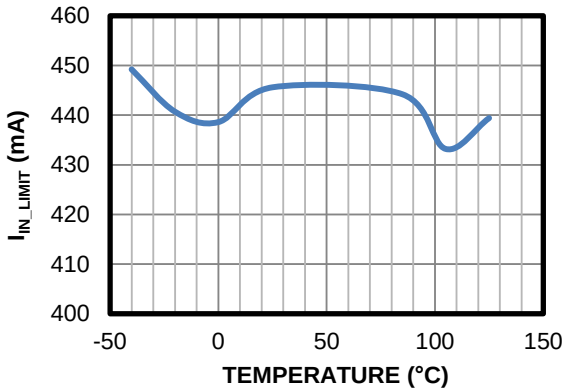
Constant Charge Current vs. Temperature



Termination Current vs. Temperature



Input Current Limit vs. Temperature



Note:

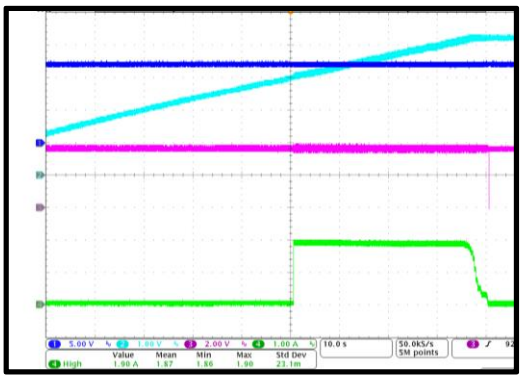
7) Efficiency is tested with R_{SENSE} and Q1.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{PMID} = 44µF, C_{IN} = 22µF, C_{SYS} = 22µF, C_{BATT} = 22µF, L = 1µH (DCR = 4.6mΩ), T_A = 25°C, unless otherwise noted.

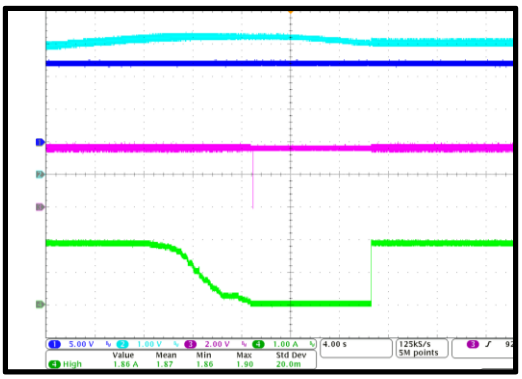
Battery Charging Curve

V_{IN} = 12V, V_{BATT_REG} = 4.2V, I_{CC} = 2A, I_{IN_LIMIT} = 3500mA



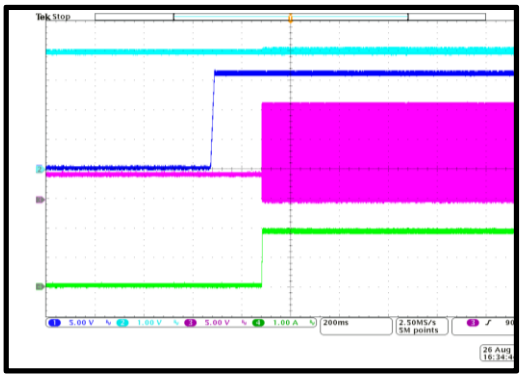
Automatic Recharge

V_{IN} = 12V, V_{BATT_REG} = 4.2V, I_{CC} = 2A, I_{IN_LIMIT} = 3500mA



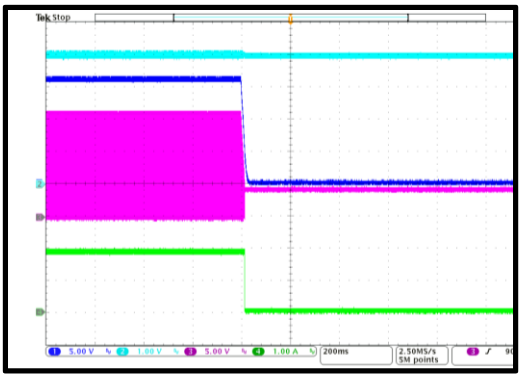
Start-Up through IN

V_{IN} = 16V, V_{BATT} = 4V, I_{CC} = 2A, I_{IN_LIMIT} = 3500mA



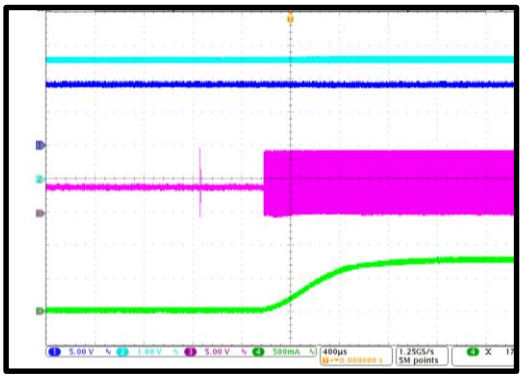
Shutdown through IN

V_{IN} = 16V, V_{BATT} = 4V, I_{CC} = 2A, I_{IN_LIMIT} = 3500mA



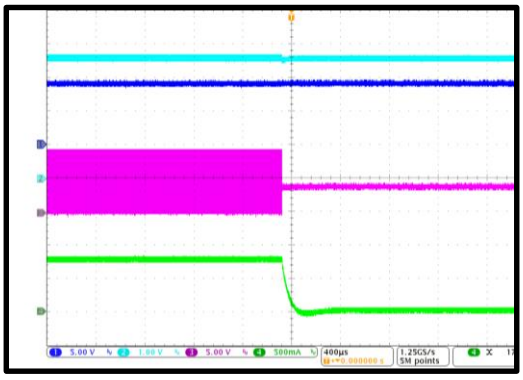
Q1 Enabled

Charge mode, V_{IN} = 9V, V_{BATT} = 3.6V, I_{CC} = 2A



Q1 Disabled

Charge mode, V_{IN} = 9V, V_{BATT} = 3.6V, I_{CC} = 2A

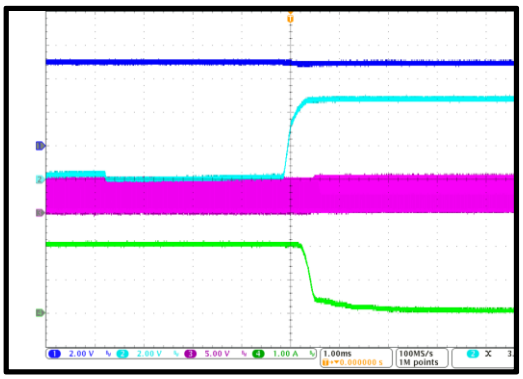


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{PMID} = 44µF, C_{IN} = 22µF, C_{SYS} = 22µF, C_{BATT} = 22µF, L = 1µH (DCR = 4.6mΩ), T_A = 25°C, unless otherwise noted.

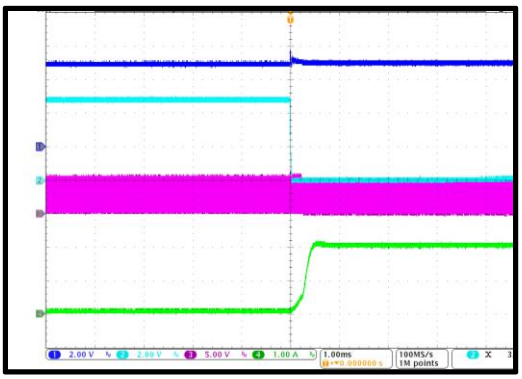
Q2 Enabled

Charge mode, V_{IN} = 5V, V_{BATT} = 3.6V, I_{CC} = 2A, I_{IN_LIMIT} = 3500mA, I_{SYS} = 3A



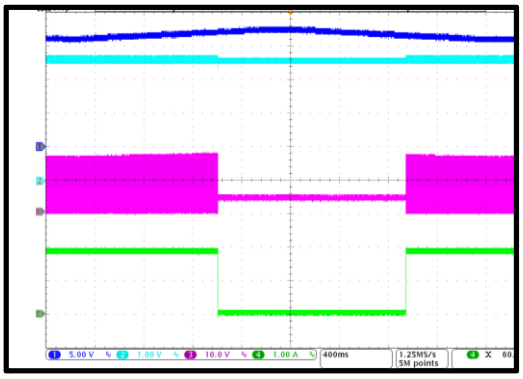
Q2 Disabled

Charge mode, V_{IN} = 5V, V_{BATT} = 3.6V, I_{CC} = 2A, I_{IN_LIMIT} = 3500mA, I_{SYS} = 3A



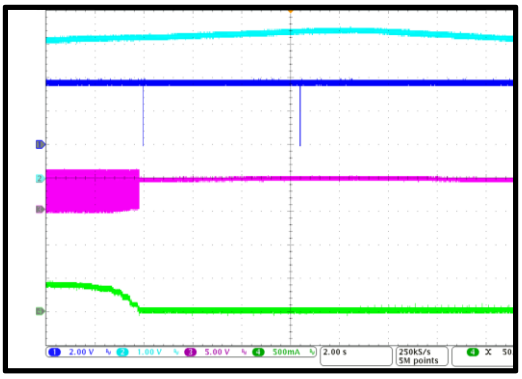
V_{IN} OVP

Charge mode; V_{IN} = 16V, V_{BATT} = 3.6V, I_{CC} = 2A, I_{IN_LIMIT} = 3500mA, V_{IN_OVP} = 16.8V



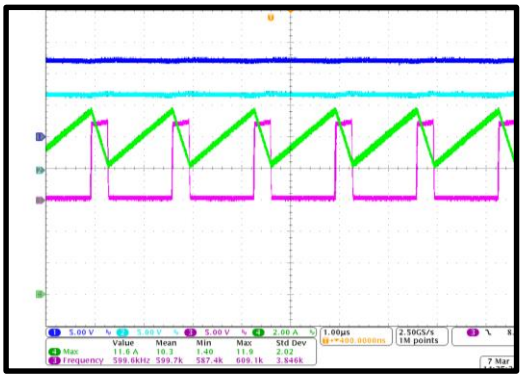
V_{BATT} OVP

Charge mode, V_{IN} = 5V, V_{BATT} = up to 4.4V, I_{CC} = 2A



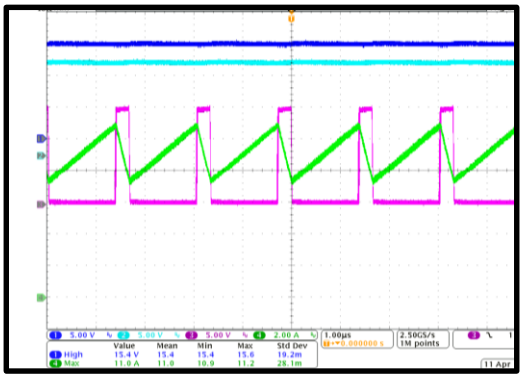
Boost Steady State Operation

Boost mode, V_{BST} = 12V, V_{BATT} = 3V, I_{BST} = 2A, I_{BST_LIMIT} = 3.65A



Boost Steady State Operation

Boost mode, V_{BST} = 15V, V_{BATT} = 3V, I_{BST} = 1.45A, I_{BST_LIMIT} = 3.65A

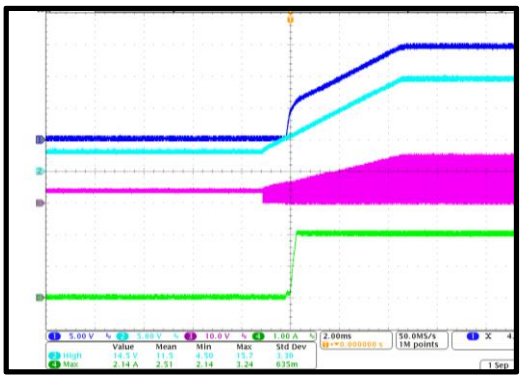


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{PMID} = 44µF, C_{IN} = 22µF, C_{SYS} = 22µF, C_{BATT} = 22µF, L = 1µH (DCR = 4.6mΩ), T_A = 25°C, unless otherwise noted.

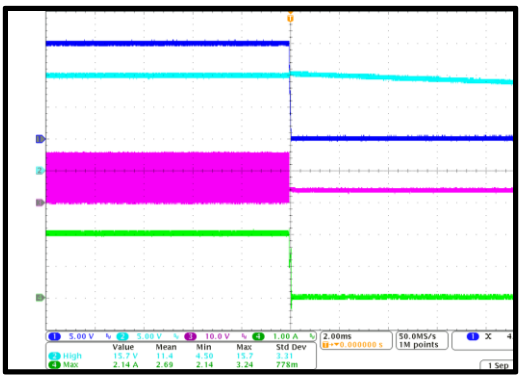
Boost Mode Enabled (Single Output)

Boost mode, V_{BST} = 15V, V_{BATT} = 3.5V, I_{BST} = 2A, I_{BST_LIMIT} = 3.65A



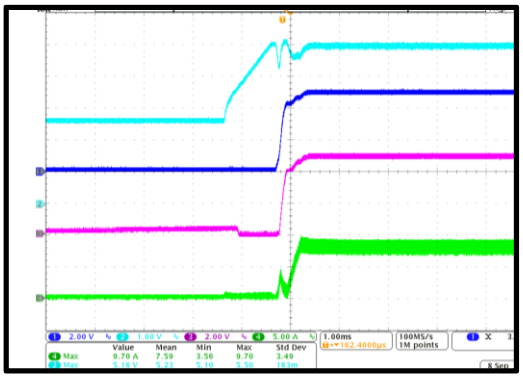
Boost Mode Disabled (Single Output)

Boost mode, V_{BST} = 15V, V_{BATT} = 3.5V, I_{BST} = 2A, I_{BST_LIMIT} = 3.65A



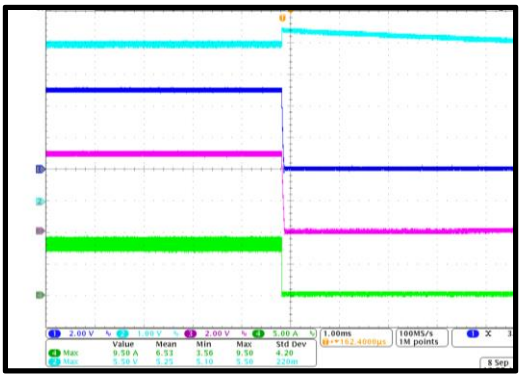
Boost Mode Enabled (Dual Output)

Boost mode, V_{BST} = 5V, V_{BATT} = 3V, I_{BST} = 2A, I_{BST_LIMIT} = 3.65A, Q2 is on, I_{SYS} = 2A



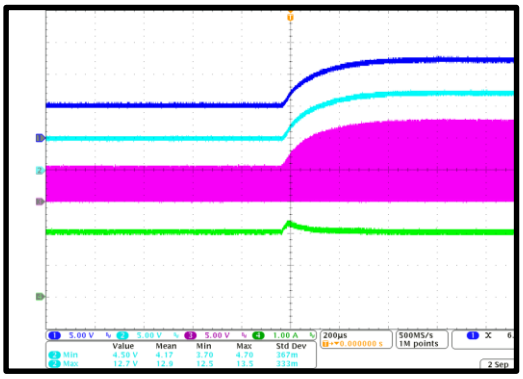
Boost Mode Disabled (Dual Output)

Boost mode, V_{BST} = 5V, V_{BATT} = 3V, I_{BST} = 2A, I_{BST_LIMIT} = 3.65A, Q2 is on, I_{SYS} = 2A



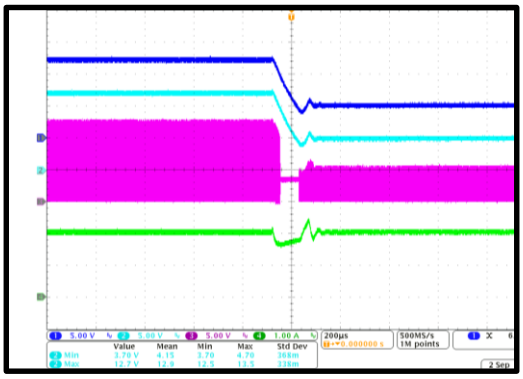
Boost Voltage Transient

Boost mode, V_{BST} = 5V to 12V, V_{BATT} = 3V, I_{BST} = 2A, I_{BST_LIMIT} = 3.65A



Boost Voltage Transient

Boost mode, V_{BST} = 12V to 5V, V_{BATT} = 3V, I_{BST} = 2A, I_{BST_LIMIT} = 3.65A

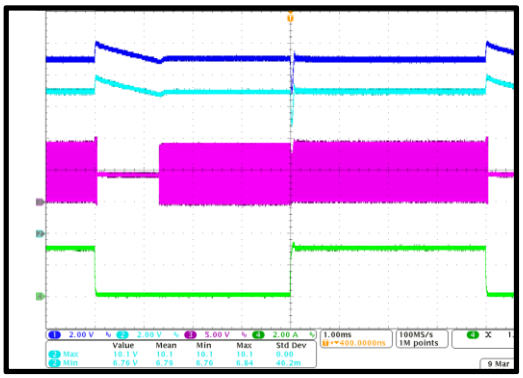


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, C_{PMID} = 44µF, C_{IN} = 22µF, C_{SYS} = 22µF, C_{BATT} = 22µF, L = 1µH (DCR = 4.6mΩ), T_A = 25°C, unless otherwise noted.

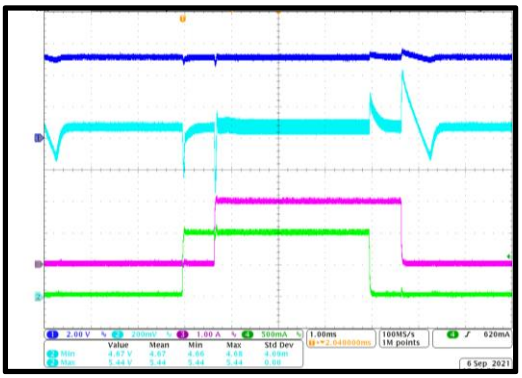
Boost Load Transient (Single Output)

Boost mode, V_{BST} = 9V, V_{BATT} = 4V,
I_{BST} = 0A to 3A, I_{BST_LIMIT} = 3.65A



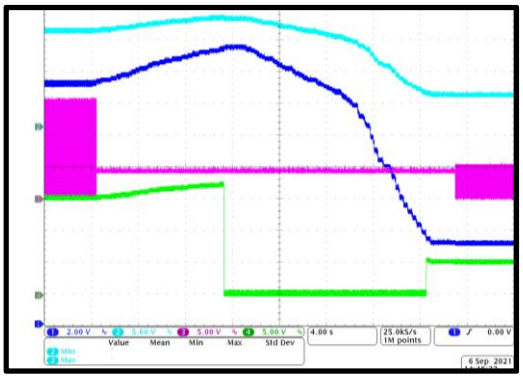
Boost Load Transient (Dual Output)

Boost mode, V_{BST} = 5V, V_{BATT} = 3V,
I_{BST} = 0A to 1A, I_{BST_LIMIT} = 3.65A, Q2 is on,
I_{SYS} = 0A to 2A



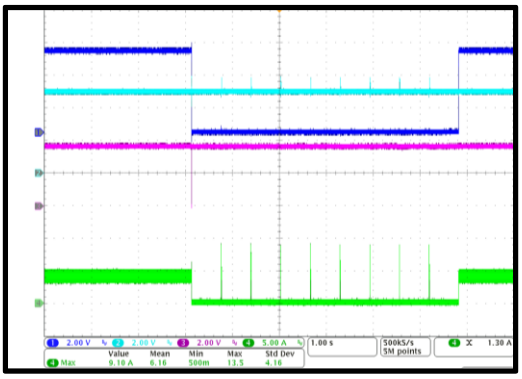
Boost OVP

Boost mode, V_{BST} = 15V, V_{BATT} = 4V,
I_{BST} = 100mA, I_{BST_LIMIT} = 3.65A, Q2 is on,
I_{SYS} = 100mA



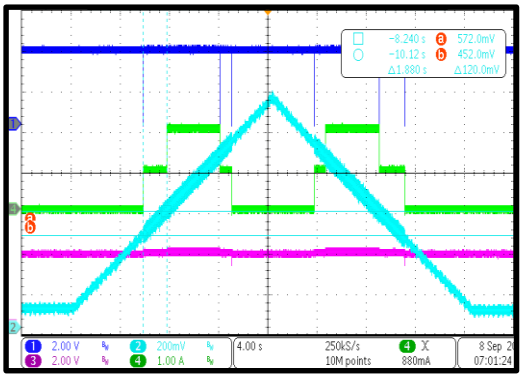
Boost Load SCP

Boost mode, V_{BST} = 5V, V_{BATT} = 4V, I_{BST} = 3A,
I_{BST_LIMIT} = 3.65A



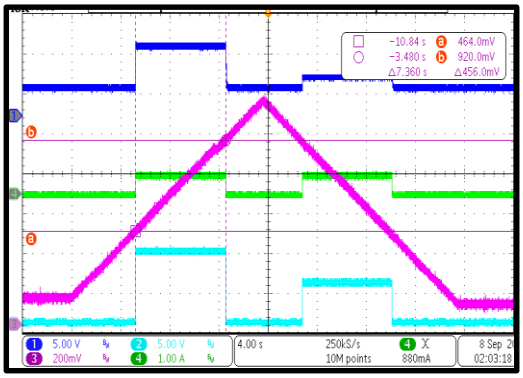
NTC Function in Charge Mode

Charge mode, V_{IN} = 5V, V_{BATT} = 3.5V, I_{CC} = 2A,
I_{IN_LIMIT} = 3500mA, JIETA_ISET = 50%,
JIETA_VSET = V_{BATT_REG} - 200mV



NTC Function in Boost Mode

Boost mode, V_{BST} = 9V, V_{BATT} = 4V,
I_{BST} = 100mA, I_{BST_LIMIT} = 3.65A



FUNCTIONAL BLOCK DIAGRAM

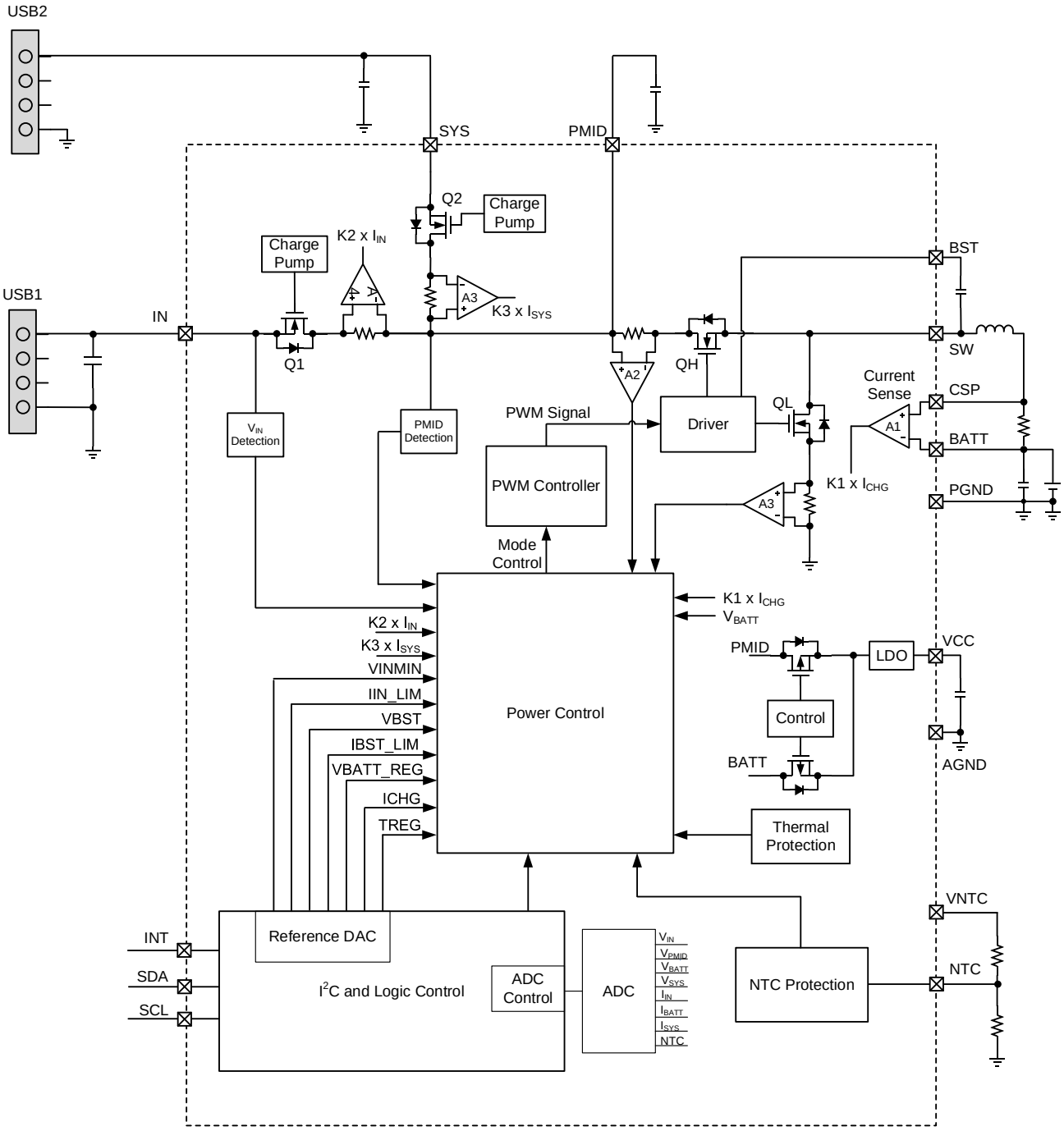


Figure 1: Functional Block Diagram

OPERATION

The MP2770 is an I²C-controlled switch-mode battery charger IC with bidirectional operation that steps up the battery voltage (V_{BATT}) to power the SYS or IN port. The MP2770 operates in charge mode, boost mode, or standby mode, depending on the input and output statuses. In charge mode, the IC can support a precision Li-ion or Li-polymer charging system in single-cell applications. In boost mode, the IC boosts V_{BATT} to a regulated voltage at the SYS or IN pin to power the load. In standby mode, the IC stops charging or boosting, and operates at a low current from either the input or the battery to reduce power consumption while the IC is not operating. The IC monitors the input and output devices to allow smooth transition between different operation modes.

Power Supply

The VCC pin provides power to the internal bias circuit and the low-side MOSFET (LS-FET) driver. VCC has an internal LDO with two inputs. One input is from PMID, and the other is from the battery. When the VCC voltage (V_{CC}) exceeds the V_{CC} UVLO threshold (V_{CC_UVLO}), the I²C interface is ready for communication and all the registers are reset to the default value.

Figure 2 shows the VCC power supply circuit.

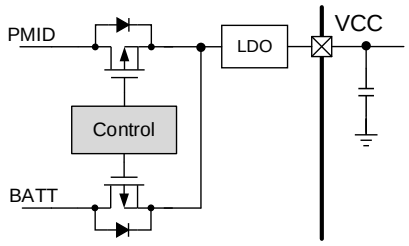


Figure 2: VCC Power Supply Circuit

Battery Charging Profile

The IC can run a charging cycle without host involvement. The host also can control the charge operations and parameters via the registers.

A new charge cycle starts when the following conditions are met:

- The input voltage (V_{IN}) exceeds the V_{IN} UVLO threshold (V_{IN_UVLO})
- V_{IN} is below V_{IN_UVLO}
- V_{IN} exceeds V_{BATT} plus the headroom voltage (V_{BATT} + V_{HDRM})
- The NTC pin voltage (V_{NTC}) is within the normal operating range
- No charge timer faults
- Charging is enabled (CONFIG[1:0] = 01)
- No battery over-voltage (OV) faults
- After 200ms delay completes

Charge Cycle

In charge mode, the IC has five control loops to regulate V_{IN}, the input current (I_{IN}), fast charge current (I_{CC}), charge termination voltage, and die temperature.

The IC provides three charging modes: pre-charge, constant current (CC), and constant voltage (CV).

Pre-Charge

When V_{IN} is good (i.e. above V_{IN_UVLO} and below V_{IN_OVP}), the IC checks V_{BATT} to determine whether pre-charging is required. The pre-charge current (I_{PRE}) can be configured via the I²C.

Constant Current (CC)

When V_{BATT} exceeds the battery pre-charge threshold (V_{BATT_PRE}), the IC enters CC mode (i.e. fast charging). I_{CC} can be configured to be up to 6A.

Constant Voltage (CV)

When V_{BATT} reaches the pre-configured battery regulation voltage (V_{BATT_REG}), I_{CC} begins to decrease.

The charge cycle completes when the following conditions are met:

- The IC works in CV charge mode
- I_{CC} is below the charge termination current (I_{TERM}) threshold for 200ms.

After termination, CHG_STAT[2:0] is set to 011, and an interrupt (INT) pulse is generated.

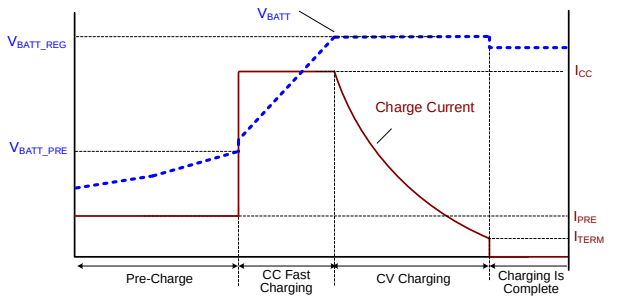


Figure 3: Battery Charging Profile

If I_{CC} does not reach I_{TERM} before the charging safety timer expires (see the Charging Safety Timer section), the changing stops, the CHGTMR_FAULT bit is set, and an INT pulse is generated.

During the entire charging process, the actual I_{CC} may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation, the input current limit (I_{IN_LIMIT}), V_{IN} limit loop regulation, or thermal regulation.

A new charge cycle starts once the following conditions are met:

- The input power is plugged in again
- Battery charging is enabled by the I²C
- V_{BATT} drops below the automatic recharge threshold once charging completes

Automatic Recharge

When charging completes, the battery may be discharged due to the system's consumption or self-discharge. If V_{BATT} is discharged below the recharge threshold and V_{IN} is valid, the IC automatically starts a new charging cycle without having to manually restart the charging cycle. The timer resets when the automatic recharge cycle begins.

Charging Safety Timer

The IC provides a charging safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer can be disabled via the I²C. The safety timer cannot operate in boost mode.

The safety timer is reset at the beginning of each new charging cycle. The following actions can restart the safety timer:

- A new charge cycle starts
- Write EN_TIMER to 1 (enables the safety timer)
- Write CONFIG[1:0] to 01 (enables charging)

The timer is suspended if one of the following faults occur:

- Battery over-voltage (OV) fault
- An NTC hot or cold fault

Input Voltage and Input Current Power Management

To meet the maximum current limit (I_{LIMIT}) specifications for USB applications, and to prevent overloading the adapter, the IC provides both V_{IN} and I_{IN} power management by continuously monitoring V_{IN} and I_{IN}. I_{IN_LIMIT} can be configured to prevent the input source from being overloaded. When I_{IN} reaches I_{IN_LIMIT}, I_{CC} decreases to prevent I_{IN} from increasing further.

If the set I_{IN_LIMIT} exceeds the adapter's rating, the back-up V_{IN} power management can prevent the input source from being overloaded. When V_{IN} drops to the V_{IN} regulation point due to a heavy load, I_{CC} reduces to prevent V_{IN} from dropping further.

Negative Temperature Coefficient (NTC) Thermistor

The VNTC pin is provided to pull-up the NTC resistor divider voltage when the IC is operating in boost charge mode. In this mode, the IC continuously monitors the battery temperature by measuring V_{NTC}. JEITA profile is also supported.

To initiate a charge cycle, V_{NTC} should be within the VHOT to VCOLD range. If V_{NTC} exceeds the VHOT to VCOLD range, charging is suspended until V_{NTC} is within the VHOT to VCOLD range.

At cool temperatures between VCOLD and VCOOL, I_{CC} or the charge voltage can be reduced by setting COOL_ACT[1:0]. The percentage by which I_{CC} is reduced can be set by JEITA_ISET[1:0]. The percentage by which the charge voltage is reduced can be set by JEITA_VSET[1:0].

At warm temperatures between VWARM and VHOT, I_{CC} or the charge voltage can be reduced by setting WARM_ACT[1:0]. The percentage by which I_{CC} is reduced can be set

by JEITA_ISET[1:0]. The percentage by which the charge voltage is reduced can be set by JEITA_VSET[1:0].

Figure 4 shows how to reduce I_{CC}.

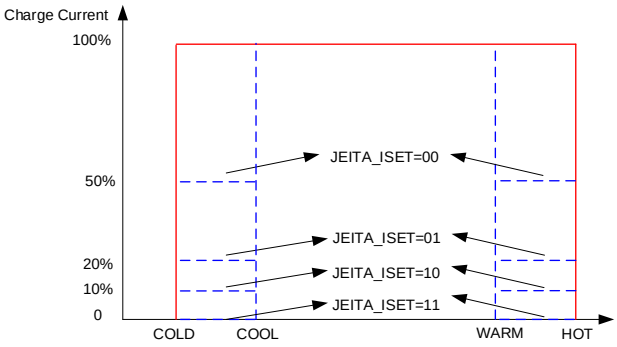


Figure 4: Reducing the Charge Current

Figure 5 shows how to reduce the charge voltage.

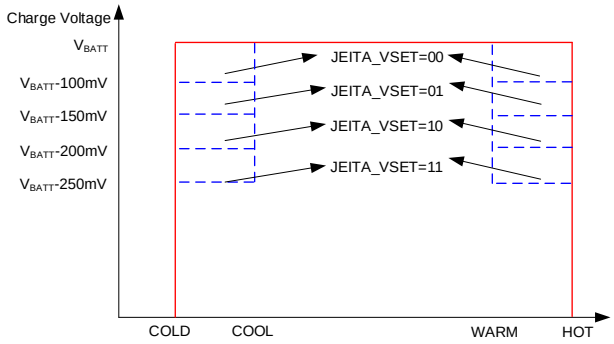


Figure 5: Reducing the Charge Voltage

The VCOLD, VCOOL, VWARM, and VHOT threshold have four configuration options.

For battery protection in boost mode, the device monitors V_{BATT}. V_{BATT} should be within the VCOLD to VHOT range. If V_{NTC} is outside of the VCOLD to VHOT range, then boost mode is suspended, and the NTC_FAULT bit is set to report the fault condition.

Once the temperature is within the cold to hot temperature range, boost mode resumes and the NTC_FAULT bit clears.

When the NTC_ACTION bit = 0, the boost charge mode is not suspended if V_{NTC} is outside of the VCOLD to VHOT range. Only an INT is asserted, and the NTC status is reported in NTC_FAULT.

Thermal Regulation and Thermal Shutdown in Charge Mode

The MP2770 continuously monitors the internal junction temperature (T_J) to maximize power delivery and prevent the device from overheating. If the internal T_J reaches the configurable thermal regulation threshold (T_{J_REG}), the MP2770 reduces I_{CC} to prevent high power dissipation. If T_J reaches 140°C, the converter shuts down. Once T_J drops to 120°C, the device resumes normal operation.

Interrupt (INT) to Host

The IC has an alert mechanism that outputs an interrupt (INT) signal via the INT pin to notify the system of an operation by outputting a 200μs, low-state INT pulse. There are six events that can trigger the INT output, described below:

- A good input source is detected
- A SYS load is plugged in
- Enters VINPPM or INPPM
- A status register change
- A fault register change
- No load is detected

See Table 1 on page 43 for more details.

Each event can be masked individually to avoid outputting an INT pulse via registers 0Ch and 0Dh.

The INT output is an open-drain that requires an external pull-up resistor in application.

Battery Over-Voltage Protection (OVP)

When V_{BATT} exceeds 104% of V_{BATT_REG}, the device stops charging, the BATT_OVP bit is set to 1, and an INT pulse is generated.

Input OVP

Once V_{IN} exceeds the V_{IN} over-voltage protection (OVP) threshold (V_{IN_OVP}), the DC/DC converter stops working, and both Q1 and Q2 turn off. V_{IN_OVP} can be set by VINOVP[1:0].

Boost Mode

The IC can supply a regulated output at the SYS or IN pin to power the load. Boost mode can be enabled once the following conditions are met:

- V_{BATT} exceeds the V_{BATT} UVLO threshold (V_{BATT_UVLO})
- V_{NTC} is within the proper range
- Boost mode is enabled (CONFIG = 11)
- After a 30ms delay once boost mode is enabled

Once boost mode is enabled, the IC boosts the PMID pin voltage (V_{PMID}) to the default voltage (5V), then Q1/Q2 is turned on linearly if enabled. The boost voltage (V_{BST}) should be set at the default voltage before boost mode is enabled. Once V_{IN} or V_{SYS} is exceeds 4.2V within 6ms, Q1/Q2 is fully turned on; otherwise, Q1/Q2 turns off and attempts to turn on again after 600ms.

The boost I_{LIMIT} (I_{BST_LIMIT}) can be set between 0.5A to 3.65A (with a 50mA step) by IBST_LIM[5:0]. When both IN and SYS output at the same time, the total output current (I_{OUT}) is limited by IBST_LIM[5:0].

In boost mode, the pulse-width modulation (PWM) step-up switching regulator switches from PWM mode to pulse-skip mode (PSM) under light-load conditions.

Battery Under-Voltage Lockout (UVLO)

In boost mode, once V_{BATT} drops below the V_{BATT_UVLO} falling threshold, the boost converter latches off, and IBST_LIM, VBST, and CONFIG are reset to the default values. Once the battery is charged again and V_{BATT} exceeds the V_{BATT_UVLO} rising threshold, the boost converter starts up again.

Boost Power Limitation

In boost mode, the battery discharge current can be configured by IBATT_DSG_LMT[2:0], which helps limit the maximum battery discharge current.

SYS Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

In boost mode, the MP2770 always monitors the current flowing through Q1 and Q2. If the Q1/Q2 I_{OUT} exceeds I_{BST_LIMIT}, the I_{OUT} loop takes control and V_{BST} drops. If V_{PMID} drops below both the the maximum value (4V) and (V_{BATT} + V_{BST_HDRM}), then Q1/Q2 turns off, IN_OC/SYS_OC is set high, and an INT pulse is generated. After a 600ms hiccup time, Q1/Q2 turns on again according to the start-up sequence. If V_{IN} or V_{SYS} exceeds 4.2V within 6ms, Q1/Q2 is fully turned on; otherwise, Q1/Q2 turns off again and repeats this procedure.

If the Q1/Q2 current exceeds the fast I_{LIMIT} (8A), then Q1/Q2 turns off, and IBST_LIM and VBST are reset to the default values. After Q1/Q2 turns off, Q1/Q2 starts up according to the start-up sequence.

If IN and SYS output at the same time, the V_{PMID} should be set at 5V by the host. If the (Q1 + Q2) current exceeds I_{BST_LIMIT}, the I_{OUT} loop takes control and V_{BST} drops. If V_{PMID} drops below both the maximum value (4V) and (V_{BATT} + V_{BST_HDRM}), then Q1 and Q2 turn off, IN_OC and SYS_OC are set high, and an INT pulse is generated. If the (Q1 + Q2) current exceeds 8A, then both Q1 and Q2 turn off. Q1 and Q2 start up again according to the start-up sequence.

Overload Capability

The MP2770 maintains a normal V_{BST} for 2ms if boost current (I_{BST}) is between the IBST_LIM[5:0] setting and 1.6 x IBST_LIM[5:0].

SYS Plug-In Detection

In standby mode, if the SYS_EN_PLUG bit is enabled, the SYS pin is pulled up to BATT via an internal 2kΩ resistor. Once V_{SYS} reaches 90% of V_{BATT}, the resistor switches to 5kΩ and SYS plug-in detection starts. Once V_{SYS} drops to 80% of V_{BATT}, a SYS plug-in is detected, the SYS_PLUG_IN bit is set to 1, and an INT pulse is generated.

The host must respond to the interrupt and enable the boost converter and Q2. The host must also clear the SYS_PLUG_IN bit for the next detection by disabling SYS_EN_PLUG and writing 0 to SYS_PLUG_IN.

No-Load Detection

In boost or pass-through mode, the Q2 current is monitored. If the Q2 current is below NOLOAD_THR[1:0] (between 30mA and 100mA), the NO_LOAD bit is set to 1 and an INT pulse is generated. The host can monitor the NO_LOAD bit to determine whether the boost converter or Q2 should be turned off.

Thermal Shutdown in Boost Mode

In boost mode, the device provides thermal shutdown by monitoring the internal T_J. If T_J reaches 140°C, the converter is shuts down. Once T_J drops to 120°C, the device resumes normal operation.

Pass-Through Mode

If a device connected at SYS port in charge mode, the MP2770 can operate in pass-through mode. In pass-through mode, the input provides power to charge the battery and provides power to the system via Q2.

When a device connected to the SYS port, a SYS plug-in is detected, the SYS_PLUG_IN bit is set to 1, and an INT pulse is generated. To prevent a high V_{IN} in pass-through mode that could damage the SYS port device, the host checks that V_{IN} is at 5V, and sets V_{IN_OVP} to 6.4V. Then the host can enable Q2 to provide power to the system. If enabled, Q2 turns on linearly. If V_{SYS} exceeds 4.2V within 6ms, Q2 is fully turned on; otherwise, Q2 turns off and attempts to turn on again after 600ms.

In pass-through mode, if I_{IN} reaches I_{IN_LIMIT} due to an increased system load, I_{CC} decreases to prevent I_{IN} from increasing further and to maintain the load. If V_{IN} drops below the V_{IN} regulation threshold due to a heavy load, I_{CC} decreases to prevent V_{IN} from dropping further.

The MP2770 provides protections in pass-through mode. If V_{IN} exceeds V_{IN_OVP}, charging stops and Q2 turns off. Once V_{IN} recovers to a normal value, the device starts charging again, and Q2 starts up according to the start-up sequence.

The MP2770 also features SYS over-current protection (OCP) in pass-through mode for SYS start-up fault or short conditions. If the Q2 current reaches the I_{LIMIT} (2.9A), Q2 is regulated at 2.9A within 6ms; otherwise, Q2 turns off. If the Q2 current exceeds the fast I_{LIMIT} (8A), Q2 turns off immediately. After a 600ms hiccup timer, Q2 turns on again. An INT pulse is generated, and the SYS_OC is set high until Q2 is fully turned on.

Standby Mode

When boost charging is disabled, the IC enters standby mode. In standby mode, all the MOSFETs and most of internal circuitry turn off to minimize the leakage and extend the battery's run time.

Watchdog Timer

The MP2770 can operate without host control when all of the registers are set to their default values. The MP2770 can also operate with host control, and has a watchdog timer to monitor the I²C interface actions. If the watchdog timer is enabled, the host must reset it periodically before it expires. If the watchdog timer expires, some of the registers reset to their default values. See the I²C Register Description section on page 26 for more details.

The following actions can reset the watchdog timer, allowing the IC to recover from a watchdog timer fault:

- Write to the WD_TIMER_RESET bit
- Toggle the WD bit (first disable the watchdog timer, then enable it again)

Analog-To-Digital Converter (ADC)

Conversion and Multiplexer

The MP2770 integrates an 8-bit ADC. In charge mode, V_{IN}, I_{IN}, V_{BATT}, I_{CC}, V_{PMID}, V_{SYS}, and V_{NTC} voltage are monitored. In boost mode, V_{IN}, V_{SYS} , V_{PMID}, V_{BATT}, I_{BST} (via the IN and SYS pins), the battery discharge current, and V_{NTC} are monitored. The ADC always works in continuous transfer mode while the device operates in charge mode or boost mode. If only the battery is present and the device is in standby mode, the ADC can be controlled by register 04h, bit[1:0].

One-Time Programmable (OTP) Memory

The MP2770 has one-time programmable (OTP) memory that allows the user to configure the default parameter values.

To configure the parameters via the OTP, set V_{IN} and V_{CC} to 5.2V, float BATT, and disable charging. Configure the default parameter values to the desired values, then write "1" to the OTP_BURN_IN bit. This bit is invalid after being configured once.

I²C INTERFACE

I²C Serial Interface

The MP2770 uses an I²C-compatible interface to flexibly set charging parameters and instantaneously report the device status. The I²C is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). Both the SDA and SCL lines are open drains that must be connected to the positive supply voltage using a pull-up resistor.

The IC operates as a slave device and receives control inputs from the master device, such as a microcontroller (MCU). The SCL line is always driven by the master device. The I²C interface supports both standard mode (up to 100kbps) and fast mode (up to 400kbps).

All transactions begin with a start (S) command and are terminated by a stop (P) command. Start and stop commands are always generated by the master. A start command is defined as a high-to-low transition on the SDA line while SCL is high. A stop command is defined as a low-to-high transition on the SDA line when the SCL is high (see Figure 6).

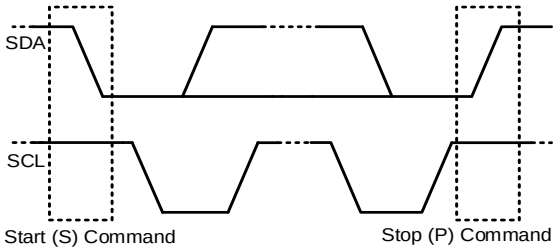


Figure 6: Start and Stop Commands

For data validity, the data on the SDA line must be stable during the high period of the clock. The high or low state of the SDA line can only change when the clock signal on the SCL line is low (see Figure 7). Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the most significant bit (MSB) first.

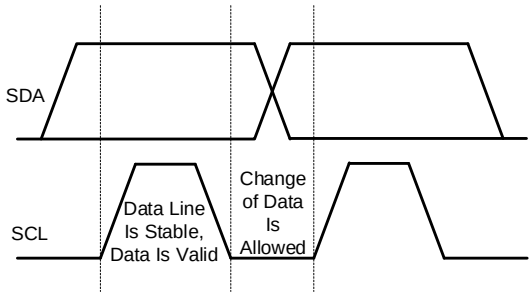


Figure 7: Bit Transfer on the I²C Bus

Each byte must be followed by an acknowledge (ACK) bit. The ACK bit is generated by the receiver to signal to the transmitter that the byte was successfully received.

The ACK signal is defined as when the transmitter releases the SDA line during the acknowledge clock pulse. This allows the receiver to pull the SDA line low, which remains low during the high period of the 9th clock pulse.

If the SDA line is high during the 9th clock pulse, this is considered a not acknowledge (NACK) signal. The master can then generate either a stop command to abort the transfer or a repeated start (Sr) command to start a new transfer.

A slave address is sent after the start command. This address is 7 bits long, followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). Figure 8 shows the address bit arrangement.

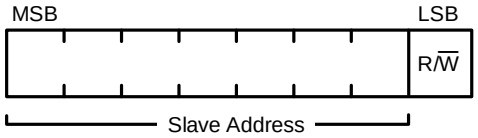


Figure 8: 7-Bit Addressing

See Figures 9–13 on page 26 for the detailed signal sequence examples. Figure 9 shows a data transfer on the I²C bus. Figure 10 shows a single write sequence. Figure 11 shows a single read sequence. Figure 12 shows a multi-write sequence. Figure 13 shows a multi-read sequence.

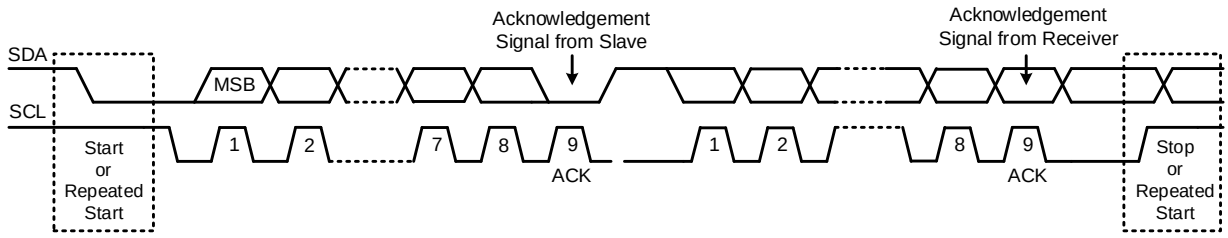


Figure 9: I²C Bus Data Transfer

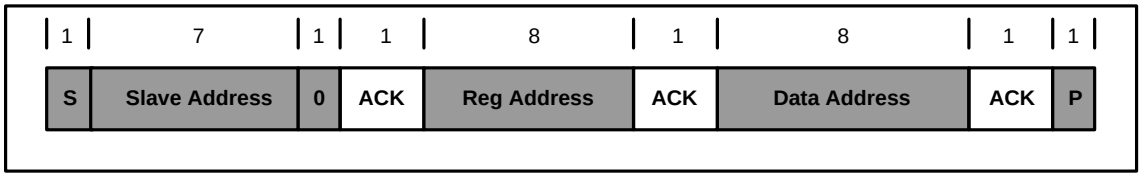


Figure 10: I²C Write Example (Write Single Register)

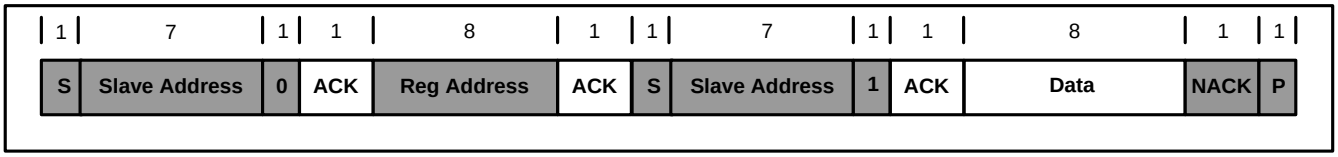


Figure 11: I²C Read Example (Read Single Register)

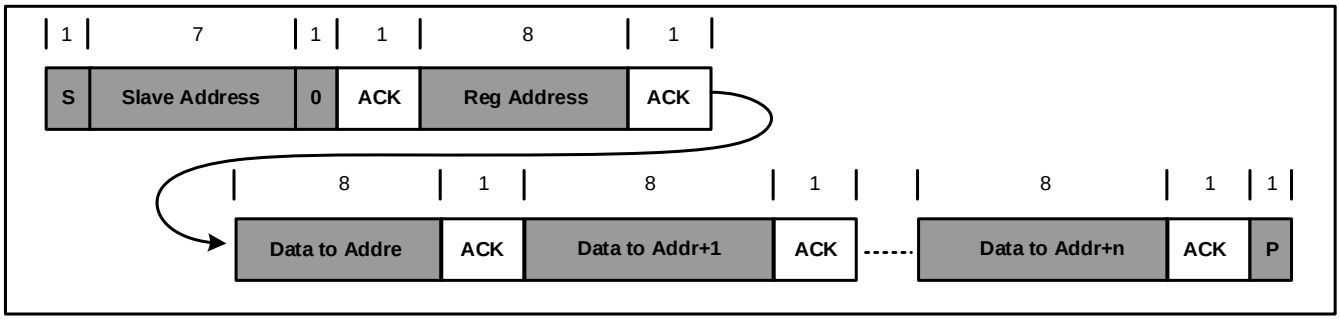


Figure 12: I²C Write Example (Write Multiple Registers)

Figure 13: I²C Read Example (Read Multiple Registers)

I²C REGISTER MAP

Register Name	Register Address	R/W	Description
REG00h	0x00	R/W	Minimum input voltage.
REG01h	0x01	R/W	Battery voltage regulation, input OVP, sense resistor, and termination current.
REG02h	0x02	R/W	Fast charge current and pre-charge current.
REG03h	0x03	R/W	Timers.
REG04h	0x04	R/W	Battery pre-charge threshold, NTC, ADC, and thermal regulation.
REG05h	0x05	R/W	Boost current limit.
REG06h	0x06	R/W	Boost voltage 1.
REG07h	0x07	R/W	Boost voltage 2.
REG08h	0x08	R/W	Charge configuration and input current limit.
REG09h	0x09	R/W	SYS load detection and discharge protection.
REG0Ah	0x0A	R/W	JEITA.
REG0Bh	0x0B	R/W	NTC action.
REG0Ch	0x0C	R/W	Interrupt mask 1.
REG0Dh	0x0D	R/W	Interrupt mask 2.
REG0Eh	0x0E	R	Status.
REG0Fh	0x0F	R	Fault 1.
REG10h	0x10	R	Fault 2.
REG11h	0x11	R	Input voltage ADC conversion (charge mode and boost mode).
REG12h	0x12	R	SYS voltage ADC conversion (boost mode).
REG13h	0x13	R	Battery voltage ADC conversion (charge mode and boost mode).
REG14h	0x14	R	Battery current ADC conversion (charge mode and boost mode).
REG15h	0x15	R	Q1 current ADC conversion (charge mode and boost mode).
REG16h	0x16	R	SYS current ADC conversion (boost mode).
REG17h	0x17	R	NTC ADC conversion (charge mode and boost mode).
REG18h	0x18	R	PMID ADC conversion (charge mode and boost mode).
REG19h	0x19	R/W	IC address and boost LS-FET peak current limit.
REG1Ah	0x1A	R/W	OTP configuration control register.

I²C REGISTER DESCRIPTION

Legend: POR = default value; WTD = watchdog; R/W = read/write; R = read-only, OTP-configurable = the register's default value can be configured via the OTP

Minimum Input Voltage (00h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	REG_RST	0	Yes	No	R/W	0: Keeps the current register settings 1: Resets the registers to their default values	This bit reset the registers to their default values. After reset, this bit go back to 0 automatically.
6	VIN_MIN[6]	0	Yes	No	R/W	7680mV.	These bits set the minimum V_{IN}. Offset: 3.12V Range: 3.12V to 18.36V Default: 4.44V OTP-configurable.
5	VIN_MIN[5]	0	Yes	No	R/W	3840mV.	
4	VIN_MIN[4]	0	Yes	No	R/W	1920mV.	
3	VIN_MIN[3]	1	Yes	No	R/W	960mV.	
2	VIN_MIN[2]	0	Yes	No	R/W	480mV.	
1	VIN_MIN[1]	1	Yes	No	R/W	240mV.	
0	VIN_MIN[0]	1	Yes	No	R/W	120mV.	

Battery Voltage Regulation, Input OVP, Sense Resistor, and Termination Current (01h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	RSNS	1	Yes	No	R/W	0: 5mΩ 1: 10mΩ	Default: 1 (10mΩ) OTP-configurable.
6	VINOVP[1]	1	Yes	No	R/W	00: 6.4V 01: 11.2V 10: 14V 11: 16.8V	These bits set V_{IN_OVP}. Default: 11 (16.8V) OTP-configurable.
5	VINOVP[0]	1	Yes	No	R/W		
4	VBATT_REG[2]	0	Yes	Yes	R/W	000: 3.6V 001: 4.1V 010: 4.15V 011: 4.2V 100: 4.3V 101: 4.35V 110: 4.4V 111: 4.45V	Default: 011 (4.2V) OTP-configurable.
3	VBATT_REG[1]	1	Yes	Yes	R/W		
2	VBATT_REG[0]	1	Yes	Yes	R/W		
1	ITERM[1]	0	Yes	Yes	R/W	00: 50mA 01: 100mA 10: 200mA 11: 400mA	Default: 01 (100mA) OTP-configurable.
0	ITERM[0]	1	Yes	Yes	R/W		

Fast Charge Current and Pre-Charge Current (02h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	ICC[5]	0	Yes	Yes	R/W	3200mA.	These bits set I_{CC}. Offset: 500mA Range: 500mA to 6A Default: 2000mA If I_{CC} exceeds 6A, the current is clamped at the register value, 110111 (6A). OTP-configurable.
6	ICC[4]	0	Yes	Yes	R/W	1600mA.	
5	ICC[3]	1	Yes	Yes	R/W	800mA.	
4	ICC[2]	1	Yes	Yes	R/W	400mA.	
3	ICC[1]	1	Yes	Yes	R/W	200mA.	
2	ICC[0]	1	Yes	Yes	R/W	100mA.	
1	IPRE[1]	0	Yes	Yes	R/W	00: 50mA 01: 100mA 10: 200mA 11: 400mA	Default: 01 (100mA) OTP-configurable.
0	IPRE[0]	1	Yes	Yes	R/W		

Timers (03h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	FSW[1]	0	Yes	Yes	R/W	00: 500kHz 01: 600kHz 10: 800kHz 11: 1000kHz	Default: 600kHz OTP-configurable.
6	FSW[0]	1	Yes	Yes	R/W		
5	WD_TIMER_RESET	0	Yes	No	R/W	0: Normal 1: Reset	Default: Normal This bit resets back to 0 after the timer resets.
4	WD[1]	0	Yes	No	R/W	00: Timer is disabled 01: 40s 10: 80s 11: 160s	These bits set the I²C watchdog timer. Default: 01 (40s) The watchdog timer is available in charge mode and boost mode. OTP-configurable.
3	WD[0]	1	Yes	No	R/W		
2	CHG_TMR[1]	1	Yes	Yes	R/W	00: 5hrs 01: 10hrs 10: 15hrs 11: 20hrs	These bits set the charger safety timer. Default: 11 (20hrs) It is whole charge stage include PRE, CC and CV. OTP-configurable.
1	CHG_TMR[0]	1	Yes	Yes	R/W		
0	EN_TIMER	1	Yes	Yes	R/W	0: Disabled 1: Enabled	This bit enables the charger safety timer. Default: 1 (enabled)

Battery Pre-Charge Threshold, NTC, ADC, and Thermal Regulation (04h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	EN_NTC	1	Yes	No	R/W	0: Disabled 1: Enabled	Default: 1 (enabled) If the NTC is disabled, then V_{NTC} is also disabled. OTP-configurable.
6	NTC_ACTION	1	Yes	No	R/W	0: Only issues an INT signal when V_{NTC} reaches the NTC threshold 1: INT and action	This bit sets the NTC action. Default: 1 OTP-configurable.
5	VBATT_PRE[1]	1	Yes	Yes	R/W	00: 2.5V 01: 2.8V 10: 3V 11: reserved	Default: 10 (3V)
4	VBATT_PRE[0]	0	Yes	Yes	R/W		
3	TJ_REG[1]	1	Yes	Yes	R/W	00: 60°C 01: 80°C 10: 100°C 11: 120°C	These bits set the thermal regulation threshold. Default: 11 (120°C)
2	TJ_REG[0]	1	Yes	Yes	R/W		
1	ADC_START	0	Yes	Yes	R/W	0: ADC conversion is not active 1: ADC conversion is active	Default: 0 This bit is only read when ADC_RATE = 1. This bit remains high during ADC conversion. This bit is self-reset if written to 1 when ADC_RATE = 0. In charge mode and boost mode, the ADC always works in continuous mode. When only the battery is present in standby mode, the ADC can be controlled by this bit.
0	ADC_RATE	0	Yes	Yes	R/W	0: One-shot conversion 1: Continuous conversion	Default: 0

Boost Current Limit (05h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VIN_DSG	0	Yes	No	R/W	0: V_{IN} discharge is disabled 1: V_{IN} discharge is enabled	This bit enables the dummy V_{IN} discharge from IN to GND. Default: 0 1000Ω dummy load

6	SYS_DSG	0	Yes	No	R/W	0: V_{SYS} discharge is disabled 1: V_{SYS} discharge is enabled	This bit enables the dummy V_{SYS} discharge from SYS to GND. Default: 0 1000Ω dummy load
5	IBST_LIM[5]	0	Yes	Yes	R/W	1600mA.	These bits set I_{BST_LIMIT}. Offset: 500mA Default: 500mA
4	IBST_LIM[4]	0	Yes	Yes	R/W	800mA.	
3	IBST_LIM[3]	0	Yes	Yes	R/W	400mA.	
2	IBST_LIM[2]	0	Yes	Yes	R/W	200mA.	
1	IBST_LIM[1]	0	Yes	Yes	R/W	100mA.	
0	IBST_LIM[0]	0	Yes	Yes	R/W	50mA.	

Boost Voltage 1 (06h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VBST[7]	0	Yes	Yes	R/W	10240mV.	Highest 8 bits of VBST[9:0]. Offset: 4.3V Range: 4.3V to 15V Default: 5V If V_{BST} is set above 16V (1001001001), it is clamped.
6	VBST[6]	0	Yes	Yes	R/W	5120mV.	
5	VBST[5]	0	Yes	Yes	R/W	2560mV.	
4	VBST[4]	0	Yes	Yes	R/W	1280mV.	
3	VBST[3]	1	Yes	Yes	R/W	640mV.	
2	VBST[2]	0	Yes	Yes	R/W	320mV.	
1	VBST[1]	0	Yes	Yes	R/W	160mV.	
0	VBST[0]	0	Yes	Yes	R/W	80mV.	

Boost Voltage 2 (07h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	RESERVED	-	-	-	-	-	-
6	RESERVED	-	-	-	-	-	-
5	BSTOVP[1]	0	Yes	No	R/W	00: 110% of V_{BATT_REG} 01: 115% of V_{BATT_REG} 10: 120% of V_{BATT_REG} 11: Reserved	These bits set the boost OVP threshold. Default: 01 (115% of V_{BATT_REG}) OTP-configurable.
4	BSTOVP[0]	1	Yes	No	R/W		

3	BSTOVP_EN	1	Yes	No	R/W	0: Disabled 1: Enabled	This bit enables boost OVP. Default: 1 (enabled) OTP-configurable.
2	VBST_SET	0	Yes	No	R/W	0: Internal DAC setting 1: External FB setting	This bit sets VBST. Default: 0 OTP-configurable.
1	VBST[9]	1	Yes	Yes	R/W	40mV.	Lowest 2 bits of VBST. Default: 11
0	VBST[8]	1	Yes	Yes	R/W	20mV.	

Charge Configuration and Input Current Limit (08h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	IIN_LIM[3]	0	Yes	No	R/W	0000: 500mA 0001: 900mA 0010: 1000mA 0011: 1200mA 0100: 1500mA 0101: 1800mA 0110: 2000mA 0111: 2100mA 1000: 2200mA 1001: 2400mA 1010: 2800mA 1011: 3000mA 1100: 3200mA 1101: 3500mA 1110: 3500mA 1111: 3500mA	These bits set I_{IN_LIMIT}. Default: 500mA OTP-configurable.
6	IIN_LIM[2]	0	Yes	No	R/W		
5	IIN_LIM[1]	0	Yes	No	R/W		
4	IIN_LIM[0]	0	Yes	No	R/W		
3	Q1_EN	1	Yes	No	R/W	0: Q1 is disabled 1: Q1 is enabled	This bit enables Q1. Default: 1 (Q1 is enabled) In boost mode, if this bit is disabled, VBST[9:0] is reset to the default value. OTP-configurable.
2	Q2_EN	0	Yes	No	R/W	0: Q2 is disabled 1: Q2 is enabled	This bit enables Q2. Default: 0 (Q2 is disabled) In boost mode, if this bit is disabled, VBST[9:0] is reset to the default value. OTP-configurable.
1	CONFIG[1]	0	Yes	Yes	R/W	00: Standby 01: Charge 10: Charge suspended 11: Boost	Default: 01 (charge)
0	CONFIG[0]	1	Yes	Yes	R/W		

SYS Load Detection and Discharge Protection (09h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	SYS_EN_PLUG	1	Yes	No	R/W	0: SYS plug-in detection is disabled 1: SYS plug-in detection is enabled	Default: 1 OTP-configurable.
6	SYS_PLUG_IN	0	Yes	No	R/W	0: SYS is not plugged in 1: A SYS plug-in is detected	When SYS_EN_PLUG is enabled, once the V_{SYS} drops below 80% of V_{BATT}, a SYS plug-in is detected, SYS_PLUG_IN is set to 1, and an INT signal is asserted. This bit can only be cleared when the host writes 0 to SYS_EN_PLUG and then to this bit. Default: 0
5	NOLOAD_THR[1]	0	Yes	No	R/W	00: 25mA 01: 50mA 00: 75mA 01: 100mA	These bits set the SYS no-load detection. Default: 01 (50mA)
4	NOLOAD_THR[0]	1	Yes	No	R/W		
3	IBATT_DSG_LIM[2]	1	Yes	No	R/W	000: IBATT_DSG_LIM is disabled 001: 5A 010: 5.5A 011: 6A 100: 6.5A 101: 7A 110: 7.5A 111: 8A	These bits set the battery discharge I_{LIMIT} in boost mode. Default: 101 (7A) OTP-configurable.
2	IBATT_DSG_LIM[1]	0	Yes	No	R/W		
1	IBATT_DSG_LIM[0]	1	Yes	No	R/W		
0	BATT_UVLO	0	Yes	No	R/W	0: 2.5V 1: 2.7V	Default: 0 (2.5V) OTP-configurable.

JEITA (0Ah)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VHOT[1]	0	Yes	No	R/W	00: 31% of V_{VNTC} (65°C) 01: 34% of V_{VNTC} (60°C) 10: 37.2% of V_{VNTC} (55°C) 11: 40.6% of V_{VNTC} (50°C)	These bits set the hot threshold. The thermistor is 103AT. Default: 01 (34% of V_{VNTC} [60°C]) OTP-configurable.
6	VHOT[0]	1	Yes	No	R/W		

5	VWARM[1]	0	Yes	No	R/W	00: 47.6% of V_{VNTC} (40°C) 01: 44.1% of V_{VNTC} (45°C) 10: 40.6% of V_{VNTC} (50°C) 11: 37.2% of V_{VNTC} (55°C)	These bits set the warm threshold. The thermistor is 103AT. Default: 01 (44.1% of V_{VNTC} [45°C]) OTP-configurable.
4	VWARM[0]	1	Yes	No	R/W		
3	VCOOL[1]	1	Yes	No	R/W	00: 72% of V_{VNTC} (0°C) 01: 70% of V_{VNTC} (5°C) 10: 67.2% of V_{VNTC} (10°C) 11: 64.3% of V_{VNTC} (15°C)	These bits set the cool threshold. The thermistor is 103AT. Default: 10 (67.2% of V_{VNTC} [10°C]) OTP-configurable.
2	VCOOL[0]	0	Yes	No	R/W		
1	VCOLD[1]	0	Yes	No	R/W	00: 74% of V_{VNTC} (-5°C) 01: 72% of V_{VNTC} (0°C) 10: 70% of V_{VNTC} (+5°C) 11: 67.2% of V_{VNTC} (+10°C)	These bits set the cold threshold. The thermistor is 103AT. Default: 01 (72% of V_{VNTC} [0°C]) OTP-configurable.
0	VCOLD[0]	1	Yes	No	R/W		

NTC Actions (0Bh)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	JEITA_VSET[1]	1	Yes	No	R/W	00: V_{BATT_REG} - 100mV 01: V_{BATT_REG} - 150mV 10: V_{BATT_REG} - 200mV 11: V_{BATT_REG} - 250mV	Default: 10 (V_{BATT_REG} - 200mV)
6	JEITA_VSET[0]	0	Yes	No	R/W		
5	JEITA_ISET[1]	0	Yes	No	R/W	00: 50% of I_{CC} 01: 20% of I_{CC} 10: 10% of I_{CC} 11: 0% of I_{CC}	Default: 00 (50% of I_{CC})
4	JEITA_ISET[0]	0	Yes	No	R/W		
3	WARM_ACT[1]	0	Yes	No	R/W	00: No action 01: Reduces V_{BATT_REG} 10: Reduces I_{CC} 11: Reduces both V_{BATT_REG} and I_{CC} when NTC is warm	These bits set the warm action. Default: 01 (reduces V_{BATT_REG})
2	WARM_ACT[0]	1	Yes	No	R/W		
1	COOL_ACT[1]	1	Yes	No	R/W	00: No action 01: Reduce V_{BATT_REG} 10: Reduces I_{CC} 11: Reduces both V_{BATT_REG} and I_{CC} when NTC is cool	These bits set the cool action. Default: 10 (reduces I_{CC})
0	COOL_ACT[0]	0	Yes	No	R/W		

Interrupt Mask 1 (0Ch)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VINOK_STAT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)

6	CHG_DONE	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
5	VDPM_STAT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
4	IDPM_STAT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
3	THERM_REG	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
2	TSD_FAULT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
1	WD_FAULT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
0	Q2_NO_LOAD	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)

Interrupt Mask 2 (0Dh)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	BATT_FAULT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
6	CHG TMR_ FAULT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
5	IN_OC	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
4	SYS_OC	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
3	BOOST_OV	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
2	RESERVED	0	Yes	No	R/W	-	-
1	SYS_PLUG_IN	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)
0	NTC_FAULT	0	Yes	No	R/W	0: Not masked 1: Masked	Default: 0 (not masked)

Status (0Eh)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VINOK_STAT	0	No	No	R	0: V_{IN} is not okay 1: V_{IN} is okay	Default: 0 (V_{IN} is not okay) Valid in charge mode and standby mode, otherwise it is 0.

6	CHG_STAT [2]	0	No	No	R	000: Not charging 001: Pre-charge mode 010: CC mode 100: CV mode 011: Charging complete	Default: 000 (not charging) Valid in charge mode
5	CHG_STAT [1]	0	No	No	R		
4	CHG_STAT [0]	0	No	No	R		
3	VINDPM_STAT	0	No	No	R	0: Normal 1: V_{IN} DPM	Default: 0 (normal) Valid in charge mode, otherwise it is 0.
2	IINDPM_STAT	0	No	No	R	0: Normal 1: I_{IN} DPM	Default: 0 (normal) Valid in charge mode, otherwise it is 0.
1	THERM_REG	0	No	No	R	0: Normal 1: Thermal regulation	Default: 0 (normal) Valid in charge mode, otherwise it is 0.
0	Q2_NO_LOAD	0	No	No	R	0: Normal 1: Q2 no load	This bit sets the Q2 no-load current threshold. Default: 0 (normal) Valid in pass-through mode and boost mode, otherwise it is 0.

Fault 1 (0Fh)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	RESERVED	-	-	-	-	-	-
6	RESERVED	-	-	-	-	-	-
5	INPUT_OV	0	No	No	R	0: Normal 1: An input over-voltage (OV) fault has occurred	Default: 0 (normal) Valid in charge mode. This bit shares INT and INT mask control of VINOK_STAT.
4	INPUT_ REMOVED/ UV	0	No	No	R	0: Normal 1: Input is removed, an under-voltage (UV) fault has occurred	Default: 0 (normal) Valid in charge mode. This bit shares INT and INT mask control of VINOK_STAT.
3	TSD_ FAULT	0	No	No	R	0: Normal 1: Thermal shutdown	Default: 0 (normal) Valid in charge mode and boost mode. In boost mode, when thermal shutdown occurs, the boost and Q1 (or Q2) are turned off, and VBST[9:0] is reset to the default value.

2	WD_FAULT	0	No	No	R	0: Normal 1: Watchdog timer expires	Default: 0 (normal) Valid in charge mode and boost mode.
1	BATT_ FAULT	0	No	No	R	0: Normal 1: A battery OV fault has occurred	Default: 0 (normal) Valid in charge mode.
0	CHGTMR _FAULT	0	No	No	R	0: Normal 1: Safety timer expires	Default: 0 (normal) Valid in charge mode.

An interrupt is asserted when any bit of this REG changes.

Fault 2 (10h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	RESERVED	-	-	-	-	-	-
6	IN_OC	0	No	No	R	0: Normal 1: A boost output OC fault on IN has occurred	Default: 0 (normal) Valid in boost mode. When an IN OC fault occurs, Q1 turns off, INT is asserted, and VBST[9:0] is reset to the default value.
5	SYS_OC	0	No	No	R	0: Normal 1: A boost output OC fault on SYS has occurred	Default: 0 (normal) Valid in boost mode and pass-through mode. In boost mode, when a SYS OC fault occurs, Q2 turns off, INT is asserted, and VBST[9:0] is reset to the default value.
4	BOOST OV	0	No	No	R	0: Normal 1: A boost OV fault has occurred	Default: 0 (normal) Valid in boost mode. When a boost OV fault occurs, Q1 (or Q2) turns off, INT is asserted, and VBST[9:0] is reset to the default value.
3	RESERVED	-	-	-	-	-	-
2	NTC_ FAULT[2]	0	No	No	R	Charge Mode: 000: Normal 001: NTC warm 010: NTC cool 011: NTC cold 100: NTC hot Boost Mode: 000: Normal 011: NTC cold 100: NTC hot	These bits set the NTC fault action. Default: 000 (normal) Valid in charge mode and boost mode. In boost mode, when an NTC fault occurs, the boost and Q1 (or Q2) are turned off, INT is asserted, and VBST[9:0] is reset to the default value.
1	NTC_ FAULT[1]	0	No	No	R		
0	NTC_ FAULT[0]	0	No	No	R		

An interrupt is asserted when any bit of this REG changes.

Input Voltage ADC Conversion (11h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VIN[7]	0	No	No	R	10240mV.	These bits set the V_{IN} ADC conversion value. Offset: 0V Range: 0V to 20.4V
6	VIN[6]	0	No	No	R	5120mV.	
5	VIN[5]	0	No	No	R	2560mV.	
4	VIN[4]	0	No	No	R	1280mV.	
3	VIN[3]	0	No	No	R	640mV.	
2	VIN[2]	0	No	No	R	320mV.	
1	VIN[1]	0	No	No	R	160mV.	
0	VIN[0]	0	No	No	R	80mV.	

SYS Voltage ADC Conversion (12h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VSYS[7]	0	No	No	R	10240mV.	These bits set the V_{SYS} ADC conversion value. Offset: 0V Range: 0V to 20.4V
6	VSYS[6]	0	No	No	R	5120mV.	
5	VSYS[5]	0	No	No	R	2560mV.	
4	VSYS[4]	0	No	No	R	1280mV.	
3	VSYS[3]	0	No	No	R	640mV.	
2	VSYS[2]	0	No	No	R	320mV.	
1	VSYS[1]	0	No	No	R	160mV.	
0	VSYS[0]	0	No	No	R	80mV.	

Battery Voltage ADC Conversion (13h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VBATT[7]	0	No	No	R	2560mV.	These bits set the V_{BATT} ADC conversion value. Offset: 0V Range: 0V to 5.1V
6	VBATT[6]	0	No	No	R	1280mV.	
5	VBATT[5]	0	No	No	R	640mV.	
4	VBATT[4]	0	No	No	R	320mV.	
3	VBATT[3]	0	No	No	R	160mV.	
2	VBATT[2]	0	No	No	R	80mV.	
1	VBATT[1]	0	No	No	R	40mV.	
0	VBATT[0]	0	No	No	R	20mV.	

Battery Current ADC Conversion (14h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	IBATT[7]	0	No	No	R	5120mA.	8 bits of I_{BATT} ADC conversion. Offset: 0A Range: 0A to 10.23A
6	IBATT[6]	0	No	No	R	2560mA.	
5	IBATT[5]	0	No	No	R	1280mA.	
4	IBATT[4]	0	No	No	R	640mA.	
3	IBATT[3]	0	No	No	R	320mA.	
2	IBATT[2]	0	No	No	R	160mA.	
1	IBATT[1]	0	No	No	R	80mA.	
0	IBATT[0]	0	No	No	R	40mA.	

Q1 Current ADC Conversion (15h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	IQ1[7]	0	No	No	R	2560mA.	8 bits of I_{Q1} ADC conversion. Offset: 0A Range: 0A to 5.115A
6	IQ1[6]	0	No	No	R	1280mA.	
5	IQ1[5]	0	No	No	R	640mA.	
4	IQ1[4]	0	No	No	R	320mA.	
3	IQ1[3]	0	No	No	R	160mA.	
2	IQ1[2]	0	No	No	R	80mA.	
1	IQ1[1]	0	No	No	R	40mA.	
0	IQ1[0]	0	No	No	R	20mA.	

SYS Current ADC Conversion (16h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	ISYS[7]	0	No	No	R	2560mA.	8 bits of I_{SYS} ADC conversion. Offset: 0A Range: 0A to 5.115A
6	ISYS[6]	0	No	No	R	1280mA.	
5	ISYS[5]	0	No	No	R	640mA.	
4	ISYS[4]	0	No	No	R	320mA.	
3	ISYS[3]	0	No	No	R	160mA.	
2	ISYS[2]	0	No	No	R	80mA.	
1	ISYS[1]	0	No	No	R	40mA.	
0	ISYS[0]	0	No	No	R	20mA.	

NTC ADC Conversion (17h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	NTC[7]	0	No	No	R	640mV.	8 bits of V_{NTC} ADC conversion. Offset: 0V Range: 0V to 1.28V
6	NTC[6]	0	No	No	R	320mV.	
5	NTC[5]	0	No	No	R	160mV.	
4	NTC[4]	0	No	No	R	80mV.	
3	NTC[3]	0	No	No	R	40mV.	
2	NTC[2]	0	No	No	R	20mV.	
1	NTC[1]	0	No	No	R	10mV.	
0	NTC[0]	0	No	No	R	5mV.	

PMID ADC Conversion (18h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	VPMID[7]	0	No	No	R	10240mV.	These bits set the V_{PMID} ADC conversion value. Offset: 0V Range: 0V to 20.4V
6	VPMID[6]	0	No	No	R	5120mV.	
5	VPMID[5]	0	No	No	R	2560mV.	
4	VPMID[4]	0	No	No	R	1280mV.	
3	VPMID[3]	0	No	No	R	640mV.	
2	VPMID[2]	0	No	No	R	320mV.	
1	VPMID[1]	0	No	No	R	160mV.	
0	VPMID[0]	0	No	No	R	80mV.	

IC Address and Boost LS-FET Peak Current Limit (19h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	RESERVED	0	No	No	-	-	-
6	RESERVED	0	No	No	-	-	-
5	RESERVED	0	No	No	-	-	-
4	I2C_PULL_UP	0	No	No	R/W	0: 1.8V 1: 3.3V	Default: 0 (1.8V) OTP.
3	LS_PK	1	No	No	R/W	0: 10.5A 1: 12A	Default: 1 (12A) OTP.
2	ADDR[2]	1	No	No	R/W	000: 44h 001: 45h 010: 46h 011: 47h 100: 48h 101: 49h 110: 4Ah 111: 4Bh	Default: 111 (4Bh) OTP.
1	ADDR[1]	1	No	No	R/W		
0	ADDR[0]	1	No	No	R/W		

OTP Configuration Control Register (1Ah)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	RESERVED	0	No	No	-	-	-
6	RESERVED	0	No	No	-	-	-
5	RESERVED	0	No	No	-	-	-
4	RESERVED	0	No	No	-	-	-
3	RESERVED	0	No	No	-	-	-
2	RESERVED	0	No	No	-	-	-
1	OTP_READ_BACK	0	No	No	R/W	0: Normal 1: Readback	Default: 0 (normal) This bit is self-clearing.
0	OTP_BUR_IN	0	No	No	R/W	0: Normal 1: Burn-in	Default: 0 (normal) This bit is self-clearing. Using this bit, the user can change the default value for OTP bits. Configure the bits to the desired values, then write this OTP_BURN_IN. Note that these bits only configurable once.

Other Controls (40h)

Bit	Name	POR	REG_RST Reset	WTD Reset	R/W	Description	Comment
7	RESERVED	0	No	No	-	-	-
6	RESERVED	0	No	No	-	-	-
5	RESERVED	0	No	No	-	-	-
4	RESERVED MFI_EN	0	No	No	R/W	0: Enabled 1: Disabled	This bit enables the MFI function. Default: 0 (enabled) OTP.
3	RESERVED BST_ DLY_EN	01	No	No	R/W	0: Disabled 1: Enabled	This bit enables the boost start-up delay. Default: 1 (enabled) OTP.
2	RESERVED	0	No	No	-	-	-
1	RESERVED	0	No	No	-	-	-
0	RESERVED	0	No	No	-	-	-

INTERRUPT TABLE

Table 1: Interrupt Table

Interrupt Name	Related Registers	Can Be Masked	Event
VINOK_STAT	VINOK_STAT changes to 1	Yes	VIN start-up sequence, when V_{IN} is good, an INT pulse is generated
CHG_DONE	CHG_STAT[1:0] changes to 11	Yes	Charging is terminated
VINDPM_STAT	VINDPM_STAT changes to 1	Yes	Enters V_{IN} regulation loop
IINDPM_STAT	IINDPM_STAT changes to 1	Yes	Enters I_{IN} regulation loop
THERM_REG	THERM_REG changes to 1	Yes	Thermal regulation starts
TSD_FAULT	TSD FAULT changes to 1	Yes	Thermal shutdown
WD_FAULT	WD_FAULT changes to 1	Yes	The watchdog timer expires
BATT_FAULT	BAT_FAULT changes to 1	Yes	A battery OV fault occurs
CHG TMR_FAULT	CHG_TMR FAULT changes to 1	Yes	The charge timer expires
BOOST_OV	BOOST_OV changes to 1	Yes	A boost OV fault occurs
IN_OC	IN_OC changes to 1	Yes	An OC fault occurs on the boost output via IN
SYS_OC	SYS_OC changes to 1	Yes	An OC fault occurs on the boost output via SYS or a SYS OC fault occurs in passthrough mode
Q2_NO_LOAD	NO_LOAD 0 changes to 1	Yes	No load is detected on SYS
SYS_PLUG_IN	SYS_PLUG_IN 0 changes to 1	Yes	SYS port load is plugged in
NTC_FAULT	NTC1_FAULT[2:0] changes	Yes	Hot/warm/cool/cold entry

OTP REGISTER MAP (FOR USER PAGE)

Register #	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
00h		VINMIN[6]	VINMIN[5]	VINMIN[4]	VINMIN[3]	VINMIN[2]	VINMIN[1]	VINMIN[0]
01h	RSNS	VINOVP[1]	VINOVP[0]	VBATT_REG[2]	VBATT_REG[1]	VBATT_REG[0]	ITERM[1]	ITERM[0]
02h	ICC[5]	ICC[4]	ICC[3]	ICC[2]	ICC[1]	ICC[0]	IPRE[1]	IPRE[0]
03h	FSW[1]	FSW[0]		WD[1]	WD[0]	CHG_TMR[1]	CHG_TMR[0]	
04h	EN_NTC	NTC_ ACTION						
07h			BSTOVP[1]	BSTOVP[0]	BSTOVP_EN	VBST_SET		
08h	IIN_LIM[3]	IIN_LIM[2]	IIN_LIM[1]	IIN_LIM[0]	Q1_EN	Q2_EN		
09h	SYS_EN_ PLUG				IBATT_DSG_ LIM[2]	IBATT_DSG_ LIM[1]	IBATT_DSG_ LIM[0]	BATT_ UVLO
0Ah	VHOT[1]	VHOT[0]	VWARM[1]	VWARM[0]	VCOOL[1]	VCOOL[0]	VCOLD[1]	VCOLD[0]
19h				I2C_PULL_UP	LS_PK	ADDR[2]	ADDR[1]	ADDR[0]
40h				MFI_EN	BST_DLY_EN			

DEFAULT OTP CONFIGURATIONS

Table 2: Default OTP Configurations

OTP Items	Default
VINMIN	4.44V
RSNS	10mΩ
VINOVP	16.8V
VBATT_REG	4.2V
ITERM	100mA
ICC	2A
IPRE	100mA
FSW	600kHz
WD	40s
CHG_TMR	20hrs
EN_NTC	Enable
NTC_ACTION	INT and Action
BSTOVP	115% of V_{BATT_REG}
BSTOVP_EN	Enabled
VBST_SET	Internal DAC setting
IIN_LIM	500mA
Q1_EN	Enabled
Q2_EN	Disabled
SYS_EN_PLUG	Enabled
IBATT_DSG_LIM	7A
BATT_UVLO	2.5V
VHOT	34% of V_{VNTC}
VWARM	44.1% of V_{VNTC}
VCOOL	67.2% of V_{VNTC}
VCOLD	72% of V_{VNTC}
I2C_PULL_UP	1.8V
LS_PK	12A
ADDR	4Bh
MFI_EN	Enabled
BST_DLY_EN	Enabled

APPLICATION INFORMATION

NTC Function

JEITA profile is supported for battery temperature management. For a given NTC thermistor, choose appropriate R_{T1} and R_{T2} values to set the NTC window. R_{T1} can be calculated with Equation (1):

$$R_{T1} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{COLD} \times V_{HOT} \times (R_{NTC\_COLD} - R_{NTC\_HOT})} \quad (1)$$

Where R_{NTC_HOT} is the NTC resistance at the upper end of the operating temperature range, R_{NTC_COLD} is the lower end of the operating temperature range, V_{HOT} is the hot temperature threshold (selected via VHOT[1:0]), and V_{COLD} is the cold temperature threshold (selected via VCOLD[1:0]).

R_{T2} can be calculated with Equation (2):

$$R_{T2} = \frac{R_{NTC\_HOT} \times R_{NTC\_COLD} \times (V_{COLD} - V_{HOT})}{V_{HOT} \times (1 - V_{COLD}) \times R_{NTC\_COLD} - V_{COLD} \times (1 - V_{HOT}) \times R_{NTC\_HOT}} \quad (2)$$

The warm temperature threshold (V_{WARM}) can be calculated with Equation (3):

$$V_{WARM} = \frac{R_{T2} \times R_{NTC\_WARM}}{R_{T1} \times (R_{T2} + R_{NTC\_WARM}) + R_{T2} \times R_{NTC\_WARM}} \quad (3)$$

The cool temperature threshold (V_{COOL}) can be calculated with Equation (3):

$$V_{COOL} = \frac{R_{T2} \times R_{NTC\_COOL}}{R_{T1} \times (R_{T2} + R_{NTC\_COOL}) + R_{T2} \times R_{NTC\_COOL}} \quad (4)$$

Using the results from the calculations in Equation (3) and Equation (4), select the nearest warm/cool threshold in register 0Ah.

If an external NTC is not available, connect R_{T1} and R_{T2} together to keep V_{NTC} within the valid NTC window (e.g. R_{T1} = R_{T2} = 10kΩ).

Selecting the Inductor

Selecting the inductor is a tradeoff between cost, size, and efficiency. A smaller inductor provides a lower inductance, but results in a higher current ripple, magnetic hysteretic losses, and output capacitance. A larger inductor provides a lower ripple current and smaller output filter capacitance, but result higher inductor DC resistance (DCR) loss.

The required inductance (L) can be estimated with Equation (5):

$$L = \frac{V_{IN} - V_{BATT}}{\Delta I_{L\_MAX}} \frac{V_{BATT}}{V_{IN} \times f_{SW}(MHz)} (\mu H) \quad (5)$$

Where V_{IN} is the input voltage, V_{BATT} is the converter's V_{OUT}, f_{SW} is the switching frequency, and ΔI_{L_MAX} is the maximum peak-to peak inductor current (typically between 20% and 40% of the maximum load current).

$$I_{PEAK} = I_{LOAD\_MAX} \times (1 + \frac{\Delta I_{LOAD\_MAX}}{2})(A) \quad (6)$$

When the device is operating across the entire 5V and 12V V_{IN} range, the maximum inductor current ripple occurs between pre-charge and CC mode (V_{BATT} =3V). For most applications, the maximum I_{CC} can be set to 6A, which gives enough margin to avoid exceeding the HS-FET peak I_{LIMIT} (I_{PEAK_HS}). To ensure loop stability, choose the inductor to be between 1µH and 3µH. Choose an inductor that does not saturate under the worst-case load condition. The inductor's saturation current should be exceed the peak current calculated with Equation (6).

Selecting the PMID Capacitor

Choose C_{PMID} based on the V_{PMID} ripple and current ripple.

Charge Mode

In charge mode, the PMID capacitor (C_{PMID}) acts as the buck converter's input capacitor. C_{PMID} can be calculated with Equation (7):

$$C_{PMID} = I_{IN} \times \frac{(V_{IN} - V_{BATT})}{\Delta V_{IN} \times V_{IN} \times f_{SW}} \quad (7)$$

Where ΔV_{IN} is the input voltage ripple (typically 1% of V_{IN}).

The input ripple current (I_{RMS_MAX}) can be calculated with Equation (8):

$$I_{RMS\_MAX} = I_{CC\_MAX} \times \frac{\sqrt{V_{BATT} \times (V_{IN} - V_{BATT})}}{V_{IN}} \quad (8)$$

Boost Mode

C_{PMID} is the boost converter's output capacitor. C_{PMID} keeps the system voltage ripple low and ensures feedback loop stability. In boost mode, C_{PMID} can be calculated with Equation (9):

$$C_{PMID} = I_{SYS} \times \frac{(V_{SYS} - V_{BATT})}{\Delta V_{SYS} \times V_{SYS} \times f_{SW}} \quad (9)$$

Where ΔV_{SYS} is the SYS input voltage ripple (typically 1% of V_{SYS}).

I_{RMS_MAX} can be calculated with Equation (10):

$$I_{RMS\_MAX} = I_{BATT} \times \frac{\sqrt{V_{BATT} \times (V_{SYS} - V_{BATT})}}{V_{SYS}} \quad (10)$$

Choose C_{PMID} to meet both the charge mode and boost mode specifications. Ensure that the ripple current temperature rise does not exceed 10°C. For the best results, use low-ESR ceramic capacitors with X5R dielectrics and small temperature coefficients.

For most applications, use three ≥22µF or PMID capacitors.

Current-Sense Compensation

The soldering tin has resistance. For a 10mΩ resistor soldered to the PCB, the total resistance between the resistor pads is between 11mΩ and 12mΩ.

Connect a resistor divider between the CSP and BATT pins for current-sense compensation.

After the PCB is assembled, apply a 2A DC current source between SW and BATT. Measure the voltage drop (V_{CS}) across the current-sense resistor on the PCB pad. Then R1 can be calculated with Equation (11):

$$R1 = \frac{V_{CS} - 2 \times RS1}{2 \times RS1} \times 10\Omega \quad (11)$$

Figure 14 shows current-sense compensation.

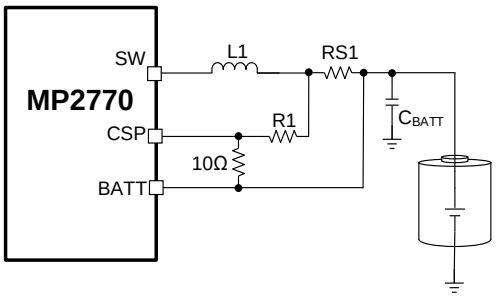


Figure 14: Current-Sense Compensation

PCB Layout Guidelinse

Efficient PCB layout is critical for stable operation (especially to meet the specified noise and efficiency requirements). For the best results, refer to Figure 15 and follow the guidelines below:

1. Place the PMID capacitor as close to PMID and PGND as possible using short, direct traces. Make this path as short as possible.
2. Place the BST capacitor between BST and SW. Make this path as short as possible.
3. Place the BST capacitor as close to the IC as possible.
4. Connect the IC's AGND and PGND together. Make this connection as close to the AGND port as possible.
5. Keep the switching node short.
6. Connect the VIN, PMID, SYS, and PGND power pads to as many coppers planes on the board as possible to improve thermal performance by dissipating heat to the PCB.

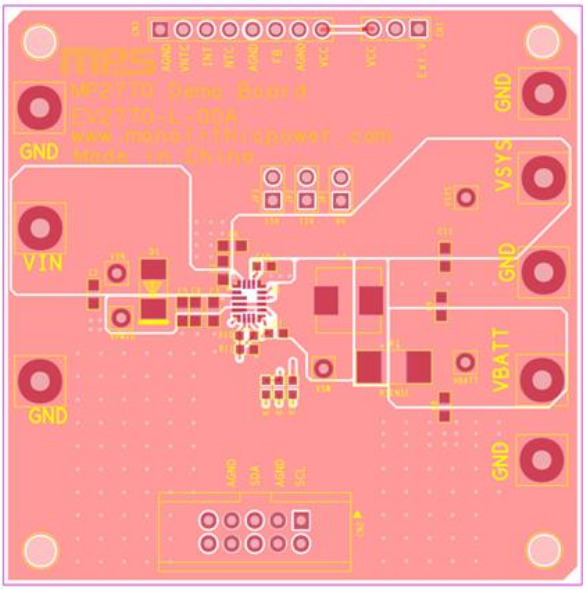


Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

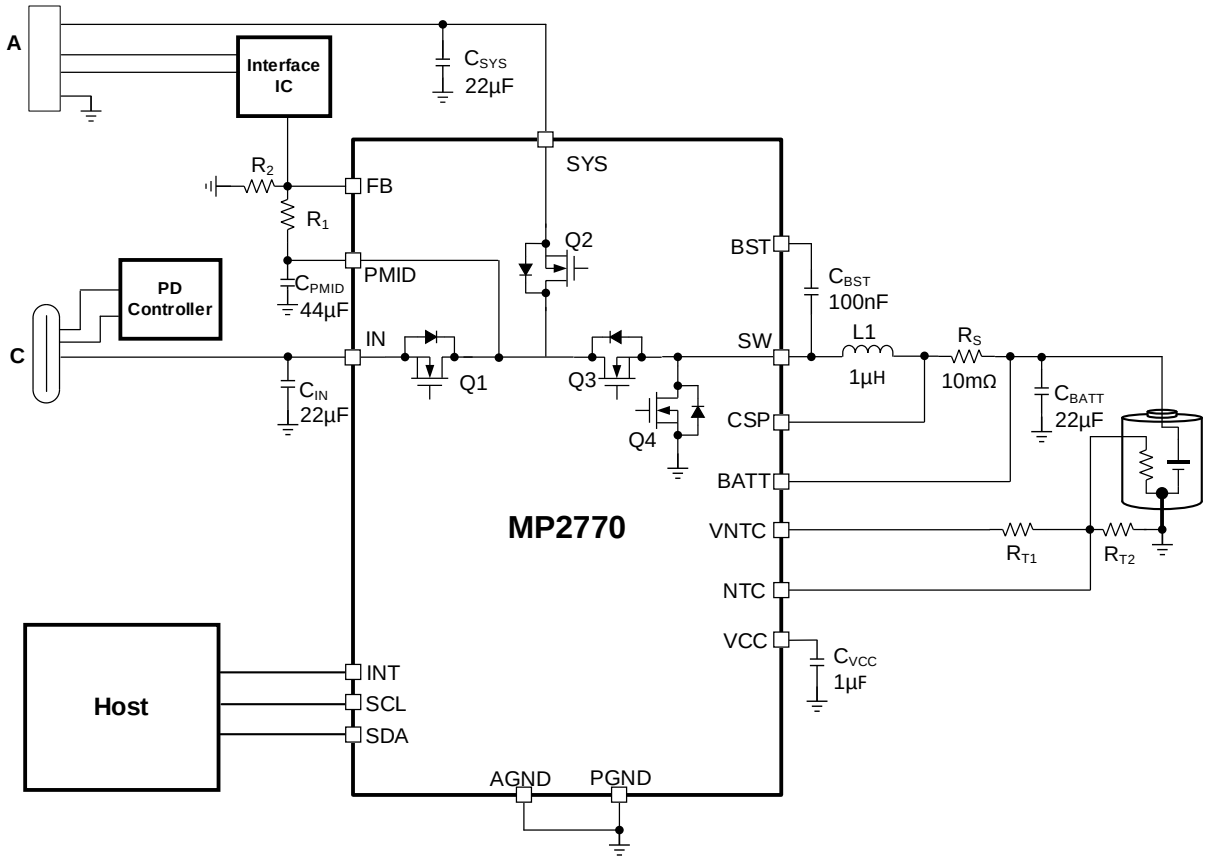


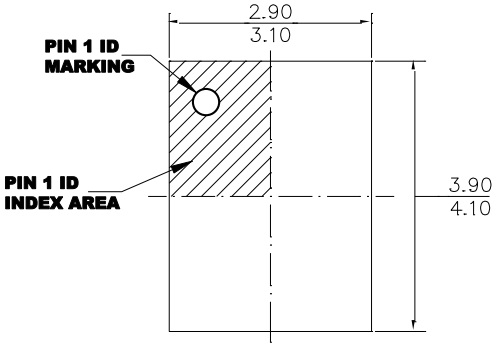
Figure 16: Typical Application Circuit

Table 3: Typical Application Bill of Materials

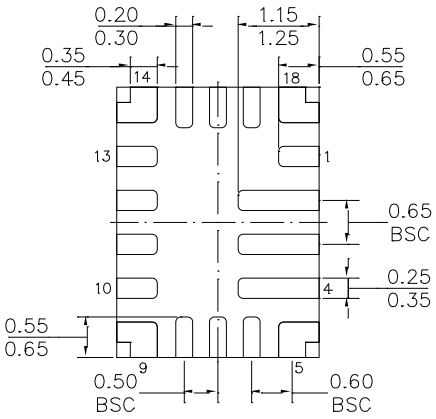
Qty	Ref	Value	Description	Package	Manufacturer
1	C_{IN}	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
2	C_{PMID}	22µF x 2	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C_{SYS}	22µF	Ceramic capacitor, 25V, X5R or X7R	0805	Any
1	C_{BATT}	22µF	Ceramic capacitor, 10V, X5R or X7R	0805	Any
1	C_{VCC}	1µF	Ceramic capacitor, 10V, X5R or X7R	0603	Any
1	C_{BST}	100nF	Ceramic capacitor, 25V, X5R or X7R	0603	Any
1	L1	1µH	Inductor, 1µH, Low DCR	SMD	Any
1	RS1	10mΩ	Film resistor, 1%	1206	Any

PACKAGE INFORMATION

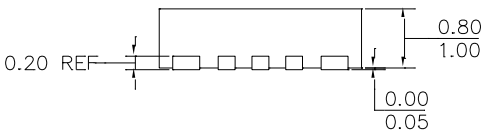
QFN-18 (3mmx4mm)



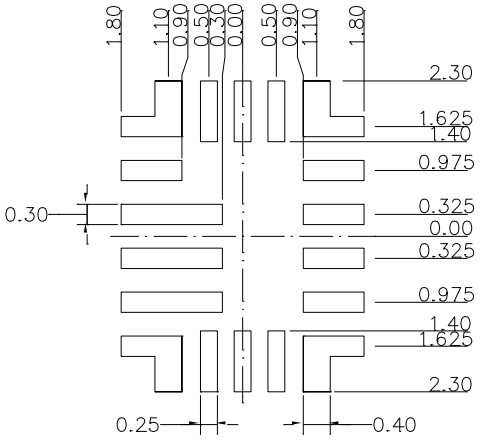
TOP VIEW



BOTTOM VIEW



SIDE VIEW

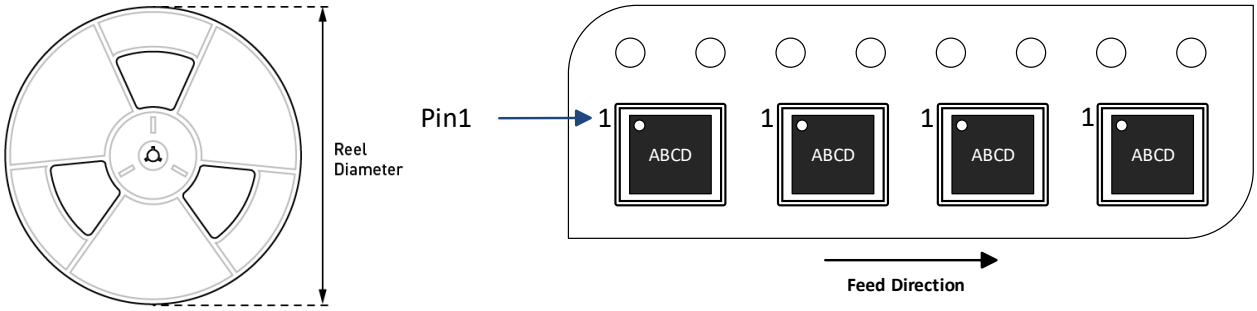


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP2770GL-xxxx-Z	QFN-18 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	4/11/2023	Initial Release	-