MP28167-N

2.8V to 22V V_{IN}, 3A I_{OUT}, Integrated Buck-Boost Converter with Four MOSFETS and PG Indication

DESCRIPTION

The MP28167-N is an integrated, synchronous buck-boost converter with four MOSFETs capable of regulating the output voltage (V_{OUT}) across a wide 2.8V to 22V input voltage (V_{IN}) range with high efficiency. The integrated V_{OUT} scaling and adjustable output constant current (CC) limit functions meet USB power delivery (PD) requirements.

The MP28167-N uses constant-on-time (COT) control in buck mode and constant-off-time control in boost mode, providing fast load transient response and smooth buck-boost mode transient. The MP28167-N provides automatic pulse-frequency modulation (PFM)/pulse-width modulation (PWM) mode and forced PWM mode. It also provides a configurable output CC limit, which supports flexible design for different applications.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), configurable soft start (SS), and thermal shutdown.

The MP28167-N is available in a QFN-16 (3mmx3mm) package.

FEATURES

- Configurable Output Voltage (V_{OUT}) via the Feedback (FB) Pin
- Wide 2.8V to 22V Operating Input Voltage (V_{IN}) Range
- 0.08V to 1.637V Reference Voltage (V_{REF}) Range with 0.8mV Resolution via the Digital Interface (1) (Default 1V V_{REF})
- Up to 3A Output Current (I_{OUT}) or 4A Input Current (I_{IN})
- Four Low On Resistance ($R_{DS(ON)}$), Internal Buck Power MOSFETs
- Adjustable Accurate Output Constant Current (CC) Limit with Internal Sensing MOSFET via the Digital Interface
- 500kHz, 750kHz, 1MHz, or 1.25MHz Selectable Switching Frequency (f_{SW})
- Output Over-Voltage Protection (OVP) with Hiccup Mode
- Output Short-Circuit Protection (SCP) with Hiccup Mode
- Over-Temperature Warning and Shutdown
- Power Good (PG) Indication
- One-Time Programmable Non-Volatile Memory
- Configurable via the Digital Interface: Line Drop Compensation, PFM/PWM Mode, Soft Start (SS), OCP, and OVP
- Configurable Enable (EN) Shutdown Discharge
- Available in a QFN-16 (3mmx3mm) Package

MPL Optimized Performance with MPS Inductor MPL-AL6050 Series

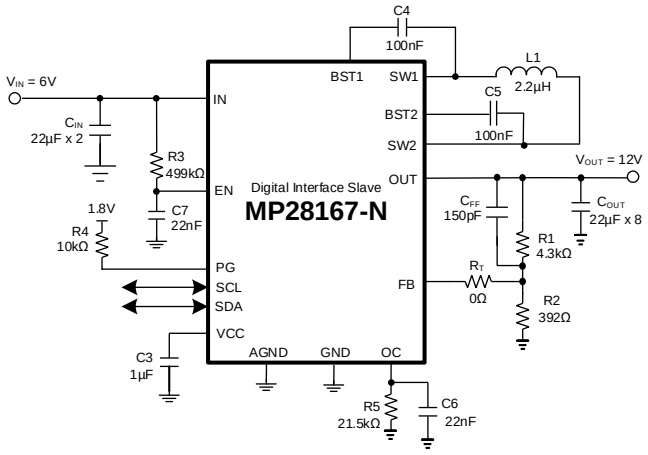
APPLICATIONS

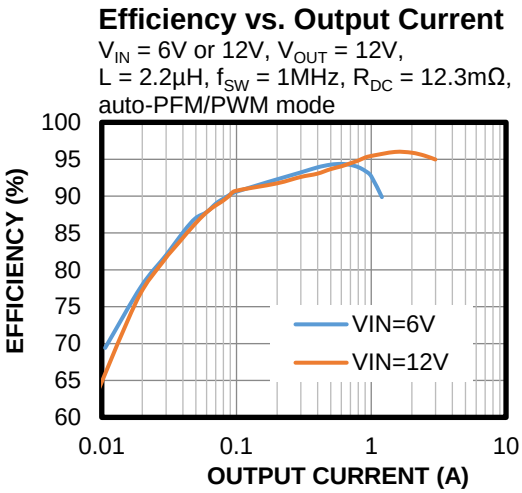
- Solid-State Drives (SSDs)
- USB Power Delivery (PD) Sourcing Ports
- Buck-Boost Bus Supplies
- Networking and Servers

Note:

1) f_{SW} decreases for applications where V_{OUT} is below 3V.

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP28167GQ-N	QFN-16 (3mmx3mm)	*See Below*	1
EVKT-MP28167-N	Evaluation kit		

* For Tape & Reel, add suffix -Z (e.g. MP28167GQ-N-Z).

TOP MARKING

$\overline{\text{CAVY}}$
LLLL

CAV: Product code of MP28167GQ-N
Y: Year code
LLLL: Lot number

EVALUATION KIT EVKT-MP28167-N

EVKT-MP28167-N kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV28167-N-Q-00A	MP28167-N evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to digital interface, one USB cable, and one ribbon cable	1

Order directly from MonolithicPower.com or our distributors.

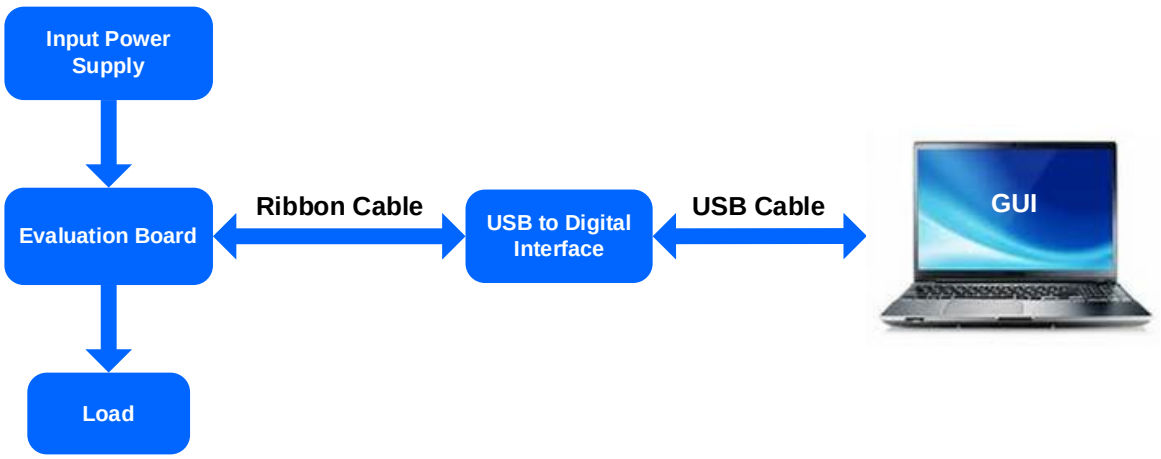
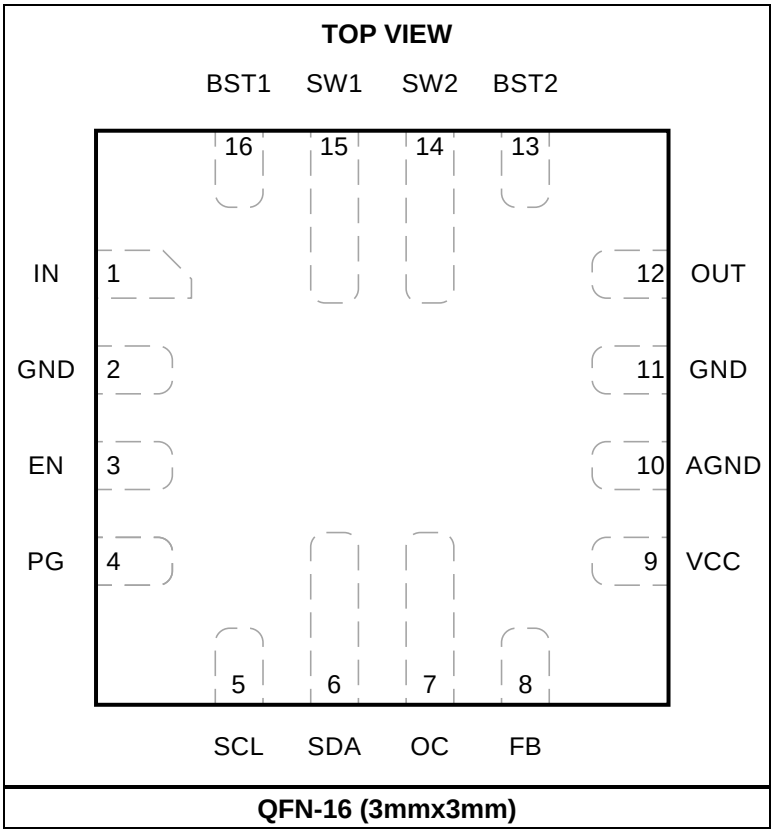


Figure 1: EVKT-MP28167-N Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	IN	**Input voltage.** IN is the drain of the internal power device, and provides power to the entire chip. The MP28167-N operates from a 2.8V to 22V input voltage (V_{IN}) range. A capacitor (C_{IN}) is required to prevent large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
2, 11	GND	**Power ground.** GND is the reference ground of the regulated output voltage (V_{OUT}). GND requires extra consideration during PCB layout. Connect GND using copper traces and vias.
3	EN	**On/off control for the entire device.** Pull EN high to turn the converter on; pull EN low or float EN to turn it off. EN has an internal 2MΩ pull-down resistor connected to ground.
4	PG	**Power good output.** PG indicates the V_{OUT} status.
5	SCL	**Digital interface clock pin.** SCL can support a digital interface clock up to 3.4MHz. If not used, SCL should be pulled up to VCC.
6	SDA	**Digital interface data pin.** If not used, SDA should be pulled up to VCC.
7	OC	**Output constant current (CC) limit setting.**
8	FB	**Feedback.** To set V_{OUT}, connect FB to the tap of an external resistor divider that is connected between the output and GND.
9	VCC	**Internal 3.65V low-dropout (LDO) regulator output.** Decouple VCC using a 1µF capacitor.
10	AGND	**Analog ground.** Connect AGND to GND using a single point.
12	OUT	**Output power.** Place the output capacitor (C_{OUT}) close to OUT and GND.
13	BST2	**Bootstrap.** Connect a 0.1µF capacitor between SW2 and BST2 to form a floating supply across the high-side MOSFET (HS-FET) driver.
14	SW2	**Second half-bridge switching node.** Connect one end of the inductor to SW2 to allow the current to run through the bridge.
15	SW1	**First half-bridge switching node.** Connect one end of the inductor to SW1 to allow the current to run through the bridge.
16	BST1	**Bootstrap.** Connect a 0.1µF capacitor between SW1 and BST1 to form a floating supply across the HS-FET driver.

ABSOLUTE MAXIMUM RATINGS (2)

Input voltage (V_{IN}) 26V
V_{OUT} 24V
V_{SWx} (DC) .....-0.3V to +24.3V
V_{SWx} (10ns) .....-7V to +26V
V_{BSTx} ..... V_{SWx} + 4V
V_{EN} .....-0.3V to +26V
V_{PG} .....-0.3V to +5.5V
All other pins .....-0.3V to +4V
Continuous power dissipation (T_A = 25°C) (3) (6) 4.8W
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....±2kV (4)
Charged-device model (CDM) .....±2kV (5)

Recommended Operating Conditions (6)

Operating input voltage (V_{IN}) range . 2.8V to 22V
Output voltage (V_{OUT}) range.....1V to 20.47V
Output current (I_{OUT}).....3A continuous current
Input current (I_{IN}).....4A continuous current
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-16 (3mmx3mm)		
EV28167-N-Q-00A (7)	26	3 °C/W
JESD51-7 (8)	50	12 °C/W

Notes:

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) Per JEDEC specification JESD22-A114. JEDEC document JEP155 states that 500V human-body model (HBM) allows for safe manufacturing with a standard ESD control process.
5) Per JEDEC specification JESD22-C101. JEDEC document JEP157 states that a 250V charged-device model (CDM) allows for safe manufacturing with a standard ESD control process.
6) The device is not guaranteed to function outside of its operating conditions.
7) Measured on an EV28167-N-Q-00A, 4-layer PCB, 64mmx64mm.
8) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown current	I_{SD}	V_{EN} = 0V		2	8	μA
Quiescent current	I_Q	No switching, the digital interface sets PFM mode		1		mA
Enable (EN) rising threshold	V_{EN_RISING}		1	1.1	1.2	V
EN hysteresis	V_{EN_HYS}			110		mV
EN pull-down resistance	R_{EN}	V_{EN} = 2V		2		MΩ
EN on to the output voltage (V_{OUT}) exceeds 90% delay	t_{DELAY}	See Figure 7 on page 24		3.6		ms
VCC regulator voltage	V_{CC}		3.3	3.65	4	V
VCC load regulation	V_{CC_LOG}	VCC current (I_{CC}) = 10mA		1		%
Input voltage (V_{IN}) under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.50	2.65	2.8	V
V_{IN} UVLO hysteresis	V_{UVLO_HYS}			160		mV
Power Converter						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	MOSFET A (SWA) and MOSFET D (SWD)		25	40	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	MOSFET B (SWB) and MOSFET C (SWC)		21	35	mΩ
Feedback (FB) voltage	V_{FB}	T_J = 25°C	990	1000	1010	mV
		T_J = -40°C to +125°C	985	1000	1015	mV
FB current	I_{FB}	V_{FB} = 1.05V		10		nA
Output discharge resistance	R_{DIS}			60	100	Ω
Switch leakage	I_{SW_LKG}	V_{EN} = 0V, V_{SWx} = 22V, T_J = 25°C			1	μA
		V_{EN} = 0V, V_{SWx} = 22V, T_J = -40°C to +125°C			5	μA
Switching frequency	f_{SW1}	FREQ = 00 (500kHz), T_J = 25°C		520		kHz
	f_{SW2}	FREQ = 01 (750kHz), T_J = 25°C		750		kHz
	f_{SW3}	FREQ = 10 (1MHz), T_J = 25°C		1		MHz
	f_{SW4}	FREQ = 11 (1.25MHz), T_J = 25°C		1.25		MHz
Minimum on time (10)	t_{ON_MIN1}	SWA, SWB, SWC, and SWD		160		ns
Maximum duty cycle	D_{MAX}	Buck mode, FREQ = 00 (500kHz)		85		%
Minimum duty cycle (10)	D_{MIN}	Boost mode, FREQ = 00 (500kHz)		15		%
Soft-start time	t_{SS}	Can be set via the digital interface, V_{REF} = 0V to 1V, default t_{SS}		3.5		ms
Protection						
Output over-voltage protection (OVP)	V_{OVP_R}		150	160	170	% of V_{REF}
Output OVP recovery	V_{OVP_F}		130	140	150	% of V_{REF}
LS-FET B valley current limit (I_{LIMIT})	I_{LIMIT2}	MOSFET B	6	8	10	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J = -40°C to +125°C (9), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
LS-FET C peak I_{LIMIT}	I_{LIMIT3}	MOSFET C		10		A
Average output current (I_{OUT}) (10)	I_{OUT_LIMIT1}	V_{OUT} = 5V, T_J = 0°C to 125°C temp range, configurable via the digital interface, IOUT_LIM bits = 14	0.85	1	1.15	A
	I_{OUT_LIMIT2}	V_{OUT} = 5V, T_J = 0°C to 125°C temp range, configurable via the digital interface, IOUT_LIM bits = 46	3.325	3.5	3.675	A
Output UVP threshold	V_{UVP}	20µs deglitch time, the UVP falling threshold is triggered	45	50	55	% of V_{REF}
Power good (PG) threshold	V_{PG_RISING}	V_{OUT} from low to high	85	90	95	% of V_{REF}
	$V_{PG\_FALLING}$	V_{OUT} from high to low		80	85	% of V_{REF}
PG sink current capability	V_{PG_LOW}	Sink 4mA			0.4	V
PG leakage	I_{PG_LKG}	V_{PULL} = 5V			5	µA
Thermal shutdown threshold (10)	T_{SD}			150		°C
Thermal shutdown hysteresis (10)	T_{SD_HYS}			20		°C
Digital Interface Specifications (10)						
Input logic high voltage	V_{IN_HIGH}	V_{DD} is pulled up from 1.8V to 5V	1.4			V
Input logic low voltage	V_{IN_LOW}				0.4	V
Output logic low voltage	V_{OUT_LOW}				0.4	V
SCL clock frequency	f_{SCL}			400	3400	kHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		160			ns
Data set-up time	t_{SU_DATA}		10			ns
Data hold time	t_{HD_DATA}		0	60		ns
Set-up time for a repeated start condition	t_{SU_START}		160			ns
Hold time for a repeated start condition	t_{HD_START}		160			ns
Bus free time between a start and a stop condition	t_{BUS_FREE}		160			ns
Set-up time for a stop condition	t_{SU_STOP}		160			ns
SCL and SDA rising time	t_{RISE}		10		300	ns
SCL and SDA falling time	t_{FALL}		10		300	ns
Suppressed spike pulse-width	t_{SPIKE}		0		50	ns
Bus line capacitance	C_{BUS}				400	pF

Notes:

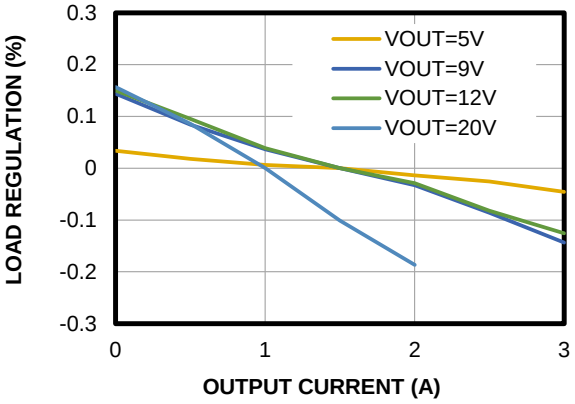
9) All min and max values are tested at T_J = 25°C. Over-temperature (OT) limits are guaranteed by design, characterization, and correlation.
10) Guaranteed by engineering sample characterization.

TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

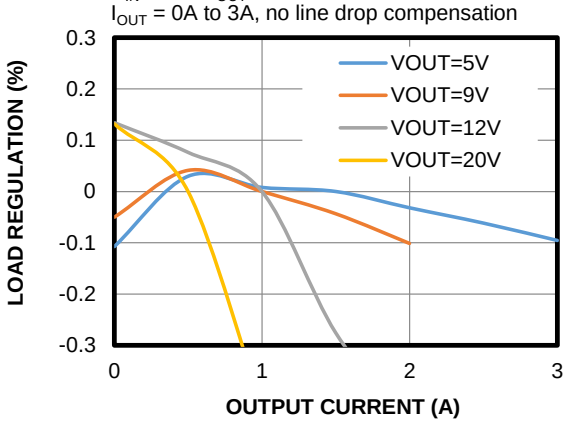
Load Regulation

V_{IN} = 12V, V_{OUT} = 5V, 9V, 12V, or 20V,
I_{OUT} = 0A to 3A, no line drop compensation



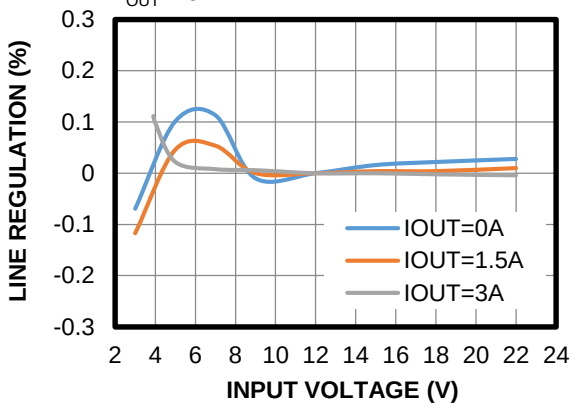
Load Regulation

V_{IN} = 6V, V_{OUT} = 5V, 9V, 12V, or 20V,
I_{OUT} = 0A to 3A, no line drop compensation



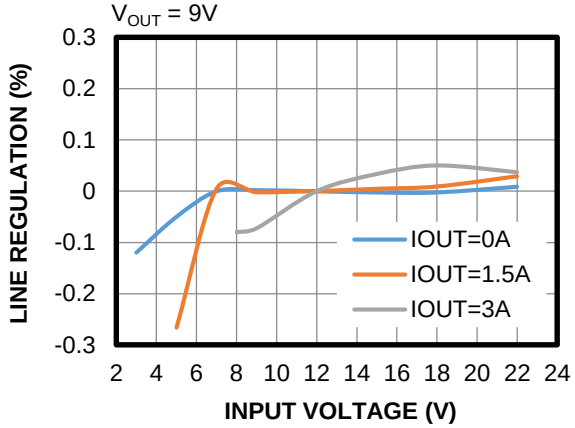
Line Regulation

V_{OUT} = 5V



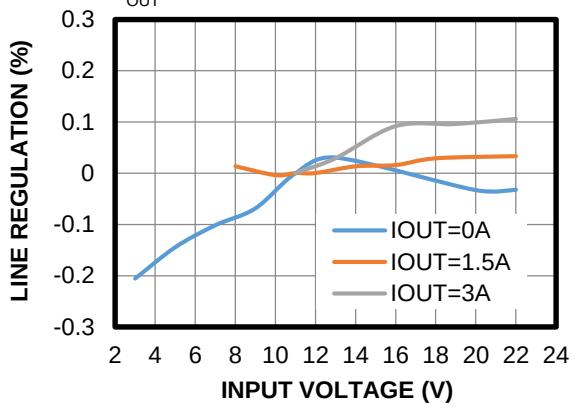
Line Regulation

V_{OUT} = 9V



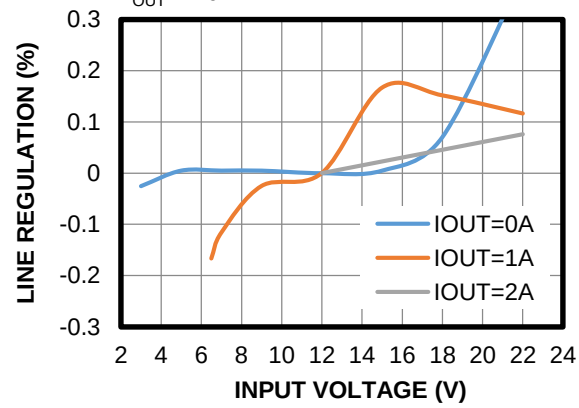
Line Regulation

V_{OUT} = 12V



Line Regulation

V_{OUT} = 20V

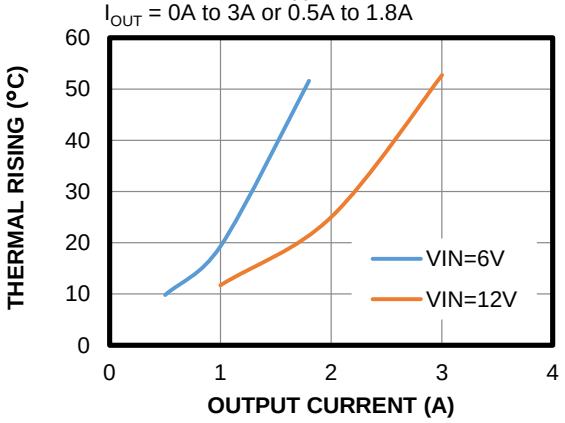


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

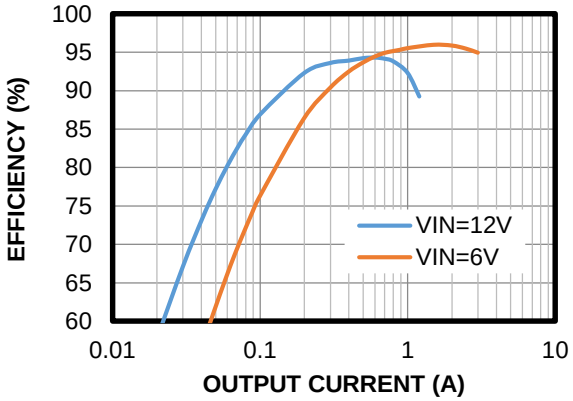
Thermal Rising vs. Output Current

V_{IN} = 6V or 12V, V_{OUT} = 12V,
I_{OUT} = 0A to 3A or 0.5A to 1.8A



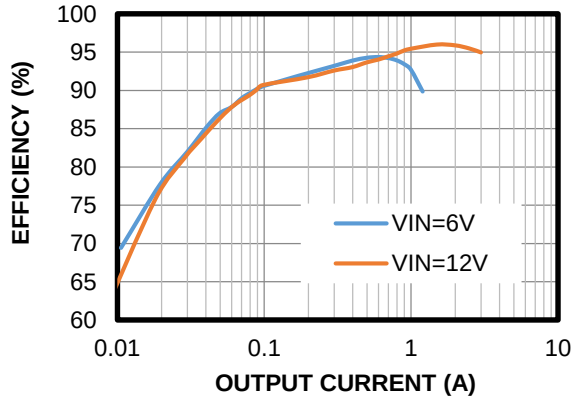
Efficiency vs. Output Current

V_{IN} = 6V or 12V, V_{OUT} = 12V,
L = 2.2µH, f_{SW} = 1MHz, R_{DC} = 12.3mΩ,
forced PWM mode



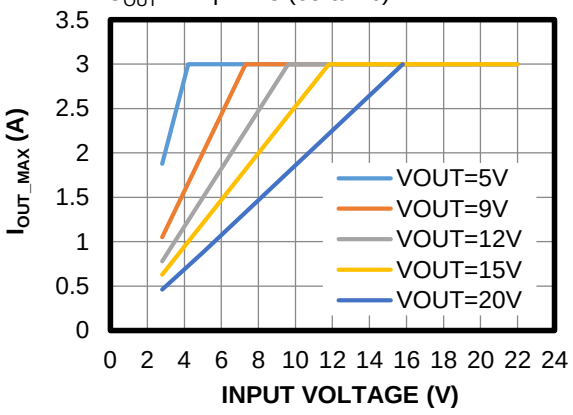
Efficiency vs. Output Current

V_{IN} = 6V or 12V, V_{OUT} = 12V,
L = 2.2µH, f_{SW} = 1MHz, R_{DC} = 12.3mΩ,
auto-PFM/PWM mode

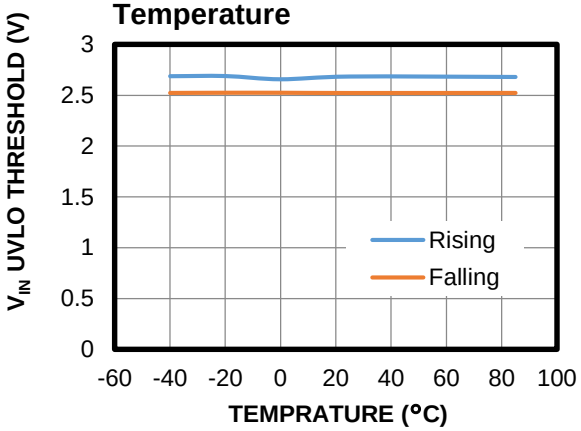


Maximum Output Current vs. Input Voltage

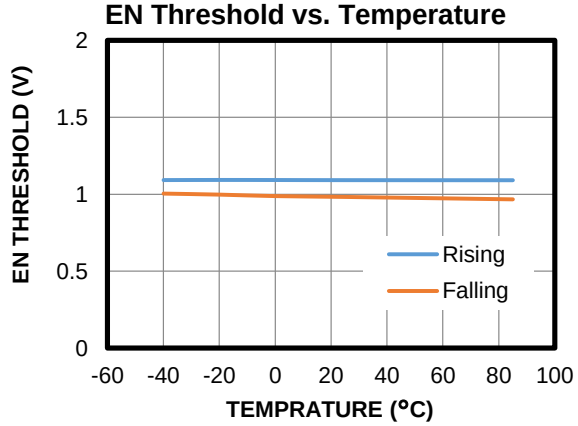
C_{OUT} = 22µF x 8 (ceramic)



V_{IN} UVLO Threshold vs. Temperature



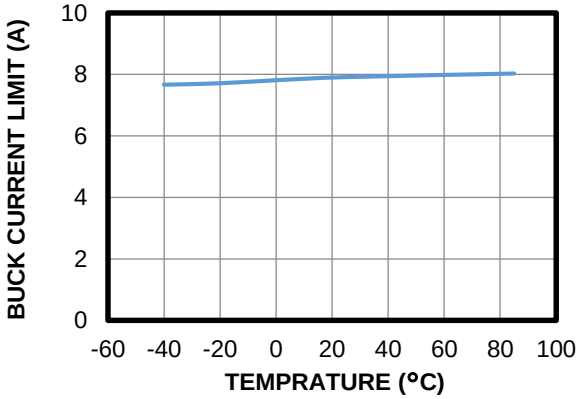
EN Threshold vs. Temperature



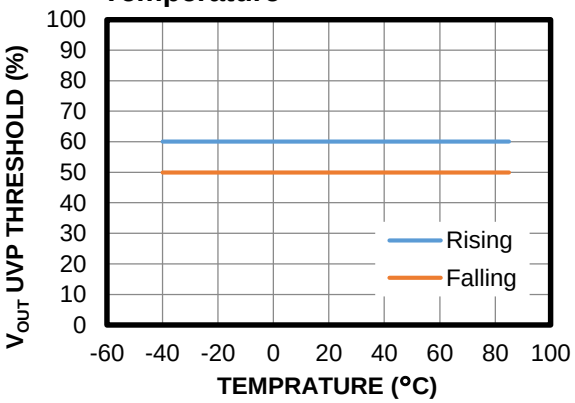
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

Buck Current Limit vs. Temperature



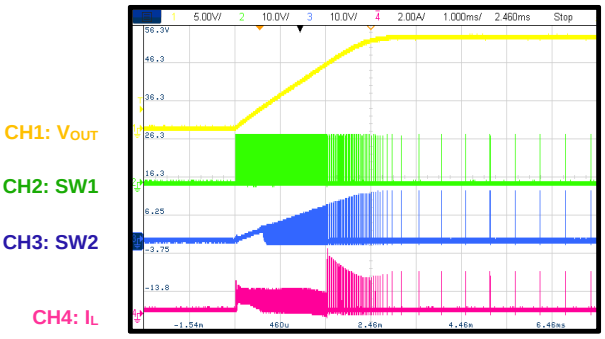
V_{OUT} UVP Threshold vs. Temperature



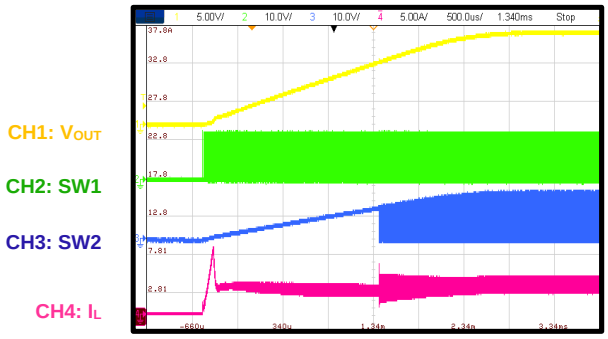
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

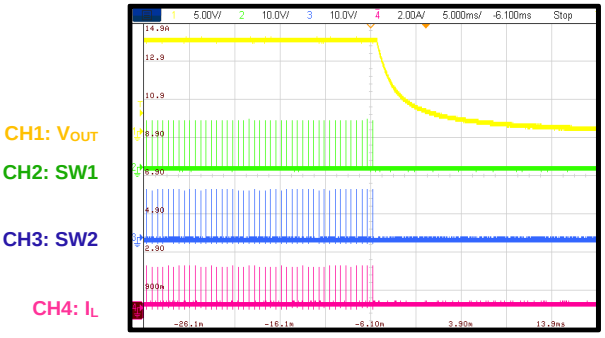
EN Bit Start-Up through the Digital Interface
Load = 0A



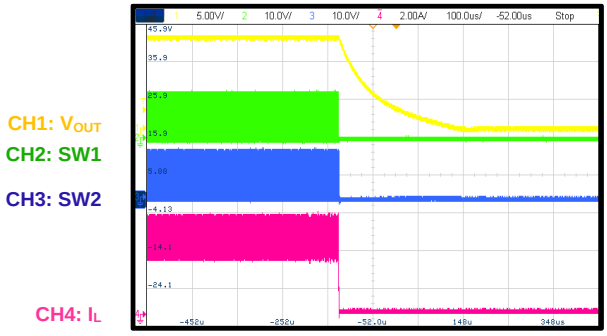
EN Bit Start-Up through the Digital Interface
Load = 3A



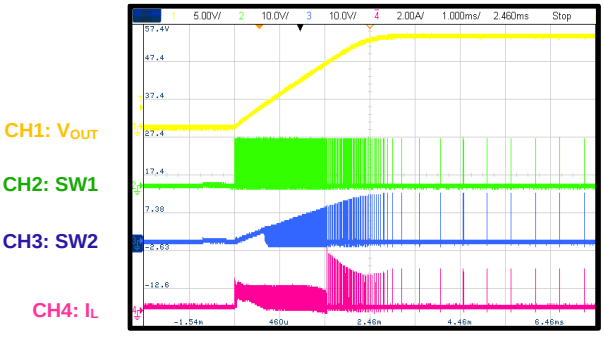
EN Bit Shutdown through the Digital Interface
Load = 0A



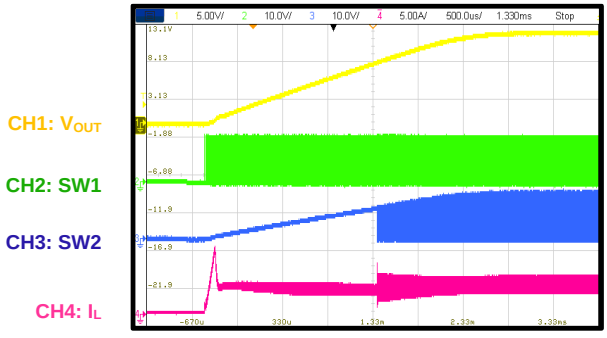
EN Bit Shutdown through the Digital Interface
Load = 3A



Start-Up through EN
Load = 0A



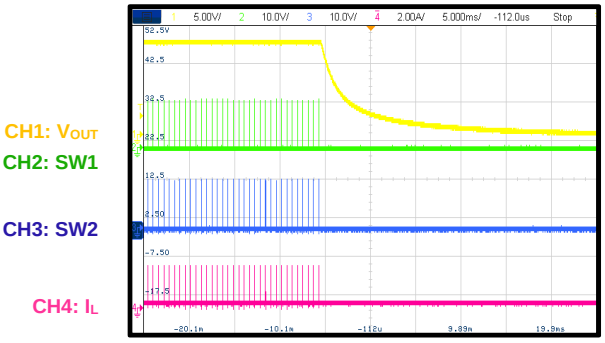
Start-Up through EN
Load = 3A



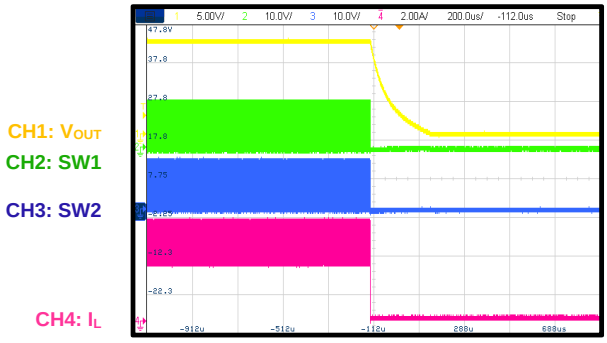
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

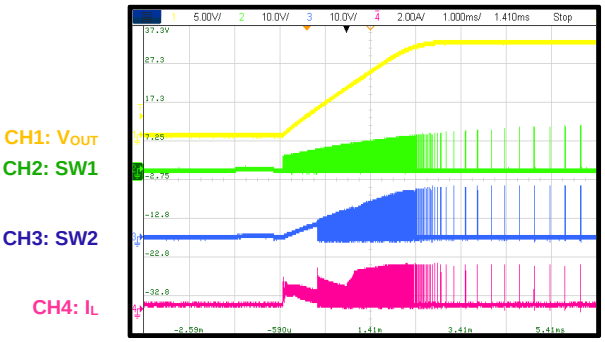
Shutdown through EN
Load = 0A



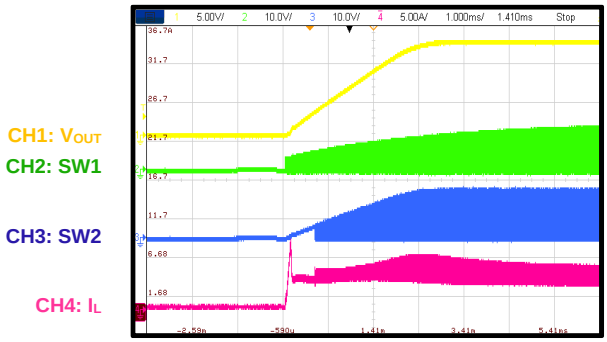
Shutdown through EN
Load = 3A



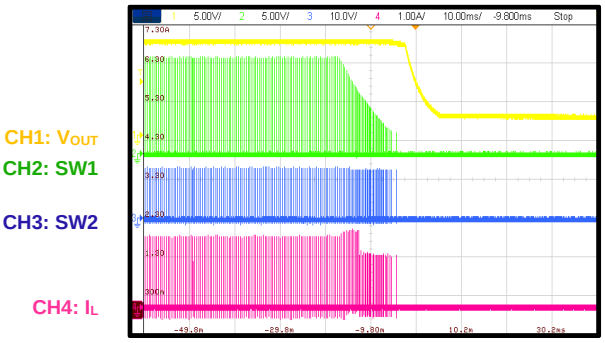
Start-Up through VIN
Load = 0A



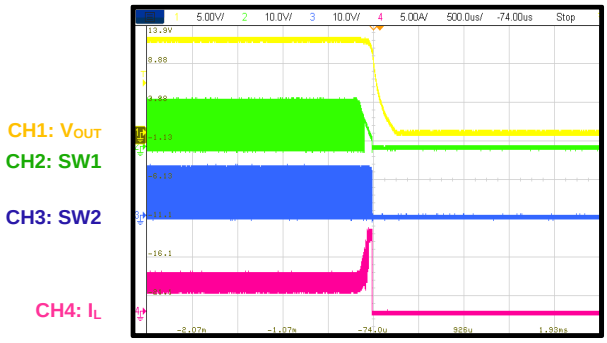
Start-Up through VIN
Load = 3A



Shutdown through VIN
Load = 0A



Shutdown through VIN
Load = 3A

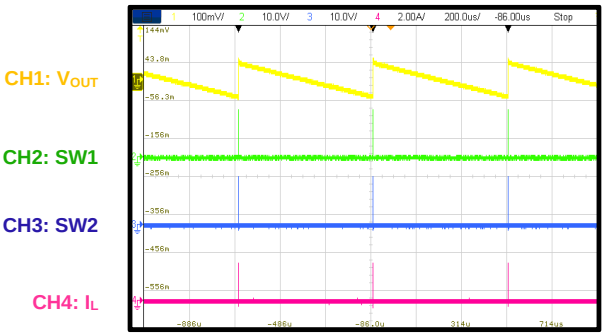


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

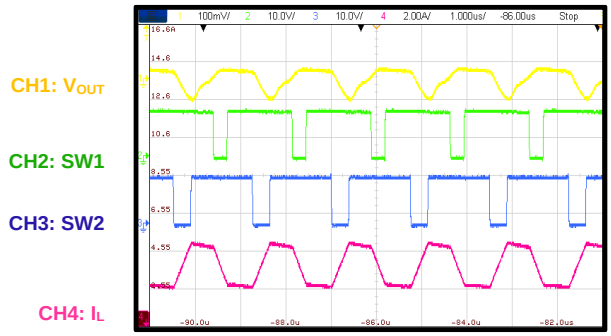
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 0A, f_{SW} = 1MHz



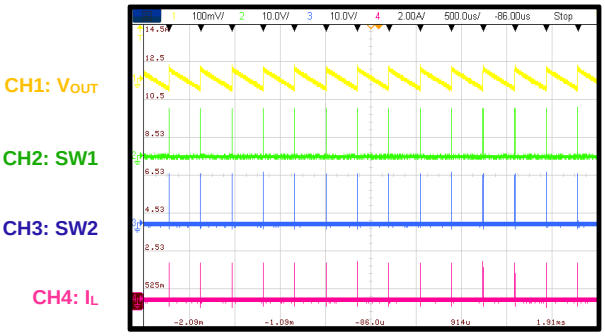
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 3A, f_{SW} = 1MHz



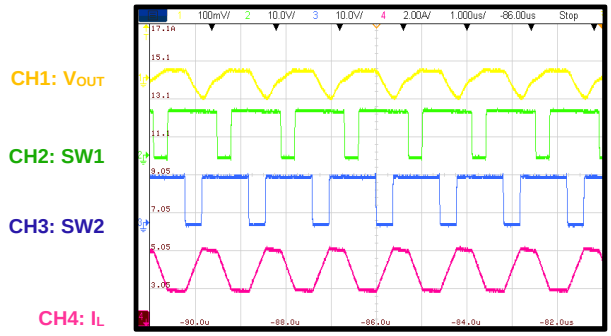
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 0A, f_{SW} = 1.25MHz



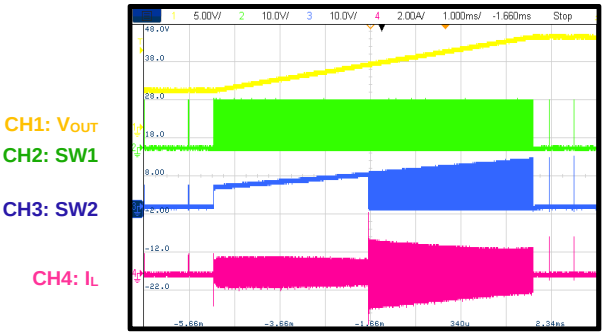
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 3A, f_{SW} = 1.25MHz



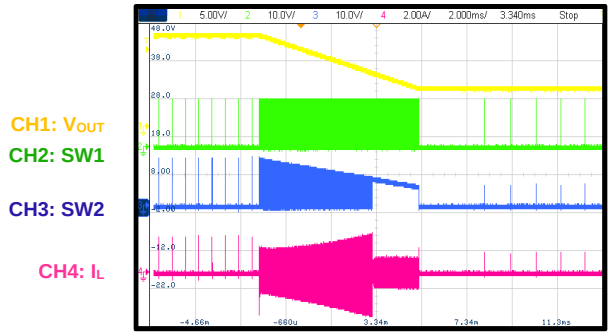
Digital Interface VID

V_{OUT} = 5V to 12V, I_{OUT} = 0A, R1 = 4.3kΩ,
R2 = 392kΩ



Digital Interface VID

V_{OUT} = 12V to 5V, I_{OUT} = 0A, R1 = 4.3kΩ,
R2 = 392kΩ

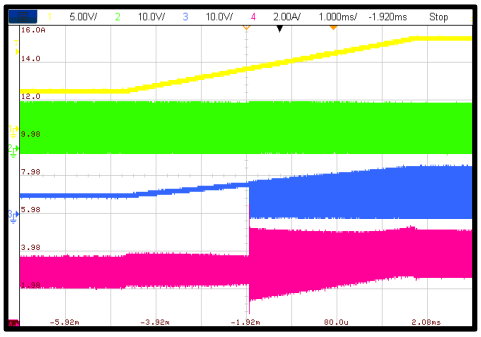


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

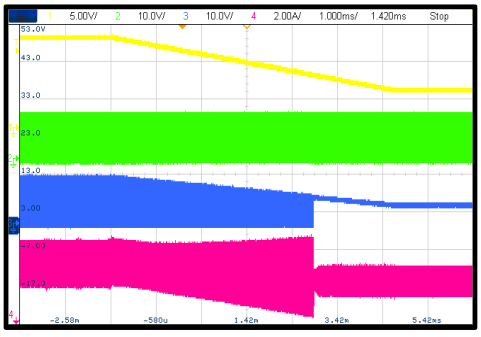
Digital Interface VID

V_{OUT} = 5V to 12V, I_{OUT} = 3A, R1 = 4.3kΩ, R2 = 392kΩ



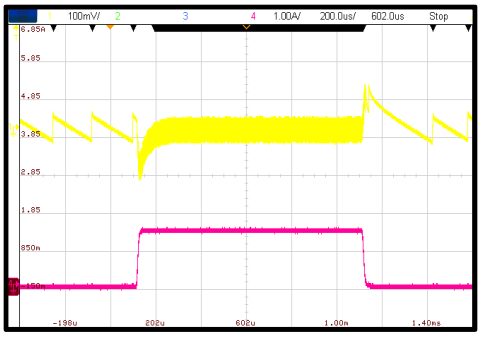
Digital Interface VID

V_{OUT} = 12V to 5V, I_{OUT} = 3A, R1 = 4.3kΩ, R2 = 392kΩ



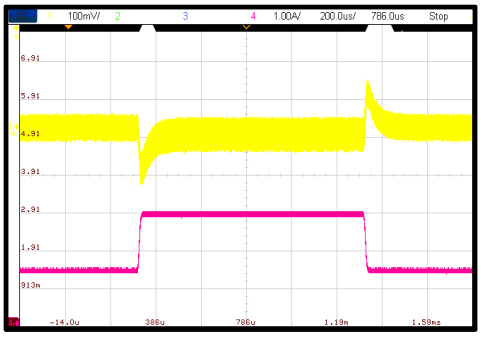
Load Transient Response

V_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 0A to 1.5A, slew rate = 150mA/µs, no line drop compensation

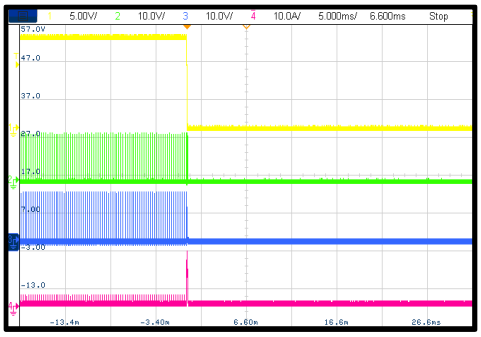


Load Transient Response

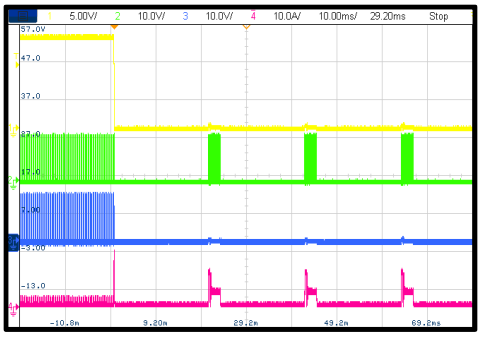
V_{IN} = 12V, V_{OUT} = 12V, I_{OUT} = 1.5A to 3A, slew rate = 150mA/µs, no line drop compensation



SCP Entry with Latch-Off Mode



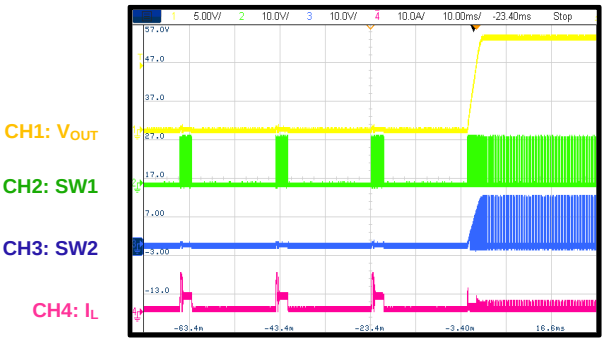
SCP Entry with Hiccup Mode



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

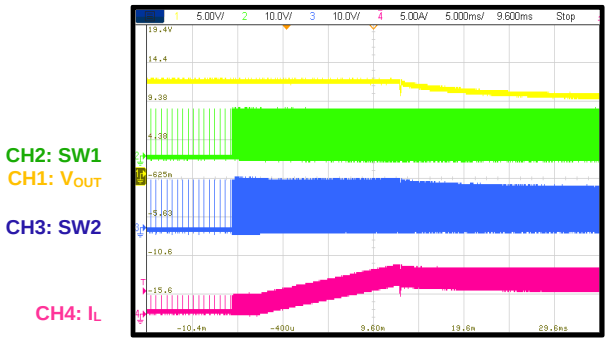
V_{IN} = 12V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

SCP Recovery with Hiccup Mode

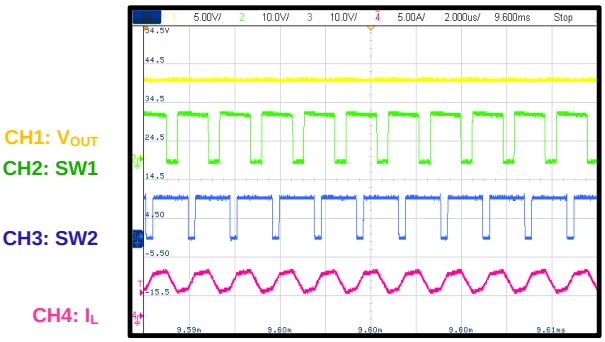


CC Current Limit Entry

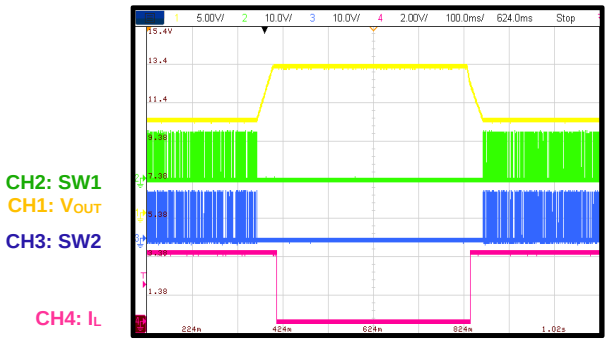
Tested with an electronic load in constant-voltage (CV) mode



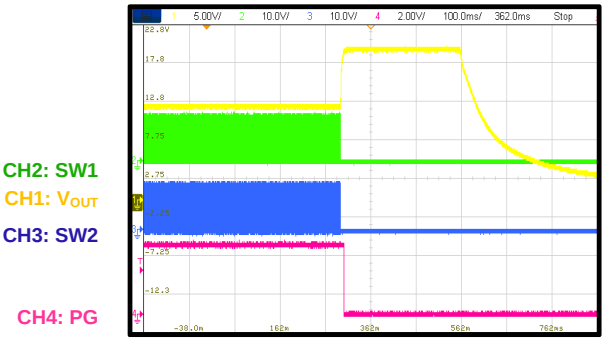
CC Current Limit Steady State



V_{OUT} OVP with Hiccup Mode



V_{OUT} OVP with Latch-Off Mode

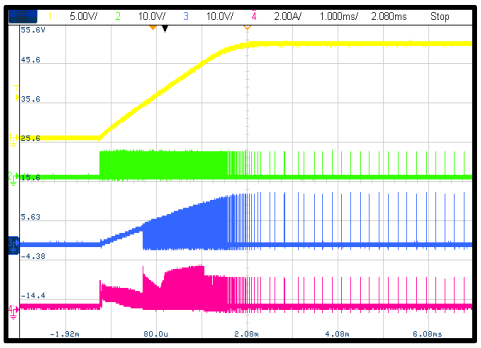


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

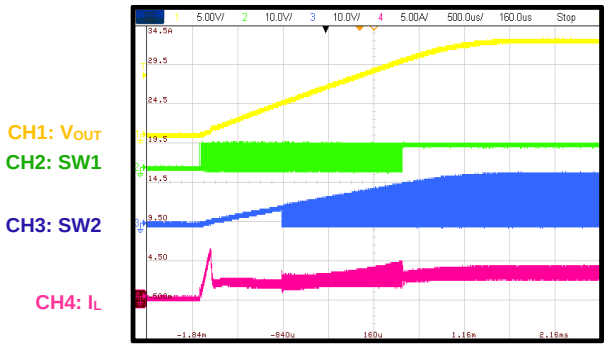
EN Bit Start-Up through the Digital Interface

Load = 0A



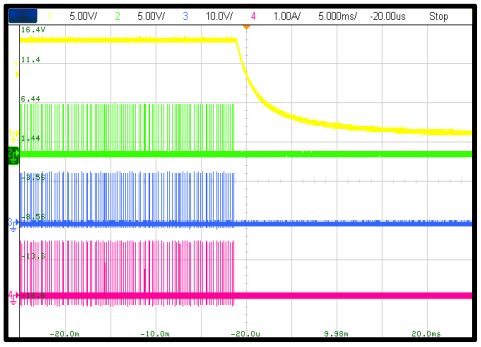
EN Bit Start-Up through the Digital Interface

Load = 1.4A



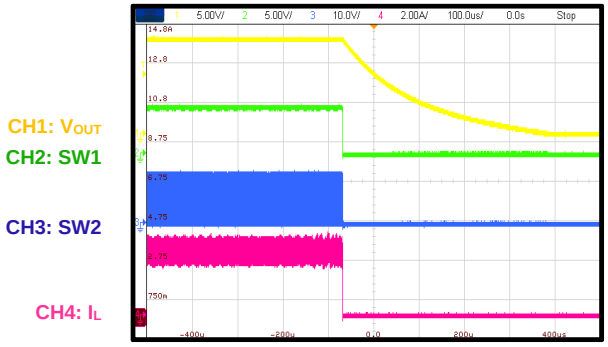
EN Bit Shutdown through the Digital Interface

Load = 0A



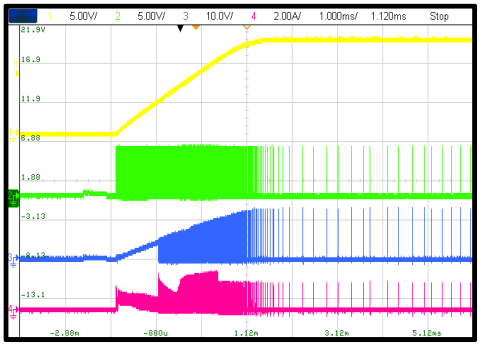
EN Bit Shutdown through the Digital Interface

Load = 1.4A



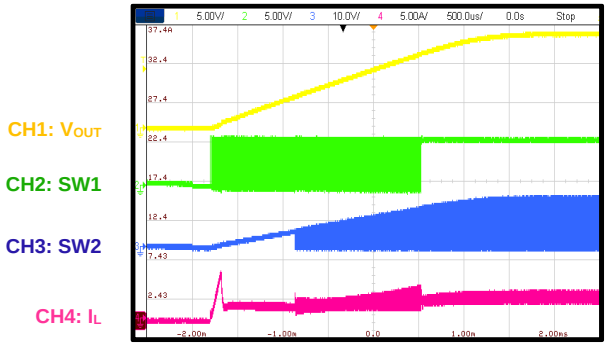
Start-Up through EN

Load = 0A



Start-Up through EN

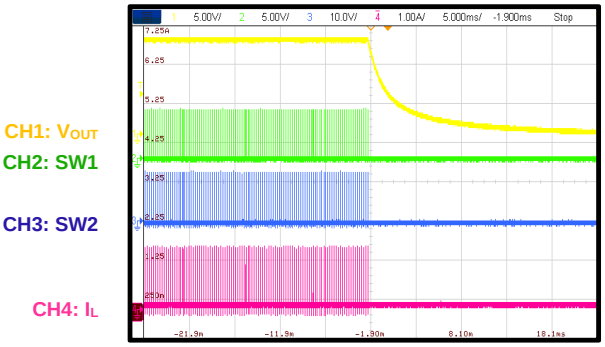
Load = 1.4A



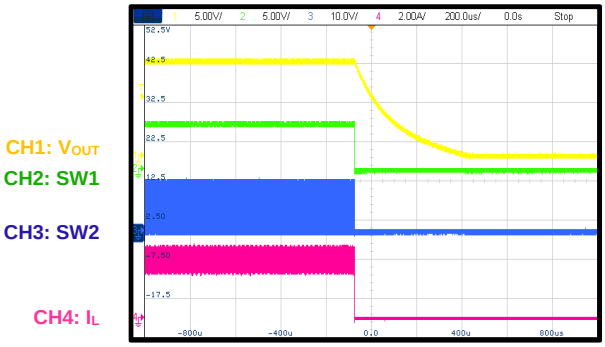
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

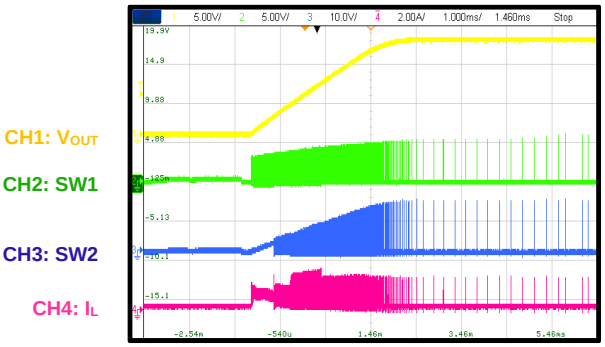
Shutdown through EN
Load = 0A



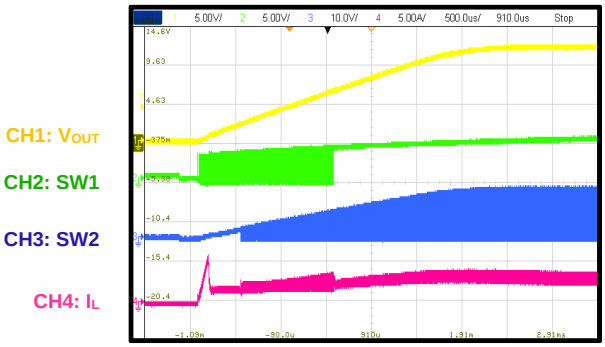
Shutdown through EN
Load =1.4A



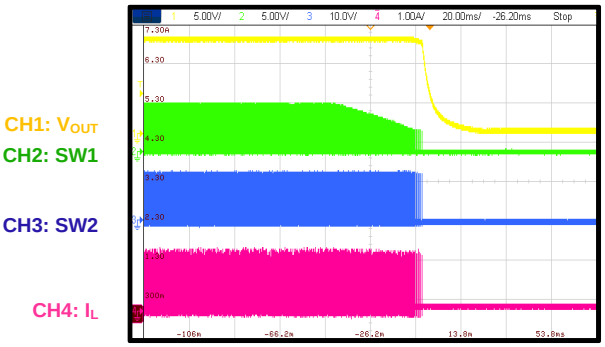
Start-Up through VIN
Load = 0A



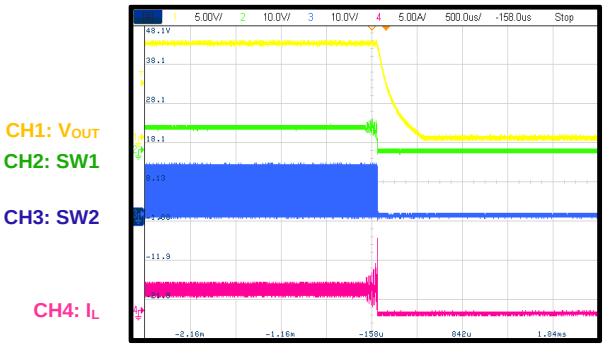
Start-Up through VIN
Load = 1.4A



Shutdown through VIN
Load = 0A



Shutdown through VIN
Load = 1.4A

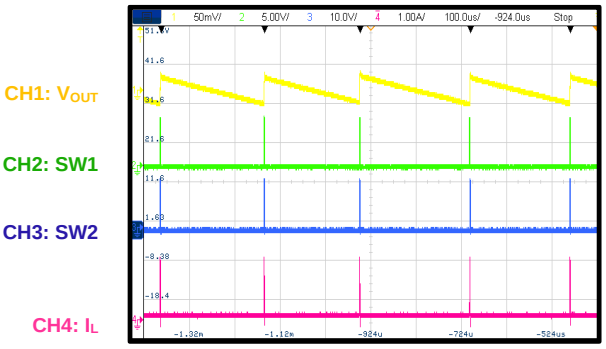


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

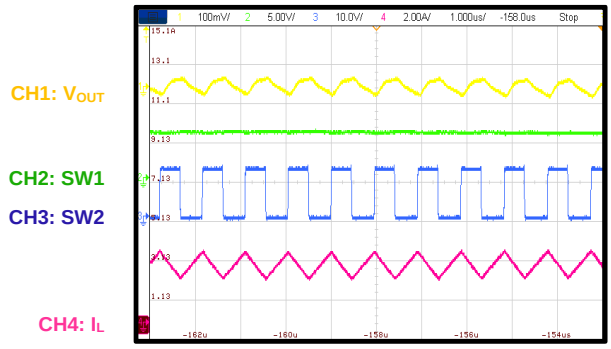
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 0A, f_{SW} = 1MHz



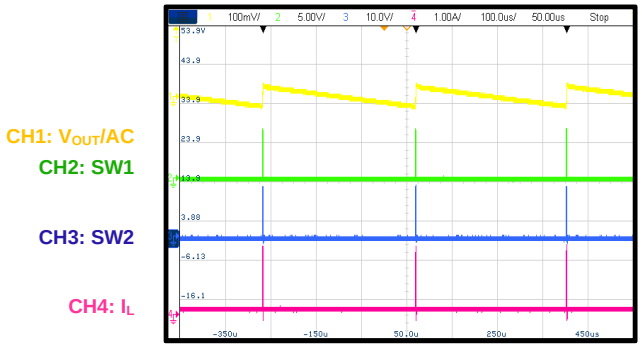
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 1.4A, f_{SW} = 1MHz



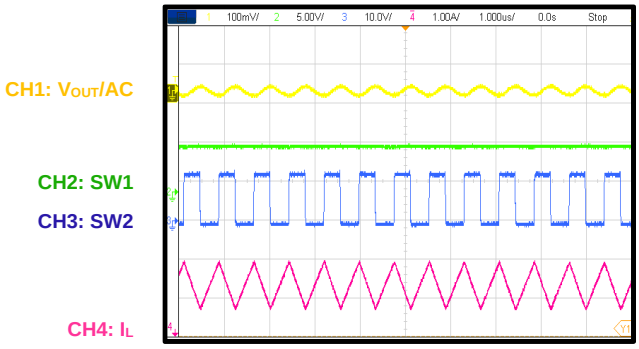
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 0A, f_{SW} = 1.25MHz



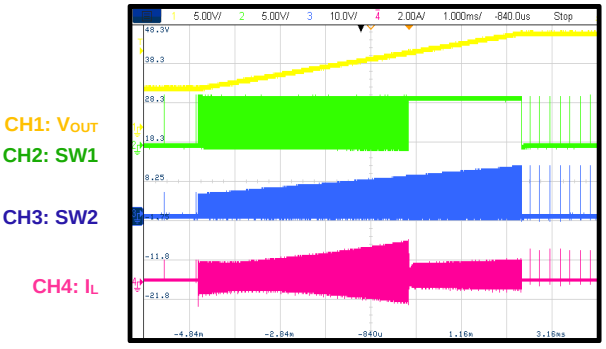
Steady State

Auto-PFM/PWM mode, V_{OUT} = 12V,
load = 1.4A, f_{SW} = 1.25MHz



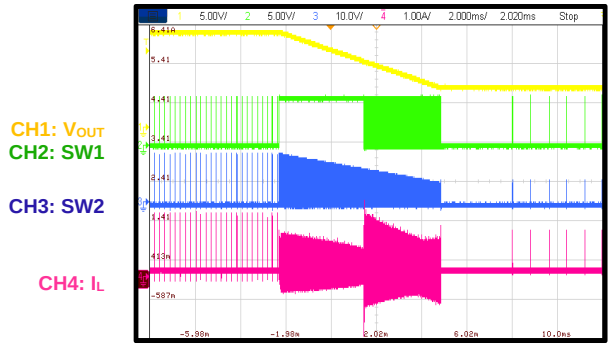
Digital Interface VID

V_{OUT} = 5V to 12V, I_{OUT} = 0A, R1 = 4.3kΩ,
R2 = 392kΩ



Digital Interface VID

V_{OUT} = 12V to 5V, I_{OUT} = 0A, R1 = 4.3kΩ,
R2 = 392kΩ

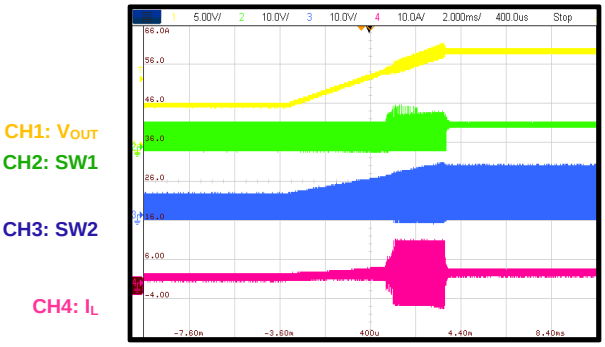


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 6V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

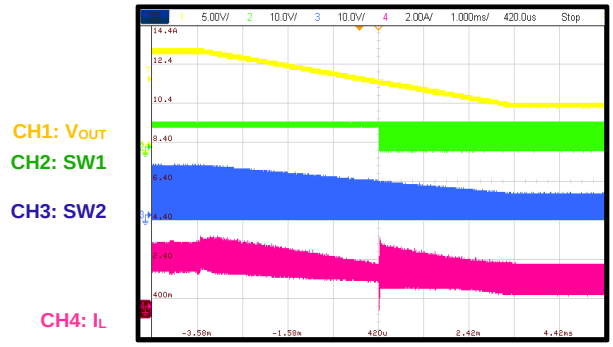
Digital Interface VID

V_{OUT} = 5V to 12V, I_{OUT} = 1.2A, R1 = 4.3kΩ, R2 = 392kΩ



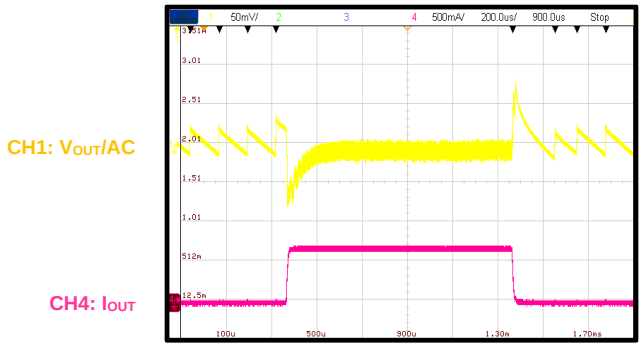
Digital Interface VID

V_{OUT} = 12V to 5V, I_{OUT} = 1.2A, R1 = 4.3kΩ, R2 = 392kΩ



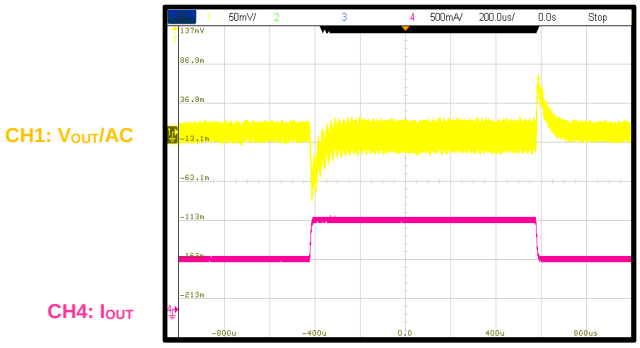
Load Transient Response

V_{IN} = 6V, V_{OUT} = 12V, I_{OUT} = 0A to 0.7A, slew rate = 150mA/µs, no line drop compensation

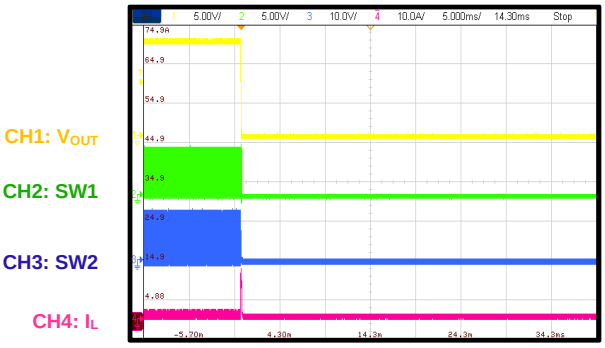


Load Transient Response

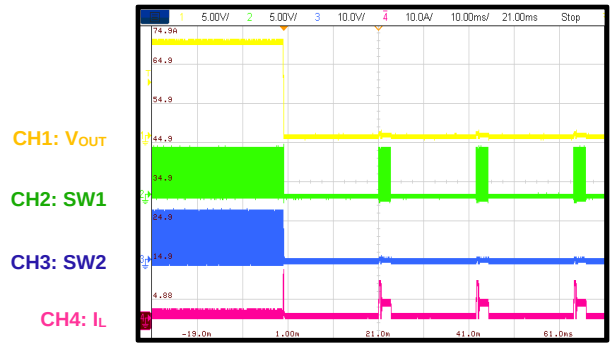
V_{IN} = 6V, V_{OUT} = 12V, I_{OUT} = 0.7A to 1.4A, slew rate = 150mA/µs, no line drop compensation



SCP Entry with Latch-Off Mode



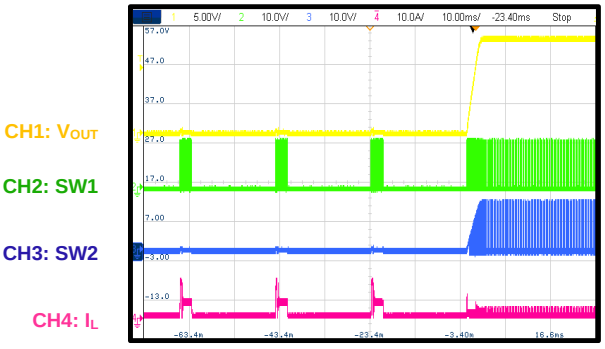
SCP Entry with Hiccup Mode



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

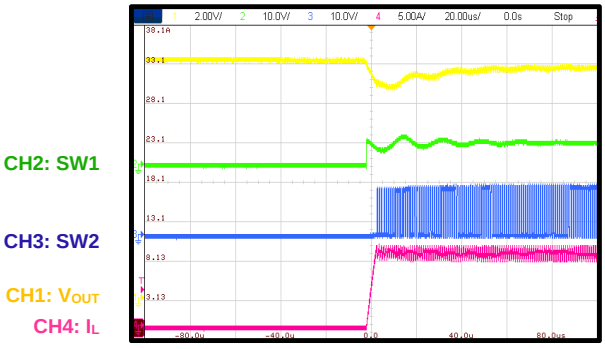
V_{IN} = 6V, V_{OUT} = 12V, L = 2.2µH, f_{SW} = 1MHz, T_A = 25°C, unless otherwise noted.

SCP Recovery with Hiccup Mode

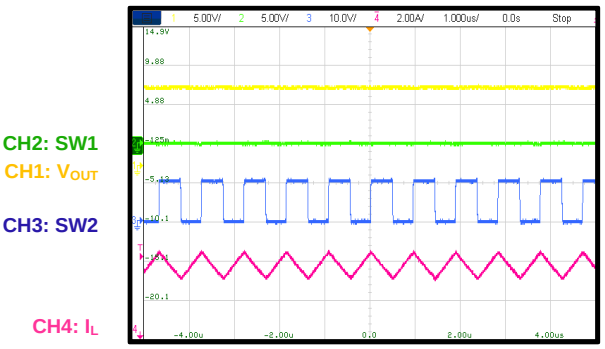


CC Current Limit Entry

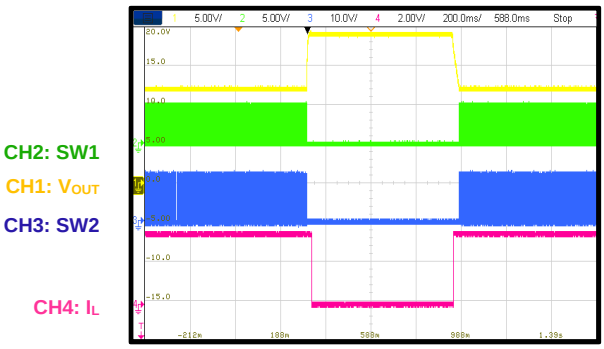
Tested with an electric load in CV mode



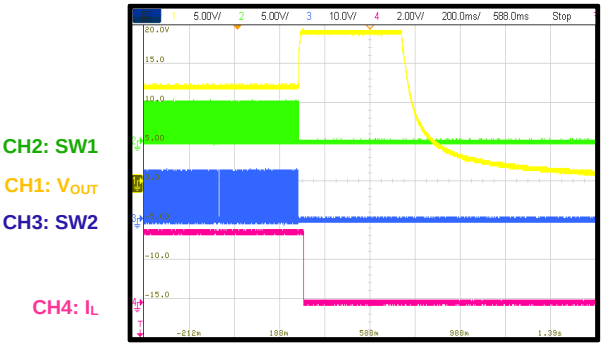
CC Current Limit Steady State



V_{OUT} OVP with Hiccup Mode



V_{OUT} OVP with Latch-Off Mode



FUNCTIONAL BLOCK DIAGRAM

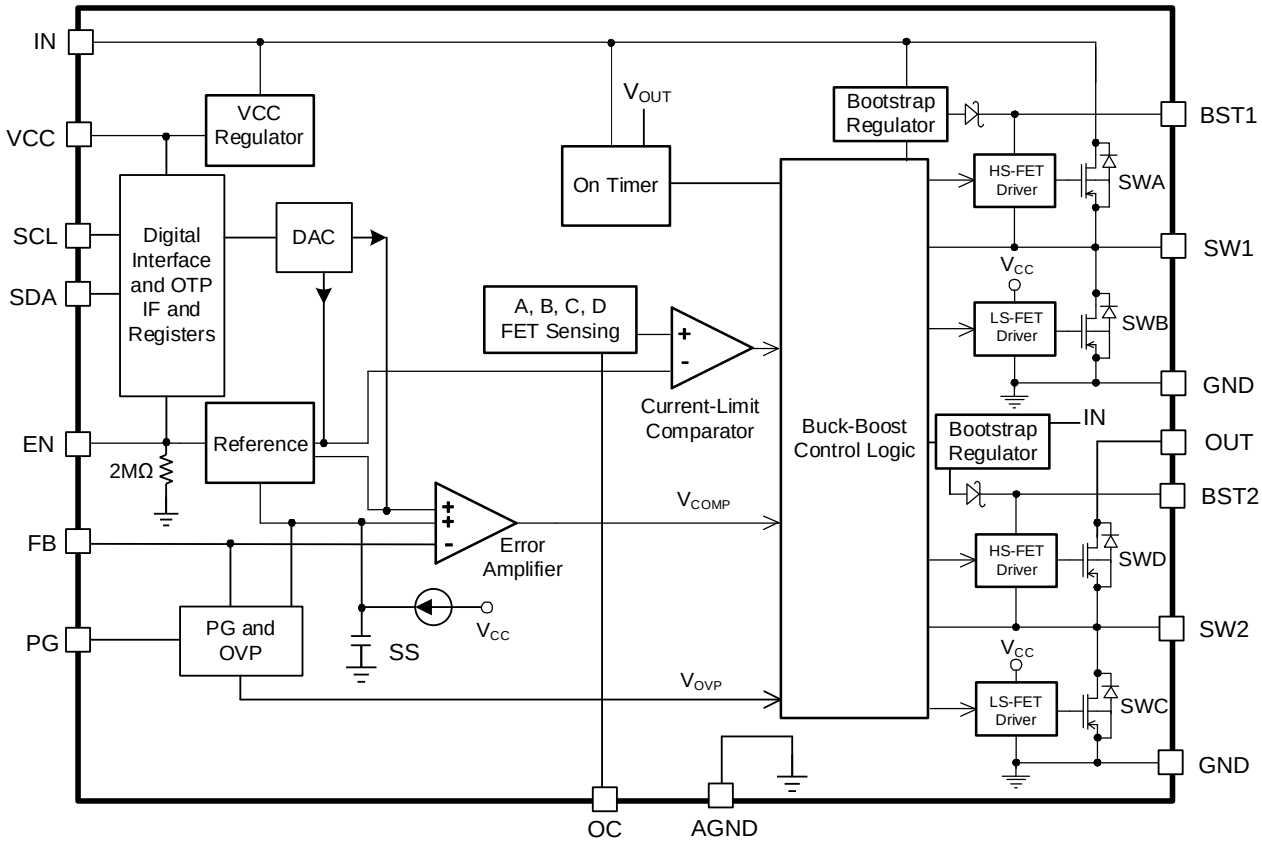


Figure 1: Functional Block Diagram

OPERATION

The MP28167-N is an integrated buck-boost converter with four MOSFETs that can operate in constant-on-time (COT) control mode with a fixed frequency. This provides fast transient response during buck, boost, and buck-boost mode. A special buck-boost control strategy provides high efficiency across the entire input voltage (V_{IN}) range and smooth transient between different modes.

Buck-Boost Operation

The MP28167-N can regulate the output voltage (V_{OUT}) to be above, below, or equal to V_{IN}. Figure 2 shows a power structure with one inductor and the four MOSFETs (SWA, SWB, SWC, and SWD).

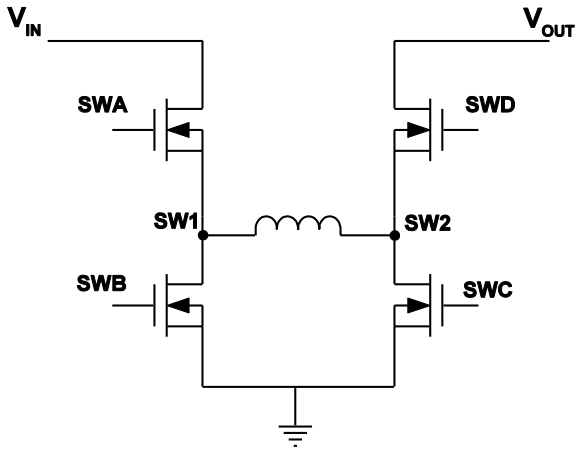


Figure 2: Buck-Boost Topology

The MP28167-N can operate in buck mode, boost mode, or buck-boost mode with different V_{IN} inputs (see Figure 3).

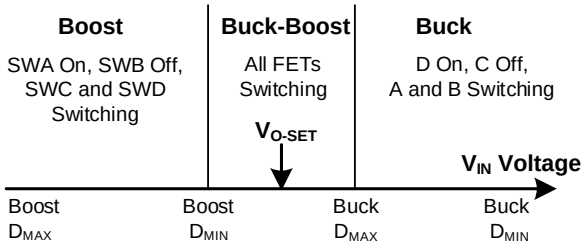


Figure 3: Buck-Boost Operation Range

Buck Mode

When V_{IN} significantly exceeds V_{OUT}, the MP28167-N operates in buck mode. In buck mode, SWA and SWB switch for buck regulation. SWC turns off, and SWD remains on to conduct the inductor current (I_L).

SWA works with COT control, and SWB turns on as a complement of SWA. In each cycle, SWB turns on to conduct I_L.

If I_L drops to the buck comparator (COMP_BUCK) voltage (V_{COMP_BUCK}), SWB turns off and SWA turns on for a fixed on time (t_{ON}). Then SWB turns on again, and the operation repeats. The COMP_BUCK signal is the error amplifier (EA) output from the V_{OUT} feedback and internal feedback (FB) reference voltage (V_{REF}) (see Figure 4).

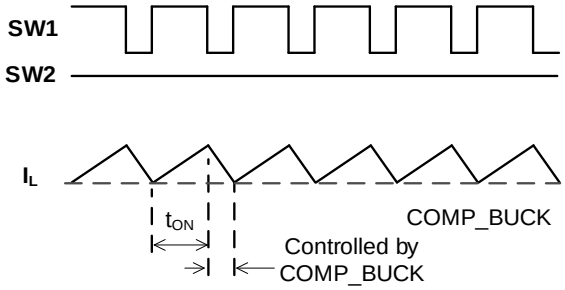


Figure 4: Buck Waveform

Boost Mode

When V_{IN} is significantly below V_{OUT}, the MP28167-N operates in boost mode. In boost mode, SWC and SWD switch for boost regulation. SWB turns off, and SWA turns on to conduct I_L.

During each period, SWC remains off with COT control, while SWD turns on as a complement of SWC to boost I_L to the output. In each cycle, SWC turns on to conduct I_L. When I_L reaches boost comparator (COMP_BOOST) voltage (V_{COMP_BOOST}), SWD turns on and SWC turns off for a fixed off time (t_{OFF}). During this period, SWD turns on to regulate V_{OUT} (see Figure 5).

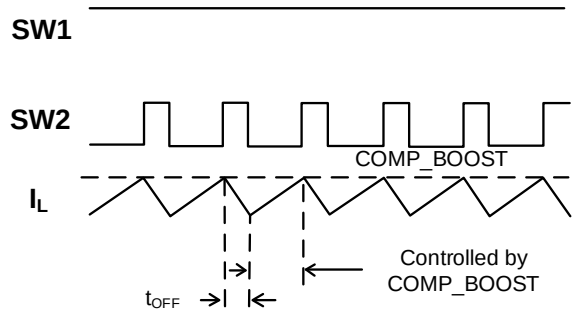


Figure 5: Boost Waveform

Buck-Boost Mode

When V_{IN} is almost equal to V_{OUT}, the MP28167-N cannot provide enough energy to operate in buck mode due to SWA's minimum t_{OFF} (t_{OFF_MIN}), or it supplies too much power to V_{OUT} in boost mode due to SWC's minimum t_{ON} (t_{ON_MIN}). The IC uses buck-boost mode to regulate V_{OUT} in these conditions.

If V_{IN} drops and SWA's t_{OFF} is close to the minimum buck t_{OFF} in buck mode, then the device enters buck-boost mode. Once the next cycle starts after the SWA and SWD (the buck high-side MOSFET [HS-FET]) t_{ON}, the boost starts up with the SWA and SWC (the boost low-side MOSFET [LS-FET]) on.

SWA and SWD turn on again for the boost mode resting period (the boost HS-FET is on). After the boost period elapses, the buck period starts, and SWB and SWD turn on until I_L drops to V_{COMP_BUCK}. Then SWA and SWD turn on until the next boost period begins. Buck and boost switching work with a one-interval period. This is called buck-boost mode.

Figure 6 shows the buck-boost waveform when V_{IN} exceeds V_{OUT} (the buck to buck-boost transient).

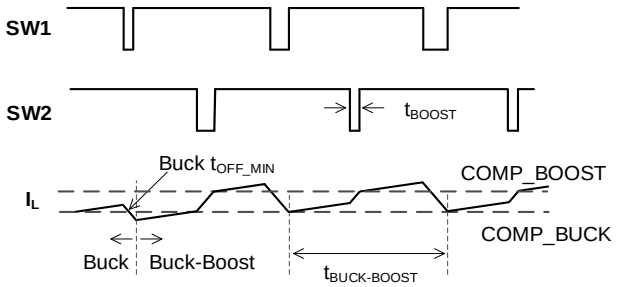


Figure 6: Buck to Buck-Boost Transient

If V_{IN} rises and the SWC t_{ON} is close to the boost t_{ON_MIN} in boost mode, then buck-boost mode is enabled. After the boost constant-off-time period (SWA and SWD on), SWB and SWD turn on until I_L drops to V_{COMP_BUCK}.

Once I_L drops to V_{COMP_BUCK}, SWA and SWD turn on for the buck t_{ON}, which is followed by boost switching (SWA and SWC on). Buck and boost switching work with a one-interval period.

Figure 7 shows the buck-boost waveform when V_{OUT} exceeds V_{IN}.

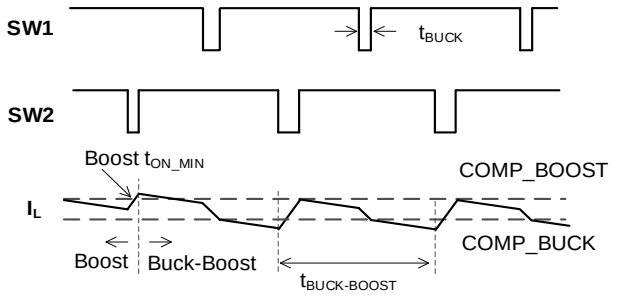


Figure 7: Boost to Buck-Boost Waveform

If V_{IN} exceeds 130% of V_{OUT} in buck-boost mode, the MP28167-N transitions from buck-boost mode to buck mode. If V_{IN} drops below 20% of V_{OUT}, the MP28167-N transitions from buck-boost mode to boost mode.

Operation Mode Selection

The MP28167-N works with a fixed frequency under heavy-load conditions. When the load current decreases, the MP28167-N operates in forced continuous conduction mode (FCCM) or pulse-skip mode (PSM) based on the MODE register setting.

Forced Continuous Conduction Mode (FCCM)

In forced continuous conduction mode (FCCM), the buck t_{ON} and boost t_{OFF} are determined by the internal circuit. This achieves a fixed frequency based on the V_{IN} / V_{OUT} ratio. When the load decreases, the average input current (I_{IN}) drops, and I_L may go negative from the output to the input during t_{OFF} (SWD on). This forces I_L to work in continuous mode with a fixed frequency, producing a lower V_{OUT} ripple (ΔV_{OUT}) than in PSM mode.

Pulse-Skip Mode (PSM)

If I_L drops to 0A in pulse-skip mode (PSM), SWD turns off to prevent the current from flowing from output to the input, forcing I_L to work in discontinuous conduction mode (DCM). Meanwhile, the internal t_{OFF} clock stretches once the MP28167-N enters DCM. The switching frequency (f_{SW}) decreases as the I_L conduction period shortens, which reduces power loss and ΔV_{OUT}.

If V_{COMP_BUCK} drops to the PSM threshold (even if the IC stretches f_{SW}), the MP28167-N stops switching to further reduce the switching power loss.

The MP28167-N recovers switching once V_{COMP_BUCK} exceeds the PSM threshold. The switching pulse skips based on V_{COMP_BUCK} under very light-load conditions. PSM has a much higher efficiency than FCCM at light loads; however, PSM may have a higher ΔV_{OUT} due to the group switching pulse.

Internal VCC Regulator

The internal 3.65V regulator (VCC) powers most of the internal circuitry. VCC takes V_{IN} and operates across the entire V_{IN} range. If V_{IN} exceeds 3.65V, the regulator's output is in full regulation. If V_{IN} drops below 3.65V, the regulator's output decreases with V_{IN}. Decouple VCC using an external 1µF ceramic capacitor.

Enable (EN) Control

The MP28167-N has an enable (EN) control pin that turns the device on and off. Pull EN high to turn on the IC on; pull EN low or float EN to turn it off.

If EN is pulled down when output discharge is enabled, the MP28167-N shuts down after 55ms. The digital interface register only resets to its default value once the MP28167-N experiences this type of shutdown. If EN is pulled high within 55ms, then the digital interface register is not reset, and the MP28167-N enables the output using the previous register setting.

If output discharge is disabled, the MP28167-N shuts down when EN is pulled down for longer than 100µs. The digital interface register is reset after a 100µs delay.

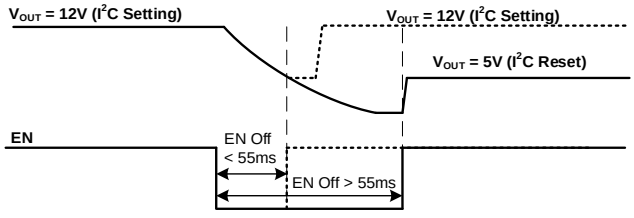


Figure 8: EN On/Off Logic for Resetting the Digital Interface Register

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient V_{IN}. The UVLO comparator monitors V_{IN}, and enables or disables the entire IC accordingly.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 3.65V. If V_{SS} is below V_{REF}, then the EA uses V_{SS} as the reference. If V_{SS} exceeds V_{REF}, then the EA uses V_{REF} as the reference.

If the output is pre-biased to a certain voltage during start-up, the IC disables both HS-FET and LS-FET switching until V_{SS} exceeds the internal feedback voltage (V_{FB}) (see Figure 9).

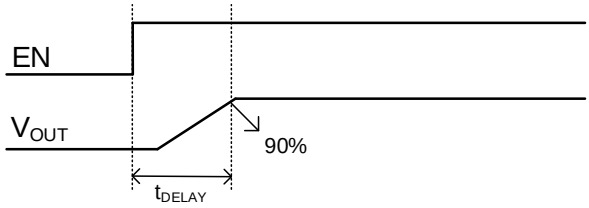


Figure 9: EN On to V_{OUT} Exceeds 90% Delay

Power Good (PG)

The MP28167-N uses a power good (PG) output to indicate whether V_{OUT} is ready. PG is an open-drain output. Connect PG to VCC or <5.5V voltage source via a pull-up resistor (e.g. 100kΩ). When V_{IN} is applied, PG is pulled down to ground before internal SS is ready. When V_{OUT} exceeds 90% of V_{REF}, PG is pulled high.

During normal operation, PG is pulled low when V_{OUT} drops below 80% of V_{REF} or V_{OUT} exceeds 150% of V_{REF}.

If EN is low or OTP occurs during UVLO, PG is pulled low immediately. If an over-current (OC) fault occurs, PG pulls low when V_{OUT} drops below 80% of V_{REF}. If an over-voltage (OV) fault occurs, PG pulls low when V_{OUT} exceeds 160% of V_{REF}.

Over-Current Protection (OCP)

The MP28167-N has a constant current (CC) limit control loop to limit the average output current (I_{OUT}). The SWA, SWB, SWC, and SWD current information is sensed, and then an algorithm calculates the average I_{OUT}.

When I_{OUT} exceeds the current-limit threshold, V_{OUT} drops.

There are two conditions that can trigger OCP:

1. If V_{OUT} exceeds 3V, V_{FB} drops below 50% of V_{REF}, and V_{OUT} drops below 3V. Then the MP28167-N enters hiccup mode or latch-off mode according to the digital interface setting.
2. If V_{OUT} is below or equal to 3V, and V_{OUT} drops below the under-voltage protection (UV) threshold (typically 50% below V_{REF}), then the MP28167-N enters hiccup mode or latch-off mode according to the digital interface setting.

In hiccup mode, the MP28167-N stops switching and recovers automatically with 12.5% a duty cycle. In latch-off mode, the MP28167-N stops switching until the IC restarts (by cycling the power on VIN or EN, or toggling the EN bit).

Over-Voltage Protection (OVP)

The MP28167-N monitors a resistor-divided V_{FB} to detect whether an output over-voltage (OV) fault has occurred. When V_{FB} exceeds 160% of the target voltage, the over-voltage protection (OVP) comparator output goes high. The output-to-ground discharge resistor turns on.

The OUT pin has an absolute OVP function. Once V_{OUT} exceeds the absolute OVP threshold (23V), the MP28167-N stops switching and the OUT discharge resistor turns on to discharge the output to ground.

Start-Up and Shutdown

If V_{IN} exceeds its UVLO rising threshold and the EN voltage (V_{EN}) exceeds its rising threshold, the device is enabled. The reference block starts up first to generate a stable V_{REF} and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitry.

Three events can shut down the chip: V_{EN} going low, V_{IN} going low, and thermal shutdown. During shutdown, the signaling path is blocked to avoid triggering any faults. Then V_{COMP_BUCK}, V_{COMP_BOOST}, and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Output Discharge

The MP28167-N has an output discharge function that provides a resistive discharge path for the external output capacitor (C_{OUT}). Output discharge is active when the part is disabled (V_{IN} is below the UVLO threshold or EN is off). If VCC is still active, the discharge path turns off when V_{OUT} drops below 50mV or after the 50ms maximum timer has elapsed. Output discharge can also be disabled via the digital interface.

Thermal Warning and Thermal Shutdown

Thermal warning and thermal shutdown prevent the part from operating at exceedingly high temperatures. If the silicon die temperature exceeds 120°C, then the OTW bit is set to 1. Once the temperature falls below its lower threshold (typically 100°C), then the OTW bit is set to 0.

If the silicon die temperature exceeds 150°C, the entire chip shuts down. Once the temperature falls below its lower threshold (typically 130°C), the chip is enabled. Thermal shutdown is a non-latch protection.

DIGITAL INTERFACE

Digital Interface

The digital interface is a two-wire, bidirectional, serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. A master device connected to the line generates the SCL signal and device address to arrange the communication sequence.

The MP28167-N is a digital interface slave, which supports both fast mode (400kHz) and high-speed mode (3.4MHz). The digital interface adds flexibility to the power supply solution. V_{OUT}, the transition slew rate, and other parameters can be controlled instantaneously via the digital interface. If the master sends an 8-bit value, then the 7-bit address should be followed by a 0 or 1 to indicate a write or read operation, respectively.

Start and Stop Commands

Start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and end of the digital interface transfer. A start command is defined as the SDA signal transitioning from high to low while the SCL is high. A stop command is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 9).

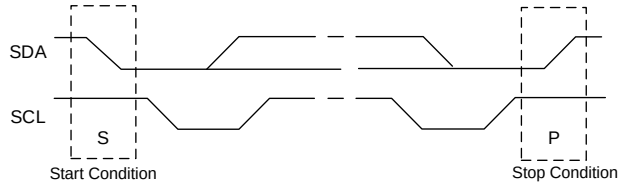


Figure 10: Start and Stop Conditions

The master generates the SCL clocks, then transmits the device address and the read/write (R/W) direction bit on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

Digital Interface Update Sequence

The MP28167-N requires a start condition, valid digital interface address, register address byte, and data byte for a single data update. The MP28167-N acknowledges each byte that has been received by pulling the SDA line low during the high period of a single clock pulse. A valid digital interface address selects the MP28167-N. The MP28167-N performs an update on the falling edge of the LSB byte. Figure 11, Figure 12 on page 28, and Figure 13 on page 28 show examples of digital interface write and read sequences.

Digital Interface Start-Up Timing

Digital interface functionality is enabled once the EN pin is active and V_{IN} exceeds the UVLO rising threshold. The digital interface works during OCP, OVP, and thermal shutdown.

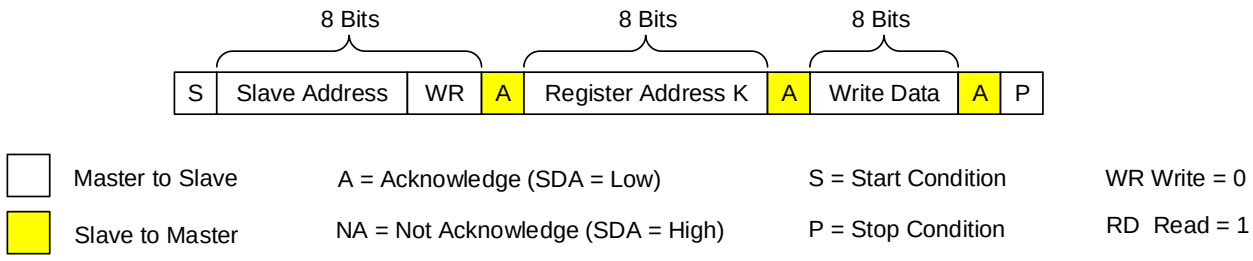


Figure 11: Digital Interface Write Example (Write Single Register)

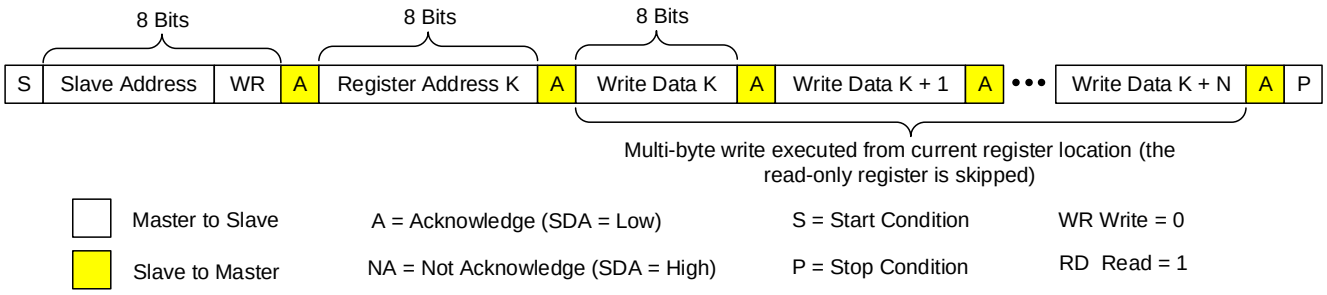


Figure 12: Digital Interface Write Example (Write Multi-Register)

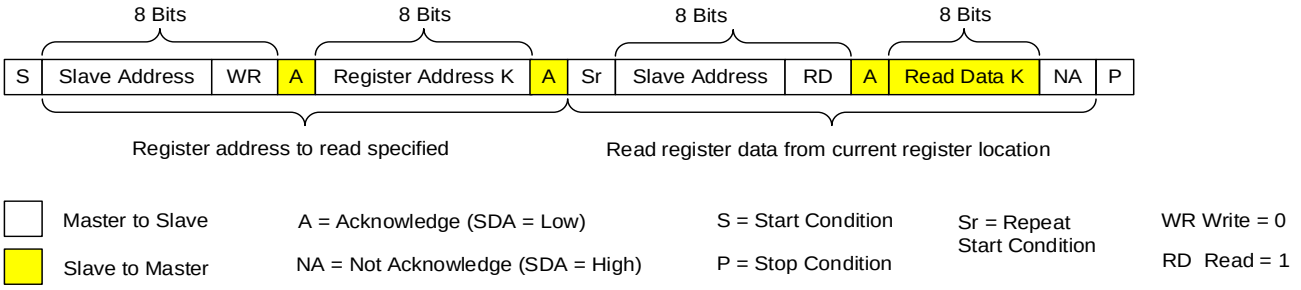


Figure 13: Digital Interface Read Example (Read Single Register)

DIGITAL INTERFACE REGISTER MAP

Add (Hex)	Name	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
00	VREF_L	R/W	RESERVED					VREF_DATA_BIT_LOW [2:0] (11)		
01	VREF_H	R/W	VREF DATA BIT HIGH [10:3] (11)							
02	VREF_GO	R/W	RESERVED						PG_DELAY_EN (11)	GO_BIT
03	IOUT_LIM	R/W	RESERVED	Output current-limit threshold (0A to 6.35A, 50mA step for 21.5kΩ OC resistor) (11)						
04	CTL1	R/W	EN (11)	HICCUP_OCP_OVP (11)	DISCHG_EN (10)	MODE (11)	FREQ (11)		RESERVED	
05	CTL2	R/W	LINE_DROP_COMP (11)		SS (11)		RESERVED			
06	RESERVED	R	RESERVED (all bits are set to “0”)						RESERVED	
07	RESERVED	R	RESERVED							
08	RESERVED	R	RESERVED							
09	Status	R	PG	OTP	OTW	CC_CV	RESERVED			
0A	INTERRUPT	W1C (12)	OTEMPP_ENTER	OT_WARNING_ENTER	OC_ENTER	OC_RECOVER	UVP_FALLING	OTEMPP_EXIT	OT_WARNING_EXIT	PG_RISING
0C	ID1	R	One-time programmable memory configuration code							
27	MFR_ID	R	Manufacturer ID: b ‘0000 1001’							
28	DEV_ID	R	Device ID: b ‘0101 1000’							
29	IC_REV	R	IC revision: b ‘0000 0001’							

Notes:

11) These items have a one-time programmable non-volatile memory. The one-time programmable memory is reloaded to the digital interface register when V_{IN} exceeds the UVLO rising threshold or during a shutdown through EN.
12) Write “0xFF” to this register to reset the interrupt.

REGISTER DESCRIPTION

Digital Interface Bus Slave Address

The MP28167-N digital interface slave address is fixed as 60h.

Output Reference Voltage (V_{REF}) Setting (00h and 01h)

Registers VREF_L H (00h) and VREF_ and (01h) set the reference voltage (V_{REF}), and are in an 11-bit direct format.

Name	VREF															
Format	Direct, unsigned binary integer															
Register Name	N/A					VREF_H D[7:0]								VREF_L D[2:0]		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	N/A					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Function	N/A					Data bit high								Data bit low		
Default Value (1000mV)	N/A					1250 integer										

V_{REF} can be calculated with Equation (1):

$$V_{REF}(mV) = V \times 0.8 \quad (1)$$

Where V is an 11-bit unsigned binary integer of VREF[10:0] between 0 and 2047.

The V_{REF} resolution is 0.8mV/LSB. The V_{REF} changing slew rate is fixed at 0.08mV/µs (see the GO_BIT D[0] section for more details on how to set V_{REF}).

VREF_GO (02h)

The VREF_GO command determines whether the output V_{REF} can be changed based on the output V_{REF} registers 00h and 01h (GO_BIT), and whether power good (PG) has a 100µs rising delay (PG_DELAY_EN).

Bits	Access	Bit Name	Default	Description
D[1]	R/W	PG_DELAY_EN	0	Sets the PG rising delay time. 0: No PG delay 1: PG has a 100µs rising delay
D[0]	R/W	GO_BIT	0	Determines whether the output V_{REF} can be changed based on registers 00h and 01h. 0: V_{REF} cannot be changed 1: V_{REF} can be changed

PG_DELAY_EN

When PG_DELAY_EN = 0, there is no PG delay. When PG_DELAY_EN D[1] = 1, PG experiences a 100µs rising delay. The default value is 0.

GO_BIT

When GO_BIT = 0, V_{REF} does not change. When GO_BIT = 1, V_{REF} changes according to registers 00h and 01h. After V_{REF} scaling is complete, GO_BIT is reset to 0 automatically.

The MP28167-N can be controlled as V_{REF} begins to change. Set GO_BIT to 1 to allow V_{REF} to change according to registers 00h and 01h. When the V_{REF} change is complete (the internal V_{REF} reaches its target value), GO_BIT is reset to 0 automatically. This prevents a false V_{REF} scaling operation.

First write V_{REF} (registers 00h and 01h), and then write GO_BIT to 1. V_{REF} changes based on the new register setting. GO_BIT resets to 0 when V_{REF} reaches its new value. The host can read GO_BIT to

determine whether V_{REF} scaling is complete. Output discharge is enabled when GO_BIT = 1. This causes V_{OUT} to decrease under light-load conditions.

IOUT_LIM (03h)

The IOUT_LIM command sets the output current limit (I_{OUT_LIMIT}) threshold.

Name	IOUT_LIM							
Format	Direct, unsigned binary integer							
Bit	7	6	5	4	3	2	1	0
Access	N/A	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default Value (3.5A)	N/A	70 integer						

IOUT_OC can be calculated with Equation (2):

$$IOUT\_OC(A) = IOUT\_LIM \times 0.05 \quad (2)$$

Where IOUT_LIM is a 7-bit unsigned binary integer of register IOUT_LIM, bits D[6:0]; and the IOUT_OC resolution is 50mA/LSB (6.35A maximum).

The OC resistor connected should be 21.5kΩ when using the IOUT_LIM register. Add a 22nF filter capacitor (C6) on OC to stabilize the constant current (CC) loop. IOUT_LIM can be configured via the digital interface. If the CC threshold should be changed after the MP28167-N has already entered CC limit operation, it is recommended to change the CC threshold step by step (e.g. 50mA per step) instead of changing the current value to the final value.

CTL1 (04h)

The CTL1 command sets the EN bit functionality, over-current protection (OCP) fault response mode, over-voltage protection (OVP) fault response mode, and switching frequency (f_{SW}). It also enables the output discharge function (DISCHG_EN), as well as automatic pulse-frequency modulation (PFM)/pulse-width modulation (PWM) mode or forced PWM.

Bits	Access	Bit Name	Default	Description
D[7]	R/W	EN	1	Enables the device. When the external EN pin is low, the converter is off, and the digital interface shuts down. When EN is high, the EN bit turns the part on or off. 1: Enables the device 0: Disables the device
D[6]	R/W	HICCUP_ OCP_OVP	1	Selects the OCP and OVP fault response mode. 1: Hiccup mode 0: Latch-off mode
D[5]	R/W	DISCHG_EN	1	Enables output discharge. 1: Enabled, output discharge occurs during a shutdown through EN or VIN 0: Disabled
D[4]	R/W	MODE	1	Enables auto-PFM/PWM mode or forced PWM mode. The default is forced PWM mode under light-load conditions. 0: Enables auto-PFM/PWM mode 1: Enables forced PWM mode
D[3:2]	R/W	FREQ	00	Sets f_{SW}. 00: 500kHz 01: 750kHz 10: 1MHz 11: 1.25MHz

CTL2 (05h)

The CTL2 command sets the line drop compensation (LINE_DROP_COMP) and soft-start time (t_{SS}).

Bits	Access	Bit Name	Default	Description
D[7:6]	R/W	LINE_DROP_COMP	00	Sets the V_{OUT} line drop compensation (the compensated voltage [V_{LINE}] vs. the load feature). 00: No compensation 01: V_{OUT} compensates 60mV when I_{OUT} = 3A 10: V_{OUT} compensates 120mV when I_{OUT} = 3A 11: V_{OUT} compensates 200mV when I_{OUT} = 3A V_{OUT} compensation is based on R1 and R2. V_{LINE} can be calculated with the following equation: $V_{LINE} = (1 + R1 / R2) \times V_{REF\_LINE}$ Where V_{REF_LINE} is 0mV when D[7:6] = 00, 12mV when D[7:6] = 01, 24mV when D[7:6] = 10, and 40mV when D[7:6] = 11.
D[5:4]	R/W	SS	10	Sets t_{SS} (V_{OUT} from 0% to 100%). For example, if V_{REF} = 1V, then: 00: 1.1ms 01: 2.2ms 10: 3.5ms 11: 4.4ms The soft-start slew rate is constant. t_{SS} changes with different V_{REF}. For example, t_{SS} = 3.5ms when V_{REF} = 1V, and t_{SS} = 5.25ms when V_{REF} = 1.5V.

STATUS (09h)

The STATUS command monitors and indicates the instantaneous values of PG, over-temperature protection (OTP), over-temperature warning (OTW), and constant current (CC) or constant-voltage (CV) output mode.

Bit	Access	Bit Name	Default	Description
D[7]	R	PG	-	Indicated whether the output power is good. 0: Output power is not good 1: Output power is good
D[6]	R	OTP	-	Indicates whether OTP has occurred. 0: OTP has not occurred 1: OTP has occurred
D[5]	R	OTW	-	Indicates whether OTW has occurred. 0: OTW has not occurred 1: OTW has occurred
D[4]	R	CC_CV	-	Indicates whether the part is operating in CC or CV output mode. 0: CV mode 1: CC mode

INTERRTUPT (0Ah)

The INTERRUPT command indicates the following: OTP entry and exit, die temperature early warning entry and exit, over-current (OC) and CC limit mode, CC limit mode recovery, V_{REF} is below the under-voltage protection (UVP) falling threshold, and the output PG rising edge. This bit is latched once it is triggered. Write “0xFF” to this register to reset all of the interrupts.

Bits	Access	Bit Name	Default	Description
D[7]	W1C	OTEMPP_ ENTER	0	Indicates an OTP entry. When this bit is high, the IC enters thermal shutdown.
D[6]	W1C	OTWARNING_ ENTER	0	Indicates a die temperature early warning entry. When this bit is high, the die temperature exceeds 120°C.
D[5]	W1C	OC_ENTER	0	Indicates whether the part is in OC or CC limit mode.
D[4]	W1C	OC_RECOVER	0	Indicates CC limit mode recovery.
D[3]	W1C	UVP_FALLING	0	Indicates V_{REF} is below the UVP falling threshold.
D[2]	W1C	OTEMPP_EXIT	0	Indicates an OTP exit.
D[1]	W1C	OTWARNING_ EXIT	0	Indicates a temperature early warning exit. When the die temperature is below 100°C, this bit is set to 1.
D[0]	W1C	PG_RISING	0	Output PG rising edge.

APPLICATION INFORMATION

Setting the Output Voltage (V_{OUT})

The external resistor divider sets V_{OUT}. R1 can be calculated with Equation (1):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (1)$$

Figure 14 shows the feedback circuit.

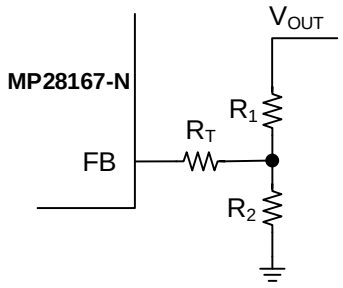


Figure 14: Feedback Network

If the digital interface is not used to set V_{OUT}, it can be set by R1, R2, and R_T. Table 1 lists the recommended resistances and inductance for common output voltages.

Table 1: Recommended Resistances and Inductance for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (μH)
5	430	107	806	4.7
9	430	53.6	787	4.7
12	430	39.2	787	4.7
15	402	28.7	402	4.7
20	390	20.5	200	3.3

Selecting the Inductor

Inductor selection is based on the operation mode. The inductance in buck mode (L_{BUCK}) can be estimated with Equation (2):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current, which is 30% to 50% of the maximum load current.

In boost mode, inductor selection is based on ΔI_L, which should be between 30% and 50% of the maximum I_{IN}.

The inductance in boost mode (L_{BOOST}) can be estimated with Equation (3):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (3)$$

A larger-value inductor reduces the ripple current; however, a larger-value inductor is also physically larger. A large inductance can also reduce the converter's bandwidth by moving the right half-plane zero to lower frequencies. This tradeoff should be determined based on the application requirements.

The inductor should support the peak current to avoid saturation. The peak current in buck mode (I_{PEAK_BUCK}) can be calculated with Equation (4)

$$I_{PEAK\_BUCK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{2 \times V_{IN\_MAX} \times f_{SW} \times L} \quad (4)$$

The peak current in boost mode (I_{PEAK_BOOST}) can be calculated with Equation (5):

$$I_{PEAK\_BOOST} = \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN\_MIN}} + \frac{V_{IN\_MIN} \times (V_{OUT} - V_{IN\_MIN})}{2 \times V_{OUT} \times f_{SW} \times L} \quad (5)$$

Where η is the MP28167-N's estimated efficiency.

A 4.7μH inductor is recommended for applications with a 500kHz f_{SW}, and a 3.3μH inductor is recommended for applications with a 750kHz f_{SW}.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists the recommended power inductors.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
Select family series (MPL-AL)	2.2μH to 4.7μH	MPS
MPL-AL6050-4R7	4.7μH	MPS
MPL-AL6050-3R3	3.3μH	MPS
MPL-AL5030-2R2	2.2μH	MPS

Visit MonolithicPower.com for more information.

Selecting the Input and Output Capacitors

It is recommended to use ceramic capacitors with an electrolytic capacitor at the input to filter the input ripple current and achieve stable operation.

Since the input capacitor (C_{IN}) absorbs the input switching current, it requires sufficient capacitance. For most applications, a 100µF electrolytic capacitor and a 22µF ceramic capacitor are sufficient.

The output capacitor (C_{OUT}) stabilizes the DC V_{OUT}. A sufficient capacitance is recommended to limit the V_{OUT} ripple (ΔV_{OUT}). The ceramic C_{OUT} should be ≥22µF x 8.

Place C_{IN} and C_{OUT} as close to the device as possible.

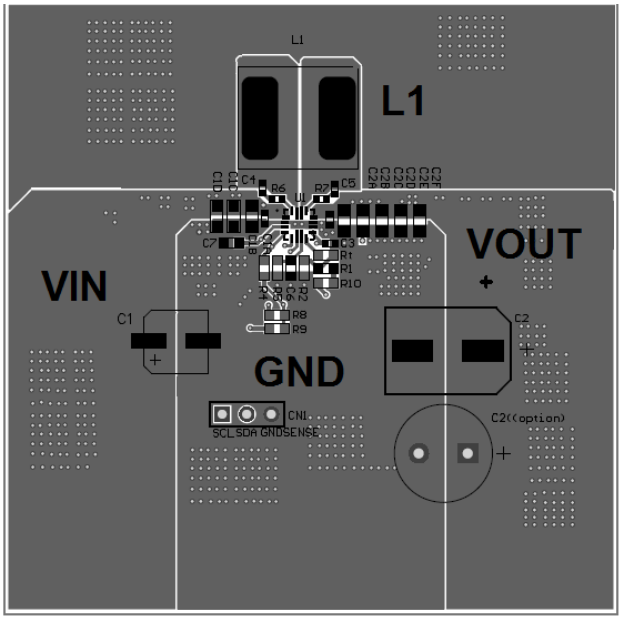
PCB Layout Guidelines [13]

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 15 and follow the guidelines below:

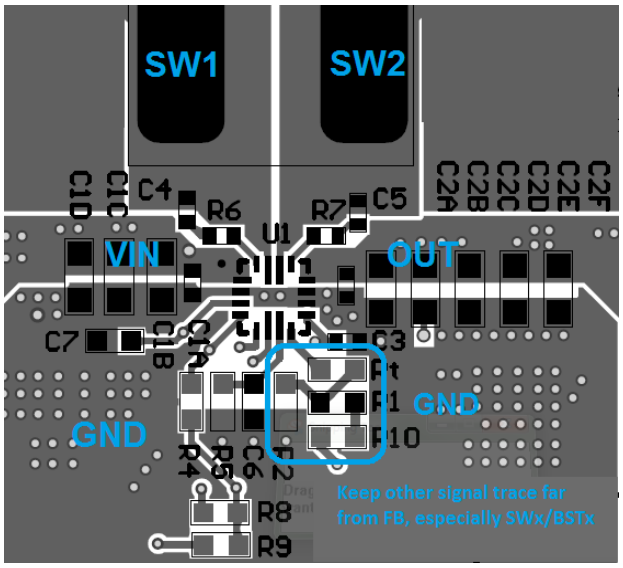
1. Place the ceramic C_{IN} and C_{OUT} close to the VIN and OUT pins, respectively.
2. Use a large copper plane for PGND.
3. Add multiple vias to improve thermal dissipation.
4. Connect AGND to PGND.
5. Connect OUT using short, direct, and wide traces.
6. Add vias under the IC.
7. It is highly recommended to route the OUT trace on both PCB layers.
8. Use a large copper plane for SW1 and SW2.
9. Place the VCC decoupling capacitor as close to VCC as possible.
10. The FB trace requires special consideration. Use a ground copper to cover this trace.
11. Route the FB trace away from other signal traces (such as SWx and BSTx).

Note:

13) The recommended PCB layout is based on Figure 16 on page 36.



Top Layer



Close-Up of Layout

Figure 15: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

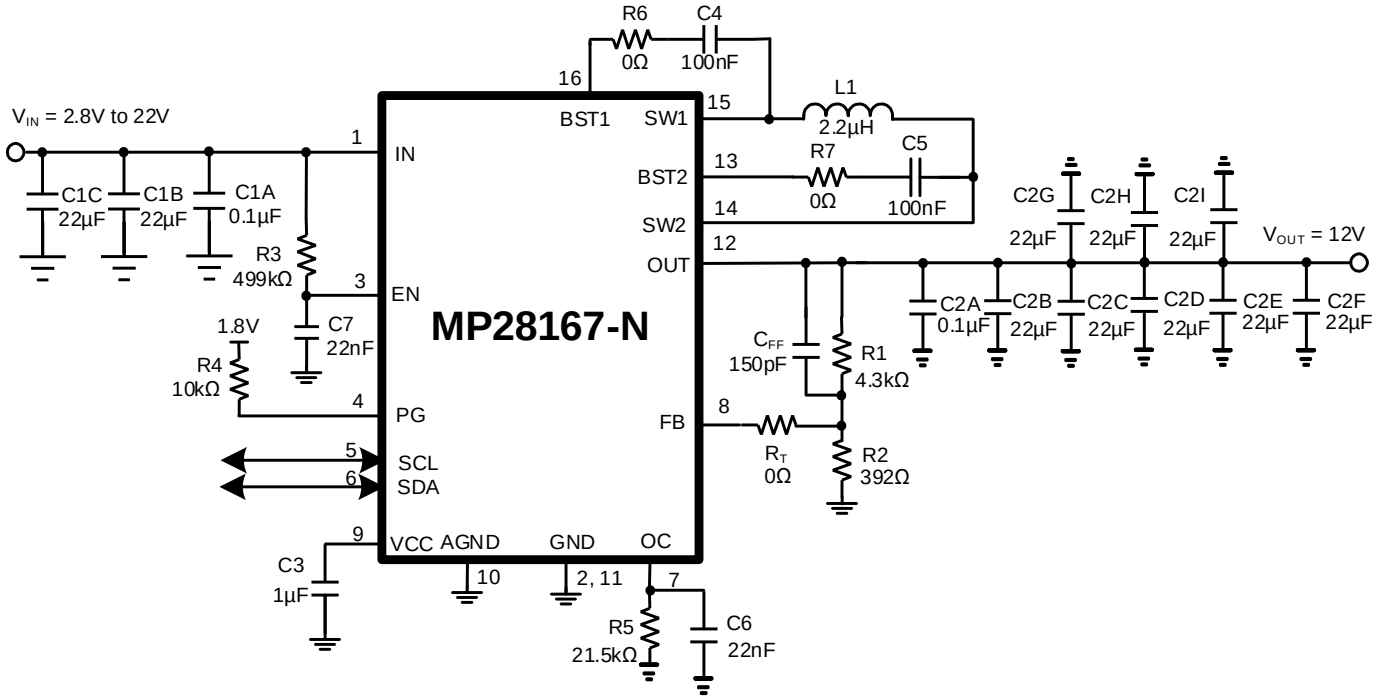
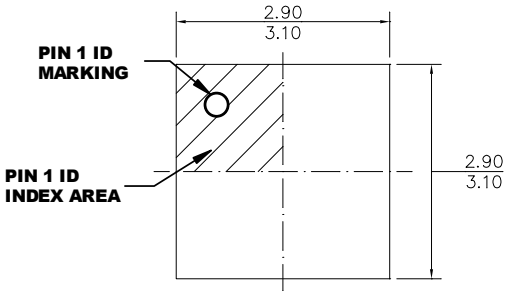


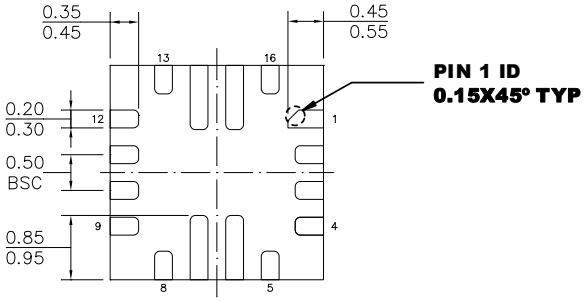
Figure 16: Typical Application Circuit (V_{OUT} = 12V)

PACKAGE INFORMATION

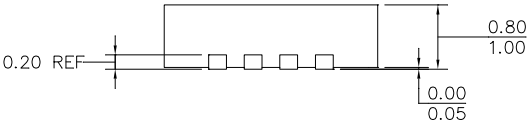
QFN-16 (3mmx3mm)



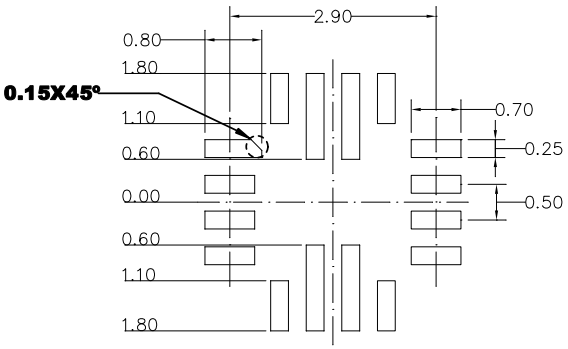
TOP VIEW



BOTTOM VIEW



SIDE VIEW

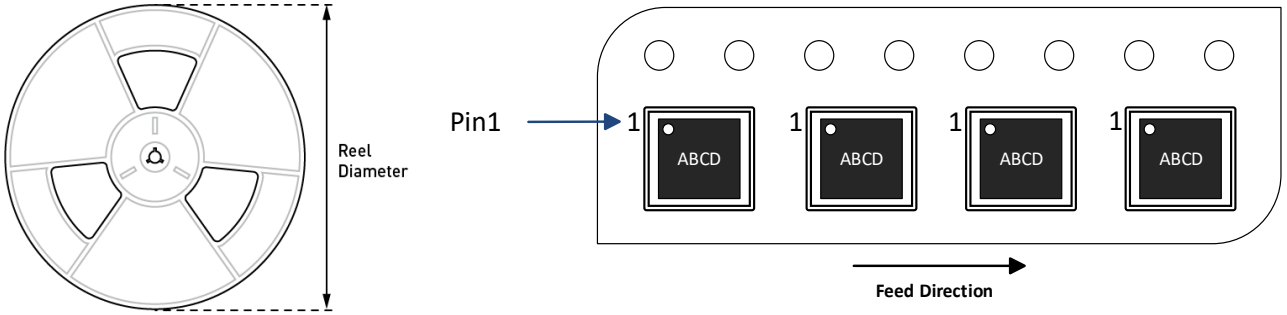


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP28167GQ -N-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13 in	12 mm	8 mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	10/24/2023	Initial Release	-