# MP2980

## 36V, Synchronous Buck-Boost Controller with Digital Interface and Current Monitor

## DESCRIPTION

The MP2980 is a synchronous, four-switch, buck-boost controller capable of regulating different output voltages with a wide input voltage ($V_{IN}$) range and high efficiency. The MP2980 provides a digital interface that supports output voltage ($V_{OUT}$) configuration, $V_{OUT}$ slew-rate control, and constant output current ($I_{OUT}$) limit configuration. This makes the MP2980 well-suited for USB power delivery (PD) designs in USB Type-C power supplies.

The MP2980 uses valley current control in buck mode and peak current control in boost mode to provide fast load transient response and smooth buck-boost mode transients. The MP2980 provides forced continuous conduction mode (FCCM) and a configurable average current limit, which support flexible designs for different applications.

The MP2980 also provides configurable over-current protection (OCP), over-voltage protection (OVP), and $V_{IN}$ under-voltage lockout (UVLO) hysteresis.

The MP2980 is available in a QFN-32 (4mmx4mm) package.

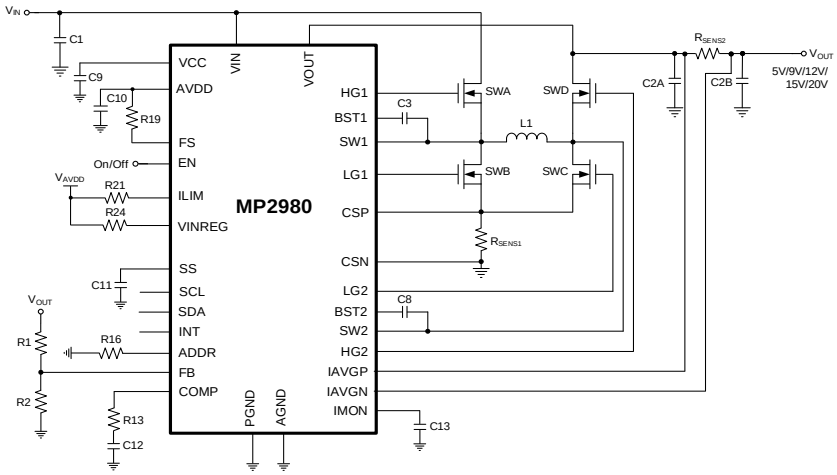
## FEATURES

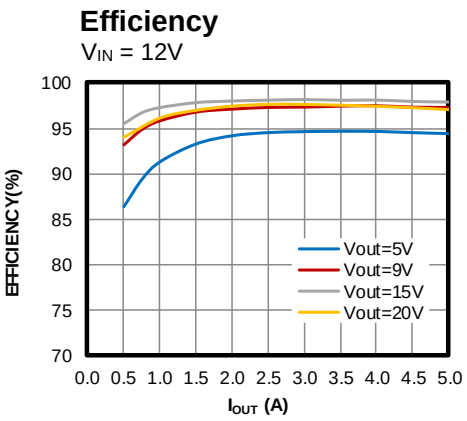
- 6V to 36V Start-Up Input Voltage ($V_{IN}$) Range
- 5V to 36V Operating $V_{IN}$ Range
- Flexible Digital Interface Control:
  - 0.5V to 28V Output Voltage ($V_{OUT}$) Range
  - 0.3V to 2.047V Reference Voltage ($V_{REF}$) Range with 1mV Step
- Selectable $V_{OUT}$ Slew Rate
- Configurable Constant Current Limit
- Output Current ($I_{OUT}$) Monitor Function (IMON)
- Configurable Soft-Start Time ($t_{SS}$)
- Switching Frequency Spread Spectrum (FSS) for EMI Optimization
- Integrated $V_{OUT}$ Discharge Function
- Selectable 200kHz, 300kHz, 400kHz, and 600kHz Switching Frequency ($f_{SW}$)
- Forced Continuous Conduction Mode (FCCM)
- Configurable $V_{IN}$ Under-Voltage Lockout (UVLO) Hysteresis
- Minimum $V_{IN}$ Regulation
- Over-Current Protection (OCP), Short-Circuit Protection (SCP), and Over-Voltage Protection (OVP)
- Interrupt Indicator for OCP, OVP, and $V_{OUT}$ Power Not Good (PNG)
- Available in a QFN-32 (4mmx4mm) Package

## APPLICATIONS

- USB Power Delivery (PD)
- Industrial PC Power Supplies
- Supercapacitor Charging

## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP2980GR | QFN-32 (4mmx4mm) | *See Below* | 1 |
| EVKT-MP2980 | Evaluation kit | N/A | N/A |

* For Tape & Reel, add suffix -Z (e.g. MP2980GR-Z).

## TOP MARKING

MPSYWW
MP2980
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
MP2980: Part number
LLLLLL: Lot number

## EVKT-MP2980 EVALUATION KIT

EVKT-MP2980 kit contents (items below can be ordered separately).

| # | Part Number | Item | Quantity |
|---|---|---|---|
| 1 | EV2980-R-00A | MP2980GR evaluation board | 1 |
| 2 | EVKT-USBI2C-02 bag | Includes one USB to digital communication interface device, one USB cable, and one ribbon cable | 1 |

**Order directly from MonolithicPower.com or our distributors.**

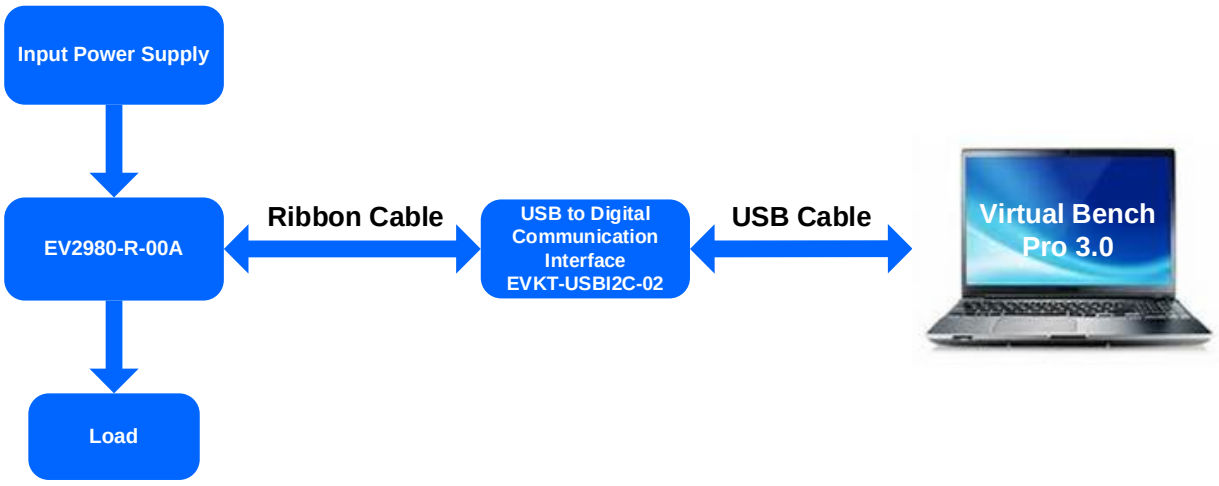
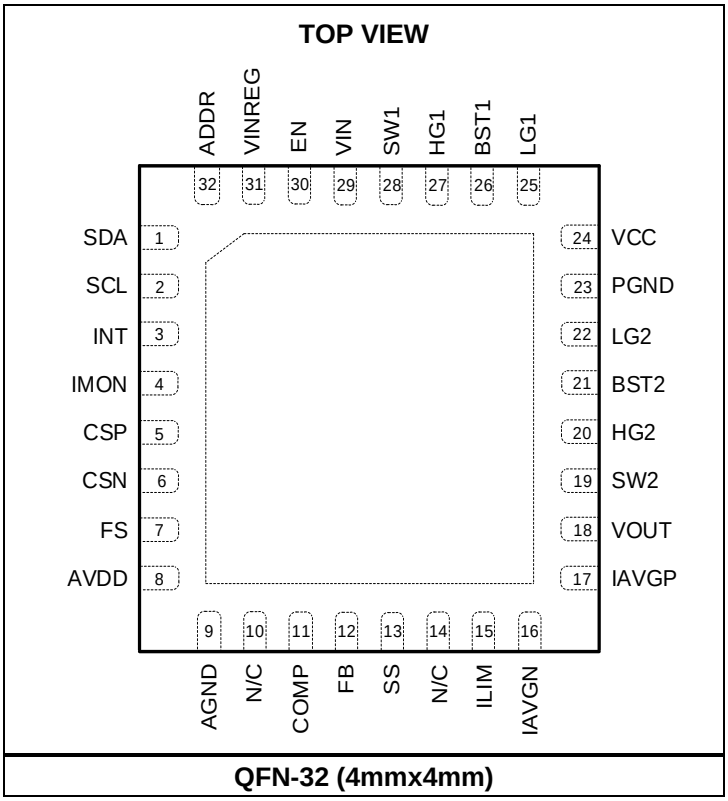



**Figure 1: EVKT-MP2980 Evaluation Kit Set-Up**

# PACKAGE REFERENCE




**QFN-32 (4mmx4mm)**

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | SDA | **Digital interface data signal.** |
| 2 | SCL | **Digital interface clock signal.** |
| 3 | INT | **Interrupt for power not good (PNG), over-current protection (OCP), over-temperature protection (OTP), and over-voltage protection (OVP) events.** In the default set-up, the INT pin is masked off in response to a PNG event. INT is an open-drain output and is pulled low if an interrupt event occurs. Once the fault is removed, INT recovers to open drain. INT is also an open drain when the IC is not enabled. |
| 4 | IMON | **Current monitor output.** The IMON pin indicates the signal between the IAVGP and IAVGN pins. |
| 5 | CSP | **Positive input of the switching current-sense signal.** Connect the CSP pin to the high side of the current-sense resistor. |
| 6 | CSN | **Negative input of the switching current-sense signal.** Connect the CSN pin to the low side of the current-sense resistor. |
| 7 | FS | **Register bits FSW[7:6] default value configuration.** The FS pin provides two different voltage levels during start-up to set the default FS voltage ($V_{FS}$):<br>$V_{FS1}$: 0.51 x AVDD to 0.68 x AVDD, FSW = 00 (200kHz)<br>$V_{FS2}$: 0.74 x AVDD or above, FSW = 10 (400kHz)<br>FS cannot be floated or connected to ground. See the Electrical Characteristics section on page 8 for different voltage settings. Changing the voltage level of FS after start-up does not affect register bits FSW[7:6]. These bits can be changed via the digital interface after start-up. |
| 8 | AVDD | **Internal control circuit bias supply.** Decouple the AVDD pin with a ≥2.2µF capacitor. |
| 9 | AGND | **Analog ground.** |
| 10, 14 | N/C | **No internal connection.** |
| 11 | COMP | **Internal error amplifier output.** Connect the COMP pin to a capacitor and a resistor in series with AGND for loop compensation. |
| 12 | FB | **Output voltage ($V_{OUT}$) feedback.** Connect a resistor divider between the FB and VOUT pins. |
| 13 | SS | **Soft-start configuration.** Connect the SS pin to an external capacitor. SS also sets the off time in hiccup. |
| 15 | ILIM | **Register bits ILIM[2:0] default value configuration.** The ILIM pin provides four different voltage levels during start-up to set the default ILIM voltage ($V_{ILIM}$):<br>$V_{ILIM1}$: ILIM = 001 (33.3mV)<br>$V_{ILIM2}$: ILIM = 011 (45.1mV)<br>$V_{ILIM3}$: ILIM = 101 (56.8mV)<br>$V_{ILIM4}$: ILIM = 111 (68.7mV)<br>Float ILIM to set ILIM = 001 by default. See the Electrical Characteristics section on page 8 for different voltage settings. Changing the voltage level of ILIM after start-up does not affect either the register bits ILIM[2:0] or the current limit threshold. These bits can be changed via the digital interface after start-up. |
| 16 | IAVGN | Negative terminal of average current limit sense input. The IAVGN pin can only be used to set the output current **($I_{OUT}$)** limit by connecting the pin to the positive terminal of the output rail. |
| 17 | IAVGP | **Positive terminal of average current limit sense input.** The IAVGP pin can only be used to set the $I_{OUT}$ limit by connecting the pin to the positive terminal of the output rail. |
| 18 | VOUT | **$V_{OUT}$ sense input.** The VOUT pin supplies power to VCC based on the VCC power logic. Connect VOUT to the output capacitor ($C_{OUT}$). |

## PIN FUNCTIONS *(continued)*

| Pin # | Name | Description |
|---|---|---|
| 19 | SW2 | **Boost switch node of the controller.** Connect the SW2 pin to the SWD source and the SWC drain. |
| 20 | HG2 | **Boost high-side MOSFET (HS-FET) gate driver.** Connect the HG2 pin directly to the SWD gate. |
| 21 | BST2 | **Bootstrap power for boost HS-FET gate driver.** Connect a capacitor between the BST2 and SW2 pins. BST2 is supplied by either VCC or BST1. |
| 22 | LG2 | **Boost low-side MOSFET (LS-FET) gate driver.** Connect the LG2 pin directly to the SWC gate. |
| 23 | PGND | **Power ground.** The PGND pin provides the gate-driving current return. |
| 24 | VCC | **Driver circuit and internal bias supply.** Place a ≥2.2μF decoupling ceramic capacitor as close to the VCC pin as possible. VCC is powered by the input voltage ($V_{IN}$) or output voltage ($V_{OUT}$). |
| 25 | LG1 | **Buck LS-FET gate driver.** Connect the LG1 pin directly to the SWB gate. |
| 26 | BST1 | **Bootstrap power for buck HS-FET gate driver.** Connect a capacitor between the BST1 and SW1 pins. BST1 is supplied by VCC or BST2. |
| 27 | HG1 | **Buck HS-FET gate driver.** Connect the HG1 pin directly to the SWA gate. |
| 28 | SW1 | **Buck switch node of the controller.** Connect the SW pin to the SWA source and the SWB drain. |
| 29 | VIN | **Input power supply and voltage sense input.** |
| 30 | EN | **Chip enable control.** If not used, connect the EN pin to the input source for automatic start-up. EN can also configure $V_{IN}$ under-voltage lockout (UVLO). Do not float this pin. |
| 31 | VINREG | **VIN regulation.** The VINREG pin sets the minimum operating $V_{IN}$ during switching. If not used, connect VINREG to AVDD. |
| 32 | ADDR | **Digital interface slave address setting.** The ADDR pin sets the default value of the ENPWR bit. |

## ABSOLUTE MAXIMUM RATINGS (1)

VIN, EN .....-0.3V to +40V
VOUT, IAVGP, IAVGN .....-0.3V to +30V
VCC .....-0.3V to +8.5V
SW1, SW2 .....
.....-1V to +40V (-5V to +45V for <20ns)
LG1, LG2 .....
.....-0.3V to +10V (-2V to +11V for <20ns)
BST1, HG1 ..... -0.3V to $V_{SW1}$ + 8.5V
BST2, HG2 ..... -0.3V to $V_{SW2}$ + 8.5V
All other pins……..0.3V to +6.5V
Continuous power dissipation (2) (5)……4.4W
Junction temperature ($T_J$)……150°C
Lead temperature……..260°C
Storage temperature……..-65°C to +150°C

### *ESD Ratings* (4)

Human body model (HBM)…….±2000V
Charged-device model (CDM)…….±2000V

### *Recommended Operating Conditions* (3)

Start-up voltage ($V_{ST}$)……6V to 36V
Operating voltage ($V_{IN}$) (5)……..5V to 36V
Output voltage ($V_{OUT}$)……..0.5V to 28V
Operating junction temp ($T_J$)….-40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| EV2980-R-00A (6) | 28 | 8 °C/W |
| JESD51-7 (7) | 42 | 9 °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101, AEC specification AEC-Q100-011. The JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. The JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. HBM is with regard to ground.
5) The operating voltage after $V_{OUT}$ is regulated to a minimum 5V voltage, and the VCC load is below 10mA.
6) Measured on the EV2980-R-00A: a 6-layer, 2oz-1oz-1oz-1oz-1oz-2oz PCB (91.4mmx66mm).
7) The $\theta_{JA}$ value given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 12V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C [8], typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Operating VCC voltage | $V_{CC}$ | $V_{IN}$ = 6V or $V_{OUT}$ = 6V, 0mA to 20mA on VCC | 5.1 | 5.95 | 6 | V |
| | | $V_{IN}$ = 12V or $V_{OUT}$ = 12V, 0mA to 60mA on VCC | 6.7 | 7.2 | 7.7 | V |
| Input voltage ($V_{IN}$) under-voltage lockout (UVLO) [9] | $V_{IN\_UVLO\_R}$ | $V_{IN}$ rising | 5 | 5.5 | 5.9 | V |
| $V_{CC}$ UVLO [9] | $V_{CC\_UVLO\_F}$ | $V_{CC}$ falling | 3.8 | 4.3 | 4.8 | V |
| VCC power source change threshold | $V_{IN\_TH\_VCC}$ | $V_{OUT}$ = 12V, ramp $V_{IN}$ from 5V to 10V | 8.1 | 8.8 | 9.5 | V |
| | $V_{OUT\_TH\_VCC}$ | $V_{IN}$ = 12V, ramp $V_{OUT}$ from 5V to 10V | 8.1 | 8.8 | 9.5 | V |
| AVDD voltage | $V_{AVDD}$ | $V_{IN}$ = 12V, 0mA to 5mA | 4.7 | 5.2 | 5.6 | V |
| Shutdown current | $I_{SD}$ | $V_{EN}$ = 0V, measured on the VIN and VOUT pins | | | 5 | µA |
| | | ENPWR = 0, $V_{IN}$ = 12V, $V_{OUT}$ = 0V, measured on VIN, $V_{EN}$ = 2V | 300 | 510 | 800 | µA |
| **Enable Control (EN Pin)** | | | | | | |
| EN turn-on threshold | $V_{EN\_ON}$ | $V_{EN}$ rising (switching) | 1.25 | 1.35 | 1.45 | V |
| EN high threshold | $V_{EN\_H}$ | $V_{EN}$ rising (micro-power) | | | 1.1 | V |
| EN low threshold | $V_{EN\_L}$ | $V_{EN}$ falling (micro-power) | 0.4 | | | V |
| EN turn-on hysteresis current | $I_{EN\_HYS}$ | EN > $V_{EN\_ON}$, EN source current | 3.2 | 4.7 | 6.2 | µA |
| EN input current | $I_{EN}$ | $V_{EN}$ = 0V, 3.3V | | 0.01 | | µA |
| ENPWR turn-on delay [10] | $t_{ENPWR\_DELAY}$ | From ENPWR = 1 to switching, $C_{SS}$ = 47nF | | 1 | | ms |
| **Feedback (FB) Control** | | | | | | |
| Reference voltage | $V_{REF}$ | VREF = 7FFH, $T_J$ = 25°C | -1% | 2.047 | +1% | V |
| | | VREF = 7FFH, $T_J$ = -40°C to +125°C | -2% | 2.047 | +2% | V |
| | | VREF = 1F4H, $T_J$ = 25°C | -2% | 0.5 | +2% | V |
| | | VREF = 1F4H, $T_J$ = -40°C to +125°C | -3% | 0.5 | +3% | V |
| FB input current | $I_{FB}$ | $V_{FB}$ = 0.52V | | | 200 | nA |
| Error amplifier transconductance | $G_{EA}$ | $V_{FB}$ = $V_{REF}$ + 10mV, $V_{COMP}$ = 2.5V | | 1220 | | µA/V |
| Compensation to current-sense gain [10] | $G_{CS}$ | $\Delta V_{CS}$ / $\Delta V_{COMP}$ | | 200 | | mV/V |
| SS charge current | $I_{CHG\_SS}$ | During soft start and overload recovery | 2 | 6 | 10 | µA |
| SS discharge current | $I_{DSG\_SS}$ | After hiccup protection is triggered | | 1 | | µA |
| VREF change slew rate | $t_{REF}$ | SR = 00 | 25 | 38 | 51 | mV/ms |
| | | SR = 11 | 130 | 150 | 170 | mV/ms |
| VINREG reference voltage | $V_{VINREG\_REF}$ | $T_J$ = 25°C | 1.188 | 1.2 | 1.212 | V |
| | | $T_J$ = -40°C to +125°C | 1.182 | 1.2 | 1.218 | V |
| VINREG input current | $I_{VINREG}$ | $V_{VINREG}$ = 1.25V | | | 50 | nA |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 12V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C (8), typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Current Limit** | | | | | | |
| Buck valley current limit | $I_{LIMIT\_BUCK}$ | | 113 | 133 | 153 | mV |
| Boost peak current limit | $I_{LIMIT\_BOOST}$ | | 130 | 150 | 170 | mV |
| Over-current protection (OCP) hiccup threshold (10) | $V_{TH\_OCP}$ | | | 60 | | % of $V_{REF}$ |
| Average constant current limit | $I_{AV\_LIMIT}$ | ILIM = 011, $V_{IAVGN}$ = 12V, ramp up $V_{IAVGP}$ | 40 | 45 | 50 | mV |
| | | ILIM = 111, $V_{IAVGN}$ = 12V, ramp up $V_{IAVGP}$ | 62.5 | 68 | 73.5 | mV |
| CSP and CSN bias current | $I_{CS\_BIAS}$ | $V_{CSP}$ = $V_{CSN}$ = 0V | | 70 | | µA |
| IAVGP and IAVGN bias current | $I_{AV\_BIAS}$ | $V_{IAVGN}$ = 5V, $V_{IAVGN}$ = 20V, IAVGP - IAVGN = 40mV | | 55 | | µA |
| **Switching Frequency** | | | | | | |
| Switching frequency | $f_{SW}$ | FSW = 10, $V_{OUT}$ = 5V | 300 | 400 | 500 | kHz |
| | | FSW = 00, $V_{OUT}$ = 5V | 140 | 200 | 260 | kHz |
| Frequency spread spectrum (FSS) span (10) | $f_{SS}$ | DITHER = 1 | | ±6 | | % of $f_{SW}$ |
| FSS modulation frequency (10) | $f_{MODULATION}$ | DITHER = 1 | | 2 | | kHz |
| **Gate Driver** | | | | | | |
| Gate source current capability (10) | $I_{HG\_SO}$ | $V_{CC}$ = 7.2V, 4.7nF load | | 0.7 | | A |
| | $I_{LG\_SO}$ | | | 0.85 | | A |
| Gate sink current capability (10) | $I_{HG\_SI}$ | $V_{CC}$ = 7.2V, 4.7nF load | | 1.6 | | A |
| | $I_{LG\_SI}$ | | | 2 | | A |
| Low-side (LS) gate output high voltage | $V_{LS\_HIGH}$ | | $V_{CC}$ - 0.05 | | | V |
| LS gate output low voltage | $V_{LS\_LOW}$ | | | | 0.05 | V |
| High-side (HS) gate output high voltage | $V_{HS\_HIGH}$ | | $V_{BST-SW}$ - 0.05 | | | V |
| HS gate output low voltage | $V_{HS\_LOW}$ | | | | 0.05 | V |
| Dead time between the HS gate and LS gate (10) | $t_{DEAD}$ | | | 30 | | ns |
| **Over-Voltage Protection (OVP)** | | | | | | |
| FB OVP trigger threshold | $V_{OVP\_RISING}$ | | 119 | 127 | 135 | % of $V_{REF}$ |
| FB OVP recovery threshold | $V_{OVP\_FALLING}$ | | 104 | 111 | 118 | % of $V_{REF}$ |
| **Thermal Protection** | | | | | | |
| Thermal shutdown (10) | $T_{SD}$ | | | 150 | | °C |
| Thermal shutdown hysteresis (10) | $T_{SD\_HYS}$ | | | 25 | | °C |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 12V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C [8], typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Good (PG) (INT Pin)** | | | | | | |
| PG upper trip threshold | $PG_{H\_FALLING}$ | PNG = 1, INT pulls low | 110 | 117 | 124 | % of $V_{REF}$ |
| | $PG_{H\_RISING}$ | PNG = 0, INT pulls high | 101 | 106.5 | 112 | % of $V_{REF}$ |
| PG lower trip threshold | $PG_{L\_FALLING}$ | PNG = 1, INT pulls low | 80 | 85.5 | 91 | % of $V_{REF}$ |
| | $PG_{L\_RISING}$ | PNG = 0, INT pulls high | 85 | 91 | 97 | % of $V_{REF}$ |
| PG delay (INT response to PNG event) | $t_{PG\_DELAY}$ | Low to high | | 10 | | µs |
| | | $V_{OUT}$ under-voltage (UV), high to low | | 2 | | µs |
| | | $V_{OUT}$ over-voltage (OV), high to low | | 6.5 | | µs |
| INT sink current capability | $I_{SINK\_INT}$ | Sink 4mA | | 0.1 | 0.4 | V |
| INT leakage current | $I_{LKG\_INT}$ | $V_{INT}$ = 5V | | | 1 | µA |
| **Digital Interface** | | | | | | |
| Input logic low voltage | $V_{LI}$ | SCL, SDA | | | 0.8 | V |
| Input logic high voltage | $V_{HI}$ | SCL, SDA | 2 | | | V |
| Logic input current | $I_{SCL\_SDA\_LKG}$ | SCL/SDA = 5V | -1 | | +1 | µA |
| Output Logic Low Voltage | $V_{LO}$ | SDA, sink 4mA | | | 0.4 | V |
| **ADDR and ILIM Pin Setting Thresholds** | | | | | | |
| ADDR configuration voltage level 1 | $V_{ADDR1}$ | Set digital interface address 60H | | | 0.23 | AVDD |
| ADDR configuration voltage level 2 | $V_{ADDR2}$ | Set digital interface address 62H | 0.27 | | 0.47 | AVDD |
| ADDR configuration voltage level 3 | $V_{ADDR3}$ | Set digital interface address 64H | 0.51 | | 0.68 | AVDD |
| ADDR configuration voltage level 4 | $V_{ADDR4}$ | Set digital interface address 66H | 0.74 | | | AVDD |
| ADDR/ILIM to ground pull-down resistor | | | | 2 | | MΩ |
| **FS Pin Setting Threshold** | | | | | | |
| FS configuration voltage level 1 | $V_{FS1}$ | FSW =00 | 0.51 | | 0.68 | AVDD |
| FS configuration voltage level 2 | $V_{FS2}$ | FSW =10 | 0.74 | | | AVDD |
| **Current Monitor Function** | | | | | | |
| IMON output voltage gain | $G_{IMON}$ | 5mV IAVG sense voltage | | 18.8 | | V/V |
| | | 55mV IAVG sense voltage | 16.92 | 18.8 | 20.68 | V/V |

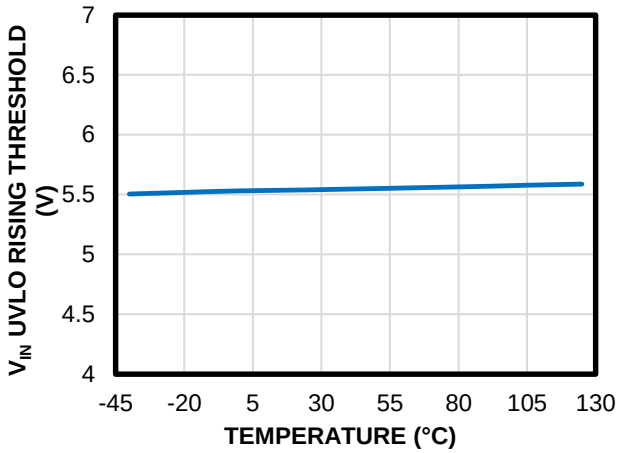
**Notes:**

8) Not tested in production. Guaranteed by over-temperature correlation.
9) The MP2980 has a 6V minimum start-up voltage, and the $V_{IN}$ UVLO falling threshold is below the $V_{CC}$ UVLO falling threshold.
10) Guaranteed by engineer sample characterization.

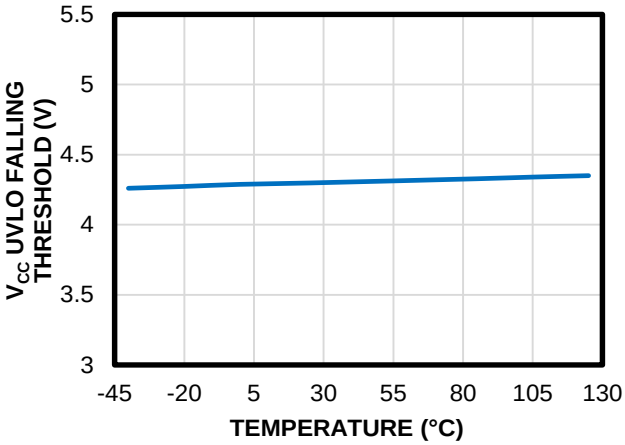
## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

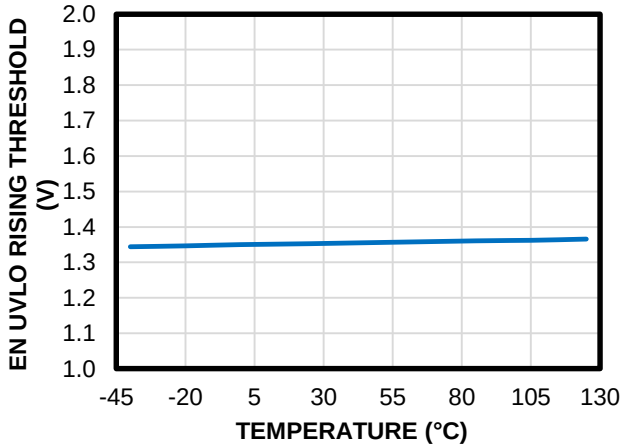
**$V_{IN}$ UVLO Rising Threshold vs. Temperature**



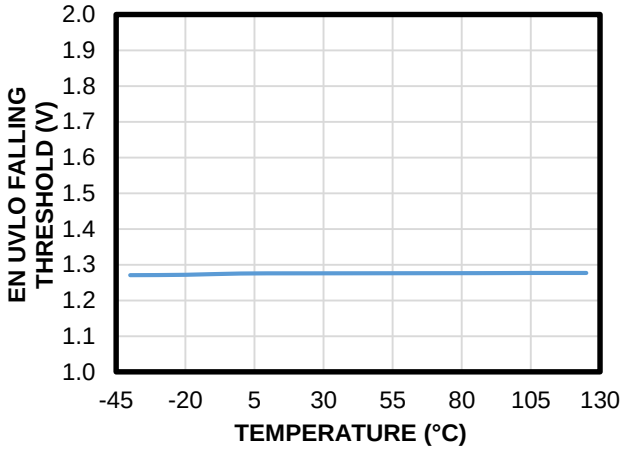

**$V_{CC}$ UVLO Falling Threshold vs. Temperature**



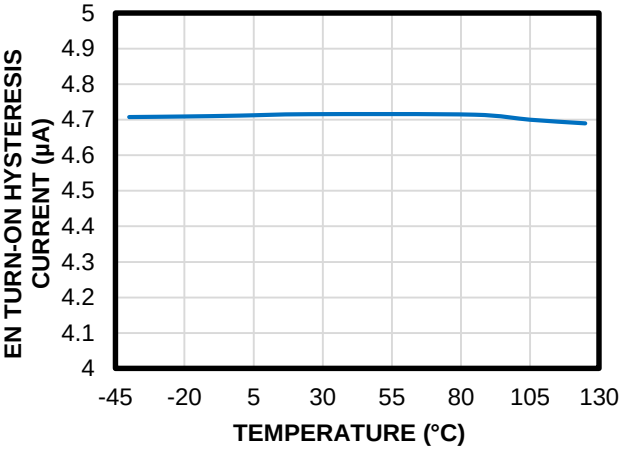

**EN UVLO Rising Threshold vs. Temperature**



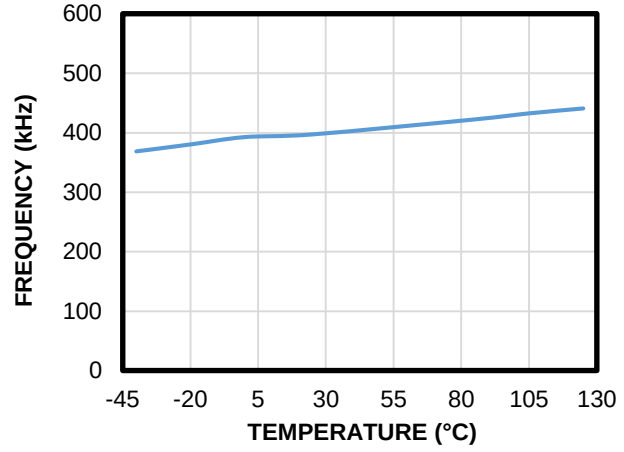

**EN UVLO Falling Threshold vs. Temperature**




**EN Turn-On Hysteresis Current vs. Temperature**



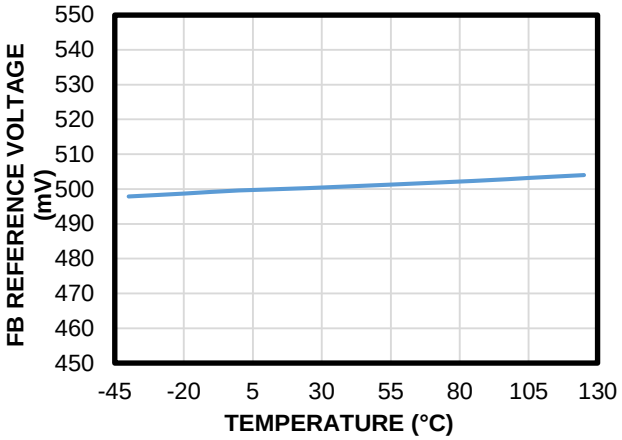

**Frequency vs. Temperature**



## TYPICAL CHARACTERISTICS *(continued)*

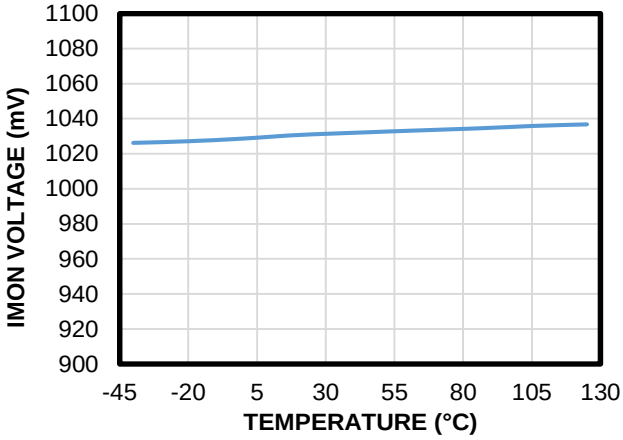
**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

### FB Reference Voltage vs. Temperature

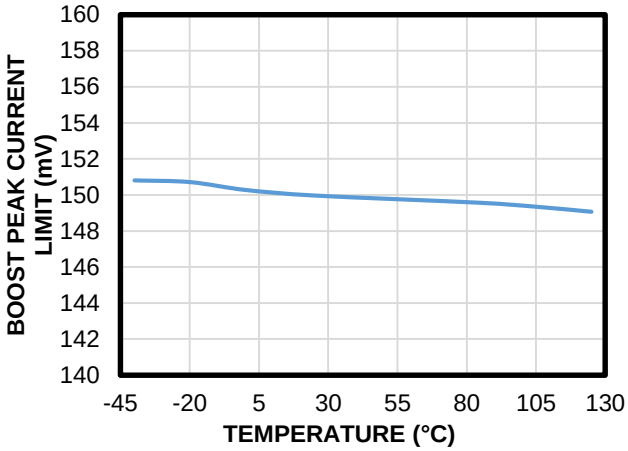



### IMON Voltage vs. Temperature

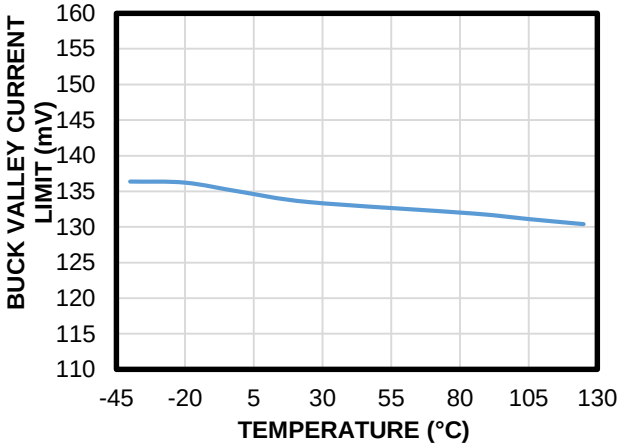
$V_{IAVGP}$ - $V_{IAVGN}$ = 55mV



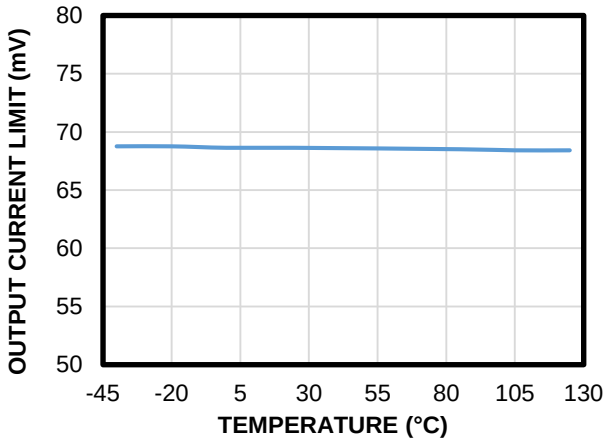

### Boost Peak Current Limit vs. Temperature




### Buck Valley Current Limit vs. Temperature




### Output Current Limit (ILIM = 111) vs. Temperature

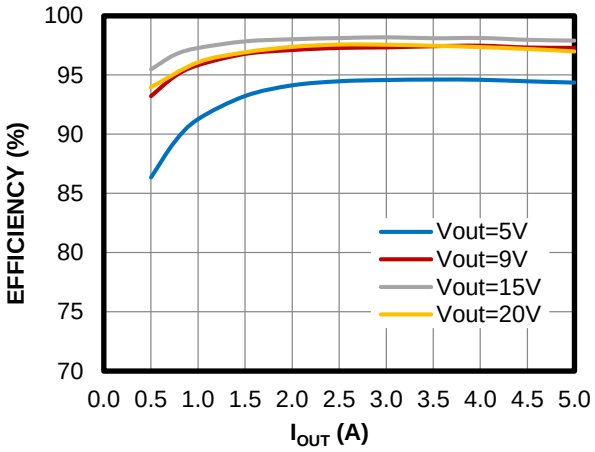


## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

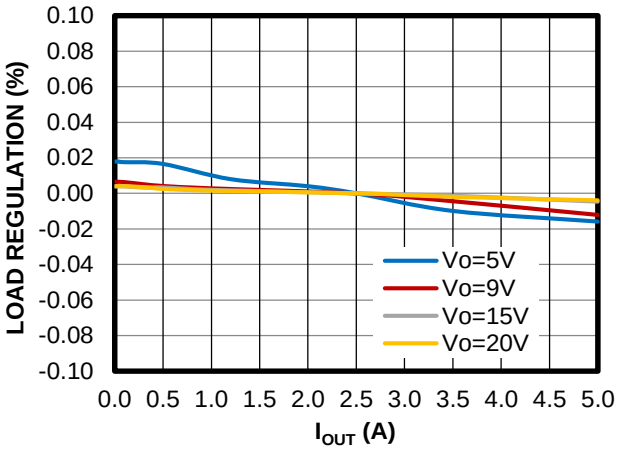
### Efficiency

$V_{IN}$ = 12V



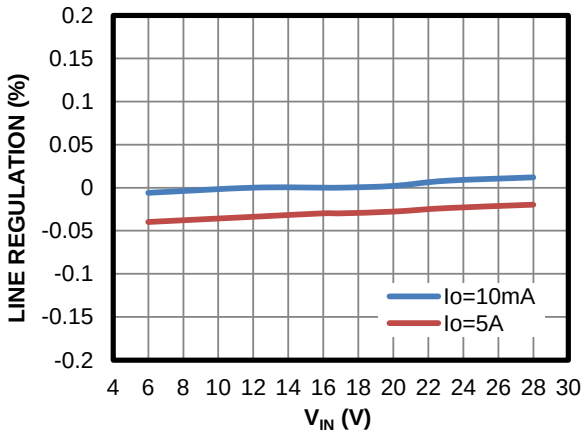

### Load Regulation

$V_{IN}$ = 12V



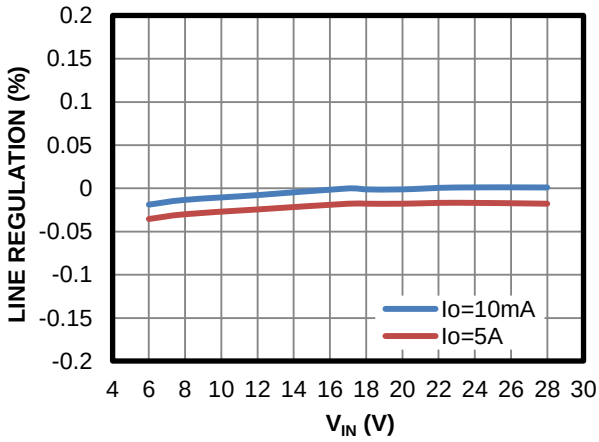

### Line Regulation

$V_{OUT}$ = 5V



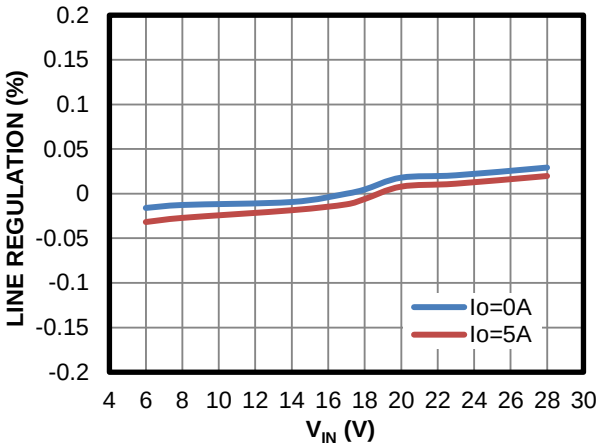

### Line Regulation

$V_{OUT}$ = 9V



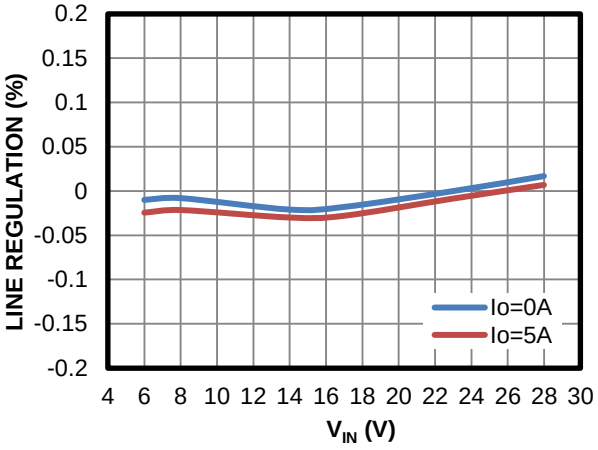

### Line Regulation

$V_{OUT}$ = 15V




### Line Regulation

$V_{OUT}$ = 20V

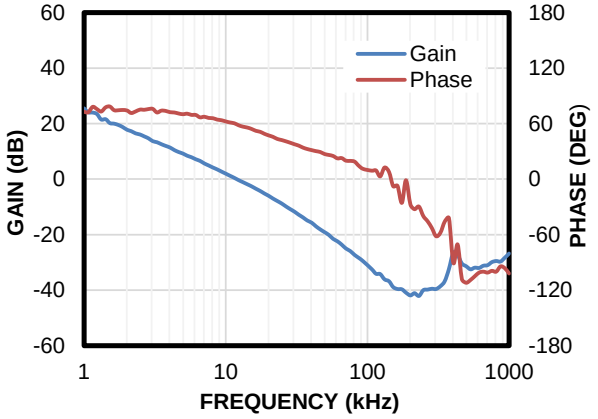


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

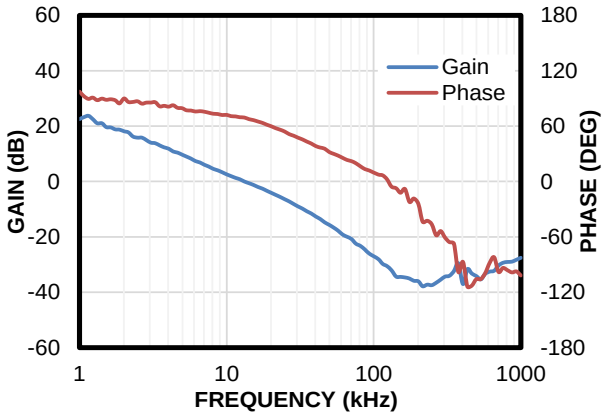
### Bode Plot

$V_{OUT}$ = 5V, $I_{OUT}$ = 3A, BW = 12.37kHz, PM = 58.149 degrees



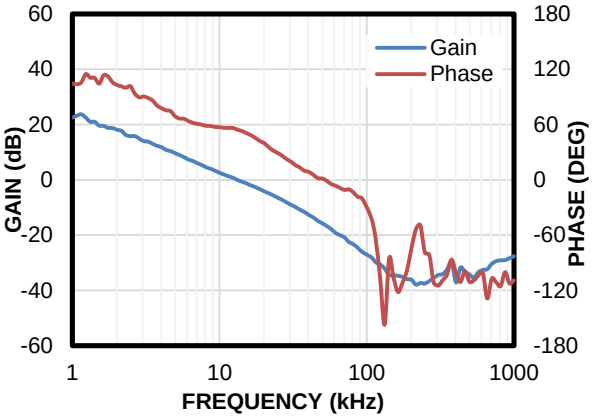

### Bode Plot

$V_{OUT}$ = 9V, $I_{OUT}$ = 3A, BW = 13.81kHz, PM = 68.188 degrees



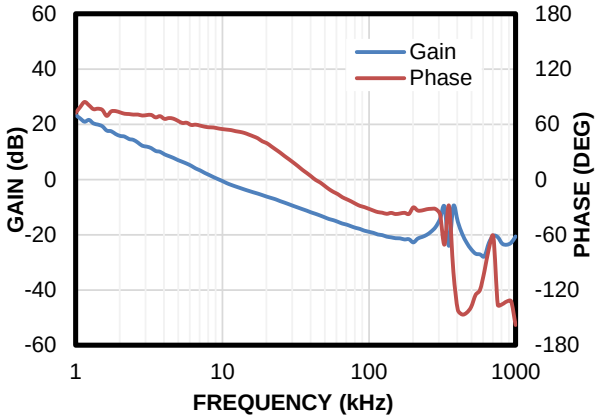

### Bode Plot

$V_{OUT}$ = 15V, $I_{OUT}$ = 3A, BW = 9.16kHz, PM = 57.613 degrees



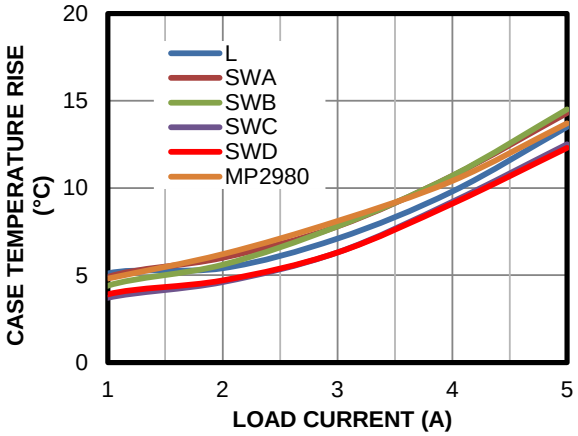

### Bode Plot

$V_{OUT}$ = 20V, $I_{OUT}$ = 5A, BW = 10kHz, PM = 54.907 degrees



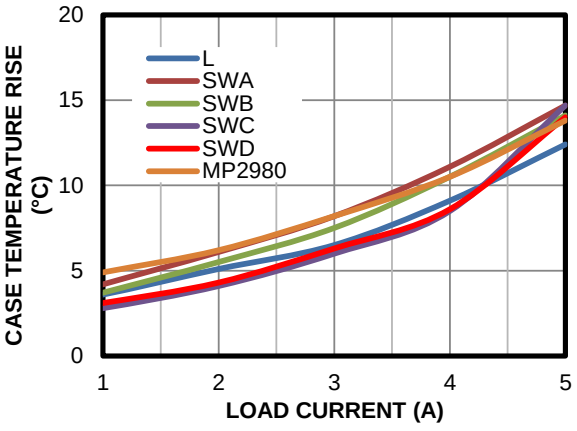

### Case Temperature Rise

$V_{IN}$ =12V, $V_{OUT}$ = 5V, FSW = 10, based on the EV2980-R-00A




### Case Temperature Rise

$V_{IN}$ = 12V, $V_{OUT}$ = 9V, FSW = 10, based on the EV2980-R-00A

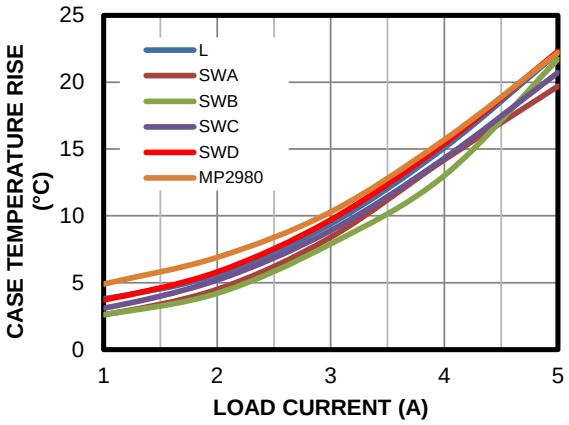


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

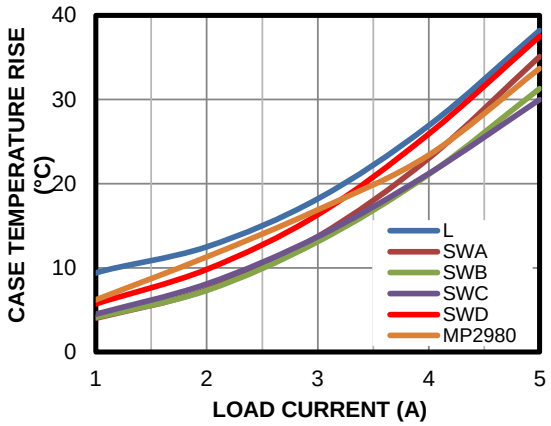
### Case Temperature Rise

$V_{IN}$ = 12V, $V_{OUT}$ = 15V, FSW = 10, based on the EV2980-R-00A




### Case Temperature Rise

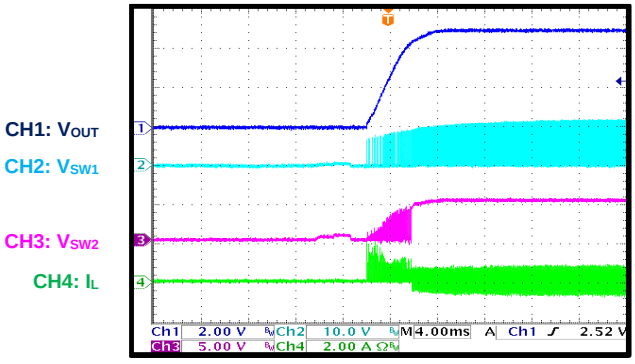
$V_{IN}$ = 12V, $V_{OUT}$ = 20V, FSW = 10, based on the EV2980-R-00A



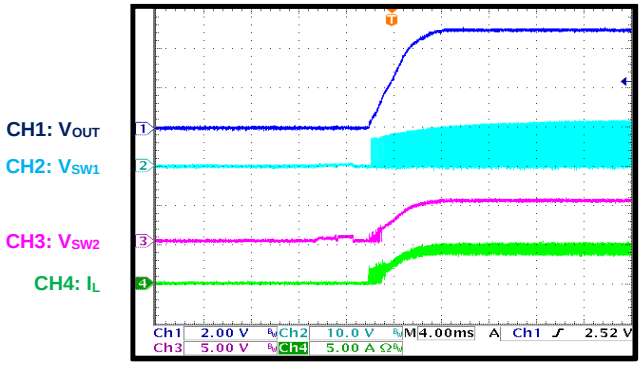
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

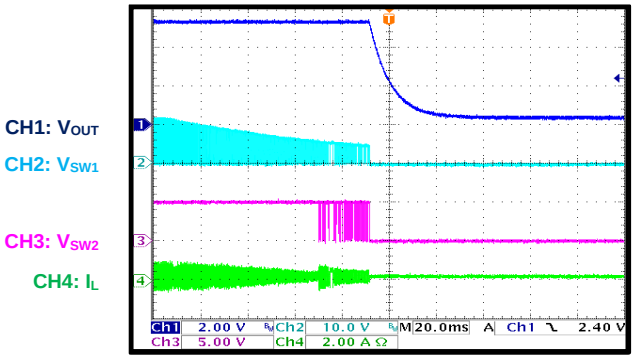
### $V_{IN}$ Start-Up
Load = 0A



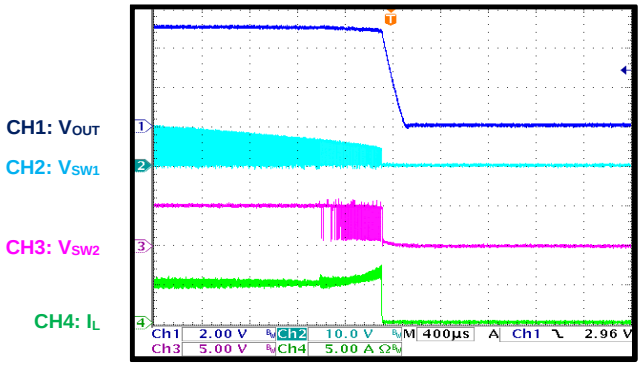

### $V_{IN}$ Start-Up
Load = 5A



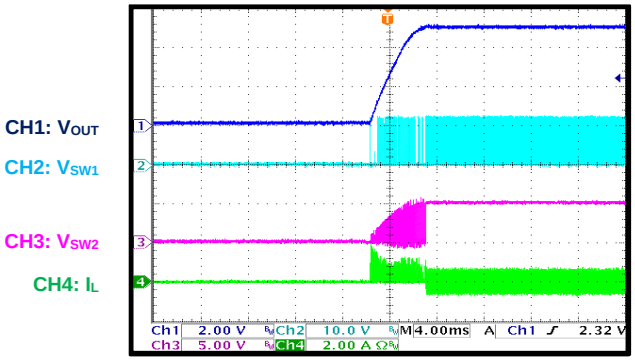

### $V_{IN}$ Shutdown
Load = 0A



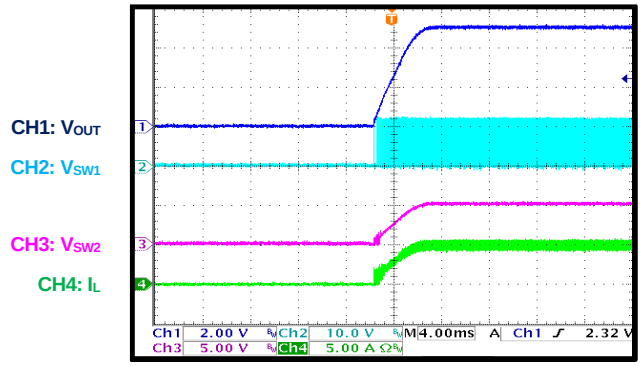

### $V_{IN}$ Shutdown
Load = 5A




### ENPWR Bit Enable via the Digital Interface
Load = 0A




### ENPWR Bit Enable via the Digital Interface
Load = 5A

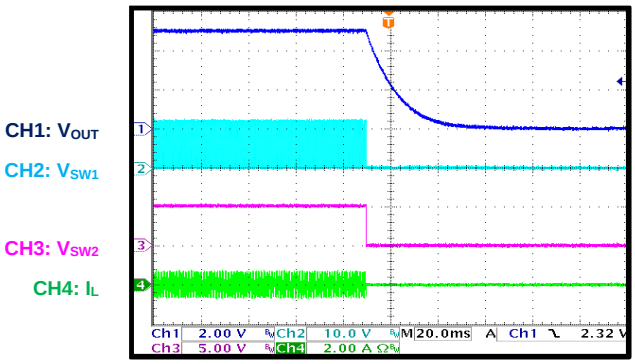


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

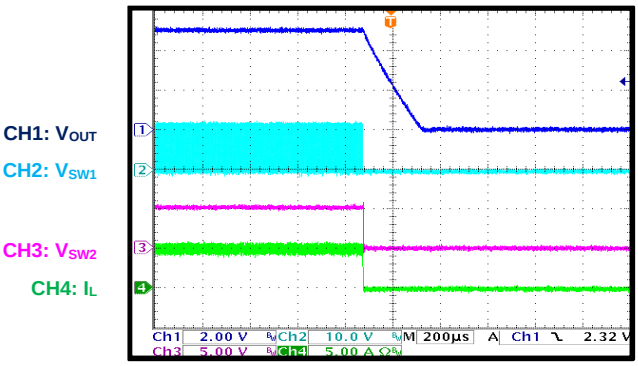
### ENPWR Bit Disable via the Digital Interface

Load = 0A



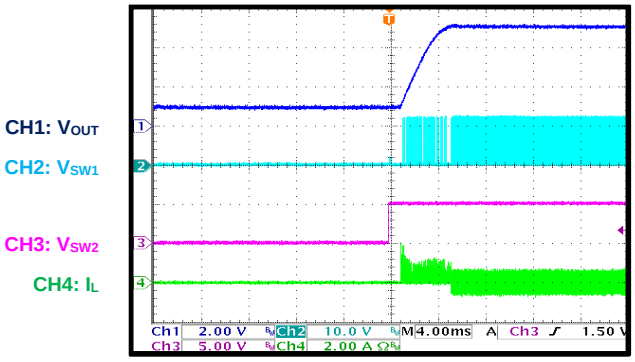

### ENPWR Bit Disable via the Digital Interface

Load = 5A



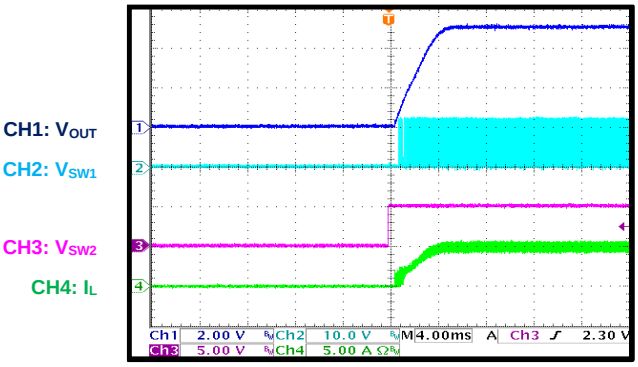

### Start-Up through EN

Load = 0A



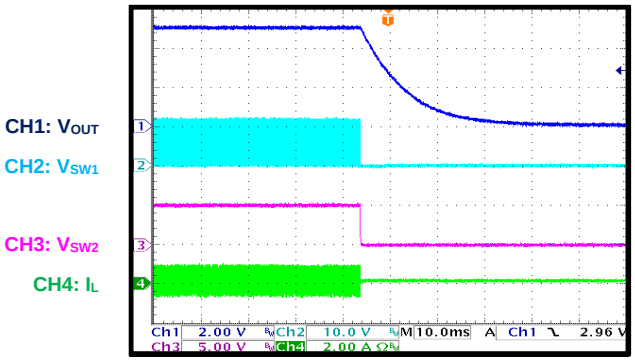

### Start-Up through EN

Load = 5A



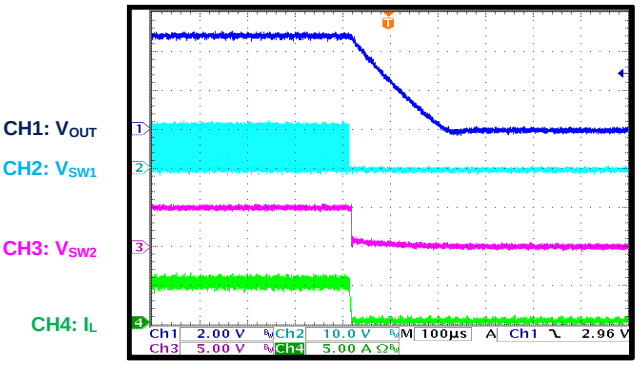

### Shutdown through EN

Load = 0A




### Shutdown through EN

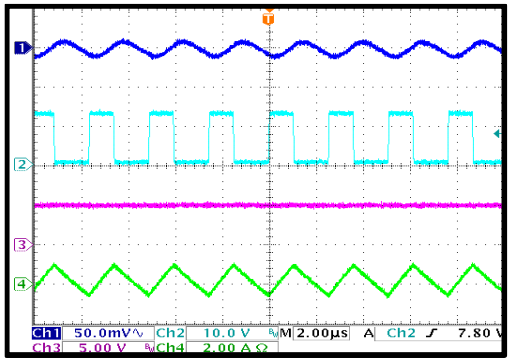
Load = 5A



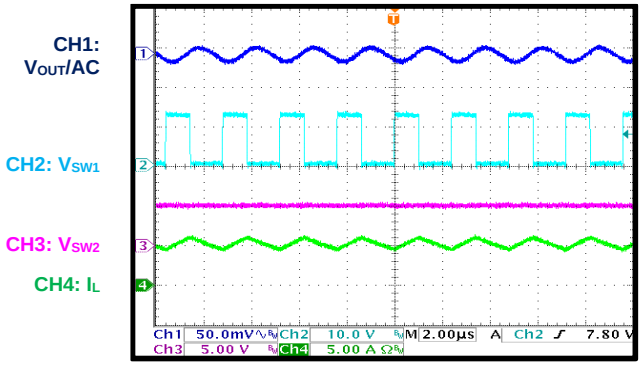
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

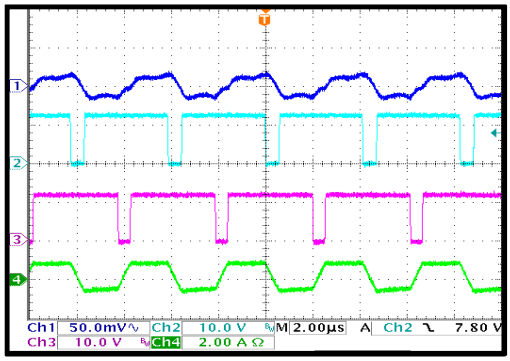
### Steady State
$V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_{OUT}$ = 0A



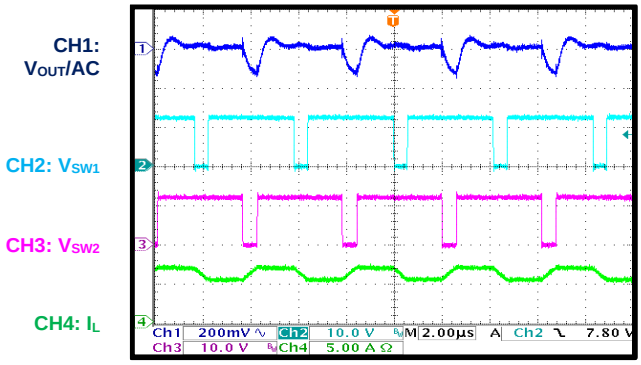

### Steady State
$V_{IN}$ = 12V, $V_{OUT}$ = 5V, $I_{OUT}$ = 5A



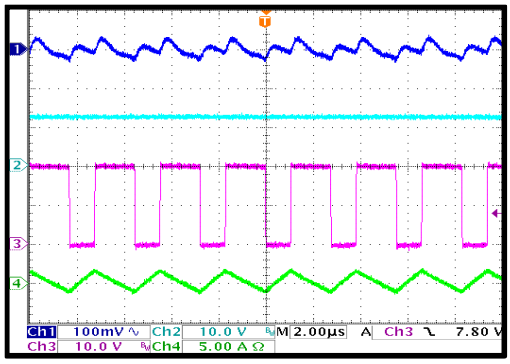

### Steady State
$V_{IN}$ = 12V, $V_{OUT}$ = 12V, $I_{OUT}$ = 0A



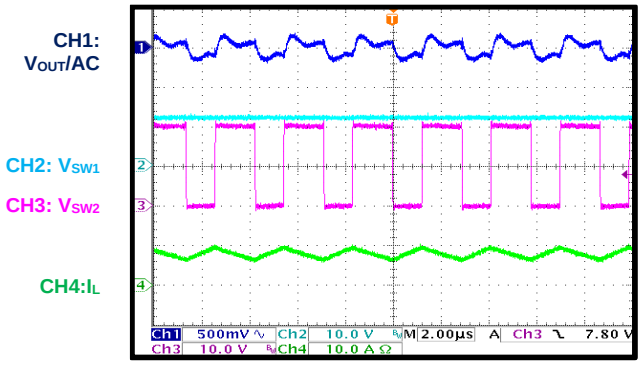

### Steady State
$V_{IN}$ = 12V, $V_{OUT}$ = 12V, $I_{OUT}$ = 5A




### Steady State
$V_{IN}$ = 12V, $V_{OUT}$ = 20V, $I_{OUT}$ = 0A




### Steady State
$V_{IN}$ = 12V, $V_{OUT}$ = 20V, $I_{OUT}$ = 5A

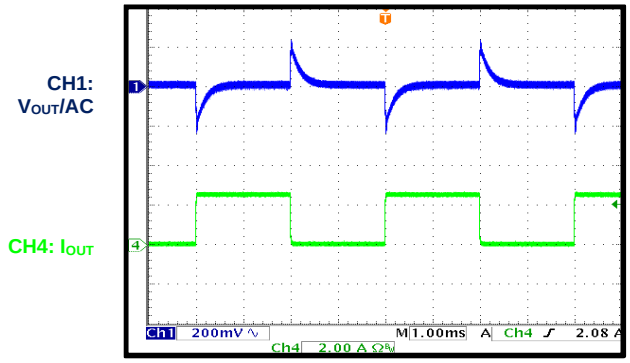


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

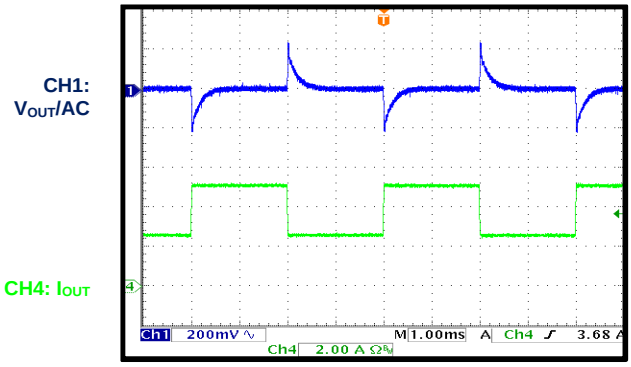
### Load Transient

$V_{IN}$ = 12V, $V_{OUT}$ = 5V, load = 0A to 2.5A, 150mA/µs



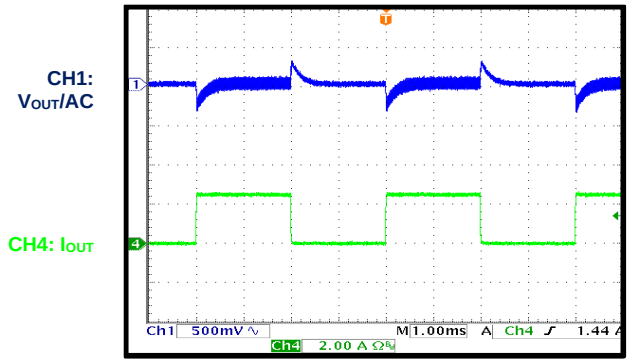

### Load Transient

$V_{IN}$ = 12V, $V_{OUT}$ = 5V, load = 2.5A to 5A, 150mA/µs



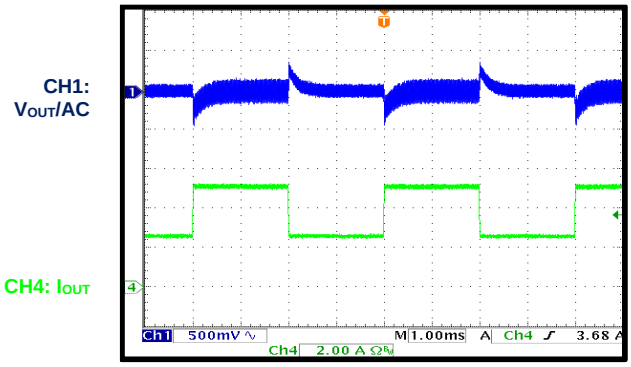

### Load Transient

$V_{IN}$ = 12V, $V_{OUT}$ = 20V, load = 0A to 2.5A, 150mA/µs



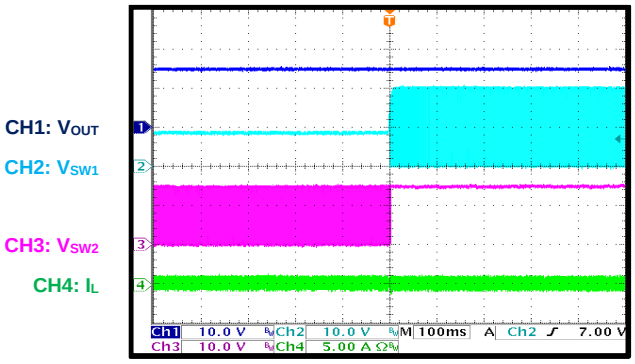

### Load Transient

$V_{IN}$ = 12V, $V_{OUT}$ = 20V, load = 2.5A to 5A, 150mA/µs



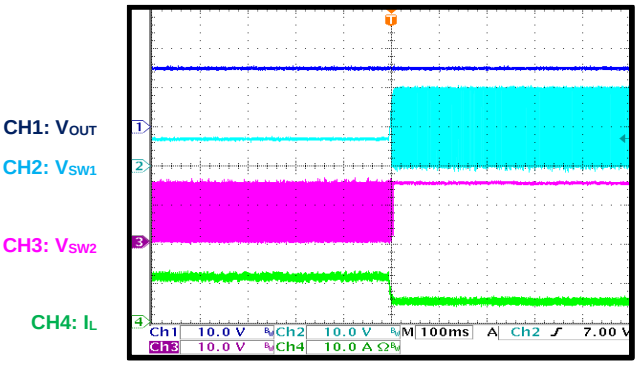

### Input Voltage Transient

$V_{IN}$ = 9V to 20V, $V_{OUT}$ = 15V, load = 0A




### Input Voltage Transient

$V_{IN}$ = 9V to 20V, $V_{OUT}$ = 15V, load = 5A

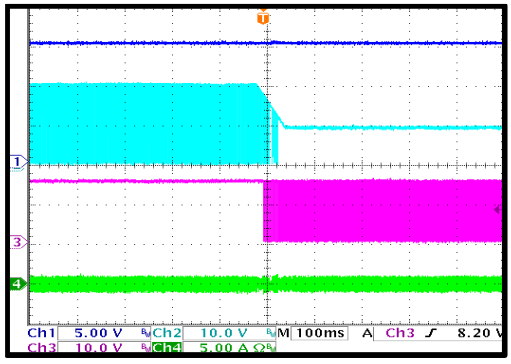


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

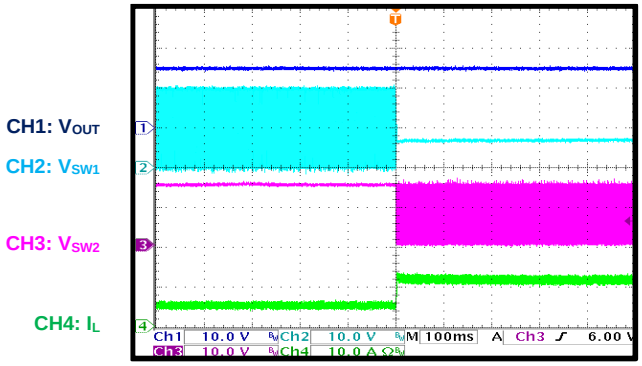
### Input Voltage Transient

$V_{IN}$ = 20V to 9V, $V_{OUT}$ = 15V, load = 0A



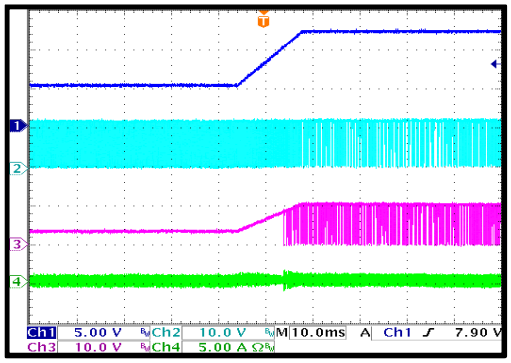

### Input Voltage Transient

$V_{IN}$ = 20V to 9V, $V_{OUT}$ = 15V, load = 5A



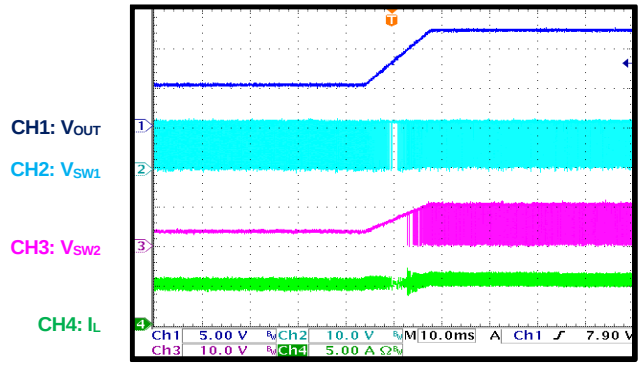

### Output Voltage Transient

$V_{OUT}$ = 5V to 12V, $I_{OUT}$ = 0A



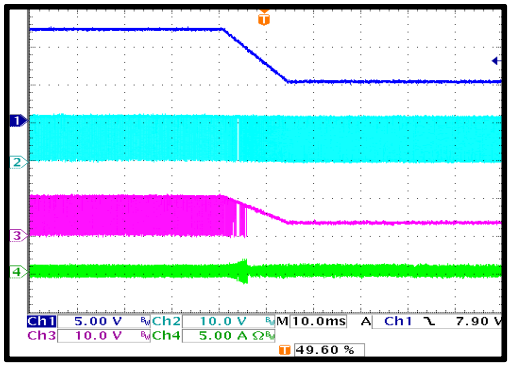

### Output Voltage Transient

$V_{OUT}$ = 5V to 12V, $I_{OUT}$ = 5A



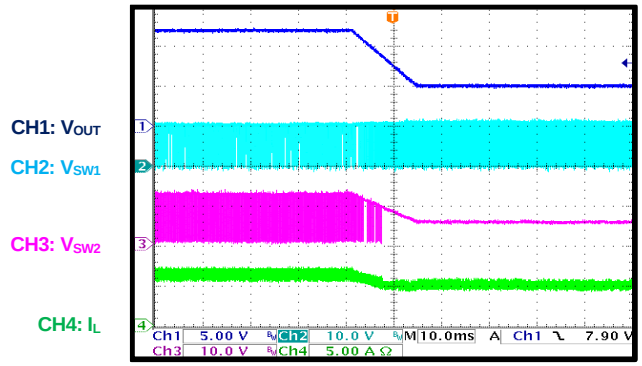

### Output Voltage Transient

$V_{OUT}$ = 12V to 5V, load = 0A




### Output Voltage Transient

$V_{OUT}$ = 12V to 5V, $I_{OUT}$ = 5A

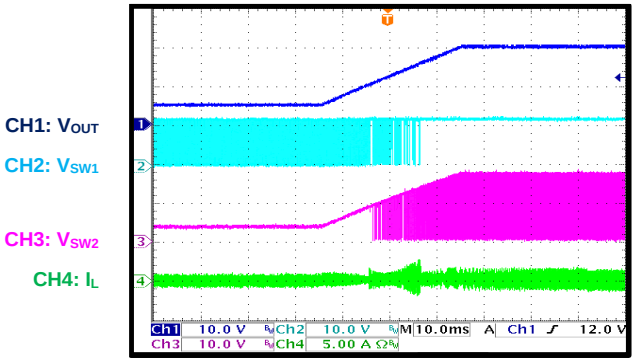


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

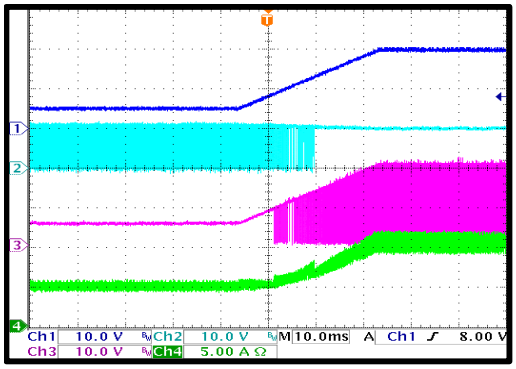
### Output Voltage Transient

$V_{OUT}$ = 5V to 20V, load = 0A



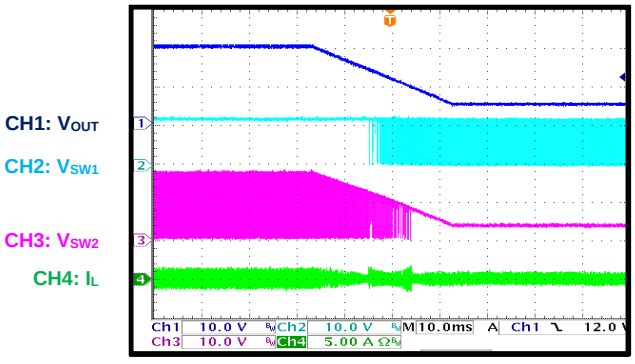

### Output Voltage Transient

$V_{OUT}$ = 5V to 20V, load = 5A



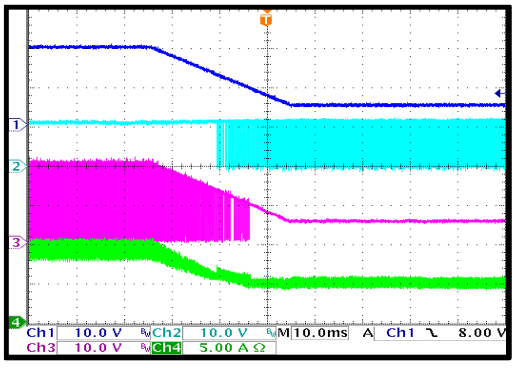

### Output Voltage Transient

$V_{OUT}$ = 20V to 5V, load = 0A

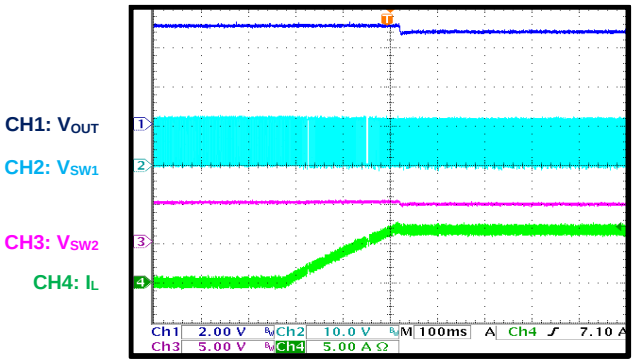



### Output Voltage Transient

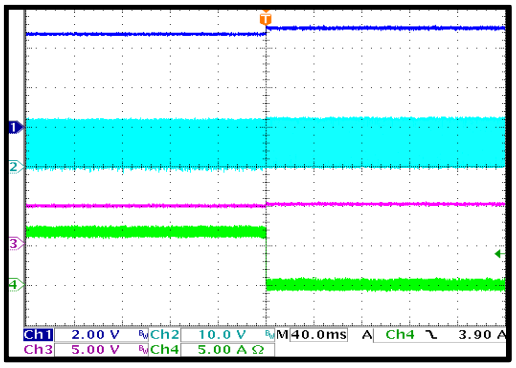
$V_{OUT}$ = 20V to 5V, load = 5A




### OCP Entry



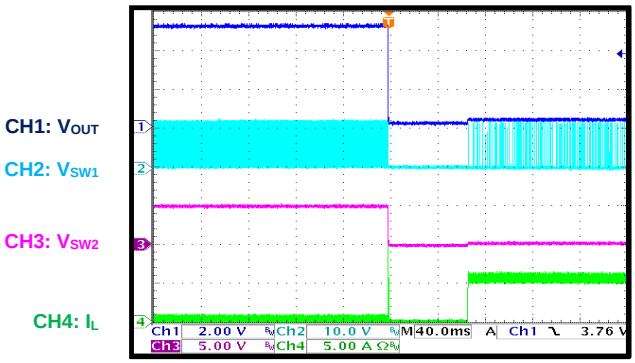

### OCP Recovery



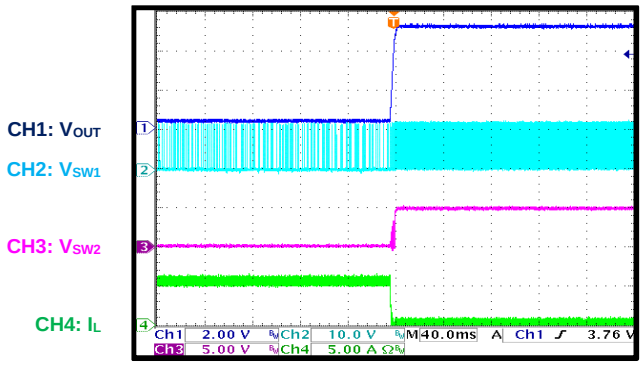
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{OUT}$ = 5V, L = 4.7µH, $T_A$ = 25°C, unless otherwise noted.**

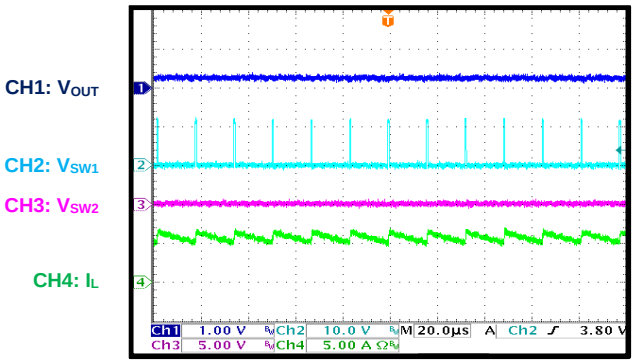
### SCP Entry




### SCP Recovery




### SCP Steady State



## FUNCTIONAL BLOCK DIAGRAM

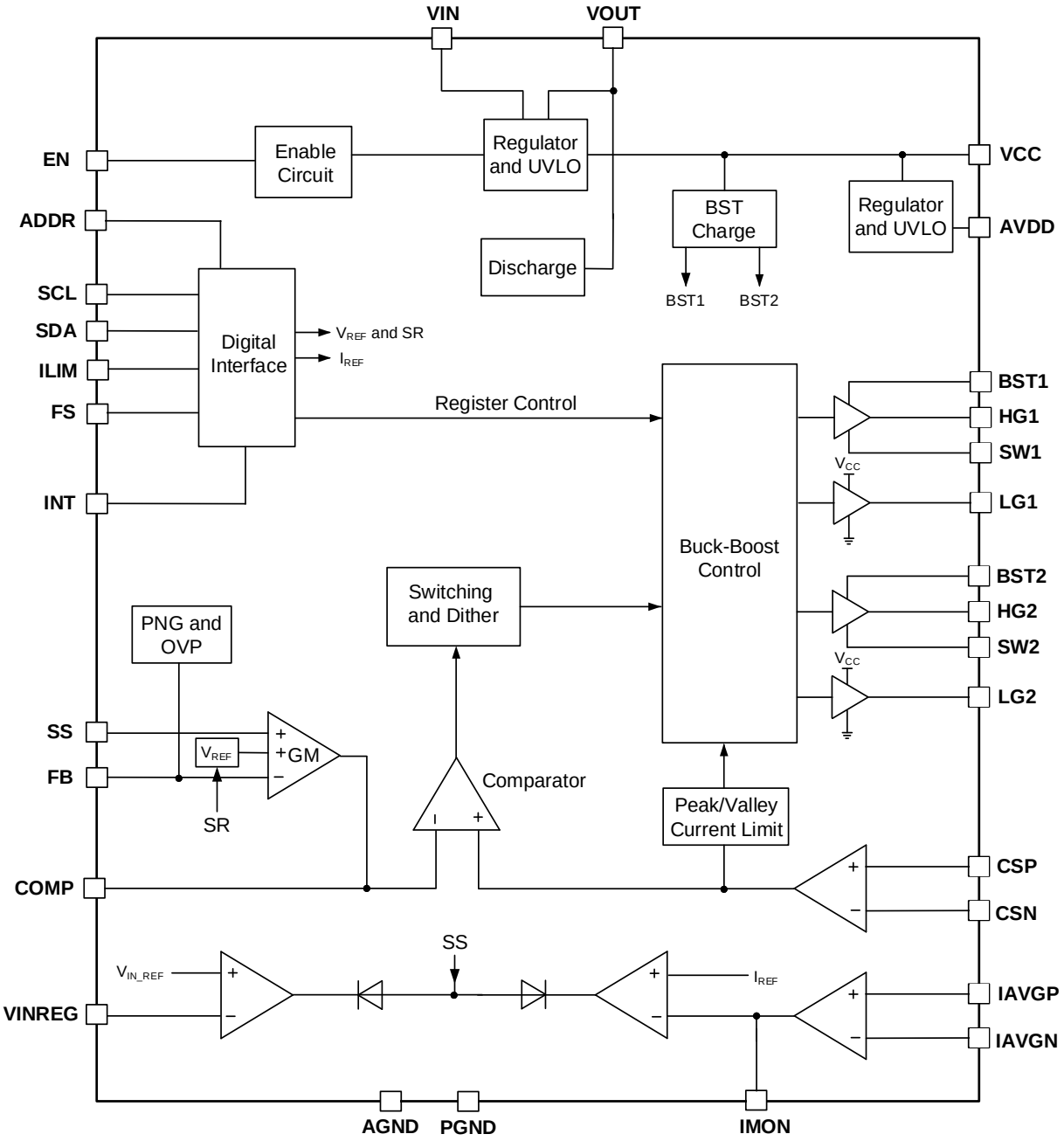



**Figure 2: Functional Block Diagram**

# OPERATION

The MP2980 is a four-switch buck-boost controller. It works with fixed frequency in buck, boost, and buck-boost modes. One special buck-boost control strategy provides high efficiency across the full input voltage ($V_{IN}$) range and smooth transients between different modes. Figure 2 on page 23 shows the functional block diagram, and the sections below describe the MP2980's functions.

## Buck-Boost Operation

The MP2980 can regulate the output voltage ($V_{OUT}$) above, equal to, or below $V_{IN}$. Figure 3 shows the single inductor, four-switch power structure using a buck-boost topology.

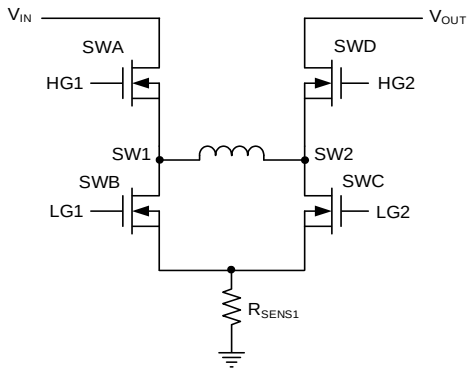



**Figure 3: Buck-Boost Topology**

Using the buck-boost topology, the MP2980 can operate in buck mode, boost mode, or buck-boost mode with different $V_{IN}$ inputs (see Figure 4).

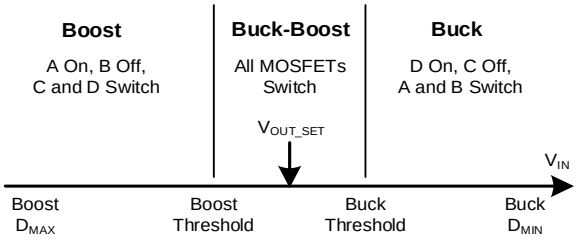



**Figure 4: Buck-Boost Operating Range**

## Buck Mode ($V_{IN} > V_{OUT}$)

If $V_{IN}$ exceeds $V_{OUT}$ significantly, the MP2980 works in buck mode. SWA and SWB switch during buck regulation, SWC is off, and SWD remains on to conduct the inductor current ($I_L$).

In each cycle of buck mode, SWA turns on when the FB voltage ($V_{FB}$) drops below the reference voltage ($V_{REF}$). After SWA turns off, SWB turns on to conduct $I_L$ until it triggers the COMP control signal. By repeating this operation, the controller regulates $V_{OUT}$.

## Boost Mode ($V_{IN} < V_{OUT}$)

If $V_{IN}$ drops below $V_{OUT}$ significantly, the MP2980 works in boost mode. In this mode, SWC and SWD switch for boost regulation, SWB is off, and SWA remains on to conduct $I_L$.

In each cycle of boost mode, SWC turns on to conduct $I_L$. If $I_L$ rises and triggers the control signal on COMP, then SWC turns off and SWD turns on for the freewheeling current. Then SWC turns on and off repeatedly to regulate $V_{OUT}$ in boost mode.

## Buck-Boost Mode ($V_{IN} \approx V_{OUT}$)

If $V_{IN}$ is close to $V_{OUT}$, the controller cannot provide sufficient energy to the load in buck mode due to SWA's minimum off time, or the controller supplies too much power to the load in boost mode due to SWC's minimum on time. Under these conditions, the MP2980 adopts buck-boost control to regulate the output.

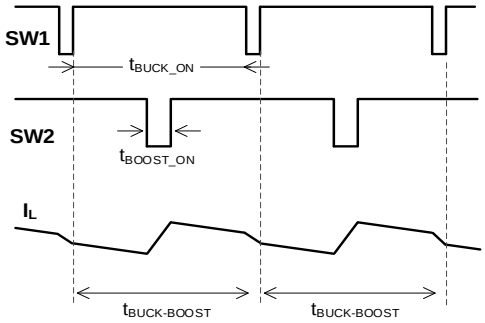



**Figure 5: Buck-Boost Waveform**

If $V_{IN}$ is close to $V_{OUT}$, the MP2980 enters buck-boost mode, and a boost switching period is inserted into each buck switching period. The MOSFETs start up in the following sequence:

1. SWA and SWD
2. SWA and SWC
3. SWA and SWD
4. SWB and SWD

Then $I_L$ can meet the required COMP voltage ($V_{COMP}$) and supply sufficient current to the output.

### Power Supply

The MP2980's internal circuit is powered by AVDD at 5.2V, and the gate drivers are powered by VCC at 7.2V. VCC is regulated from $V_{IN}$ and $V_{OUT}$, while AVDD is powered by $V_{CC}$.

When $V_{IN}$ is supplied and EN is pulled high, the MP2980 tries to regulate VCC at 7.2V. At the same time, AVDD is regulated at 5.2V. If the AVDD voltage ($V_{AVDD}$) exceeds the under-voltage lockout (UVLO) threshold and the ENPWR bit is high, the device starts switching and regulates $V_{OUT}$ with soft-start control. If $V_{IN}$ and $V_{OUT}$ both exceed 8.8V, the device powers VCC using the lower voltage source between $V_{IN}$ and $V_{OUT}$ to reduce power loss. Otherwise, the device powers VCC using the higher voltage power source between $V_{IN}$ and $V_{OUT}$ to generate sufficient $V_{CC}$. VCC and BST have separate UVLO thresholds that keep the gate signal off. Both VCC and BST must have sufficient voltage to enable switching, except for the $V_{AVDD}$ UVLO threshold.

The MP2980 operates between a 6V and 36V $V_{IN}$ range. When VCC is powered from $V_{OUT}$ after start-up, the device can operate until $V_{IN}$ drops below 5V.

When the MP2980 shuts down via $V_{AVDD}$ UVLO or the EN signal, the digital interface cannot respond to the host, and COMP is immediately pulled low. The VCC, AVDD, and BST voltages drop slowly with leakage, but all logic is off.

### Start-Up

After start-up, the MP2980 starts switching using soft-start control. The soft-start circuit charges current to the SS pin and ramps up the soft-start voltage ($V_{SS}$) from 0V. $V_{SS}$ is then fed to the error amplifier (EA) to control $V_{OUT}$. After the soft-start signal rises to the configured $V_{REF}$ (set via the VREF bits), soft start completes and closed-loop regulation starts. $V_{SS}$ rises and clamps at 0.6V above $V_{REF}$ in steady state, unless a protection is triggered.

The MP2980 typically starts up in buck mode since $V_{OUT}$ is below $V_{IN}$ significantly. If there is some bias voltage on VOUT, the device does not switch until the soft-start signal exceeds $V_{FB}$, which is proportional to the VOUT bias voltage.

During soft start, the IC works in automatic pulse-frequency modulation (PFM) mode. Neither over-voltage protection (OVP) nor over-current protection (OCP) in hiccup mode work during the soft-start period.

### Enable (EN) and Configurable Under-Voltage Lockout (UVLO)

The EN pin enables and disables the MP2980. When applying a voltage exceeding the EN high threshold (>1.1V), the device starts up some of the internal circuits in micro-power mode. If the EN voltage ($V_{EN}$) exceeds the turn-on threshold (1.35V), then the MP2980 enables all functions and starts switching. Switching is disabled once $V_{EN}$ drops below its lower threshold (<1.28V).

If $V_{EN}$ is below 0.4V, the MP2980 shuts down completely. After shutdown, the device sinks a small amount of current from the input power (typically <1μA). EN is compatible with voltages up to 40V. For automatic start-up, connect EN directly to VIN. During EN shutdown, the digital interface resets to its default value after a 200ms discharge time.

The MP2980 features a configurable UVLO hysteresis. During start-up, EN sources a 4.7μA current out of EN once $V_{EN}$ exceeds 1.35V (see Figure 6).

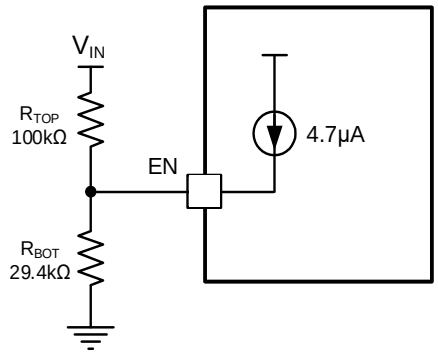



**Figure 6: $V_{IN}$ UVLO Configuration**

$V_{IN}$ must decrease to exceed the current source and stops switching after the IC starts up. The $V_{IN}$ start switching threshold ($V_{IN\_ON}$) can be calculated with Equation (1):

$$V_{IN\_ON}\ (V) = V_{EN\_ON}(V) \times (1 + \frac{R_{TOP}}{R_{BOT}}) = 5.95V \quad (1)$$

Where $V_{EN\_ON}$ is typically about 1.35V.

The $V_{IN}$ stop switching threshold ($V_{IN\_OFF}$) can be calculated with Equation (2):

$$V_{IN\_OFF}(V) = V_{EN\_OFF}(V) \times (1+\frac{R_{TOP}}{R_{BOT}}) - 4.7\mu A \times R_{TOP}(k\Omega)/1000 = 5.16V \quad (2)$$

Where $V_{EN\_OFF}$ is about 1.28V.

### Forced Continuous Conduction Mode (FCCM)

The MP2980 works in forced continuous conduction mode (FCCM). The buck on time and boost off time are determined by the internal circuit to obtain a fixed frequency based on the $V_{IN}$ / $V_{OUT}$ ratio. When the load decreases, the average input current drops, and $I_L$ may go negative from $V_{OUT}$ to $V_{IN}$ during the SWD on period. This forces $I_L$ to work in continuous mode with fixed frequency, generating a low $V_{OUT}$ ripple.

### Switching Current Limit

The MP2980 senses the low-side MOSFET (LS-FET) current via the CSP and CSN pins. It provides the valley current limit in buck mode and peak current limit in boost mode for each cycle-by-cycle switch. In buck mode, the next period does not start before $I_L$ drops to the valley current limit. As a result, the MP2980 may foldback the frequency when the valley current limit is triggered. The switching current limit can be configured via an external sense resistor. The SWB and SWC current signal is blanked internally for about 180ns to enhance noise rejection.

If the cycle-by-cycle current limit is triggered, then the interrupt OCP bit is set to 1; if the OCP bit is not masked off, then INT is pulled low.

Under an over-current (OC) condition, the MP2980 reaches the cycle-by-cycle current limit. The device may also trigger hiccup protection or latch-off protection, depending on the OCP_MODE bit setting. In hiccup mode, the IC turns off once $V_{FB}$ drops below 60% of $V_{REF}$. Once the soft-start period finishes, the device reaches the switching current limit. It attempts recovery after a fixed off time that is configured by the SS capacitor ($C_{SS}$) discharge period. In latch-off mode, the IC turns off if $V_{FB}$ falls below 60% of $V_{REF}$. Once latch-off protection is triggered, the chip does not recover until a new power cycle is initiated by toggling EN or the ENPWR bit. If the hiccup mode and latch-off protections are disabled, the IC continues switching with a cycle-by-cycle current limit. The hiccup mode and latch-off protections are masked during the soft-start period.

Based on the cycle-by-cycle switching current limit, the maximum input current ($I_{IN\_MAX}$) in buck mode can be calculated with Equation (3):

$$I_{IN\_MAX}(A) = \frac{V_{OUT}}{V_{IN}} \times \eta \times (\frac{I_{LIMIT\_BUCK}(mV)}{R_{SENSE}(m\Omega)} + \frac{V_{IN} - V_{OUT}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT}}{V_{IN}} \times 10^3) \quad (3)$$

Where $I_{LIMIT\_BUCK}$ is typically 133mV and $R_{SENSE}$ is the cycle-by-cycle switching current limit sense resistor.

$I_{IN\_MAX}$ in boost mode can be calculated with Equation (4):

$$I_{IN\_MAX}(A) = \frac{I_{LIMIT\_BOOST}(mV)}{R_{SENSE}(m\Omega)} - \frac{V_{IN}}{2 \times L(\mu H) \times f_{SW}(kHz)} \times \frac{V_{OUT} - V_{IN}}{V_{OUT}} \times 10^3) \quad (4)$$

Where η is the efficiency, and $I_{LIMIT\_BOOST}$ is typically 150mV.

### Average Current Limit

The IAVGP and IAVGN pins sense the MP2980's output current ($I_{OUT}$). A sense resistor can be connected to the VOUT line for average $I_{OUT}$ limit control. Once the sensed signal exceeds the current limit $V_{REF}$, an internal EA pulls down $V_{SS}$. Eventually, $V_{SS}$ replaces $V_{REF}$ to control COMP, and $I_L$ is limited by COMP to transfer less energy to the output. Soft start regulates the output low until the average load current drops.

If the switching current is regulated by the average current limit and does not trigger the cycle-by-cycle current limit, the MP2980 does not trigger hiccup mode or latch-off protection, even if the average current limit is reached. This provides constant current charge. If only the average current limit is triggered, the interrupt OCP bit is not set to 1, and INT is not pulled low.

It is recommended to add a 100Ω/220nF current sense filter (see Figure 14 on page 42).

### Overload and Short-Circuit Protection (SCP)

If an overload fault occurs, the MP2980 limits $I_{OUT}$ using average current limit loop regulation. If the average current limit loop is disabled, the cycle-by-cycle switching current limit works. Under cycle-by-cycle current limit conditions, if the IC works in boost mode, the SWC peak current is limited. If the IC works in buck mode, SWB remains on until $I_L$ drops to $I_{LIMIT\_BUCK}$, and then the next cycle can begin. Therefore, $I_L$ can be controlled in all work modes.

### Output Voltage Regulation

The MP2980 regulates $V_{OUT}$ via the feedback on the FB pin. $V_{FB}$ is compared to the internal reference, which is between 300mV and 2.047V depending on the VREF register bit setting. The EA output on COMP controls $I_L$ to supply $V_{OUT}$.

### Switching Frequency and Frequency Spread Spectrum (FSS)

The MP2980 configures the switching frequency ($f_{SW}$) via a 2-bit FSW register. $f_{SW}$ is selectable at 200kHz, 300kHz, 400kHz, or 600kHz. A 400kHz $f_{SW}$ is typically recommended.

The MP2980 provides frequency spread spectrum (FSS). If DITHER = 1 (0x02, D[4]), FSS is enabled. If DITHER = 0, FSS is disabled. FSS minimizes peak emissions at certain frequencies (see Figure 7).

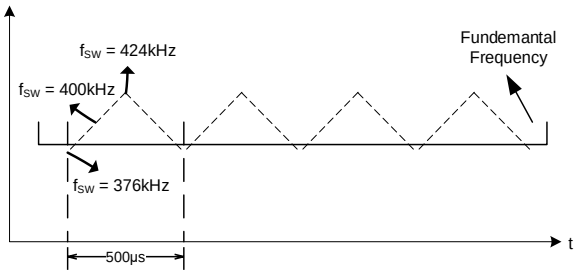



**Figure 7: Frequency Spread Spectrum**

The MP2980 uses a 2kHz triangle wave to modulate the internal oscillator. The FSS span is ±6%.

FSS can be enabled at a $f_{SW}$ of 200kHz, 300kHz, 400kHz, or 600kHz.

### Gate Driver and Bootstrap (BST) Power

The MP2980 provides four N-channel MOSFET gate drivers for the H-bridge MOSFETs (see Figure 3 on page 24). Each driver is capable of sourcing and sinking current. During buck operation, LG1 and HG1 switch while HG2 remains on. During boost operation, LG2 and HG2 switch while HG1 remains on. LG1 and LG2 are powered by the VCC power, and HG1 and HG2 are powered by the BST1 and BST2 power.

Connect capacitors between BST1 and SW1 and between BST2 and SW2 to supply power, which can be provided via an internal diode from VCC or from charging each other.

### Over-Voltage Protection (OVP)

The MP2980 monitors the FB pin. If $V_{FB}$ exceeds 127% of $V_{REF}$ and OVP_MODE = 01, then the IC discharges the $V_{OUT}$ capacitor via an internal discharge resistor. It stops discharging when $V_{FB}$ drops to 111% of the regulation voltage. If OVP_MODE = 00, there is no logic to stop switching, even if $V_{FB}$ exceeds the OVP threshold. If OVP_MODE = 10, the IC latches off when $V_{OUT}$ rises to 127% of $V_{REF}$.

### Interrupt (INT Pin)

The INT pin indicates interrupt for the following fault events: OCP (also the switching peak cycle-by-cycle current limit), FB OVP, over-temperature protection (OTP), and $V_{OUT}$ power not good (PNG) reporting.

When any of these faults is triggered, the corresponding register bit is set to 1. At the same time, INT pulls low to indicate an interrupt signal, depending on the related mask register setting.

INT is an open-drain output. When the MP2980 is disabled, INT is an open drain.

### Current Monitor Output

The MP2980 senses the average load current via a sense resistor and outputs a voltage signal on the IMON pin. The signal is amplified by the difference between the IAVGP pin voltage ($V_{IAVGP}$) and IAVGN pin voltage ($V_{IAVGN}$). It is recommended to connect a small capacitor between IMON and AGND. The IMON output voltage ($V_{IMON}$) can be calculated with Equation (5):

$$V_{IMON}\ (mV) = GAIN \times I_{OUT}\ (A) \times R_{SENS}\ (m\Omega) \quad (5)$$

The IMON gain is typically 18.8V/V. $R_{SENS}$ is the average load current sense resistor.

### Configurable Soft-Start Time (SS Pin)

The MP2980 provides a SS pin to configure the soft-start time ($t_{SS}$). The soft-start charge current ($I_{SS}$) is typically about 6μA. $t_{SS}$ can be estimated with Equation (6):

$$t_{SS}(ms) = C_{SS}(nF) \times V_{REF}(V) / I_{SS}(\mu A) \quad (6)$$

Where $I_{SS}$ is typically about 6μA, $C_{SS}$ is 47nF, and $V_{REF}$ is 0.5V. $t_{SS}$ is about 3.9ms.

### Slew-Rate Control and Output Discharge

The MP2980 sets the $V_{REF}$ change slew-rate via the internal SR bits. There are four $V_{REF}$ change (rising and falling) slew rates that can be selected based on the application specifications: 38mV/ms, 50mV/ms, 75mV/ms, or 150mV/ms.

During voltage transients, the discharge function works when GO-BIT = 1. The discharge function is automatically disabled after GO_BIT resets to 0, meaning the $V_{REF}$ change completes. If $V_{OUT}$ has not been discharged to the target voltage when the $V_{REF}$ change completes due to excess output capacitance, the OVP discharge function or the DISCHG bit can be used to continue discharging $C_{OUT}$.

The output discharge function can be enabled by any of the conditions below:

1. If GO_BIT = 1 and discharge works until a 20ms delay passes after GO_BIT resets to 0.
2. DISCHG = 1.
3. If OVP_MODE = 01 and $V_{FB}$ exceeds 127% of $V_{REF}$.
4. If the ENPWR bit shuts down and discharge works until a 200ms delay passes.
5. If the EN pin is off and discharge works until a 200ms delay passes.
6. If the $V_{IN}$ UVLO threshold is triggered but AVDD has residual voltage, the MP2980 discharges for 200ms. This discharge function may pause if $V_{AVDD}$ drops.

### Current Limit Control (ILIM Pin)

During start-up, the ILIM pin status is latched to the register and sets the default value of the ILIM bits. After start-up, changes in the pin status do not affect the register status unless the pin setting is adjusted and the IC is restarted.

### Frequency Control (FS Pin)

During start-up, the FS pin status is latched to the register and sets the default value of the FSW bits. After start-up, changes in the pin status do not affect the register status unless the pin setting is adjusted and the IC is restarted.

### VIN Regulation Loop (VINREG Pin)

The VINREG pin sets the minimum operating $V_{IN}$. If $V_{IN}$ drops to the configured level, the MP2980 pulls down SS and decreases $I_{OUT}$ to maintain $V_{IN}$. If $V_{IN}$ drops below the VINREG threshold, the MP2980 stops converting power to VOUT.

### Thermal Protection

The MP2980 integrates a temperature monitor circuit. If the junction temperature ($T_J$) exceeds 150°C, the MP2980 shuts down. Once the temperature drops below 125°C, the IC resumes normal operation. If OTP is triggered and INT is not masked, the pin is pulled low.

### Digital Interface

The MP2980 integrates a digital interface. The four device addresses are defined as 1100xxx, set via the ADDR resistor divider from AVDD. The R/W bits follow the 7-bit address, where 0 indicates a write command and 1 indicates a read command. The device works as a slave and supports standard mode (100kbps) and fast mode (400kbps) communication. The ADDR pin setting also impacts the default value of the ENPWR bit.

Table 1 shows the configurable device address.

**Table 1: Device Address Setting**

| Device Address | $R_{TOP}$ | $R_{BOT}$ | ENPWR Bit Default Value |
|---|---|---|---|
| 60h | NS | 0Ω | 1 |
| 62h | 100kΩ | 59kΩ | 1 |
| 64h | 68kΩ | 100kΩ | 0 |
| 66h | 0Ω | NS | 0 |

See the Register Description section on page 30 for more details on the digital interface and register control functions.

### Digital Interface Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse to ensure that it remains stable (low) during the clock pulse's high period.

Figure 8 shows the format for data transfers. After the start command (S), a slave address is sent. This address is 7 bits long, followed by an eighth data direction bit (R/W). A 0 indicates a transmission (write), and a 1 indicates a request for data (read). A data transfer is always terminated by a stop command (P), which is generated by the master. If the master wants to communicate on the bus, it can generate a repeated start command (Sr) and address another slave without first generating a stop command.

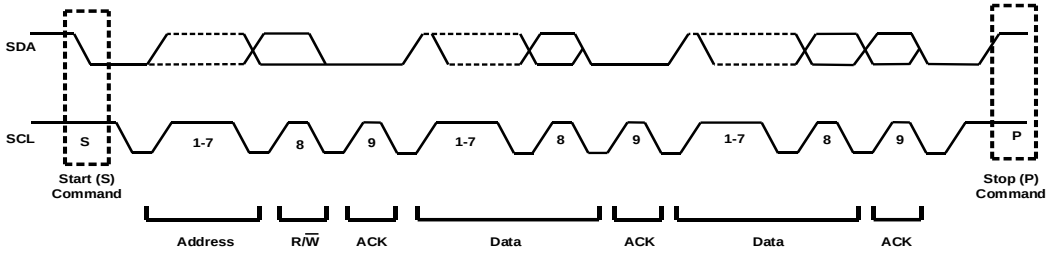
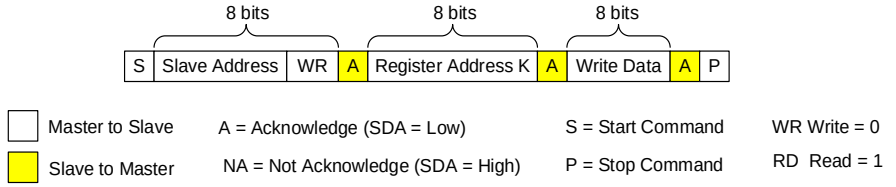



**Figure 8: Complete Data Transfer**

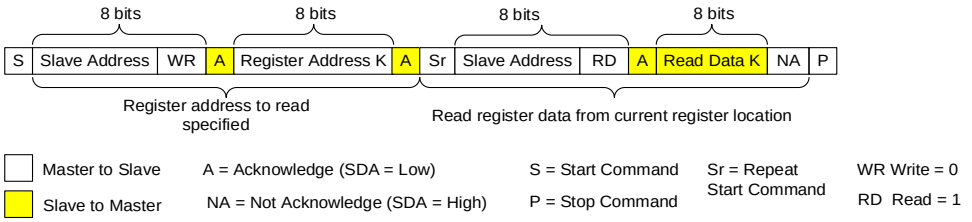
The MP2980 includes a complete digital interface slave controller. The digital interface slave fully complies with the digital interface specification requirements. It requires a start command, a valid digital interface address, a register address byte, and a data byte for a single data update.

After receiving each byte, the MP2980 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid digital interface address selects the MP2980. The MP2980 then performs an update on the falling edge of the LSB byte.

Figure 9 shows an example of the digital interface read and write command.




**Digital Interface Write Example**




**Digital Interface Read Example**

**Figure 9: Digital Interface Read and Write**

# REGISTER DESCRIPTION

## Register Map

| Addr | Register | Type | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **00h** | REF_LSB | R/W | - | - | - | - | - | VREF_L | | | 0000 0100 |
| **01h** | REF_MSB | R/W | VREF_H | | | | | | | | 0011 1110 |
| **02h** | CONTROL1 | R/W | SR | | DISCHG | DITHER | PNG_ LATCH | RESERVED (11) | GO_BIT | ENPWR | 0100 010x (12) |
| **03h** | CONTROL2 | R/W | FSW | | - | BB_ FSW | OCP_MODE | | OVP_MODE | | xx00 0101 (12) |
| **04h** | ILIM | R/W | - | - | - | - | - | ILIM | | | 0000 1xxx (12) |
| **05h** | INTERRUPT_ STATUS | R/W | - | - | - | OTP | - | OVP | OCP | PNG | 0000 0000 |
| **06h** | INTERRUPT_ MASK | R/W | - | - | - | M_OTP | - | M_OVP | M_OCP | M_PNG | 0000 0001 |

**Notes:**

11) Reserved bit. Do not write values to this bit in application.
12) "x" means that it is determined based on the external pin setting during start-up. See the register function descriptions on page 31 for more details.

### REF_LSB (00h)

**Format:** Direct

The REF_LSB command sets the feedback reference voltage ($V_{REF}$) low for 3 bits.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 2:0 | R/W | VREF_L | 3’b 100 | Sets the feedback $V_{REF}$ low for 3 bits. LSB = 1mV. |

### REF_MSB (01h)

**Format:** Direct

The REF_LSB command sets the feedback $V_{REF}$ high for 8 bits. The FB reference data format requires a total of 11 bits to set $V_{REF}$. If $V_{REF}$ is an 11-bit, unsigned binary integer of VREF[10:0], then $V_{FB}$ (V) = $V_{REF}$ / 1000.

| Name | VREF | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct, unsigned binary integer | | | | | | | | | | | | | | | |
| Register Name | N/A | | | | | VREF_H[7:0] | | | | | | | | VREF_L[2:0] | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | N/A | | | | | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | N/A | | | | | Data bit high | | | | | | | | Data bit low | | |
| Default Value (0.5V) | N/A | | | | | 500 integer | | | | | | | | | | |

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:0 | R/W | VREF_H | 8’b 00111110 | Feedback $V_{REF}$ high 8 bits. LSB = 8mV. |

### CONTROL1 (02h)

**Format:** Unsigned binary

The CONTROL1 command sets the $V_{REF}$ changing slew rate, output-to-ground discharge, frequency spread spectrum (FSS), PNG_LATCH, and the $V_{REF}$ change function enable bit.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:6 | R/W | SR | 2'b 01 | Configures the $V_{REF}$ changing slew rate.<br><br>2'b 00: 38mV/ms<br>2'b 01: 50mV/ms<br>2'b 10: 75mV/ms<br>2'b 11: 150mV/ms<br><br>This SR control only works after soft start finishes. During the soft-start period, the $V_{OUT}$ slew rate is controlled by soft start.<br><br>$V_{OUT}$ slew rate = $V_{REF}$ slew rate x feedback ratio<br><br>Where feedback ratio = (R1 + R2) / R2. |
| 5 | R/W | DISCHG | 1'b 0 | Sets the on/off control of the output-to-ground discharge path.<br><br>1'b 0: Turn off the discharge path, where the DISCHG bit function works even when the ENPWR bit is low<br>1'b 1: The MP2980 discharges $V_{OUT}$ via an internal resistor<br><br>This bit does not affect the output discharge behavior in the following cases:<br><br>1. $V_{OUT}$ changed via the digital interface<br>2. ENPWR bit shutdown<br>3. EN pin shutdown<br>4. Output over-voltage protection (OVP) when OVP_MODE enables discharge<br>5. Trigger $V_{IN}$ UVLO threshold<br>If GO_BIT = 1, the VOUT discharge path automatically turns on. After GO_BIT resets to 0 with a 20ms extra delay, the VOUT discharge path turns off.<br><br>It is typically recommended to set the slew rate low to allow $V_{OUT}$ to follow the $V_{REF}$ change using this internal discharge current. If $V_{OUT}$ cannot follow the $V_{REF}$ change even with the discharge due to a large output capacitor ($C_{OUT}$), then there is an additional 20ms of discharge. |
| 4 | R/W | DITHER | 1'b 0 | Enables FSS.<br><br>1'b 0: Disable dither<br>1'b 1: Enable dither |
| 3 | R/W | PNG_LATCH | 1'b 0 | Sets the power not good (PNG) status reset and control. See the PNG bit description on page 35.<br><br>1'b 0: The PNG bit status recovers to 0 once $V_{OUT}$ returns to its normal voltage range<br>1'b 1: The PNG bit status latches to 1 once $V_{OUT}$ exceeds the power good voltage range |
| 2 | R/W | RESERVED | 1'b 1 | Reserved. |

| | | | | |
|---|---|---|---|---|
| 1 | R/W | GO_BIT | 1’b 0 | Enables the $V_{REF}$ change function.<br><br>If GO_BIT = 1, enable the output change based on the VREF register. When the command completes (internal $V_{REF}$ steps to the target $V_{REF}$), GO_BIT automatically resets to 0. This prevents false operation of $V_{OUT}$ scaling.<br><br>Write the VREF registers (00h and 01h registers) first, then write GO_BIT = 1. $V_{REF}$ and $V_{OUT}$ change based on the new VREF. GO_BIT resets to 0 when $V_{REF}$ reaches a new level. The host reads GO_BIT to determine whether the $V_{REF}$ scaling is finished.<br><br>The $V_{OUT}$ discharge path is enabled when GO_BIT = 1, regardless of the DISCHG bit setting. This helps pull $V_{OUT}$ from high to low under light-load conditions. After GO_BIT resets to 0, the discharge continues and turn off after a 20ms delay.<br><br>1’b 0: $V_{OUT}$ cannot be changed<br>1’b 1: $V_{OUT}$ changes based on the VREF registers. After $V_{REF}$ reaches the new level set via the VREF bits, GO_BIT resets to 0 automatically |
| 0 | R/W | ENPWR | 1’b x | Enables power switching.<br><br>1’b 0: Enable power switching<br>1’b 0: Disable power switching but other internal control circuits work<br><br>The default value is determined via the ADDR pin setting. See Table 1 on page 28 for more details.<br><br>If ENPWR resets from 1 to 0, the MP2980 resets the VREF bits to 0.5V (0011 1110 100). The MP2980 resets VREF one-time only to ensure that VREF can be changed to the required value via the digital interface after ENPWR = 0. The host must re-write VREF again if the system requires the previous VOUT value after ENPWR = 0.<br><br>After ENPWER is set to 0, the discharge function works for 200ms. |

### CONTROL2 (03h)

**Format:** Unsigned binary

The CONTROL2 command sets the switching frequency ($f_{SW}$), buck-boost $f_{SW}$, over-current protection (OCP), and over-voltage protection (OVP).

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:6 | R/W | FSW | 2'b x0 | Sets $f_{SW}$. The default value is determined via the FS pin setting during start-up. See the Electrical Characteristics section on page 8 for the FS pin setting levels.<br><br>Writable during both ENPWR = 0 and ENPWR = 1 conditions. $f_{SW}$ changes smoothly after the digital interface writes these bits.<br><br>2'b 00: 200kHz<br>2'b 01: 300kHz<br>2'b 10: 400kHz<br>2'b 11: 600kHz |
| 4 | R/W | BB_FSW | 1'b 0 | Sets the buck-boost $f_{SW}$.<br><br>1'b 0: Set the buck-boost $f_{SW}$ equal to 40% of the base $f_{SW}$<br>1'b 1: Set the buck-boost $f_{SW}$ equal to 80% of the base $f_{SW}$ |
| 3:2 | R/W | OCP_MODE | 2'b 01 | Sets OCP after triggering the cycle-by-cycle switching current limit (valley current limit in buck mode, or peak current limit in boost mode).<br><br>2'b 00: No hiccup mode or latch-off protection. $I_L$ is limited by the cycle-by-cycle current limit<br>2'b 01: Hiccup protection after triggering the switching current limit and FB < 60% of $V_{REF}$. The off period is controlled by the SS discharge<br>2'b 10: Latch-off protection. The IC must start up again<br>2'b 11: Reserved |
| 1:0 | R/W | OVP_MODE | 2'b 01 | Sets OVP protection mode after triggering the threshold at 127% of $V_{REF}$.<br><br>2'b 00: No protection after OVP, where $V_{OUT}$ is regulated by COMP. No discharge after OVP<br>2'b 01: Discharge $V_{OUT}$ via an internal resistor and stop switching once $V_{FB}$ exceeds 127% of $V_{REF}$. Recover once $V_{FB}$ drops to 111% of $V_{REF}$<br>2'b 10: Latch-off protection. No discharge after OVP<br>2'b 11: Reserved |

### ILIM (04h)

**Format:** Unsigned binary

The ILIM command sets the average current limit.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 2:0 | R/W | ILIM | 3'b xxx | Sets the average current limit. Can be used to configure the output current ($I_{OUT}$) limit. The default value is determined via the ILIM pin setting during start-up. Float the ILIM pin to set the ILIM bits = 001. See the Electrical Characteristics section on page 8 for the ILIM pin setting levels.<br>3'b 000: 27.9mV current limit threshold<br>3'b 001: 33.3mV current limit threshold<br>3'b 010: 39.3mV current limit threshold<br>3'b 011: 45.1mV current limit threshold<br>3'b 100: 51.2mV current limit threshold<br>3'b 101: 56.8mV current limit threshold<br>3'b 110: 62.8mV current limit threshold<br>3'b 111: 68.7mV current limit threshold |

### INTERRUPT_STATUS (05h)

**Format:** Unsigned binary

The INTERRUPT_STATUS command shows the over-temperature protection (OTP), OVP, OCP, and power not good (PNG) events.

| Bits | Access | Bit Name | Default | Description | Reset Condition |
|---|---|---|---|---|---|
| 4 | R/W | OTP | 1'b 0 | Enables the OTP indication.<br>1'b 0: Normal state<br>1'b 1: Chip enters OTP state | This bit is latched once triggered.<br>Write 0xFF to this register to reset the interrupt status and INT state. |
| 2 | R/W | OVP | 1'b 0 | Enables the $V_{OUT}$ OVP indication.<br>1'b 0: Normal state<br>1'b 0: Chip enters OTP state | |
| 1 | R/W | OCP | 1'b 0 | Enables the cycle-by-cycle switching current limit indication.<br>1'b 0: Normal state<br>1'b 0: Cycle-by-cycle current limit is triggered, $V_{FB}$ < 60% of $V_{REF}$, and soft start completes | |
| 0 | R/W | PNG | 1'b 0 | Enables the $V_{OUT}$ PNG indicator.<br>1'b 0: Normal state<br>1'b 0: Output power is not good. This indicates when $V_{OUT}$ is not within its upper and lower thresholds<br>The PNG_LATCH bit controls the PNG reset behavior. | Related to the PNG_LATCH setting:<br>PNG_LATCH = 0: This bit indicates the instantaneous value. INT indicates the instantaneous state<br>PNG_LATCH = 1: This bit is latched once triggered. Write 0xFF to reset the interrupt status and INT state |

### INTERRUPT_MASK (06h)

**Format:** Unsigned binary

The INTERRUPT_MASK command sets the M_OTP, M_OVP, M_OCP, and M_PNG masks.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 4 | R/W | M_OTP | 1'b 0 | 1'b 0: Does not mask off the OTP alert<br>1'b 1: Mask off the OTP alert<br>M_OTP = 1 only masks the INT output. This is similar for other mask bits. |
| 2 | R/W | M_OVP | 1'b 0 | 1'b 0: Does not mask off the OVP alert<br>1'b 1: Mask off the OVP alert<br>M_OVP = 1 only masks the INT output. |
| 1 | R/W | M_OCP | 1'b 0 | 1'b 0: Does not mask off the OCP alert<br>1'b 1: Mask off the OCP alert<br>M_OCP = 1 only masks the INT output. |
| 0 | R/W | M_PNG | 1'b 1 | 1'b 0: Does not mask off the PNG alert<br>1'b 1: Mask off the PNG alert<br>M_PNG = 1 only masks the INT output. |

# APPLICATION INFORMATION

## Output Voltage Setting

The default $V_{OUT}$ is set via a resistor divider connected to FB. The default $V_{REF}$ is 0.5V. The bottom resistor in the resistor divider is typically between 1kΩ and 50kΩ.

The top resistor in the feedback resistor divider (R1) can be estimated using Equation (7):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (7)$$

It is possible to use the digital interface to select the FB $V_{REF}$ and obtain another $V_{OUT}$.

## Selecting the Inductor

The inductor selection is based on the operation mode. The inductance in buck mode ($L_{BUCK}$) can be calculated with Equation (8):

$$L_{BUCK} = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

Where $\Delta I_L$ is the peak-to-peak inductor ripple current, which is about 30% to 50% of the maximum load current.

In boost mode, the inductor selection is based on limiting $\Delta I_L$ to about 30% to 50% of the maximum input current ($I_{IN\_MAX}$). The target inductance for boost mode ($L_{BOOST}$) can be calculated with Equation (9):

$$L_{BOOST} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (9)$$

$I_{IN\_MAX}$ can be calculated with Equation (10):

$$I_{IN\_MAX} = \frac{V_{OUT} \times I_{LOAD\_MAX}}{V_{IN} \times \eta} \quad (10)$$

Where $I_{LOAD\_MAX}$ is the maximum load current, and η is the efficiency.

Choosing a larger inductance reduces the ripple current but also increases the inductor size and reduces the converter's achievable bandwidth by moving the right half-plane zero to lower frequencies. It is recommended to select the appropriate balance based on the application specifications.

## Selecting the Input Capacitor

In buck mode, the MP2980 has a discontinuous input current. In boost mode, the MP2980 has a continuous input current. A capacitor is required to supply the AC current during buck mode while maintaining the DC $V_{IN}$. For the best performance, place ceramic capacitors as close to VIN as possible. Capacitors with X5R or X7R ceramic dielectrics are recommended due to their stable temperature characteristics. The capacitors must also have a ripple current rating exceeding the converter's maximum input ripple current. The input ripple current in buck mode ($I_{CIN\_RMS}$) can be estimated with Equation (11):

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (11)$$

The worst-case condition in buck mode occurs at $V_{IN}$ = 2 x $V_{OUT}$, which can be calculated with Equation (12):

$$I_{CIN\_RMS} = \frac{I_{OUT}}{2} \quad (12)$$

For simplification, choose an input capacitor ($C_{IN}$) with an RMS current rating greater than half of the maximum load current.

$C_{IN}$ determines the converter's input voltage ripple ($\Delta V_{IN}$). If there is a $\Delta V_{IN}$ requirement in the system, choose $C_{IN}$ to meets the specifications.

In buck mode, $\Delta V_{IN}$ can be estimated with Equation (13):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

The worst-case condition occurs at $V_{IN}$ = 2 x $V_{OUT}$, which can be calculated with Equation (14):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (14)$$

## Selecting the Output Capacitor

In boost mode, $I_{OUT}$ is discontinuous and the output capacitor ($C_{OUT}$) must be capable of reducing the output voltage ripple ($\Delta V_{OUT}$).

A higher capacitance may be required to decrease $\Delta V_{OUT}$ and the transient response. Low-ESR capacitors such as X5R or X7R ceramic capacitors are recommended. If using ceramic capacitors, the capacitance dominates the impedance at $f_{SW}$. This means $\Delta V_{OUT}$ is independent of the ESR. $\Delta V_{OUT}$ can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} \quad (15)$$

If using hybrid, polymer, or low-ESR electrolytic capacitors, the ESR dominates the impedance at $f_{SW}$. $\Delta V_{OUT}$ can be estimated using Equation (16):

$$\Delta V_{OUT} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}} \quad (16)$$

Where $R_{ESR}$ is the equivalent series resistance of $C_{OUT}$.

For a 100W USB PD application, a 100µF polymer capacitor and four 22µF ceramic capacitors are recommended.

Choose $C_{OUT}$ to meet the $\Delta V_{OUT}$ and load transient requirements of the design. Consider capacitance derating when designing high $V_{OUT}$ applications.

### Selecting the External MOSFET

The MP2980 requires four external N-channel power MOSFETs. Figure 10 shows two for the top switches (switches A and D) and two for the bottom switches (switches B and C). In buck mode, SWA and SWB switch while SWD remains on. In boost mode, SWC and SWD switch while SWA remains on.

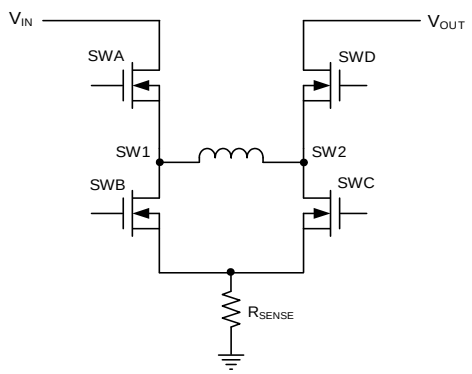



**Figure 10: Buck-Boost Topology**

There are five critical parameters for selecting a MOSFET, which are described below:

1. Maximum drain-to-source voltage ($V_{DS\_MAX}$): SWA and SWB must withstand the maximum $V_{IN}$ and the transient spikes at SW1 during switching. Therefore, it is recommended to select $V_{DS\_MAX}$ for SWA and SWB at 1.5 x $V_{IN}$.

   SWC and SWD have $V_{OUT}$ and transient spikes at SW2 during switching. Therefore, it is recommended to select SWC and SWD at ≥1.5 x $V_{OUT}$.

2. Maximum continuous drain current ($I_{D\_MAX}$): SWA, SWB, SWC, and SWD must be able to withstand the maximum $I_L$ and peak $I_L$ during switching.

3. MOSFET threshold voltage ($V_{TH}$): The MP2980's driver voltages are supplied by VCC. The gate plateau voltages of the MOSFETs should be below the converter's minimum $V_{CC}$, otherwise the MOSFETs may not fully improve during start-up or overload conditions.

4. Total gate charge ($Q_G$): All switches ($Q_G$) should be less than 50nC (at a 7.2V gate condition). If there are two MOSFETs in parallel, each MOSFET's $Q_G$ must be smaller than 25nC.

5. Drain-source on resistance ($R_{DS(ON)}$): A lower $R_{DS(ON)}$ is optimal for managing the case temperature rise of the MOSFETs as well as obtaining higher efficiency. See the calculations for the conduction and switching loss for MOSFET SWA, SWB, SWC, and SWD $R_{DS(ON)}$ selection below.

### MOSFET SWA

When the MP2980 works in boost mode, SWA remains on. The conduction power loss of SWA ($P_{C\_LOSS\_SWA}$) can be calculated with Equation (17):

$$P_{C\_LOSS\_SWA} = (I_{OUT}\times\frac{V_{OUT}}{V_{IN}})^2\times R_{DS(ON)\_SWA} \quad (17)$$

Assume that the MOSFET junction-to-ambient thermal resistance is 50°C/W (determined by the board power dissipation), and that the maximum acceptable temperature rise is 50°C.

The maximum power loss is 1W. $P_{C\_LOSS\_SWA}$ is estimated relative to the 1W power loss with Equation (18):

$$P_{C\_LOSS\_SWA} < 1W \quad (18)$$

Based on Equation (18), the MOSFET $R_{DS(ON)}$ can be selected.

When the MP2980 works in buck mode, $P_{C\_LOSS\_SWA}$ can be calculated with Equation (19):

$$P_{C\_LOSS\_SWA} = \frac{V_{OUT}}{V_{IN}} \times I_{OUT}^2 \times R_{DS(ON)\_SWA} \quad (19)$$

The switching loss of SWA ($P_{SW\_LOSS\_SWA}$) can be calculated with Equation (20):

$$P_{SW\_LOSS\_SWA} = \frac{1}{2} \times V_{IN} \times I_{OUT} \times (t_{ON} + t_{OFF}) \times f_{SW} \quad (20)$$

The switch on time ($t_{ON}$) and the switch off time ($t_{OFF}$) are based on the MOSFET datasheet information (see Figure 11).

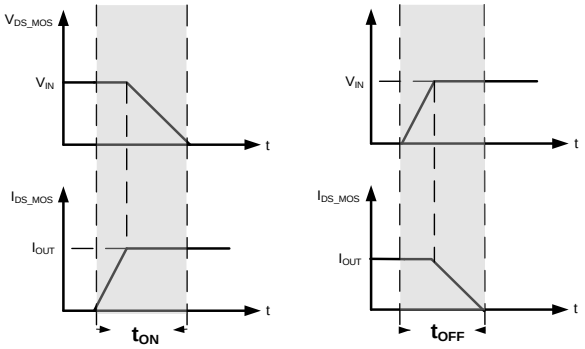



**Figure 11: Switch On Time and Switch Off Time**

### MOSFET SWB

When the MP2980 works in buck mode, its conduction loss ($P_{C\_LOSS\_SWB}$) can be calculated with Equation (21):

$$P_{C\_LOSS\_SWB} = (1 - \frac{V_{OUT}}{V_{IN}}) \times I_{OUT}^2 \times R_{DS(ON)\_SWB} \quad (21)$$

### MOSFET SWC

When the MP2980 works in boost mode, SWB remains off. Its conduction loss in boost mode ($P_{C\_LOSS\_SWC}$) can be calculated with Equation (22):

$$P_{C\_LOSS\_SWC} = (1 - \frac{V_{IN}}{V_{OUT}}) \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DS(ON)\_SWC} \quad (22)$$

When the MP2980 works in boost mode, the SWC switching loss ($P_{SW\_LOSS\_SWC}$) can be calculated with Equation (23):

$$P_{SW\_LOSS\_SWC} = \frac{1}{2} \times V_{OUT} \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}}) \times (t_{ON} + t_{OFF}) \times f_{SW} \quad (23)$$

### MOSFET SWD

When the MP2980 works in buck mode, SWD remains on. Its conduction loss ($P_{C\_LOSS\_SWD}$) can be calculated with Equation (24):

$$P_{C\_LOSS\_SWD} = I_{OUT}^2 \times R_{DS(ON)\_SWD} \quad (24)$$

When the MP2980 works in boost mode, $P_{C\_LOSS\_SWD}$ can be calculated with Equation (25):

$$P_{C\_LOSS\_SWD} = (\frac{V_{IN}}{V_{OUT}}) \times (I_{OUT} \times \frac{V_{OUT}}{V_{IN}})^2 \times R_{DS(ON)\_SWD} \quad (25)$$

The dead time and the LS-FET switching loss can be ignored.

### Compensation Components

The COMP pin controls system stability and transient response. COMP is the output of the internal EA. A series capacitor-resistor combination sets a pole-zero combination to control the control system's characteristics.

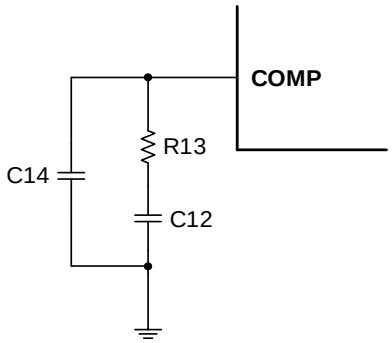



**Figure 12: COMP External Compensation**

The COMP external compensation sets one pole and one zero (see Figure 12). The pole's frequency ($f_{P1}$) can be calculated with Equation (26):

$$f_{P1} = \frac{1}{2\pi \times C14 \times R13} \quad (26)$$

The zero's pole ($f_{Z1}$) can be calculated with Equation (27)

$$f_{Z1} = \frac{1}{2\pi \times C12 \times R13} \quad (27)$$

When the MP2980 works in buck mode, the DC gain of the voltage feedback loop ($A_{VDC}$) can be calculated with Equation (28):

$$A_{VDC} = R_{LOAD} \times \frac{G_{CS}}{R_{SENSE}} \times A_{V\_EA} \times \frac{V_{FB}}{V_{OUT}} \quad (28)$$

Where $A_{V\_EA}$ is the EA voltage gain (300V/V), $G_{CS}$ is the COMP to current-sense gain, $R_{SENSE}$ is the current-sense resistor, and $R_{LOAD}$ is the load resistor.

The system has two important poles. One pole is from the compensation capacitor (C12) and the EA's output resistor. Its frequency ($f_{P2}$) can be calculated with Equation (29):

$$f_{P2} = \frac{G_{EA}}{2\pi \times C12 \times A_{V\_EA}} \quad (29)$$

Where $G_{EA}$ is the EA transconductance (1220μA/V).

The second pole is from $C_{OUT}$ and the load resistor. Its frequency ($f_{P3}$) can be calculated with Equation (30):

$$f_{P3} = \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} \quad (30)$$

The system may have another significant zero if there is a large output capacitance or high ESR. This zero's frequency ($f_{ESR}$) can be located with Equation (31):

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}} \quad (31)$$

When the MP2980 works in boost mode, $A_{VDC}$ can be calculated with Equation (32):

$$A_{VDC} = \frac{V_{IN} \times A_{V\_EA} \times R_{LOAD} \times V_{FB} \times G_{CS} \times R13}{2 \times V_{OUT}^{\ 2} \times R_{SENSE}} \quad (32)$$

There is also a right-half-plane zero that exists in boost mode. Its frequency ($f_{RHPZ}$) can be calculated with Equation (33):

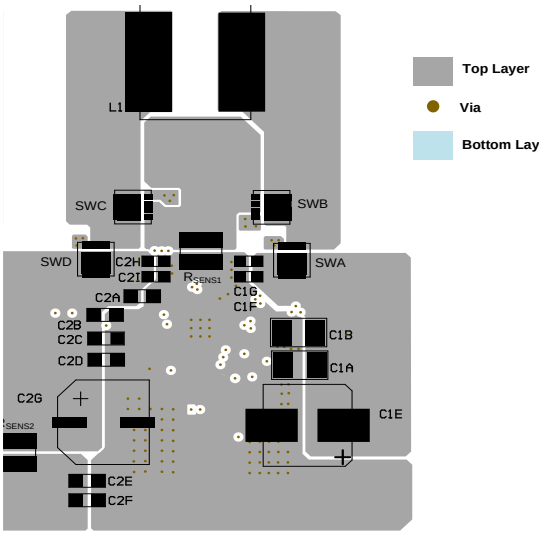
$$f_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \quad (33)$$

The right half-plane zero increases the gain and reduces the phase simultaneously, resulting in a smaller phase and gain margin. The worst-case condition occurs when $V_{IN}$ is at its minimum and the output power is at its maximum.

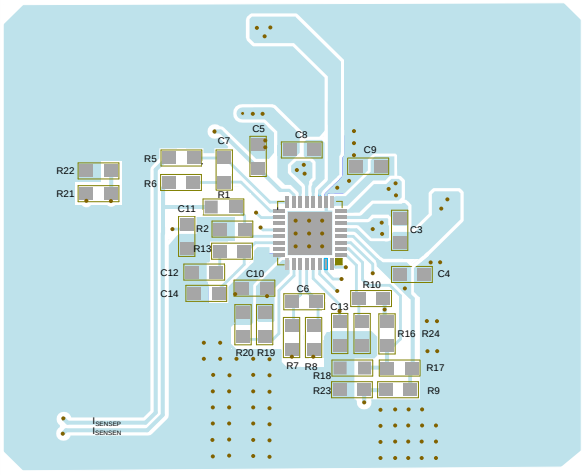
## PCB Layout Guidelines

Efficient layout is critical for stable operation. Improper layout may result in reduced performance, EMI issues, resistive loss, and even system instability. For the best results, refer to Figure 13 and follow the steps below:

1. In buck mode, place the input power loop — including the input filter capacitor ($C_{IN}$), the power MOSFETs (SWA and SWB), and the cycle-by-cycle current sense resistor ($R_{SENS1}$) — as close as possible.
2. In boost mode, place the output power loop — including the output filter capacitor ($C_{OUT}$), the power MOSFETs (SWC and SWD), and the cycle-by-cycle current sense resistor ($R_{SENS1}$) — as close as possible.
3. Use wide copper traces and power loop vias to improve thermal dissipation.
4. Connect the exposed pad to ground.
5. Place vias on the exposed pad for thermal dissipation on the IC.
6. Place small decoupling capacitors close to VIN, VOUT, and AGND.
7. Lay out the gate drive traces and return paths as directly as possible.
8. Lay out the forward and return traces close together to minimize the inductance of the gate drive path. They can either run side by side, or on top of each other on adjacent layers.
9. Use Kelvin connections to $R_{SENS2}$ for the average current sense and $R_{SENS1}$ for the cycle-by-cycle current.
10. Route lines in parallel from the $R_{SENS1}$ and $R_{SENSE2}$ terminals to the IC pins.
11. Avoid crossing noisy areas, such as SW1 and SW2, or gate drive traces.
12. Place the filter capacitor for the current-sense signal as close to the IC pins as possible.
13. Place the VCC and AVDD capacitors as close to the VCC and AVDD pins as possible.
14. Place the BST1 bootstrap capacitor close to the IC, and connect it directly to the BST1 and SW1 pins.
15. Place the BST2 bootstrap capacitor close to the IC, and connect it directly to the BST2 and SW2 pins.
16. To ensure the feedback loop is far from any noise source, place the FB dividers (R1 and R2) as close to the FB and AGND pins as possible.
17. Separate the power and signal paths to ensure that no power or switching current flows through the AGND connections.
18. Connect the PGND and AGND traces near the PGND pin, near the VCC capacitor PGND connection, or near the PGND connection of the cycle-by-cycle current-sense resistor ($R_{SENS1}$).




**Top Layer**



**Bottom Layer**

**Figure 13: Recommended PCB Layout**

# TYPICAL APPLICATION CIRCUIT

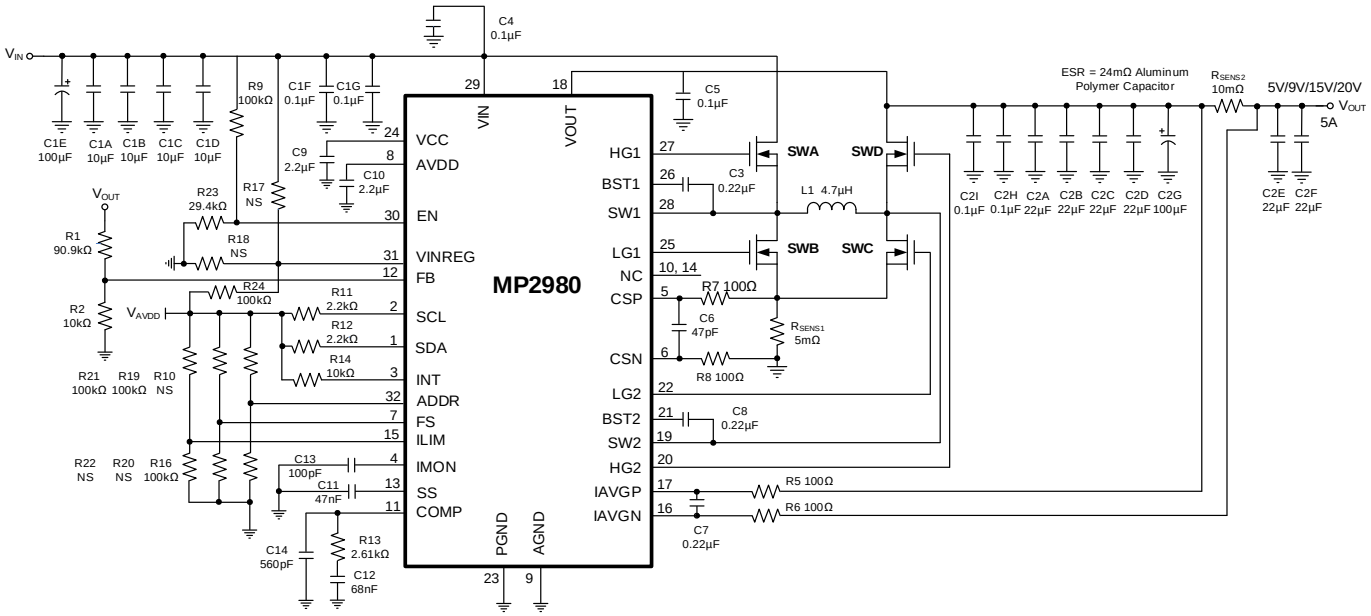


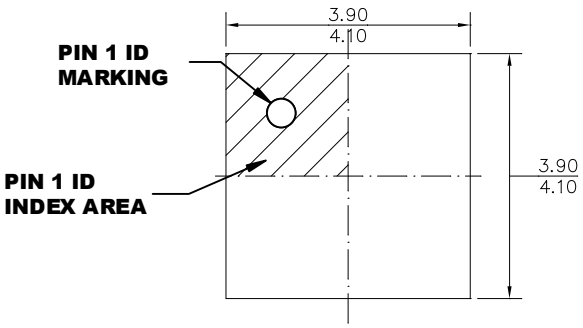

**Figure 14: Typical Application Circuit ($V_{IN}$ = 12V, $V_{OUT}$ = 5V/9V/15V/20V for 100W)**

**Note:**

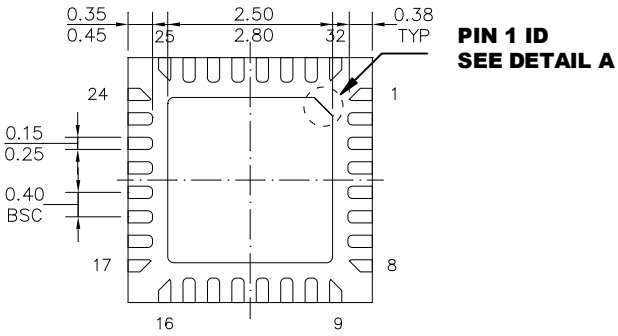
13) For USB PD applications, it is recommended to set ADDR equal to AVDD, which turns off the MP2980 by default. Otherwise, set ADDR equal to AGND, which turns on the MP2980 by default (see Table 1 on page 28).

# PACKAGE INFORMATION

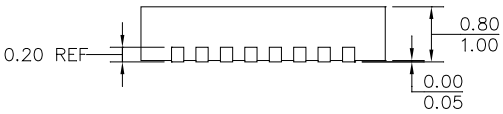
## QFN-32 (4mmx4mm)



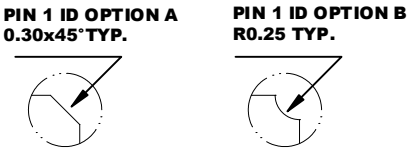

**TOP VIEW**



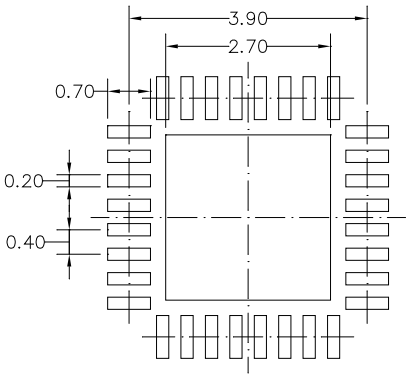

**BOTTOM VIEW**




**SIDE VIEW**




**DETAIL A**

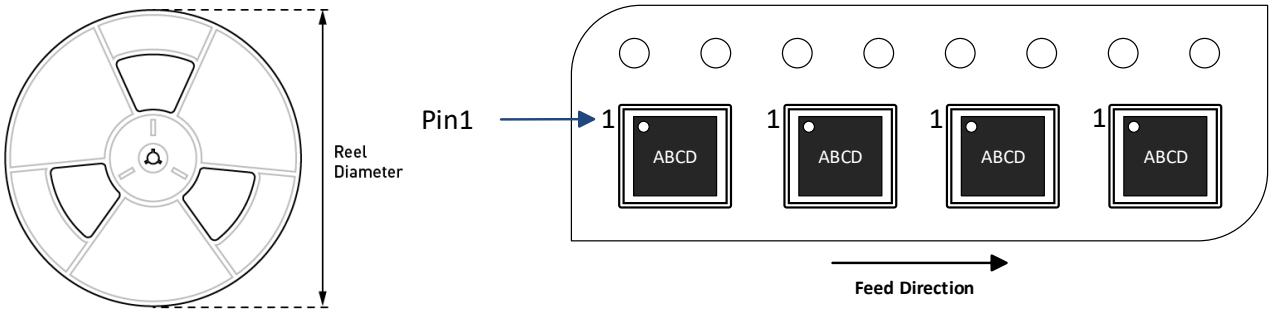



**RECOMMENDED LAND PATTERN**

## NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP2980GR-Z | QFN-32 (4mmx4mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 11/9/2023 | Initial Release | - |