MP4054A

Primary-Side Control, Offline LED Controller with Active PFC, NTC and PWM Dimming

DESCRIPTION

The MP4054A is a primary-side-control, offline LED lighting controller. In a tiny TSOT23-8 package, it achieves high power factor (PF) and accurate LED current for isolated, single-power-stage lighting applications.

This simplifies LED-lighting-system design significantly by eliminating the secondary-side feedback components and the optocoupler.

The MP4054A integrates power factor correction (PFC) and valley switching mode to reduce MOSFET switching losses.

The MP4054A has NTC function and allows PWM dimming.

To enhance system reliability and safety, the MP4054A has multiple internally integrated protection features, including over-voltage protection (OVP), short-circuit protection (SCP), primary-side over-current protection (OCP), brown-out protection, over-temperature protection (OTP), cycle-by-cycle current limit, VCC under-voltage lockout (UVLO), and auto-restart function.

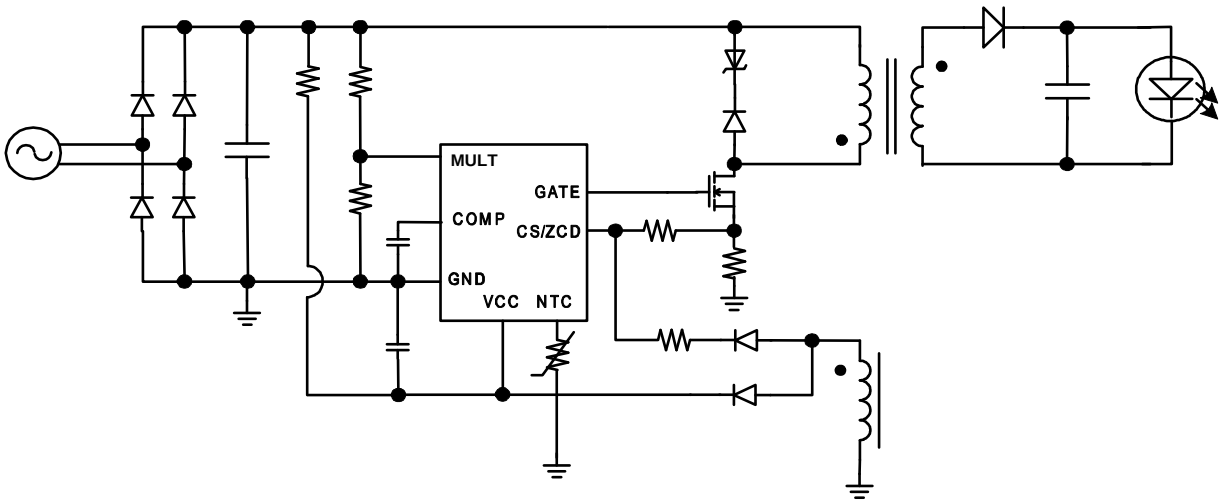
FEATURES

- Real-Current Control without Secondary-Feedback Circuit
- <2% Line/Load Regulation
- NTC Thermal Current Fold-Back
- PWM Dimming Available
- High PF (≥0.9) over Universal Input Voltage
- Valley Switching Mode for Improved Efficiency
- Brown-Out Protection
- Over-Voltage Protection
- Short-Circuit Protection
- Over-Temperature Protection
- Primary-Side Over-Current Protection
- Cycle-By-Cycle Current Limit
- VCC Under-Voltage Lockout Protection
- Auto-Restart Function
- Available in TSOT23-8 Package

APPLICATIONS

- Solid-State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

Part Number	Package	Top Marking
MP4054AGJ*	TSOT23-8	*See Below*

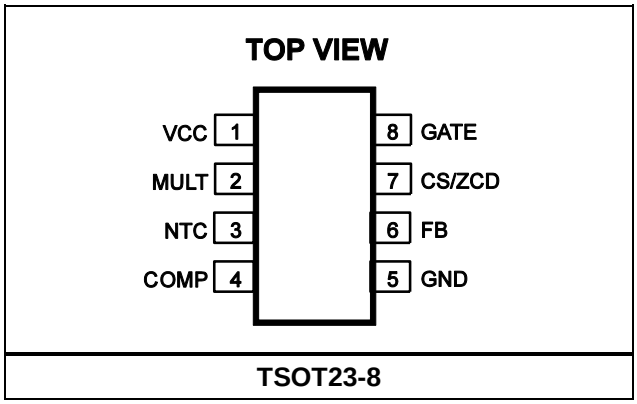
* For Tape & Reel, add suffix –Z (e.g. MP4054AGJ–Z)

TOP MARKING

|ALRY

ALR: product code of MP4054AGJ;
Y: year code.

PACKAGE REFERENCE



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

VCC ..... -0.3V to +30V
GATE Drive Voltage ..... -0.3V to +17V
CS/ZCD ..... -0.3V to 6.5V
Other Analog Inputs and Outputs.. -0.3V to 6.5V
Max. GATE Source Current 0.8A
Max. GATE Sink Current ..... -1A
Continuous Power Dissipation (T_A = +25°C) (2)
TSOT23-8 ..... 1.25W
Junction Temperature ..... -40°C to +150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage VCC ..... 12V to 28V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSOT23-8……....	100....	55..	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX) = (T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

Typical values are at VCC = 20V, T_J = +25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Voltage						
Operating Range	VCC	After turn on	12		28	V
Turn-On Threshold	VCC_{ON}	VCC rising edge	23.0	25.5	28.0	V
Turn-Off Threshold	VCC_{OFF}	VCC falling edge	8.4	9.5	11.0	V
Hysteretic Voltage	VCC_{HYS}		14.2	15.7	17.3	V
Supply Current						
Start-Up Current	$I_{STARTUP}$	VCC= VCC_{ON} -1V		20	50	µA
Quiescent Current	I_Q	No switching		0.6	0.85	mA
Operating Current Under Fault Condition		No switching		2		mA
Operating Current	I_{CC}	f_s =70kHz,C_{GATE}=1nF		2	3	mA
Multiplier						
Linear Operation Range	V_{MULT}		0		3	V
Gain	K(5)			1.3		1/V
Brown-Out Protection Threshold			270	300	330	mV
Brown-Out Detection Time			25	42	60	ms
Brown-Out Protection Hysteretic Voltage			70	100	130	mV
NTC						
High-Threshold Voltage	$V_{H\ NTC}$		1.17	1.23	1.29	V
Low-Threshold Voltage	$V_{L\ NTC}$		0.67	0.77	0.87	V
Shutdown Threshold	V_{SD_NTC}		0.355	0.39	0.425	V
Shutdown-Voltage Hysteretic			85	100	115	mV
Pull-Up Current Source	I_{PULL_UP}		44	54	64	µA
Leakage Current	$I_{LEAKAGE}$				1	µA
Error Amplifier						
Reference Voltage	V_{REF}		0.401	0.413	0.425	V
Transconductance(6)	G_{EA}			125		µA/V
Upper Clamp Voltage	V_{COMP_H}		4.5	4.75	5.1	V
Lower Clamp Voltage	V_{COMP_L}		1.42	1.5	1.58	V
Max. Source Current(6)	I_{COMP_SOURCE}			50		µA
Max. Sink Current(6)	I_{COMP_SINK}			-200		µA

ELECTRICAL CHARACTERISTICS *(continued)*

Typical values are at VCC = 20V, T_J = +25°C, unless otherwise noted.
Minimum and maximum values are at VCC = 20V, T_J = -40°C to +125°C, unless otherwise noted, guaranteed by characterization.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Current Sense Comparator and Zero Current Detector						
CS/ZCD Bias Current	$I_{BIAS\_CS/ZCD}$				500	nA
Leading-Edge-Blanking Time	t_{LEB_CS}		290	400	650	ns
Current-Sense Clamp Voltage	V_{CS_CLAMP}		1.9	2.0	2.1	V
Over-Current Protection, Leading-Edge-Blanking Time	$t_{LEB\_CS\_OCP}$		190	280	480	ns
Over-Current Protection Threshold	V_{CS_OCP}		2.36	2.46	2.56	V
Zero-Current Detection Threshold	V_{ZCD_T}	V_{ZCD} falling edge	0.270	0.295	0.318	V
Zero-Current Detect Hysteresis	V_{ZCD_HYS}		562	595	628	mV
ZCD Blanking Time	t_{LEB_ZCD}	After turn-off, V_{MULT_O}[5] >0.3V	1.2	1.6	2.1	µs
		After turn-off, V_{MULT_O} ≤0.3V	0.6	0.8	1.1	µs
Over-Voltage Blanking Time	t_{LEB_OVP}	After turn-off, V_{MULT_O} >0.3V	1.2	1.6	2.1	µs
		After turn-off, V_{MULT_O} ≤0.3V	0.6	0.8	1.1	µs
Over-Voltage Protection Threshold	V_{ZCD_OVP}	1.6µs delay after turn-off	4.9	5.1	5.4	V
Minimum Off Time	t_{OFF_MIN}		4	5.5	8	µs
Starter						
Start-Timer Period	t_{START}			190		µs
Gate Driver						
Output-Clamp Voltage	V_{GATE_CLAMP}	VCC=28V	13.0	14.5	17.0	V
Minimum-Output Voltage	V_{GATE_MIN}	VCC=VCC_{OFF} + 50mV	6.7			V
Max. Source Current[6]	I_{GATE_SOURCE}			0.8		A
Max. Sink Current[6]	I_{GATE_SINK}			-1		A
Thermal Shutdown						
Thermal Shutdown Threshold[6]	T_{SD}			150		°C
Thermal Shutdown Recovery Hysteresis[6]	T_{HYS}			25		°C

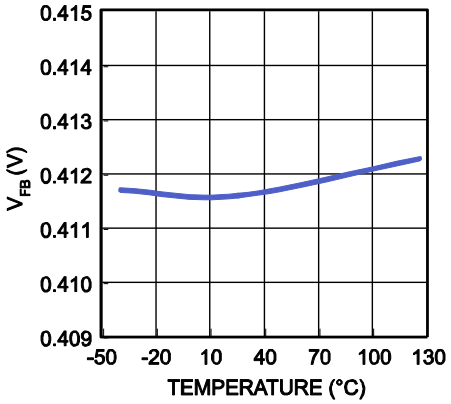
Notes:

5) The multiplier output V_{MULT_O} is given by: $V_{CS}=V_{MULT\_O}=K•V_{MULT}•(V_{COMP}-1.5)$
6) Guaranteed by characterization.

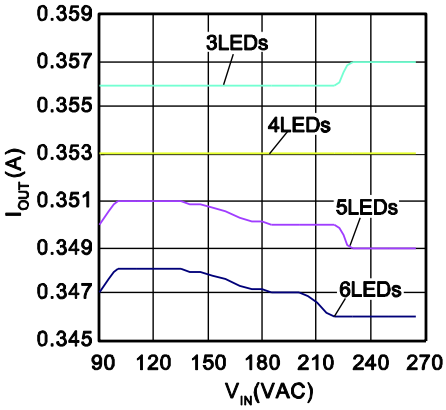
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 90VAC to 264VAC, Isolated Flyback Converter, 6 LEDs in series, V_{OUT} = 20V, I_{LED}=350mA, T_A = 25°C, unless otherwise noted.

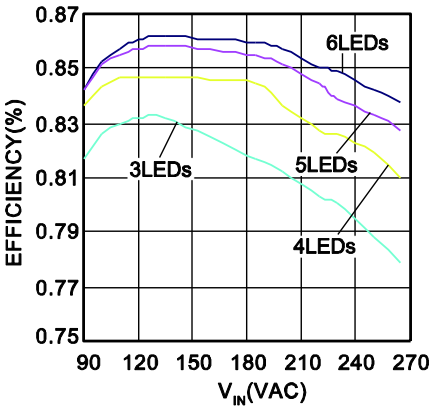
V_{FB} Temperature Tendency



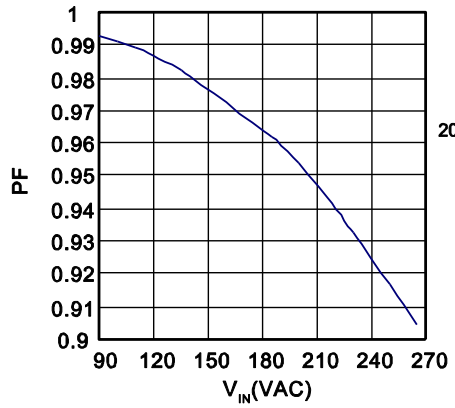
Line/Load Regulation



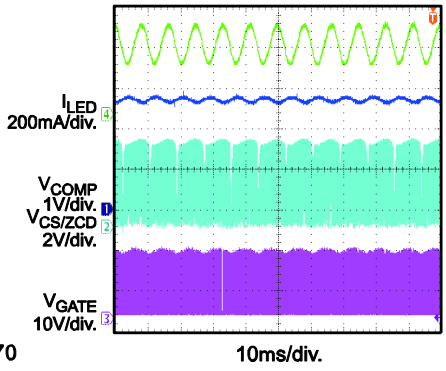
Efficiency



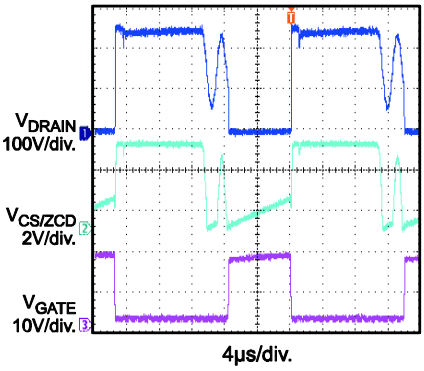
PF @Full Load



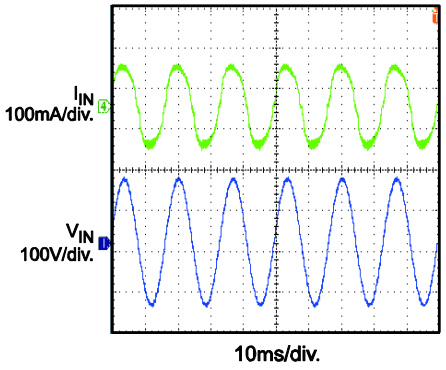
Steady State
V_{IN} =110V



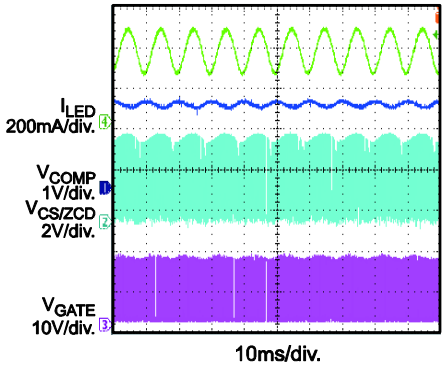
Steady State
V_{IN} =110V



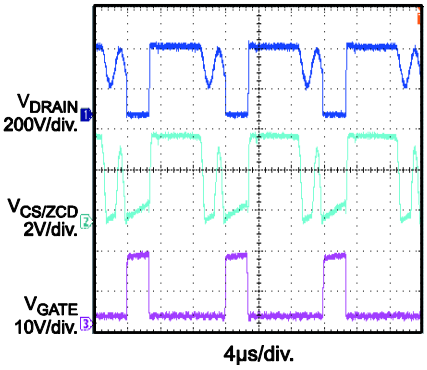
Steady State
V_{IN} =110V



Steady State
V_{IN} =230V



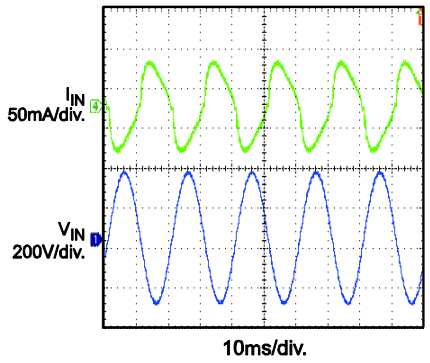
Steady State
V_{IN} =230V



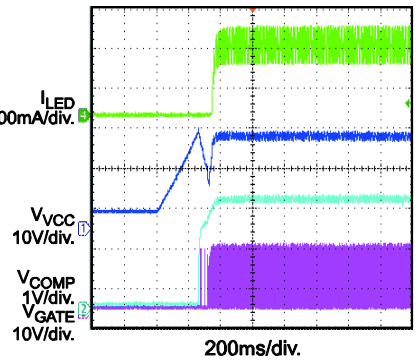
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 90VAC to 264VAC, Isolated Flyback Converter, 6 LEDs in series, V_{OUT} = 20V, I_{LED}=350mA, T_A = 25°C, unless otherwise noted.

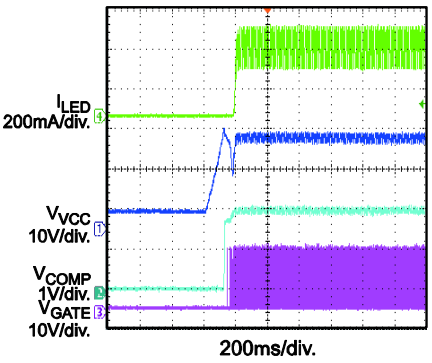
Steady State
V_{IN} =230V



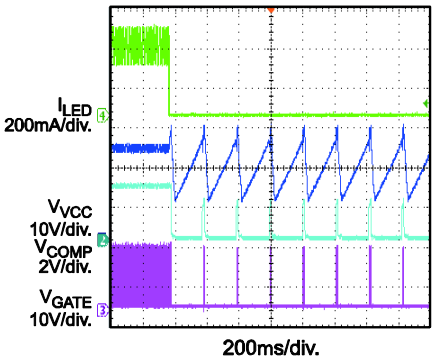
VIN Start up
V_{IN} = 110V



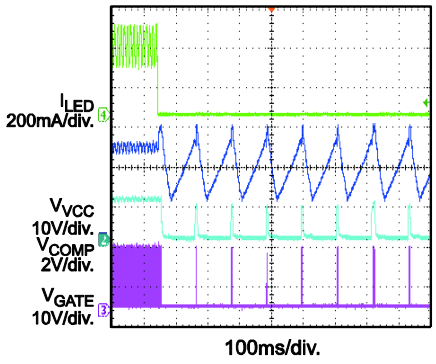
VIN Start up
V_{IN} = 230V



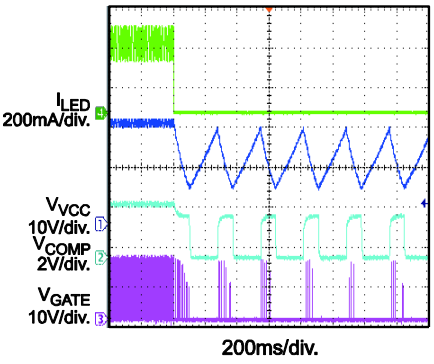
Open LED Protection
V_{IN} = 110V, Open LED @ Working



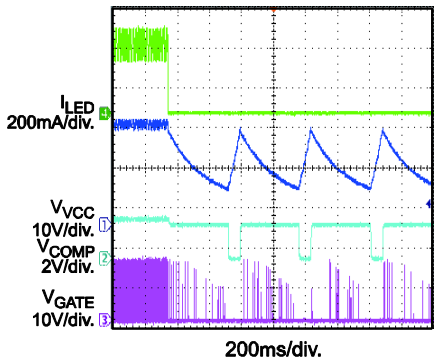
Open LED Protection
V_{IN} =230V, Open LED @ Working



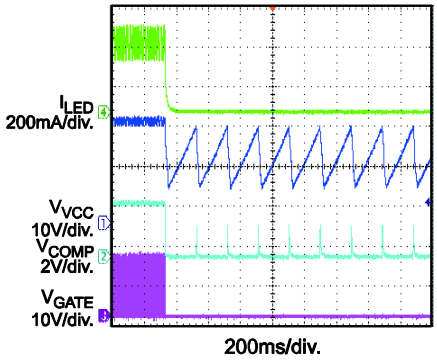
Short Circuit Protection
V_{IN} =110V
Short LED+ to LED- @ Working



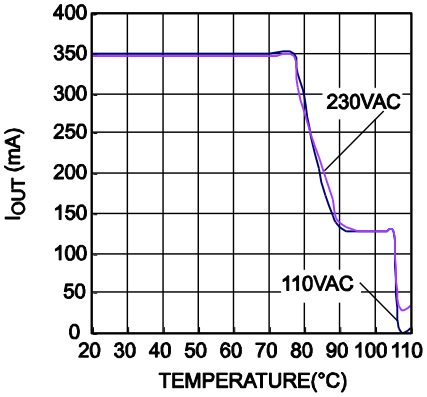
Short Circuit Protection
V_{IN} =230V
Short LED+ to LED- @ Working



Primary-Side OCP Protection
V_{IN} =230V
Short primary winding @ Working



NTC Curve
R_{NTC}=220kΩ



PIN FUNCTIONS

Pin #	Name	Description
1	VCC	**Power Supply Input.** Supply power for the control signals and driving high-current MOSFET. Bypass to ground with an external bulk capacitor (typically 4.7µF).
2	MULT	**Multiplier Input.** Connect to the tap of resistor divider between the rectified AC line and GND. The half-wave sinusoid provides a reference signal for the internal-current-control loop. MULT is used for brown-out protection detection.
3	NTC	**LED Temperature Protection.** Connect an NTC resistor from this pin to GND can reduce the output current to protect the LED when ambient temperature rising high. Apply an external PWM signal on this pin can dim the LED with PWM mode. A 2.2nF to 4.7nF ceramic cap is recommended to connect from NTC to GND to bypass the high frequency noise when activate temperature protection. For PWM dimming, the cap can be removed.
4	COMP	**Loop Compensation Input.** Connect a compensation network to stabilize the LED driver and maintain an accurate LED current.
5	GND	**Ground.** Current return for the control signal and the gate-drive signal.
6	FB	**Feedback Input.** If the accurate LED current is needed, connect this pin to the LED-current-sensing resistor.
7	CS/ZCD	**Current-Sense and Zero-Current Detection.** This is a MPS proprietary dual function pin. When the gate driver turns on, CS/ZCD senses the MOSFET current. The difference between the sensed voltage and the internal sinusoidal-current-reference determines when the MOSFET turns off. When the gate driver turns off, the zero crossing (after blanking time) triggers GATE turn-on signal. Connect CS/ZCD to a resistor divider through a diode between the auxiliary winding and GND. Output over-voltage condition is detected through ZCD. During every turn-off interval, if the ZCD voltage exceeds the over-voltage protection threshold, after the 1.6µs (V_{MULT_O}>0.3V) or 0.8µs (V_{MULT_O}≤0.3V) blanking time, over-voltage protection is triggered and the system stops switching until auto-restart. CS/ZCD is used for primary-side over-current protection. If the sensing voltage reaches 2.46V (after blanking time), the primary-side over-current protection is triggered and the system stops switching until auto-restart. A 10pF ceramic cap is recommended to connect CS/ZCD to GND to bypass the high-frequency noise. In order to reduce RC delay influence on the accuracy of the current-sensing signal, a 1kΩ down-side resistance (R_{ZCD2} in Figure 7) from CS/ZCD is recommended.
8	GATE	**Gate Drive Output.** This totem-pole output stage can drive a high-power MOSFET with a peak current of 0.8A source and 1A sink. The high-voltage limit is clamped to 14.5V to avoid excessive gate-drive voltage. The drive-voltage is higher than 6.7V to guarantee a sufficient drive capacity.

FUNCTION DIAGRAM

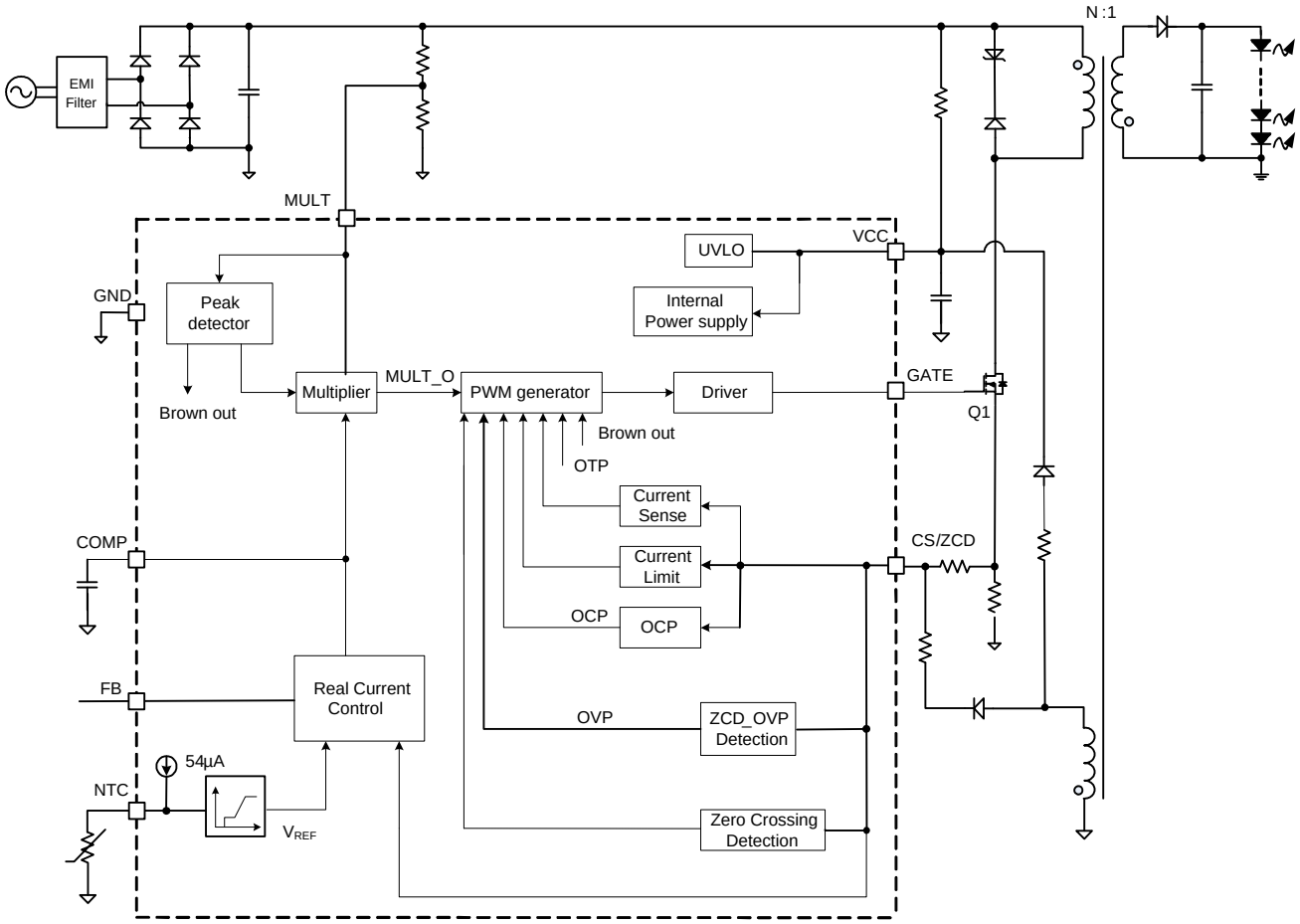


Figure 1: MP4054A Function Block Diagram

OPERATION

The MP4054A is a primary-side control, offline LED controller. It incorporates all the features of high-performance LED lighting. The LED current is controlled accurately with the real-current control method from primary-side information. Active power factor correction (PFC) eliminates unwanted harmonic noise on the AC line. The rich protection features achieve high safety and reliability in real application.

Start Up

Initially, the VCC cap is charged by the start-up resistor from the AC line. When VCC reaches 25.5V, the control logic activates and the gate driver signal begins to switch; the power supply is taken over by the auxiliary winding.

The chip shuts down when VCC drops below 9.5V.

The high hysteretic voltage allows for a small VCC capacitor (typically 4.7μF) to shorten the start-up time.

Valley Switching Mode

During the external MOSFET ON-time (t_{ON}), the rectified-input voltage (V_{BUS}) charges the primary-side inductor (L_P) causing the primary-side current (I_{PRI}) to increase linearly from zero to peak value (I_{PK}). When the MOSFET turns off, the energy stored in the inductor is transferred to the secondary-side, which activates the secondary-side diode to power the load. The secondary current (I_{SEC}) decreases linearly from its peak value to zero. When the secondary current decreases to zero, the MOSFET drain-source voltage starts oscillating, which is caused by the primary-side magnetizing inductance and parasitic capacitances—the voltage ring also is reflected on the auxiliary winding (see Figure 2). To improve primary-control precision, the chip monitors when ZCD voltage falls to zero twice before the next switching period. The zero-current detector from CS/ZCD generates GATE turn-on signal when the ZCD voltage falls below 0.295V the second time (see Figure 3).

This virtually eliminates switch turn-on loss and diode reverse-recovery losses, ensuring high efficiency and low EMI noise.

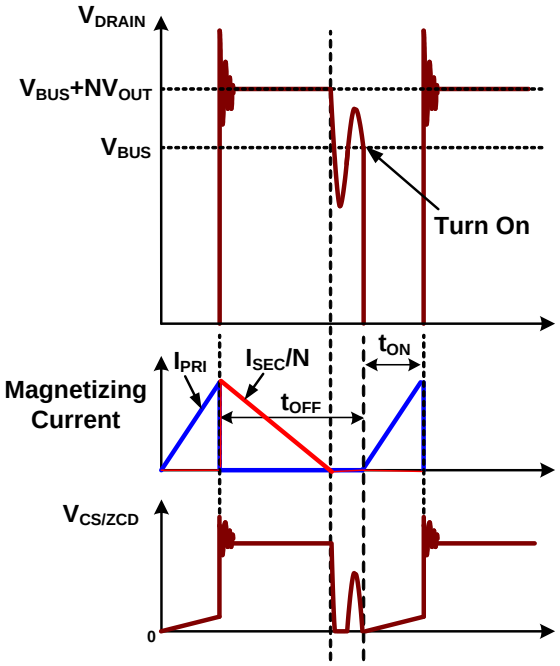


Figure 2: Valley Switching Mode

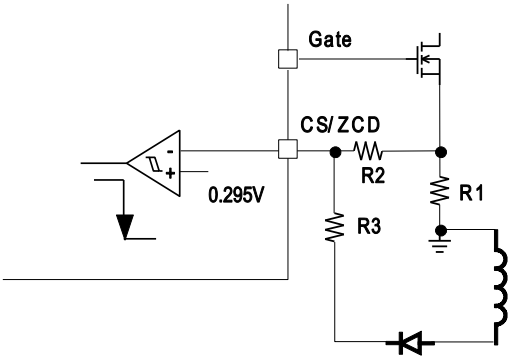


Figure 3: Zero-Current Detector

Real-Current Control

The proprietary real-current-control method allows the MP4054A to control the secondary-side LED current using primary-side information. The mean value of the output LED current is calculated approximately as:

$$I_o \approx \frac{N \cdot V_{REF}}{2 \cdot R_S}$$

- N—Turn ratio between primary side and secondary side;

- V_{REF}—The feedback reference voltage (typical 0.413V);
- R_S—The sensing resistor connected between the MOSFET source and GND.

Power-Factor Correction (PFC)

MULT is connected to a pull-up resistor from the rectified-instantaneous-line voltage; the multiplier output is sinusoidal. This signal sets the sinusoidal primary side peak current. This achieves a high power factor (PF).

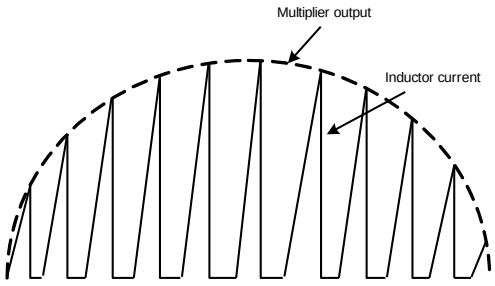


Figure 4: Power-Factor Correction

The maximum output voltage of the multiplier is clamped to 2.0V, setting the cycle-by-cycle current limit.

VCC Under-Voltage Lockout (UVLO)

When the VCC voltage drops below the UVLO threshold 9.5V, the IC stops switching and shuts down; the operating current is very low under this condition. VCC is then charged by the external resistor from the AC line. Figure 5 shows the typical waveform of UVLO.

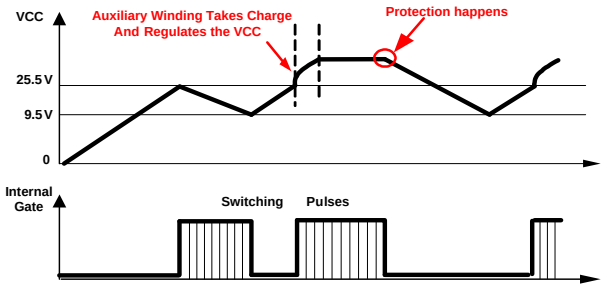


Figure 5: VCC Under-Voltage Lockout

Auto Starter

The MP4054A integrates an auto-restart that begins timing when the MOSFET turns off. If ZCD fails to send a turn-on signal after 190μs, a turn-on signal is initiated. This avoids an unnecessary IC shut down if ZCD misses detection.

Minimum Off Time

The MP4054A operates with variable switching frequency. The frequency changes with the input instantaneous line voltage. To limit the maximum frequency and enhance EMI performance, the chip employs an internal minimum OFF-time of 5.5μs.

Leading-Edge Blanking (LEB)

Internal leading-edge-blanking (LEB) is employed to prevent a switching pulse from terminating prematurely due to parasitic capacitance discharging when the MOSFET turns on. During the blanking time, the path from CS/ZCD to the current comparator input is blocked. Figure 6 shows the leading-edge blanking time. The LEB time of primary-side OCP detection is relatively short at 280ns.

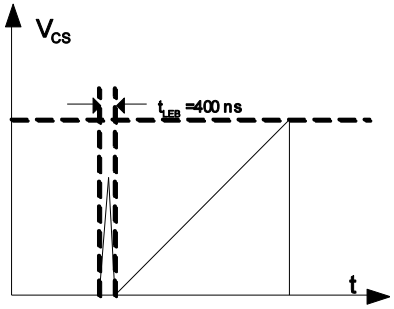


Figure 6: Leading-Edge Blanking

Output Over-Voltage Protection (OVP)

Output over-voltage protection prevents component damage from over-voltage conditions. The auxiliary winding's positive plateau voltage is proportional to the output voltage; the OVP uses the auxiliary-winding voltage instead of directly monitoring the output voltage.

Figure 7 shows the OVP circuit. Once the ZCD voltage is higher than 5.1V and exceeds the OVP blanking time (during the gate turn-off interval), the OVP signal is latched, turning the gate driver off. When VCC drops below UVLO, the IC restarts.

The output OVP setting point is calculated as:

$$V_{OUT\_OVP} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot \frac{R_{ZCD2}}{R_{ZCD1} + R_{ZCD2}} = 5.1V$$

- V_{OUT_OVP}—The output over-voltage protection point;
- N_{AUX}— The auxiliary winding turns;
- N_{SEC}— The secondary winding turns

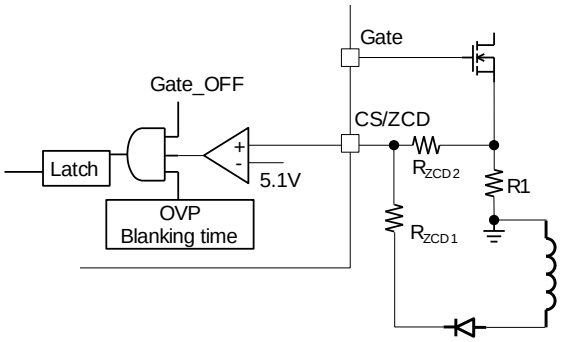


Figure 7: OVP Sampling Unit

To prevent a voltage spike from an OVP mis-trigger, OVP sampling has a t_{LEB_OVP} blanking period, typically 1.6µs when V_{MULT_O} > 0.3V and 0.8µs when V_{MULT_O} ≤ 0.3V (see Figure 8).

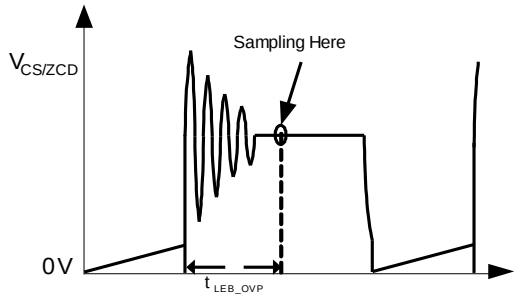


Figure 8: ZCD Voltage and OVP Sampler

A current-limit resistor between the output of the auxiliary winding and the ZCD resistor divider also works as a suppresser to avoid an OVP mis-trigger.

Output Short-Circuit Protection (SCP)

If an output short occurs, ZCD cannot detect the transformer's zero-current-crossing signal, so the 190µs auto-restart timer triggers the MOSFET's turn-on signal. The switching frequency of the power circuit drops to about 5kHz and the output current is limited to its nominal current. The auxiliary-winding voltage drops to follow the secondary-winding voltage, VCC drops to less than the UVLO threshold, and then the system restarts. This sequence limits both the output power and IC temperature if an output short occurs.

Primary-Side Over-Current Protection (OCP)

The primary-side over-current protection prevents device damage from excessive current, such as a primary winding short circuit. If the CS/ZCD voltage rises to 2.46V during the gate turn-on interval (see Figure 9), the primary-side over-current protection signal is latched, turning the gate driver off. When VCC drops below UVLO, the IC restarts.

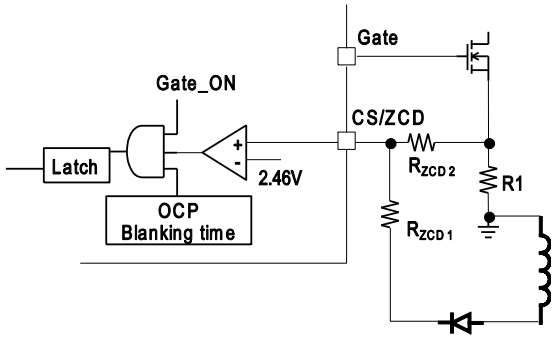


Figure 9: Primary-Side OCP Sampling Unit

Brown-Out Protection

The MP4054A has brown-out protection; the internal peak detector detects the peak value of the rectified sinusoid waveform on MULT. If the peak value is less than the brown-out protection threshold, 0.3V for typically 42ms, MP4054A identifies this as a brown-out, dropping COMP to zero and disabling the power circuit. If the peak value exceeds 0.4V, the IC restarts and the COMP voltage rises again softly. This feature prevents the transformer and LED current from saturating during fast ON/OFF switching (see Figure 10).

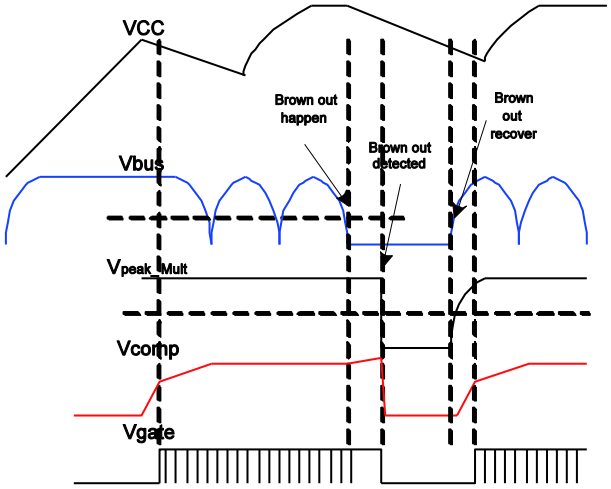


Figure 10: Brown-Out Protection Waveforms

NTC Thermal Protection

The NTC provides LED thermal protection. A NTC resistor to monitor the LED temperature can be connected to this pin directly. The internal pull-up resistor generates a corresponding voltage on the external NTC resistor, and the LED current changes as NTC voltage changes. Figure 11 shows the NTC curve.

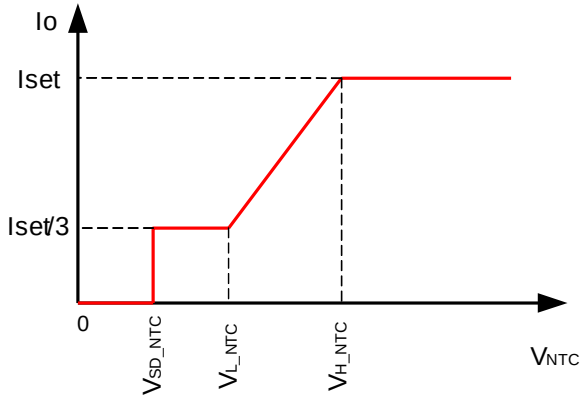


Figure 11: NTC Curve

If the NTC voltage drops below V_{SD_NTC}, the LED current drops to minimum output, the minimum output current is determined by gate minimum on time. (equal to 400ns LEB time)

PWM Dimming

The MP4054A can accept direct PWM dimming signal. Applying a PWM signal (>200Hz) on NTC pin can achieve dimming performance.

Following the NTC curve of Figure 11, if the high level of the PWM signal is higher than V_{H_NTC}, the internal reference voltage V_{REF} is full scale. And if the low level of the PWM signal is lower than V_{SD_NTC}, the internal reference voltage V_{REF} is at the minimal value. Then the internal reference voltage of EA can be modulated as the external PWM dimming signal to capture the duty cycle information.

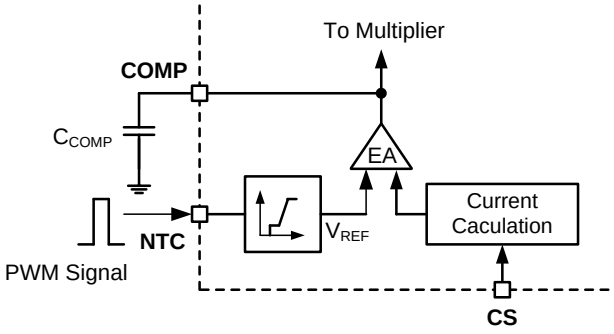


Figure 12: PWM Dimming

With large COMP cap, the loop response is slow. As long as the PWM frequency is higher than 200Hz, the duty cycle information can be filtered and averaged by COMP. Then, by the close loop control, the output LED current linearly changes with dimming duty from maximum to minimum.

IC Thermal Shut Down

To prevent thermal damage to the system and IC, if internal temperatures exceed 150°C, the MP4054A stops switching and the IC is latched off until VCC drops below UVLO and restarts.

NON-ISOLATED APPLICATIONS

Although isolated solutions can prevent electric shock from the grid when touching the load, they cause power loss and increase costs. Non-isolated solutions achieve higher efficiency and are highly cost-effective.

Generally, the flyback converter is used for offline, isolated applications. For the non-isolated applications, a low-side buck-boost topology is used. The MP4054A can operate in *both* offline isolated and non-isolated LED-lighting applications (see Figure 19).

Operation of Low-Side Buck-Boost

The low-side buck-boost equates to a flyback converter with a 1:1 turn ratio transformer. As opposed to an isolated solution, there is not a separate primary and secondary winding, making a smaller core size. This saves cost and improves the efficiency of the driver.

The Selection of FET & Rectifier Diode

Since it is just an inductor for non-isolated solution, compared with isolated solution, at same output voltage, the power FET can be selected with lower voltage rating. But, oppositely, the voltage rating of rectifier diodes for output and aux-winding must be increased.

Improvement of RF EMI

C12 in Figure 19 is added for RF EMI improvement. The recommended value is from 10nF to 68nF with 630V rating.

Improvement of PFC & THD

The 1:1 ratio reduces the converter's duty cycle using the same specifications. Based on the PFC principle in an isolated solution, the converter's PF and THD drops. A non-isolated solution is suitable particularly for high-output voltage since the higher output voltage can extend the duty cycle to improve PF, THD and efficiency.

For a non-isolated solution with low-output voltage, the tapped inductor can be applied to improve the PF and THD.

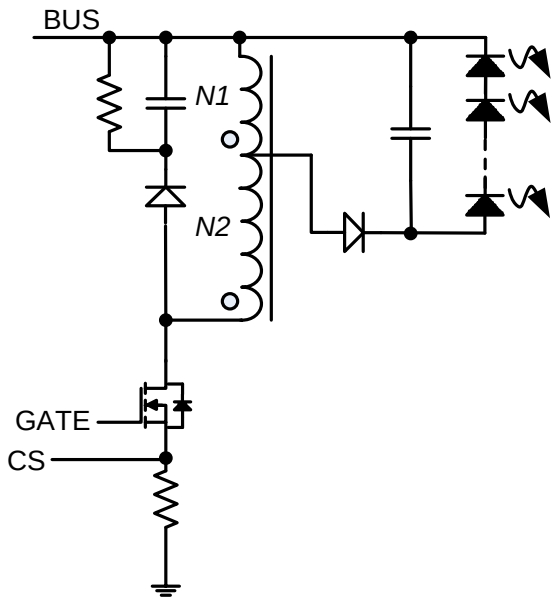


Figure 13: Tapped-Inductor for Low-Side Buck-Boost Solution

Shown in Figure 13, the tapped-inductor includes two windings (N1 & N2) and a tap to connect the rectifier diode. When the power FET is turned on, the current goes through both of the windings. When the power FET is off, only N1 conducts the current through the rectifier diode. The stored energy of N2 is released by flux couple. The tapped inductor features a turn ratio similar to the transformer in an isolated solution.

The nominal turns ratio is

$$n = \frac{N1 + N2}{N1} > 1$$

The duty cycle of the converter is extended by the tapped inductor, which makes the improved PF and THD available.

Like the transformer, the snubber is necessary to clamp the voltage spike.

However, the non-dimmable solution usually needs to cover the universal input range. The input range is very wide, from 85VAC to 264VAC. MULT is used to detect the input-voltage signal, but the resistor divider of MULT

is fixed. At high-line input, the signal for MULT is very low, which results in an adverse affect on the internal multiplier sampling; this affects the PFC performance.

Figure 14 shows an improved circuitry on the MULT resistor divider; this adjusts the ratio of the divider to enhance THD.

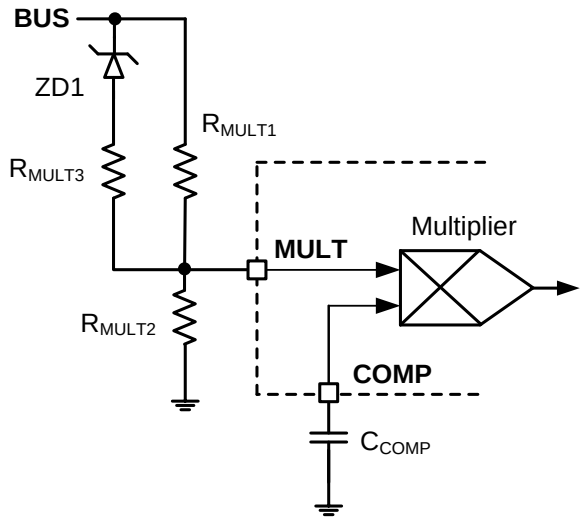


Figure 14: THD Improved Circuitry

The ZD1 is a HV Zener diode. The common voltage rating is from 80V to 130V.

At low line input, ZD1 does not conduct. The MULT signal is:

$$V_{MULT} = V_{BUS} \times \frac{R_{MULT2}}{R_{MULT1} + R_{MULT2}}$$

When the input voltage rises above ZD1 threshold, R_{MULT3} is paralleled with R_{MULT1} to increase the ratio of the divider; this raises the MULT signal.

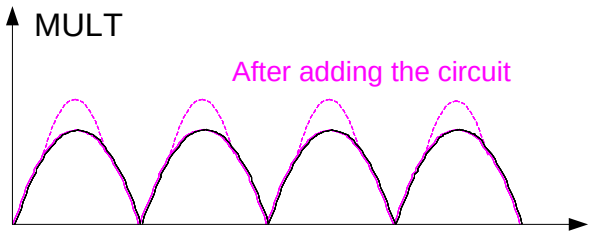


Figure 15: The MULT Signal with THD Improved Circuitry

As shown in Figure 15, after adding the THD improved circuitry, the MULT voltage rises. The input current at the top of BUS is increased while the input current at the zero-crossing is reduced. This results in the input current becoming more sinusoidal, improving THD.

Operation of High-Side Buck/Buck-Boost

The MP4054A features FB pin, which is used to receive the feedback signal of LED current directly. So, the MP4054A can be designed in high-side Buck or Buck-Boost application to achieve excellent LED current accuracy regulation, especially for very high load regulation requirement.

Figure 20 is a 7.2W high-side Buck solution.

High-side Buck solution can achieve higher efficiency. But the system just works @ $V_{IN}>V_{OUT}$ based on step-down converter's operation. But the input voltage of PFC solution is a sinusoid wave. When $V_{IN}<V_{OUT}$, the gate keeps ON and V_{OUT} drops, so the solution is suitable for the low V_{OUT} application (relative to input voltage). And since the system is out of control at zero-crossing, it has adverse effect on THD.

High-side Buck-boost's operation is similar as low-side Buck-boost. With LED current sample, it can cover very wide output voltage range, like up to 100V voltage difference.

Layout Considerations of High-Side Solution

Since GND is not connected on a stable point but on switching for high-side solution, the noise impact is serious. Good layout is very important for high-side solution's stable operation.

The external feedback resistors should be placed next to the FB pin. And the switching loop is sensitive to noise, so the switch node traces should be short and away from the feedback network. The switching loop includes input/output caps, MOS & rectifier diode.

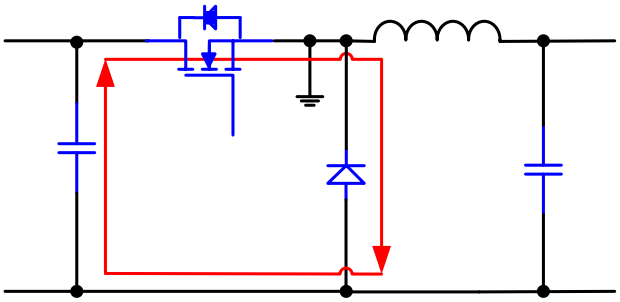


Figure 16: The Switching Loop of High-Side Buck

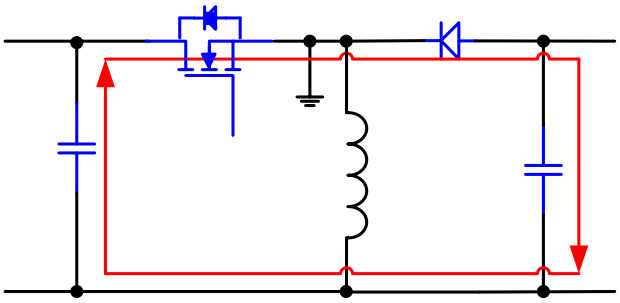


Figure 17: The Switching Loop of High-Side Buck-Boost

TYPICAL APPLICATION CIRCUITS

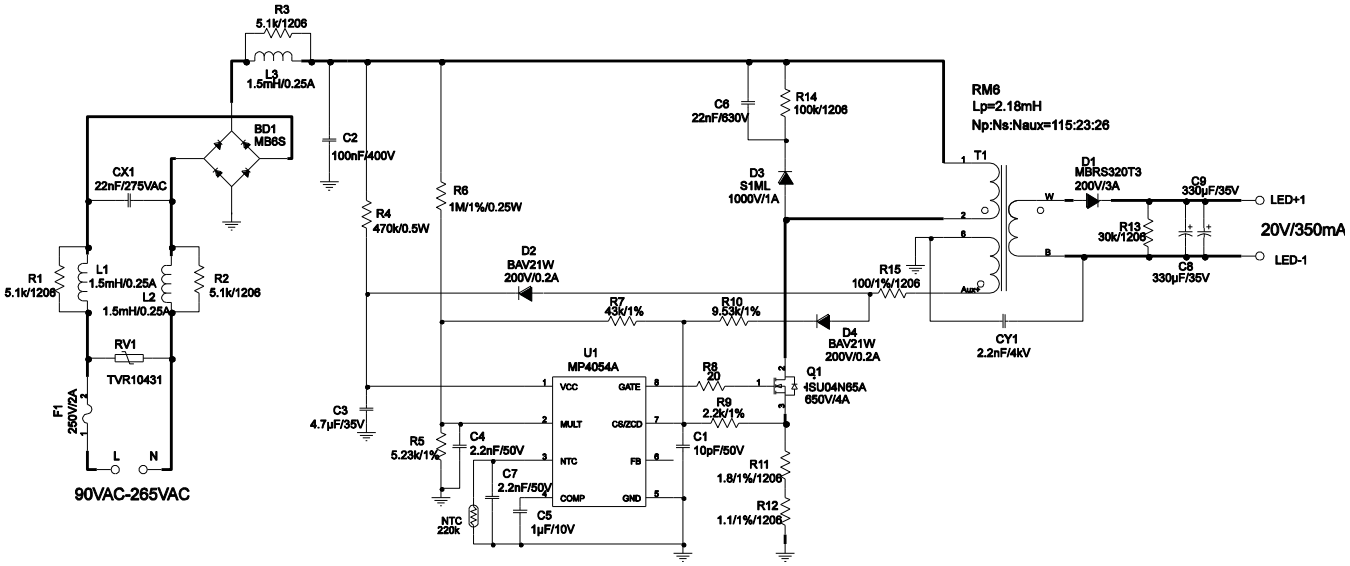


Figure 18: A19 Bulb Driver, 90-265VAC Input, Isolated Flyback Converter, V_O =20V, I_{LED}=350mA

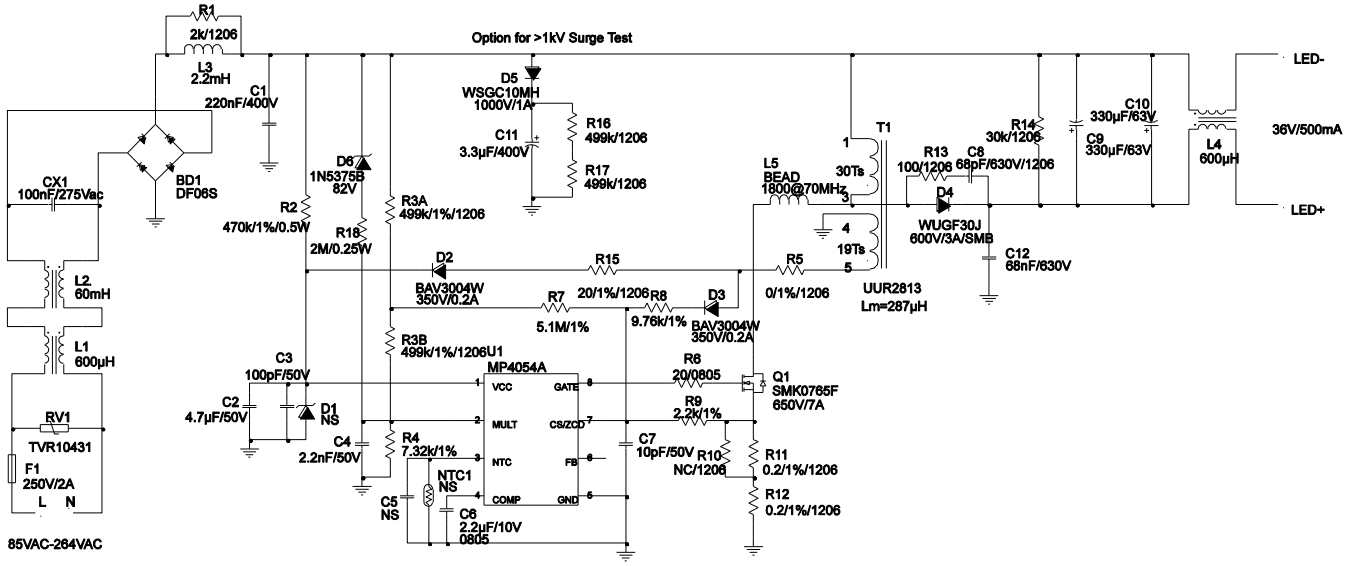


Figure 19: T8 Driver, 85-265VAC Input, Low-side Buck-boost Converter, V_O =36V, I_{LED}=500mA

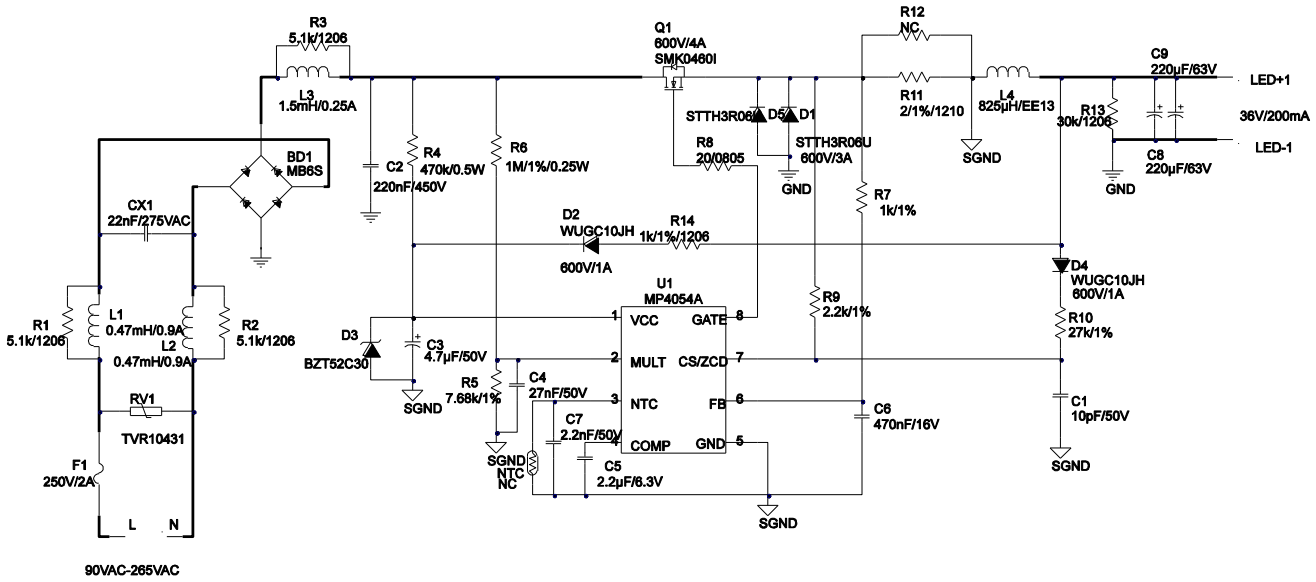
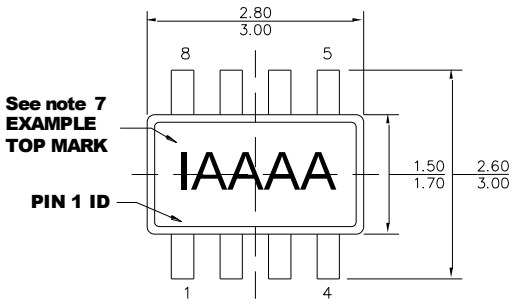


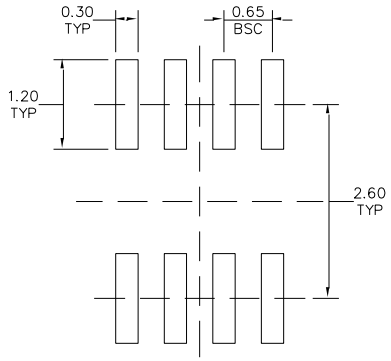
Figure 20: A19 Bulb Driver, 90-265VAC Input, High-side Buck Converter, V_O =36V, I_{LED}=200mA

PACKAGE INFORMATION

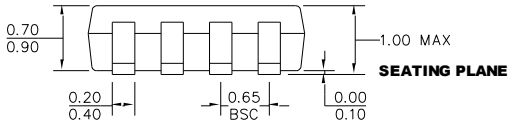
TSOT23-8



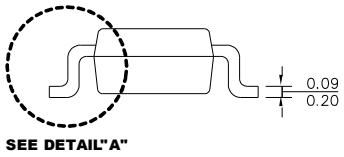
TOP VIEW



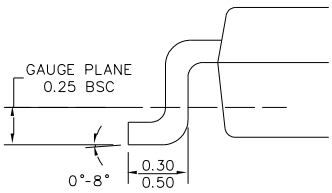
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA
6) DRAWING IS NOT TO SCALE
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)