MP5030D

USB Charging Port Controller with Load Detection Supporting CDP, DCP Modes

DESCRIPTION

The MP5030D integrates a USB current-limit switch and charging port identification circuitry. The MP5030D achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limit programmable. The MP5030D supports dedicated charging port (DCP) and charging downstream port (CDP) schemes for battery charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for external user interaction.

The MP5030D provides linear line drop compensation, load current detection, and status indication.

Full protection features include hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

The MP5030D requires a minimal number of readily available, standard, external components to complete the USB switch and charging mode auto-detection solution. The MP5030D is available in a QFN-10 (1.5mmx2mm) package.

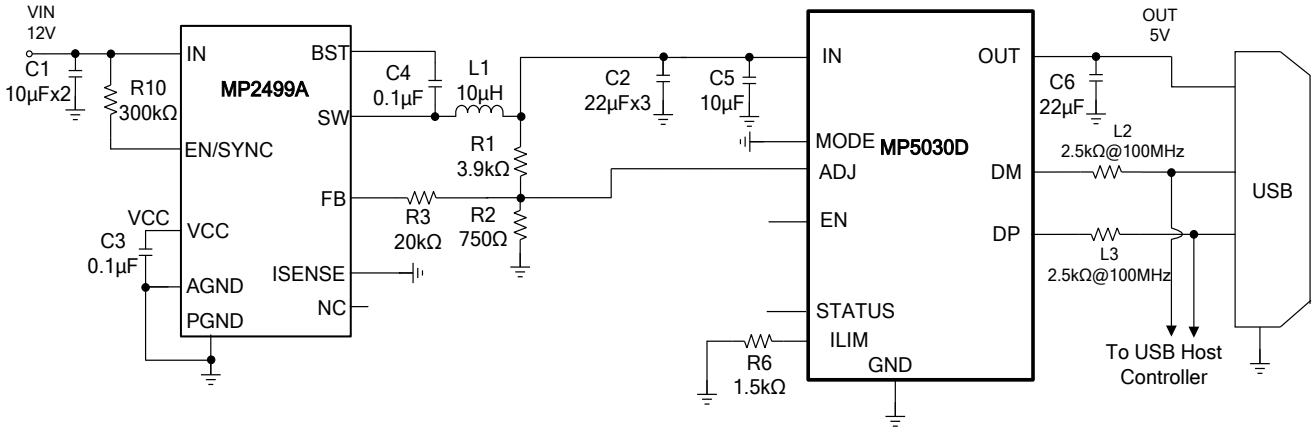
FEATURES

- Load Current Detection and Status Indication
- Up to 14V Operating Input Voltage Range
- Support DCP Schemes for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- Supports CDP Mode Handshaking
- Line Drop Compensation
- Programmable High-Accuracy Current Limit
- 32mΩ Low $R_{DS(ON)}$ Power MOSFET
- Input Over-Voltage Shutdown Protection
- Compatible with Buck, Boost, and AC/DC Converters
- Available in a QFN-10 (1.5mmx2mm) Package

APPLICATIONS

- USB Power Supplies
- AC/DC Wall Adapter with USB Ports
- Cigarette Lighter Adapters
- Power Bank

TYPICAL APPLICATION



CDP Mode Set-Up for USB2.0 Application

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5030DGQH	QFN-10 (1.5mmx2mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5030DGQH–Z).

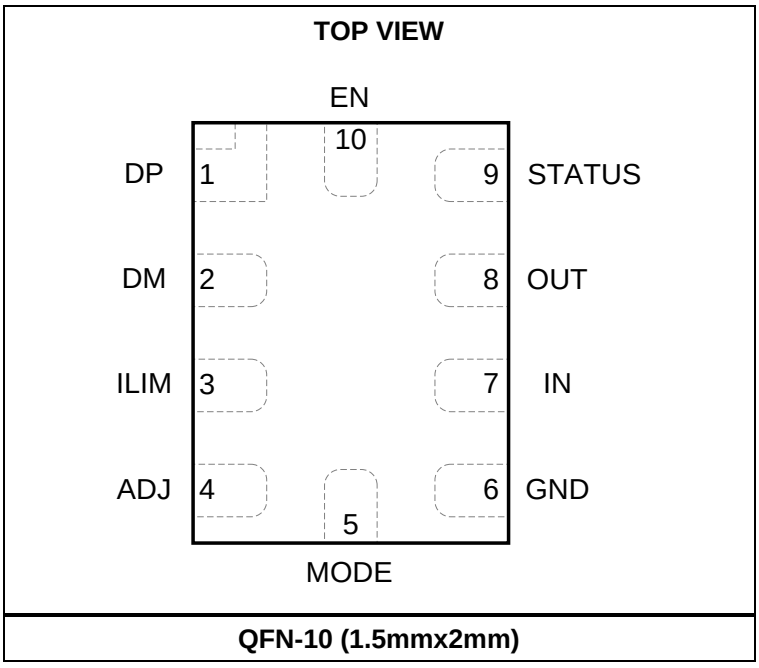
TOP MARKING

HQ

LL

HQ: Product code of MP5030DGQH
LL: Lot number

PACKAGE REFERENCE



QFN-10 (1.5mmx2mm)

PIN FUNCTIONS

Package Pin #	Name	Description
1	DP	**D+ data line to the USB connector.** DP is the input/output pin used for handshaking with portable devices.
2	DM	**D- data line to USB connector.** DM is the input/output pin used for handshaking with portable devices.
3	ILIM	**Current-limit level set.** Place a resistor between ILIM and GND to achieve a high-accuracy current limit.
4	ADJ	**Output voltage adjustment.** ADJ sinks a current from the upstream DC/DC converter's FB pin to ground to regulate the DC/DC converter's output voltage. ADJ also supports a line drop compensation function.
5	MODE	**USB mode control.** Float MODE to operate the USB in DCP mode. Pull MODE low to operate the USB in CDP mode. MODE has a 1MΩ pull-up resistor to an internal +1.2V source.
6	GND	**Ground.**
7	IN	**Supply voltage.**
8	OUT	**Output of the USB current-limit switch.**
9	STATUS	**Open-drain output.** Pull STATUS low when the load current is higher than the typical 90mA threshold. STATUS is an open drain during no-load conditions.
10	EN	**Enable pin for the IC.** EN has an internal auto pull-up current to VCC. Float EN or apply a logic high voltage to EN to enable the IC. Pull EN to logic low to disable the IC.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +16V
Output voltage (V_{OUT}).....-0.3V to +16V
All other pins .....-0.3V to +6V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
..... 2.23W
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) 5V (4)
Output voltage (V_{OUT})..... Follow with V_{IN}
Output current (I_{OUT}).....Up to 3A
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-10 (1.5mmx2mm)			
EV5030D-QH-00A (5)	56	18	°C/W
JESD51-7 (6)	130	25	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on EV5030D-QH-00A, 2-layer PCB, 4.4cmx2.9cm, 2Oz copper.
3) The device is not guaranteed to function outside of its operating conditions.
4) For lower V_{IN} applications, refer to the Operation section on page 12.
5) Measured on EV5030D-QH-00A, 4.4cmx2.9cm, 2-layer PCB, 2Oz copper.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to 125°C [7], typical value tested at T_J = +25°C unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO1}	ADJ begins working	2.7	3	3.3	V
UVLO hysteresis	$V_{UVLOHYS1}$			880		mV
Second V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO2}	Power MOSFET turns on	3.7	3.9	4.1	V
Second UVLO hysteresis	$V_{UVLOHYS2}$			500		mV
EN rising threshold	V_{EN_R}		1.15	1.21	1.27	V
EN hysteresis	V_{EN_HYS}			200		mV
EN auto pull-up current	I_{EN_UP}		11	16	21	µA
Supply current	I_Q	V_{IN} = 5V, no load		250	320	µA
Shutdown current	I_{Q_STD}			40	60	µA
USB Power MOSFET						
On resistance	R_{DSON}	V_{IN} = 5V		32	50	mΩ
Input discharge resistance	R_{DIS}	Turn-on during V_{IN} OVP or high-to-low voltage change period		72		Ω
Soft-start time	T_{SS}	V_{IN} = 5V, no load, 10 - 90%		290		µs
Current Limit						
USB current limit	I_{LIMIT}	R_{ILIM} = 1.5kΩ, V_{IN} = 5V, V_{OUT} drops 10%, T_J = +25°C	3.13	3.35	3.57	A
	I_{LIMIT}	R_{ILIM} = 1.5kΩ, V_{IN} = 5V, V_{OUT} drops 10%, T_J = -40°C to +125°C	3	3.35	3.7	A
Load current detect rising	$I_{LOADDEC\_R}$	STATUS pulls low, T_J = +25°C	30	90	140	mA
Load current detect falling	$I_{LOADDEC\_F}$	STATUS open drain, T_J = +25°C	20	80	130	mA
STATUS						
STATUS pin leakage	I_{STATUS}	Pull up to 5V			1	µA
STATUS output	V_{STATUS}	Sink 1mA			250	mV
STATUS pull-low deglitch	T_{STATUS_LOW}		100	200	300	ms
Output Voltage Control						
Default V_{IN}	V_{IN_Def1}	I_{OUT} = 0A, T_J = +25°C	-1%	5.0	+1%	V
	V_{IN_Def2}	I_{OUT} = 0A, T_J = -40°C to +125°C	-2%	5.0	+2%	V
V_{ADJ} sink current capability	I_{sink}	V_{FB} = 800mV	500			µA
Line drop compensation	$V_{IN\_5\_C}$	I_{OUT} = 2.4A, only 5V_{IN} active		240	400	mV
Protection						
V_{IN} OVP threshold	V_{OV_TH}	V_{IN} rising edge, V_{IN} = 5V	110	115	120	%
V_{IN} OVP recovery threshold	$V_{OV\_Recovery}$	Reset mode to 5V default	5.25	5.4	5.55	V
OVP deglitch time [8]	T_{OVP_DE}			10		µs
OCP on time of hiccup	T_{HIC_ON}			2		ms
OCP off time of hiccup	T_{HIC_OFF}			2		s
Shutdown temperature [8]	T_{STD}			150		°C
Hysteresis [8]	T_{HYS}			25		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C [7], typical value tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
BC 1.2 DCP Mode						
DP/DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = +25°C			50	Ω
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$		1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM\_1.2V}$			300		kΩ
Divider Mode						
DP/DM output voltage	$V_{DP/DM}$	V_{IN} = V_{OUT} = 5V	2.5	2.7	2.85	V
DP/DM output impendence	$R_{DP/DM}$		18	22	28	kΩ
CDP Mode						
MODE pin logic low voltage	V_{MODE_L}	To enable CDP mode			0.5	V
DM CDP output voltage	V_{DM_SRC}	VDP = 0.6V	0.5	0.6	0.7	V
DP rising lower window threshold for V_{DM_SRC} activation	V_{DAT_RE}		0.3	0.35	0.4	V
DP rising lower window threshold hysteresis for V_{DM_SRC} activation	$V_{DAT\_RE\_HYS}$			50		mV
DP rising upper window threshold for V_{DM_SRC} de-activation	V_{LGC_SRC}		0.8	0.9	1	V
DP rising upper window threshold hysteresis for V_{DM_SRC} de-activation	$V_{LGC\_SRC\_HYS}$			50		mV
VDM_SRC on/off deglitch time	$V_{DM\_SRC\_Deglitch}$		3	5	7.5	ms
RDP down, RDM down	R_{DP/DM_Down}	Only enabled when V_{DP} > 0.35V/5µs	14.25	19.5	24.8	kΩ
DP, DM to ground leakage	I_{DP/DM_LKG}	V_{DM} = 1V, V_{DP} = 1V			1	µA

NOTES:

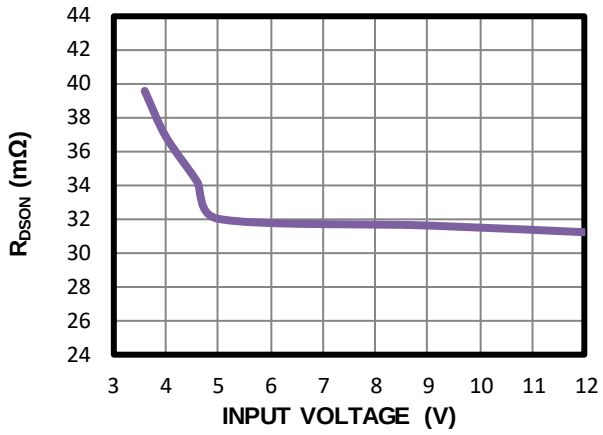
7) Not tested in production, guaranteed by over-temperature correlation.

8) Guaranteed by engineering sample characterization.

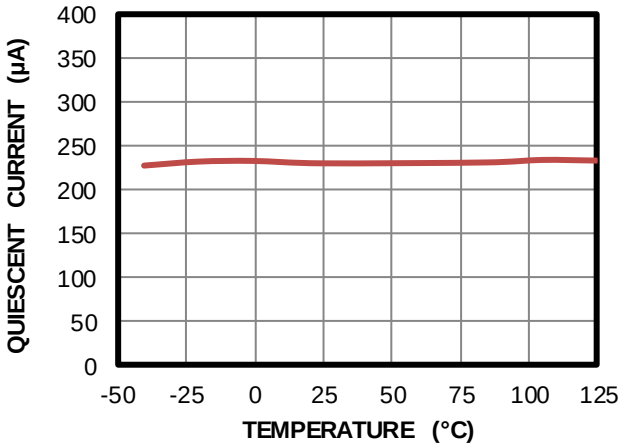
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted.

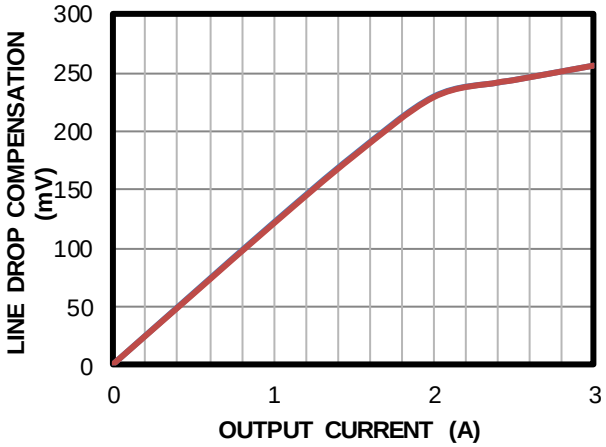
$R_{DS(ON)}$ vs. Input Voltage



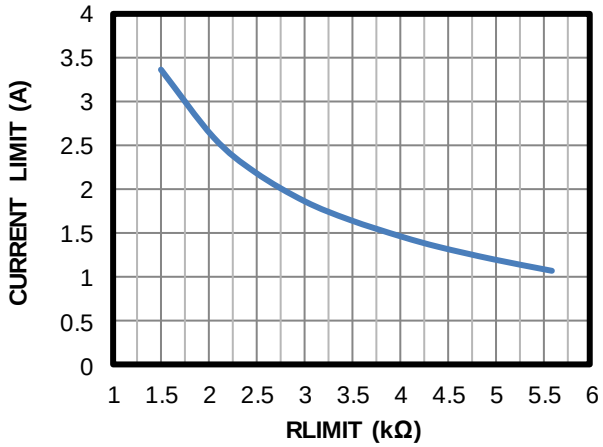
Quiescent Current vs. Temperature



Line Drop Compensation



Current Limit vs. R_{LIMIT}

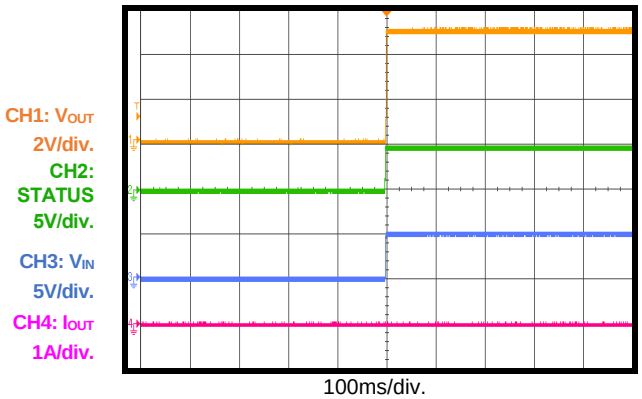


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted. Connect the MP5030D input to the MP2499A output, system V_{IN} = 12V is the MP2499A input voltage.

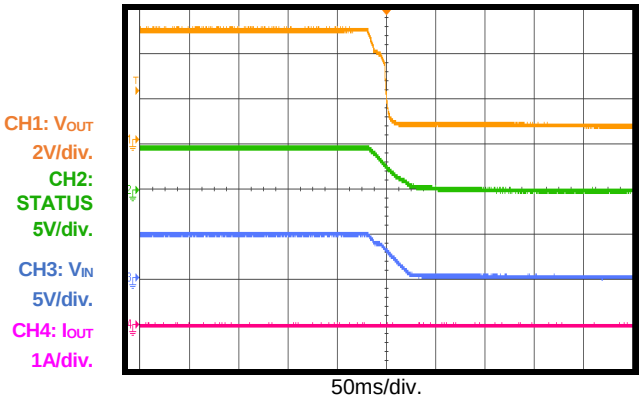
Start-Up through Input Voltage

I_{OUT} = 0A



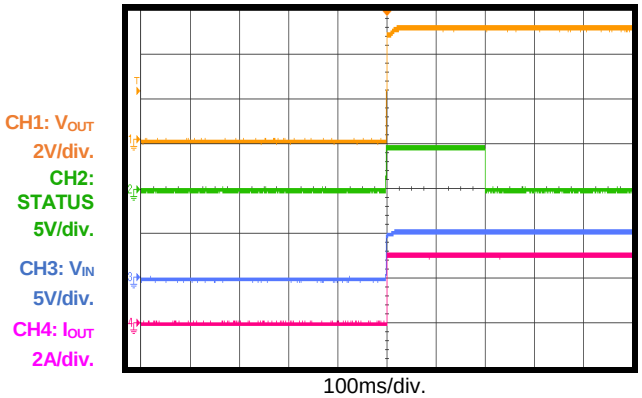
Shutdown through Input Voltage

I_{OUT} = 0A



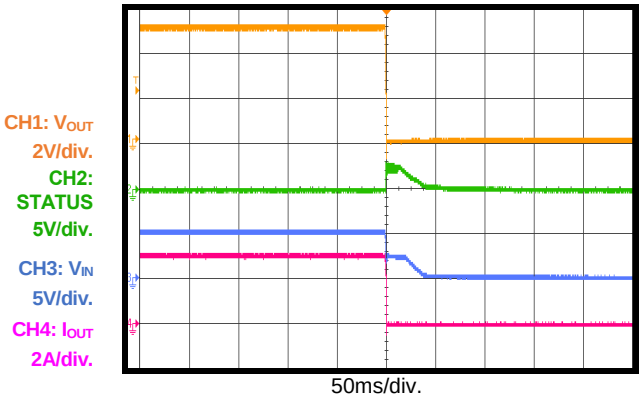
Start-Up through Input Voltage

I_{OUT} = 3A



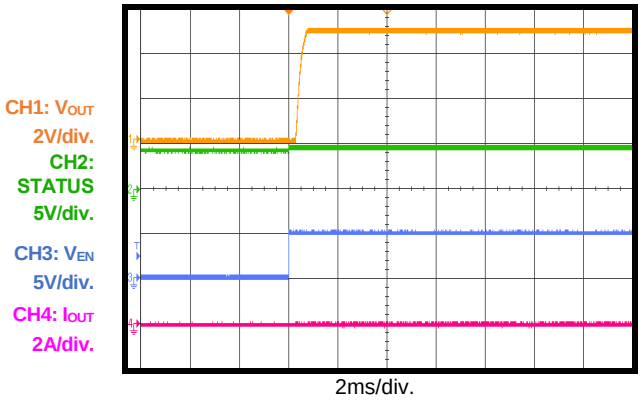
Shutdown through Input Voltage

I_{OUT} = 3A



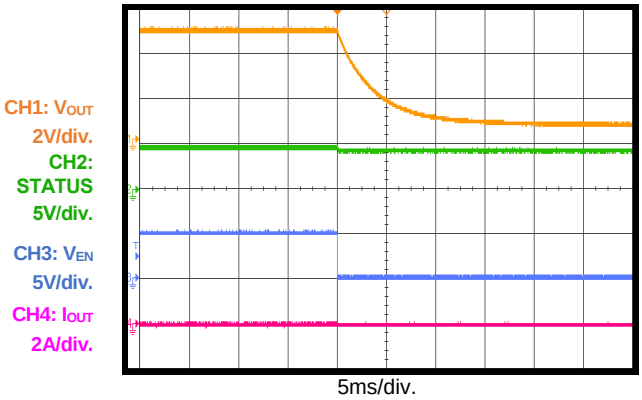
EN Start-Up

I_{OUT} = 0A



EN Shutdown

I_{OUT} = 0A

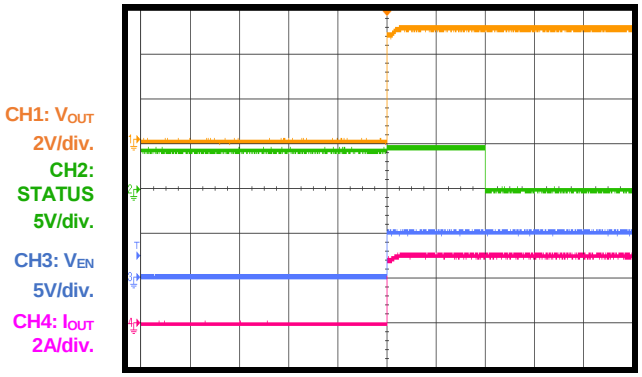


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted. Connect the MP5030D input to the MP2499A output, system V_{IN} = 12V is the MP2499A input voltage.

EN Start-Up

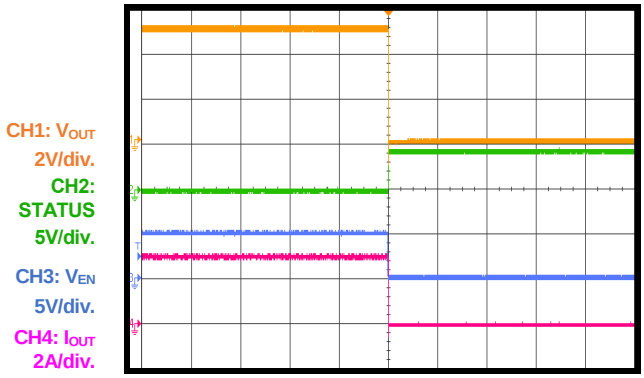
I_{OUT} = 3A



100ms/div.

EN Shutdown

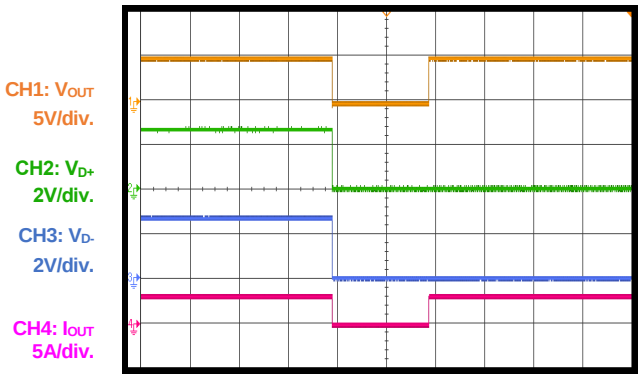
I_{OUT} = 3A



100ms/div.

MODE Changes from Float to GND

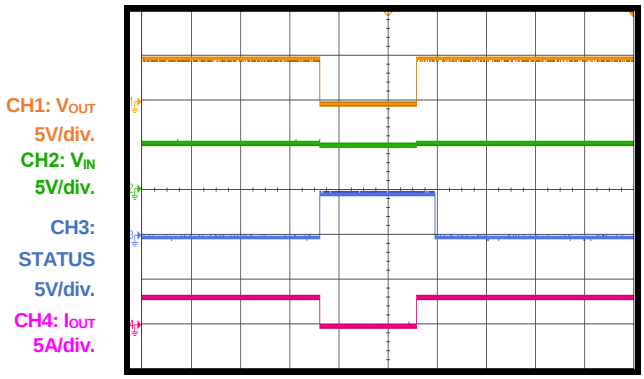
D+ and D- floating, I_{OUT} = 3A



500ms/div.

MODE Changes from Float to GND

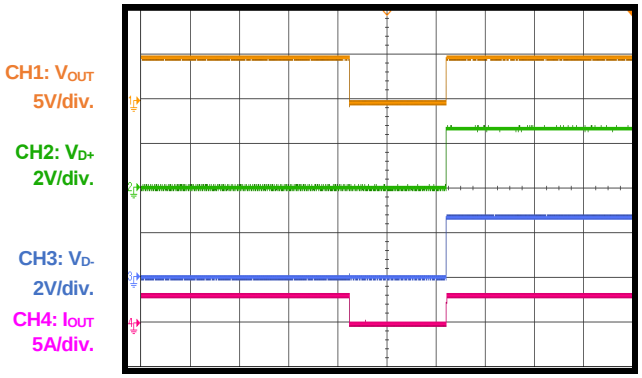
D+ and D- floating, I_{OUT} = 3A



500ms/div.

MODE Changes from GND to Float

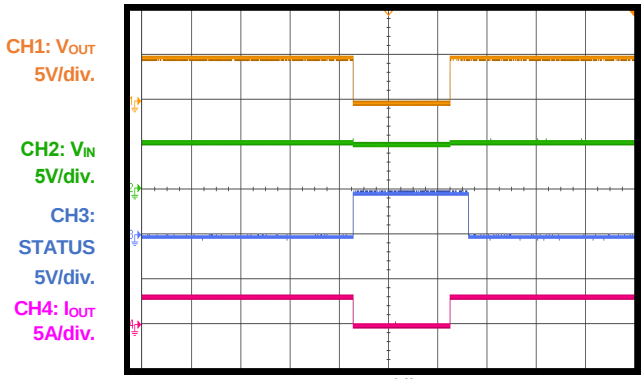
D+ and D- floating, I_{OUT} = 3A



500ms/div.

MODE Changes from GND to Float

D+ and D- floating, I_{OUT} = 3A



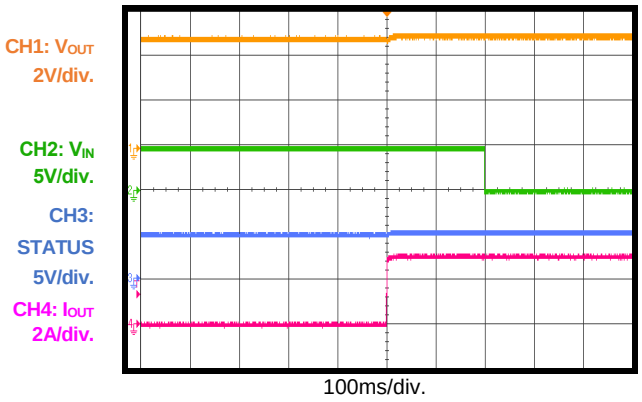
500ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted. Connect the MP5030D input to the MP2499A output, system V_{IN} = 12V is the MP2499A input voltage.

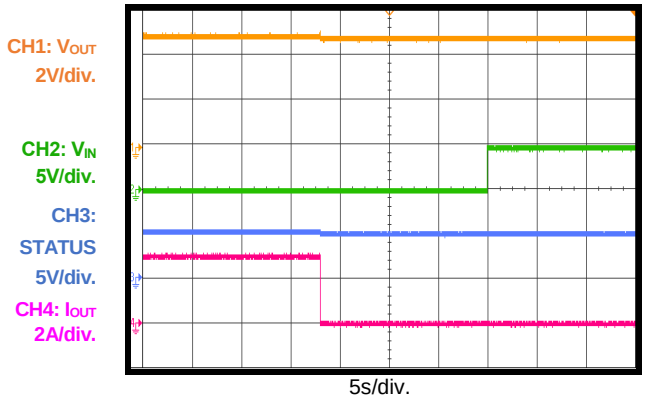
Status Function

I_{OUT} = 0 - 3A

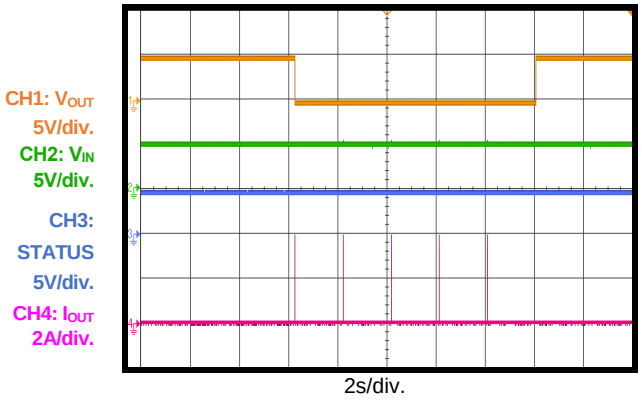


Status Function

I_{OUT} = 3 - 0A

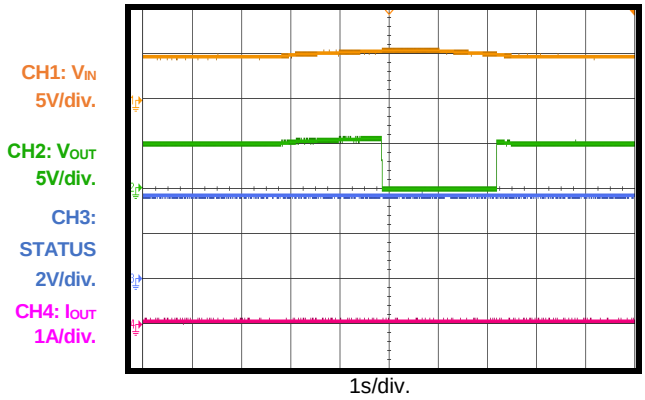


Short-Circuit Protection Entry and Recovery



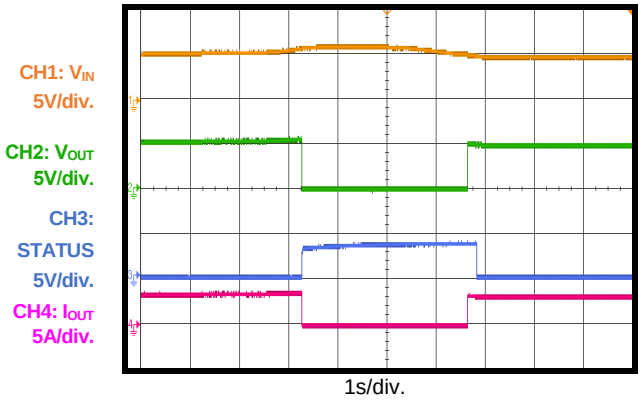
Input Over-Voltage Protection

I_{OUT} = 0A



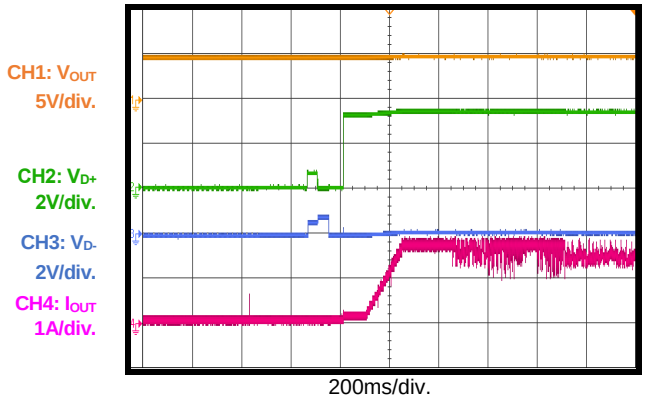
Input Over-Voltage Protection

I_{OUT} = 3A



CDP Mode Detection

Mobile Phone Plug-In

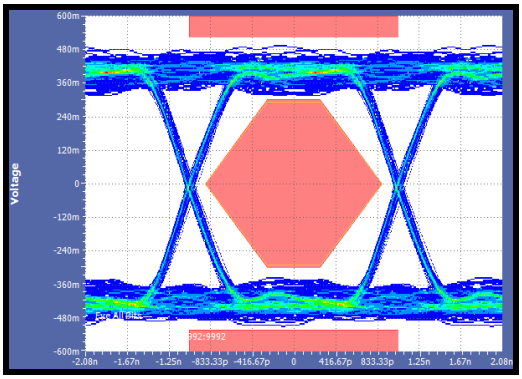


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, R_{ILIM} = 1.5kΩ, T_A = 25°C, unless otherwise noted. Connect the MP5030D input to the MP2499A output, system V_{IN} = 12V is the MP2499A input voltage.

Eye Pattern Test

Recommended CDP Mode Set-Up



BLOCK DIAGRAM

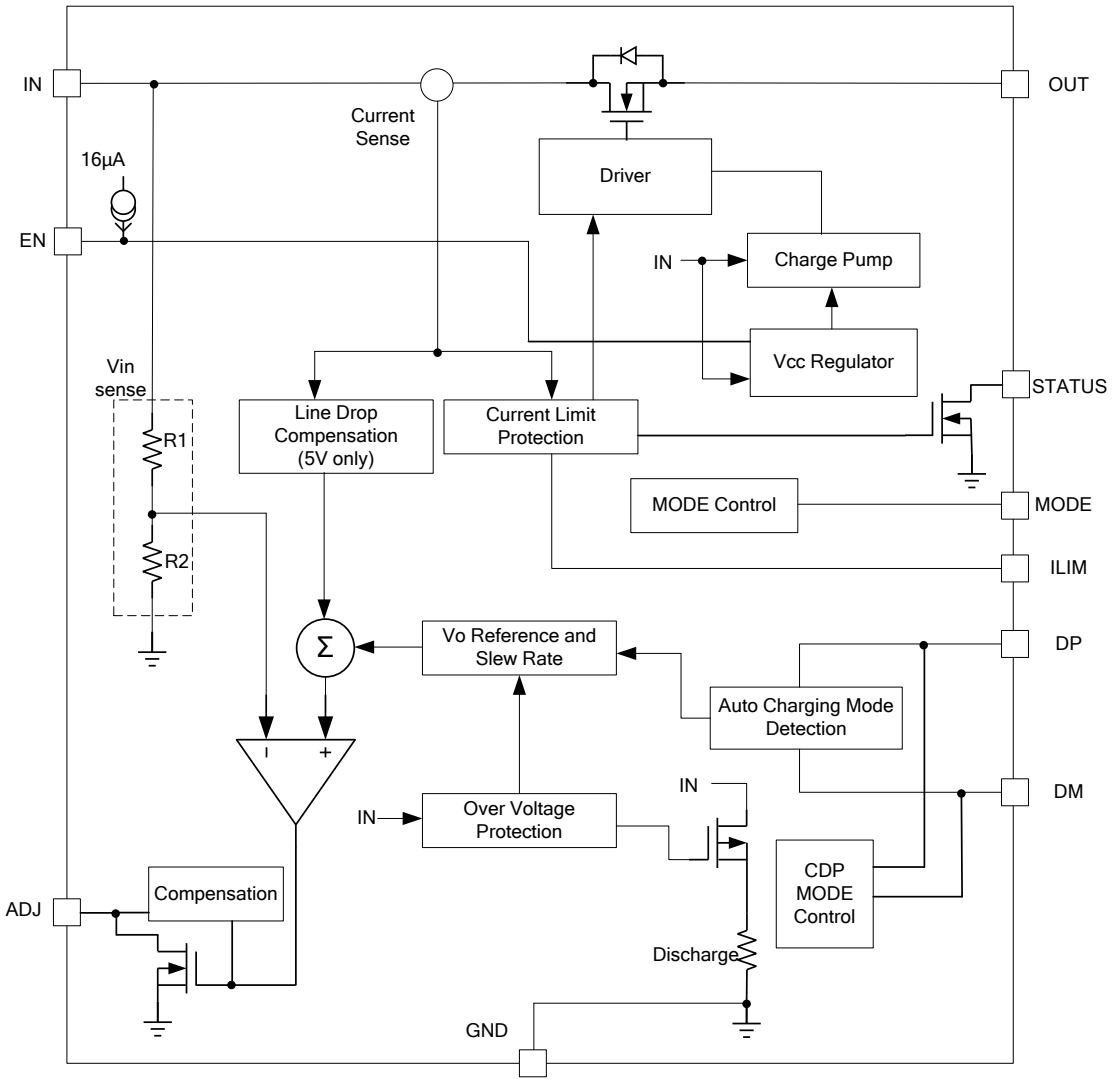


Figure 1: Functional Block Diagram

OPERATION

The MP5030D integrates a USB current-limit switch and charging port identification circuitry. The MP5030D achieves 3A of continuous output current over a wide input supply range.

The output of the USB switch is current-limited with an adjustable current-limit threshold. The MP5030D supports DCP and CDP schemes for battery charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for external user interaction.

The MP5030D provides line drop compensation, load current detection, and status indication. Full protection features include hiccup current limiting, input over-voltage protection (OVP), and thermal shutdown.

Operation Supply Voltage

The MP5030D has a two-stage input voltage threshold: the first threshold is around 3V, and the second threshold is the under-voltage lockout (UVLO) of the power MOSFET. When V_{IN} is higher than the first threshold, the MP5030D's ADJ block beings working. This sinks a current to adjust the upstream regulator's output to an accurate 5V. Afterward, the MP5030D enters a fully working state.

Under Voltage Lockout (UVLO)

UVLO protects the chip from operating at an insufficient supply voltage. The MP5030D's second UVLO comparator monitors the input voltage. Once the input voltage is higher than the second UVLO threshold, the power MOSFET starts to turn-on after a fixed delay with a controlled slew rate.

Internal Soft Start (SS)

The internal soft start prevents the output voltage from overshooting during start-up and prevents inrush current at the input.

MODE Selection

The MP5030D supports DCP and CDP mode through the MODE pin control. Pull MODE low to set the USB in CDP mode. Float MODE to set the USB in DCP mode (see Table 1).

The MP5030D supports dynamic changing USB charging modes. For example, when pulling MODE from floating to logic low, V_{BUS} turns off with an output discharge. Afterward, V_{BUS} restarts and enters CDP mode.

In DCP mode, the MP5030D can provide power for the USB devices with protocol auto-detection. The MP5030D supports the following charging schemes:

- USB battery charging specification BC1.2/Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode

In CDP mode, the MP5030D performs CDP handshaking with a portable device. The MP5030D follows the BC1.2 CDP handshaking specification.

V_{BUS} is always around 5V with current limit and line drop compensation.

Table 1: MODE Selection

MODE Pin Status	Supported Charge Mode
Float	DCP mode, divider mode, 1.2V/1.2V mode
Logic low	CDP mode

Line Drop Compensation

The MP5030D can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant 5V load-side voltage. Line drop compensation is achieved through ADJ. The MP5030D increases the input voltage by 240mV at an output of 2.4A (see Figure 2).

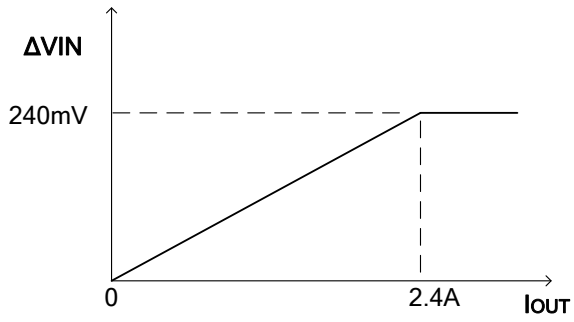


Figure 2: Line Drop Compensation

V_{ADJ} sinks a controlled current slowly. The line drop compensation amplitude linearly increases as the load current increases.

In no-load condition, if the input voltage is lower than 5V (typically), ADJ sinks a current to regulate the upstream regulator's output voltage to 5V. If the input voltage is higher than 5V (typically), MP5030D stops regulating the input voltage. For a quick load transient response, ADJ should always be working while the IC is on. Configure the R1/R2 default output voltage to be <5V. It is recommend to set the buck output as 4.9V, so R1 = 3.9kΩ and R2 = 0.75kΩ.

Figure 3 shows the typical ADJ usage. The ADJ sink current capability is 500μA. ADJ requires the feedback current through R1 to be less than 500μA. Calculate R1 with Equation (1):

$$R1(k\Omega) > \frac{\Delta V(V)}{0.5} \quad (1)$$

Where ΔV is the maximum line drop compensation value. To this, add the differential voltage between 5V and the voltage buck set.

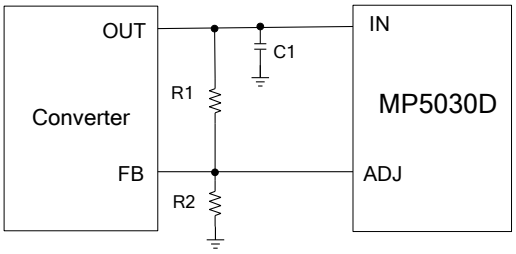


Figure 3: ADJ Configure

Input Over-Voltage and Discharge

To protect the downstream device from an over-voltage condition, the MP5030D provides an input over-voltage protection (OVP) shutdown function.

An accurate and fast comparator monitors the over-voltage condition of the input. If the input voltage rises above the threshold, the gate of the internal MOSFET is pulled low quickly and the power MOSFET is shut down. The input-to-ground discharge path is active at this time. When the input voltage falls below 5.4V (typically), the MP5030D exits OVP mode.

Over-Current Protection (OCP)

The MP5030D provides a constant current limit. The current-limit threshold is adjustable via an external resistor.

Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to keep the power MOSFET current constant.

For the current limit setting, refer to the Current Limit vs. R_{Limit} curve on page 6. If the set current limit is less than 500mA, the current limit accuracy worsens slightly. An external R_{Limit} resistor can set the current limit threshold. If an over-current (OC) condition occurs but V_{OUT} > 3.5V, the MP5030D works in constant-current (CC) limit mode without hiccup. If OCP is triggered and V_{OUT} < 3.5V for 2ms, the MP5030D enters hiccup mode. In hiccup mode, the MP5030D turns off the power MOSFET (see Figure 4).

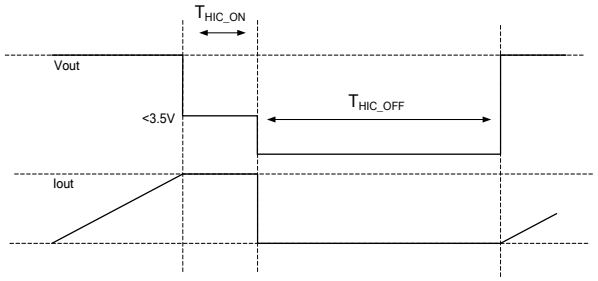


Figure 4: Over-Current Protection

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may greatly exceed the current-limit threshold before the control loop can respond. If the current reaches the internal secondary current-limit level (about 6A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. The fast-off response time value is 700ns, typically. If the fast-off works, the power MOSFET remains off for 80μs. Afterward, the power MOSFET turns on again if the part is still in a short-circuit condition. The MP5030D treats this as an over-current condition again to enter hiccup or thermal shutdown. After the short-circuit condition is removed, the MP5030D recovers automatically.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 125°C), the chip is enabled again.

Load Current Detection and Status Indication

STATUS is an open-drain output. When the load current is larger than 90mA (typically) for longer than 200ms, STATUS is pulled low by a <100Ω resistor. When the load current is smaller than 80mA (typically) for longer than 15s, STATUS becomes an open-drain output.

During the first power-up, STATUS is an open-drain output.

During the MODE transition, V_{BUS} restarts with a fixed delay time, and STATUS resets to an open-drain output.

If a fault condition occurs (OTP, OCP, SCP, OVP), STATUS resets to an open-drain output.

APPLICATION INFORMATION

Selecting the Input Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications. When selecting an input capacitor, be sure to consider the pre-stage converter stability as well. The input capacitor of the MP5030D will be the output capacitor of the converter. Ensure that the converter is stable with additional output capacitors.

Selecting the Output Capacitor

Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22µF ceramic capacitor is recommended for most applications.

Selecting the ILIM Resistor

The current-limit value can be set by the ILIM resistor. For the programmable current limit, refer to the Current Limit vs. R_{Limit} curve on page 6.

The current-limit threshold is recommended to be 10% higher than the maximum load current. For example, if the system's full load is 3A, set the current limit to 3.3A.

Selecting the V_{ADJ} Resistor

ADJ has an internal, controlled current sink. Line drop compensation is achieved through ADJ. The ADJ sink current capability is 500µA. The pre-side converter should be a kΩ level feedback resistor. The current through the high-side feedback resistor should be less than 500µA (see Figure 5).

There is another V_{ADJ} configuration to limit the maximum output voltage by inserting R3 between FB and V_{ADJ}. With R3, the maximum output voltage can be limited by Equation (2):

$$V_{OUT\_MAX}(V) = \frac{R_1 + R_2 // R_3}{R_2 // R_3} \times V_{FB}(V) \quad (2)$$

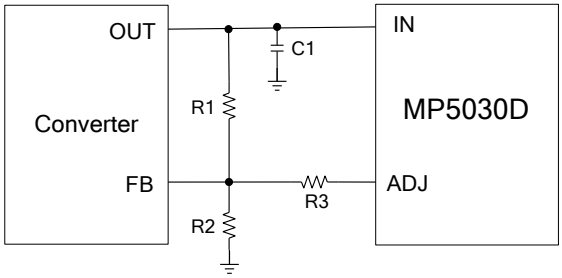


Figure 5: V_{ADJ}-Set Maximum V_{OUT}

Other Considerations

The upstream DC/DC converter should have a higher current-limit threshold than the MP5030D's current limit.

PCB Layout Guidelines [9]

Efficient PCB layout is critical for stable operation and thermal dissipation. For the best results, refer to Figure 6 and follow the guidelines below.

1. Use short, direct and wide traces to connect the IC's IN and OUT pins.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place a ceramic input decoupling capacitor as close to the IN and GND pins as possible to improve EMI performance.
5. Keep the V_{ADJ} trace to the pre-side converter FB pin as short as possible to avoid noise injection.

NOTE:

9) The recommended layout is based on the Typical Application Circuit shown in Figure 7.

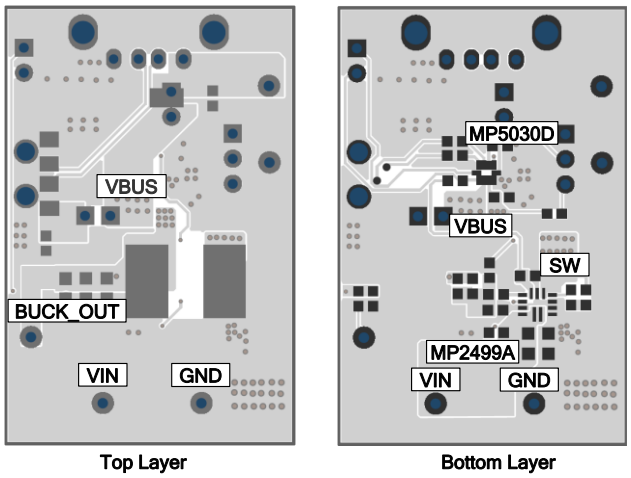


Figure 6: Recommended Layout

TYPICAL APPLICATION CIRCUITS

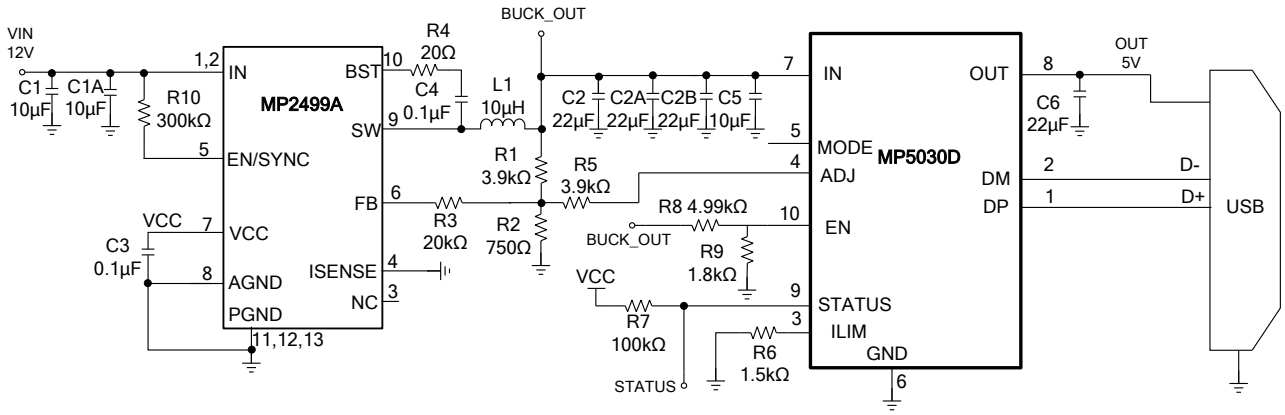


Figure 7: MP5030D + MP2499A for CLA Car Charger, DCP Mode (10)

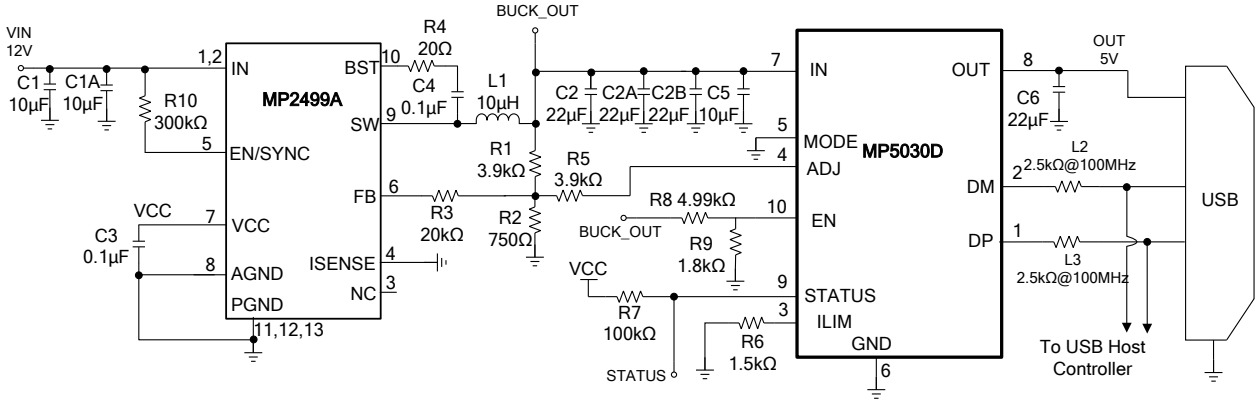


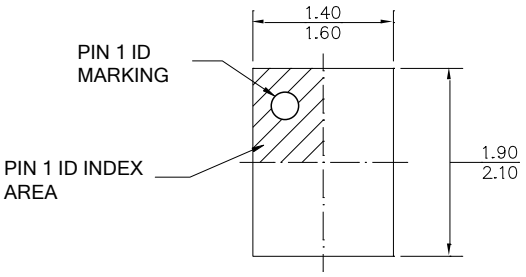
Figure 8: MP5030D + MP2499A for CDP Mode (10)

NOTE:

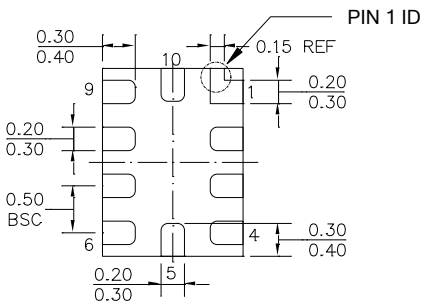
10) Pull STATUS up to the MP2499A's VCC pin through a 10 - 100kΩ resistor.

PACKAGE INFORMATION

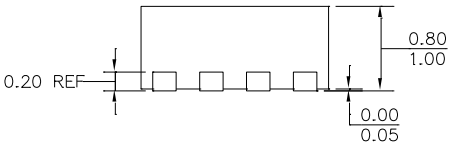
QFN-10 (1.5mmx2mm)



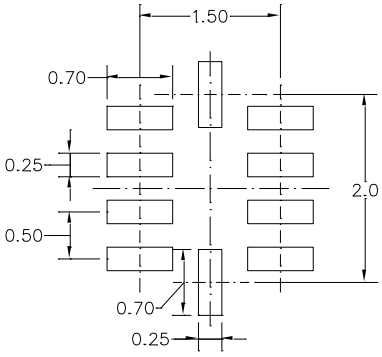
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.