MP5408M

36V, 6A, Frequency Programmable, Step-Down Converter with Smart, Dual, USB Charging Ports

The Future of Analog IC Technology

DESCRIPTION

The MP5408M integrates a monolithic, step-down, switch-mode converter with two USB current-limit switches and charging port identification circuitry for each port. The MP5408M achieves 6A of output current with excellent load and line regulation over a wide input-supply range.

The output of the USB switch is current-limited. Both USB ports support DCP schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode and USB Type-C 5V@3A DFP mode, eliminating the need for outside user interaction.

Full protection features include hiccup current limiting, output over-voltage protection (OVP), and thermal shutdown.

The MP5408M requires a minimal number of readily available, standard, external components and is available in a QFN-26 (5mmx5mm) package.

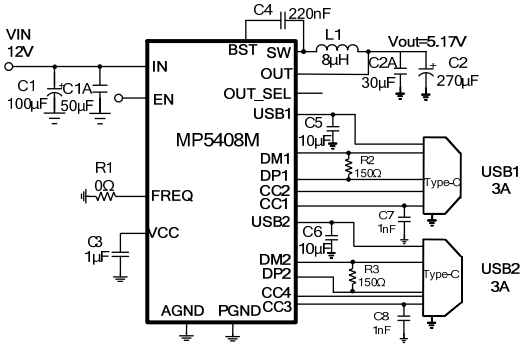
FEATURES

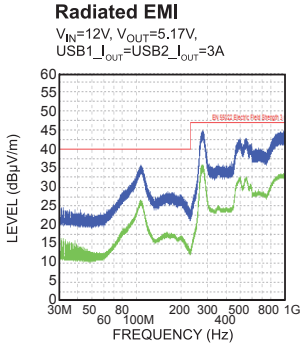
- EMI Reduction Technique
- Wide 6V to 36V Operating Input Voltage Range
- Selectable Output Voltage: 5.1V, 5.17V, and 5.3V
- 90mV Line Drop Compensation
- Accurate USB1/USB2 Output Current Limit
- 18mΩ/15mΩ Low $R_{DS(ON)}$ Internal Buck Power MOSFETs
- 13mΩ/13mΩ Low $R_{DS(ON)}$ Internal USB1/USB2 Power MOSFETs
- Frequency Adjustable (235kHz to 2.2MHz)
- Forced Continuous Conduction Mode (CCM) Operation
- Hiccup Current Limit for both Buck and USB
- Supports DCP Schemes for BC1.2, Divider Mode, and 1.2V/1.2V Mode
- Supports USB Type-C 5V @ 3A DFP Mode
- ±8kV HBM ESD Rating for USB, DP, and DM pins
- Available in a QFN-26 (5mmx5mm) Package

APPLICATIONS

- USB Dedicated Charging Ports (DCP)
- USB Type-C 5V @ 3A DFP
- Automotive Cigarette Lighter Adapters
- Power Supply for Linear Chargers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5408MGU	QFN-26 (5mmx5mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5408MGU–Z)

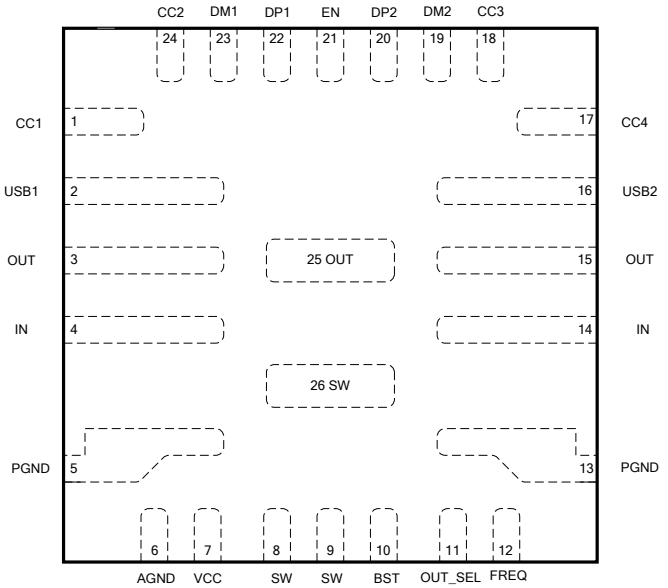
TOP MARKING

MPSYYWW
MP5408M
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5408M: Product code of MP5408MGU
LLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-26 (5mmx5mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 40V
V_{SW} ..... -0.3V (-5V for <10ns) to V_{IN} + 0.3V (43V for <10ns)
V_{BST} ..... V_{SW} + 5.5V
V_{EN} ..... -0.3V to +10V (2)
V_{OUT}, V_{USB} ..... -0.3V to +6.5V
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = +25°C) (3)
QFN-26 (5mmx5mm) 6.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Operation input voltage range ..... 6V to 36V
Output current 3A (USB1), 3A (USB2)
Operating junction temp. (T_J) ... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-26 (5mmx5mm)			
JESD51-7 (5)	44	9	°C/W
50mmx50mm 4-Layer PCB	20	2	°C/W

NOTES:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) For details on EN's ABS max rating, please refer to the EN Control section on page 11.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on 4 layers PCB (50mmx50mm).
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7 and 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, CC1 = CC3 = 5.1kΩ, T_J = -40°C to +125°C (6), typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		13	18	μA
Supply current (quiescent)	I_{Q1}	No switching		1	2	mA
	I_{Q2}	CC floating, V_{BUS} disabled, T_J = +25°C		200	300	μA
EN rising threshold	$V_{EN\ Rising}$		-3%	1.235	+3%	V
EN hysteresis	$V_{EN\ HYS}$			200		mV
EN pull-up current	I_{EN}		4	8	12	μA
Thermal shutdown (7)	T_{TSD}			165		°C
Thermal hysteresis (7)	T_{TSD_HYS}			20		°C
VCC regulator	V_{CC}		4.2	4.5	4.85	V
VCC load regulation	$V_{CC\ LOG}$	I_{CC} = 50mA		1	3	%
Step-Down Converter						
V_{IN} under-voltage lockout threshold rising	V_{IN_UVLO}		4.6	5	5.4	V
V_{IN} under-voltage lockout threshold hysteresis	V_{UVLO_HYS}			700		mV
HS switch on resistance	$R_{DSON\ HS}$			18		mΩ
LS switch on resistance	$R_{DSON\ LS}$			15		mΩ
Output voltage	V_{OUT}	OUT_SEL = low, T_J = +25°C	-1.5%	5.1	+1.5%	V
		OUT_SEL = float, T_J = +25°C	-1%	5.17	+1%	
		OUT_SEL = float, T_J = -40°C to +125°C	-2%	5.17	+2%	
		OUT_SEL = high, T_J = +25°C	-1.5%	5.3	+1.5%	
Output over-voltage protection	V_{OVP_R}		5.45	5.85	6.25	V
Output OVP recovery	$V_{OVP\ F}$		5.3	5.7	6.1	V
Output to ground resistance	$R_{Discharge}$			175		kΩ
Low-side current limit	$I_{LS\ LIMIT}$			-2		A
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = +25°C			1	μA
		V_{EN} = 0V, V_{SW} = 36V or 0V, T_J = -40°C to +125°C			5	
High-side current limit	I_{LIMIT}	40% duty cycle	9	13		A
Oscillator frequency	F_{SW1}	Pull R_{FREQ} to GND		235		kHz
	F_{SW2}	R_{FREQ} = 66.5kΩ		350		
	F_{SW3}	R_{FREQ} = 9.53kΩ		2200		
	F_{SW4}	R_{FREQ} = float	350	450	530	
Maximum duty cycle	D_{MAX}	FREQ = 450kHz		95		%

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 = CC3 = 5.1kΩ, T_J = -40°C to +125°C [6], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum off time	T_{OFF_MIN}			110		ns
Minimum on time [7]	T_{ON_MIN}			130		ns
Soft-start time	T_{SS}	Output from 10% to 90%, T_J = +25°C		2		ms
USB Switch (USB1 and USB2)						
Under-voltage lockout threshold rising	V_{USB_UVR}		3.7	4	4.3	V
Under-voltage lockout threshold hysteresis	V_{USB_UVHYS}			200		mV
Switch on resistance	R_{DSON_SW}			13		mΩ
Output discharge resistance	R_{DIS_USB}	Apply 5V voltage on USB output, CC pin float		500		kΩ
USB OVP clamp	V_{USB_OV}		5.3	5.6	5.9	V
Current limit	I_{Limit1}	V_{OUT} drops 10% , Type-C mode	3.1	3.45	3.8	A
	I_{Limit2}	T_J = +25°C , V_{OUT} drops 10%, Type-A mode	2.6	2.75	2.9	
Line drop compensation	V_{DROP_COM}	Iout=2.4A , V_{OUT} = 5V, T_J = +25°C		90		mV
V_{BUS} soft-start time	T_{SS}	Output from 10% to 90%	1	2	3	ms
Hiccup mode on time	T_{HICP_ON2}	OC, V_{OUT} drops 10%, T_J = +25°C	3.5	5	6.5	ms
		OC, V_{OUT} drops 10%, T_J = -40°C to +125°C	3	5	7	
Hiccup mode off time	T_{HICP_OFF}	V_{OUT} connected to GND		2		s
BC1.2 DCP Mode						
DP and DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA, T_J = +25°C		85	155	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, T_J = -40°C to +125°C		85	160	
Divider Mode						
DP/DM output voltage	$V_{DP/DM\_Divider}$		2.55	2.7	2.85	V
DP/DM output impedance	$R_{DP/DM\_Divider}$	T_J = +25°C	14	22	30	kΩ
		T_J = -40°C to +125°C	12	22	34	
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$	V_{OUT} = 5V, T_J = +25°C	1.12	1.2	1.28	V
		V_{OUT} = 5V, T_J = -40°C to +125°C	1.1	1.2	1.3	
DP/DM output impedance	$R_{DP/DM\_1.2V}$	T_J = +25°C	70	105	140	kΩ
		T_J = -40°C to +125°C	60	105	150	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, CC1 = CC3 = 5.1kΩ, T_J = -40°C to +125°C [6], typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
USB Type-C 5V @ 3A Mode – CC1, CC2, CC3, and CC4						
CC resistor to disable Type-C mode	R_A	CC1 and CC3	70		90	kΩ
CC voltage to enable V_{CONN}	V_{Ra}				0.75	V
CC voltage to enable V_{BUS}	V_{Rd}		0.9		2.45	V
CC detach threshold	V_{Detach}		2.75			
CC voltage falling debounce timer	$T_{CC\_debounce}$	V_{BUS} enable deglitch	100	144	200	ms
CC voltage rising debounce timer	$T_{PD\_debounce}$	V_{BUS} disable deglitch	10	15	20	ms
V_{CONN} output power	P_{VCONN}	V_{CONN} comes from the buck output with some series resistance, T_J = +25°C	1			W

NOTES:

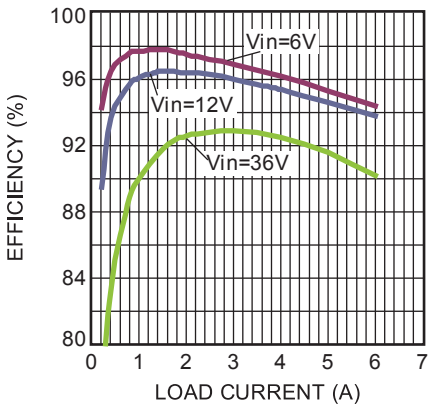
6) All min/max parameters are tested at T_J = 25°C. Limits over temperature are guaranteed by design, characterization, and correlation.

7) Guaranteed by design and characterization test.

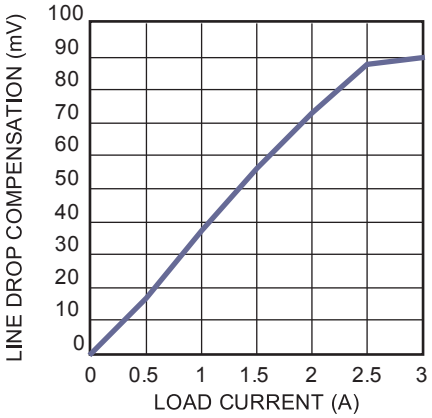
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 5.17V, L = 8µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Load Current

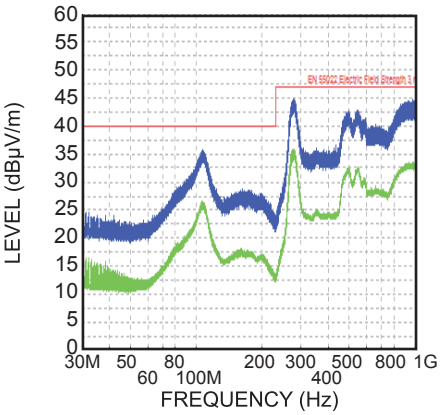


Line Drop Compensation vs. Load Current



Radiated EMI

V_{IN}=12V,V_{OUT}=5.17V,
USB1_I_{OUT}=USB2_I_{OUT}=3A

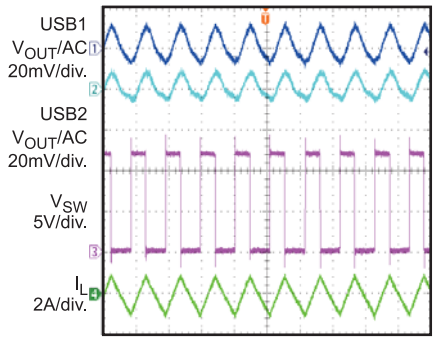


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5.17V, L = 8µH, T_A = 25°C, unless otherwise noted.

Output Ripple

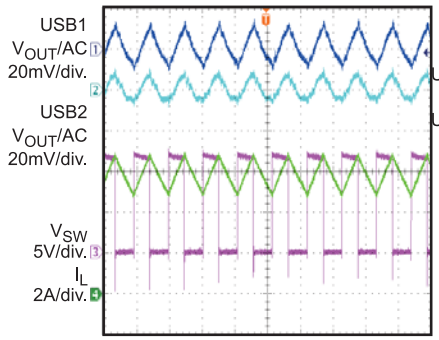
V_{IN}=12V, V_{OUT}=5.17V,
USB1_I_{OUT}=USB2_I_{OUT}=0A



4µs/div.

Output Ripple

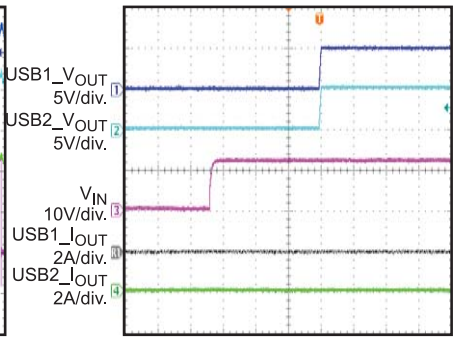
V_{IN}=12V, V_{OUT}=5.17V,
USB1_I_{OUT}=USB2_I_{OUT}=3A



4µs/div.

Power Start-Up

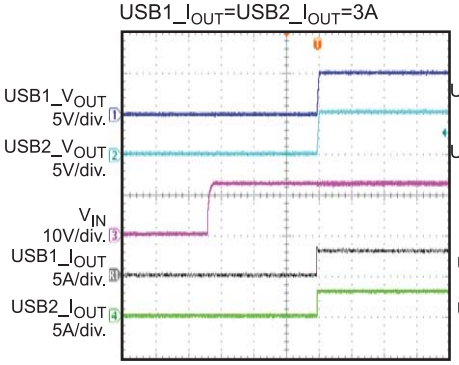
V_{IN}=12V, V_{OUT}=5.17V,
USB1_I_{OUT}=USB2_I_{OUT}=0A



40ms/div.

Power Start-Up

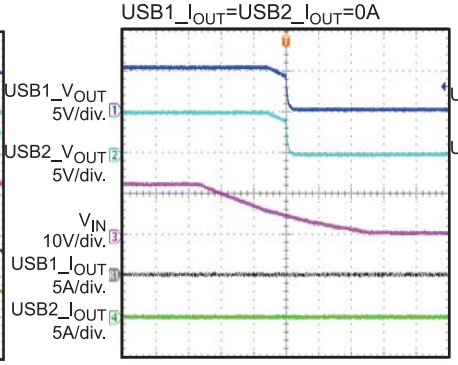
V_{IN}=12V, V_{OUT}=5.17V,
USB1_I_{OUT}=USB2_I_{OUT}=3A



40ms/div

Power Shutdown

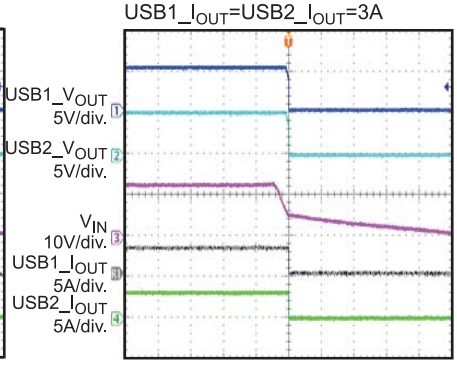
V_{IN}=12V, V_{OUT}=5.17V,
USB1_I_{OUT}=USB2_I_{OUT}=0A



20ms/div

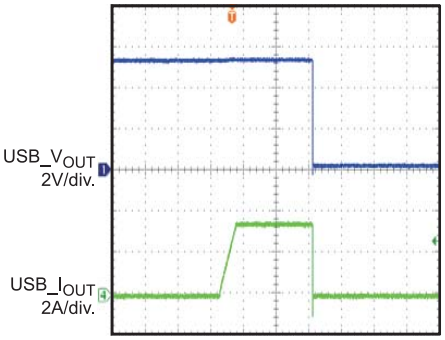
Power Shutdown

V_{IN}=12V, V_{OUT}=5.17V,
USB1_I_{OUT}=USB2_I_{OUT}=3A



10ms/div

USB Over-Current Protection



2ms/div

PIN FUNCTIONS

QFN 5x5 Pin #	Name	Description
1	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the V_{CONN} pin of the plug.
2	USB1	**USB1 output.**
3, 15, 25	OUT	**Buck output.** OUT is the power input for USB1 and USB2.
4, 14	IN	**Supply voltage.** IN is the drain of the internal power device and provides power to the entire chip. The MP5408M operates from a 6V to 36V input voltage. The input capacitor (C_{IN}) prevents large voltage spikes at the input. Place C_{IN} as close to the IC as possible.
5, 13	PGND	**Power ground.** PGND is the reference ground of the regulated output voltage. PGND requires extra care during the PCB layout. Connect PGND with copper traces and vias.
6	AGND	**Analog ground.** Connect AGND to PGND.
7	VCC	**Internal 4.5V LDO regulator output.** Decouple VCC with a 1µF capacitor.
8, 9, 26	SW	**Switch output.** Use a wide PCB trace to make the connection.
10	BST	**Bootstrap.** A 0.22µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver.
11	OUT_SEL	**Buck output voltage set.** By setting OUT_SEL to low, float, or high, three different output voltages can be achieved: 5.1V, 5.17V, or 5.3V.
12	FREQ	**Switching frequency program input.** Connect a resistor from FREQ to GND to set the switching frequency. Float FREQ or connect FREQ to VCC for the default 450kHz frequency. Connect FREQ to ground for a 235kHz internal frequency.
16	USB2	**USB2 output.**
17	CC4	**Configuration channel.** CC4 is used to detect connections and configure the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power over the V_{CONN} pin of the plug.
18	CC3	**Configuration channel.** CC3 is used to detect connections and configure the interface across the USB2 Type-C cables and connectors. Once a connection is established, CC3 or CC4 is reassigned to provide power over the V_{CONN} pin of the plug.
19	DM2	**D- data line to USB2 connector.** DM2 is the input/output used for handshaking with portable devices.
20	DP2	**D+ data line to USB2 connector.** DP2 is the input/output used for handshaking with portable devices.
21	EN	**On/off control input.** EN has an internal auto pull-up with a 8µA current source.
22	DP1	**D+ data line to USB1 connector.** DP1 is the input/output used for handshaking with portable devices.
23	DM1	**D- data line to USB1 connector.** DM1 is the input/output used for handshaking with portable devices.
24	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB1 Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the V_{CONN} pin of the plug.

BLOCK DIAGRAM

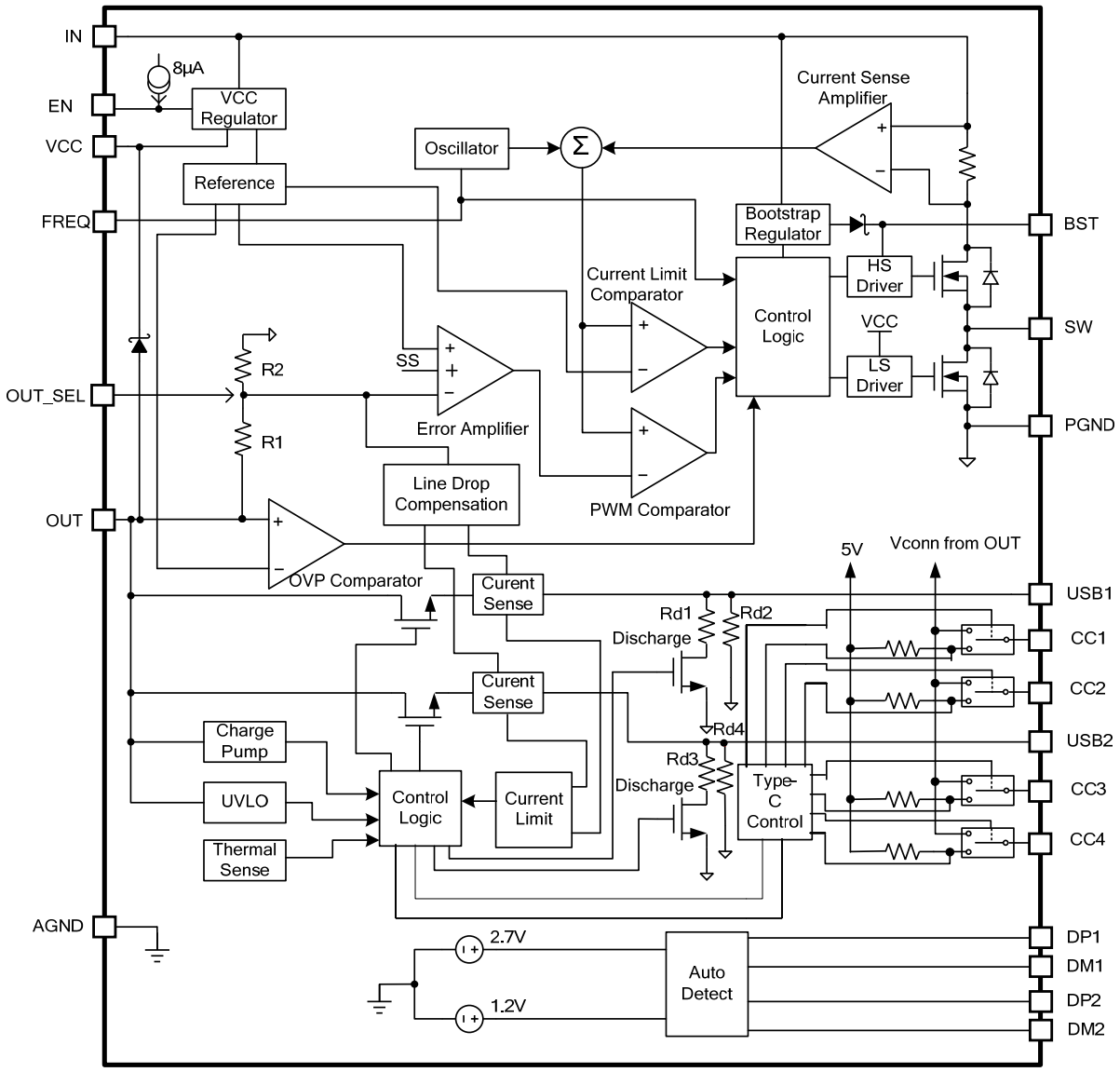


Figure 1: Functional Block Diagram

OPERATION

BUCK CONVERTER SECTION

The MP5408M integrates a monolithic, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs and two USB current-limit switches with charging-port auto-detection. The MP5408M offers a compact solution that achieves 6A of continuous output current with excellent load and line regulation over a wide input supply range.

The MP5408M operates in a fixed-frequency, peak-current-mode control to regulate the output voltage. The internal clock initiates the pulse-width modulation (PWM) cycle, which turns on the integrated high-side power MOSFET (HS-FET). The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the power switch is off, it remains off until the next clock cycle begins. If the duty cycle reaches 95% (450kHz switching frequency) in one PWM period, the current in the power MOSFET does not reach the COMP-set current value, and the power MOSFET turns off.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal reference (REF) and outputs V_{COMP}. V_{COMP} controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Internal VCC Regulator

The 4.5V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.5V, the output of the regulator is in full regulation. If V_{IN} is less than 4.5V, the output decreases with V_{IN}. VCC requires an external 1µF ceramic decoupling capacitor.

After the buck output starts up, the internal VCC LDO output is biased by the buck output through a Schottky diode.

Enable (EN) Control

The MP5408M has an enable (EN) control pin. An internal 8µA pull-up current allows EN to be floated for automatic start-up. Pull EN high or float EN to enable the IC. Pull EN low to disable the IC.

EN is clamped internally using a 7.6V series Zener diode and a 10V break-down voltage of the ESD cell (see Figure 2).

Connect EN through a pull-up resistor to V_{IN} to enhance the EN pull-up current ability. This requires limiting the EN voltage below 10V or limiting EN input current below 500µA if the EN pull-up voltage is larger than 10V.

For example, if connecting EN to V_{IN} = 36V, then R_{PULLUP} ≥ (36V - 10V) / 500µA = 52kΩ.

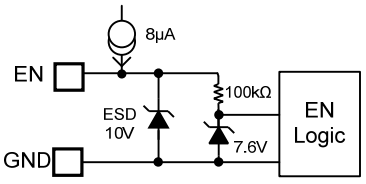


Figure 2: Zener Diode between EN and GND

Setting the Switching Frequency

Connect a resistor from FREQ to ground to set the switching frequency (see Table 1). The value of the frequency can be calculated approximately with Equation (1):

$$FREQ(kHz) = \frac{1000000}{42.5 \times R_{FREQ}(K\Omega) + 53.7} \quad (1)$$

The frequency vs. R_{FREQ} is shown in Figure 3.

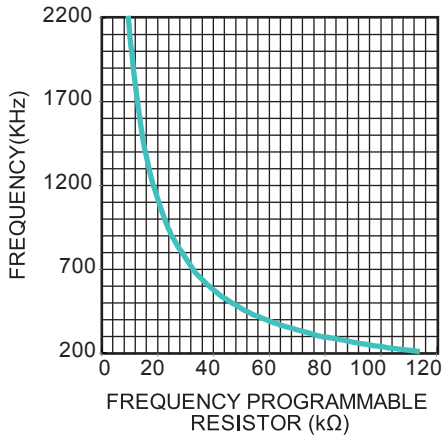


Figure 3: Switching Frequency vs. R_{FREQ}

Table 1: Recommended Resistor Values for Typical Switching Frequency

R_{FREQ} (kΩ)	F_S (kHz)
0	235
66.5	350
NS	450
45.8	500
22.3	1000
14.6	1500
9.53	2200

Two internal comparators monitor FREQ's logic voltage to enable FREQ to float or short to GND. During power-up, there is another internal source current on FREQ. The frequency is locked at 450kHz when a voltage greater than 2V and a current greater than 8μs is sensed on FREQ. The frequency is locked at 235kHz when a voltage less than 0.1V and a current greater than 8μs is sensed on FREQ. Leave FREQ floating or connect FREQ to VCC to achieve the 450kHz default switching frequency. Short FREQ to ground to achieve a 235kHz frequency (see Figure 4).

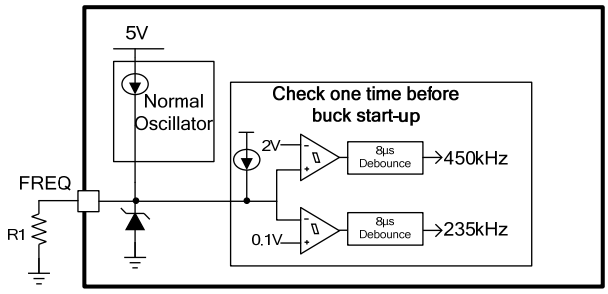


Figure 4: Switching Frequency Functional Block

Electromagnetic Interference (EMI)

Based on MPS's flip-chip package technology, the MP5408M integrates two sets of EMI filters to reduce the input path's parasitic inductance dramatically. Simultaneously, the input pin and GND pin are assigned on two sides symmetrically, partially cancelling the magnetic field inside those two filters (see Figure 5). The magnetic field in the overlap area (A1) is partially cancelled.

Using the above technique, the radiated emission performance is improved greatly.

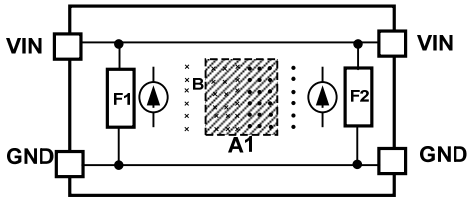


Figure 5: EMI Reduction

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input voltage. The UVLO rising threshold is 5V, and its falling threshold is 4.3V.

Internal Soft Start (SS)

Soft start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference. The SS time is set to 2ms internally. If the output of the MP5408M is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Forced CCM Operation

The MP5408M works in forced continuous conduction mode (CCM) continuously. The MP5408M operates in a fixed switching frequency regardless of whether it is operating in light load or full load. The advantage of CCM is the controllable frequency, smaller output ripple, and sufficient bootstrap charge time, but it also has low efficiency at light-load condition. A proper inductance should be selected to avoid triggering the low-side switch's negative current limit (typically 2A, from SW to GND). If the negative current limit is triggered, the low-side switch turns off, and the high-side switch turns on when the internal clock comes around.

Buck Over-Current Protection (OCP)

The MP5408M has a cycle-by-cycle over-current limit when the inductor peak current exceeds the current-limit threshold, and the FB voltage drops below the under-voltage (UV)

threshold (typically 50% below the reference). Once UV is triggered, the MP5408M enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead-shorted to ground. This reduces the average short-circuit current greatly, alleviates thermal issues, and protects the regulator. The MP5408M exits hiccup mode once the over-current condition is removed.

Buck Output Over-Voltage Protection (OVP)

The MP5408M has output over-voltage protection (OVP). If the output is higher than 5.85V, the high-side switch stops turning on. The low-side switch turns on to discharge the output voltage until the output decreases to 5.7V, and then the chip resumes normal operation.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by VIN and VCC through D1, D2, M1, C4, L1 and C2 (see Figure 5). BST capacitor C4 voltage will be charged up quickly by VCC through M1. The 2.5μA input to BST current source also can charge the BST capacitor when low-side switch doesn't turn-on.

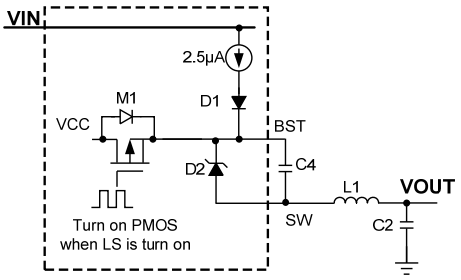


Figure 6: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both IN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, IN low, and thermal shutdown. In shutdown, the signaling path is blocked to avoid any fault triggering. Then V_{COMP} and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Buck Output Impedance

The Buck doesn't involve output discharge function during EN shutdown. After EN shutdown, there is only two feedback resistor connected to the OUT pin, which has a typical resistance of 175kΩ in total. Refer to the block diagram.

USB CURRENT-LIMIT SWITCH SECTION

Over-Current Protection (OCP) and Hiccup

The MP5408M integrates two USB current-limit switches. The MP5408M provides built-in soft-start circuitry which controls the rising slew rate of the output voltage to limit inrush current and voltage surges.

When the load current reaches the current-limit threshold the USB power MOSFET works in constant current-limit mode (see Figure 7). If the over-current limit condition lasts more than 5ms (V_{OUT} does not drop too low), the corresponding USB channel enters hiccup mode with 5ms of on-time and 2s of off-time. Another USB channel works normally.

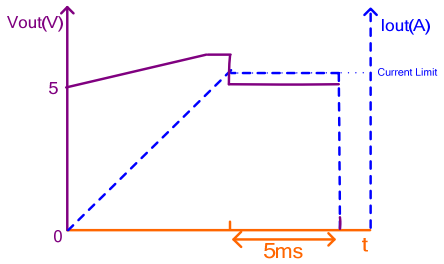


Figure 7: Over-Current Limit

After the soft start finishes, if the USB output voltage is lower than 3.5V and lasts longer than 50μs, the MP5408M enters hiccup without having to wait 5ms (see Figure 8). This can prevent abnormal thermal rise during the constant resistor (CR) load over-current case.

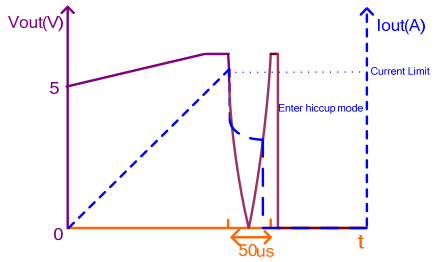


Figure 8: Over-Current Limit for CR Load

Fast Response for Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short-circuit event, the current may exceed the current limit threshold before the control loop is able to respond. If the current reaches the 7A secondary current limit level, a fast turn-off circuit activates to turn off the power MOSFET. This can help limit the peak current through the switch, keeping the buck output voltage from dropping too much and affecting another USB channel. The total short-circuit response time is less than 1µs.

When the fast turn-off function is triggered, the MOSFET turns off for 100µs and restarts with a soft start. During the restart process, if the short still remains, the MP5408M regulates the gate voltage to hold the current at a normal current limit level.

Output Line Drop Compensation

The MP5408M can compensate for an output voltage drop, such as high impedance caused by a long trace, to maintain a fairly constant output voltage at the load-side voltage.

The internal comparator compares the current-sense output voltage of the two current-limit switches and uses the larger current-sense output voltage to compensate for the line drop voltage.

The line drop compensation amplitude increases linearly as the load current increases. It also has an upper limitation. The line drop compensation at a 3A output current is 90mV.

USB Output Over-Voltage Clamp

To protect the device at the cable terminal, the USB switch output has a fixed over-voltage protection (OVP) threshold. When the input voltage is higher than the OVP threshold, the output voltage is clamped at 5.6V.

USB Output Discharge and Impedance

Each USB switch involves a fast discharge path that can quickly discharge the external output capacitor's energy during power shutdown. This function will be active when the CC pins are released or the part is disabled (input voltage is under UVLO or enable off). The discharge path is turned off when USB output voltage is discharged lower than 50mV. After turn-off the fast discharge path, there is only a high impedance resistor (typical 500kΩ) from USB1 or USB2 to ground.

Auto-Detection

The MP5408M integrates a USB dedicated charging port auto-detect function. This function recognizes most mainstream portable devices and supports the following charging schemes:

USB battery charging specification BC1.2/ Chinese Telecommunications Industry standard YD/T 1591-2009

- Apple divider mode
- 1.2V/1.2V mode
- USB Type-C 5V @ 3A DFP mode

The auto-detect function is a state machine that supports all of the DCP charging schemes above. Connect DP and DM with 150Ω resistor for DCP mode.

USB Type-C Mode and V_{CONN}

For USB Type-C solutions, two pins (CC1 and CC2) on the connector are used to establish and manage the source-to-sink connection. The general concept for setting up a valid connection between a source and a sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 9).

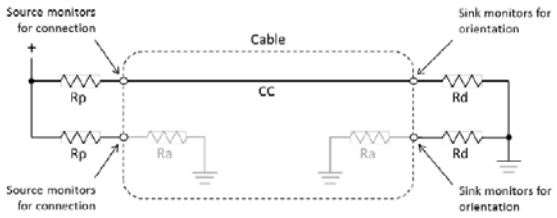


Figure 9: Current Source/Pull-Down CC Model

Initially, a source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. The choice of Rp is a function of the pull-up termination voltage and the source's detection circuit. This indicates that either a sink, a powered cable, or a sink connected via a powered cable has been attached. Prior to the application of V_{CONN}, a powered cable exposes Ra (typically 1kΩ) on its V_{CONN} pin. Ra represents the load on V_{CONN} plus any resistive elements to ground. In some cable plugs, this might be a pure resistance, and in others, it may simply be the load.

The source must be able to differentiate between the presence of Rd and Ra to know whether there is a sink attached and where to apply V_{CONN}. The source is not required to source V_{CONN} unless Ra is detected.

Two special termination combinations on the CC pins as seen by a source are defined for directly attached accessory modes: Ra/Ra for audio adapter accessory mode, and Rd/Rd for debug accessory mode (see Figure 10 and Table 2).

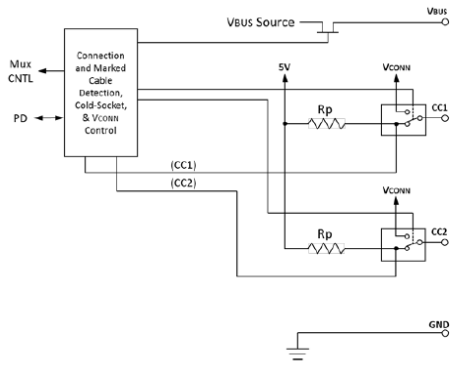


Figure 10: CC Functional Block

A port that behaves as a source has the following functional characteristics.

1. The source uses a MOSFET to enable or disable the power delivery across V_{BUS}. Initially, the source is disabled.
2. The source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a sink. The presence of an Rd pull-down resistor on CC1 or CC2 indicates that a sink is being attached. The value of Rp indicates the initial USB Type-C current level supported by the host. The MP5408M's Rp is 10kΩ, which represents a 3A current level.
3. The source uses the CC pull-down characteristic to detect and determine which CC pin is intended to supply VCONN (when Ra is discovered).
4. Once a sink is detected, the source enables V_{BUS} and V_{CONN}.
5. The source monitors the continued presence of Rd to detect a sink detach. When a detach event is detected, the source is removed, and V_{BUS} and V_{CONN} return to step 2.

Disable Type-C Mode (Type-A Mode)

During the MP5408M initial start-up, the IC sources 10μA for 20μs on CC1. If the CC1 voltage falls into a 400mV to 1.2V voltage range, USB1 latches in Type-A mode unless the part is re-enabled. Type-C mode is disabled, so CC is attached, the detach logic is, disabled and V_{BUS} is always enabled. The current limit changes to a Type-A spec. The same logic is implemented on CC3 for USB2.

To trigger Type-A mode, the external pull-down resistor should be 70 - 90kΩ. Do not connect extra capacitors on CC1 and CC3.

In normal Type-C mode application, a 1nF capacitor should be added on CC1 and CC3 respectively to avoid falsely trigger Type-A mode. Refer to the typical schematic for detail.

The MP5408M also supports debug mode and audio adapter accessory mode in Type-C applications. If two Ra resistors pull down CC1 and CC2, or two Rd resistors pull down CC1 and CC2, there is no action inside the IC (V_{BUS} is not enabled).

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 145°C), the chip is enabled.

Table 2: CC Logic Truth Table

EN	CC of USB1 (8)	CC of USB2 (8)	Buck	V_{CONN} (USB1)	USB1	VCONN (USB2)	USB2
0	X	X	Disabled	Disabled	Disabled	Disabled	Disabled
1	AUDIO	Open or AUDIO or DEBUG	Disabled	Disabled	Disabled	Disabled	Disabled
	DEBUG		Disabled	Disabled	Disabled	Disabled	Disabled
	"A" (9)		Enabled	Disabled	Enabled	Disabled	Disabled
	Rd, Ra		Enabled	Enabled	Enabled	Disabled	Disabled
	Open		Disabled	Disabled	Disabled	Disabled	Disabled
1	AUDIO	Rd, Ra	Enabled	Disabled	Disabled	Enabled	Enabled
	DEBUG		Enabled	Disabled	Disabled	Enabled	Enabled
	"A"		Enabled	Disabled	Enabled	Enabled	Enabled
	Rd, Ra		Enabled	Enabled	Enabled	Enabled	Enabled
	Open		Enabled	Disabled	Disabled	Enabled	Enabled
1	AUDIO	"A"	Enabled	Disabled	Disabled	Disabled	Enabled
	DEBUG		Enabled	Disabled	Disabled	Disabled	Enabled
	"A"		Enabled	Disabled	Enabled	Disabled	Enabled
	Rd, Ra		Enabled	Enabled	Enabled	Disabled	Enabled
	Open		Enabled	Disabled	Disabled	Disabled	Enabled

NOTES:

8) USB1 and USB2 are symmetric to each other.

9) "A" means Type-A mode. CC1 (CC3 for USB2) is requested to be pulled down by a 80.6kΩ resistor to enter this mode.

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use an inductor with a DC current rating at least 25% higher than the maximum load current. Select an inductor with a small DC resistance for optimum efficiency. For most designs, the inductor value can be derived with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Selecting the Buck Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current while maintaining the DC input voltage. Use low ESR capacitors for optimum performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. 100µF electrolytic and 50µF ceramic capacitors are recommended in applications with a 235kHz switching frequency.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using an electrolytic capacitor, place two additional high-quality ceramic capacitors as close to IN as possible. Estimate the input voltage ripple caused by the capacitance with Equation (5):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Selecting the Buck Output Capacitor

The device requires an output capacitor (C2) to maintain the DC output voltage. Estimate the output voltage ripple with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (6)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For an electrolytic capacitor, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (7)$$

A 100 - 270µF capacitor with an ESR less than 50mΩ (e.g.: polymer capacitor or tantalum capacitor) and three 10µF ceramic capacitors are recommended in the application.

For CLA applications, set the switching frequency to be 235kHz for better thermal performance (see Table 3).

Table 3: Recommended External Components

Switching Frequency	Inductor	Input Cap	Buck Output Capacitor
235kHz	8µH	50µF ceramic cap + 100µF E-cap	30µF ceramic cap + 270µF Polymer cap
450kHz	4.7µH	50µF ceramic cap + 100µF E-cap	30µF ceramic cap + 270µF Polymer cap

ESD Protection for I/O Pins

Higher ESD levels should be considered for all USB I/O pins. The MP5408M features high ESD protection up to ±8kV human body model on DP, DM, USB1, and USB2, and ±5.5kV human body model on CC1 through CC4. The ESD structures can withstand high ESD both in normal operation and when the device is powered off. To further extend DP and DM's ESD level for covering complicated application environments, additional resistors and capacitors can be added (see Figure 11).

Similar R-C networks cannot be added on CC1 or CC2 because the CC line must support 200mA of current and 300kHz of signaling. Additional ESD diodes can be added on the CC pins.

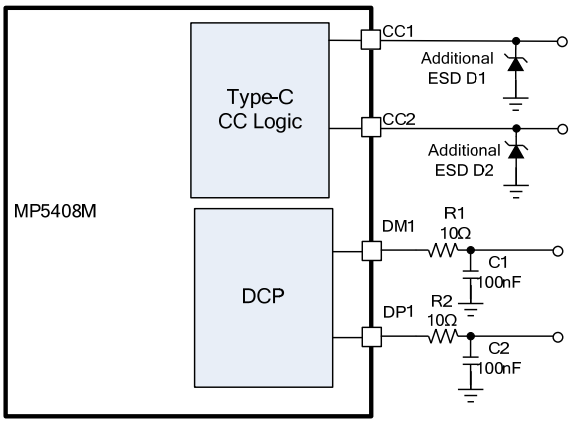


Figure 11: Recommended I/O Pins ESD Enhancing

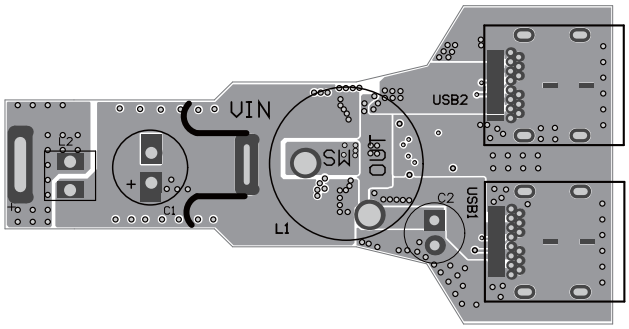
PC Board Layout [10]

Efficient PCB layout is critical for stable operation and thermal dissipation. For best results, refer to Figure 12 and follow the guidelines below.

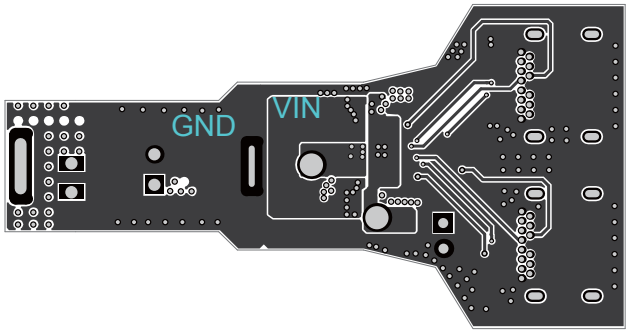
1. Use short, direct, and wide traces to connect OUT.
2. Add vias under the IC.
3. Route the OUT trace on both PCB layers.
4. Place the buck output ceramic capacitor C2A and C2B on one side and C2C on the other side.
5. Add a large copper plane for PGND.
6. Add multiple vias to improve thermal dissipation.
7. Connect AGND to PGND.
8. Place a large copper plane for SW, USB, and USB2.
9. Route the USB1 and USB2 traces on both PCB layers.
10. Add multiple vias.
11. Place two ceramic input decoupling capacitors as close to IN and PGND as possible to improve EMI performance.
12. Place the VCC decoupling capacitor as close to VCC as possible.

NOTE:

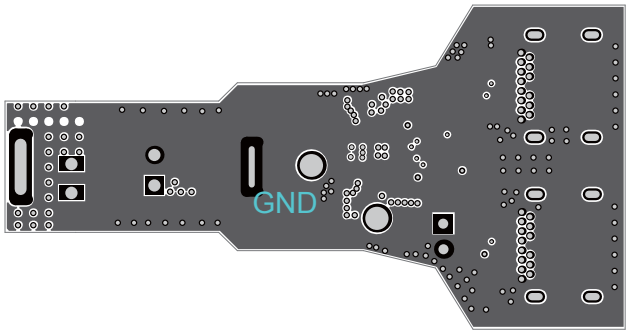
10) The recommended layout is based on the Typical Application Circuits in Figure 13 through Figure 15.



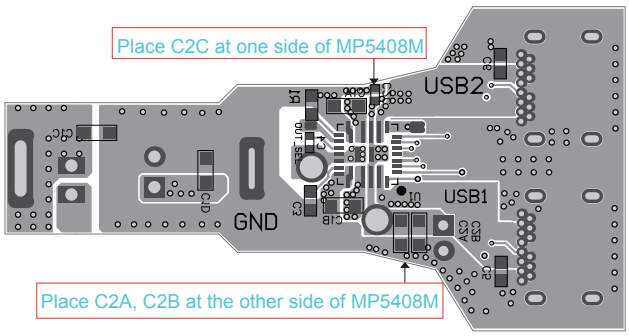
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 12: Recommended Layout

TYPICAL APPLICATION CIRCUITS

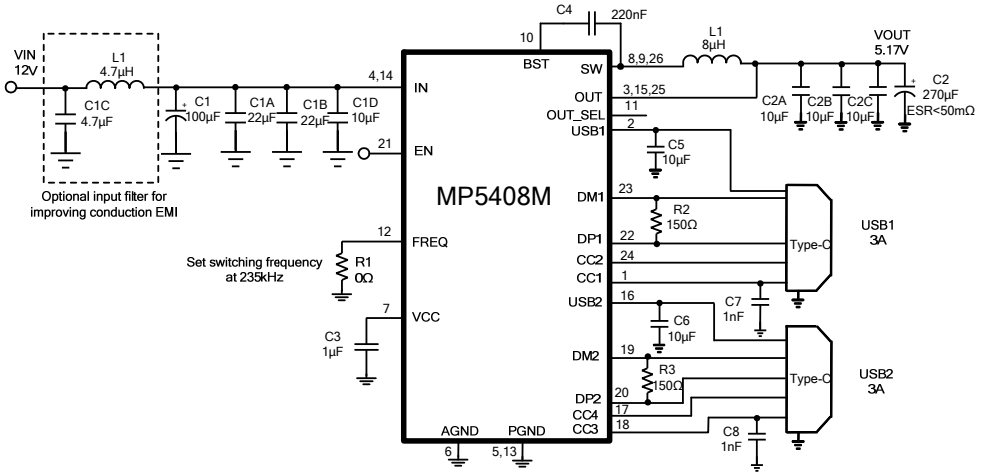


Figure 13: Dual USB Type-C 5V/3A DFP Ports (11)

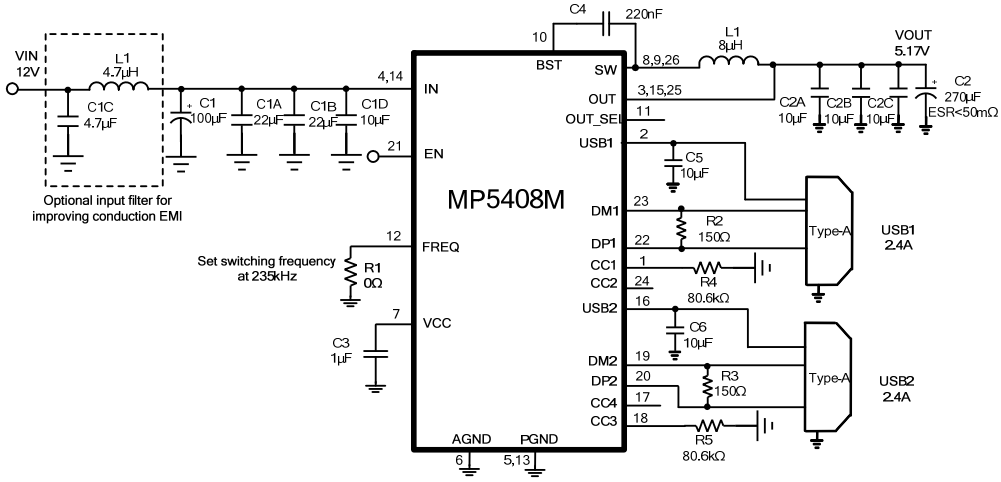


Figure 14: Dual USB Type-A 5V/2.4A Ports (11)

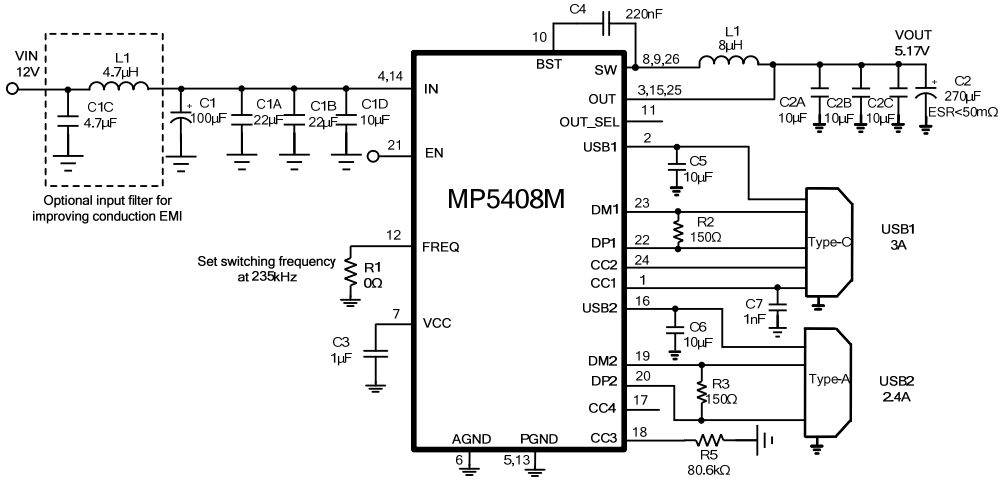


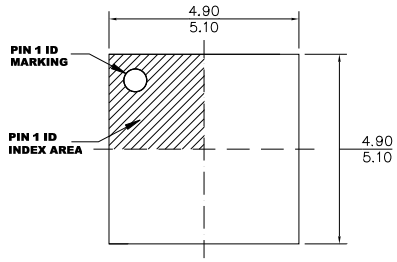
Figure 15: One Type-C 5V/3A DFP Port, One Type-A 5V/2.4A Port (11)

NOTE:

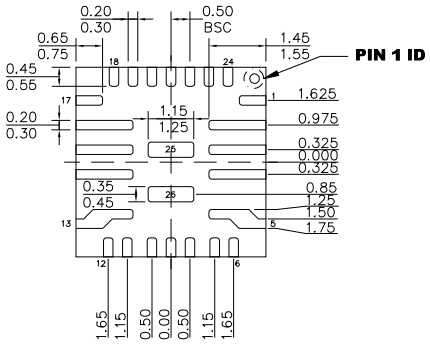
11) See Figure 11 for I/O pins' ESD protection enhancing details.

PACKAGE INFORMATION

QFN-26 (5mmx5mm)

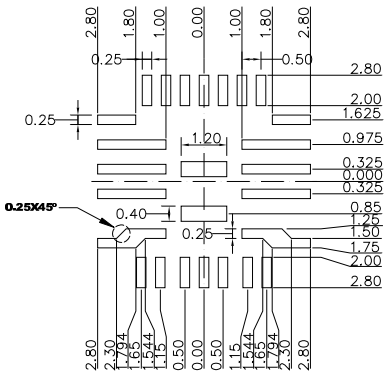


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERNS OF PIN 2~4 AND 14~16 HAVE THE SAME LENGTH AND WIDTH.
2) LAND PATTERNS OF PIN 5 AND PIN13 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) REFERENCEIS MO-220.
6) DRAWING IS NOT TO SCALE.