MP5470B

4V-16V, Power Management IC with Four 3A/3A/2A/2A Buck Converters and Flexible System Setting via I²C and MTP

DESCRIPTION

The MP5470B is a complete power management IC that integrates four high-efficiency, step-down DC/DC converters and a flexible logic interface.

Constant-on-time (COT) control provides fast transient response. The programmable switching frequency (up to 1.6MHz) reduces the external inductor and capacitor size greatly. Full protection features include under-voltage lockout (UVLO), over-current protection (OCP), over-voltage protection (OVP), and thermal warning/shutdown.

The output voltage is adjustable through the I²C bus or can be preset by the three-time programmable multi-time programmable (MTP) e-fuse. The power on/off sequence is also programmable by the MTP.

The MP5470B requires a minimal number of external components, and is available in a space-saving QFN-22 (3mmx4mm) package.

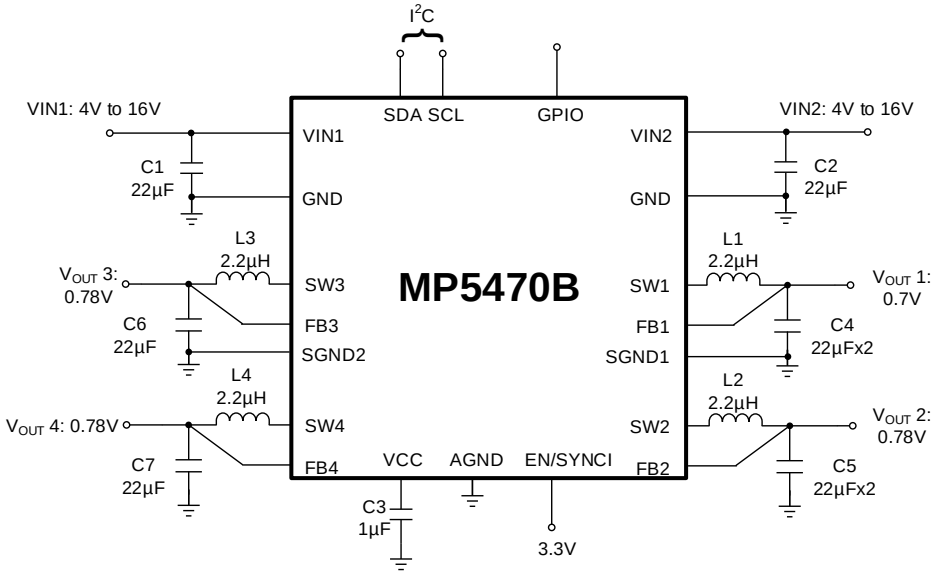
FEATURES

- ***Four High-Efficiency Buck Converters***
- Channel 1: 3A Maximum Output Current
- Channel 2: 3A Maximum Output Current
- Channel 3: 2A Maximum Output Current
- Channel 4: 2A Maximum Output Current
- Out-of-Phase Operation
- Wide 4V to 16V Operating Input Range
- Fast Load Transient Response
- Low $R_{DS(ON)}$ and High Efficiency
- Integrated Bootstrap Capacitor
- Adjustable Switching Frequency
- One GPIO Pin
- Power Good (PG) Indication
- I²C-Programmable Forced PWM or Auto PFM/PWM
- MTP Register Value
- Output Over-Current Protection (OCP)
- Output Over-Voltage Protection (OVP)
- ***System***
- I²C Slave
- Flexible Power On/Off Sequence via MTP
- Flexible DC/DC On/Off Control via MTP
- Enable (EN) Pin

APPLICATIONS

- Enterprise SSD
- NVDIMM
- DSLR
- FPGA-Based Design
- General 12V Power System

TYPICAL APPLICATION



MTP E-FUSE SELECTION TABLE BY DEFAULT

OTP Items	Buck 1	Buck 2	Buck 3	Buck 4
Output voltage	0.70V	0.78V	0.78V	0.78V
Initial on/off	On	On	On	On
Mode	PFM	PFM	PFM	PFM
Soft-start delay/time slot #	2ms / 2	2ms / 2	2ms / 2	2ms / 2
Soft-start time (0% to 100% V_O)	2.8ms	4.7ms	2ms	4.7ms
Valley current limit	4.2A	4.2A	3A	3A
Initial phase delay	0°	90°	180°	270°
Additional phase delay	0ns	0ns	0ns	0ns
Buck output discharge EN	Enabled	Enabled	Enabled	Enabled
Buck output limit EN	Enabled	Enabled	Enabled	Disabled
Buck parallel mode operation	Unparalleled		Unparalleled	
Switching frequency	800kHz			
VIN UVLO rising	5.8V			
GPIO	ADD			
Shutdown delay EN	Disabled			
PG delay time	0.2ms			
Software initial I²C slave address	0x68			
MTP configure code	0x00			
MTP revision number	0x00			

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP5470BGL-xxxx**	QFN-22 (3mmx4mm)	*See Below*
MP5470BGL-0000	QFN-22 (3mmx4mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP5470BGL-XXXX–Z).

** "xxxx" is the configuration code identifier for the register setting stored in the MTP. The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number, even if ordering the "0000" code. MP5470BGL-0000 is the default version.

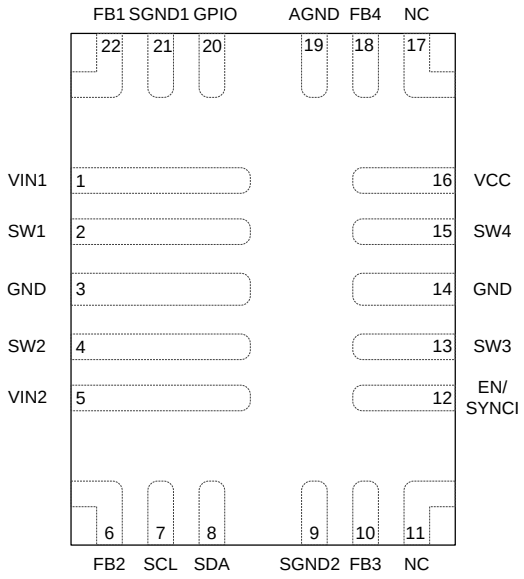
TOP MARKING

MPYW
5470
BLLL

MP: MPS prefix
Y: Year code
W: Week code
5470B: Part number
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-22 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VIN1	**Supply voltage input of buck 1 and buck 4.** The MP5470B operates from a 4V to 16V input rail. Use a ceramic capacitor to decouple the input rail. Connect VIN1 using a wide PCB trace. VIN1 and VIN2 should be connected together.
2	SW1	**Buck 1 switch output.** Connect SW1 using a wide PCB trace.
3, 14	GND	**Power ground.** GND requires special consideration during PCB layout. Connect GND with copper traces and vias.
4	SW2	**Buck 2 switch output.** Connect SW2 using a wide PCB trace.
5	VIN2	**Supply voltage input of buck 2 and buck 3.** The MP5470B operates from a 4V to 16V input rail. Use a ceramic capacitor to decouple the input rail. Connect VIN2 using a wide PCB trace. VIN1 and VIN2 should be connected together.
6	FB2	**Feedback of buck 2.** Connect buck 2's output to FB2 directly or through a feedback resistor divider.
7	SCL	**I²C clock signal input.**
8	SDA	**I²C data.**
9	SGND2	**Remote-sense ground of buck 3 and buck 4.** Kelvin-connect SGND2 to buck 3 and buck 4 output capacitors' ground nodes.
10	FB3	**Feedback of buck 3.** Connect buck 3's output to FB3 directly or through a feedback resistor divider.
11, 17	NC	**No connection.**
12	EN/SYNCI	**Enable control pin.** Pull EN/SYNCI to logic high to enable the MP5470B. Pull EN/SYNCI to logic low to disable the MP5470B. EN has a 2MΩ internal pull-down resistor. Apply a clock on EN/SYNCI to synchronize the switching frequency to the external clock.
13	SW3	**Buck 3 switch output.** Connect SW3 using a wide PCB trace.
15	SW4	**Buck 4 switch output.** Connect SW4 using a wide PCB trace.
16	VCC	**Internal 3.3V LDO output.** The driver and control circuits are powered from the VCC voltage. Decouple VCC with a 1μF ceramic capacitor placed as close to VCC as possible. X7R or X5R-grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
18	FB4	**Feedback of buck 4.** Connect buck 4's output to FB4 directly or through a feedback resistor divider.
19	AGND	**Analog ground.** Connect AGND to GND.
20	GPIO	**General pin input/output.** When the MTP/I²C configures GPIO as ADD, this pin can program four different I²C slave addresses. When the MTP/I²C configures GPIO as PG, this pin is the power good output. PG is an open drain. Pull PG low when any enabled regulator falls below the under-voltage (UV) threshold. Pull PG low when all regulators are disabled. When the MTP/I²C configures GPIO as the output port, this pin outputs high/low logics determined by a related register. The output port is an open-drain structure. When the MTP/I²C configures GPIO as a SYNC output, this pin has a synchronous output. SYNC out has a phase-shifted clock output to synchronize another device's switching frequency.
21	SGND1	**Remote-sense ground of buck 1 and buck 2.** Kelvin-connect SGND2 to buck 1 and the buck 2 output capacitor's ground node.
22	FB1	**Feedback of buck 1.** Connect buck 1's output to FB1 directly or through a feedback resistor divider.

ABSOLUTE MAXIMUM RATINGS (1)

V_{VIN1}, $_{VIN2}$ ..... -0.3V to +18V
V_{SWx} .....-0.6V (-7V for <10ns) to V_{INx} + 0.3V (22V for <10ns)
EN/SYNCI, FBx ..... -0.3V to 6V (2)
GPIO, VCC, SCL, SDA.....-0.3V to 4V
Continuous power dissipation (T_A = 25°C) (3) 4.31W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

Recommended Operating Conditions (4)

Step-down regulator (V_{IN})..... 4V to 16V
Step-down regulator (V_{OUT}) ..... 0.55V to 7V or V_{IN} * D_{MAX}, if V_{IN} < 7V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-22 (3mmx4mm)			
EV5470B-L-00A (5)	29	4	°C/W
JESD51-7 (6)	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For EN/SYNCI's rating, see the EN/SYNCI section on page 15.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on EV5470B-L-00A, 4-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 12V, T_J = -40°C to +125°C [7], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (no switching)	I_{IN}	No switching, FB high, PFM		1500	2500	μA
Shutdown current	I_{IN_STD}	I²C, VCC, and MTP are active		40	80	μA
Default oscillation frequency	f_{SW}		-15%	800	+15%	kHz
EN rising threshold	V_{EN_R}		-2.5%	1.21	+2.5%	V
EN hysteresis	V_{EN_F}			150		mV
EN input current	I_{EN}	V_{EN} = 2V		1		μA
Frequency SYNC input range [8]	f_{SYNCI}		500		1600	kHz
PG UV rising	$V_{PG\_UV\_R}$		88%	92%	97%	V_{REF}
PG UV falling	$V_{PG\_UV\_F}$			87%		V_{REF}
PG rise delay [9]	$t_{PG\_R\_DLY}$	MTP adjustable		200		μs
PG falling delay [9]	$t_{PG\_F\_DLY}$			50		μs
Power good, output port sink current capability	V_{PG_Sink}	Sink 1mA			0.4	V
ADD pin voltage threshold 1	V_{ADD_1}	To set I²C address 1			20%	V_{CC}
ADD pin voltage threshold 2	V_{ADD_2}	To set I²C address 2	33%		45%	V_{CC}
ADD pin voltage threshold 3	V_{ADD_3}	To set I²C address 3	56%		71%	V_{CC}
ADD pin voltage threshold 4	V_{ADD_4}	To set I²C address 4	80%			V_{CC}
ADD pin input current	I_{ADD}	V_{ADD} = 2V		0		μA
Frequency sync output range	f_{SYNCO}	Open drain	500		1600	kHz
Frequency sync output duty	D_{SYNCO}	2.2kΩ resistor pulled up to VCC		50		%
VCC UVLO rising	V_{CC_R}		2.8	3.0	3.2	V
VCC UVLO hysteresis	V_{CC_HYS}			100		mV
VCC voltage	V_{CC}	I_{CC} = 0mA	3.1	3.3	3.5	V
VCC voltage regulation	V_{CC_RG}	I_{CC} = 0mA to 25mA		1		%
Thermal shutdown [9]	T_{OTP_R}			160		°C
Thermal hysteresis [9]	T_{Hys}			20		°C
Step-Down Regulator						
VIN1 UVLO rising	V_{IN1_R}	Adjustable by MTP	5.6	5.8	6.0	V
VIN1 UVLO hysteresis	V_{IN1_HYS}			800		mV
VIN2 UVLO rising	V_{IN2_R}	Adjustable by MTP	5.6	5.8	6.0	V
VIN2 UVLO hysteresis	V_{IN2_HYS}			800		mV
Feedback voltage accuracy	V_{FB1}		-1.5%	0.70	+1.5%	V
	V_{FB2}		-1.5%	0.78	+1.5%	V
	V_{FB3}		-1.5%	0.78	+1.5%	V
	V_{FB4}		-1.5%	0.78	+1.5%	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = 12V, T_J = -40°C to +125°C [7], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Buck 1, Buck 2 (3A DC/DC)						
HS switch on resistance [9]	HS_{RON1}			58		mΩ
LS switch on resistance	LS_{RON1}			25		mΩ
Low-side current limit (source)	$I_{LS\_Valley1}$	Valley limit during OCP	3.2	4.2	5.2	A
Low-side current limit (sink)	I_{CL_PWM1}	Forced PWM mode, OVP, discharge		-2		A
Minimum on time [9]	t_{ON_MIN1}			33		ns
Minimum off time [9]	t_{OFF_MIN1}			113		ns
Output OVP rising threshold	V_{OVP1_H}		115%	120%	125%	V_{REF}
Output OVP recovery threshold	V_{OVP1_L}			114%		V_{REF}
Output discharge resistor [9]	R_{SW1}/R_{SW2}			45		Ω
Soft-start time of buck 1	t_{SS_B1}	V_{OUT} = 10% to 90%		2.1		ms
Soft-start time of buck 2	t_{SS_B2}	V_{OUT} = 10% to 90%		3.5		ms
Buck 3, Buck 4 (2A DC/DC)						
HS switch on resistance [9]	HS_{RON2}			70		mΩ
LS switch on resistance	LS_{RON2}			50		mΩ
Low-side current limit (source)	$I_{LS\_Valley2}$	Valley limit during OCP	2	3	4	A
Low-side current limit (sink)	I_{CL_PWM2}	Forced PWM mode, OVP, discharge		-1.5		A
Minimum on time [9]	t_{ON_MIN2}			31		ns
Minimum off time [9]	t_{OFF_MIN2}			133		ns
Output OVP rising threshold	V_{OVP2_H}		115%	120%	125%	V_{REF}
Output OVP recovery threshold	V_{OVP2_L}			114%		V_{REF}
Output discharge resistor [9]	R_{SW3}/R_{SW4}			45		Ω
Soft-start time of buck 3	t_{SS_B3}	V_{OUT} = 10% to 90%		1.5		ms
Soft-start time of buck 4	t_{SS_B4}	V_{OUT} = 10% to 90%		3.5		ms
I²C Interface Specifications [10]						
Input logic high	V_{IH}		1.4			V
Input logic low	V_{IL}				0.4	V
Output voltage logic low	V_{OUT_L}	Sink 4mA			0.4	V
SCL clock frequency	f_{SCL}				3.4	MHz
SCL high time	t_{HIGH}		60			ns
SCL low time	t_{LOW}		200			ns
Data set-up time	$t_{SU.DAT}$		10			ns
Data hold time	$t_{HD.DAT}$			70		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = V_{IN2} = 12V, T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Set-up time for repeated start	$t_{SU.STA}$		160			ns
Hold time for (repeated) start	$t_{HD.STA}$		160			ns
Bus free time between a start and a stop condition	t_{BUF}		160			ns
Set-up time for stop condition	$t_{SU.STO}$		160			ns
Rise time of SCL and SDA	t_R		10		300	ns
Fall time of SCL and SDA	t_F		10		300	ns
Pulse width of suppressed spike	t_{SP}		0		50	ns
Capacitance bus for each bus line	C_B				400	pF

Notes:

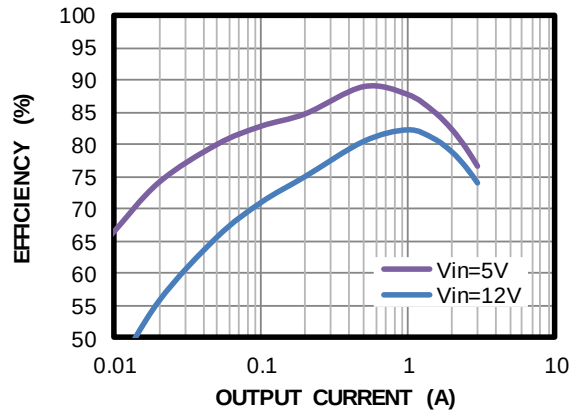
7) Not tested in production, guaranteed by over-temperature correlation.
8) This function has limitations—only a SYNC IN close to the current system switching frequency can be used.
9) Guaranteed by engineering sample characterization.
10) The maximum I²C bus voltage should be lower than 4V. A typical bus voltage of 1.8V or 3.3V is recommended.

TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board. VIN1 = VIN2 = 12V, T_A = 25°C, buck 1 to buck 4 output 0.6V/1V/5V/1.8V, switching frequency 800kHz, unless otherwise noted.

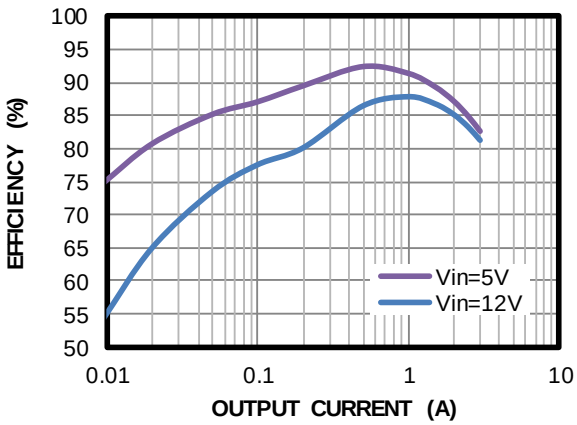
Efficiency, V_{OUT} = 0.6V

Buck 1 works in auto PFM/PWM mode



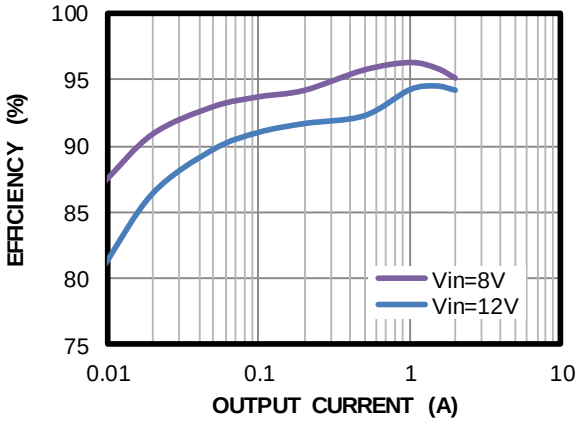
Efficiency, V_{OUT} = 1V

Buck 2 works in auto PFM/PWM mode



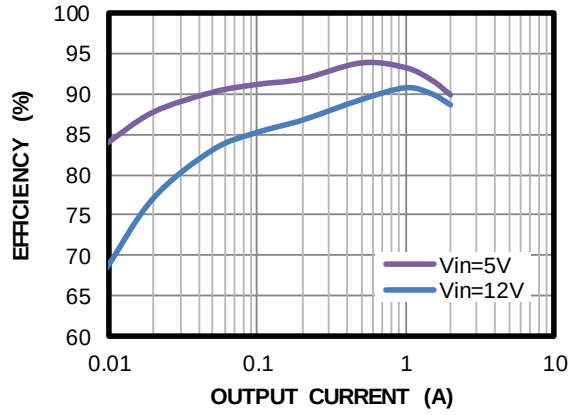
Efficiency, V_{OUT} = 5V

Buck 3 works in auto PFM/PWM mode



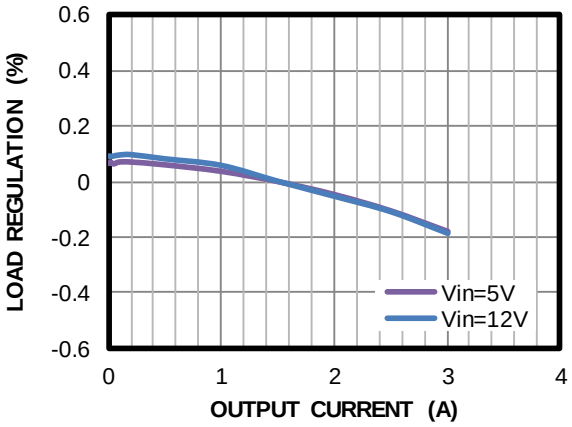
Efficiency, V_{OUT} = 1.8V

Buck 4 works in auto PFM/PWM mode



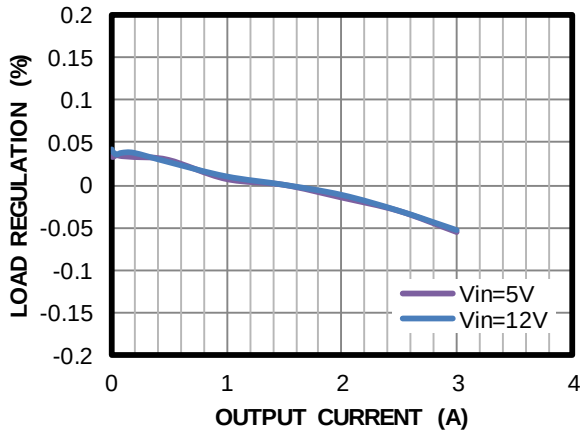
Load Regulation

Buck 1 works in auto PFM/PWM mode



Load Regulation

Buck 2 works in auto PFM/PWM mode

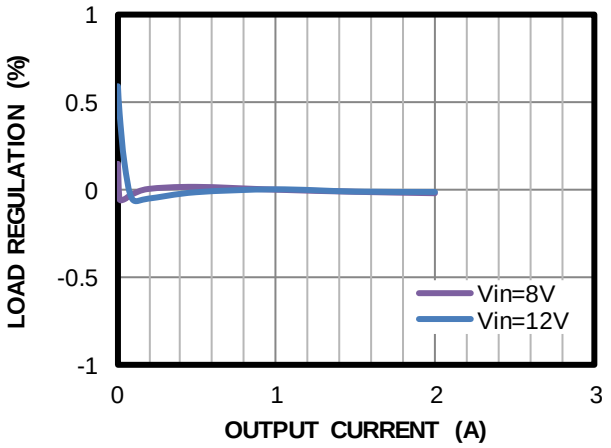


TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. VIN1 = VIN2 = 12V, T_A = 25°C, buck 1 to buck 4 output 0.6V/1V/5V/1.8V, switching frequency 800kHz, unless otherwise noted.

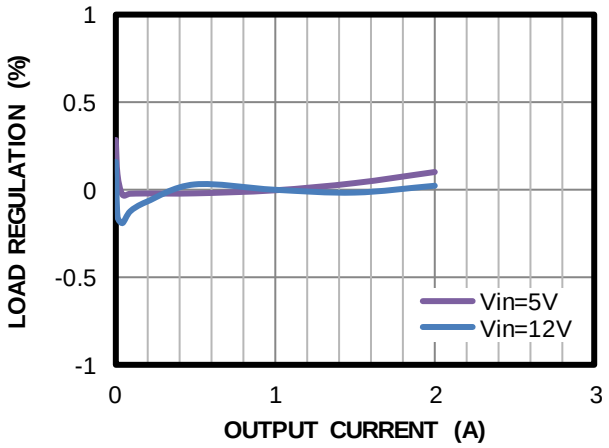
Load Regulation

Buck 3 works in auto PFM/PWM mode

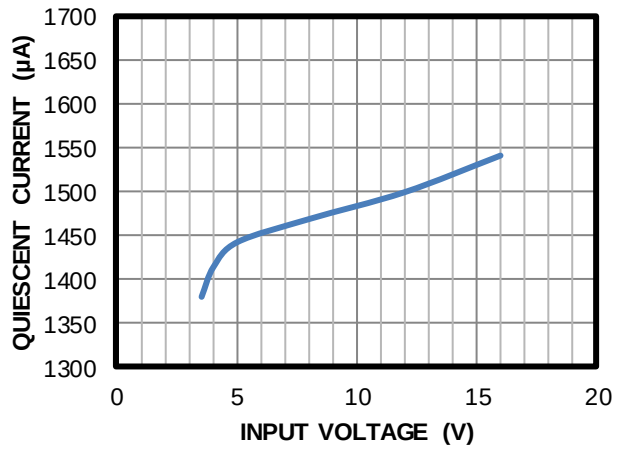


Load Regulation

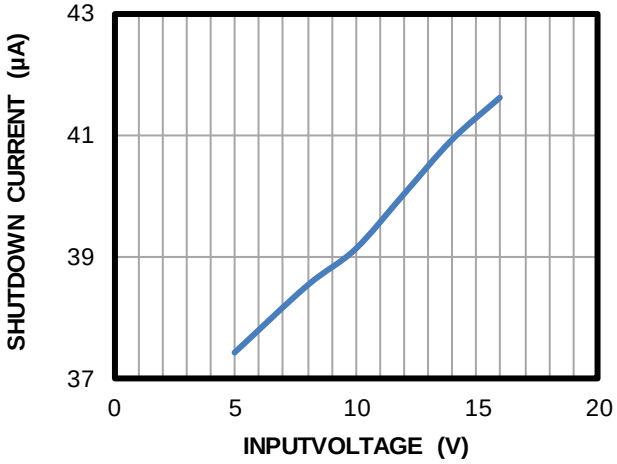
Buck 4 works in auto PFM/PWM mode



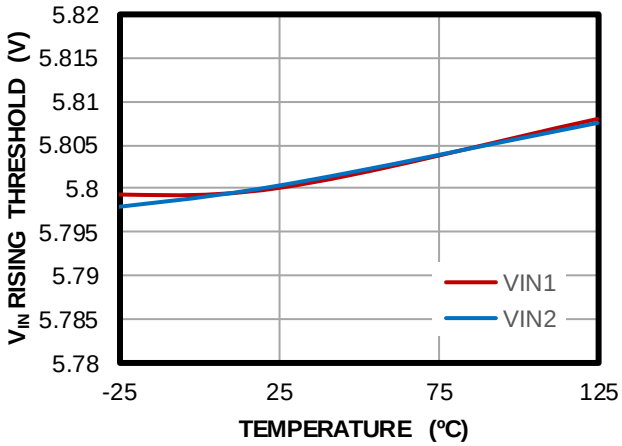
Quiescent Current vs. Input Voltage



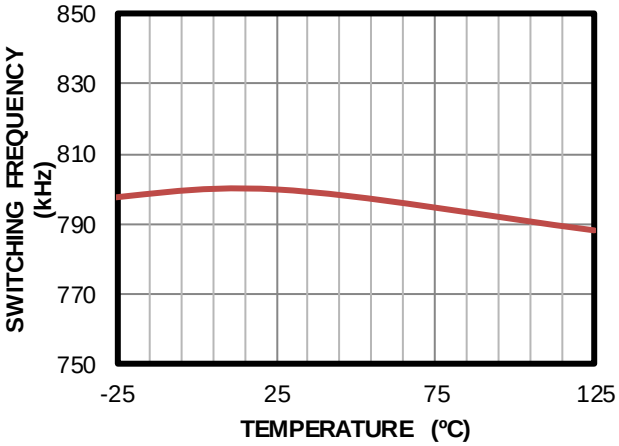
Shutdown Current vs. Input Voltage



V_{IN} Rising Threshold vs. Temperature



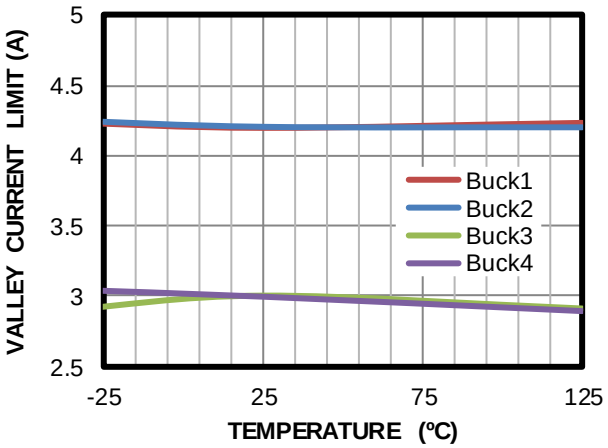
Switching Frequency vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

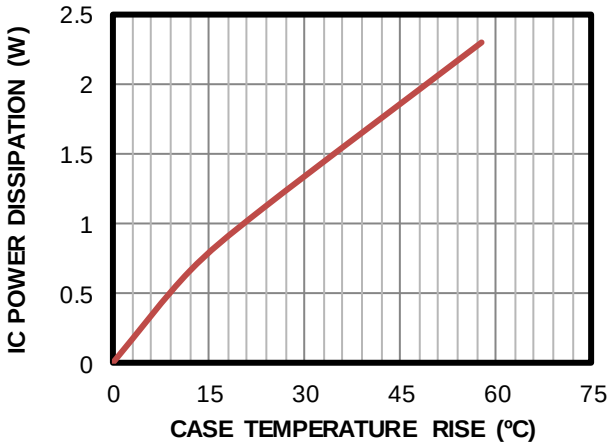
Performance waveforms are tested on the evaluation board. VIN1 = VIN2 = 12V, T_A = 25°C, buck 1 to buck 4 output 0.6V/1V/5V/1.8V, switching frequency 800kHz, unless otherwise noted.

Valley Current Limit vs. Temperature



IC Power Dissipation vs. Case Temperature Rise

Tested on 4-layer PCB (6.35cmx6.35cm)

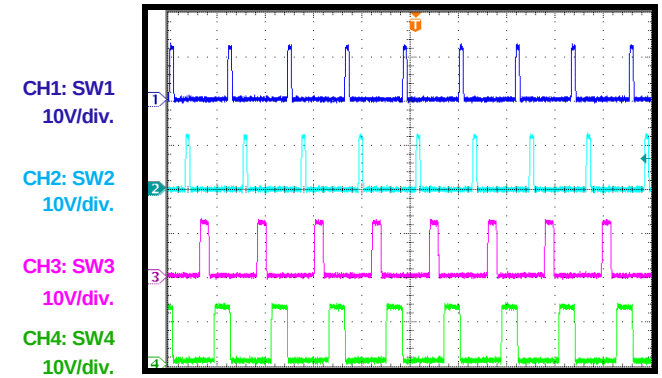


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board. VIN1 = VIN2 = 12V, T_A = 25°C, buck 1 to buck 4 output 0.78V/0.78V/1.8V/3.3V, switching frequency 800kHz, unless otherwise noted.

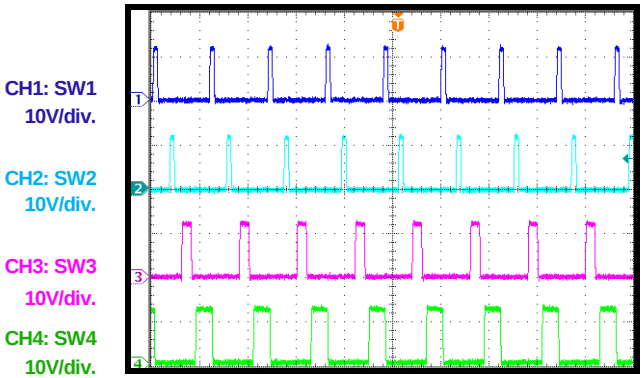
Steady State

Each channel buck with half-load



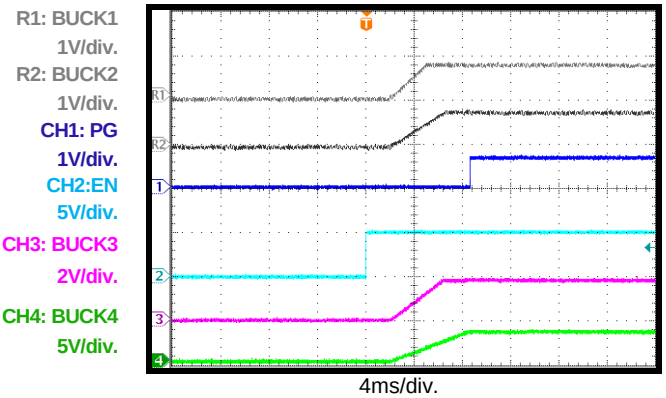
Steady State

Each channel buck with full load



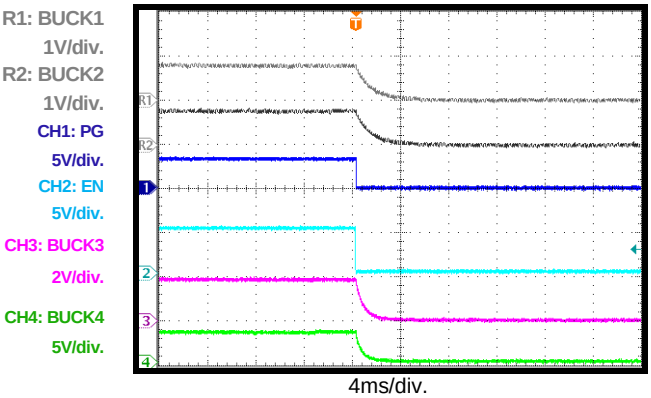
EN Power On

Each channel buck without load



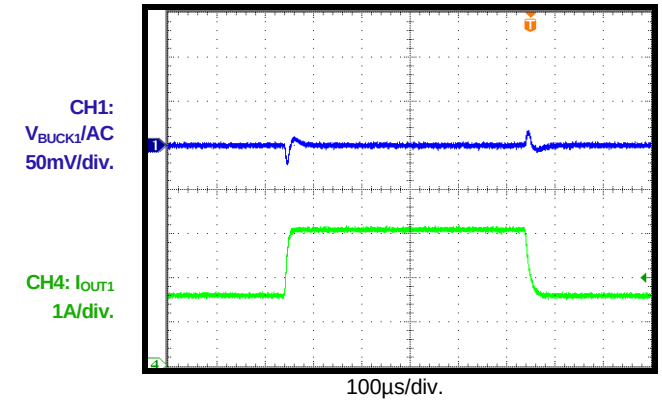
EN Power Off

Each channel buck without load



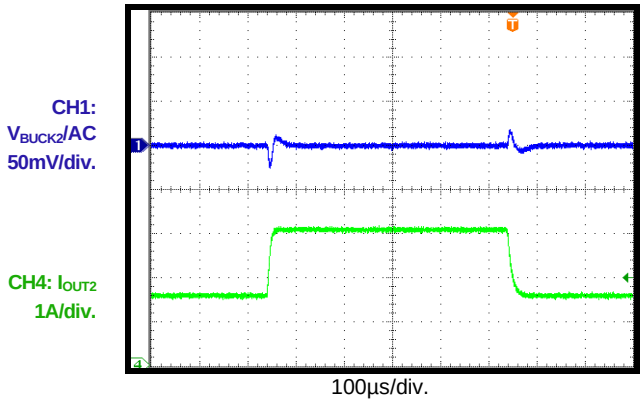
Load Transient Response

Buck 1, I_{OUT} transient from 1.5A to 3A, slew rate = 0.8A/µs



Load Transient Response

Buck 2, I_{OUT} transient from 1.5A to 3A, slew rate = 0.8A/µs

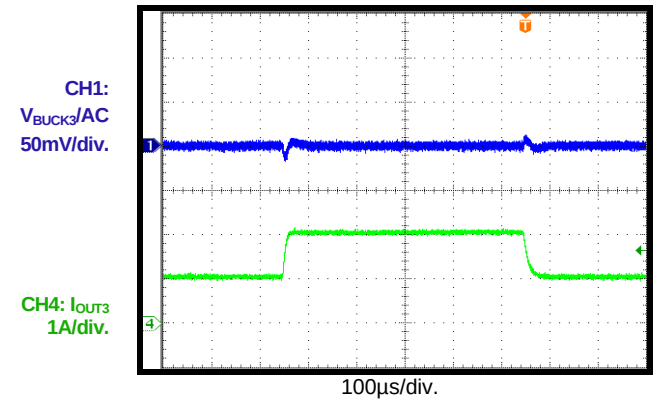


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board. VIN1 = VIN2 = 12V, T_A = 25°C, buck 1 to buck 4 output 0.78V/0.78V/1.8V/3.3V, switching frequency 800kHz, unless otherwise noted.

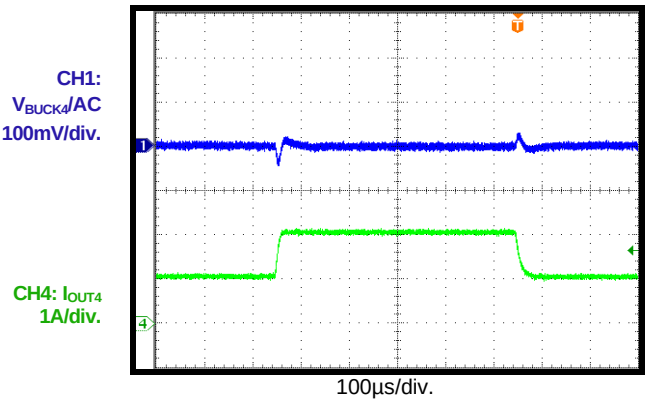
Load Transient Response

Buck 3, I_{OUT} transient from 1A to 2A, slew rate = 0.8A/µs



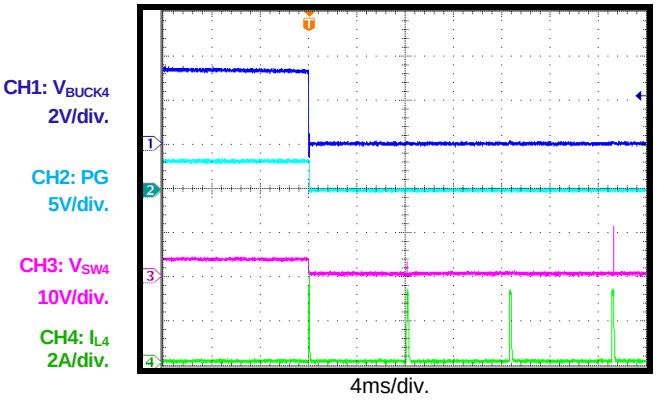
Load Transient Response

Buck 4, I_{OUT} transient from 1A to 2A, slew rate = 0.8A/µs



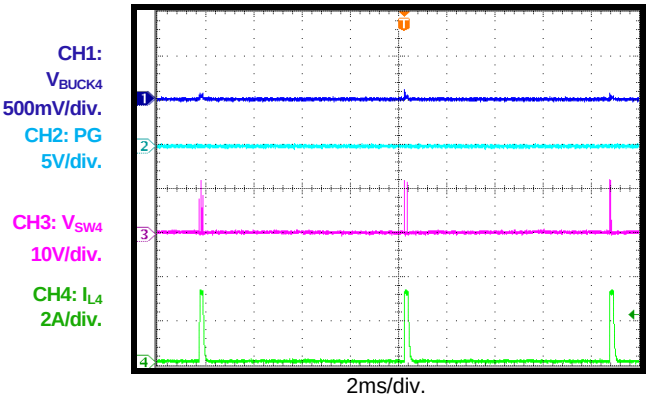
SCP Entry

Buck 4 output 3.3V, I_O = 0A



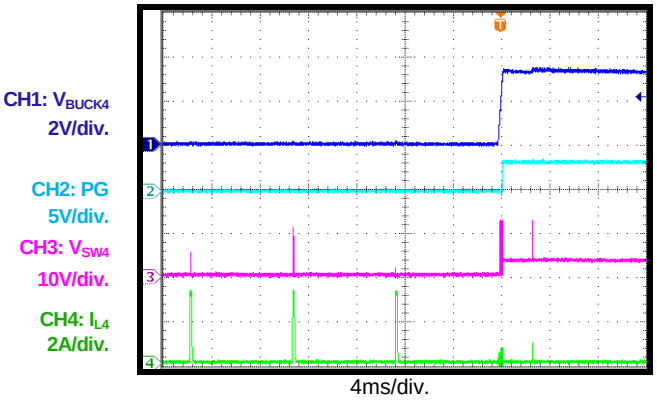
SCP Steady State

Buck 4 output 3.3V, I_O = 0A



SCP Recovery

Buck 4 output 3.3V, I_O = 0A



FUNCTIONAL BLOCK DIAGRAM

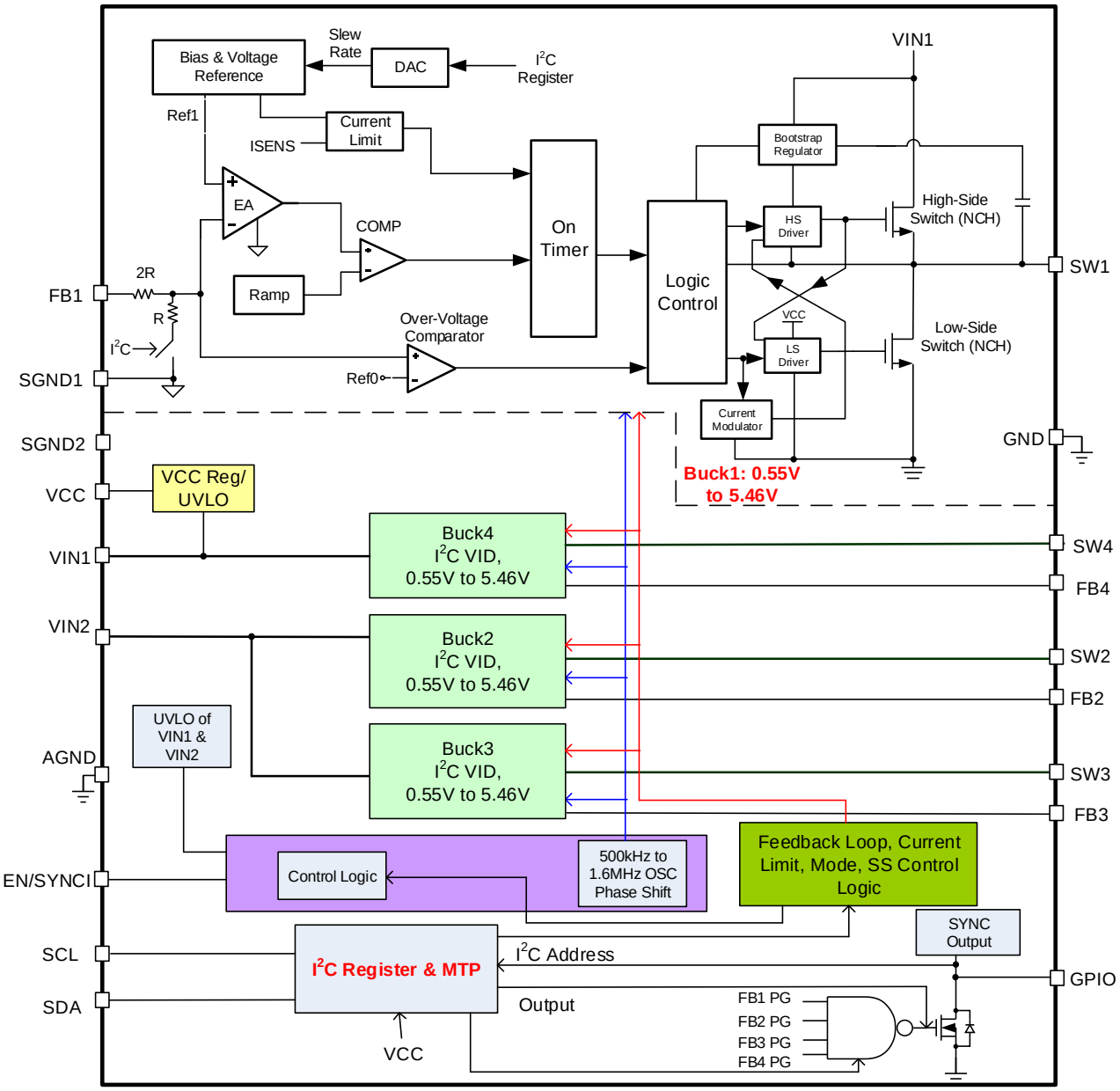


Figure 1: Functional Block Diagram

ANALOG OPERATION

High-Efficiency Buck Regulators

Buck 1 to buck 4 are synchronous, step-down, DC/DC converters with built-in soft start, compensation, and hiccup current limit protection. Fixed-frequency, constant-on-time (COT) control provides a fast transient response. The switching clock is locked and phase-shifted from buck 1 to buck 4 during continuous conduction mode (CCM) operation.

Power Supply and UVLO

VIN1 is the power supply of buck 1 and buck 4. VIN2 is the power supply of buck 2 and buck 3. VIN1 also powers the VCC LDO regulator. It is recommended to connect VIN1 and VIN2 together during application. When the input voltage exceeds the under-voltage lockout (UVLO) rising threshold voltage, the corresponding buck powers up. The buck shuts down when the input voltage falls below the UVLO falling threshold voltage. See the state machine diagram on page 31 for more detail.

Enable and Switching Frequency SYNC Input (EN/SYNCI)

EN/SYNCI is a digital control pin that turns the regulator on and off. Drive EN/SYNCI high to turn on the regulator. Drive EN/SYNCI low to turn off the regulator. EN/SYNCI is pulled low automatically by an internal resistor when EN/SYNCI is floating.

Connecting EN/SYNCI directly to a voltage source requires limiting the amplitude of the voltage source to ≤6V to prevent damage. A resistor divider is needed when pulling EN/SYNCI up to a $12V_{IN}$ supply.

For external clock synchronization, connect a clock with a frequency range between 500kHz and 1.6MHz to EN/SYNCI. Buck 1's SW rising edge will synchronize with the external clock rising edge. Select an external clock signal with a pulse width less than 1.7µs. After synchronization, the buck 1 to buck 4 phase shift continues to follow the MTP definition.

The MP5470B default switching frequency should be set close to the sync input's frequency. For example, when the external SYNCI clock is 500kHz, the internal switching frequency should be set at 533kHz via the I²C or MTP. The I²C and MTP functions, including the ADD pin function, are kept active when EN/SYNCI is pulled low.

Thermal Shutdown

The MP5470B employs thermal shutdown by internally monitoring the junction temperature of the IC. If the junction temperature exceeds the 160°C threshold, the converter shuts off. This is a non-latch protection. There is a hysteresis of about 20°C. Once the junction temperature drops to about 140°C, a soft start is initiated.

Pre-Bias Start-Up

The MP5470B has been designed for monotonic start-up into a pre-biased V_{OUT}. If the output is pre-biased to a certain voltage during start-up, the internal BST voltage is refreshed and charged, and the soft-start reference begins ramping up. If the BST voltage exceeds its rising threshold voltage and the soft-start reference voltage exceeds the sensed output voltage at FB, the MP5470B begins to soft start.

Power Good (PG)

The MP5470B has power good (PG) register bits (bits D4 to D7 of the status register), which indicate whether the enabled buck's output voltage is ready or not. When buck x's feedback voltage (V_{FB}) exceeds 92% of the reference voltage (V_{REF}), the corresponding PGx bit in the status register is set to 1 after a 200µs default time or other MTP-programmed delay time. During normal operation, the PGx bit is set to 0 when the corresponding buck regulator falls below the under-voltage (UV) threshold with a 50µs delay.

The MP5470B's GPIO pin can be configured as a dedicated PG pin. PG is a wired AND output of FB1 PG to FB4 PG signals (see Figure 2).

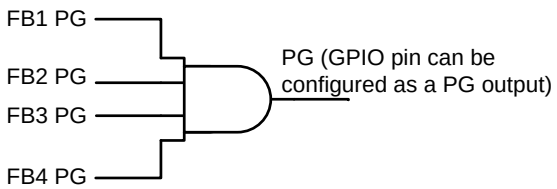


Figure 2: GPIO Configured as a PG Output Logic

PG is pulled low when any enabled regulator falls below the UV threshold. PG is pulled low when all regulators are disabled.

During UVLO, if EN/SYNCI is low, or an over-temperature protection (OTP) occurs, the PG pin is pulled low immediately. When an over-current condition occurs, PG is pulled low when V_{FB} drops below 87% of V_{REF} after a 50µs delay. The PG function does not indicate an output over-voltage condition.

Output Over-Voltage Protection (OVP)

The MP5470B monitors the output voltage and enters over-voltage protection (OVP) discharge mode once the output voltage exceeds 120% of V_{REF} for longer than 2.5µs. In OVP discharge mode, the low-side MOSFET (LS-FET) is turned on until the low-side current drops to the negative current limit. This discharges the output to keep the output voltage within the normal range. If the output voltage over-voltage condition still remains, the LS-FET turns on again after a fixed delay to repeat the discharge behavior.

The MP5470B exits this discharge mode when V_{FB} drops below 114% of V_{REF}.

If the input voltage of the MP5470B during OVP discharge mode exceeds 18V (the input OVP threshold), the MP5470B stops switching until the input voltage drops below 16V. Then the MP5470B enters discharge mode again. This input OVP function is active only during an output over-voltage (OV) condition.

The OVP function can be enabled or disabled through the I²C and MTP interface.

Output Discharge

To discharge the energy of the output capacitor during a power-off sequence or shutdown sequence, there is a typical 45Ω discharge resistor from SWx to ground. The discharge function can be enabled or disabled through the I²C and MTP interface.

Soft Start (SS)

The MP5470B employs a soft start (SS) mechanism to ensure a smooth output during power-up. When the MP5470B is enabled and the BST voltage reaches its rising threshold, the internal DAC outputs a ramp voltage (reference voltage). The output voltage ramps up smoothly with the reference voltage. When the DAC output reaches the final voltage, it stops at that level. At this point, the soft start finishes, and the MP5470B enters steady-state operation.

The start-up delay and soft-start slew rate are both programmable by the MTP.

Out-of-Phase Operation and Clock SYNC Out

Buck 1 to buck 4 are frequency-locked and phase-shifted. The phase shift can be changed by the MTP (see Figure 3). The phase shift feature is the same for the EN/SYNCI input case.

When the GPIO pin is configured in SYNC output mode, the MP5470B outputs a 180° phase shift from the internal clock's rising edge (50% duty pulse). SYNC output is an open-drain output, and an external 2.2kΩ to 10kΩ pull-up resistor should be added to it. The SYNC out function is still active, even if buck 1 to buck 4 all enter light-load sleep mode. The SYNC out signal is enabled when the EN voltage exceeds the EN rising threshold voltage.

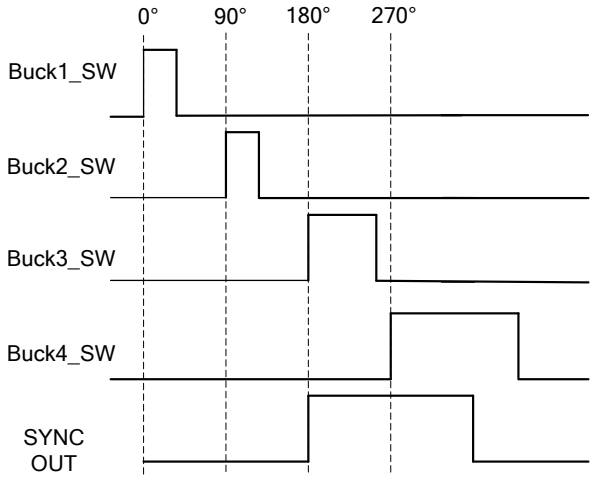


Figure 3: Phase Shift Example

VCC Regulator

A 3.3V internal regulator powers most of the internal circuitries. A decoupling capacitor is needed to stabilize the regulator and reduce the ripple. This regulator takes the V_{IN1} input and operates in the full V_{IN1} range.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP5470B has valley current-limit control. The inductor current is monitored during the LS-FET on state. When the sensed inductor current exceeds the valley current-limit threshold, the device enters over-current protection (OCP) mode. The high-side MOSFET (HS-FET) is not allowed to turn on until the valley current limit is removed. Meanwhile, the output voltage drops until it is below the UV threshold (typically 45% of the reference).

Once UV and OC are both triggered, the MP5470B enters hiccup mode to restart the related power rail periodically. The hiccup duty cycle must be very small to reduce power dissipation during a short-circuit condition. During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the MP5470B disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the OC condition still remains when soft start finishes, the MP5470B repeats this operation. OCP is a non-latch protection.

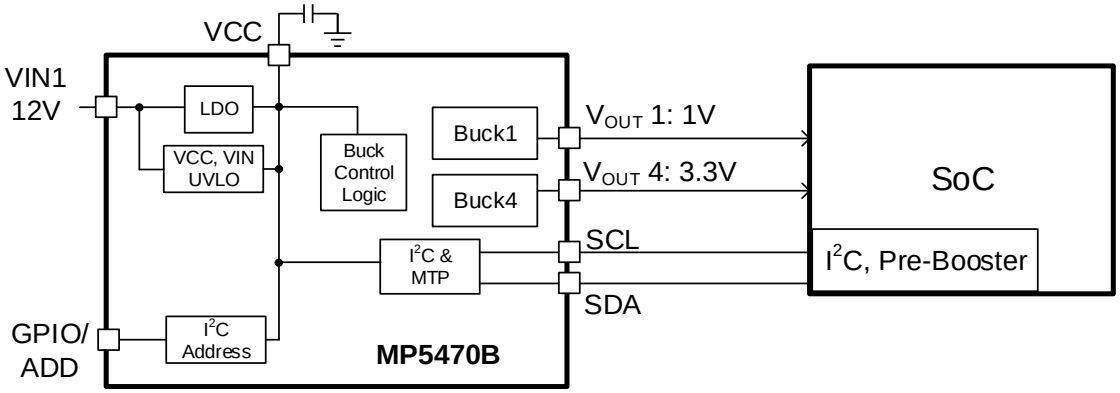


Figure 4: I²C Start-Up Block

DIGITAL INTERFACE

Multiple-Time Programming (MTP)

The I²C and MTP blocks are active with a 100µs delay after VCC's voltage exceeds the 2V rising threshold, regardless of whether EN/SYNCI's voltage is high or low. Figure 4 shows a system-level application example.

When VIN1 powers up and EN/SYNCI is pulled high, the MP5470B starts up with a safe mode that allows the system on-chip processor (SoC) to start up without damage. In safe mode, only one or two power rails turn on. For example, if V_{OUT} 1 = 1V and V_{OUT} 4 = 3.3V, the other power rails are off. The default buck 1 to buck 4 configurations are determined by the MTP e-fuse. The MTP data is loaded into the corresponding I²C registers during the initial power-up, and the I²C registers directly control the parameters for buck 1 to buck 4. For the MTP load to the I²C register condition, V_{CC} must be greater than 2V during the initial power-up, and the MTP programming must be completed.

Toggling EN/SYNCI on and off will not reload the MTP registers into the I²C registers.

The I²C register and MTP table are correlated to each other. The MTP table can be accessed and programmed through the I²C interface up to three times.

After buck 1 and buck 4 power up, the SoC programs the MP5470B I²C register and MTP. Refer to the I²C Bus Slave Address section on page 29 for steps on identifying a valid slave address. When SoC writes to the I²C register, the I²C register can take effect immediately, or can be burned via the MTP. VCC rises up to 5.2V when the MTP is programmed. To protect the power device, the buck regulators shut down when burning the MTP fuse. After MTP programming is done, the buck regulators start up sequentially. In normal buck operation, the I²C master can read and write the register's data in line. Figure 5 shows the timing graph during the PMIC start-up period.

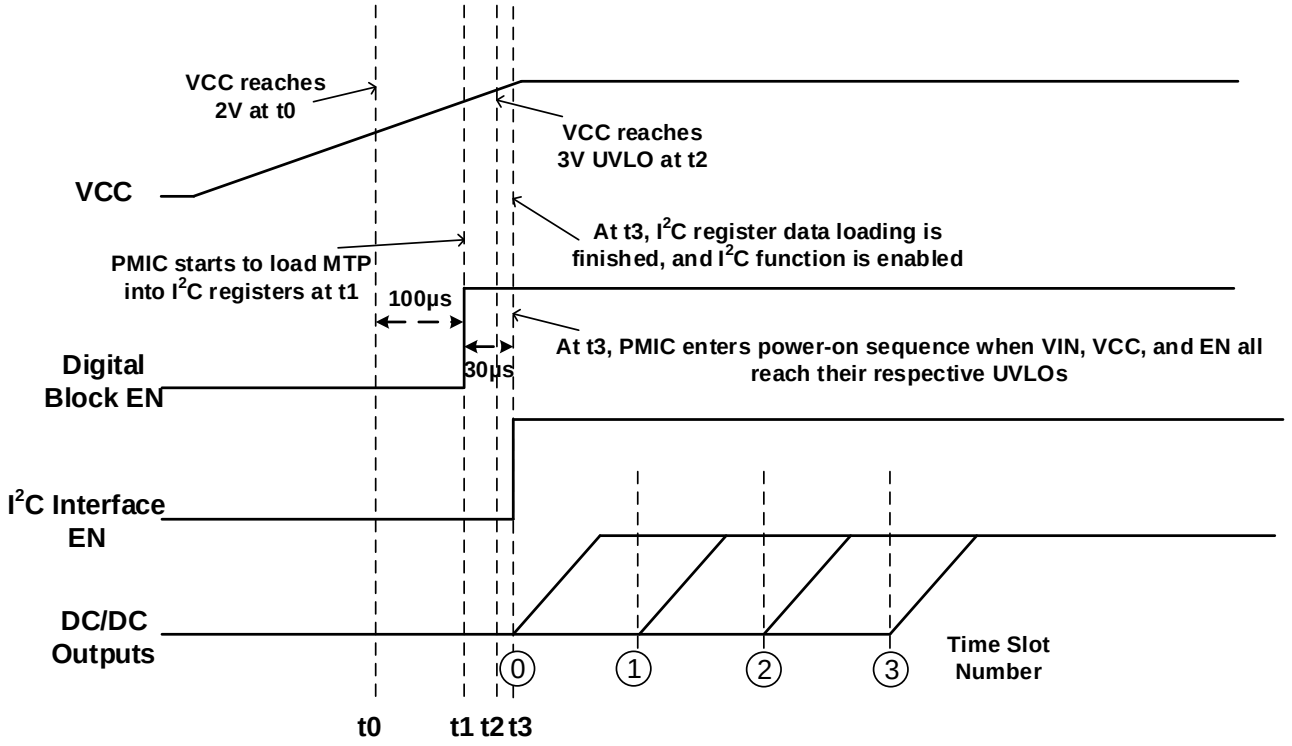


Figure 5: Power-On Timing Graph with MTP-Burned IC

Safety Consideration for Writing the MTP

Several protection items can reduce the failure rate in MTP writing. There are three steps to take before writing the MTP registers:

1. Refer to the MTP table. The MTP_program bit should be set to 1. The I²C register is locked to prevent a write operation until the MTP programming finishes. The SoC can read the I²C register during this period.
2. The MP5470B checks the MTP burning power supply. If it is greater than 5.1V, then continue the MTP write operation. Otherwise, abort and unlock the I²C write protection.
3. The MP5470B calculates the sum of all related I²C registers to be burned in the MTP register, and generates a 16-bit checksum data. Checksum is not truly a sum of all I²C registers, but rather is an arithmetic value that combines all data. The checksum results are also written to the MTP register.

After the MTP write operation finishes, a delay (typically 100ms) must pass before the MP5470B sets the MTP_program bit to 0 and the I²C register write protection is unlocked. The SoC can read the I²C register. If the MTP_program bit goes to 0, then the MTP programming is complete.

After the MTP write operation is completed, the SoC can read the MTP register data to verify that the correct value is saved into the MTP registers. If anything is incorrect, the SoC writes to the MTP again.

During VIN power-up, before loading the MTP data into the I²C register, the MP5470B performs a checksum calculation for all related MTP registers and compares the result with the checksum byte. If they match, then the MTP data is loaded into the I²C register. Otherwise, the I²C register uses a hard-coded default value. There is an I²C register flag bit that indicates the checksum error.

MTP Table

	REG (0x)	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Buck1	40			Soft-start delay 1		Additional phase delay 1	Soft-start time 1		
	41	Vout_Limit_EN1	Mode 1	Current limit 1		VOUT_OVP_EN1	Phase delay select 1		VOUT_Dis_EN1
	42	Vout_Select 1	V_Ref1						
Buck2	43			Soft-start delay 2		Additional phase delay 2	Soft-start time 2		
	44	Vout_Limit_EN2	Mode 2	Current limit 2		VOUT_OVP_EN2	Phase delay select 2		VOUT_Dis_EN2
	45	Vout_Select 2	V_Ref2						
Buck3	46			Soft-start delay 3		Additional phase delay 3	Soft-start time 3		
	47	Vout_Limit_EN3	Mode 3	Current limit 3		VOUT_OVP_EN3	Phase delay select 3		VOUT_Dis_EN3
	48	Vout_Select 3	V_Ref3						
Buck4	49			Soft-start delay 4		Additional phase delay 4	Soft-start time 4		
	4A	Vout_Limit_EN4	Mode 4	Current limit 4		VOUT_OVP_EN4	Phase delay select 4		VOUT_Dis_EN4
	4B	Vout_Select 4	V_Ref4						
System	4C	EN1	EN2	EN3	EN4		UVLO		OP_BIT
System	4D	FREQ		Shutdown_Delay_EN	I²C slave address				
System	4E	ADD_PG_OP_SYNCOUT			PG_Delay			Parallel_2	Parallel_1
System	4F	MTP configure code. “0x00” refers to the standard MP5470B, and “0x01” refers to the MP5470B-0001 part number.							
System	50	MTP revision number: The MTP value may need to be updated after a period of time. This bit stores the revision number.							
System	51	Checksum 1 of MTP register 0x40 to 0x50: • When writing the I²C register’s data into the MTP, the MP5470B performs a checksum of all related I²C registers and writes the result in this bit and the next byte. • During power-up, the MP5470B calculates and compares the MTP cell’s data with 0x51-0x52 register’s content. If they match, then load the MTP data to the I²C register. Otherwise, the I²C register ignores the presented MTP data and uses the default setting.							
System	52	Checksum 2 of MTP register 0x40 to 0x50.							

MTP Table Description

<table>
<tr><th>NAME</th><th>BIT</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>Soft-start delay</td><td>D[5:4]</td><td>Soft-start delay 1 = 10
Soft-start delay 2 = 10
Soft-start delay 3 = 10
Soft-start delay 4 = 10</td><td>The delay time between when EN goes high and the system is ready to when buck V_{OUT} starts to ramp up. 2 bits can set four different values:
D[5:4] = 00: 0ms, time slot 0
D[5:4] = 01: 1ms, time slot 1
D[5:4] = 10: 2ms, time slot 2
D[5:4] = 11: 3ms, time slot 3
Refer to the Power-On Sequence section on page 31 for the time slot definition.</td></tr>
<tr><td>Additional phase delay</td><td>D[3]</td><td>Delay 1 = 0
Delay 2 = 0
Delay 3 = 0
Delay 4 = 0</td><td>Set to 1, this bit can add a 100ns phase delay to the buck high-side switch turn-on edge.</td></tr>
<tr><td>Soft-start time</td><td>D[2:0]</td><td>Soft-start time 1 = 101
Soft-start time 2 = 110
Soft-start time 3 = 100
Soft-start time 4 = 110</td><td>This bit is the soft-start slew rate setting bit of each buck regulator. The below slew rate is the internal reference voltage slew rate. If the Vout_Select bit is set to 1, the V_{OUT} slew rate is 3 (three times the Vout_Select bit).
D[2:0] = 000: 2.67mV/µs soft-start slew rate
D[2:0] = 001: 1.6mV/µs soft-start slew rate
D[2:0] = 010: 1mV/µs soft-start slew rate
D[2:0] = 011: 0.67mV/µs soft-start slew rate
D[2:0] = 100: 0.4mV/µs soft-start slew rate
D[2:0] = 101: 0.25mV/µs soft-start slew rate
D[2:0] = 110: 0.167mV/µs soft-start slew rate
D[2:0] = 111: 0.1mV/µs soft-start slew rate
For available soft-start times vs. V_{OUT}, refer to the table below.
Soft-start time (ms): V_{OUT} from 0% to 100%, Vout_Select = 1 when V_{OUT} > 1.8V.
<table>
<tr><th>3 bits</th><th>Slew rate (mV/µs)</th><th>V_{OUT} = 5.01V</th><th>V_{OUT} = 3.3V</th><th>V_{OUT} = 2.5V</th><th>V_{OUT} = 1.8V</th><th>V_{OUT} = 1V</th><th>V_{OUT} = 0.6V</th></tr>
<tr><td>000</td><td>2.67</td><td>0.6</td><td>0.4</td><td>0.3</td><td>0.7</td><td>0.4</td><td>0.2</td></tr>
<tr><td>001</td><td>1.6</td><td>1.0</td><td>0.7</td><td>0.5</td><td>1.1</td><td>0.6</td><td>0.4</td></tr>
<tr><td>010</td><td>1</td><td>1.7</td><td>1.1</td><td>0.8</td><td>1.8</td><td>1.0</td><td>0.6</td></tr>
<tr><td>011</td><td>0.67</td><td>2.5</td><td>1.6</td><td>1.2</td><td>2.7</td><td>1.5</td><td>0.9</td></tr>
<tr><td>100</td><td>0.4</td><td>4.2</td><td>2.8</td><td>2.1</td><td>4.5</td><td>2.5</td><td>1.5</td></tr>
<tr><td>101</td><td>0.25</td><td>6.7</td><td>4.4</td><td>3.3</td><td>7.2</td><td>4.0</td><td>2.4</td></tr>
<tr><td>110</td><td>0.167</td><td>10.0</td><td>6.6</td><td>5.0</td><td>10.8</td><td>6.0</td><td>3.6</td></tr>
<tr><td>111</td><td>0.1</td><td>16.7</td><td>11.0</td><td>8.3</td><td>18.0</td><td>10.0</td><td>6.0</td></tr>
</table>
</td></tr>
</table>

Vout_Limit_EN	D[7]	Vout_Limit_EN1 = 1 Vout_Limit_EN2 = 1 Vout_Limit_EN3 = 1 Vout_Limit_EN4 = 0	Limits the maximum output voltage of each power rail. D[7] = 0: The maximum output voltage has no limit and depends on the I²C V_{OUT} setting, maximum duty cycle, or absolute voltage limit D[7] = 1: The maximum output voltage is limited to 1.830V (FB voltage)
Mode	D[6]	Mode 1 = 0 Mode 2 = 0 Mode 3 = 0 Mode 4 = 0	Selects the mode (auto PFM/PWM mode or forced PWM mode). D[6] = 0: Auto PFM/PWM mode D[6] = 1: Forced PWM mode
Current limit	D[5:4]	Current limit 1 = 10 Current limit 2 = 10 Current limit 3 = 01 Current limit 4 = 01	Sets the current limit of buck 1 to buck 4. D[5:4] = 00: 2A valley-current limit for 1A output current application D[5:4] = 01: 3A valley-current limit for 2A output current application D[5:4] = 10: 4.2A valley-current limit for 3A output current application D[5:4] = 11: 5A valley-current limit for 4A peak output current application
Phase delay select	D[2:1]	Phase delay select 1 = 00 Phase delay select 2 = 01 Phase delay select 3 = 10 Phase delay select 4 = 11	Sets phase delay. 00: 0° delay 01: 90° delay 10: 180° delay 11: 270° delay
VOUT_OVP_EN	D[3]	VOUT_OVP_EN1 = 0 VOUT_OVP_EN2 = 0 VOUT_OVP_EN3 = 0 VOUT_OVP_EN4 = 0	Enable bit of buck 1 to buck 4's output OVP function. D[3] = 0: Disable OVP function D[3] = 1: Enable OVP function
VOUT_DIS_EN	D[0]	VOUT_DIS_EN1 = 1 VOUT_DIS_EN2 = 1 VOUT_DIS_EN3 = 1 VOUT_DIS_EN4 = 1	Enable bit of buck 1 to buck 4's output discharge function. D[0] = 0: Disable discharge function D[0] = 1: Enable discharge function

Vout_Select	D[7]	Vout_Select 1 = 0 Vout_Select 2 = 0 Vout_Select 3 = 0 Vout_Select 4 = 0	Selects the internal feedback divider ratio. D[7] = 0: The FB voltage is fed directly to the error amplifier. V_{FB} equals V_{REF} D[7] = 1: The FB voltage is divided by 3 and compared with V_{REF}. V_{FB} is three times V_{REF} Note: If the AVS function is used, D[7] is set to 0.
V_Ref	D[6:0]	V_Ref1 = 0.700V V_Ref2 = 0.780V V_Ref3 = 0.780V V_Ref4 = 0.780V	Sets the internal reference voltage from 550mV to 1.82V, 10mV per step. The voltage slew rate is fixed at 2.6mV/µs. D[6:0] = 000 0000: 550mV D[6:0] = 000 0001: 560mV ... D[6:0] = 111 1111: 1.82V
EN1, EN2, EN3, EN4	D[7:4]	EN1 = 1 EN2 = 1 EN3 = 1 EN4 = 1	Enable bit of each buck regulator. 1: Enable 0: Disable
UVLO	D[2:1]	D[2:1] = 10	Sets the input UVLO threshold of VIN1 and VIN2. 00: UVLO rising is 3.5V 01: UVLO rising is 4.5V 10: UVLO rising is 5.8V 11: UVLO rising is 8.5V
OP_BIT	D[0]	D[0] = 0	When the ADD_PG_OP_SYNCOUT bit is set to 10, GPIO is configured as an output port. OP_BIT sets the output port to logic high or low. This bit is only valid when ADD_PG_OP_SYNCOUT = 10. Otherwise, this bit is not needed. 0: GPIO is pulled low with a certain resistance 1: GPIO is an open drain
FREQ	D[7:6]	D[7:6] = 01: 800kHz	Frequency set of the buck regulator. The buck 1 to buck 4 switching frequency is always the same, and cannot support different frequencies from buck 1 to buck 4. D[7:6] = 00: 533kHz D[7:6] = 01: 800kHz D[7:6] = 10: 1060kHz D[7:6] = 11: 1600kHz
Shutdown_ Delay_EN	D[5]	D[5] = 0	The MP5470B offers two kinds of shutdown sequences when EN/SYNCI goes low. The first is a buck 1 to buck 4 shutdown following the reverse of the power-on sequence. The second is when buck 1 to buck 4 shut down at the same time. See the detailed description of the shutdown sequence on page 31. D[5] = 0: Shut down at the same time D[5] = 1: Shutdown sequence is the reverse of the power-on sequence
I²C slave address	D[4:0]	D[4:0] = 01000	Sets the A5 to A1 bits of the slave I²C address. See the I²C bus slave address section on page 29.

ADD_PG_OP_SYNCOUT	D[7:6]	D[7:6] = 00	Sets GPIO's function. D[7:6] = 00: GPIO is configured as ADD, which sets the I²C slave address D[7:6] = 01: GPIO is configured as PG, which indicates the buck regulator's power status D[7:6] = 10: GPIO is an OP (output port) and works in output mode. OP is an open-drain structure, and its logic is controlled by the I²C register bit. The MTP OP_BIT bit sets the default status D[7:6] = 11: GPIO is a SYNC output, which outputs a clock signal to synchronize the downstream device's switching frequency. SYNC output is an open-drain structure
PG_Delay	D[4:2]	D[4:2] = 000	Sets the PG delay timer. 000: 0.2ms 001: 5ms 010: 25ms 011: 75ms 100: 200ms
Parallel_2	D[1]	0	Sets buck 3 and buck 4 to work in parallel mode. FB3 and FB4 are paralleled as the feedback pin. The default value is 0. After entering parallel mode, buck 4's I²C/MTP register is invalid. The current limit is double buck 3's register setting. 0: Non-parallel mode 1: Parallel mode
Parallel_1	D[0]	0	Sets buck 1 and buck 2 to work in parallel mode. FB1 and FB2 are paralleled as the feedback pin. The default value is 0. After entering parallel mode, buck 2's I²C/MTP register is invalid. The current limit is double buck 1's register setting. 0: Non-parallel mode 1: Parallel mode

Vref1 to Vref4, Reference Voltage Truth Table

D[6:0]	V_{REF} (mV)	D[6:0]	V_{REF} (mV)	D[6:0]	V_{REF} (mV)
0000000	550	0101011	980	1010110	1410
0000001	560	0101100	990	1010111	1420
0000010	570	0101101	1000	1011000	1430
0000011	580	0101110	1010	1011001	1440
0000100	590	0101111	1020	1011010	1450
0000101	600	0110000	1030	1011011	1460
0000110	610	0110001	1040	1011100	1470
0000111	620	0110010	1050	1011101	1480
0001000	630	0110011	1060	1011110	1490
0001001	640	0110100	1070	1011111	1500
0001010	650	0110101	1080	1100000	1510
0001011	660	0110110	1090	1100001	1520
0001100	670	0110111	1100	1100010	1530
0001101	680	0111000	1110	1100011	1540
0001110	690	0111001	1120	1100100	1550
0001111	700	0111010	1130	1100101	1560
0010000	710	0111011	1140	1100110	1570
0010001	720	0111100	1150	1100111	1580
0010010	730	0111101	1160	1101000	1590
0010011	740	0111110	1170	1101001	1600
0010100	750	0111111	1180	1101010	1610
0010101	760	1000000	1190	1101011	1620
0010110	770	1000001	1200	1101100	1630
0010111	780	1000010	1210	1101101	1640
0011000	790	1000011	1220	1101110	1650
0011001	800	1000100	1230	1101111	1660
0011010	810	1000101	1240	1110000	1670
0011011	820	1000110	1250	1110001	1680
0011100	830	1000111	1260	1110010	1690
0011101	840	1001000	1270	1110011	1700
0011110	850	1001001	1280	1110100	1710
0011111	860	1001010	1290	1110101	1720
0100000	870	1001011	1300	1110110	1730
0100001	880	1001100	1310	1110111	1740
0100010	890	1001101	1320	1111000	1750
0100011	900	1001110	1330	1111001	1760
0100100	910	1001111	1340	1111010	1770
0100101	920	1010000	1350	1111011	1780
0100110	930	1010001	1360	1111100	1790

0100111	940	1010010	1370	1111101	1800
0101000	950	1010011	1380	1111110	1810
0101001	960	1010100	1390	1111111	1820
0101010	970	1010101	1400		

Output Voltage Setting

FB1 to FB4 are the output voltage feedback pins. FBx can be connected to the buck output directly, or connected to a resistor divider network for a higher output voltage. If connecting FB to V_{OUT} directly (using buck 1 as an example), the I²C bit Vout_Select1 can set FB1 to equal Ref1, or to equal 3 * Ref1. The table above shows the Ref1 voltage range (0.55V to 1.82V). After setting the Vout_Select1 bit to 1, the buck 1 output voltage range changes to 1.65V to 5.46V.

For a better load transient response, set V_{REF} to a lower value and use a feedback resistor divider to set the final V_{OUT}. In this case, a feed-forward capacitor can be added to sense the V_{OUT} change more quickly. This operation is similar to the feedback configuration shown in Figure 6, but without AVS.

If connecting FBx to the resistor divider network (using buck 1 as an example), the I²C bit Vout_Select1 = 0 can set FB1 to equal Ref1. The table above shows the Ref1 voltage range (0.55V to 1.82V). The buck 1 output voltage can be calculated with Equation (1):

$$V_{O1} = \frac{R1 + R2}{R2} \times V_{ref1} \quad (1)$$

If using a resistor divider, the AVS function is supported. The direct V_{OUT}-to-FB path should be cut off. If the AVS function is chosen, set Vout_Select = 0.

During I²C DVS, the voltage change slew rate is 2.6mV/μs when Vout_Select = 0. The slew rate is 7.8mV/μs when Vout_Select = 1.

The Vout_Limit_EN bit can clamp the maximum output voltage to 1.830V (FB voltage, blank the Vout_Select bit).

The absolute maximum output voltage is limited to 7V or the maximum duty cycle.

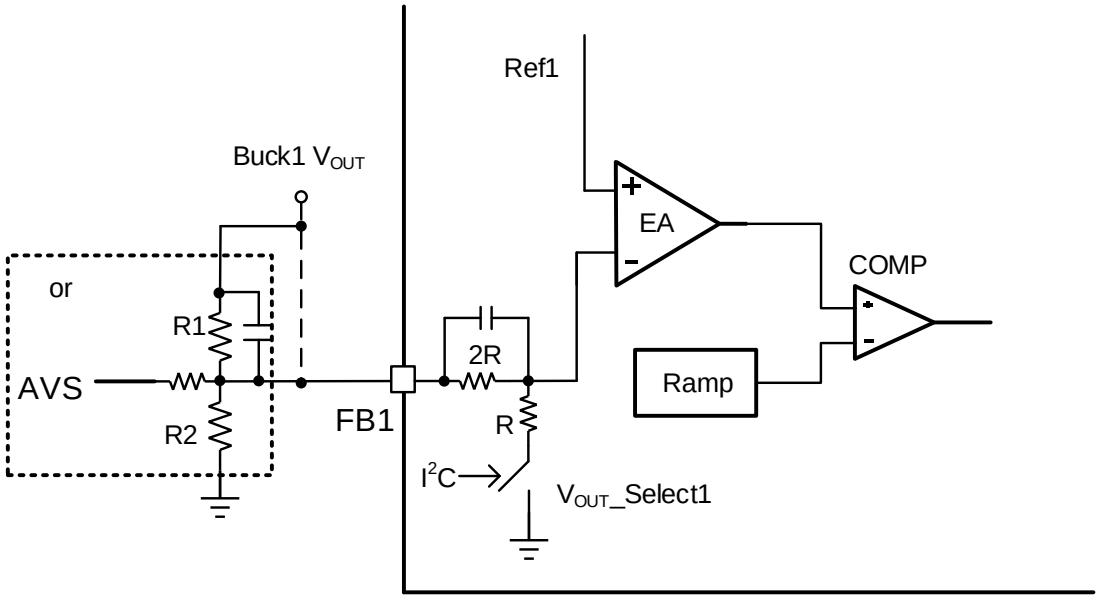


Figure 6: Output Voltage Setting

I²C Register Map

	REG (0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Buck1	00	R/W			Soft-start delay 1		Additional phase delay 1	Soft-start time 1		
	01	R/W	Vout_ Limit_EN1	Mode 1	Current limit 1		VOUT_OVP _EN1	Phase delay select 1		VOUT_Dis _EN1
	02	R/W	Vout_ Select1	V_Ref1						
Buck2	03	R/W			Soft-start delay 2		Additional phase delay 2	Soft-start time 2		
	04	R/W	Vout_ Limit_EN2	Mode 2	Current limit 2		VOUT_OVP _EN2	Phase delay select 2		VOUT_Dis _EN2
	05	R/W	Vout_ Select2	V_Ref2						
Buck3	06	R/W			Soft-start delay 3		Additional phase delay 3	Soft-start time 3		
	07	R/W	Vout_ Limit_EN3	Mode 3	Current limit 3		VOUT_OVP _EN3	Phase delay select 3		VOUT_Dis _EN3
	08	R/W	Vout_ Select3	V_Ref3						
Buck4	09	R/W			Soft-start delay 4		Additional phase delay 4	Soft-start time 4		
	0A	R/W	Vout_ Limit_EN4	Mode 4	Current limit 4		VOUT_OVP _EN4	Phase delay select 4		VOUT_Dis _EN4
	0B	R/W	Vout_ Select4	V_Ref4						
System	0C	R/W	EN1	EN2	EN3	EN4		UVLO		OP_BIT
System	0D	R/W	FREQ (533kHz/800kHz/ 1.06MHz/1.6MHz)		Shutdown _Delay_ EN	I²C slave address				
System	0E	R/W	ADD_PG_OP_ SYNCOUT		MTP_ Program	PG_Delay			Parallel_2*	Parallel_1*
System	0F	R/W	MTP configure code. “0x00” refers to the standard MP5470B. “0x01” refers to the MP5470B-0001 part number.							
System	10	R/W	MTP revision number: The MTP value may need to be updated after a period of time. This bit stores the revision number.							
System	11	W	MTP program password							
Status	12	R	PG1	PG2	PG3	PG4	OT warning	OT protection		
System	13	R	Vendor ID (1000)				Checksum flag	Current MTP page index		

Note: The parallel_1 and _2 bits only take effect when EN/SYNCI turns on. After EN/SYNCI turns on, changing these bits will not change the parallel mode.

Description of Register Bits

Most register bits share the same description in the MTP table. The tables below list the description of different register bits. The I²C register's default value is decided by the MTP table.

All I²C registers can be reset by VCC UVLO. VIN2 < UVLO does not reset the registers. When VIN2 UVLO occurs, buck 2 and buck 3 are off. They turn on again when VIN2 UVLO recovers, but cannot follow the power-on sequence. They turn on at the same time once VIN2 UVLO is released.

Over-temperature protection (OTP) will not reset the I²C register.

1. REG 0x0E System

NAME	BITS	DESCRIPTION
MTP_Program	D[5]	The default value of this bit is 0. If D[5] = 1, the I²C register's data is burned to the MTP table. Once the system starts to burn I²C register data to the MTP table, the I²C register write operation is locked (NACK), but the read operation is not locked until the MTP write operation finishes (typically 100ms). The system auto-sets D[5] to 0 to wait for the next MTP burning command. The current MTP page index will add one after MTP programming is done. When programming MTP, rewrite each I²C register (0x00 to 0x10), even if keeping the same values as before.

2. REG 0x11 System

NAME	BITS	DESCRIPTION
MTP program password	D[7:0]	To access the MTP_PROGRAM bit, the correct password should be entered into this register.

3. REG 0x12 Status

NAME	BITS	DESCRIPTION	
PG1	D[7]	Power good indicator for buck 1. 1: Power is good 0: Power is not good	These bits always reflect the current state of the device.
PG2	D[6]	Power good indicator for buck 2.	
PG3	D[5]	Power good indicator for buck 3.	
PG4	D[4]	Power good indicator for buck 4.	
OT warning	D[3]	Die temperature early warning bit. When the bit is high, the die temperature is above 120°C.	
OT protection	D[2]	Over-temperature condition indication. When the bit is high, the IC is in thermal shutdown.	

4. REG 0x13 System

NAME	BITS	DESCRIPTION
Checksum flag	D[3]	D[3] = 1: The current MTP page has a CRC or checksum error D[3] = 0: The current MTP's data passes the CRC check The checksum flag only works after MTP has been programmed. For a part that has never been MTP-programmed (new part), this bit is always high.
Current MTP page index	D[2:0]	D[2:0] stores the current MTP page index information. 000: Default page. There are three pages that can be used 001: First page 011: Third page

I²C Bus Slave Address

The slave address is 7 bits followed by an eighth data direction bit (read or write). There are two ways to program the I²C slave address:

1. Use an external GPIO when it is configured as an ADD pin. In this way, the I²C slave address is decided by both ADD and the I²C register setting.
2. Use the I²C/MTP register to set the I²C slave address. When the external GPIO is set to a non-ADD function, the I²C slave address is fully controlled by the I²C/MTP register setting.

Use ADD to Set the I²C Slave Address

If GPIO is configured as an ADD pin, it can be used to program four different slave addresses. A resistor divider from VCC to GND can achieve an accurate reference voltage. Connect ADD to this reference voltage to set different I²C addresses. The internal circuit changes the I²C address accordingly. Under this control method, the lower 2 bits of the I²C address are determined by the ADD voltage (bits A1 and A2), and the higher 3 bits (A3, A4, and A5) are determined by the I²C/MTP register setting. Table 1 shows the four voltage thresholds for four I²C addresses and recommended setting resistors.

Table1: I²C Slave Address Set by ADD Voltage (with I²C Address Software Default Setting)

ADD Voltage	ADD Upper Resistor R1 (kΩ)	ADD Lower Resistor R2 (kΩ)	I²C Address	
			Binary	Hex
<20% V_{CC}	No connection	100	1101 0**00**	68H
33% V_{CC} to 45% V_{CC}	500	300	1101 0**01**	69H
56% V_{CC} to 71% V_{CC}	300	500	1101 0**10**	6AH
>80% V_{CC}	100	No connection	1101 0**11**	6BH

Use I²C or MTP to set the I²C Slave Address

When the external GPIO is set to a non-ADD function, the MP5470B can still offer a programmable I²C slave address via the I²C or MTP. The I²C register REG0D D[4:0] or MTP register REG4D D[4:0] can program the A5, A4, A3, A2, and A1 bits (see Table 2).

*These bits are programmable by the MTP e-fuse or I²C register. The higher 2 bits (A7 and A6) are fixed to 1 internally.

Table 2: I²C Slave Address Set by I²C/MTP Register Setting

	A7	A6	A5	A4	A3	A2	A1
Setting Value	1	1	0*	1*	0*	0*	0*

By default, the slave address is 0x68, A[7:1] = 1101 000.

When the I²C register's slave address bits are changed, the new address takes effect immediately. The I²C master should use a new slave address to continue communication.

Example of a Three-Piece MP5470B Application in One System

Figure 7 shows a system-level block diagram using three MP5470B devices. From U1 to U3, the GPIO pin is configured as ADD to set different I²C slave addresses.

During the initial input power-up, U1's EN/SYNCI pin is pulled up automatically, enabling the OUT1 and OUT4 outputs. U2 and U3's buck regulators are off by default by pulling the EN pins to ground. The SoC gets basic power from OUT1 and OUT4 before its I²C master block can begin working. The SoC checks U1 to U3's I²C register values and configures them to the correct one if needed. The I²C register value is saved to the MTP. Afterward, the SoC GPIO1 and GPIO2 output a high signal to enable U2 and U3. The rest of the U1 to U3 power rails are turned on sequentially.

The SoC can write the register MTP revision number to mark that the MP5470B has been programmed. At the next input start-up, the SoC reads the MTP revision number bit to check if it equals the correct value or not. The SoC checks the page index and CRC flag as well. If there are no errors, the SoC enters normal boot mode; otherwise, the SoC reprograms the MTP.

If U2's GPIO pin is changed from ADD to PG, the I²C slave address changes to the I²C register's value automatically. To complete PG and ADD's external component connection, pull GPIO up with a resistor to VCC or 3.3V.

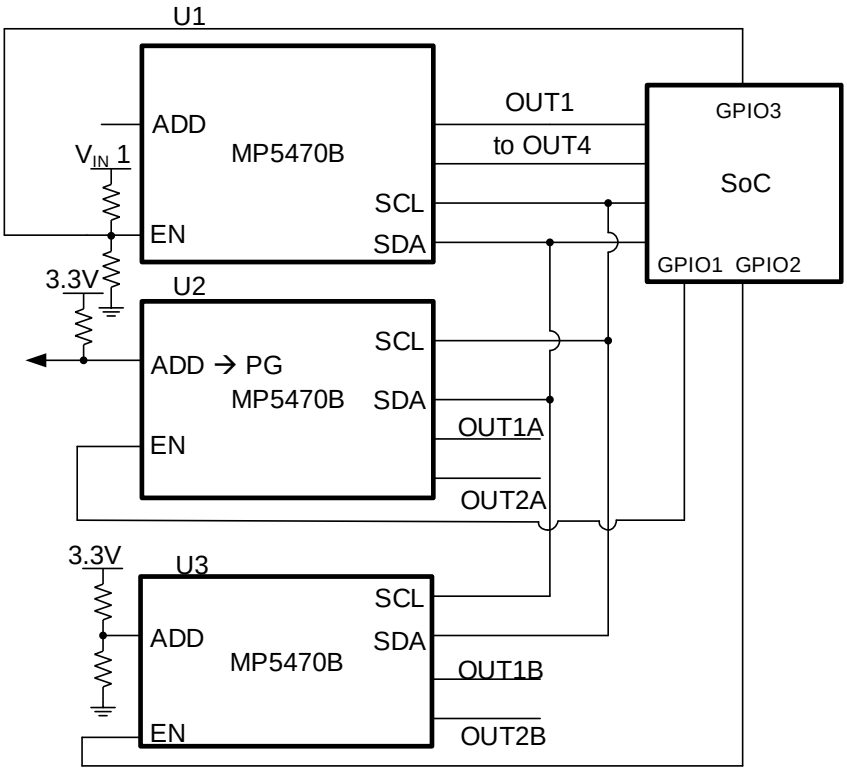


Figure 7: Multiple PMIC Usages in One System

POWER CONTROL

State Machine Diagram of Buck Switchers

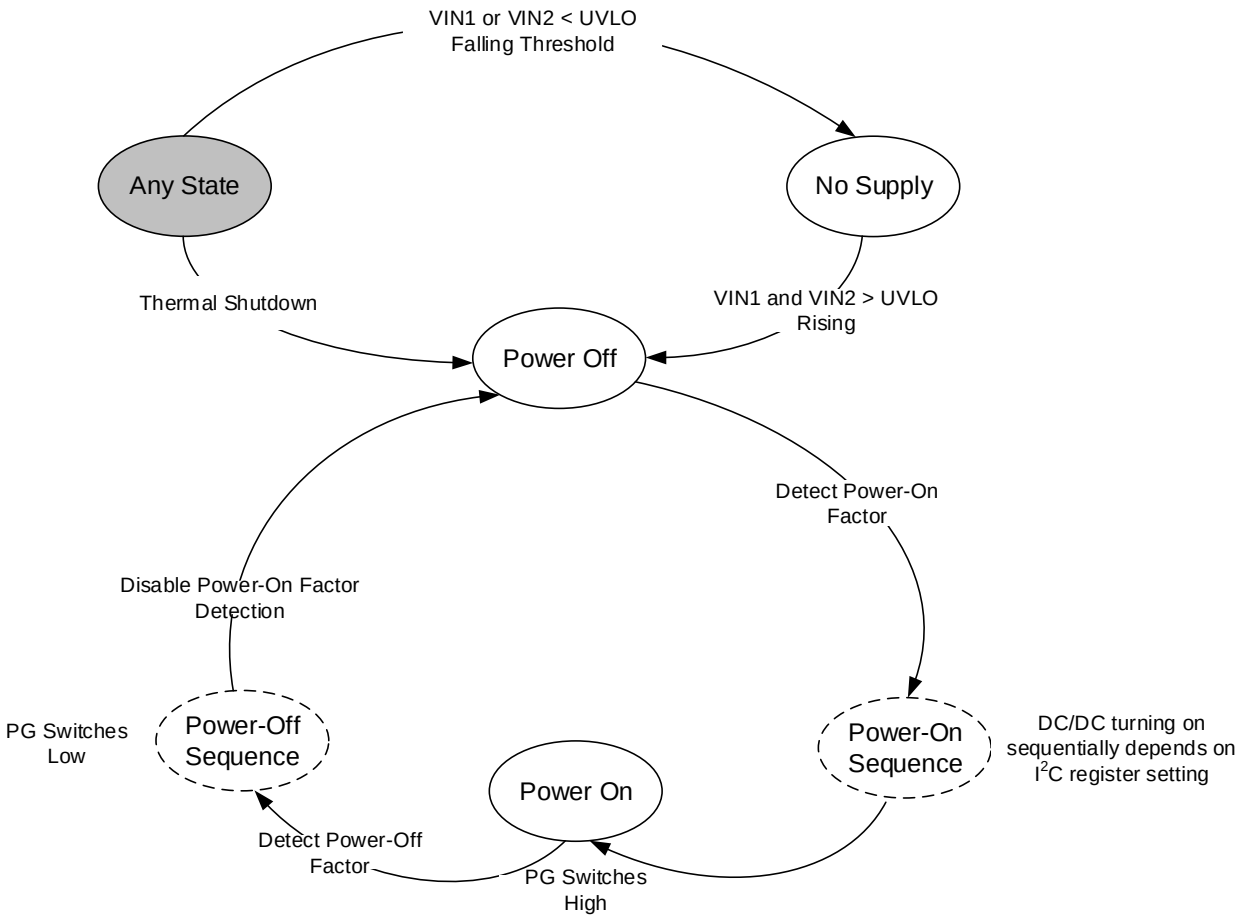


Figure 8: Power Control State Machine Diagram

State Machine Description

The state machine has the following statuses:

No Supply

The PMIC's input pin has a UVLO detection circuit. If the input voltage (VIN1) is lower than the UVLO rising threshold, all of the PMIC's functions are disabled. If VIN2 is lower than the UVLO rising threshold, buck 2 and buck 3 are disabled.

Power Off

All buck regulators are turned off. In this state, the I²C and MTP are still active and the PMIC is always monitoring the power-on factor. Once the power-on factor is detected, the state changes to the power-on sequence.

Power-On Sequence

Buck 1 to buck 4 turn on sequentially according to the order programmed by the MTP e-fuse. If the power-off factor is detected during the power-on sequence, the PMIC changes back to the power-off state.

Power On

Buck 1 to buck 4 are turned on. The PG output switches high. In this state, the PMIC monitors the power-off factor continuously.

Power-Off Sequence

The PMIC changes to this state when it detects the power-off factor in the power-on state. Buck 1 to buck 4 either turn off sequentially in the reverse order of the power-on sequence, or turn off at the same time, depending on the setting of the Shutdown_Delay_EN bit.

Power-On Factor

The PMIC has the following power-on factors:

EN/SYNCI Pin

If EN/SYNCI pulls high, the system changes from the power-off state to the power-on sequence. The related EN bit determines each buck's on or off state.

Thermal Recovery

If the MP5470B is in a power-off state due to the die's temperature exceeding the thermal protection threshold, the PMIC enters the power-on sequence again when the die's temperature decreases.

Power-On Sequence

There are four slots for power-on sequence timing. All buck regulators can be programmed to the power-on time slots 0 to 3 by the MTP e-fuse (see Figure 9).

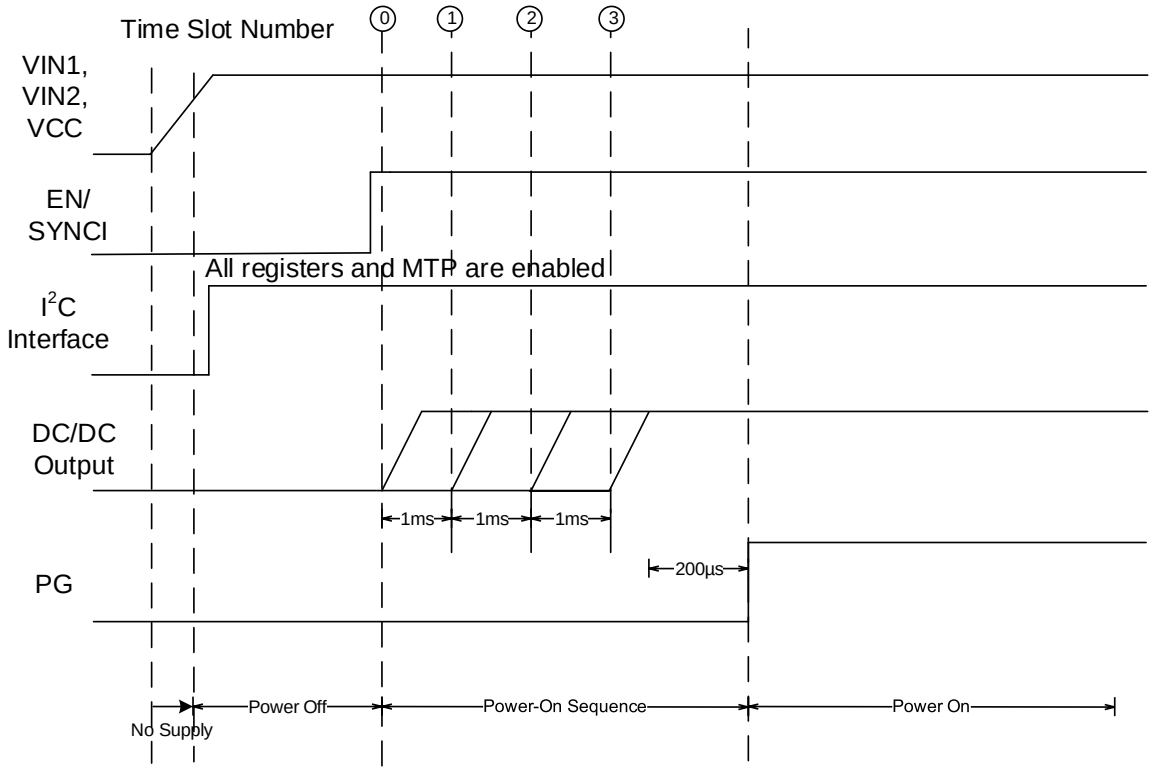


Figure 9: Power-On Sequence

Buck Regulator Turn-On

The MP5470B provides a programmable power-on sequence. The MTP configuration table has bits to set the time slot number (start-up delay timer) for each channel. The default power-on sequence is shown in the default MTP configuration table.

Power-Off Factor

EN/SYNCI – Hardware-Initiated Power-Off

The MP5470B supports a controlled power-off through the EN/SYNCI pin. When EN/SYNCI is pulled low, the system enters the power-off sequence.

Power-Off Sequence

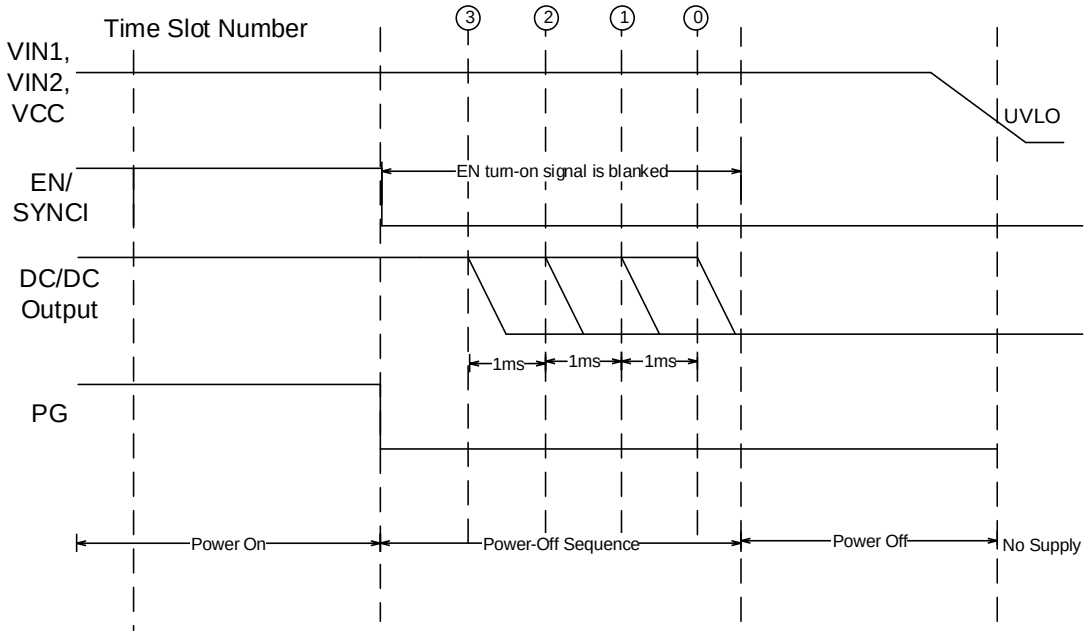


Figure 10: Power-Off Sequence when Shutdown_Delay_EN = 1

PG is pulled low before the DC/DC output starts turning off. The DC/DC output power-off sequence is the reverse order of the power-on sequence when Shutdown_Delay_EN is set to 1 (see Figure 10).

To discharge the output voltage fully, the EN/SYNCI signal is blanked during the power-off sequence period. Within this power-off sequence period, the MP5470B continues working in output discharge mode, regardless of whether the external EN/SYNCI pin is pulled high or low.

All the DC/DC outputs power off at the same time when Shutdown_Delay_EN is set to 0 (see Figure 11).

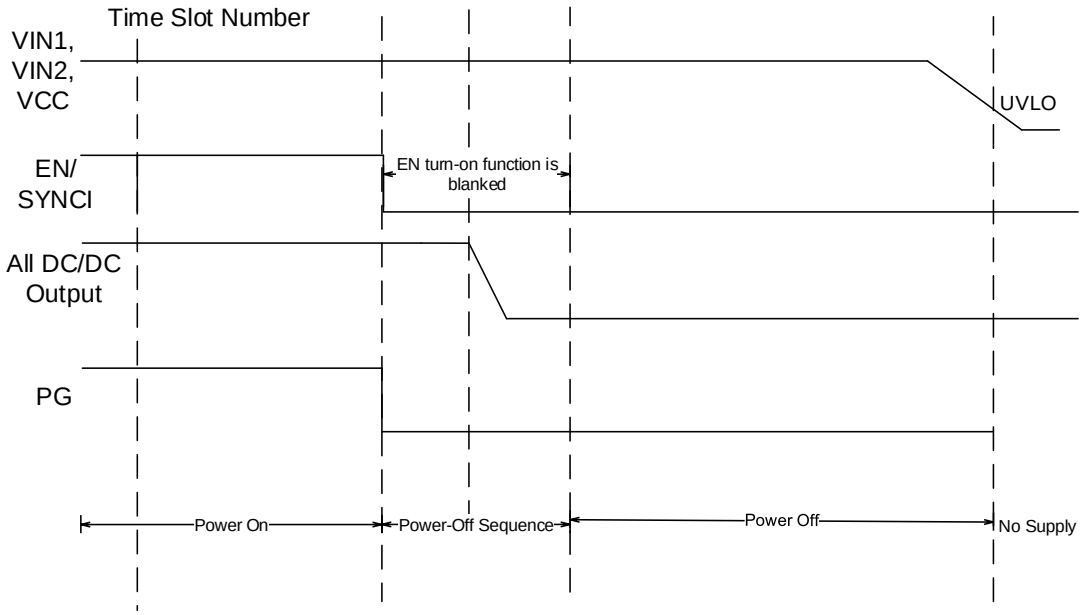


Figure 11: Power-Off Sequence when Shutdown_Delay_EN = 0

Shutdown Sequence

When the input voltage is below the UVLO falling threshold or the IC is over-temperature, the PMIC enters the shutdown sequence. All of the bucks turn off at the same time (see Figure 12).

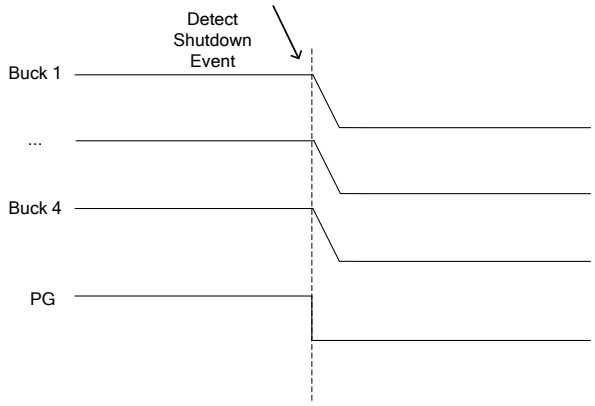


Figure 12: Shutdown Sequence

Thermal Warning and Shutdown

Thermal warning and shutdown prevent the part from operating at exceedingly high temperatures. When the silicon die temperature exceeds 120°C, the MP5470B sets the OT warning bit to 1.

If the die temperature exceeds 160°C, the system enters the shutdown sequence. When the temperature recovers to 140°C, the regulator enters the power-on sequence.

I²C INTERFACE

I²C Serial Interface Description

The I²C is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connected to the line, a master device generates the SCL signal and device address, and arranges the communication sequence. The MP5470B interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, or other parameters can be controlled by the I²C interface instantaneously.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 13).

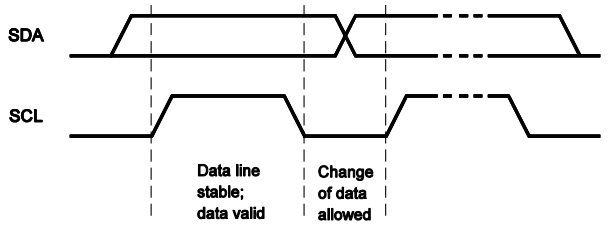


Figure 13: Bit Transfer on the I²C Bus

Start and stop are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 14).

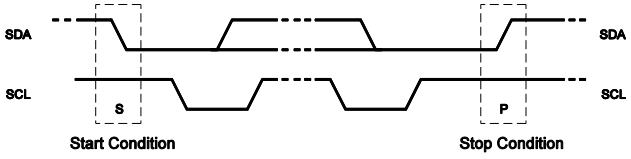


Figure 14: Start and Stop Conditions

Start (s) and stop (P) conditions are always generated by the master. The bus is considered to be busy after the start condition. The bus is considered free again once a minimum of 4.7µs passes after the stop condition. The bus remains busy if a repeated start (Sr) is generated instead of a stop condition. The start and repeated start conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8 bits long. Each byte must be followed by an acknowledge (ACK) bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable-low during the high period of this clock pulse.

Figure 15 shows the format that data transfers follow. After the start condition, a slave address is sent. This address is 7 bits long, followed by an eighth data direction bit (R/W). A 0 indicates a write transmission (Wr), and a 1 indicates a read request for data (R). A data transfer is always terminated by a stop condition generated by the master. However, if the master still wishes to communicate on the bus, it can generate a repeated start condition and address another slave without first generating a stop condition.

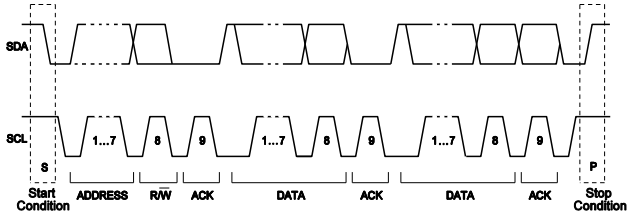
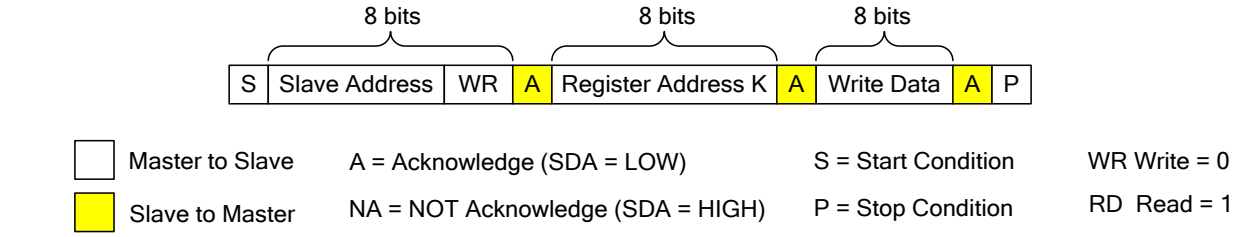


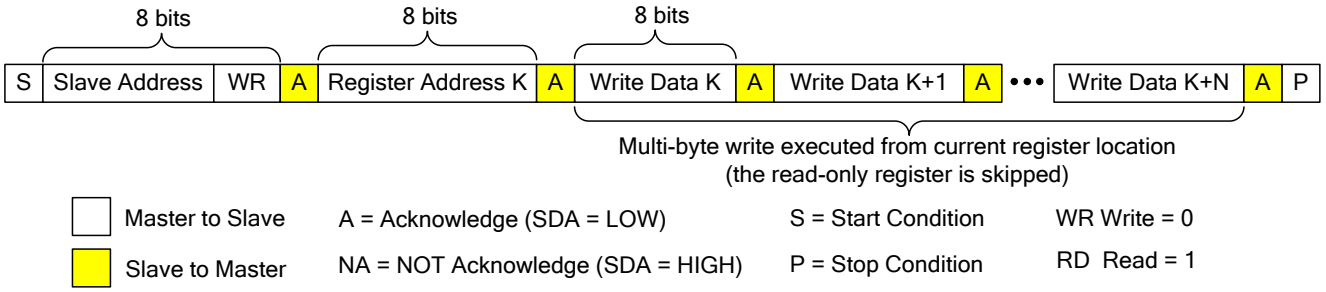
Figure 15: Complete Data Transfer

The MP5470B includes a full I²C slave controller. The I²C slave fully complies with the I²C specification requirements. It requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP5470B acknowledges the receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP5470B. The MP5470B performs an update on the falling edge of the LSB byte.

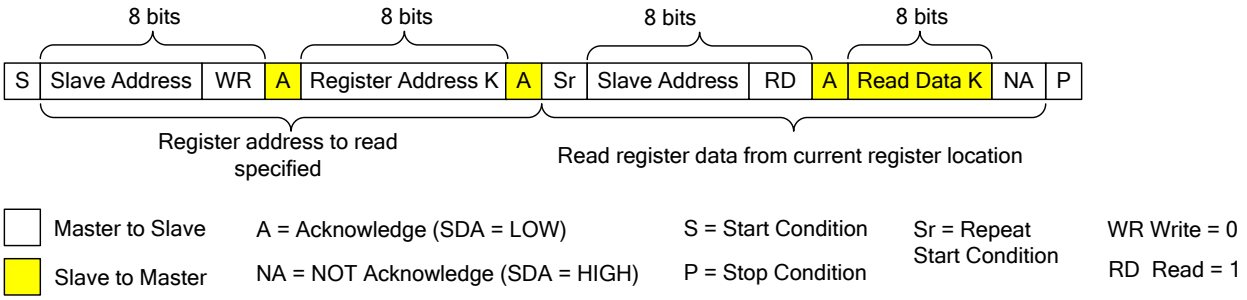
Examples of an I²C write and read sequence are shown below.



I²C Write Example – Write Single Register



I²C Write Example – Write Multi-Register



I²C Read Example – Read Single Register

APPLICATION INFORMATION

Selecting the Inductor

For most applications, use a 0.47µH to 3.3µH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived with Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose an inductor ripple current that is approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Use a larger inductor for improved efficiency under light-load conditions.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. Low-ESR ceramic capacitors with X5R or X7R dielectrics are recommended for best results because of their low ESR and small temperature coefficients. For most applications, use a 10 or 22µF capacitor for VIN1, and a 10 or 22µF capacitor for VIN2.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Step-Down Regulator

Output Capacitor

The output capacitor for the step-down regulator maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C2}\right) \quad (7)$$

Where L_1 is the inductor value, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation.

PCB Layout Guidelines (11)

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 16 and follow the guidelines below:

1. Connect the input ground to the GND pin using the shortest and widest trace possible.
2. Connect the input capacitor to the VIN pin using the shortest and widest trace possible.
3. Ensure that all feedback connections are short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas, such as FB.
6. Place the VCC decoupling capacitor close to the VCC and AGND pins.

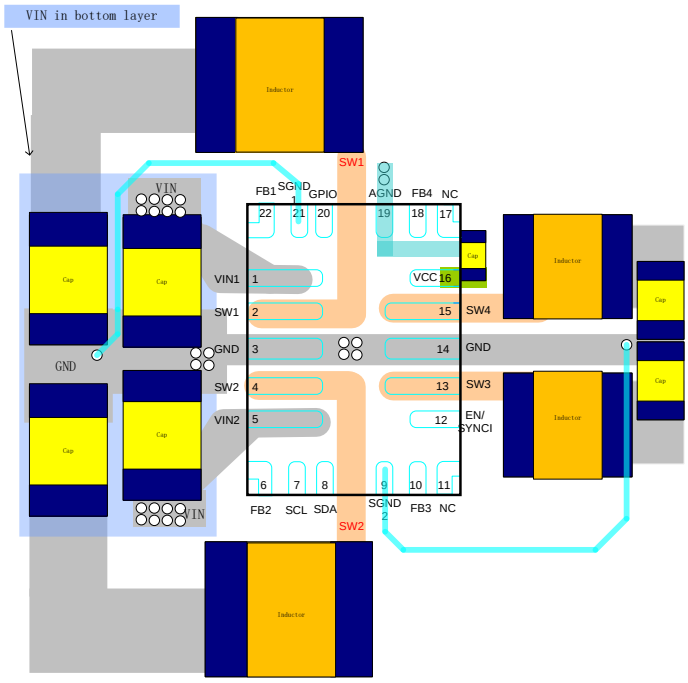


Figure 16: Recommended Layout

Note:

11) The recommended layout is based on the Typical Application Circuits shown on page 39.

TYPICAL APPLICATION CIRCUITS

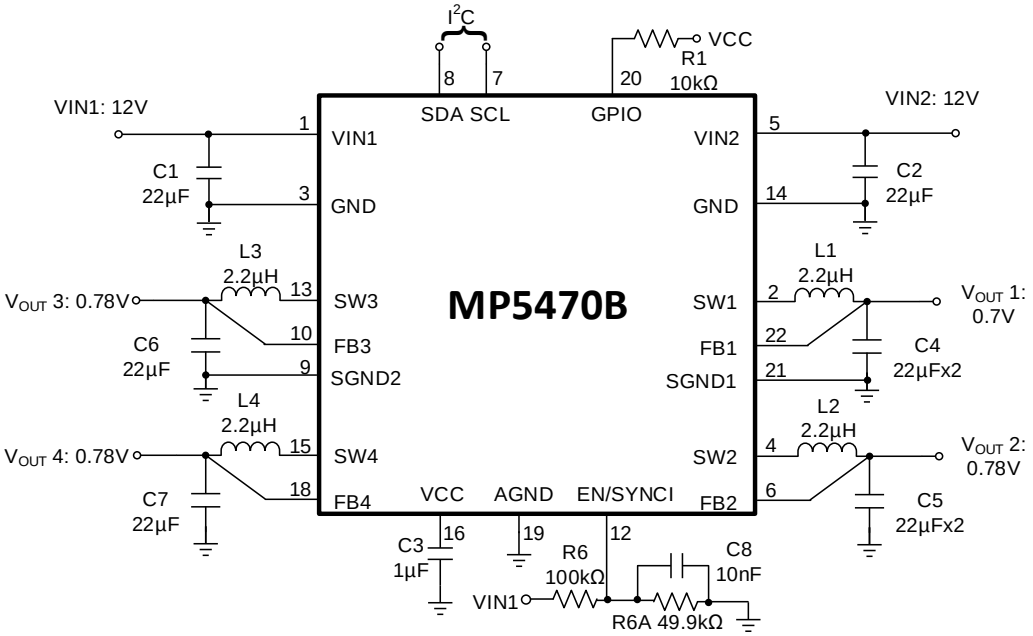


Figure 17: 12V$_{IN}$ Typical Application Circuit

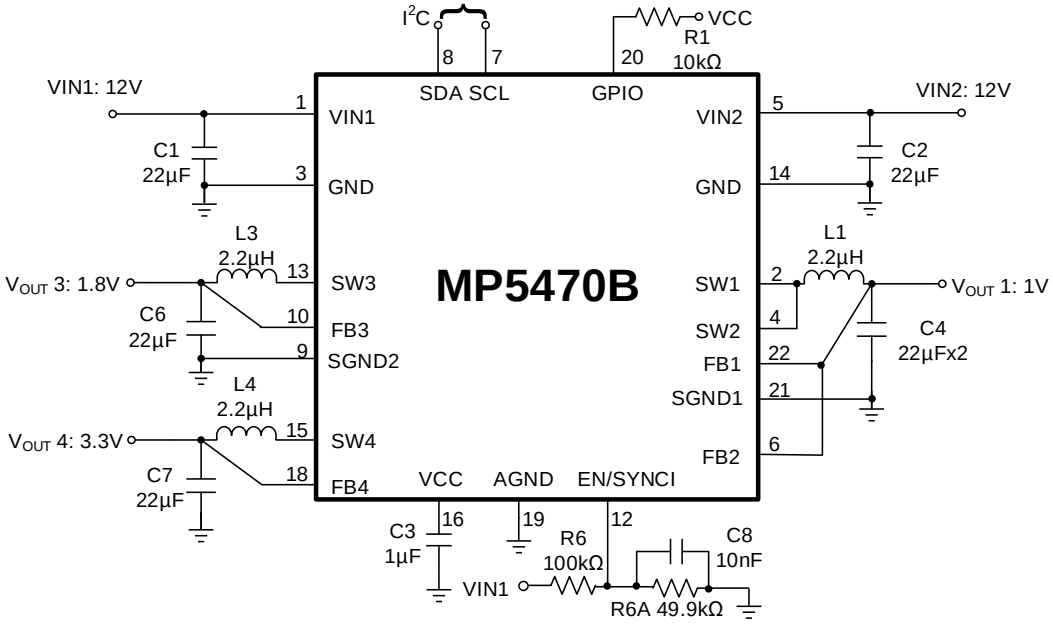
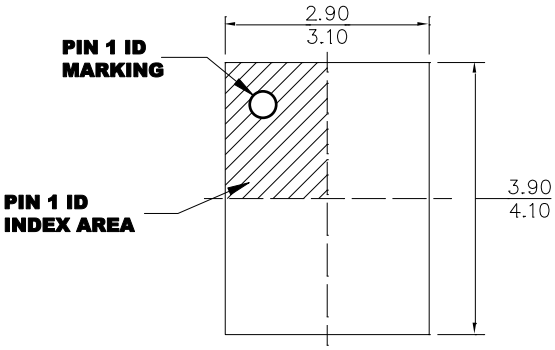


Figure 18: 12V$_{IN}$, Buck 1 and Buck 2 Working in Parallel Mode to Provide Higher Output Current

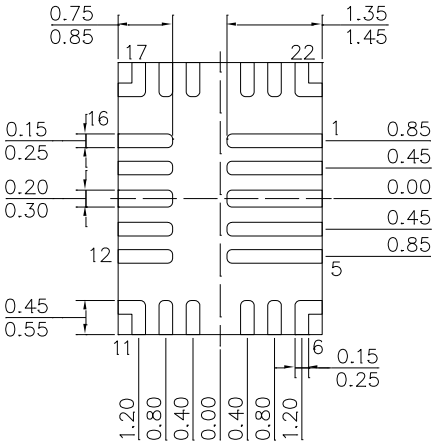
Note: Connect FB1 to FB2 for parallel mode feedback.

PACKAGE INFORMATION

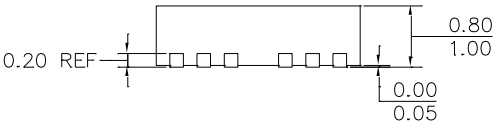
QFN-22 (3mmx4mm)



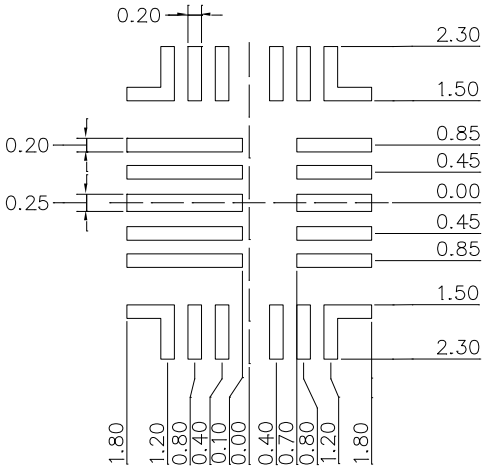
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.