MP5493

36V, 0.6A, 550kHz, Synchronous Buck Supercapacitor Charger and Boost for PLC Mode

DESCRIPTION

The MP5493 is an energy backup and management unit that provides a very compact and efficient energy management solution for the power line carrier (PLC) in power meters. The MP5493 consists of a buck DC/DC converter combined with a bidirectional DC/DC converter that supports a supercapacitor charger and boost topology. The MP5493 uses the bidirectional converter to achieve optimal energy transfer and to provide the most cost-effective energy storage solution.

The MP5493 achieves high power conversion efficiency across a wide load range by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce switching and gate driving losses. Thermal shutdown provides reliable and fault-tolerant operation.

The MP5493 is available in a cost-effective TSOT23-8 package.

FEATURES

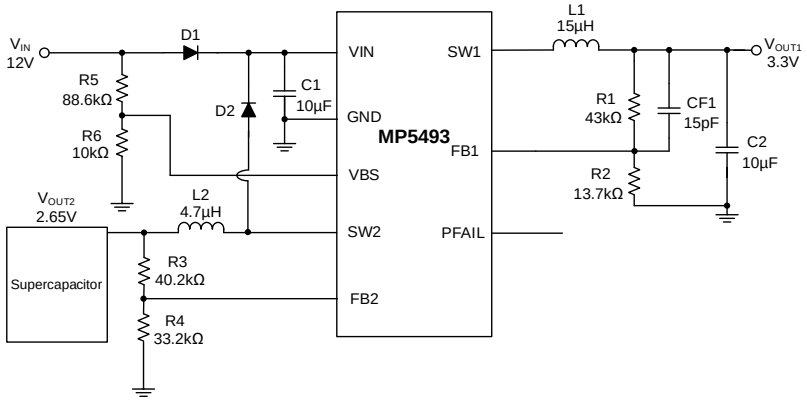
- Wide 5V to 36V Operating Input Voltage (V_{IN})
- Real-Time Input Shutdown Detection to Enable Boost Mode
- Input Status Indicator
- Buck Converter:
  - 600mA Continuous Output Current (I_{OUT})
  - 600mΩ/320mΩ Internal Power MOSFETs
  - Power-Save Mode for Light Loads
  - Internal Soft Start (SS)
  - Low-Dropout (LDO) Mode
  - Short-Circuit Protection (SCP) with Hiccup Mode
  - Adjustable Output from 0.8V
- Bidirectional Converter for Supercapacitor Charger and Boost
  - 600mΩ/320mΩ Internal Power MOSFETs
  - Adjustable Output from 1.2V for Supercapacitor Charger
- Over-Temperature Protection (OTP)
- Available in a TSOT23-8 Package

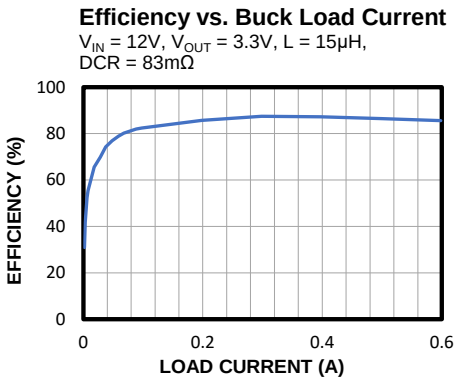
MPL Optimized Performance with MPS Inductor MPL-AL4020 Series, MPL-SE5040 Series, and MPL-SE6040 Series

APPLICATIONS

- PLC Modules
- Power Meters
- Backup Capacitor Systems
- Power Failure Backup Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5493GJ	TSOT23-8	*See Below*	*1*

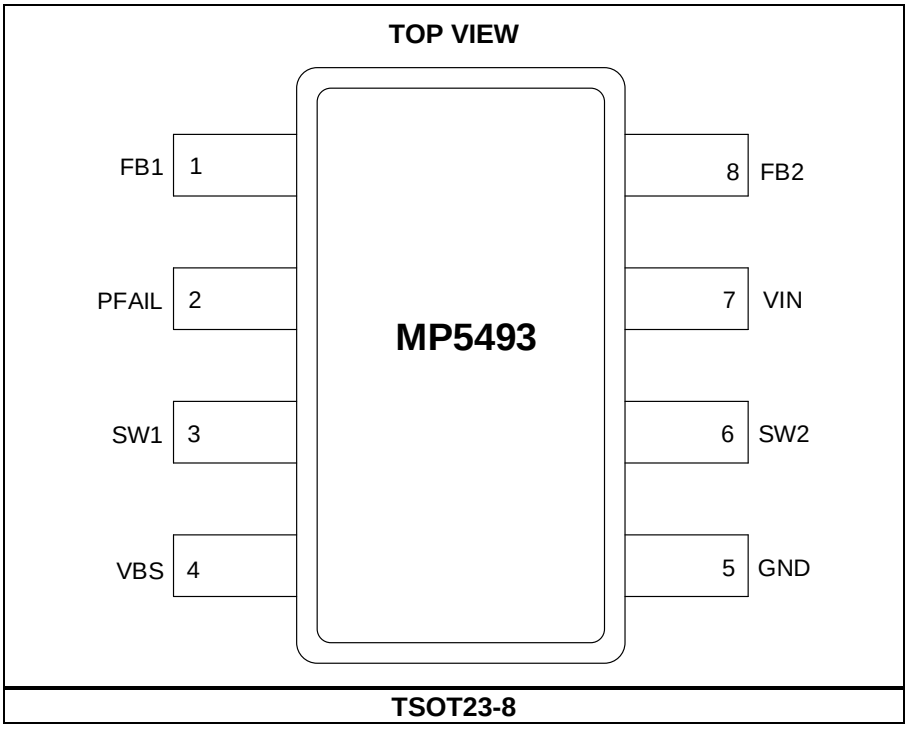
* For Tape & Reel, add suffix -Z (e.g. MP5493GJ-Z).

TOP MARKING

|BRQY

BRQ: Product code of MP5493GJ
Y: Year code

PACKAGE REFERENCE



TSOT23-8

PIN FUNCTIONS

Pin #	Name	Description
1	FB1	**Buck feedback.** The FB1 pin is the buck's error amplifier (EA) input. Connect an external resistor divider between the output and GND to set the output voltage (V_{OUT}).
2	PFAIL	**Power fail indicator.** The PFAIL pin is the open drain of an internal MOSFET. Connect PFAIL to an external power source via a 10kΩ to 500kΩ pull-up resistor. If the VBS voltage (V_{VBS}) is below its under-voltage lockout (UVLO) falling threshold ($V_{VBS\_UVLO\_FALLING}$), the MOSFET turns on and PFAIL is pulled down to indicate input shutdown.
3	SW1	**Buck output switching node.** The SW1 pin is the buck's switching output. SW1 is connected internally to the high-side MOSFET (HS-FET) source and the low-side MOSFET (LS-FET) drain. Connect SW1 to a power inductor.
4	VBS	**V_{IN} bus voltage detection.** Connect an external resistor divider between the VIN and GND pins to set the BOOST release mode threshold.
5	GND	**System ground.** The GND pin is the reference ground of V_{OUT} and requires careful consideration during PCB layout. Connect GND using wide PCB traces.
6	SW2	**Supercapacitor charger output switching node.** The SW2 pin is the supercapacitor charger's switching output. SW2 is connected internally to the HS-FET source and LS-FET drain. Connect SW2 to a power inductor.
7	VIN	**Input supply.** The VIN pin is the input of the converters and supplies power to the internal regulator. Place a decoupling capacitor connected to ground as close as possible to VIN to reduce switching spikes on the input.
8	FB2	**Supercapacitor charger feedback.** The FB2 pin is the supercapacitor charger's EA input. Connect an external resistor divider between the output and GND to set V_{OUT}.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +40V
Switching voltage (V_{SW1}, V_{SW2}).....-0.3V (-5V for <10ns) to V_{IN} + 0.3V (45V for <10ns)
All other pins .....-0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2) 2.97W (4)
Storage temperature.....-65°C to +150°C
Junction temperature .....150°C
Lead temperature .....260°C

ESD Ratings

Human body model (HBM) ..... ±1000V
Charged-device model (CDM) ..... ±750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) .....5V to 36V
Output voltage (V_{OUT1}).....0.8V to 0.95 x V_{IN}
Output voltage (V_{OUT2}).....1.2V to 0.92 x V_{IN}
Operating junction temp..... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

TSOT23-8
EVL5493-J-00A (4).....42.1.....15.5.....°C/W
JESD51-7 (5).....87.....50.....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on the EVL5493-J-00A, a 2-layer PCB (50mmx50mm).
5) Measured on JESD51-7, a 4-layer PCB. The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted. (6)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current	I_{SD}	V_{VBS} = 0V		47	70	μA
Quiescent supply current	I_Q	V_{VBS} = V_{FB1} = V_{FB2} = 1.5V		450	800	μA
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		4.4	4.65	4.9	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		3.9	4.2	4.4	V
V_{VBS} UVLO rising threshold	$V_{VBS\_UVLO\_RISING}$		0.9	1.05	1.2	V
V_{VBS} UVLO falling threshold	$V_{VBS\_UVLO\_FALLING}$		0.9	1	1.1	V
V_{VBS} UVLO hysteresis	V_{VBS_HYS}			50		mV
PFAIL low voltage	V_{PG_L}	I_{PFAIL} = 3mA			0.4	V
Thermal shutdown (7)	T_{SD}			160		°C
Thermal hysteresis (7)	T_{HYS}			30		°C
Channel 1						
Feedback voltage	V_{FB1}	T_J = 25°C	0.792	0.8	0.808	V
		T_J = -40°C to +125°C	0.788	0.8	0.812	V
Feedback current	I_{FB1}	V_{FB1} = 0.84V		50	100	nA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS1}$			600		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS1}$			320		mΩ
High-side (HS) switch leakage current	I_{LKG_HS1}	V_{IN} = 36V			1	μA
Low-side (LS) switch leakage current	I_{LKG_LS1}	V_{IN} = 36V			1	μA
Peak current limit	I_{PEAK1}		0.7	0.9	1.1	A
Valley current limit	I_{VALLEY}		0.4	0.6	0.8	A
Zero-current detection (ZCD) threshold	I_{ZCD1}			50		mA
Maximum duty cycle (7)	D_{MAX1}			95		%
Switching frequency	f_{SW1}	T_J = 25°C	470	550	630	kHz
		T_J = -40°C to +125°C	450	550	700	kHz
Minimum on time (7)	t_{ON_MIN1}			80		ns
Minimum off time (7)	t_{OFF_MIN1}			190		ns
Soft-start time	t_{SS}	10% V_{OUT} to 90% V_{OUT}		0.35		ms
Channel 2 (Supercapacitor Charge Mode)						
Feedback voltage	V_{FB2}	T_J = 25°C	1.188	1.2	1.212	V
		T_J = -40°C to +125°C	1.182	1.2	1.218	V
Feedback current	I_{FB2}	V_{FB2} = 1.26V		50	100	nA
HS-FET on resistance	$R_{DS(ON)\_HS2}$			600		mΩ
LS-FET on resistance	$R_{DS(ON)\_LS2}$			320		mΩ
HS-FET leakage current	I_{LKG_HS2}	V_{IN} = 36V			1	μA
LS-FET leakage current	I_{LKG_LS2}	V_{IN} = 36V			1	μA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = 25°C, unless otherwise noted. (6)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Peak current limit	I_{PEAK2}		200	400	600	mA
Zero-current detection (ZCD) threshold	I_{ZCD2}			50		mA
Maximum duty cycle (7)	D_{MAX2}			92		%
Minimum on time (7)	t_{ON_MIN2}			80		ns
HS-FET off time during charging (7)	t_{OFF}			12		µs
Channel 2 (Boost Mode)						
Peak current limit	I_{PEAK_BOOST}		1.5	2	2.5	A
Boost peak threshold	V_{PEAK}		10.5	11	11.5	V
Boost valley threshold (8)	V_{VALLEY}		7.5		11	V
Boost UVLO falling threshold (9)	$V_{BOOST\_FALLING}$		0.34	0.37	0.4	V
Switching frequency	f_{SW2}	T_J = 25°C	470	550	630	kHz
		T_J = -40°C to +125°C	450	550	700	kHz

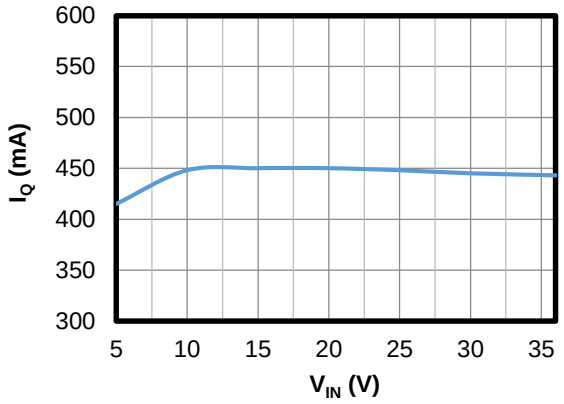
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Not tested in production. Derived by sample characterization.
8) There are six boost valley threshold settings determined by V_{IN} when channel 2 starts to boost. See Table 1 on page 14 for more information.
9) The supercapacitor's UVLO threshold in boost mode is determined by the V_{FB2} falling threshold.

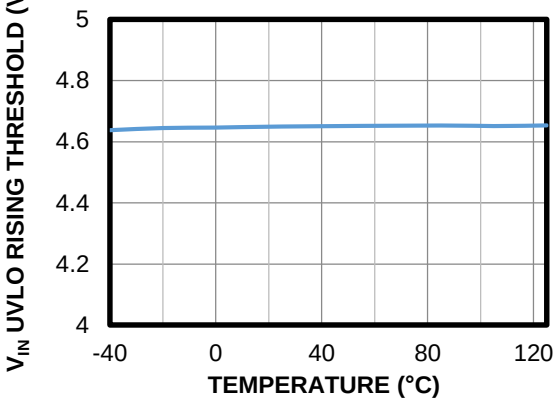
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

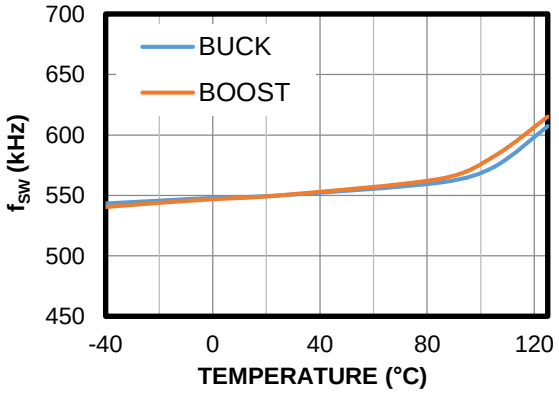
Quiescent Supply Current vs. Input Voltage



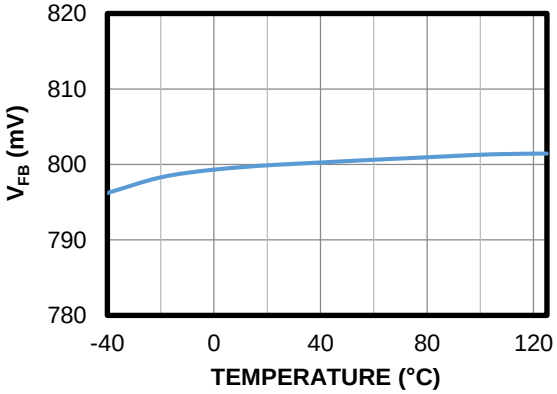
V_{IN} UVLO Rising Threshold vs. Temperature



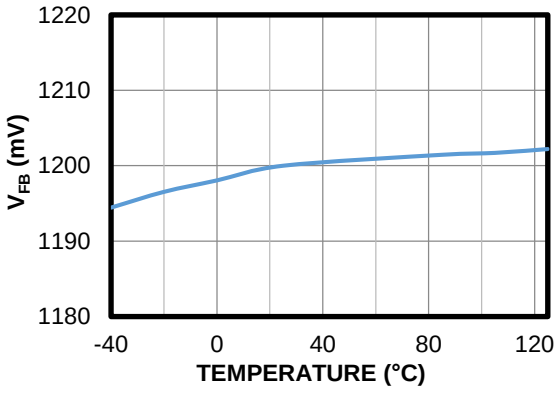
Switching Frequency vs. Temperature



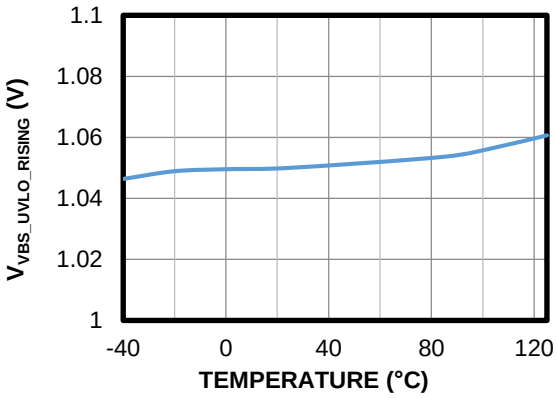
Feedback Voltage vs. Buck Temperature



Feedback Voltage vs. Supercapacitor Charger Temperature



V_{VBS} UVLO Rising Threshold vs. Temperature

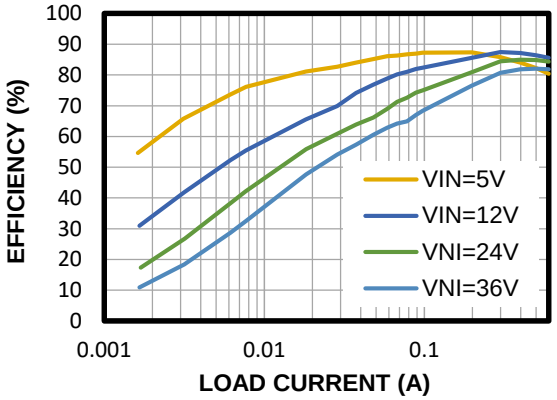


TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board with the circuits on page 19. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.65V, L1 = 15µH, L2 = 4.7µH, and T_A = 25°C, unless otherwise noted.

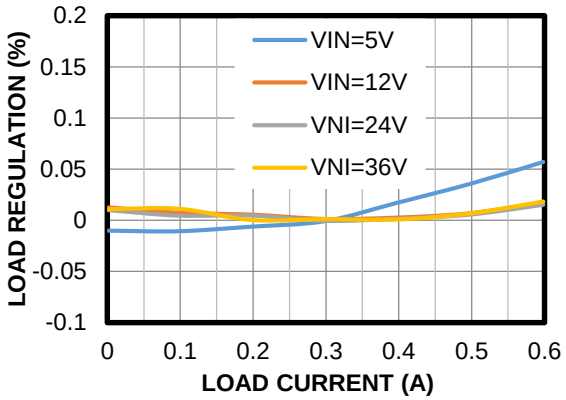
Efficiency vs. Buck Load Current

V_{OUT} = 3.3V, L = 15µH, DCR = 83mΩ



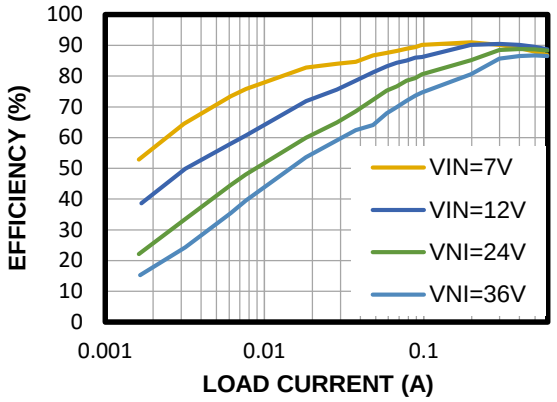
Buck Load Regulation

V_{OUT} = 3.3V, L = 15µH



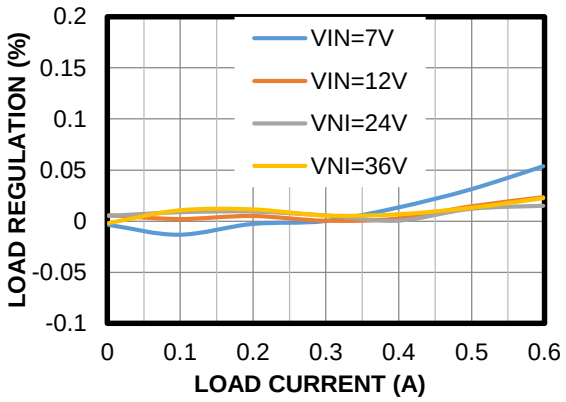
Efficiency vs. Buck Load Current

V_{OUT} = 5V, L = 22µH, DCR = 97mΩ

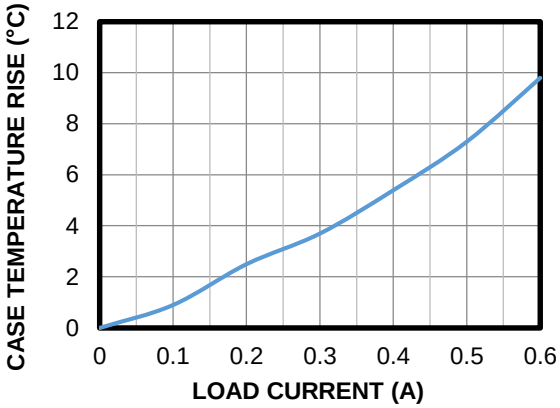


Buck Load Regulation

V_{OUT} = 5V, L = 22µH

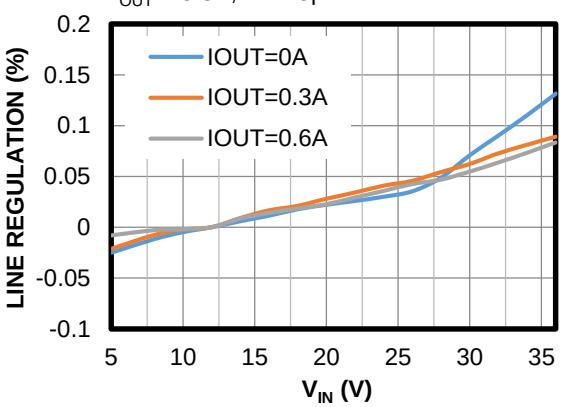


Case Temperature Rise vs. Buck Load Current



Buck Line Regulation

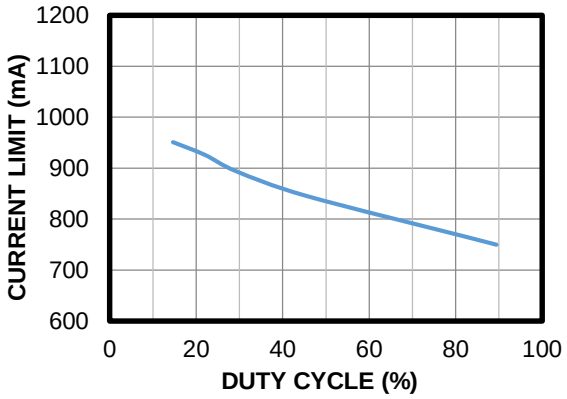
V_{OUT} = 3.3V, L = 15µH



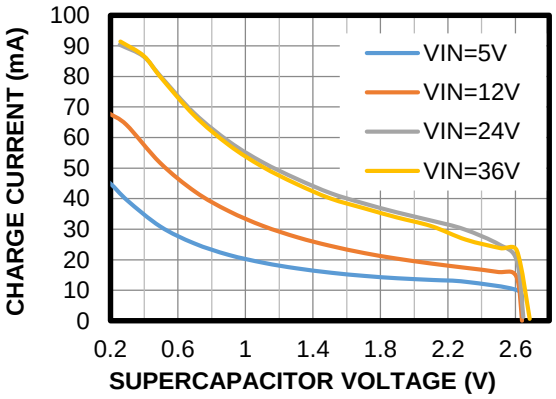
TYPICAL CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board with the circuits on page 19. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.65V, L1 = 15µH, L2 = 4.7µH, and T_A = 25°C, unless otherwise noted.

Peak Current Limit vs. Buck Duty Cycle

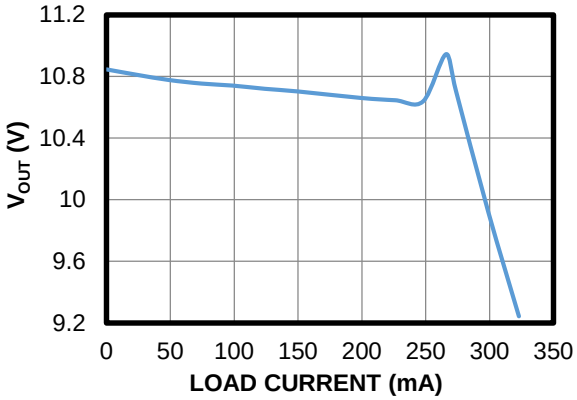


Charge Current vs. Supercapacitor Voltage



Boost Load Regulation

2.65V supply at V_{OUT2}, add load and measure the voltage on VIN

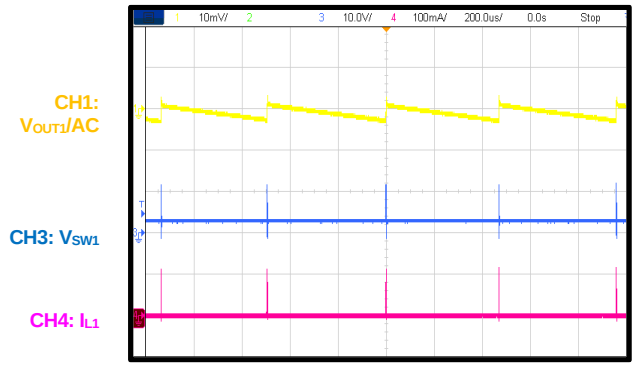


TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board with the circuits on page 19. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.65V, L1 = 15µH, L2 = 4.7µH, and T_A = 25°C, unless otherwise noted.

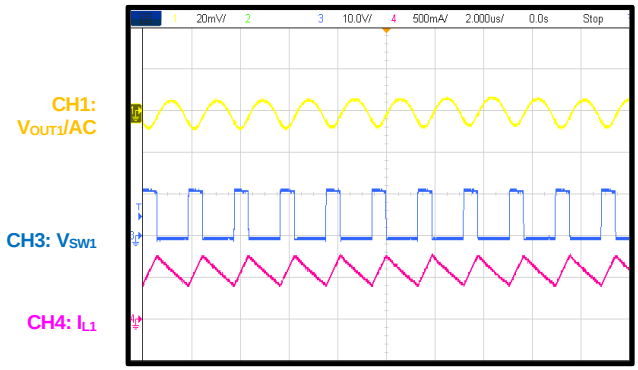
Buck 1 Steady State

I_{OUT1} = 0A



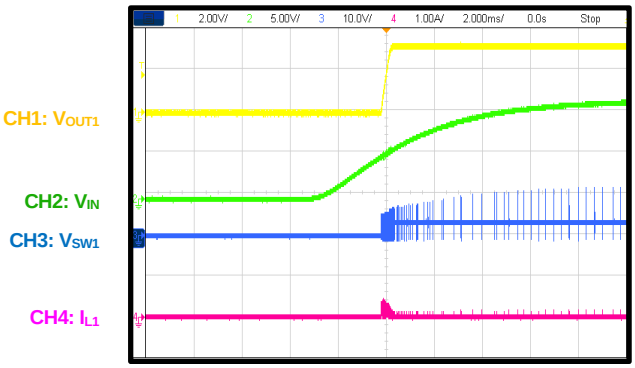
Buck 1 Steady State

I_{OUT1} = 0.6A



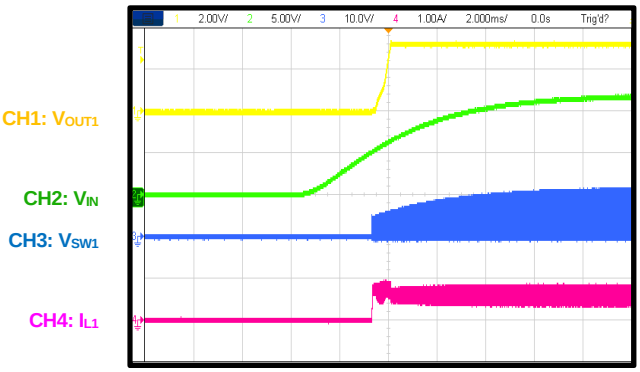
Start-Up through Buck 1 VIN

I_{OUT1} = 0A



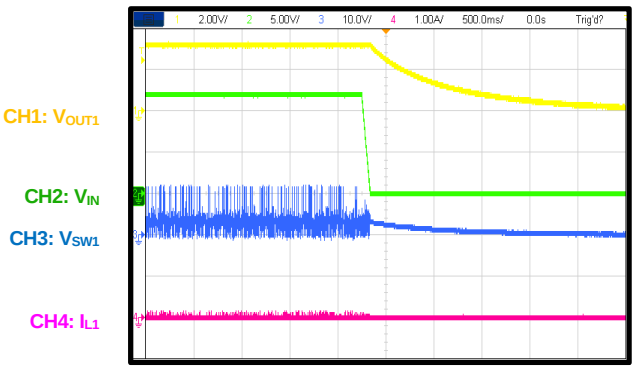
Start-Up through Buck 1 VIN

I_{OUT1} = 0.6A



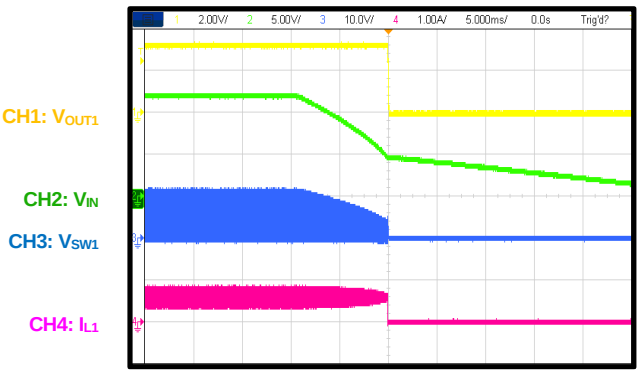
Shutdown through Buck 1 VIN

I_{OUT1} = 0A



Shutdown through Buck 1 VIN

I_{OUT1} = 0.6A

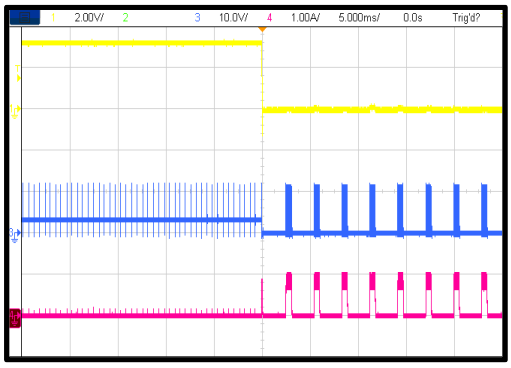


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board with the circuits on page 19. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.65V, L1 = 15µH, L2 = 4.7µH, and T_A = 25°C, unless otherwise noted.

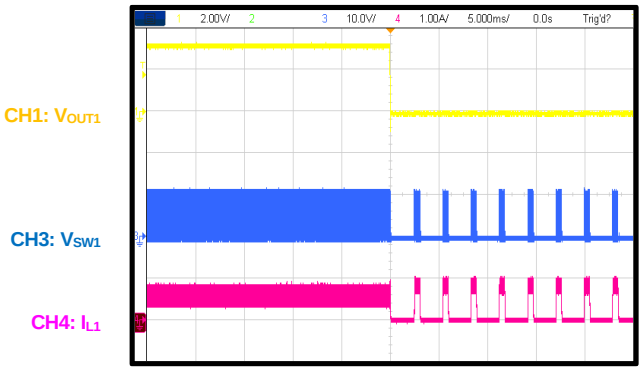
Short-Circuit Protection Entry

I_{OUT1} = 0A



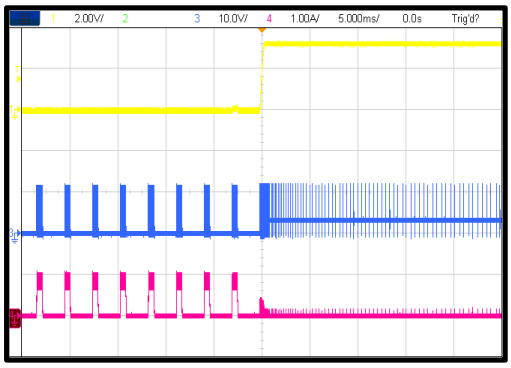
Short-Circuit Protection Entry

I_{OUT1} = 0.6A



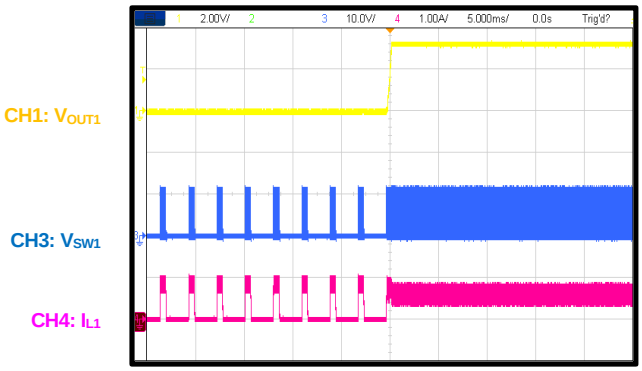
Short-Circuit Protection Recovery

I_{OUT1} = 0A



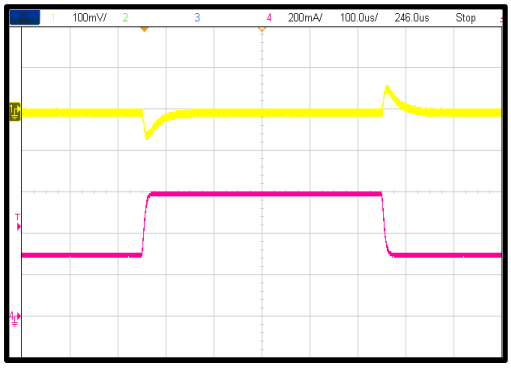
Short-Circuit Protection Recovery

I_{OUT1} = 0.6A



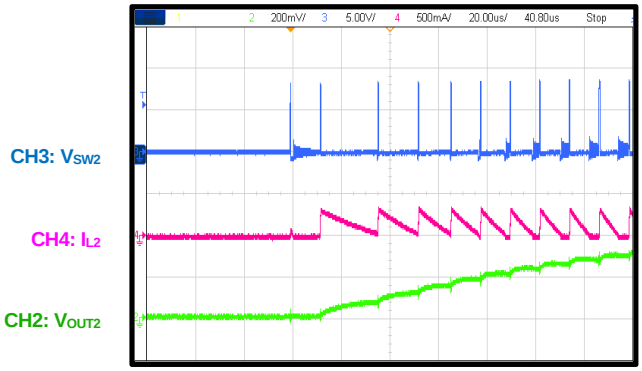
Load Transient

I_{OUT1} = 0.3A to 0.6A, 80mA/µs



Buck 2 Charge Capacitor

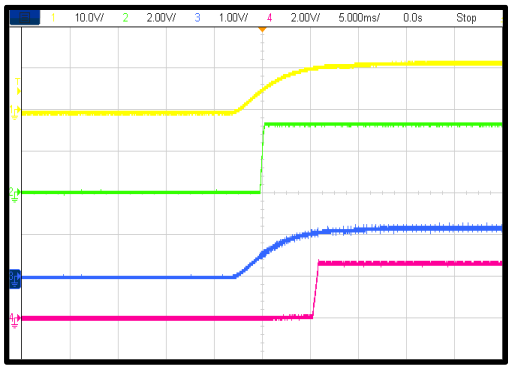
V_{IN} = 12V, V_{OUT2} = 2.65V, C_{OUT2} = 47µF



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

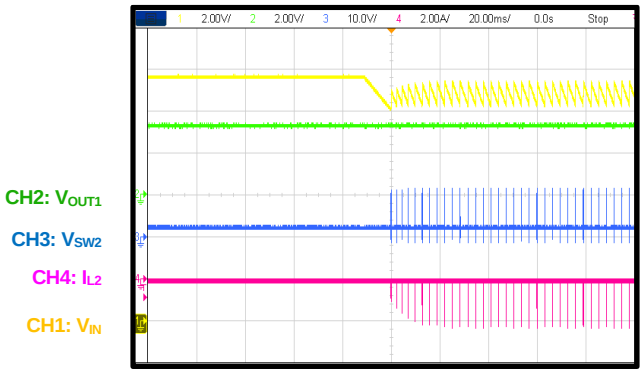
Performance waveforms are tested on the evaluation board with the circuits on page 19. V_{IN} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 2.65V, L1 = 15µH, L2 = 4.7µH, and T_A = 25°C, unless otherwise noted.

Start-Up



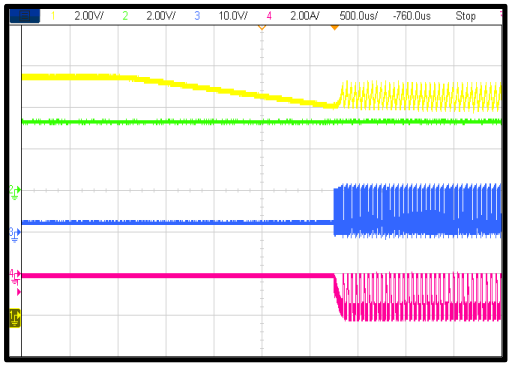
Energy Release Mode Entry

I_{OUT1} = 0A



Energy Release Mode Entry

I_{OUT1} = 0.6A



FUNCTIONAL BLOCK DIAGRAM

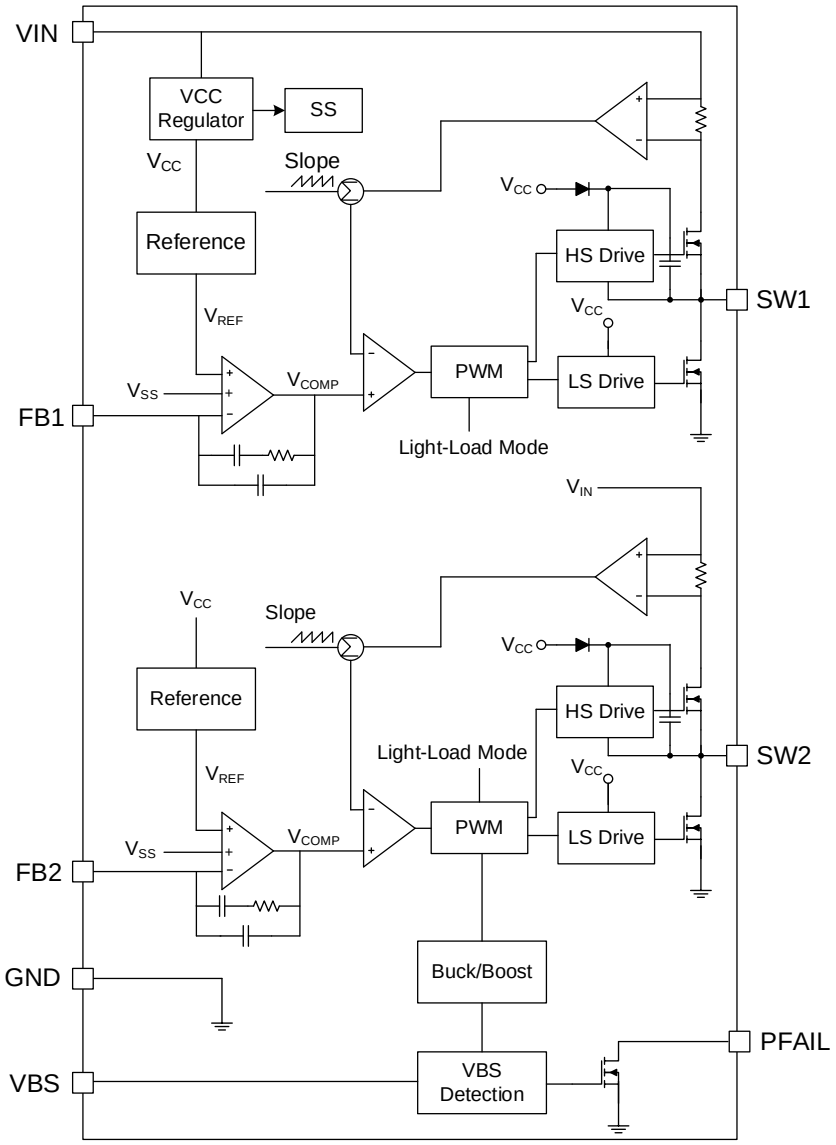


Figure 1: Functional Block Diagram

OPERATION

The MP5493 is an energy backup and management unit in a TSOT23-8 package, which provides a very compact and efficient energy management solution for the power line carrier (PLC) in power meters. The MP5493 consists of a buck DC/DC converter (Channel 1) combined with a bidirectional DC/DC converter (Channel 2) that supports a supercapacitor charger and boost topology. The MP5493 uses the bidirectional converter to achieve optimal energy transfer and to provide the most cost-effective energy storage solution.

The integrated bidirectional converter operates in buck mode to charge the supercapacitor when the VBS pin voltage (V_{VBS}) exceeds its under-voltage lockout (UVLO) rising threshold ($V_{VBS\_UVLO\_RISING}$) and the buck converter's output voltage (V_{OUT}) reaches the regulation voltage. If the input voltage (V_{IN}) shuts down suddenly, the integrated bidirectional converter operates in boost mode to transfer the energy from the supercapacitor to VIN.

V_{IN} Start-Up

When V_{IN} starts up, V_{VBS} starts up after V_{IN}. If V_{IN} exceeds its UVLO rising threshold ($V_{IN\_UVLO\_RISING}$), the buck converter starts up first.

If V_{VBS} exceeds $V_{VBS\_UVLO\_RISING}$ and the buck converter's V_{OUT} reaches the regulation voltage, the supercapacitor charger starts up and charges the supercapacitor. Figure 2 shows the MP5493's start-up sequence.

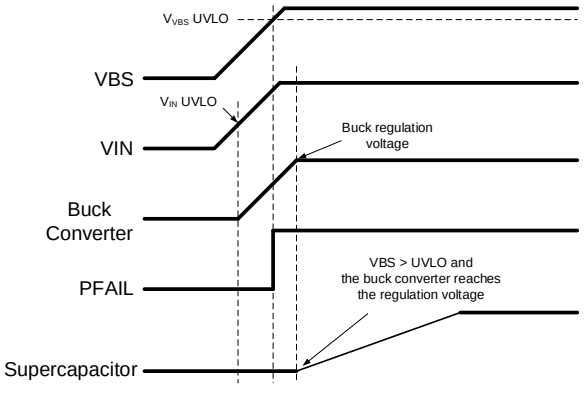


Figure 2: System Start-Up Sequence

V_{IN} Shutdown

After V_{IN} drops, the MP5493 enters release mode.

Once V_{VBS} drops to its UVLO falling threshold ($V_{VBS\_UVLO\_FALLING}$), the PFAIL pin is pulled low to indicate that V_{IN} has dropped. At the same time, Channel 2 enters boost mode to transfer the energy from the supercapacitor to VIN.

In boost mode when the low-side MOSFET (LS-FET) turns on, the inductor current (I_L) flows in a negative direction. The LS-FET remains off until the negative current limit threshold is tripped. Then the high-side MOSFET (HS-FET) turns on until the internal clock ends. The LS-FET turns on again and repeat this action until V_{IN} is charged to the boost peak threshold.

If V_{IN} exceeds the boost peak threshold, the MP5493 stop boosting until V_{IN} drops to the boost valley threshold. The MP5493 has six boost valley thresholds that are determined by V_{IN} when V_{VBS} drops below $V_{VBS\_UVLO\_FALLING}$ (1V typically). Table 1 shows the six boost valley threshold configurations. The boost valley threshold can be regulated by selecting the resistance of the resistor divider connected to VBS.

Table 1: Boost Valley Threshold Configuration

Condition (V_{IN} when V_{VBS} drops to 1V)	Boost Valley Threshold (Typical)
V_{IN} < 8V	8V
8V < V_{IN} < 8.5V	8.5V
8.5V < V_{IN} < 9V	9V
9V < V_{IN} < 9.5V	9.5V
9.5V < V_{IN} < 10V	10V
10V < V_{IN}	10.5V

When the supercapacitor rail's feedback (FB) voltage, which is also the FB2 pin voltage (V_{FB2}), drops below the boost UVLO falling threshold ($V_{BOOST\_FALLING}$), the system shuts down the bidirectional converter, and V_{IN} continue to drops. Once V_{IN} falls below $V_{IN\_UVLO\_FALLING}$, the MP5493 shuts down.

Figure 3 shows the MP5493's entire working sequence after V_{IN} shutdown.

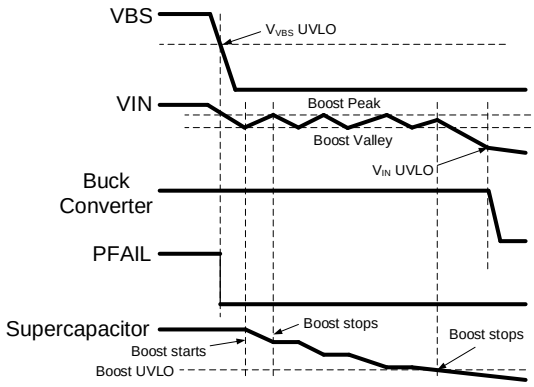


Figure 3: Power Shutdown Sequence

If V_{IN} recovers in release mode and V_{VBS} exceeds its rising threshold, the MP5493 stops boosting. When the buck converter's V_{OUT} reaches the regulation voltage, the bidirectional converter enters buck charge mode again to recharge the supercapacitor.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the buck converter operates in a fixed-frequency, peak current mode control to regulate V_{OUT}. A pulse-width modulation (PWM) cycle initiated by the internal clock turns on the HS-FET. The HS-FET remains on until its current reaches the value set by the COMP voltage (V_{COMP}). When the HS-FET turns off, the LS-FET turns on, and I_L flows through the LS-FET. To avoid shoot-though, a dead time is inserted to prevent the HS-FET and LS-FET from turning on at the same time. For each switching cycle, the HS-FET turns on and off with a minimum on time (t_{ON_MIN}) and minimum off time (t_{OFF_MIN}).

Pulse-Skip Mode (PSM)

Under light-load conditions, the MP5493's buck converter enters pulse-skip mode (PSM) to improve efficiency. PSM is triggered when V_{COMP} drops below the internal sleep mode threshold, which generates a pause command to block the turn-on clock pulse. Thus, the HS-FET does not turn on, which reduces gate driving and switching losses.

When V_{COMP} exceeds the sleep mode threshold, the pause signal resets, and the chip resumes normal PWM operation. Whenever the pause command changes from low to high, the PWM signal goes high immediately and turns on the HS-FET.

Under-Voltage Lockout (UVLO)

V_{IN} UVLO protects the chip from operating at an insufficient supply voltage. See the Electrical Characteristics section on page 5 for the V_{IN} UVLO rising and falling thresholds.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP5493's buck converter provides valley current limit control and peak current limit control.

During the LS-FET on period, I_L is monitored. When the sensed I_L exceeds the valley current limit threshold, over-current protection (OCP) is triggered. The HS-FET does not turn on until I_L drops below the valley current limit.

During the HS-FET on period, I_L is sensed and compared to the peak current limit (I_{PEAK}). If I_{PEAK} is triggered, the on pulse is terminated immediately. V_{OUT} drops until V_{FB} falls below the under-voltage (UV) threshold (typically 50% of the reference). Once a UV condition is triggered, the MP5493 enters hiccup mode.

In hiccup mode, the chip disables the output power stage and attempts to soft start (SS) again automatically. This is especially useful when the output is dead-shorted to ground. If the over-current (OC) condition remains after SS ends, the device repeats this operation cycle until the OC condition is removed, and the output rises back to regulation levels. OCP is a non-latch protection.

Low-Dropout (LDO) Operation

When V_{IN} is close to V_{OUT}, the MP5493's buck converter continues to increase the HS-FET's on time after reaching channel 1's minimum off time (t_{OFF_MIN1}) to improve dropout. When the current in the HS-FET does not reach the value set by COMP within one PWM cycle, the HS-FET remains on to prevent a turn-off operation. At this time, the switching frequency (f_{SW}) decreases instead of remaining constant. The MP5493's buck converter supports up to a 95% maximum duty cycle.

Internal Soft Start (SS)

Soft start (SS) prevents V_{OUT} from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V during the SS time (t_{SS}). When V_{SS} is below V_{REF}, V_{SS} overrides V_{REF} as the error amplifier (EA) reference. When V_{SS} exceeds V_{REF}, the EA uses V_{REF} as the reference.

Thermal Shutdown

Thermal shutdown prevents the device from operating at exceedingly high temperatures and protects it from thermal runaway. The silicon die temperature is monitored internally. If the die temperature exceeds the thermal shutdown threshold (T_{SD}) (160°C typically), the device shuts down. Once the temperature drops below the difference between T_{SD} and thermal hysteresis (T_{HYS}) (130°C typically), the device restarts and resumes normal operation.

Power Fail Indicator (PFAIL)

The PFAIL pin is an open-drain output and is connected to an external supply via a 10kΩ to 500kΩ pull-up resistor. When V_{VBS} exceeds $V_{VBS\_UVLO\_RISING}$, the PFAIL pin voltage (V_{PFAIL}) is pulled up to the external supply voltage via the pull-up resistor. If V_{VBS} is below $V_{VBS\_UVLO\_FALLING}$, the internal MOSFET turns on to pull PFAIL to ground.

When VIN and VBS are not available, and PFAIL is connected to an external supply via a pull-up resistor, PFAIL is clamped low. Figure 4 shows the relationship between the PFAIL clamped voltage and pull-up current.

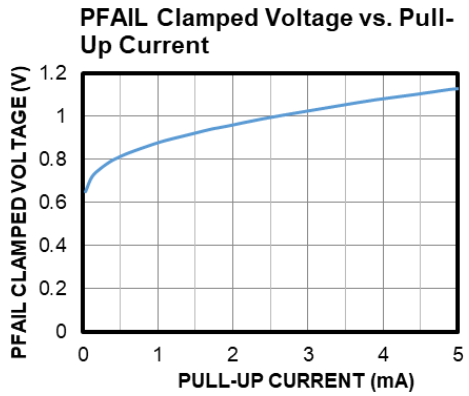


Figure 4: PFAIL Clamped Voltage vs. Pull-Up Voltage

Supercapacitor Charger

Once V_{VBS} exceeds $V_{VBS\_UVLO\_RISING}$ and the buck converter reaches the regulation output voltage, the bidirectional converter operates in buck mode to charge the supercapacitor.

The supercapacitor charger uses I_{PEAK} control to charge the supercapacitor. If V_{OUT} is low, I_L reaches I_{PEAK}, then HS-FET shuts down and LS-FET turns on until the zero-current detection (ZCD) current is detected. After a fixed HS-FET off time (t_{OFF}, 12µs typically), HS-FET turns on again. t_{OFF} limits the average charging current. Figure 5 shows the supercapacitor charger's working process.

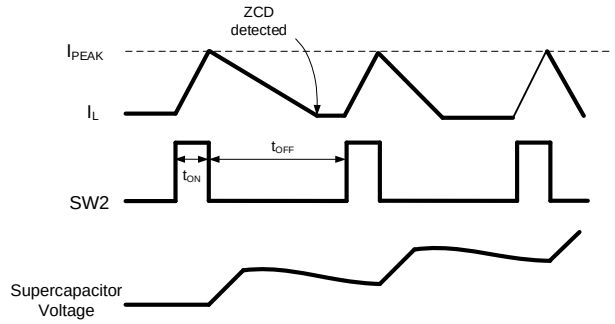


Figure 5: Charging Process of the Supercapacitor Charger

If V_{OUT} increases and approaches the regulation output voltage, then Channel 2's COMP voltage (V_{COMP2}) drops low, and the HS-FET turns off when I_L exceeds the current determined by V_{COMP2}.

It takes about 18 minutes to fully charge a 2.7V, 10F supercapacitor when V_{IN} = 12V and L2 = 4.7µH. Increase L2 to increase the average charging current, then decrease the charging time consumption. If L2 increases to 10µH, the charging time decreases to about 13 minutes.

APPLICATION INFORMATION

Component Selection

Setting the Output Voltage

Set the MP5493's V_{OUT} using a resistor divider (see Figure 6).

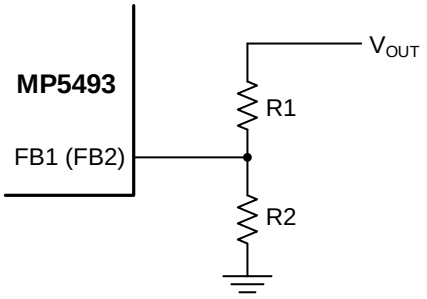


Figure 6: Feedback Network

The FB resistor (R1) also sets the FB loop bandwidth using the internal compensation network. Choose R1 to be around 43kΩ to achieve optimal stability performance and transient response. Then R2 can be calculated with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1} \quad (1)$$

Where the buck converter's V_{FB} is 0.8V, and the supercapacitor charger's V_{FB} is 1.2V.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AL4020 Series, MPL-SE5040 Series, and MPL-SE6040 Series**

The inductor supplies constant current to the output load while being driven by the switching V_{IN}. A larger-value inductor results in less ripple current and a lower output voltage ripple, but also has a larger physical size, higher series resistance, and lower saturation current.

To determine the inductance, allow the peak-to-peak ripple current in the inductor to be approximately 30% to 40% of the maximum load current, and choose a peak inductor current to be below the maximum switch current limit. With low-ESR output capacitors (e.g. MLCC), the inductor current ripple is 60% to 100% of the maximum load current, which further reduces the inductor size and power loss.

The inductance (L) can be calculated with Equation (2):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current (I_{L_PEAK}) can be calculated with Equation (3):

$$I_{L\_PEAK} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (3)$$

Where I_{OUT} is the load current.

MPS inductors are optimized and tested for use with a complete line of integrated circuits.

Table 2 shows the recommended power inductors. Select a part number based on the design requirements.

Table 2: Power Inductor Selection

Part Number	Inductance	Position
MPL-SE5040	15μH	L1
MPL-SE6040	22μH	L1
MPL-AL4020	4.7μH	L2

Visit MonolithicPower.com under Products > Inductors for more information.

Selecting the Input Capacitor

The step-down converter's input current is discontinuous and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC V_{IN}. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

The input capacitor (C_{IN}) requires an adequate ripple current rating because it absorbs the input switching current. The RMS current in C_{IN} can be calculated with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst case occurs at V_{IN} = 2 x V_{OUT}, which can be calculated using Equation (5):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

C_{IN} can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1µF ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C_{OUT}) maintains the DC V_{OUT}. Ceramic capacitors are recommended. Low-ESR capacitors are preferred to limit the output voltage ripple (ΔV_{OUT}), which can be estimated using Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right) \quad (7)$$

Where R_{ESR} is the equivalent series resistance (ESR) of C_{OUT}.

When using ceramic capacitors, the capacitance dominates the impedance at f_{SW} and causes the majority of ΔV_{OUT}. For simplification, ΔV_{OUT} can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at f_{SW}. For simplification, ΔV_{OUT} can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. Inadequate layout design can result in poor line or load regulation and stability issues for the high-frequency switching converter. For the best results, refer to Figure 7 and follow the guidelines below:

1. Keep the path of the input decoupling capacitor, VIN, SW, and PGND, as short as possible using short and wide traces.
2. Keep the external FB divider resistors as close to the sense pins (FB1, FB2, VBS) as possible.
3. Run the FB trace far from the inductor, switching node, and noisy power traces. If possible, run the FB trace on the opposite side of the PCB from the inductor, separated by a ground plane.
4. Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

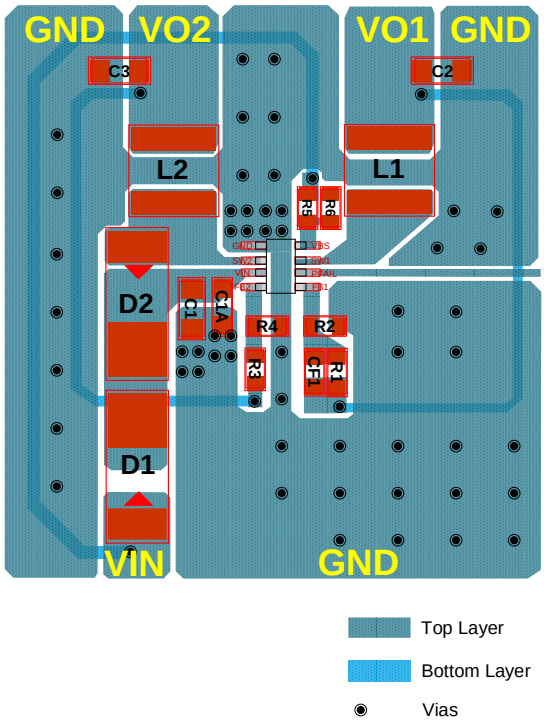


Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

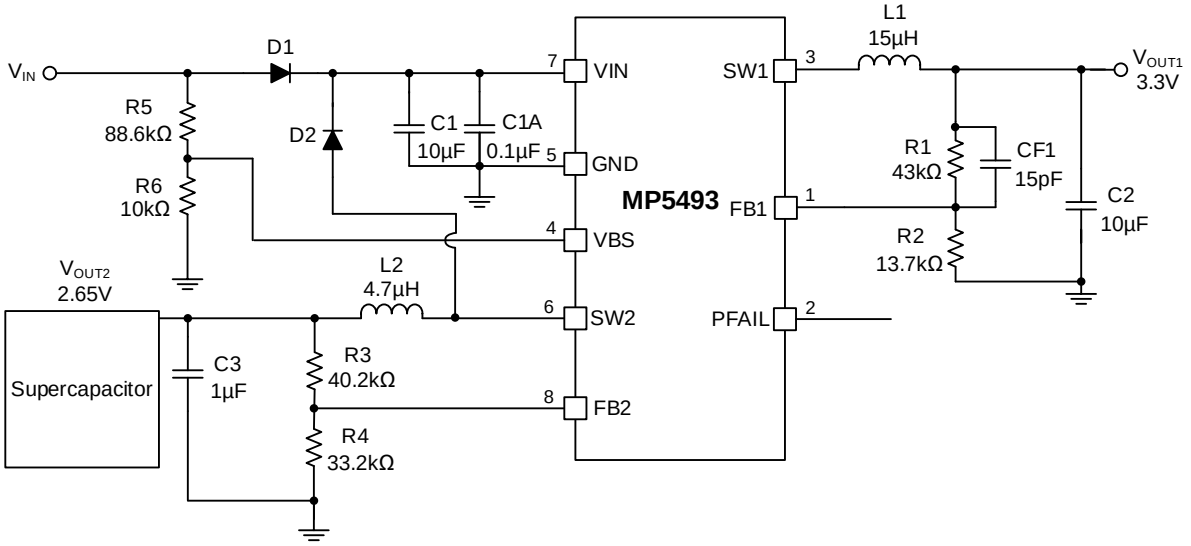


Figure 8: Typical Application Circuit (V_{OUT1} = 3.3V, V_{OUT2} = 2.65V) (10)

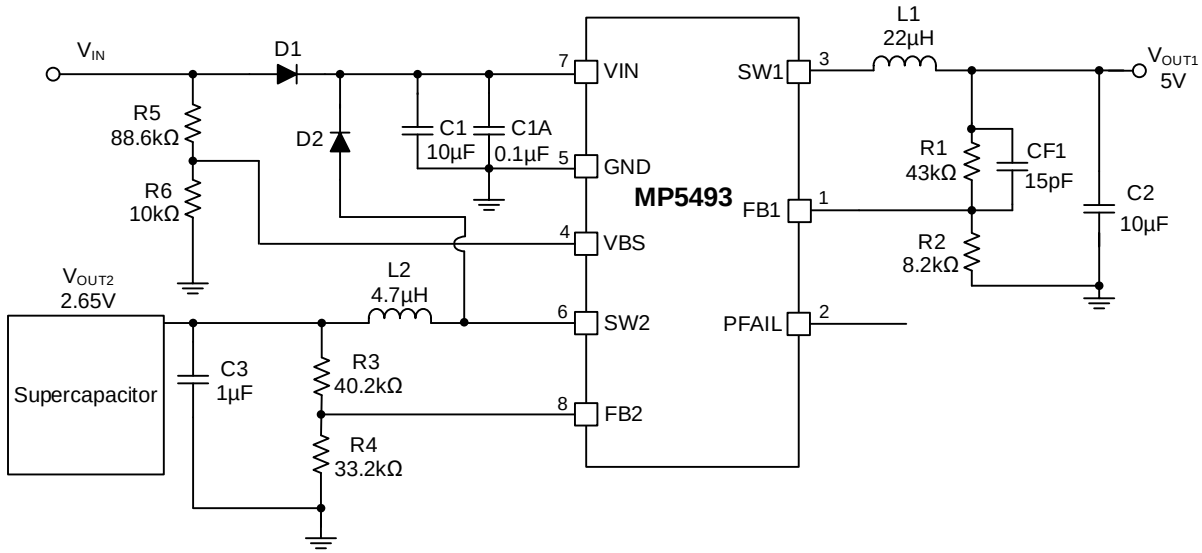


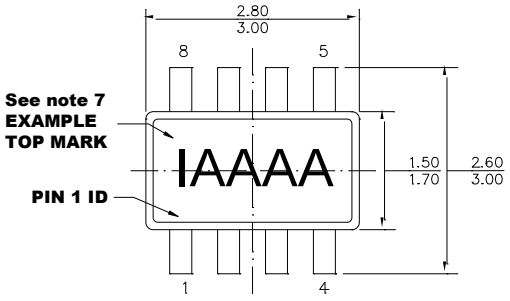
Figure 9: Typical Application Circuit (V_{OUT1} = 5V, V_{OUT2} = 2.65V) (10)

Note:

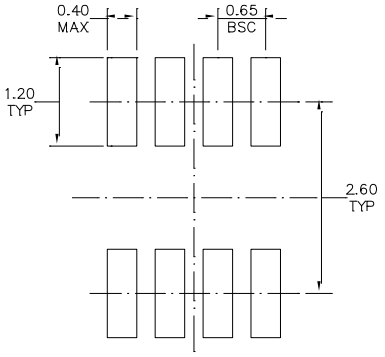
10) R5 and R6 are given for V_{IN} = 12V. R5 and R6 may need to be adjusted if V_{IN} changes, based on the V_{VBS} UVLO rising threshold, falling threshold, and target boost valley threshold.

PACKAGE INFORMATION

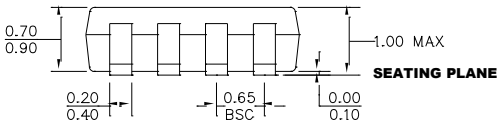
TSOT23-8



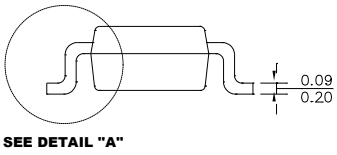
TOP VIEW



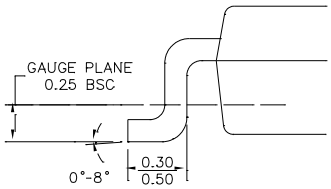
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

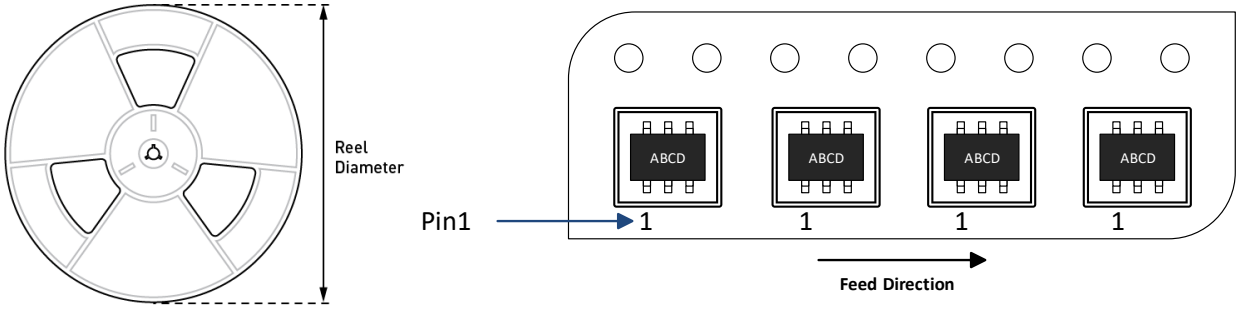


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5493GJ-Z	TSOT23-8	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/21/2023	Initial Release	-