MP5520

2.7V to 16V, Power Loss Protection Management IC with Dual E-Fuses and Power-Sharing Function

DESCRIPTION

The MP5520 is a high-efficiency, monolithic converter designed for power management in enterprise and datacenter SSDs. It integrates dual-input current-limit switches (e-fuses), a bidirectional buck-boost converter, and a bidirectional power-sharing converter.

The low on resistance ($R_{DS(ON)}$) e-fuses are designed for V_{IN} up to 16V and 6V, respectively. Both e-fuses provide input current limiting and can block reverse currents. Soft start (SS) prevents inrush current during system start-up.

The bidirectional buck-boost converter provides energy management. Backup energy is stored in high-voltage capacitors. MPS's patented energy storage and release management control circuit minimizes the storage capacitor (C_{STRG}) requirement. The converter pumps V_{IN} to a higher V_{STRG}, and if there is a V_{IN} outage, the converter releases the energy to the system across a hold-up time. The configurable charging current ramps up V_{STRG} in a controlled manner. Paired with the e-fuses' reverse-current blocking, the backup energy is fully utilized to support the load during V_{IN} loss.

Constant-on-time (COT) control is used when the bidirectional converter releases the energy from C_{STRG}, which minimizes the voltage drop during the transition from charge mode to backup mode. The total solution size is minimized since this converter only requires one inductor.

The bidirectional power-sharing converter provides power sharing between the e-fuses. It can be configured to either boost power-sharing mode or buck power-sharing mode. The internal ADC accurately monitors V_{INx}, I_{INx}, and P_{INx}. To guarantee long-term reliability, the MP5520 offers C_{STRG} health monitoring.

The MP5520 requires a minimal number of readily available, standard external components, and is available in a QFN-37 (5mmx6mm) package.

FEATURES

- Input Current Limit Switches (E-Fuses):
  - Wide V_{INx}: 2.7V to 16V V_{IN1} (E-Fuse 1) and 2.7V to 6V V_{IN2} (E-Fuse 2)
  - Low On Resistance ($R_{DS(ON)}$): 20mΩ E-Fuse 1 and 22mΩ E-Fuse 2
  - Selectable Reverse-Current Blocking
  - Configurable Input Brownout
  - Power Disable Function
- 36V Charge and Backup Converter (PLP):
  - Supports Up to 36V V_{STRG}
  - Charge Operation
    - External Pin to Set V_{STRG} and Power Failure Threshold
    - Configurable Charging Current
  - Backup Operation:
    - Up to 10A Peak Current Capability
    - Up to 7A Valley Current Capability
    - Configurable f_{SW}
- Bidirectional Power-Sharing Converter:
  - Selectable Boost-Sharing Mode or Buck-Sharing Mode
  - Selectable Standalone Mode or Power-Sharing Mode
  - Configurable Regulated Voltage with External FB Resistor or I^2C Control in Standalone Buck Mode
- System:
  - MTP Configurable Up to 1,000 Times
  - Digital I^2C for Status Monitoring and Operation Control
  - Health Monitoring for C_{STRG}
  - Internal 8-Bit ADC to Monitor I_{INx}, V_{INx}, and P_{INx} with a 60kSPS Sampling Rate
  - System Power Failure and Interrupt Indicators
  - Available in a QFN-37 (5mmx6mm) Package

APPLICATIONS

- Enterprise Solid-State Drives (SSDs)
- Power Backup Solutions

TYPICAL APPLICATIONS

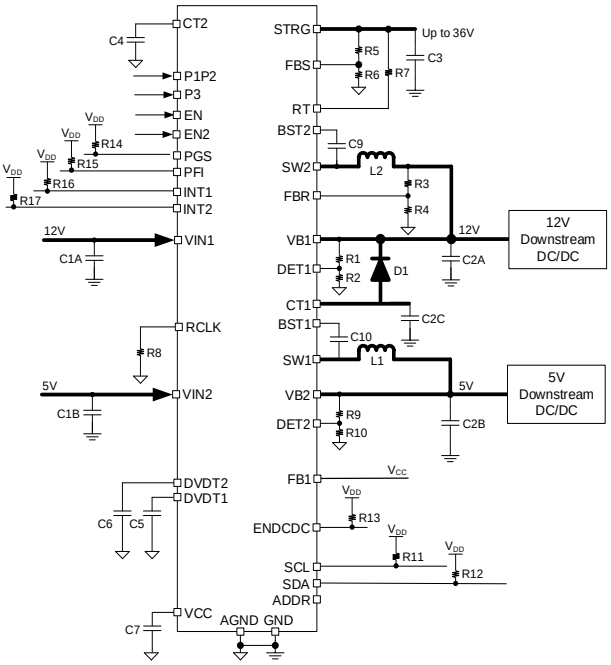


Figure 1: Typical Application 1 (1)

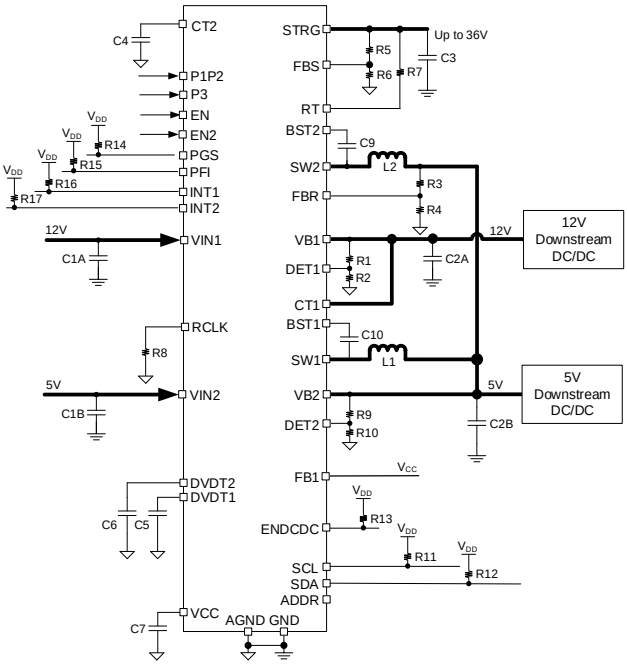


Figure 2: Typical Application 2 (2)

Notes:

1) The power-sharing converter operates in boost-sharing mode. The PLP regulates the 12V bus voltage (V_{BUS}) during buck release. For more details, refer to the Appendix: Logic Flow of Application 1 section on page 63.
2) The power-sharing converter operates in buck-sharing mode. The PLP regulates the 5V V_{BUS} during buck release.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP5520GQJ-xxxx**	QFN-37 (5mmx6mm)	*See Below*	1
EVKT-MP5520	Evaluation Kit	-	-

* For Tape & Reel, add suffix -Z (e.g. MP5520GQJ-xxxx-Z).

** "xxxx" is the configuration code identifier for the register setting stored in the multiple-time programmable (MTP) memory. The default number is "0000". Each "x" can be a hexadecimal value between 0 and F. Contact an MPS FAE to create this unique number.

TOP MARKING

MPSYYWW

MP5520

LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP5520: Part number
LLLLLLL: Lot number

EVALUATION KIT (EVKT-MP5520)

EVKT-MP5520 kit contents (items below can be ordered separately):

#	Part Number	Item	Quantity
1	EV5520-QJ-00A	MP5520 evaluation board	1
2	EVKT-USBI2C-02-BAG	Includes one USB to I^2C communication interface, one USB cable, and one ribbon cable	1
3	MP5520GQJ-xxxx	MP5520 PMIC (can be used for MTP configuration)	2

Order directly from MonolithicPower.com or our distributors.

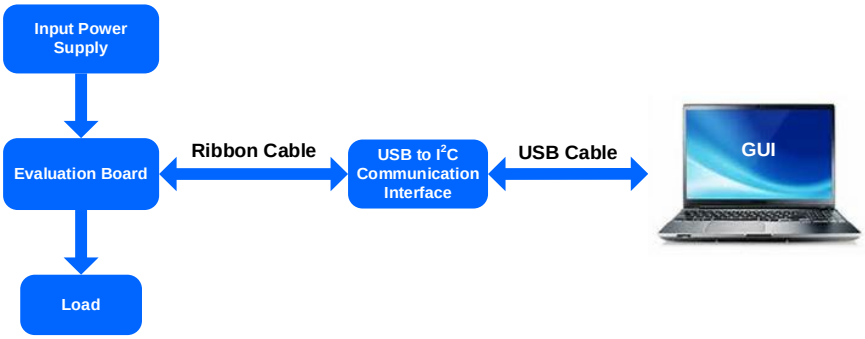
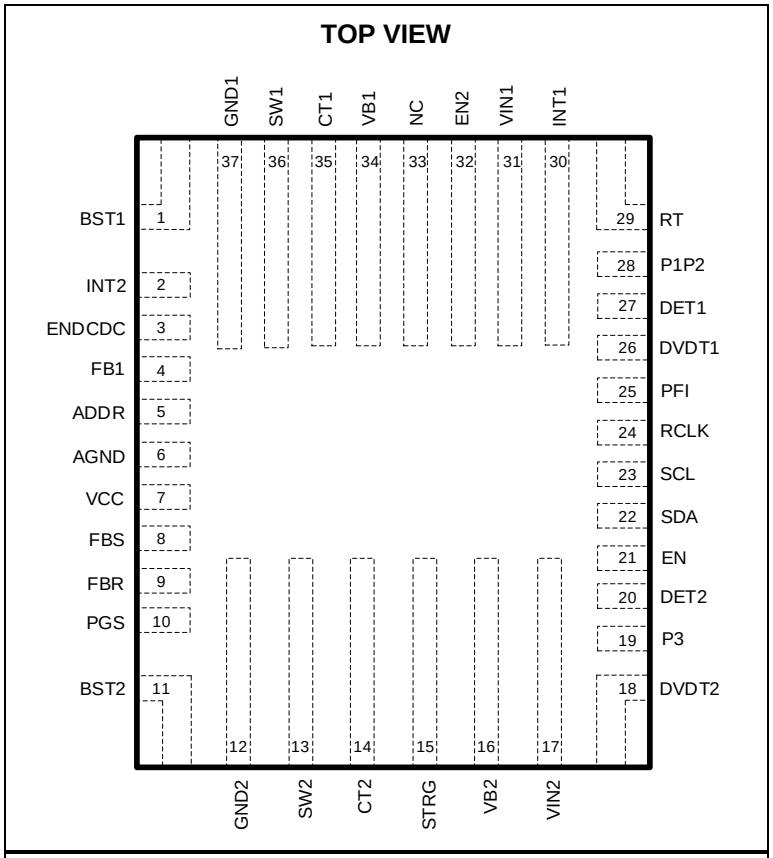


Figure 3: EVKT-MP5520 Evaluation Kit Set-Up

PACKAGE REFERENCE



QFN-37 (5mmx6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST1	**Bidirectional power-sharing converter's high-side MOSFET (HS-FET) bootstrap.** Connect a capacitor (typically 100nF) between the BST1 and SW1 pins to supply the HS-FET's driving voltage.
2	INT2	**Interrupt indication 2.** The INT2 pin is an open-drain output. The CAPTEST_DONE status is reported to the system via INT2. This status can be disabled by the corresponding mask registers. See the STATUS2 (38h) section on page 54 and the MSK_INT2 (3Ah) section on page 55.
3	ENDCDC	**Enable for the downstream DC/DC converters**. The ENDCDC pin is an open-drain output. If EN2 is configured to SAS mode and soft start (SS) for both e-fuses completes, then ENDCDC is pulled high. If EN2 is configured to PCIe mode and e-fuse 1's SS completes, then ENDCDC is pulled high. If the buck release completes, ENDCDC is pulled low.
4	FB1	**Power-sharing converter's output voltage feedback in standalone buck mode.** The internal reference is 0.6V by default. The reference voltage (V_{FB1_REF}) can be configured via the internal I^2C register.
5	ADDR	**I^2C address.** There are three I^2C addresses. Pull the ADDR pin low to set the I^2C address to 33h. Pull ADDR high to set the I^2C address to 35h. Float ADDR to set the I^2C address to 37h.
6	AGND	**Internal signal ground.**
7	VCC	**Internal power supply.** The VCC pin is supplied internally. Connect a minimum 1μF ceramic capacitor between the VCC and AGND pins to guarantee a clean internal power supply.
8	FBS	**Storage voltage feedback.** Connect a voltage divider to the FBS pin to set the storage voltage (V_{STRG}) during the 36V charge and backup converter's (PLP) charging.
9	FBR	**Release voltage feedback.** Connect a voltage divider to the FBR pin to set the regulated release voltage (V_{BUS_RLS}) during PLP release.
10	PGS	**Storage voltage power good (PG) indicator.** The PGS pin is an open-drain output. If V_{STRG} exceeds the I^2C's configured threshold, PGS is pulled high.
11	BST2	**PLP's HS-FET bootstrap.** Connect a capacitor (typically 100nF) between the BST2 and SW2 pins to supply the HS-FET's driving voltage.
12	GND1	**System power ground 1.** The GND1 pin requires thick, wide routing on the board layer to conduct current.
13	SW2	**PLP switching node.** Connect the SW2 pin to one end of the inductor using wide routing to enable the current to flow.
14	CT2	**Connection between the PLP's blocking FET and HS-FET.** Connect a minimum 2.2μF ceramic capacitor between the CT2 pin and power ground to achieve stable operation. The capacitor must have a voltage rating equal to that of the storage capacitor (C_{STRG}).
15	STRG	**Storage voltage.** Connect the STRG pin to C_{STRG} to generate backup energy.
16	VB2	**E-fuse 2 power output.**
17	VIN2	**E-fuse 2 power input.**
18	DVDT2	**E-fuse 2 SS time configuration.** Connect a capacitor between the DVDT2 pin and ground to configure e-fuse 2's SS time (t_{DVDT2}).
19	P3	**Power disable for the e-fuses' on/off control.** If the P1P2 pin is pulled low and the P3 pin is pulled high, then both e-fuses are turned off. There is an internal 500kΩ pull-down resistor. P3 has a 1ms deglitch time.
20	DET2	**E-fuse 2 output voltage detection.** Connect a voltage divider to the DET2 pin to set the detection threshold for e-fuse 2's output voltage (V_{B2}). If V_{B2} is below this threshold, DET2 is triggered. Triggering the DET1 and DET2 pins controls whether the PFI goes high or low, as well as PLP release. There are four control modes: DET1 is only triggered, DET2 is only triggered, both DET1 and DET2 are triggered, and either DET1 or DET2 is triggered.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
21	EN	**Enable for the e-fuses.** Pull the EN pin logic low to turn off the e-fuses.
22	SDA	**I²C interface data.**
23	SCL	**I²C interface clock.** The SCL pin can support up to a 3.4MHz I²C clock.
24	RCLK	**Internal reference clock.** Connect a 100kΩ external resistor to the RCLK pin to set the internal clock frequency.
25	PFI	**Power failure indicator.** The PFI pin is an open-drain output. If DET1 or DET2 is triggered, PFI goes high. During buck release, PFI remains high to indicate buck release.
26	DVDT1	**E-fuse 1 SS time configuration.** Connect a capacitor between the DVDT1 pin and ground to configure e-fuse 1's SS time (t_{DVDT1}).
27	DET1	**E-fuse 1 output voltage detection.** Connect a voltage divider to the DET1 pin to set the detection threshold for e-fuse 1's output voltage (V_{B1}). If V_{B1} is below this threshold, DET1 is triggered. Triggering DET1 and DET2 controls whether the PFI goes high or low, as well as PLP release. There are four control modes: DET1 is only triggered, DET2 is only triggered, both DET1 and DET2 are triggered, and either DET1 or DET2 is triggered.
28	P1P2	**Power disable for the e-fuses' on/off control.** If the P1P2 pin is pulled low and the P3 pin is pulled high, then both e-fuses are turned off. There is an internal 500kΩ pull-down resistor. P1P2 has a 1ms deglitch time.
29	RT	**Resistor connection for the capacitor health test.** Connect an external resistor to the RT pin to set the discharging current for the capacitor test.
30	INT1	**Interrupt pin 1.** The INT1 pin is an open-drain output. The over-current (OC), over-voltage (OV), and C_{STRG} failure statuses are reported to the system via INT1. These statuses can be disabled by the corresponding mask registers. See the STATUS1 (37h) section on page 53 and the MSK_INT1 (39h) section on page 54.
31	VIN1	**E-fuse 1 power input.**
32	EN2	**Mode selection.** The EN2 pin selects PCIe mode or SAS mode. If EN2 is pulled high, the MP5520 enters SAS mode, where the e-fuses turn on simultaneously only if the VIN1 pin voltage (V_{IN1}) and the VIN2 pin voltage (V_{IN2}) exceed their UVLO thresholds (V_{IN1_UVLO} and V_{IN2_UVLO}, respectively). In SAS mode, boost charge starts after the e-fuses turn on, DET1 and DET2 both exceed the PFI low threshold, and FBR exceeds the FBR charging threshold. If EN2 is pulled low, the MP5520 enters PCIe mode, where the e-fuses can be turned on separately. If V_{IN1} exceeds V_{IN1_UVLO}, e-fuse 1 turns on. Boost charge starts if e-fuse 1 is on, DET1 exceeds the PFI low threshold, and FBR exceeds the FBR charging threshold.
33	NC	**No connection.** It is recommended to float the NC pin.
34	VB1	**E-fuse 1 power output.**
35	CT1	**Connection to the power-sharing converter's HS-FET drain.** In boost-sharing mode, connect the CT1 pin to VB1 using an external diode for reverse-current blocking between VB1 and CT1. Connect a minimum 0.1µF ceramic capacitor between CT1 and power ground to achieve stable operation. In buck-sharing mode, CT1 and VB1 can be connected directly. The capacitor must have a voltage rating equal to that of e-fuse 1's output capacitor.
36	SW1	**Bidirectional power-sharing converter switching node.** Connect the SW1 pin to the power-sharing converter's inductor using wide routing to enable the current to flow.
37	GND2	**System power ground 2.** The GND2 pin requires thick, wide routing on the board layer to conduct current.

ABSOLUTE MAXIMUM RATINGS (3)

VIN1 .....-0.3V to +18V
VB1, CT1 .....-0.3V to +18V
VIN2 .....-0.3V to +6.5V
VB2 .....-0.3V to +6.5V
STRG .....-0.3V to +40V
SW1 .....
-0.3V (-5V < 10ns) to VIN1 + 0.7V (23V < 10ns)
SW2 .....
-0.3V (-5V < 10ns) to STRG + 0.7V (45V < 10ns)
BST1 ..... SW1 + VCC
BST2 ..... SW2 + VCC
CT2, RT 40V
ADDR, RCLK, or EN2 .....-0.3V to +5.5V
All other pins .....-0.3V to +6V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Continuous power dissipation (4) 4W

ESD Ratings

Human body model (HBM) 2000V
Charged-device model (CDM).....750V

Recommended Operating Conditions (5)

VIN1 .....2.7V to 16V
VB1 .....2.7V to 16V
VIN2 .....2.7V to 5.7V
VB2 .....2.7V to 5.7V
STRG .....3V to 36V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-37 (5mmx6mm)…… 29.5…15.5...°C/W

Notes:

3) Exceeding these ratings may damage the device.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
5) The device is not guaranteed to function outside of its operating conditions.
6) The θ_{JA} value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 5V, V_{CC} = 5V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
E-Fuse 1						
V_{IN1} under-voltage lockout (UVLO) rising threshold	$V_{IN1\_UVLO\_RISING}$	I²C-configurable, register 03h, bits[7:6] = 01	8.75	9.25	9.75	V
V_{IN1} UVLO falling threshold	$V_{IN1\_UVLO\_FALLING}$	I²C-configurable, register 03h, bits[7:6] = 01, register 03h, bits[5:4] = 01	8	8.5	9	V
E-fuse 1 on resistance	$R_{DS(ON)1}$			20		mΩ
E-fuse 1 leakage current	I_{LK1}			1		μA
VB1 clamping voltage	V_{CLAMP1}		13.2	13.7	14.2	V
VB1 over-voltage (OV) threshold	V_{OV1_TH}		13.8	14.3	14.9	V
E-fuse 1 current limit	I_{LIM1}	Register 3Bh, bits[4:0] = 01011	1.7	2	2.3	A
VB1 soft-start (SS) time	t_{DVDT1}	C_{DVDT1} = 10nF, 10% to 90% of V_{B1}		2.7		ms
E-Fuse 2						
V_{IN2} UVLO rising threshold	$V_{IN2\_UVLO\_RISING}$	I²C-configurable, register 02h, bits[7:6] = 10	3.45	3.75	4.05	V
V_{IN2} UVLO falling threshold	$V_{IN2\_UVLO\_FALLING}$	I²C-configurable, register 02h, bits[7:6] = 10, register 02h, bits[5:4] = 11	2.5	2.8	3.1	V
E-fuse 2 on resistance	$R_{DS(ON)2}$			22		mΩ
E-fuse 2 leakage current	I_{LK2}			2		μA
VB2 clamping voltage	V_{CLAMP2}		5.7	6	6.3	V
VB2 OV threshold	V_{OV2_TH}		5.9	6.3	6.7	V
E-fuse 2 current limit	I_{LIM2}	Register 3Ch, bits[4:0] = 01011	1.7	2	2.3	A
VB2 SS time	t_{DVDT2}	C_{DVDT2} = 10nF, 10% to 90% of V_{B2}		2.5		ms
36V Charge and Backup Converter						
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS\_PLP}$			50		mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS\_PLP}$			35		mΩ
High-side (HS) blocking FET on resistance	$R_{DS\_DIS\_PLP}$			37		mΩ
FBR charging threshold	V_{CH_FBR}			0.816		V
FBR release threshold	V_{RLS_FBR}			0.8		V
Pre-charge current	I_{PRE_CHRG}	Register 0Eh, bits[5:4] = 00		50		mA
Switching frequency of release buck in backup mode	f_{SW_RLS}	Register 08h, bits[3:2] = 01		1		MHz
Low-side (LS) valley current limit of buck release	I_{LS_PLP}	Register 08h, bits[6:5] = 01, T_J = 25°C	2.4	3	3.6	A

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, V_{CC} = 5V, T_J = -40°C to +125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Boost refresh threshold	$V_{S\_REFRESH}$		100.5	101	101.85	% of V_{REF}
Capacitor test measurement repeatability (8)		$V_{S\_REFRESH}$ = 101%, LSB timer = 0.5ms, V_{STRG} sensing method	-3		+3	%
Bidirectional Power-Sharing Converter						
HS-FET on resistance	$R_{DS(ON)\_HS\_PS}$			30		mΩ
LS-FET on resistance	$R_{DS(ON)\_LS\_PS}$			18		mΩ
Switching frequency in standalone mode	f_{SW_PS}	Register 0Fh, bits[1:0] = 01		1		MHz
LS valley current limit	I_{LS_PS}	Register 0Fh, bits[3:2] = 01, T_J = 25°C	2.2	3	3.8	A
System						
VCC regulation voltage		Max V_{IN1}, V_{IN2}, V_{B1}, V_{B2} > 5V	4.7	5	5.3	V
E-fuse turn-on threshold with VIN recovery	V_{ON}	Register 01h, bits[3:2] = 00		50		mV
E-fuse turn-on delay with VIN recovery	t_{ON_DELAY}	Register 01h, bits[1:0] = 00		0.85		ms
E-fuse reverse-current blocking threshold	I_{RCB}			240		mA
DET1, DET2, FBR, and FBS reference voltage	V_{REF}		0.792	0.8	0.808	V
		T_J = -40°C to +125°C	0.788	0.8	0.812	
FB1 reference voltage	V_{REF_FB1}	Register 10h, bits[6:0] = 0111011	0.594	0.6	0.606	V
		T_J = -40°C to +125°C, register 10h, bits[6:0] = 0111011	0.591	0.6	0.609	
DETx, FBR, FBS, and FB1 leakage current	I_{LKG}			10		nA
PFI low threshold	V_{PFI_L}		0.808	0.816	0.824	V
		T_J = -40°C to +125°C	0.8	0.816	0.832	
PFI high threshold	V_{PFI_H}		0.792	0.8	0.808	V
		T_J = -40°C to +125°C	0.788	0.8	0.812	
PFI rising delay	$t_{D\_PFI\_H}$			2		µs
PFI falling delay	$t_{D\_PFI\_L}$	Register 06h, bits[2:1] = 00		200		µs
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{HYS}			25		°C
Thermal warning (8)	T_{WRN}			120		°C
Thermal warning hysteresis (8)	T_{WRN_HYS}			20		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 5V, V_{CC} = 5V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Logic Interface						
High-level input voltage	V_{IH1}	P1P2 and P3	1.2			V
	V_{IH2}	SDA, SCL, and EN	1.4			V
Low-level input voltage	V_{IL}	P1P2, P3, SDA, SCL, and EN			0.5	V
Input leakage current	I_{LKG_SDA}	V_{SDA} = 5V		10		nA
	I_{LKG_SCL}	V_{SCL} = 5V		10		nA
	I_{LKG_EN}	V_{EN} = 5V		10		nA
	I_{LKG_EN2}	V_{EN2} = 5V		10		nA
	I_{LKG_P1P2}	V_{P1P2} = 5V		10		µA
	I_{LKG_P3}	V_{P3} = 5V		10		µA
	I_{LKG_ADDR}	V_{ADDR} = 5V		10		nA
Output leakage current	I_{LKG_PFI}	V_{PFI} = 5V		2		µA
	I_{LKG_PGS}	V_{PGS} = 5V		2		µA
	I_{LKG_ENDCDC}	V_{ENDCDC} = 5V		10		nA
	I_{LKG_INT1}	V_{INT1} = 5V		2		µA
	I_{LKG_INT2}	V_{INT2} = 5V		2		µA
Low-level output voltage	V_{OUT_L}	SDA, INT1, INT2, PGS, PFI, and ENDCDC sink current = 3mA			0.2	V

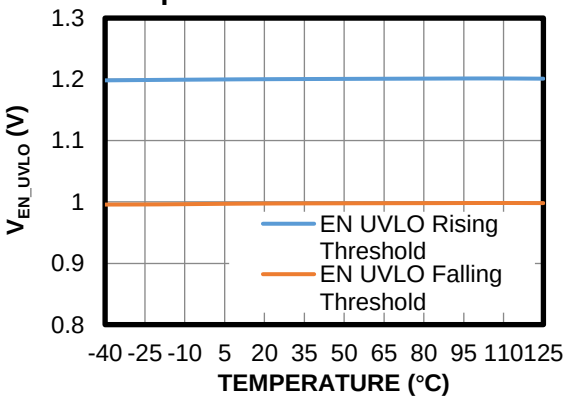
Notes:

7) Not tested in production. Guaranteed by over-temperature correlation.
8) Guaranteed by design or engineering sample characterization.

TYPICAL CHARACTERISTICS

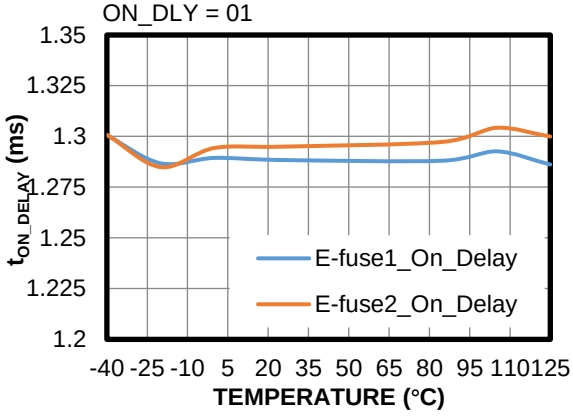
V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

EN UVLO Threshold vs. Temperature



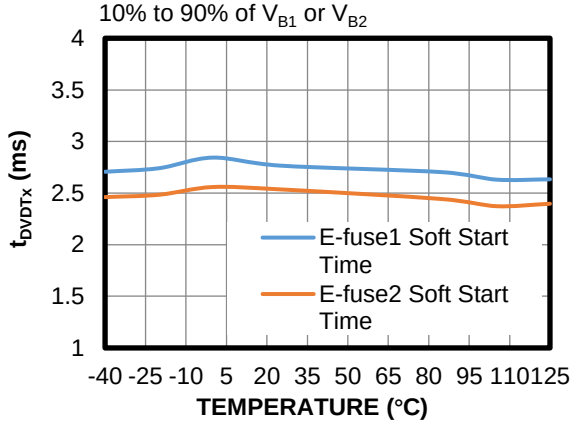
E-Fuse Turn-On Delay vs. Temperature

ON_DLY = 01

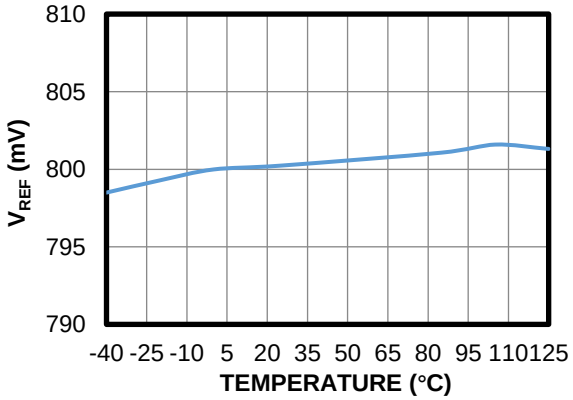


E-Fuse Soft-Start Time vs. Temperature

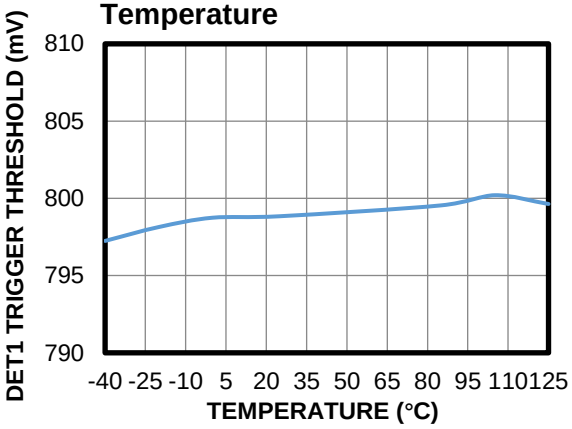
C_{DVDT1} = C_{DVDT2} = 10nF,
10% to 90% of V_{B1} or V_{B2}



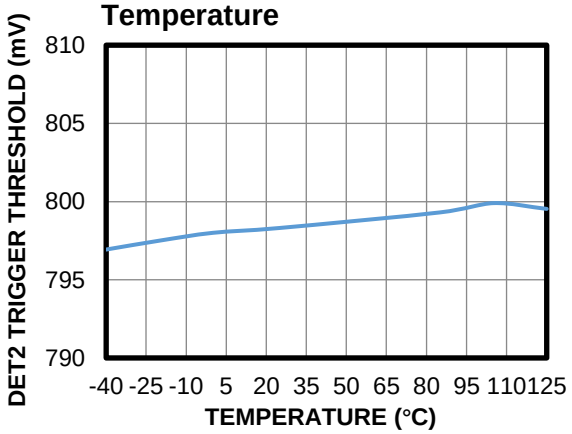
FBS Reference Voltage vs. Temperature



DET1 Trigger Threshold vs. Temperature



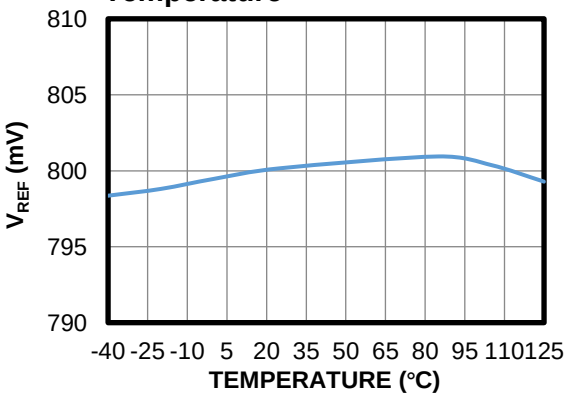
DET2 Trigger Threshold vs. Temperature



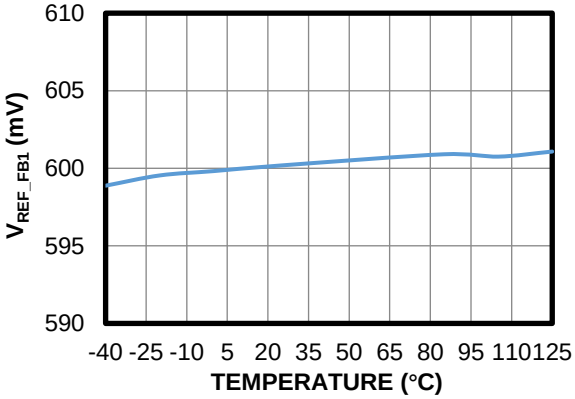
TYPICAL CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

FBR Release Threshold vs. Temperature

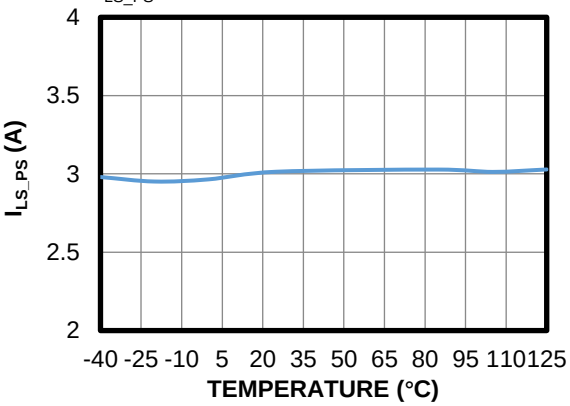


FB1 Reference Voltage vs. Temperature

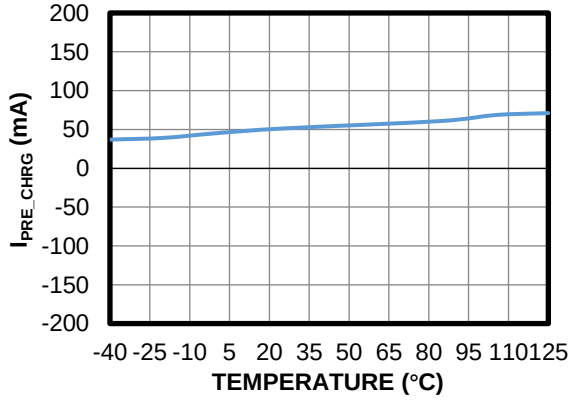


Power-Sharing Converter Valley Current Limit vs. Temperature

I_{LS_PS} = 3A

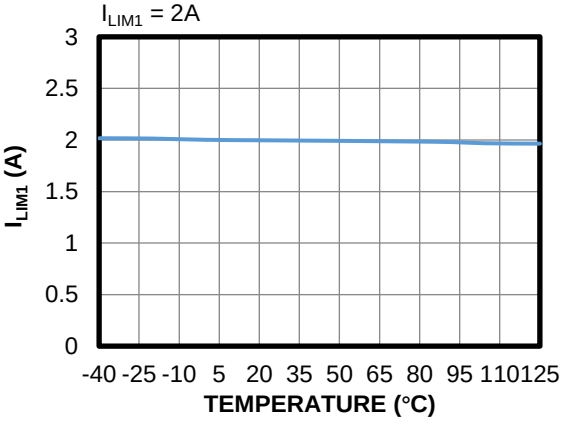


Boost Pre-Charge Current vs. Temperature



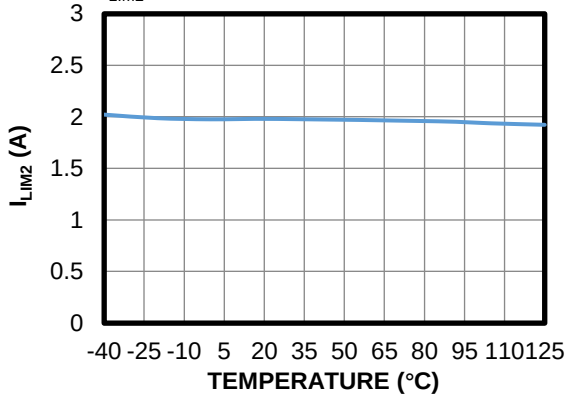
E-Fuse 1 Current Limit vs. Temperature

I_{LIM1} = 2A



E-Fuse 2 Current Limit vs. Temperature

I_{LIM2} = 2A

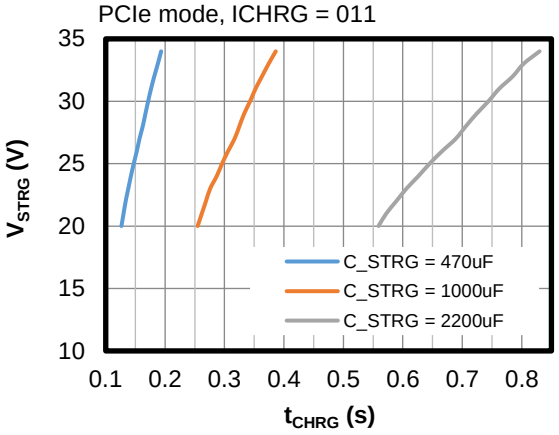


TYPICAL CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

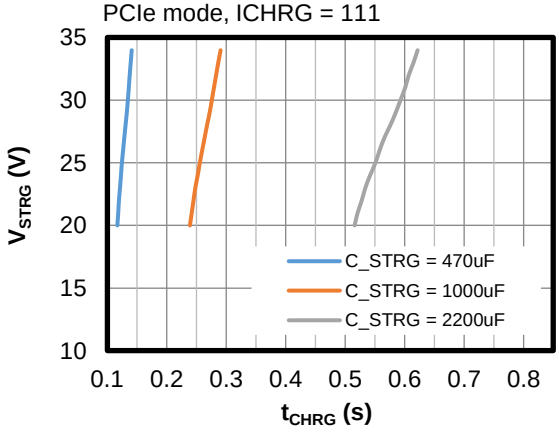
Storage Voltage vs. Charge Time

PCIe mode, ICHRG = 011



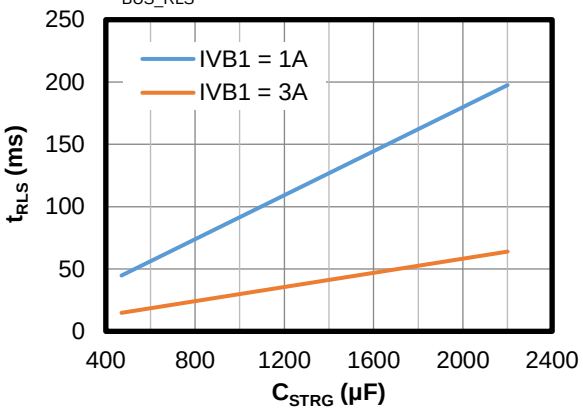
Storage Voltage vs. Charge Time

PCIe mode, ICHRG = 111



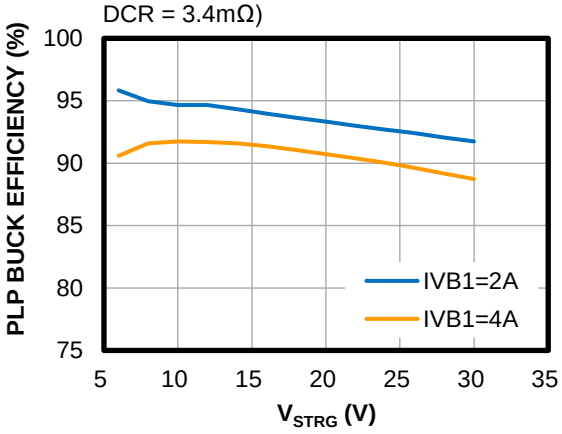
Release Time vs. Storage Capacitance

V_{BUS_RLS} = 6V



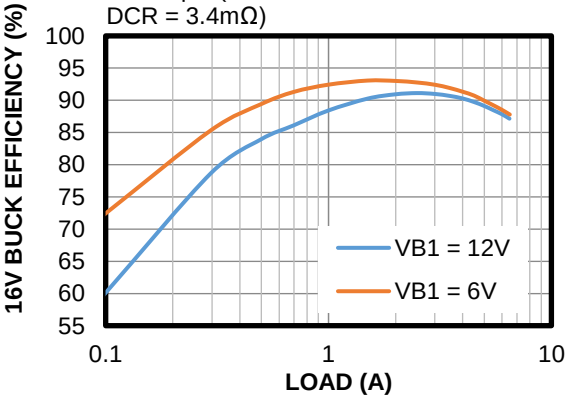
PLP Buck Efficiency vs. Storage Voltage

L = 1.5µH (MPL-AY1050-1R5, DCR = 3.4mΩ)



Power-Sharing Converter Efficiency vs. Load (Standalone Buck Mode)

L = 1.5µH (MPL-AY1050-1R5, DCR = 3.4mΩ)

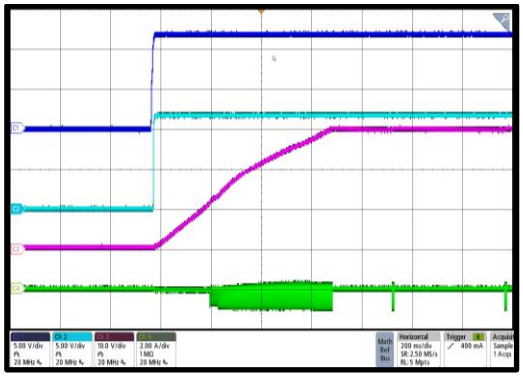


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

Input Start-Up

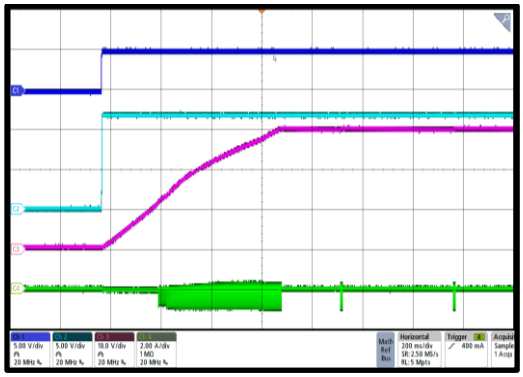
I_{VB1} = 3A



200ms/div.

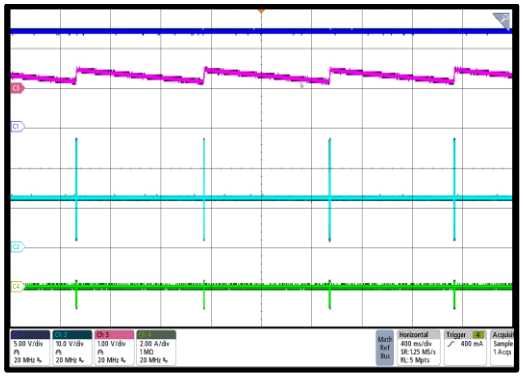
Start-Up through EN

I_{VB1} = 3A



200ms/div.

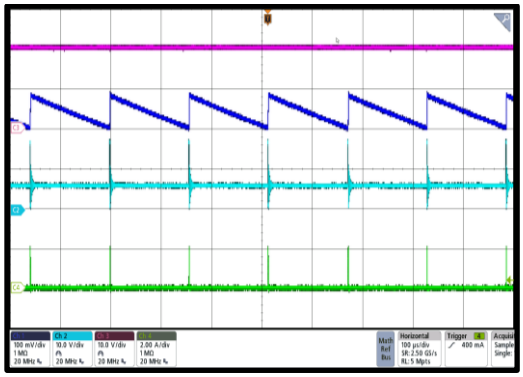
Boost Steady State



400ms/div.

PLP Buck Steady State

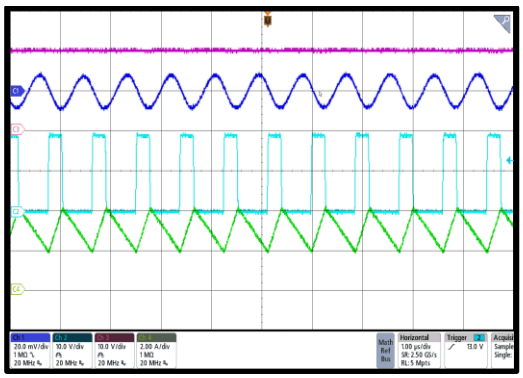
V_{STRG} = 20V, I_{VB1} = 0A, 22µF ceramic capacitor on VB1



100µs/div.

PLP Buck Steady State

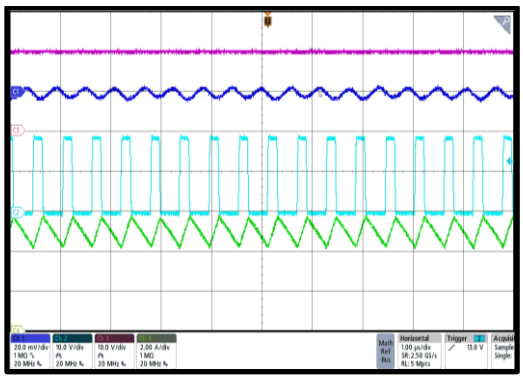
V_{STRG} = 20V, I_{VB1} = 3A, 22µF ceramic capacitor on VB1



1µs/div.

PLP Buck Steady State

V_{STRG} = 20V, I_{VB1} = 5A, 22µF ceramic capacitor on VB1



1µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

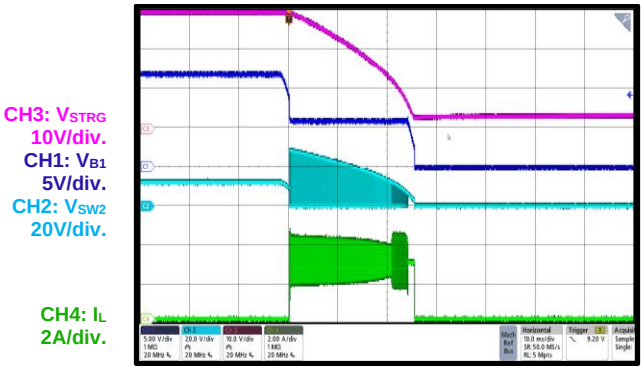
PLP Buck Release

I_{VB1} = 1A

20ms/div.

PLP Buck Release

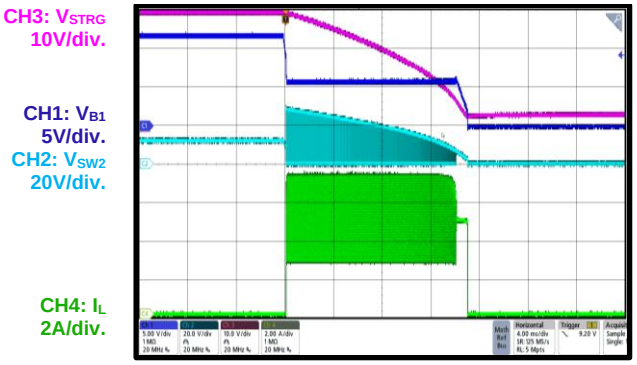
I_{VB1} = 3A



10ms/div.

PLP Buck Release

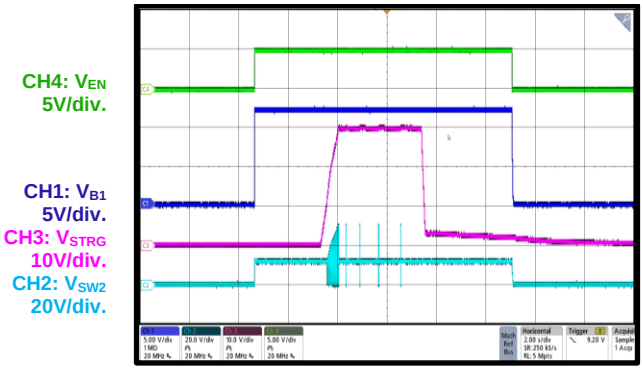
I_{VB1} = 5A



4ms/div.

Start-Up Sequence

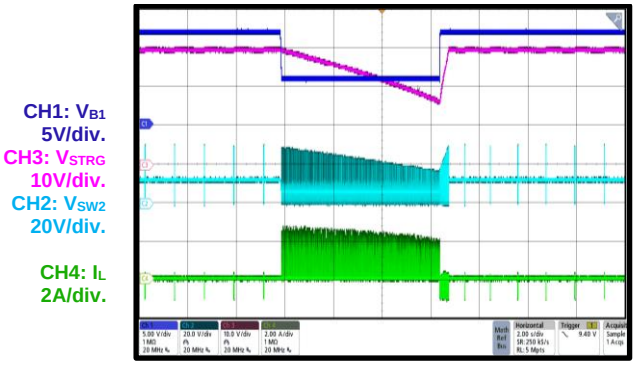
Starts up in the following sequence: EN on, ENCH bit on, ENCH bit off, EN off



2s/div.

VIN1 Shutdown and Recovery during Release

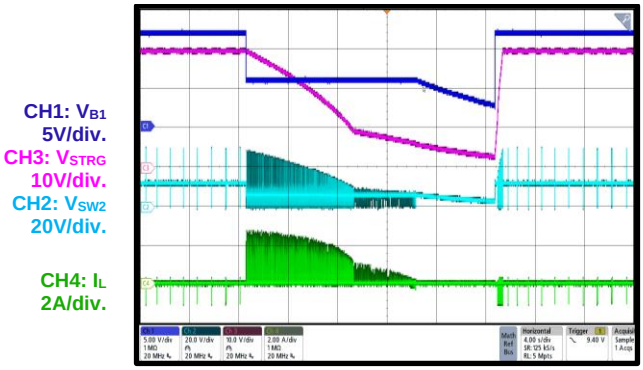
QPOR = 0, I_{VB1} = 0A



2s/div.

VIN1 Shutdown and Recovery during Release

QPOR = 1, I_{VB1} = 0A



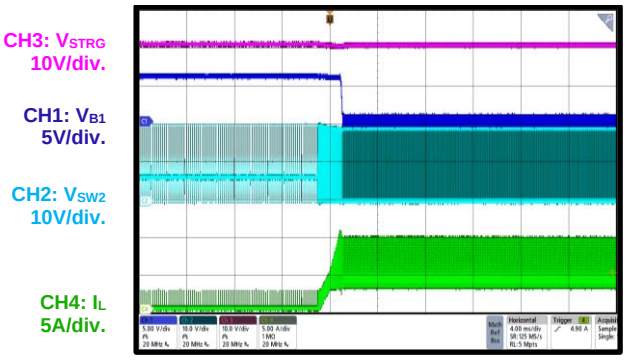
4s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

PLP Buck OCP

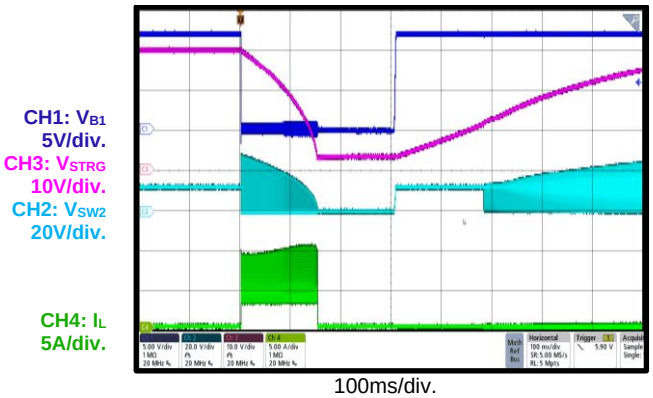
V_{STRG} = 20V, I_{LIM_RLS} = 3A, add 7A load (3.2mA/µs) on VB1



4ms/div.

VB1 SCP and Recovery

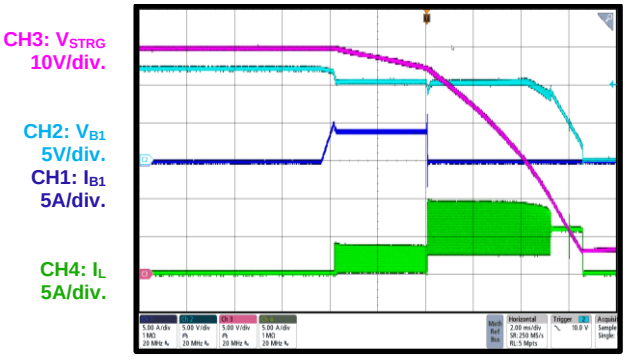
I_{LIM_RLS} = 3A, short VB1 with wire, then recover



100ms/div.

CLBK Function

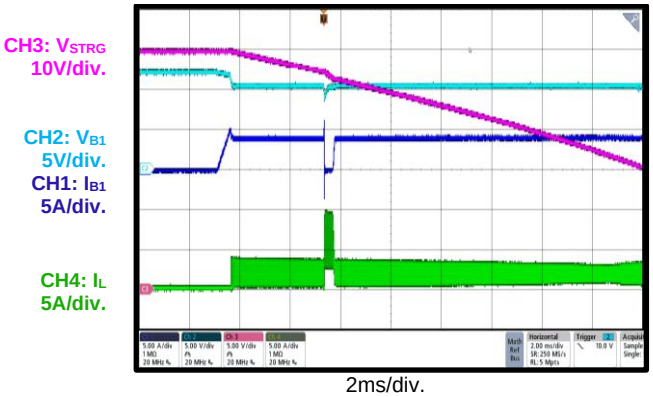
QPOR = 1, MAX_RLS_TIMER_CLBK = 6.3ms, VS_TH_CLBK = 92%



2ms/div.

CLBK Function

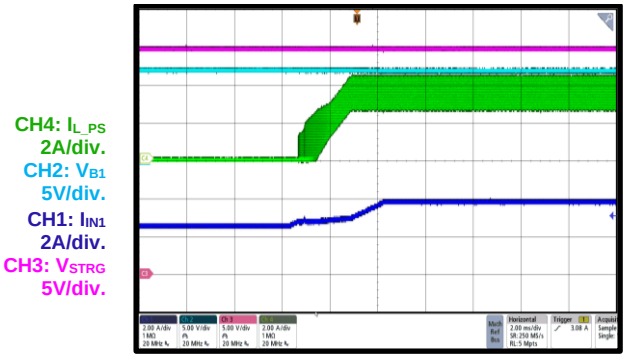
QPOR = 0, MAX_RLS_TIMER_CLBK = 6.3ms, VS_TH_CLBK = 92%



2ms/div.

Boost Power Sharing

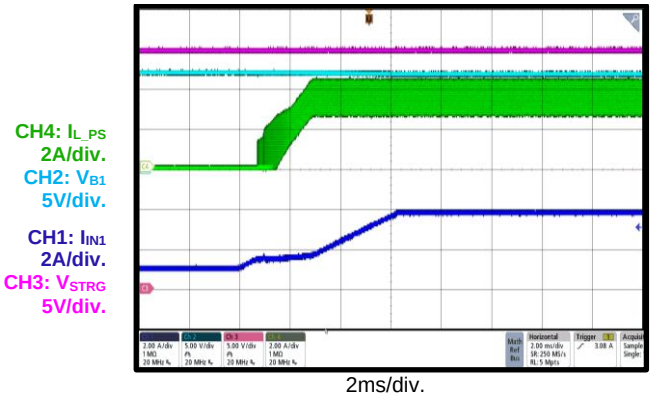
SAS mode, V_{IN1} = 12V, V_{IN2} = 5V, I_{LIM1} = 4A, I_{LIM2} = 6A, add 2.5A to 5A load on VB1, PWR_SHARE_LIM = I_{LIM} x 62%



2ms/div.

Boost Power Sharing

SAS mode, V_{IN1} = 12V, V_{IN2} = 5V, I_{LIM1} = 4A, I_{LIM2} = 6A, add 1A to 5A load on VB1, PWR_SHARE_LIM = I_{LIM} x 31%



2ms/div.

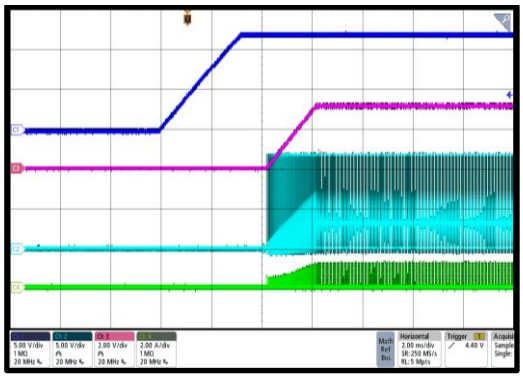
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

Power-Sharing Converter Input Start-Up

Standalone mode, R_{FB1_UP} = 64.9kΩ, R_{FB1_LOWER} =15kΩ, start-up without load

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

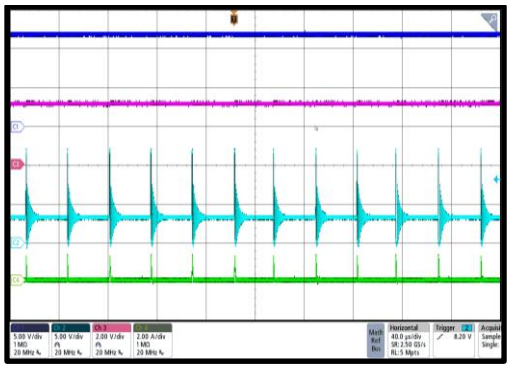


2ms/div.

Power-Sharing Converter Steady State

Standalone mode, without load

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

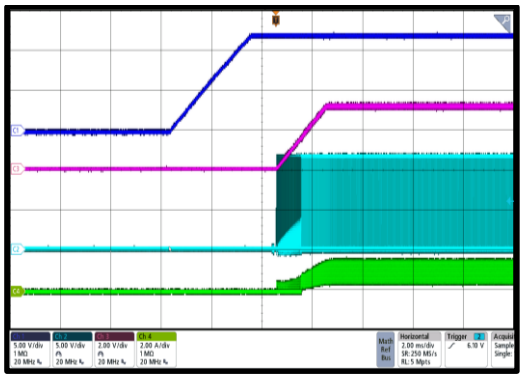


40µs/div.

Power-Sharing Converter Input Start-Up

Standalone mode, start-up with 1A load

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

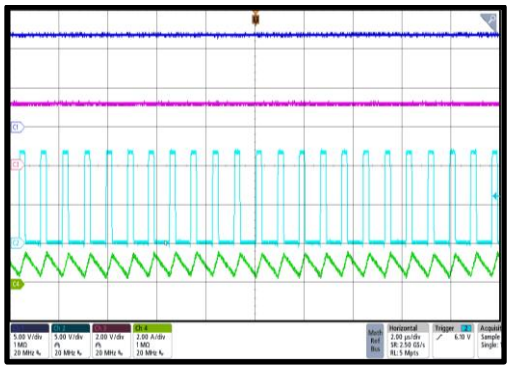


2ms/div.

Power-Sharing Converter Steady state

Standalone mode, 1A load

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

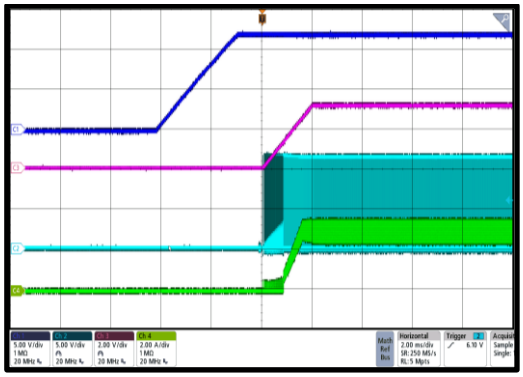


2µs/div.

Power-Sharing Converter Input Start-Up

Standalone mode, start-up with 3A load

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

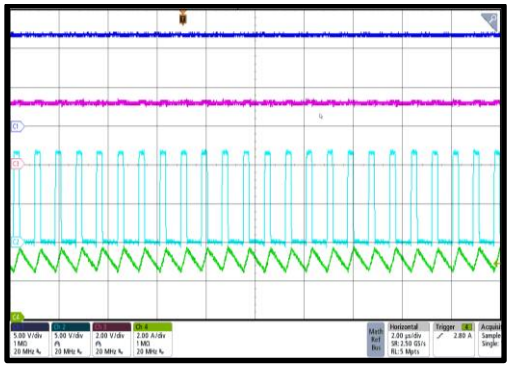


2ms/div.

Power-Sharing Converter Steady state

Standalone mode, 3A load

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.



2µs/div.

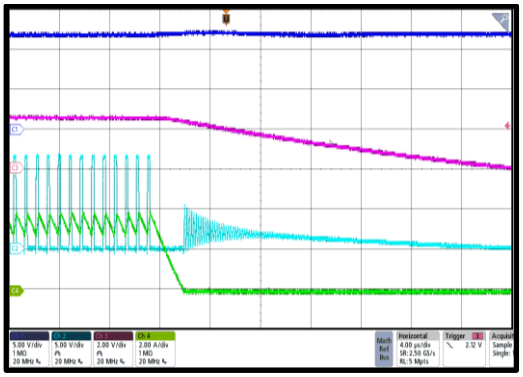
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN1} = 12V, V_{IN2} = 0V, V_{STRG} = 27.2V, V_{DET1} = 8.96V, V_{BUS_RLS} = 6V, L_{PLP} = L_{PS} = 1.5µH, T_A = 25°C, unless otherwise noted.

Power-Sharing Converter OCP

I_{LIM_RLS} = 3A

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.

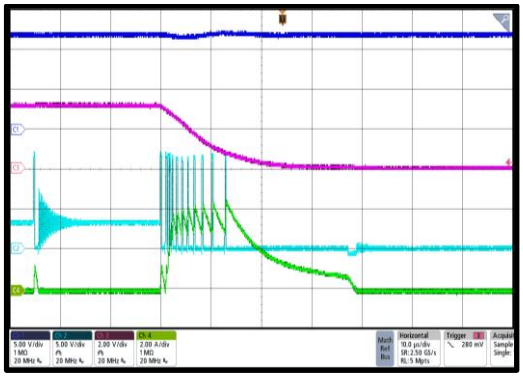


4µs/div.

Power-Sharing Converter SCP Entry

I_{LIM_RLS} = 3A

CH1: V_{B1} 5V/div.
CH3: PS Output 2V/div.
CH2: V_{SW1} 5V/div.
CH4: I_{L_PS} 2A/div.



10µs/div.

FUNCTIONAL BLOCK DIAGRAM

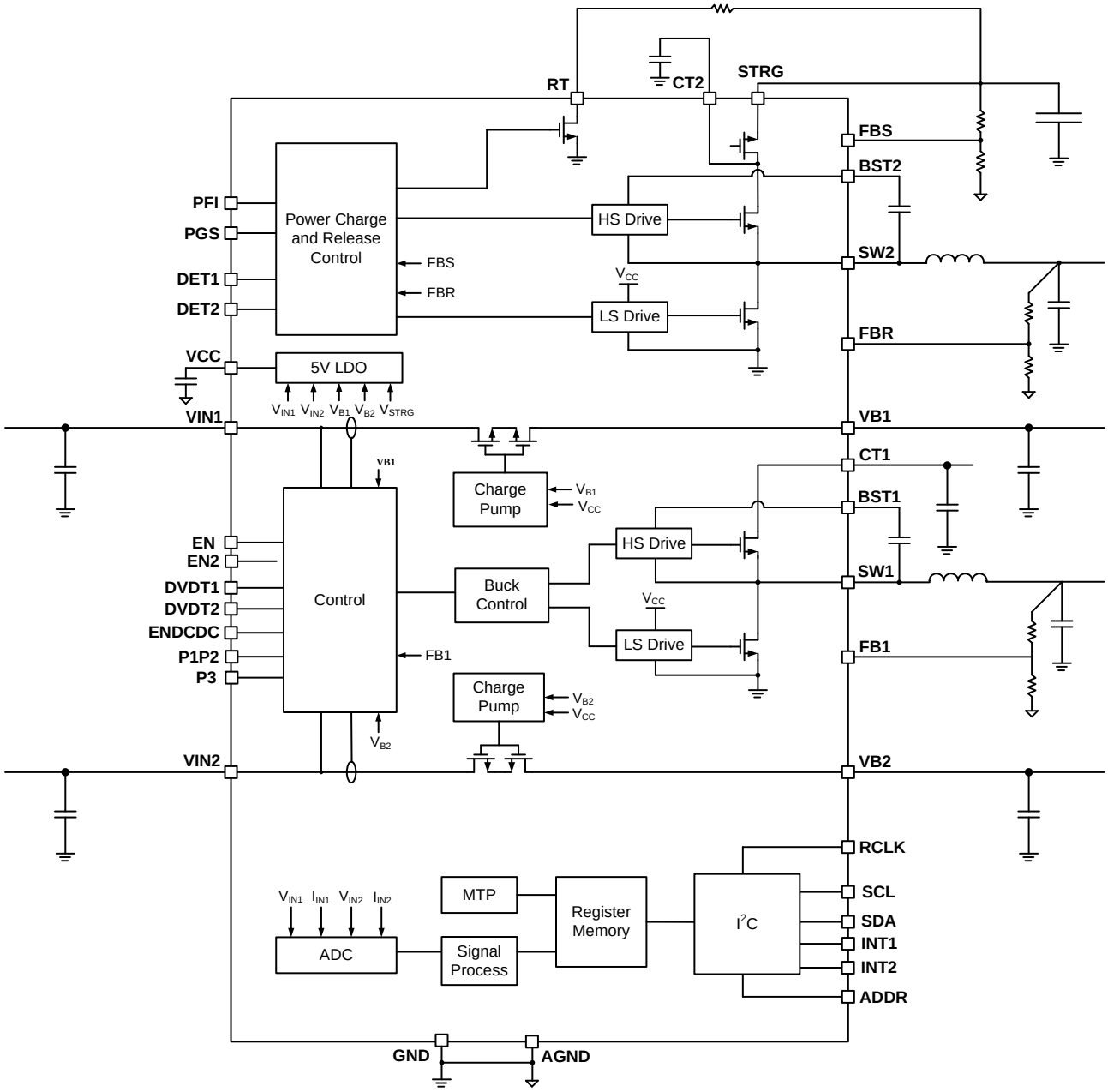


Figure 4: Functional Block Diagram

OPERATION

The MP5520 is an energy backup and management unit that is available in a QFN-37 (5mmx6mm) package. It provides a compact and efficient energy management solution for solid-state drive (SSD) applications. MPS's patented, lossless energy storage and release management circuits use a bidirectional charge and backup converter to achieve optimal energy transfer and provide cost-effective energy storage solutions. An additional bidirectional power-sharing converter is integrated to implement power sharing under heavy-load conditions.

The MP5520 also provides an I^2C interface to write control commands and monitor the system status. The internal analog-to-digital converter (ADC) accurately monitors the input voltages (V_{INx}), input currents (I_{INx}), and input powers (P_{INx}) (where x = 1 or 2) . The MP5520 offers health monitoring for the storage capacitor (C_{STRG}).

Internal Clock (RCLK)

The MP5520's internal clock (RCLK) generates an accurate timing reference. The internal clock is critical for the capacitor health test and input power monitoring. This reference clock's operating frequency is determined by the resistor connected to the RCLK pin. It is recommended to connect a 100kΩ resistor between the RCLK pin and power ground for normal operation.

E-Fuses' Soft Start (SS) (DVDT1 and DVDT2)

The e-fuses provide soft start (SS) to prevent an input inrush current between VINx and VBx. The external capacitors connected to the DVDT1 and DVDT2 pins set the SS time for e-fuse 1 (t_{DVDT1}) and e-fuse 2 (t_{DVDT2}), respectively. The DVDTx capacitors (C_{DVDTx}) are charged by an internal current source (about 2.8μA) and becomes saturated at about 1V.

When the e-fuses operate separately, t_{DVDT1} can be calculated with Equation (1):

$$t_{DVDT1}\ (ms) = 0.34 \times C_{DVDT1}\ (nF) \quad (1)$$

Where t_{DVDT1} is the SS time for V_{B1} to rise from 0V to V_{IN1} (12V), and C_{DVDT1} is the external capacitor connected to DVDT1.

t_{DVDT2} can be calculated with Equation (2):

$$t_{DVDT2}\ (ms) = 0.28 \times C_{DVDT2}\ (nF) \quad (2)$$

Where t_{DVDT2} is the SS time of V_{B2} rising from 0V to V_{IN2} (5V), and C_{DVDT2} is the external capacitor connected to DVDT2.

Both e-fuses can support pre-biased start-up as long as V_{INx} exceeds its under-volage lockout (UVLO) threshold (V_{IN1_UVLO} and V_{IN2_UVLO}, respectively) (see Figure 5).

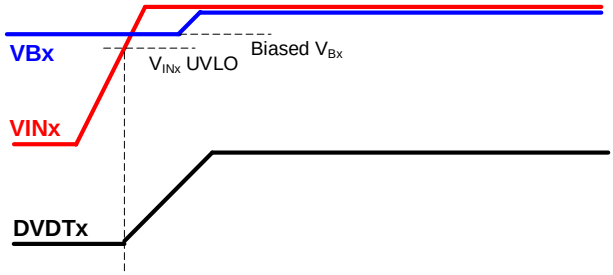


Figure 5: E-Fuses Turn On with Biased V_{Bx}

E-Fuses' Current Limits

In steady state, the input currents flowing through e-fuse 1 (I_{IN1}) and e-fuse 2 (I_{IN2}) are limited based on the current limit settings in register 3Bh, bits[4:0] and register 3Ch, bits [4:0], respectively. The current limits of e-fuse 1 (I_{LIM1}) and e-fuse 2 (I_{LIM2}) are configurable between 1A and 6A.

High-side MOSFET (HS-FET) Drain of the Power-Sharing Converter (CT1)

The CT1 pin is the connection point between the power-sharing converter's high-side MOSFET (HS-FET) drain and VB1. In boost-sharing mode, CT1 can be connected to VB1 using an external diode to achieve reverse-current blocking between VB1 and CT1. Connect a minimum 0.1μF ceramic capacitor between CT1 and power ground to achieve stable operation. In buck-sharing mode, CT1 and VB1 can be connected directly. The capacitor must have a voltage rating equal to that of e-fuse 1's output capacitor.

Blocking FET Source of the 36V Charge and Backup Converter (PLP) (CT2)

An internal blocking FET placed between the HS-FET of the 36V charge and backup converter (PLP) and the STRG pin limits the current during the pre-charge stage. The CT2 pin is the connection point between the blocking FET and the HS-FET. Typically, a minimum 2.2µF capacitor should be connected to CT2. The capacitor's voltage rating must be equal to that of C_{STRG}.

If the ENCH bit is set to 0, the blocking FET turns off, and the PLP stops switching.

E-Fuses' Enable (EN) Control

The EN pin works with the EN1 and EN2 bits to enable the internal circuit of the e-fuses. The e-fuses are enabled after the EN pin and the corresponding ENx bit goes high. In application, the EN pin cannot be connected to a voltage exceeding 6V.

When the EN pin is pulled low, both e-fuses are forced off. At the same time, the buck release circuit is initiated to support the downstream load.

Mode Selection (EN2)

The EN2 pin selects PCIe mode or SAS mode. If EN2 is pulled high, the MP5520 is configured as SAS mode, where the e-fuses turn on simultaneously only if the VIN1 voltage (V_{IN1}) and VIN2 voltage (V_{IN2}) exceed their UVLO thresholds (V_{IN1_UVLO} and V_{IN2_UVLO}, respectively). In SAS mode, boost charge starts after the e-fuses turn on, DET1 and DET2 exceed the PFI low threshold and FBR exceeds the FBR charging threshold.

If EN2 is pulled low, MP5520 is configured as PCIe mode, where the e-fuses can be turned on separately. If V_{IN1} exceeds V_{IN1_UVLO}, e-fuse 1 turns on. Boost charge starts if e-fuse 1 is on, DET1 exceeds the PFI low threshold, and FBR exceeds the FBR charging threshold. Only DET1 controls the power backup.

In real applications, EN2 can be connected to VCC or power ground directly without requiring a resistor. Table 1 shows the detailed configurations for PCIe mode and SAS mode.

Table 1: PCIe Mode and SAS Mode Configurations

Items	PCIe Mode	SAS Mode
E-fuse 2	Disable	Enable
E-FUSE_ ON_CTRL	E-fuse 1 turns on only if V_{IN1} > V_{IN1_UVLO} and EN is pulled high	Both e-fuses turn on only if V_{IN1} > V_{IN1_UVLO} and V_{IN2} > V_{IN2_UVLO}, respectively, and EN is pulled high
DET mode	Only DET1 controls the power backup	When either DET1 or DET2 is triggered, release occurs
ENDCDC	Only regarding V_{B1}	Regarding both V_{B1} and V_{B2}
Power-sharing converter enable	Disabled	Decided by code
Power-sharing converter mode	Standby mode	Power-sharing mode

Enable Control of the 36V Charge and Backup Converter (PLP) (ENCH)

If the ENCH bit is set to 1, the PLP is enabled. When FBR and DET exceed the FBR charging threshold and the PFI low threshold, respectively, the MP5520 begins to charge up the storage voltage (V_{STRG}). When the ENCH bit it is set to 0, the boost charge is terminated.

The ENCH bit also controls the device's buck release. If the ENCH bit is set to 0 and input power loss occurs, the buck release circuit does not become activated to support the downstream DC/DC.

Fast Discharge of the Storage Capacitor

The MP5520 can initiate fast discharge when the following conditions are met:

1. The STRG_DISCHRG_EN bit is set to 1 in register 09h (RLS_CTRL2).
2. The DISCHRG_PATH_ISO bit is set to 0 in register 07h (CHRG_CTRL2).
3. The ENCH_DISCHRG bit is set 1 in register 41h (SYS_CTRL2).
4. If V_{STRG} exceeds 2.9V.
5. The ENCH bit is set to 0 in register 06h (CHRG_CTRL1).

If the above conditions are not met, C_{STRG} fast discharge is terminated.

Once all the conditions are met, a 160mA current source is activated and the RT FET turns on to quickly discharge V_{STRG}. Figure 6 shows the C_{STRG} fast discharge logic.

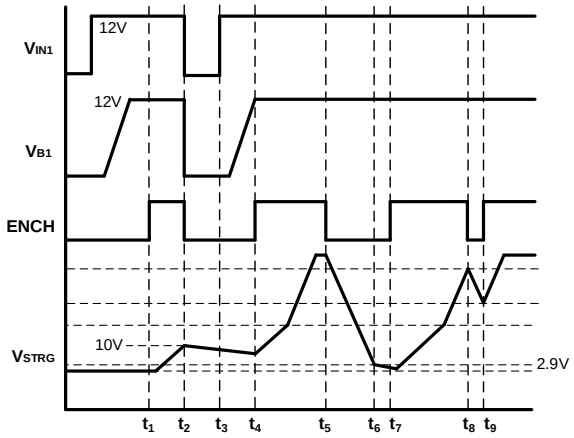


Figure 6: C_{STRG} Fast Discharge Logic

The C_{STRG} fast discharge logic occurs in the following sequence:

- At t_1, the PLP is enabled, and the IC enters pre-charge after a charge delay if the ENCH bit is set to 1.
- At t_2, V_{IN1} is lost during the pre-charge stage, where V_{STRG} is 10V. There is no PLP buck release, and V_{STRG} is not discharged at this point.
- Between t_2 and t_3, there is no voltage on VIN1 or VB1, so V_{CC} is not present. The MP5520's I^2C interface resets, and the ENCH bit is set to 0.
- At t_3, V_{IN1} returns and e-fuse 1 turns on, resulting in V_{B1} rising up to 12V. There is no PLP charge because the ENCH bit is set to 0.
- At t_4, if the host sends an ENCH = 1 command, the PLP is enabled. The MP5520 begins to charge V_{STRG} to the target value once FBR exceeds the FBR charging threshold, and DET exceeds the PFI low threshold.
- Between t_4 and t_5, the host sends the following commands: STRG_DISCHRG_EN and ENCH_DISCHRG = 1, and DISCHRG_PATH_ISO = 0.
- At t_5, if the host sends an ENCH = 0 command, C_{STRG} fast discharge begins.
- Between t_5 and t_6, C_{STRG} fast discharge will exit if any of the required conditions are not met.
- At t_6, C_{STRG} fast discharge stops once V_{STRG} drops below 2.9V.
- At t_7, the PLP is enabled again after the ENCH bit is set to 1.
- At t_8, the host sends an ENCH = 0 command when V_{STRG} is still being charged and is below the target value. C_{STRG} fast discharge begins at this point as well.
- At t_9, if the host sends an ENCH = 1 command when V_{STRG} exceeds 2.9V, PLP boost charge is enabled to charge C_{STRG} immediately.

STRG Capacitor Resistor Discharge

The tantalum capacitor leakage test will be implemented only once in the SSD life cycle, and is not used otherwise during normal operation. If no password is typed, the MP5520 ensures that RT FET is on when the ENCH bit is set to 0 during normal operation.

The MP5520 can only initiate resistor discharge on C_{STRG} when the following conditions are met:

1. The STRG_DISCHRG_EN bit is set to 0 in the RLS_CTRL2 register.
2. The DISCHRG_PATH_ISO bit is set to 1 in the CHRG_CTRL2 register.
3. The ENCH_DISCHRG bit is set to 1 in the SYS_CTRL2 register.

4. The ENCH bit is set to 0 in the CHRG_CTRL1 register.

Figure 7 shows the C_{STRG} resistor discharge path.

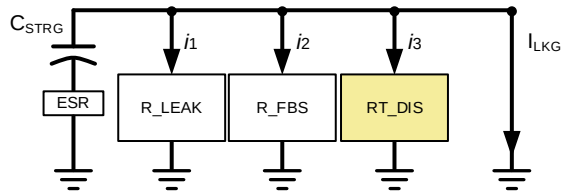


Figure 7: C_{STRG} Resistor Discharge Path

Once the required conditions are met, C_{STRG} resistor discharge is activated for the tantalum leakage test. After the tantalum leakage test is complete, the DISCHRG_PATH_ISO bit in the CHRG_CTRL2 register and the IC power must be reset before setting the ENCH bit to 1. Figure 8 shows the C_{STRG} resistor discharge logic.

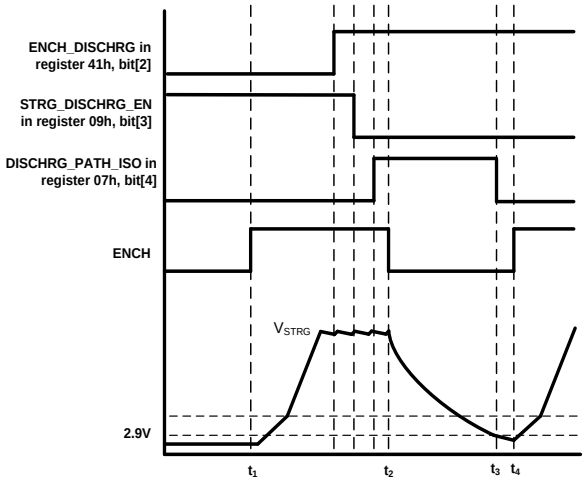


Figure 8: C_{STRG} Resistor Discharge Logic

Enable (EN) Control for Downstream DC/DC Converter (ENDCDC)

The ENDCDC pin is configured to enable the downstream DC/DC converter. If the EN2 pin is set to SAS mode (V_{IN1} = 12V and V_{IN2} = 5V), then ENDCDC goes high after SS for the e-fuses completes. If the EN2 pin is set to PCIe mode (V_{IN1} = 12V only), then ENDCDC goes high after e-fuse 1's SS completes. ENDCDC goes low after PLP buck release finishes.

Figure 9 shows the waveforms of the ENDCDC logic.

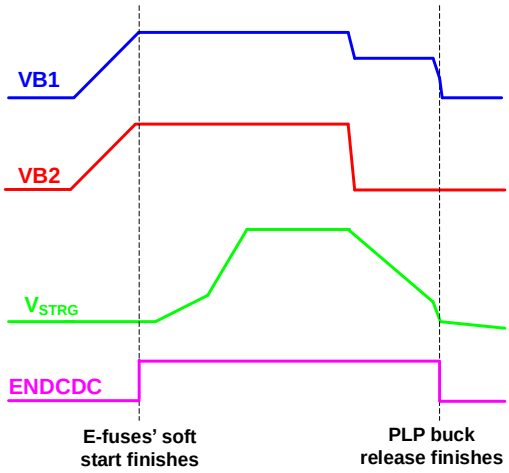


Figure 9: ENDCDC Logic

Power Disable (P1P2 and P3)

The P1P2 and P3 pins are used for power disable as well as the e-fuses' on/off control. There is an internal 500kΩ pull-down resistor. P1P2 and P3 have a 1ms deglitch time. Table 2 shows the P1P2 and P3 logic.

Table 2: P1P2 and P3 Logic

P1P2	P3	Power Mode
L	L	E-fuses on
L	H	E-fuses off
H	L	E-fuses on
H	H	E-fuses on

I²C Address

The ADDR pin sets the MP5520's I²C slave address. Three logic states can be selected by connecting ADDR to VCC (logic high), to ground (logic low), or floating ADDR. Table 3 shows the address setting.

Table 3: I²C Address Setting

ADDR Status	Logic Low	Logic High	Floating
I²C address	33h	35h	37h

VCC

The MP5520's internal circuits are powered by the VCC regulation voltage (V_{CC}), which is supplied from an internal low-dropout (LDO) generated by V_{IN1}, V_{IN2}, V_{B1}, V_{B2}, or V_{STRG}, depending on the operating conditions. V_{CC} is 5V when V_{IN1}, V_{IN2}, V_{B1}, or V_{B2} exceeds 5V.

If V_{IN1}, V_{IN2}, V_{B1}, and V_{B2} are all below 5V, and the PLP is not releasing, V_{CC} is almost equal to the maximum voltage of V_{IN1}, V_{B1}, V_{IN2}, and V_{B2}. If the PLP is releasing and V_{STRG} exceeds 4.6V, then V_{CC} is 4.6V and is supplied by V_{STRG}.

Place a minimum 1µF decoupling capacitor on VCC to support a sufficient level of energy.

Input Power Failure Detection (DET1 and DET2) and Indication (PFI)

The DET1 and DET2 pins are connected to V_{IN1} (or V_{B1}) and V_{IN2} (or V_{B2}), respectively, to detect an input power failure. DETx is triggered to indicate power loss if the DETx voltage (V_{DETx}) drops below the 0.8V reference voltage (V_{DET_REF}). DETx is released if V_{DETx} exceeds 102% of V_{DET_REF}. Correspondingly, the PFI goes low if DETx is released, and the PFI goes high if DETx is triggered.

The PFI pin also indicates PLP buck release. If the MP5520 is in buck release mode, PFI remains high, regardless of whether DETx exceeds the PFI low threshold.

The power loss thresholds for V_{IN1} (or V_{B1}) and V_{IN2} (or V_{B2}) are configured via the resistor divider connected to DET1 and DET2, respectively. The e-fuses turn off once the corresponding DETx is triggered. The failure criteria is selected by the EN2 pin's logic level.

See the Application Information section on page 58 for more details on selecting the resistor divider.

Interrupt Indicators (INT1 and INT2)

The INT1 and INT2 pins indicate issues defined in register 37h (STATUS1) and register 38h (STATUS2). If no issues are found, INT1 and INT2 remain high. If any issues are found, INT1 or INT2 are pulled low, depending on the I^2C settings.

INT1 indicates the status bits in the STATUS1 register. Once any bit in the STATUS1 register is triggered and set to 1 (meaning an issue has been found), and if the corresponding mask bit in register 39h is set to 0 (not masked), then INT1 is pulled low. If the corresponding mask bit is set to 1 (masked), INT1 is not pulled low to indicate that the status bit is triggered.

INT2 indicates the status bits in the STATUS2 register. Once any bit in the STATUS2 register is triggered and set to 1 (meaning an issue has been found), and if the corresponding mask bit in register 3Ah is set to 0 (not masked), then INT2 is pulled low. If the corresponding mask bit is set to 1 (masked), then INT2 is not pulled low to indicate that the status bit is triggered.

The STATUS1 and STATUS2 registers provide a self-reset function after reading. For example, after the STATUS1 register is read by the I^2C master, all the bits in STATUS1 are cleared to 0, and INT1 is pulled high again. After the STATUS2 register is read by the I^2C master, all the bits in STATUS2 are cleared to 0, and INT2 is pulled high again. Figure 10 shows how INT1 and INT2 self-reset after reading.

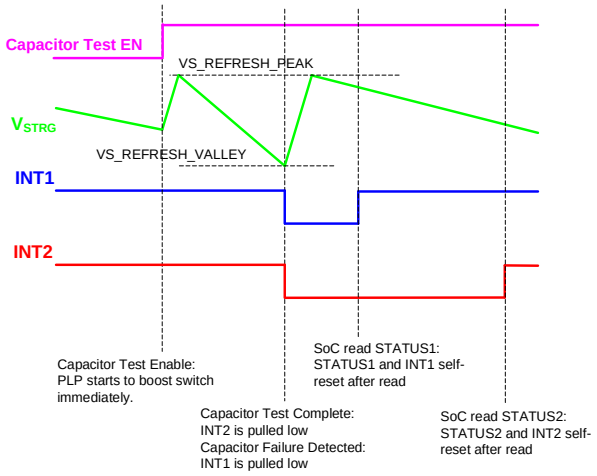


Figure 10: INT1 and INT2 Self-Reset Logic after Read

Boost Charge Regulation (FBS)

When PLP operates in boost charge mode, the resistor divider connected to the FBS pin configures V_{STRG}. The resistor divider sets the peak and valley values of V_{STRG} during boost refresh. If the FBS voltage (V_{FBS}) is equal to the reference voltage (V_{REF}) multiplied by the V_{STRG} refresh threshold, then the PLP stops switching, and V_{STRG} and V_{FBS} discharge slowly. If V_{FBS} drops to V_{REF}, the PLP switches to boost charge

C_{STRG}. The V_{STRG} refresh threshold is configured to 101%.

See the Application Information section on page 58 for more details on selecting the resistor divider.

Storage Voltage Power Good (PG) Indicator (PGS)

The PGS pin indicates the V_{STRG} power good (PG) threshold. PGS is pulled high if ENCH is logic high, V_{FBS} exceeds the PGS rising threshold, a V_{STRG} over-voltage (OV) condition (where V_{FBS} exceeds 115% of V_{REF}) is not triggered, and the blocking FET keeps turning on.

If V_{FBS} drops below the PGS falling threshold or the blocking FET turns off, then PGS is pulled low. The PGS thresholds are set via the PGS_TH bits in the CHRG_CTRL2 register.

If a V_{STRG} OV condition is triggered (where V_{FBS} exceeds 115% of V_{REF}), or ENCH is set to 0 (PLP stops switching), then PGS also goes low.

Buck Release Regulation (FBR)

The FBR pin determines the operation of the PLP converter. If FBR exceeds the FBR charging threshold and DETx exceeds the PFI low threshold, then the converter enters boost charge mode. When DETx drops below the PFI high threshold and FBR drops below the FBR release threshold, then the converter enters buck release mode. In buck release mode, the resistor divider connected to FBR configures the regulation voltage.

See the Application Information section on page 58 for more details on selecting the resistor divider.

VIN Deglitch and Recovery Control (QPOR)

The multiple-time programmable (MTP)-trimmed bit (QPOR) in the RLS_CTRL1 register controls the MP5520's behavior when VIN recovers. If QPOR is set to 0, the e-fuse turns on again once VIN recovers, and the MP5520 enters boost charge mode once FBR exceeds the FBR charging threshold and DETx exceeds the PFI low threshold.

If QPOR is set to 1, the e-fuse does not turn on until PLP buck release finishes. PLP buck release finishes once V_{STRG} drops below the threshold set in register 3Dh.

If QPOR is set to 1, the MP5520 resets all the registers after PLP buck release finishes (see Figure 11).

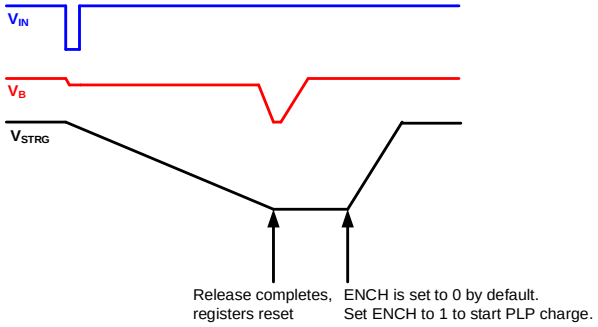


Figure 11: Reset Registers after PLP Release Completes

Bidirectional Power-Sharing Converter Regulation (FB1)

When the MP5520's bidirectional power-sharing converter operates in standalone buck mode and starts up, the resistor divider connected to the FB1 pin configures buck output voltage (V_{BUCK}) regulation. See the Application Information section on page 58 for more details on selecting the resistor divider.

If GO_BIT is set to 0 using register 10h, bit[7], the FB1 reference cannot be changed via the I^2C. If GO_BIT is set to 1, the FB1 reference can be changed by configuring the BUCK_VOUT_REF bits (via register 10h, bits[6:0]).

If FB1 is connected to VCC, the bidirectional power-sharing converter can switch and operate in power-sharing mode but not standalone mode.

System Start-Up

When the input power is on, VCC and the I^2C interface are enabled. The e-fuse MOSFETs from V_{INx} to V_{Bx} turns on when the following conditions are met:

1. V_{INx} exceeds its UVLO threshold.
2. The EN pin voltage (V_{EN}) is logic high, and the EN bit is set 1.
3. The difference between V_{INx} and V_{Bx} exceeds the threshold (100mV by default).

Afterwards, the V_{Bx} capacitors are charged up from 0V to V_{INx}, and the slew rate is controlled by C_{DVDTx}.

Set ENCH to 1 to enable C_{STRG} charging. The boost charging circuit begins to work after FBR exceeds the FBR charging threshold, DETx exceeds the PFI low threshold, and both e-fuses' SS are complete.

There is an I²C-configurable charge delay time after DVDTx completes. This ensures that the e-fuse is fully turned on before starting to charge C_{STRG}. The charge delay is set via the CHRG_DLY bits in the CHRG_CTRL2 register.

The charging circuit begins to charge V_{STRG} with a pre-charge current. Once V_{STRG} rises close to V_{Bx}, the charging circuit starts to switch and operate in boost charge mode, then charges V_{STRG} up to the target voltage. The boost converter's average input current is controlled during boost charge mode.

Figure 12 shows the typical waveforms of start-up sequence.

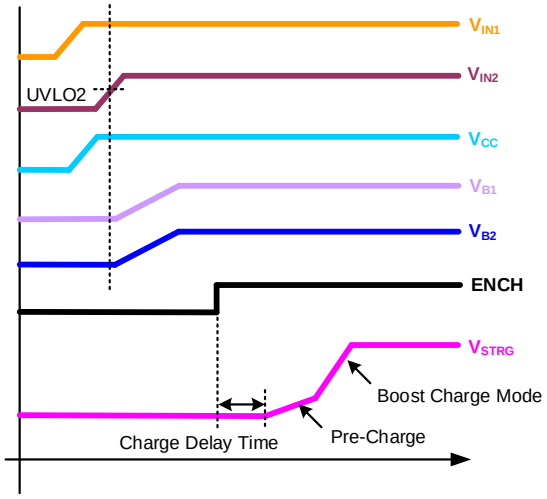


Figure 12: System Start-Up Sequence

Boost Charge Mode

After start-up, the PLP converter operates as a boost converter and charges up V_{STRG} to the set value. After V_{STRG} reaches the regulation value set by the FBS resistors, the MP5520 operates in burst mode to minimize the converter's power loss. This is also known as boost refresh. During boost refresh, when V_{STRG} is charged up and V_{FBS} reaches the boost refresh threshold, the boost converter stops switching and the V_{STRG} slowly releases. When V_{STRG} drops below the regulation value, boost charge burst mode initiates and charges C_{STRG}. Figure 13 shows the waveforms during boost refresh.

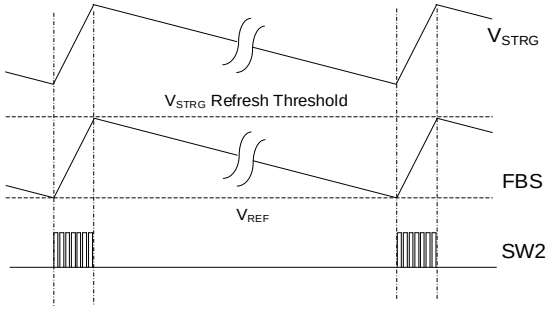


Figure 13: Boost Refresh

In boost charge mode, the boost converter's average input current is controlled. The average current can be configured via the I²C.

Buck Release Mode

If a power failure occurs, the MP5520 enters buck release mode to support the system power with the storage energy.

Power failure is determined by DET configurations. Once the MP5520 detects a power failure, the corresponding e-fuse turns off, and the PLP converter changes from boost charge mode to buck release mode to support the load with V_{STRG}.

Constant-on-time (COT) control is used in buck release mode. The switching frequency (f_{SW}) can be configured via the FSW_RLS bits in the RLS_CTRL1 register.

When the input power recovers, the MP5520's exit from buck release mode depends on the QPOR bit in the RLS_CTRL1 register. If QPOR is set to 0, buck release stops and the e-fuse turns on once VIN recovers. If QPOR is set to 1, buck release continues and the e-fuse cannot turn back on until either V_{STRG} is discharged below RLS_UVLO, or the IC resets.

If buck release completes and VIN is not recovered yet, then the e-fuse remains off, and VBx is discharged using an internal discharge circuit. This discharge circuit is activated as long as V_{CC} exceeds its UVLO threshold (V_{CC_UVLO}).

Bidirectional Power-Sharing Converter Operation

The bidirectional power-sharing converter can be configured to work in standalone mode or power-sharing mode. COT control is used, and f_{SW} is configurable via the FSW_BUCK bits in BUCK_CTRL1.

In buck standalone mode, V_{BUCK} is regulated by FB1. The converter starts to switch when V_{B1} is established by e-fuse 1.

In buck power-sharing mode, the power-sharing converter shares the load current with e-fuse 2 and regulates e-fuse 2's current. E-fuse 2's current is clamped once it reaches the current threshold (configurable via the I^2C). The power-sharing converter then begins to provide the additional current to the load.

Figure 14 shows the detailed behavior in buck power-sharing mode.

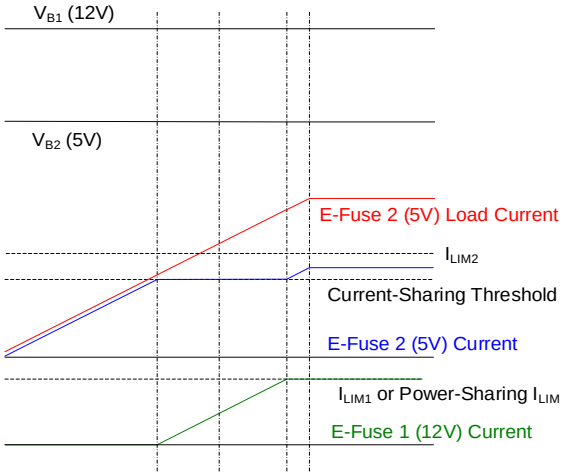


Figure 14: Buck Power-Sharing Mode

In boost power-sharing mode, the power-sharing converter shares the load current with e-fuse 1 and regulates e-fuse 1's current. E-fuse 1's current is clamped once it reaches the current threshold (configurable via the I^2C, with 31% x I_{LIM1} or 62% x I_{LIM1}). The power-sharing converter then starts to provide additional current to the load.

Figure 15 shows the detailed behavior in boost power-sharing mode.

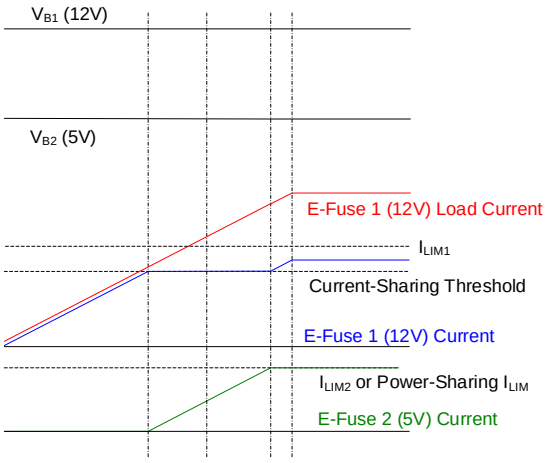


Figure 15: Boost Power-Sharing Mode

Forced Capacitor Health Test

The internal discharge FET's drain is connected to the RT pin. After the discharge FET turns on, V_{STRG} is discharged via the external resistor and discharge FET until V_{FBS} drops to V_{REF}. Since the discharge current is determined by the external resistor, the proper resistor size must be selected to sufficiently handle the power dissipation.

Once discharge begins, the discharge timer starts to count using the least significant bit (LSB) step configured via the LSB_DISCHRG_TIMER bit. If V_{STRG} drops to the regulated voltage, the discharge time counter stops and V_{STRG} is measured and stored in the VSTRG2 register. The discharge timer's counting number is stored in the CAP_TIMER register. Figure 16 shows the capacitor test procedure.

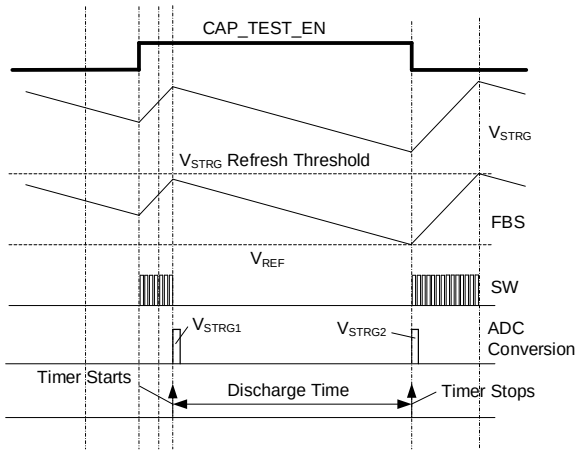


Figure 16: Capacitor Test Procedure

To check the forced capacitor test results, if the CAP_TIMER value is below CAP_FAIL_TH, then the MP5520 considers C_{STRG} to be insufficient and sets the CAP_ ERR bit in the STATUS1 register to 1. The error bit is not reset until it is written to 1, or the STATUS1 register is read by the I²C master.

The voltages at the forced capacitor test's start and end points (V_{STRG1} and V_{STRG2}, respectively) are stored in their corresponding registers and are converted from the ADC to real voltages.

V_{STRG1} can be calculated with Equation (3):

$$V_{STRG1} = \left(1 + \frac{R_{FBS1}}{R_{FBS2}}\right) \times \frac{V_{STRG1\_ADC} \times 0.09375 + 795.3125}{1000} \quad (3)$$

Where R_{FBS1} is the high-side resistor connected to FBS, and R_{FBS2} is the low-side resistor connected to FBS.

V_{STRG2} can be calculated with Equation (4):

$$V_{STRG2} = \left(1 + \frac{R_{FBS1}}{R_{FBS2}}\right) \times \frac{V_{STRG2\_ADC} \times 0.09375 + 795.3125}{1000} \quad (4)$$

C_{STRG} from the forced capacitor test can be calculated with Equation (5):

$$C_{STRG} = \left\{ \frac{V_{STRG1} + V_{STRG2}}{2 \times \left[R_{DIS} // (R_{FBS1} + R_{FBS2})\right]} + I_{LKG\_CSTRG} \right\} \times \frac{t_{DISCHG}}{V_{STRG1} - V_{STRG2}} \quad (5)$$

Where R_{DIS} is the discharge resistor connected between the STRG and RT pins in parallel with the FBS voltage divider, and I_{LKG_CSTRG} is the STRG pin leakage current.

The discharge time (t_{DISCH}) can be calculated with Equation (6):

$$t_{DISCH} = CAP\_TIMER\_FORCED \times LSB\_DISCHRG\_TIMER \quad (6)$$

The FBS voltage divider can be disregarded when the RT resistance is significantly smaller than the FBS voltage divider value.

Register 54h and register 55h can also be used to store V_{STRG1} and V_{STRG2} sensing during the first forced capacitor health test. V_{STRG1} and V_{STRG2} can continue to be used as references to calculate C_{STRG}.

The initial V_{STRG} in register 33h is automatically loaded to register 54h after the first forced capacitor health test or once the rising edge of VS_LOADING_EN in register 07h, bit[5] is detected.

The final V_{STRG} in register 34h is automatically loaded to register 55h after the first forced capacitor health test or once the rising edge of VS_LOADING_EN in register 07h, bit[5] is detected.

CAPTEST_DONE in the STATUS2 register indicates the end of the capacitor health test. The status is reported to the system via INT2, which can be enabled by the corresponding mask registers. VS_LOADING_EN's rising edge must occur after CAPTEST_DONE to obtain the correct value from register 33h and register 34h.

C_{STRG} can be calculated with the voltages in register 54h and register 55h, as well as the timer in register 35h. The data in register 54h and register 55h can be reloaded until the next rising edge of VS_LOADING_EN in register 07h, bit[5]. This sensing method improves the noise immunity of capacitor health test ADC. Figure 17 shows the V_{STRG} sensing logic.

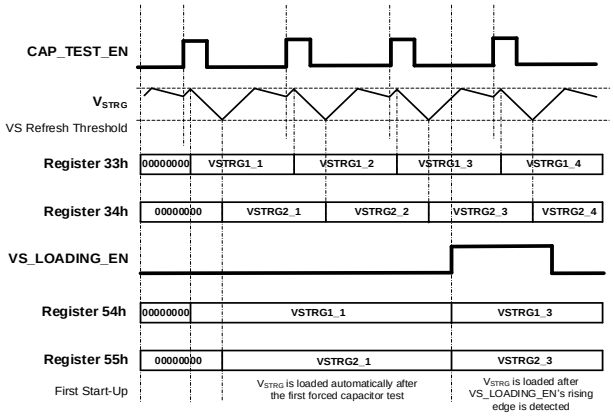


Figure 17: V_{STRG} Sensing Logic

Deep Capacitor Health Test

A deep capacitor health test provides another method to monitor the C_{STRG} health with fixed delta discharged V_{STRG} (8V or 12V). The delta V_{STRG} during deep capacitor test mode must be selected using the DV_DEEP bit in the CAP_TEST_CTRL register. The deep capacitor health test is selected by setting the CAP_TEST_MODE bit and DEEP_EN bit to 1 in the CAP_TEST_CTRL register. This test can only cover V_{STRG} between 14V and 30V.

Similar to the forced capacitor health test, the deep capacitor health test behaves as a one-time test and both of them control the discharge current via an external resistor between the RT and STRG pins.

When deep discharge starts, the discharge timer starts to count with the LSB step set by the LSB_DISCHRG_TIMER bit, and V_{STRG} is sensed and saved into the DEEP_CAP_TEST_START_ADC register. Once V_{STRG} drops to the regulated voltage, the discharge time counter stops. The discharge timer's counting number is stored in the CAP_TIMER_DEEP register.

The voltage at the capacitor test's starting point (V_{STRG1_DEEP}) is stored in the DEEP_CAP_TEST_START_ADC register. The conversion from ADC to the real voltages can be calculated with Equation (7):

$$V_{STRG1\_DEEP} = V_{STRG1\_DEEP\_ADC} \times 0.075 + 12.5 \quad (7)$$

Where $V_{STRG1\_DEEP\_ADC}$ is the ADC value recorded in the DEEP_CAP_TEST_START_ADC register. C_{STRG} from the deep capacitor test can be calculated with Equation (8):

$$C_{STRG} = \frac{t_{DISCH}}{\left[R_{DIS} // (R_{FBS1} + R_{FBS2})\right] \times \ln\left(\frac{V_{STRG1\_DEEP} + \left[R_{DIS} // (R_{FBS1} + R_{FBS2})\right] \times I_{LKG\_CSTRG}}{(V_{STRG1\_DEEP} - V_{DELTA\_DEEP}) + \left[R_{DIS} // (R_{FBS1} + R_{FBS2})\right] \times I_{LKG\_CSTRG}}\right)} \quad (8)$$

t_{DISCH} can be calculated with Equation (9):

$$t_{DISCH} = CAP\_TIMER\_DEEP \times LSB\_DISCHRG\_TIMER \quad (9)$$

Output Over-Voltage (OV) Clamping

The clamping values of e-fuse 1 and e-fuse 2's output voltages (V_{CLAMP1} and V_{CLAMP2}) are typically 13.7V and 6V, respectively.

The clamping trigger thresholds slightly exceeds the clamping voltages (14.3V and 6.3V, respectively). Once V_{Bx} exceeds the trigger threshold, the clamping circuit starts to work and pulls V_{Bx} to the clamping voltage. It generally takes a few microseconds to start clamping. The clamping circuit releases when V_{INx} drops below the V_{Bx} clamping voltage. Figure 18 shows the voltage clamping procedure.

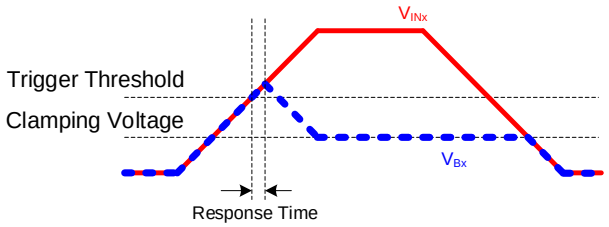


Figure 18: Output Clamping Response

Reverse-Current Blocking

Both e-fuses feature reverse-current blocking. If the reverse current flowing from V_{Bx} to V_{INx} is triggered, the corresponding switch turns off to prevent reverse current flow. The e-fuses' reverse blocking function can be disabled via the RVS_BLK_EN1 and RVS_BLK_EN2 bits in the E-FUSE_CTRL4 and E-FUSE_CTRL5 registers, respectively.

Storage Over-Voltage Protection (OVP)

If V_{FBS} exceeds 115% of V_{REF}, the bidirectional converter's HS-FET and low-side MOSFET (LS-FET) are forced to turn off, and the boost charge process is terminated. This process avoids further charging the storage components, and protects the components and device from potential OV conditions. If V_{STRG} over-voltage protection (OVP) occurs, then PGS goes low.

V_{STRG} OVP can be enabled or disabled via the OVP_VS_EN bit in the CHRG_CTRL2 register.

Over-Current Protection (OCP) of Buck Release Mode and the Power-Sharing Converter

When COT control is used with the buck converter, the HS-FET's on time is fixed. As long as the current is limited the instant when the HS-FET turns on, there is no current runaway. The MP5520 implements the valley current limit for the LS-FET during both PLP buck release mode and buck power-sharing mode.

The LS-FET current is sensed during its on time. The HS-FET cannot turn on in one cycle unless the LS-FET current is below the valley current limit. This mechanism is useful when the load current increases due to a load change or shorted output. It avoids current runaway and protects the system from over-current (OC) stress.

Figure 19 shows valley current limit protection. The load current increases at t_1. To support the additional current, the inductor current (I_L) ramps up after a fixed on time, with a shorter HS-FET off time. The HS-FET cannot turn on again until the low-side (LS) current reaches the valley current threshold.

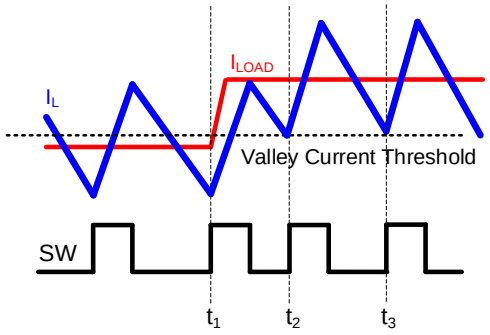


Figure 19: Valley Current Limit Protection

8-Bit Analog-to-Digital Converter (ADC)

The MP5520 integrates an 8-bit ADC to monitor and report V_{INx}, I_{INx}, and P_{INx} of the e-fuses. V_{INx} and I_{INx} are sensed and sent to the ADC with a 60k/s sampling rate. The maximum, minimum, and average (across 1s) I_{INx} and V_{INx} are stored in the corresponding registers. Once the ADC is enabled, all of the registers are automatically refreshed. Table 4 shows the LSB of the 8-bit ADC.

Table 4: 8-Bit ADC LSB

Parameter (where x = 1 or 2)	LSB	Unit
V_{IN1_LSB}	75	mV
V_{IN2_LSB}	25	mV
I_{INx_LSB}	0.0075 x I_{LIMx}	A
P_{INx_LSB}	256 x V_{INx_LSB} (V) x I_{INx_LSB} (A)	W

I_{LIM1} and I_{LIM2} change with the I^2C ILIM settings via the ILIM1 bit in register 3Bh and the ILIM2 bit in register 3Ch, respectively.

E-fuse 1's input power (P_{IN1}) can be calculated with Equation (10):

$$P_{IN1} = P_{IN1\_ADC} \times P_{IN1\_LSB} = V_{IN1\_ADC} \times V_{IN1\_LSB} \times I_{IN1\_ADC} \times I_{IN1\_LSB} \times 256 \quad (10)$$

E-fuse 2's input power (P_{IN2}) can be calculated with Equation (11):

$$P_{IN2} = P_{IN2\_ADC} \times P_{IN2\_LSB} = V_{IN2\_ADC} \times V_{IN2\_LSB} \times I_{IN2\_ADC} \times I_{IN2\_LSB} \times 256 \quad (11)$$

Monitor Ratio Registers

To provide more flexibility for adjusting the current LSB, the MP5520 provides the IIN_5V_MON_R register for the 5V e-fuse current monitor ratio and the IIN_12V_MON_R register for the 12V e-fuse current monitor ratio.

The default value of the IIN_5V_MON_R and IIN_12V_MON_R registers is 40h. The LSB is linearly proportional to the reciprocal values set in IIN_5V_MON_R and IIN_12V_MON_R. For example, if the IIN_5V_MON_R register is set to 80h, the 5V e-fuse current's ADC LSB is set to be half of the default value; if the IIN_5V_MON_R register is set to 20h, the 5V e-fuse current's ADC LSB is set to be twice of the default value.

The monitor ratio only changes the current and power of the ADC LSBs. It does not change the input current limit.

Thermal Protection

The MP5520 monitors the die temperature. If the die temperature exceeds the thermal warning threshold (typically 120°C), the thermal warning register is triggered to issue a warning to the system. If the e-fuse or die temperature increases up to 150°C, the MP5520 triggers over-temperature protection (OTP), then both e-fuses turn off to avoid operating at high temperatures and potentially damaging components.

I²C INTERFACE

I²C Serial Interface

The I²C is a two-wire, bidirectional, serial interface that consists of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage (V_{BUS}) when they are idle. A master device connected to the line generates the SCL signal and device address, then arranges the communication sequence. The MP5520 interface is an I²C slave that supports fast mode (400kHz) and high-speed mode (3.4MHz). The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate, and other parameters can be controlled via the I²C interface. When the master sends the address as an 8-bit value, the 7-bit address should be followed by a direction bit to indicate a read/write (R/W) operation, where 0 means write and 1 means read.

Start and Stop Commands

The start (S) and stop (P) commands are signaled by the master device, indicating the beginning and end of the I²C transfer. In the start condition, the SDA signal transitions from high to low while the SCL remains high. In the stop condition, the SDA signal transitions from low to high while the SCL remains high (see Figure 20).

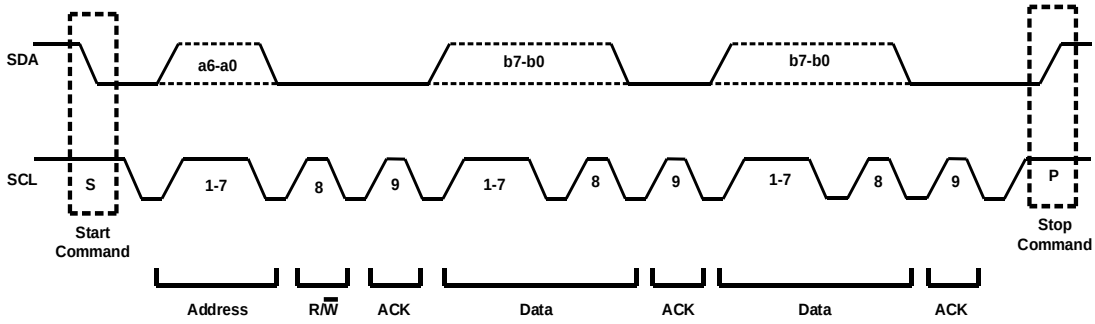


Figure 20: Start and Stop Conditions

The master then generates the SCL clocks and transmits the device address and the R/W direction bit on the SDA line.

Transfer Data

Data is transferred in 8-bit bytes by the SDA line. Each data byte must be followed by an acknowledge (ACK) bit.

I²C Update Sequence

The MP5520 requires a start command, valid I²C address, register address byte, and data byte for a single data update. The device acknowledges receiving each byte by pulling the SDA line low during a single clock pulse's high period. A valid I²C address selects the MP5520, then the device performs an update on the LSB byte's falling edge. Figure 21 shows an example of writing to a single register. Figure 22 on page 33 shows an example of writing to multiple registers, and Figure 23 shows an example of reading a single register.

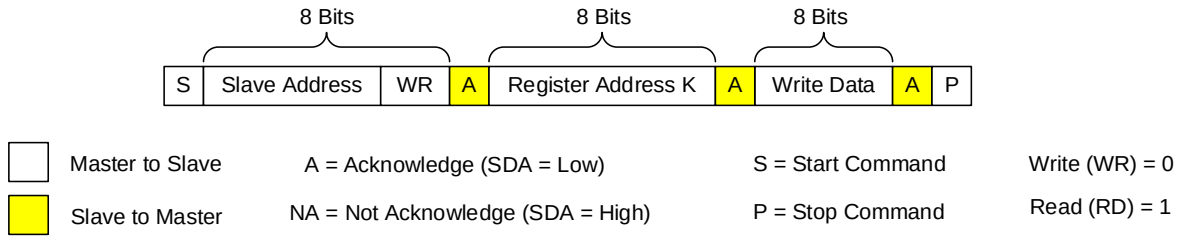


Figure 21: I²C Write Single Register Example

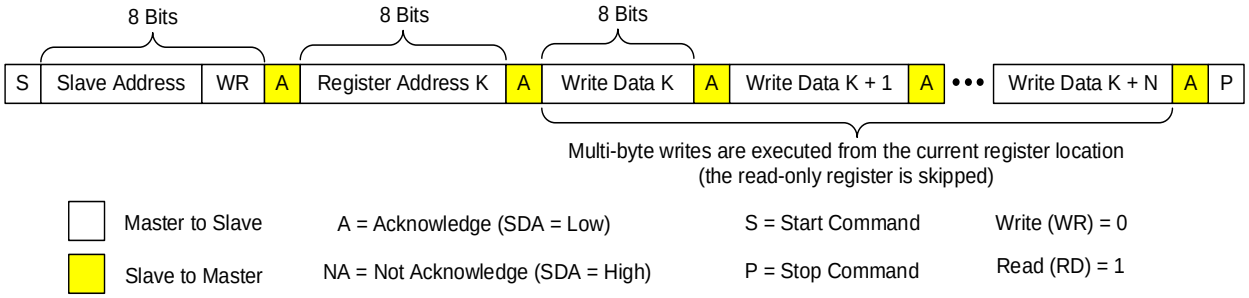


Figure 22: I²C Write Multiple Registers Example

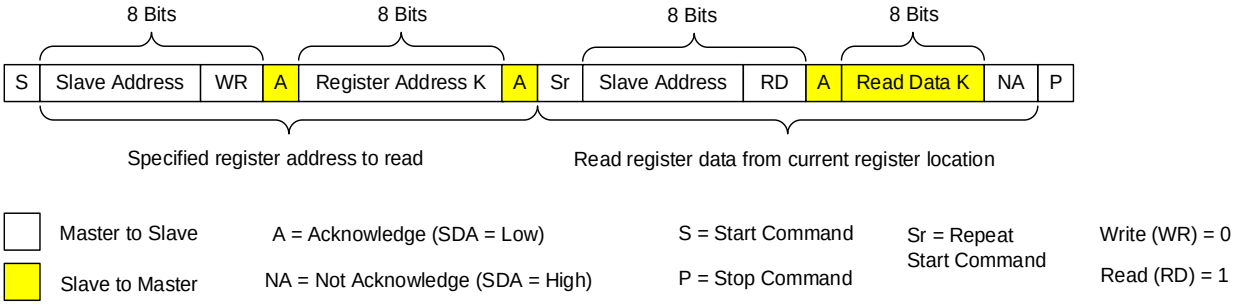


Figure 23: I²C Read Single Register Example

REGISTER DESCRIPTION (9)

FUNCTIONAL MTP1 USER TRIM BITS

No.	Name	D7	D6	D5	D4	D3	D2	D1	D0
1	E-FUSE_CTRL3	UVLO1_RISING		UVLO1_FALLING		N/A			
2	E-FUSE_CTRL2	UVLO2_RISING		UVLO2_FALLING		N/A			
3	E-FUSE_CTRL1	N/A	E-FUSE_ON_CTRL	BOOST_SHARING	N/A	VIN_RECOVER_TH		VIN_RECOVER_DLY	
4	E-FUSE_CTRL4	RVS_BLK_EN1	EN1	OVP1		RVS_BLK_EN2	EN2	OVP2	
5	CHRG_CTRL1	N/A	N/A	VS_LOADING_EN	DISCHRG_PATH_ISO	N/A	PGS_TH		OVP_VS_EN
6	RLS_CTRL1	N/A	ILIM_RLS		N/A	FSW_RLS		DET_MODE	
7	RLS_CTRL2	MAX_RLS_TIMER_BCKP				N/A			
8	CAP_TIMER_CTRL	VOUT_TRANS_SLEW_RATE		PWR_SHARE_LIM	N/A				
9	BUCK_CTRL1	BUCK_MODE_R	ADC_EN	SW_SLEW_RATE		ILIM_PS		FSW_PS	
10	BUCK_CTRL2	GO_BIT	BUCK_VOUT_REF						
11	CAP_TEST_CTRL	RAMP_BUCK		CAP_TEST_EN	DV_DEEP	E-FUSE_RST	ENCH_DISCHRG	DEEP_EN	TOGGLE_EN
12	CAP_FAIL_TH_FORCED	CAP_FAIL_TH_FORCED							
13	INT_MASK2	MSK_OTW	MSK_OT	MSK_PFI	MSK_PGS	MSK_CAPTEST_DONE	N/A	MSK_POR	N/A

REGISTER DESCRIPTION *(continued)* (9)

FUNCTIONAL MTP2 USER TRIM BITS

No.	Name	D7	D6	D5	D4	D3	D2	D1	D0
1	E-FUSE_ CTRL4	N/A						ON_DLY1	
2	E-FUSE_ CTRL5	N/A						ON_DLY2	
3	CHRG_ CTRL1	N/A	ENCH	ICHRG			PFI_FALL_DLY		PLP_HS
4	CHRG_ CTRL2	CHRG_DLY		N/A					
5	RLS_ CTRL1	QPOR	N/A						
6	CAP_TIM ER_CTR L	LSB_DISCHRG_TIMER			N/A				
7	SYS_ CTRL	N/A		IPRECHRG		N/A			
8	PS_ CTRL1	PS_ EN	N/A						
9	INT_ MASK1	MSK_ LIM1	MSK_ LIM2	MSK_ OV1	MSK_ OV2	MSK_ UV2	MSK_ UV1	N/A	MSK_ FORCED_ CAP_ERR
10	ILIM1	N/A			ILIM1				
11	ILIM2	N/A			ILIM2				
12	RLS_ UVLO	RLS_UVLO							

Note:

9) See the Register Map section on page 36 for the descriptions and default values.

REGISTER MAP

Add	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	MTP_CODE	RO (10)	MTP_CODE							
01h	E-FUSE_CTRL1	R/W (11)	RV (12)				VIN_RECOVER_TH		VIN_RECOVER_DLY	
02h	E-FUSE_CTRL2	R/W (11)	UVLO2_RISING		UVLO2_FALLING		RV (12)			
03h	E-FUSE_CTRL3	R/W (11)	UVLO1_RISING		UVLO1_FALLING		RV (12)			
04h	E-FUSE_CTRL4	R/W (11)	RVS BLK_EN1	EN1	OVP1		RV (12)		ON_DLY1	
05h	E-FUSE_CTRL5	R/W (11)	RVS BLK_EN2	EN2	OVP2		RV (12)		ON_DLY2	
06h	CHRG_CTRL1	R/W (11)	RV (12)	ENCH	ICHRG			PFI_FALL_DLY		PLP_HS
07h	CHRG_CTRL2	R/W (11)	CHRG_DLY		VS_LOADING_EN	DISCHRG_PATH_ISO	RV (12)	PGS_TH		OVP_VS_EN
08h	RLS_CTRL1	R/W (11)	QPOR	ILIM_RLS		PWR_SHARE_LIM	FSW_RLS		DET_MODE	
09h	RLS_CTRL2	R/W (11)	MAX_RLS_TIMER_BCKP				STRG_DISCHRG_EN	RV (12)		
0Ah	-	RV (12)	RV (12)							
0Bh	CAP_TIMER_CTRL	R/W (11)	LSB_DISCHRG_TIMER			RV (12)				
0Ch	-	RV (12)	RV (12)							
0Dh	-	RV (12)	RV (12)							
0Eh	SYS_CTRL	R/W (11)	RV (12)		I_PRECHRG		RV (12)	ADC_EN	RV (12)	
0Fh	PS_CTRL1	R/W (11)	PS_EN	RV (12)	SW_SLEW_RATE		ILIM_PS		FSW_PS	
10h	PS_CTRL2	R/W (11)	GO_BIT	BUCK_VOUT_REF						
11h	PS_CTRL3	R/W (11)	PS_MODE	VOUT_TRANS_SLEW_RATE		RV (12)				
12h	IIN_5V_MON_R	R/W (11)	IIN_5V_MON_R							
13h	IIN_12V_MON_R	R/W (11)	IIN_12V_MON_R							
14h	VINMIN_5V_1S	RO (10)	VINMIN_5V_1S							
15h	VINAVG_5V_1S	RO (10)	VINAVG_5V_1S							
16h	VINMAX_5V_1S	RO (10)	VINMAX_5V_1S							
17h	VINMIN_5V	RO (10)	VINMIN_5V							
18h	VINMAX_5V	RO (10)	VINMAX_5V							
19h	IINMIN_5V_1S	RO (10)	IINMIN_5V_1S							
1Ah	IINAVG_5V_1S	RO (10)	IINAVG_5V_1S							

REGISTER MAP *(continued)*

Add	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1Bh	IINMAX_5V_1S	RO (10)	IINMAX_5V_1S							
1Ch	IINMIN_5V	RO (10)	IINMIN_5V							
1Dh	IINMAX_5V	RO (10)	IINMAX_5V							
1Eh	PINMIN_5V_1S	RO (10)	PINMIN_5V_1S							
1Fh	PINAVG_5V_1S	RO (10)	PINAVG_5V_1S							
20h	PINMAX_5V_1S	RO (10)	PINMAX_5V_1S							
21h	PINMIN_5V	RO (10)	PINMIN_5V							
22h	PINMAX_5V	RO (10)	PINMAX_5V							
23h	VINMIN_12V_1S	RO (10)	VINMIN_12V_1S							
24h	VINAVG_12V_1S	RO (10)	VINAVG_12V_1S							
25h	VINMAX_12V_1S	RO (10)	VINMAX_12V_1S							
26h	VINMIN_12V	RO (10)	VINMIN_12V							
27h	VINMAX_12V	RO (10)	VINMAX_12V							
28h	IINMIN_12V_1S	RO (10)	IINMIN_12V_1S							
29h	IINAVG_12V_1S	RO (10)	IINAVG_12V_1S							
2Ah	IINMAX_12V_1S	RO (10)	IINMAX_12V_1S							
2Bh	IINMIN_12V	RO (10)	IINMIN_12V							
2Ch	IINMAX_12V	RO (10)	IINMAX_12V							
2Dh	PINMIN_12V_1S	RO (10)	PINMIN_12V_1S							
2Eh	PINAVG_12V_1S	RO (10)	PINAVG_12V_1S							
2Fh	PINMAX_12V_1S	RO (10)	PINMAX_12V_1S							
30h	PINMIN_12V	RO (10)	PINMIN_12V							
31h	PINMAX_12V	RO (10)	PINMAX_12V							
32h	CAP_TEST_CTRL	R/W (11)	RV (12)	CAP_TEST_EN	RV (12)	DV_DEEP	RV (12)		DEEP_EN	TOGGLE_EN
33h	VSTRG1	RO (10)	VSTRG1							
34h	VSTRG2	RO (10)	VSTRG2							
35h	CAP_TIMER	RO (10)	CAP_TIMER_FORCED							
36h	CAP_FAIL_TH	RW (11)	CAP_FAIL_TH_FORCED							
37h	STATUS1	1O (13)	ILIM1	ILIM2	OV1	OV2	UV2	UV1	RV (12)	CAP_ERR
38h	STATUS2	1O (13)	OTW	OT	PFI	PGS	CAPTEST_DONE	RV (12)	POR	RV (12)
39h	INT_MASK1	R/W (11)	MSK_ILIM1	MSK_ILIM2	MSK_OV1	MSK_OV2	MSK_UVLO2	MSK_UVLO1	RV (12)	MSK_CAP_ERR
3Ah	INT_MASK2	R/W (11)	MSK_OTW	MSK_OT	MSK_PFI	MSK_PGS	MSK_CAPTEST_DONE	RV (12)	MSK_POR	RV (12)
3Bh	ILIM1	R/W (11)	RV (12)			ILIM1				

REGISTER MAP *(continued)*

Add	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
3Ch	ILIM2	R/W (11)	RV (12)			ILIM2				
3Dh	RLS_UVLO	R/W (11)	RLS_UVLO							
3Eh	CAP_ TIMER_ DEEP	RO (10)	CAP_TIMER_DEEP							
41h	SYS_CTRL2	R/W (11)	RV (12)	E-FUSE_ ON_CTRL	SHARING_ MODE	RV (12)	E-FUSE_ RST	ENCH_ DISCHRG	RV (12)	
53h	DEEP_ CAP_TEST_ START_AD C	RO (10)	DEEP_CAP_TEST_START_ADC							
54h	VSTRG1_ STORED	RO (10)	VSTRG1_STORED							
55h	VSTRG2_ STORED	RO (10)	VSTRG2_STORED							

Notes:

10) "RO" refers to read only. This bit can be read but writes have no effect.
11) "R/W" refers to read/write. This bit can be read or written by the I^2C master.
12) "RV" refers to reserved. This bit is reserved for future expansion and its value must not be modified.
13) "1O" refers to writing 1 to reset. This bit can only be set (e.g. write 1) but not reset (e.g. write 0). Writing 0 has no effect.

MTP_CODE (00h)

Format: Unsigned binary

The MTP_CODE command configures the unique code of the customer.

Bits	Access	Bit Name	Default	Description
7:4	RO	MTP_CODE	0000	Configures the MTP code.

E-FUSE_CTRL1 (01h)

Format: Unsigned binary

The E-FUSE_CTRL1 command sets the VIN recovery threshold as well as the delay time when VIN recovers.

Bits	Access	Bit Name	Default	Description
3:2	R/W	VIN_RECOVER_TH	01	Sets the threshold to turn on the e-fuse when VIN recovers. Once VIN recovers and the difference between the input voltage (V_{INx}) and VB voltage (V_{Bx}) exceeds the threshold, the e-fuse turns on. 00: $V_{INx} > V_{Bx}$ + 50mV 01: $V_{INx} > V_{Bx}$ + 100mV 10: $V_{INx} > V_{Bx}$ + 200mV 11: $V_{INx} > V_{Bx}$ + 300mV
1:0	R/W	VIN_RECOVER_DLY	00	Sets the delay time to turn on the e-fuse when VIN recovers. Once VIN recovers and the difference between V_{INx} and V_{Bx} exceeds the threshold, the e-fuse turns on after the delay time. 00: 0.85ms 01: 2.7ms 10: 3.7ms 11: 4.7ms

E-FUSE_CTRL2 (02h)

Format: Unsigned binary

The E-FUSE_CTRL2 command sets the VIN2 pin voltage (V_{IN2}) rising and falling under-voltage lockout (UVLO) thresholds.

Bits	Access	Bit Name	Default	Description
7:6	R/W	UVLO2_RISING	10	Sets the V_{IN2} rising UVLO threshold ($V_{IN2\_UVLO\_RISING}$). 00: 2.75V 01: 3.25V 10: 3.75V 11: 4.25V
5:4	R/W	UVLO2_FALLING	00	Sets the V_{IN2} UVLO falling threshold ($V_{IN2\_UVLO\_FALLING}$). If UVLO2_RISING = 00, then UVLO2_FALLING is set to: 00: 2.6V 01: 2.5V 10: 2.4V 11: 2.3V If UVLO2_RISING = 01, then UVLO2_FALLING is set to: 00: 3V 01: 2.85V 10: 2.7V 11: 2.55V If UVLO2_RISING = 10, then UVLO2_FALLING is set to: 00: 3.4V 01: 3.15V 10: 2.95V 11: 2.8V If UVLO2_RISING = 11, then UVLO2_FALLING is set to: 00: 3.75V 01: 3.45V 10: 3.2V 11: 3V

E-FUSE_CTRL3 (03h)

Format: Unsigned binary

The E-FUSE_CTRL3 command sets the VIN1 pin voltage (V_{IN1}) rising and falling UVLO thresholds.

Bits	Access	Bit Name	Default	Description
7:6	R/W	UVLO1_RISING	01	Sets the V_{IN1} rising UVLO threshold ($V_{IN1\_UVLO\_RISING}$). 00: 8.75V 01: 9.25V 10: 9.75V 11: 10.25V
5:4	R/W	UVLO1_FALLING	01	Sets the V_{IN1} falling UVLO threshold ($V_{IN1\_UVLO\_FALLING}$). If UVLO1_RISING = 00, then UVLO1_FALLING is set to: 00: 8.4V 01: 8.15V 10: 7.95V 11: 7.75V If UVLO1_RISING = 01, then UVLO1_FALLING is set to: 00: 8.75V 01: 8.4V 10: 8.15V 11: 7.95V If UVLO1_RISING = 10, then UVLO1_FALLING is set to: 00: 9.2V 01: 8.75V 10: 8.4V 11: 8.15V If UVLO1_RISING = 11, then UVLO1_FALLING is set to: 00: 9.5V 01: 8.95V 10: 8.55V 11: 8.3V

E-FUSE_CTRL4 (04h)

Format: Unsigned binary

The E-FUSE_CTRL4 command controls the functions described below, which are mainly for configuring e-fuse 1.

Bits	Access	Bit Name	Default	Description
7	R/W	RVS_BLK_EN1	1	0: Disables the 12V e-fuse reverse blocking function 1: Enables the 12V e-fuse reverse blocking function
6	R/W	EN1	1	0: Turns off the 12V e-fuse 1: Turns on the 12V e-fuse
5:4	R/W	OVP1	10	Sets the 12V e-fuse's clamped voltage when a V_{IN1} over-voltage (OV) fault occurs. 00: 3.8V clamped voltage 01: 6V clamped voltage 10: 13.7V clamped voltage 11: N/A

1:0	R/W	ON_DLY1	01	Sets the turn-on delay of the 12V e-fuse. 00: N/A 01: 1ms 10: 4ms 11: 8ms

E-FUSE_CTRL5 (05h)

Format: Unsigned binary

The E-FUSE_CTRL5 command controls the functions described below, which are mainly for configuring e-fuse 2.

Bits	Access	Bit Name	Default	Description
7	R/W	RVS_BLK_EN2	1	0: Disables the 5V e-fuse reverse blocking function 1: Enables the 5V e-fuse reverse blocking function
6	R/W	EN2	1	0: Turns off the 5V e-fuse 1: Turns on the 5V e-fuse
5:4	R/W	OVP2	01	Sets the 5V e-fuse's clamped voltage when a V_{IN2} OV fault occurs. 00: 3.8V clamped voltage 01: 6V clamped voltage 10: N/A 11: N/A
1:0	R/W	ON_DLY2	01	Sets the turn-on delay of the 5V e-fuse. 00: N/A 01: 1ms 10: 4ms 11: 8ms

CHRG_CTRL1 (06h)

Format: Unsigned binary

The CHRG_CTRL1 command sets the charge and backup converter's (PLP) charge configuration, including charge enable, average charge current, PFI falling delay time, and the high-side MOSFET (HS-FET) logic in boost charge mode.

Bits	Access	Bit Name	Default	Description
6	R//W	ENCH	1	Enables the PLP converter. 0: Disables charge 1: Enables charge
5:3	R/W	ICHRG	011	Sets the PLP input average current in boost charge mode. 000: 50mA 001: 100mA 010: 200mA 011: 300mA 100: 400mA 101: 500mA 110: 600mA 111: 700mA
2:1	R/W	PFI_FALL_DLY	00	00: 0.2ms 01: 1ms 10: 2ms 11: 8ms

0	R/W	PLP_HS	1	Sets the on/off control of the PLP's boost charge HS-FET channel. 0: Turns off the HS-FET channel 1: Turns on the HS-FET channel

CHRG_CTRL2 (07h)

Format: Unsigned binary

The CHRG_CTRL2 command sets the PLP charge configuration, including the charge delay time, VS_LOADING_EN and DISCHRG_PATH_ISO for natural discharge, PGS rising threshold, and the storage voltage (V_{STRG}) over-voltage protection (OVP) function.

Bits	Access	Bit Name	Default	Description
7:6	R/W	CHRG_DLY	01	Sets the delay time before the PLP begins charging. 00: 0.1ms 01: 1ms 10: 5ms 11: 10ms
5	R/W	VS_LOADING_EN	0	Loads the VSTRG1 and VSTRG2 data from registers 33h and 34h to registers 54h and 55h. 0: Loads V_{STRG} only after the first forced capacitor health test 1: Loads V_{STRG} after the rising edge of this bit is detected
4	R/W	DISCHRG_PATH_ISO	0	Sets the impedance isolation for the tantalum leakage test only. Reset this bit to 0 after the tantalum leakage test. 0: Activates the STRG-to-CT2 discharge path with impedance 1: No STRG-to-CT2 discharge path
2:1	R/W	PGS_TH	11	If the FBS voltage (V_{FBS}) exceeds the PGS_TH rising threshold, then PGS goes high. If V_{FBS} falls below the PGS_TH falling threshold, then PGS goes low. 00: 92% x V_{REF} (rising), 88% x V_{REF} (falling) 01: 94% x V_{REF} (rising), 90% x V_{REF} (falling) 10: 96% x V_{REF} (rising), 92% x V_{REF} (falling) 11: 98% x V_{REF} (rising), 94% x V_{REF} (falling)
0	R/W	OVP_VS_EN	0	0: Disables storage OVP 1: Enables storage OVP

RLS_CTRL1 (08h)

Format: Unsigned binary

The RLS_CTRL1 command sets the PLP buck release configuration, including QPOR, the valley current limit for the low-side MOSFET (LS-FET), power-sharing current threshold, switching frequency (f_{SW}), and trigger mode for PLP buck release.

Bits	Access	Bit Name	Default	Description
7	R/W	QPOR	1	0: The e-fuse turns back on once V_{INx} recovers 1: The e-fuse remains off until V_{STRG} drops to its UVLO threshold Note: When QPOR = 1, if VIN recovers before buck release completes, then the IC automatically resets the registers after buck release completes.

6:5	R/W	ILIM_RLS	11	Sets the valley current limit for the LS-FET during PLP release. 00: 1A 01: 3A 10: 5A 11: 7A
4	R/W	PWR_SHARE_LIM	1	Sets the input current threshold to trigger power sharing. 0: I_{LIM} x 62% 1: I_{LIM} x 31%
3:2	R/W	FSW_RLS	01	Sets f_{SW} for the PLP buck release. 00: 500kHz 01: 1MHz 10: 1.5MHz 11: 2MHz
1:0	R/W	DET_MODE	00	Configures the trigger mode for the PLP release, based on the DETx pins. 00: When either of the DETx pins is triggered, release occurs 01: When both of the DETx pins are triggered, release occurs 10: Only DET1 controls power backup 11: Only DET2 controls power backup

RLS_CTRL2 (09h)

Format: Unsigned binary

The RLS_CTRL2 command sets the PLP buck release configuration, including the PLP release time threshold and internal discharge current source.

Bits	Access	Bit Name	Default	Description
7:4	R/W	MAX_RLS_TIMER_BCKP	1111	Sets the user-configurable timer. When the PLP release time is longer than this time, the POR bit in the STATUS2 register is set to 1. 0000 to 1111: 5ms per LSB, from 0ms to 75ms
3	R/W	STRG_DISCHRG_EN	1	Enables the internal discharge current source. 0: Disables STRG fast discharge 1: Enables STRG fast discharge

CAP_TIMER_CTRL (0Bh)

Format: Unsigned binary

The CAP_TIMER_CTRL command sets the least significant bit (LSB) step for both the forced capacitor health test timer and deep capacitor health test timer.

Bits	Access	Bit Name	Default	Description
7:5	R/W	LSB_DISCHRG_TIMER	001	Sets the LSB step of the capacitor test times (CAP_TIMER and CAP_TIMER_DEEP). 000: 0.5ms 001: 2ms 010: 4ms 011: 8ms 100: 16ms 101: 32ms 110: 64ms 111: 128ms

SYS_CTRL (0Eh)

Format: Unsigned binary

The SYS_CTRL command sets the input constant current of the PLP converter in pre-charge mode. It also controls the analog-to-digital converter (ADC) enable.

Bits	Access	Bit Name	Default	Description
5:4	R/W	IPRECHRG	11	Sets the input constant current of the PLP converter in pre-charge mode. 00: 50mA 01: 100mA 10: 150mA 11: 200mA
2	R/W	ADC_EN	0	0: Disables ADC 1: Enables ADC

PS_CTRL1 (0Fh)

Format: Unsigned binary

The PS_CTRL1 command sets the bidirectional power-sharing converter configuration, including PS_EN, SW_SLEW_RATE, the peak or valley current limit, and f_{SW}.

Bits	Access	Bit Name	Default	Description
7	R/W	PS_EN	1	0: Disables the bidirectional power-sharing converter 1: Enables the bidirectional power-sharing converter
5:4	R/W	SW_SLEW_RATE	00	Configures the bidirectional power-sharing converter's switching slew rate. This bit can be configured after MTP1 configuration and resetting VCC. 00: 1x 01: 2x 10: 3x 11: 4x
3:2	R/W	ILIM_PS	11	Selects the bidirectional power-sharing converter current limit. In buck power-sharing mode, this is the valley current limit: 00: 1A 01: 3A 10: 5A 11: 7A In boost power-sharing mode, this is the peak current limit: 00: 1.5A 01: 3A 10: 4.5A 11: 6A
1:0	R/W	FSW_PS	01	Selects the bidirectional power-sharing converter's f_{SW}. 00: 500kHz 01: 1MHz 10: 1.5MHz 11: 2MHz

PS_CTRL2 (10h)

Format: Unsigned binary

The PS_CTRL2 command configures the bidirectional power-sharing converter when it works in standalone mode as a buck converter.

Bits	Access	Bit Name	Default	Description
7	R/W	GO_BIT	0	Determines whether the bidirectional power-sharing converter's output voltage can be adjusted via the I^2C by configuring BUCK_VOUT_REF. 0: Disables voltage adjustment via the I^2C 1: Enables voltage adjustment via the I^2C
6:0	R/W	BUCK_VOUT_REF	0111011 = 600mV	Sets the bidirectional power-sharing converter's output voltage reference. 0101000 to 1111111: 10mV per LSB, from 400mV to 1.27V

PS_CTRL3 (11h)

Format: Unsigned binary

The PS_CTRL3 command sets the bidirectional power-sharing converter mode as well as the transition slew rate of the FB1 reference when the BUCK_VOUT_REF bits in the BUCK_CTRL2 register are changed.

Bits	Access	Bit Name	Default	Description
7	R/W	PS_MODE	0	Selects the bidirectional power-sharing converter mode. In standalone mode, the bidirectional power-sharing converter regulates its output voltage using the FB1 pin. In power-sharing mode, the bidirectional power-sharing converter regulates its output current to support the additional load current when the power-sharing current threshold is triggered on the corresponding e-fuse. 0: Standalone mode 1: Power-sharing mode
6:5	R/W	VOUT_TRANS_SR	00	Sets the transition slew rate of the FB1 reference when the BUCK_VOUT_REF bits in the BUCK_CTRL2 register are changed. 00: 10mV/µs 01: 5mV/µs 10: 1mV/µs 11: 0.5mV/µs

IIN_5V_MON_R (12h)

Format: Unsigned binary

The IIN_5V_MON_R command adjusts the current LSB for the 5V e-fuse.

Bits	Access	Bit Name	Default	Description
7:0	R/W	IIN_5V_MON_R	01000000 = 40	Sets the 5V e-fuse power monitor ratio. This bit adjusts the input current range that can be monitored using the ADC.

IIN_12V_MON_R (13h)

Format: Unsigned binary

The IIN_12V_MON_R command adjusts the current LSB for the 12V e-fuse.

Bits	Access	Bit Name	Default	Description
7:0	R/W	IIN_12V_MON_R	01000000 = 40	Sets the 12V e-fuse power monitor ratio. This bit adjusts the input current range that can be monitored using the ADC.

VINMIN_5V_1S (14h)

Format: Linear

The VINMIN_5V_1S command records the minimum input voltage of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMIN_5V_1S	00000000	Records the minimum input voltage of the 5V e-fuse in the last 1s.

VINAVG_5V_1S (15h)

Format: Linear

The VINAVG_5V_1S command records the average input voltage of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINAVG_5V_1S	00000000	Records the average input voltage of the 5V e-fuse in the last 1s.

VINMAX_5V_1S (16h)

Format: Linear

The VINMAX_5V_1S command records the maximum input voltage of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMAX_5V_1S	00000000	Records the maximum input voltage of the 5V e-fuse in the last 1s.

VINMIN_5V (17h)

Format: Linear

The VINMIN_5V command records the minimum input voltage of the 5V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMIN_5V	00000000	Records the minimum input voltage of the 5V e-fuse after start-up.

VINMAX_5V (18h)

Format: Linear

The VINMAX_5V command records the maximum input voltage of the 5V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMAX_5V	00000000	Records the maximum input voltage of the 5V e-fuse after start-up.

IINMIN_5V_1S (19h)

Format: Linear

The IINMIN_5V_1S command records the minimum input current of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMIN_5V_1S	00000000	Records the minimum input current of the 5V e-fuse in the last 1s.

IINAVG_5V_1S (1Ah)

Format: Linear

The IINAVG_5V_1S command records the average input current of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINAVG_5V_1S	00000000	Records the average input current of the 5V e-fuse in the last 1s.

IINMAX_5V_1S (1Bh)

Format: Linear

The IINMAX_5V_1S command records the maximum input current of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMAX_5V_1s	00000000	Records the maximum input current of the 5V e-fuse in the last 1s.

IINMIN_5V (1Ch)

Format: Linear

The IINMIN_5V command records the minimum input current of the 5V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMIN_5V	00000000	Records the minimum input current of the 5V e-fuse after start-up.

IINMAX_5V (1Dh)

Format: Linear

The IINMAX_5V command records the maximum input current of the 5V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMAX_5V	00000000	Records the maximum input current of the 5V e-fuse after start-up.

PINMIN_5V_1S (1Eh)

Format: Linear

The PINMIN_5V_1S command records the minimum input power of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMIN_5V_1s	00000000	Records the minimum input power of the 5V e-fuse in the last 1s.

PINAVG_5V_1S (1Fh)

Format: Linear

The PINAVG_5V_1S command records the average input power of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINAVG_5V_1s	00000000	Records the average input power of the 5V e-fuse in the last 1s.

PINMAX_5V_1S (20h)

Format: Linear

The PINMAX_5V_1S command records the maximum input power of the 5V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMAX_5V_1s	00000000	Records the maximum input power of the 5V e-fuse in the last 1s.

PINMIN_5V (21h)

Format: Linear

The PINMIN_5V command records the minimum input power of the 5V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMIN_5V	00000000	Records the minimum input power of the 5V e-fuse after start-up.

PINMAX_5V (22h)

Format: Linear

The PINMAX_5V command records the maximum input power of the 5V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMAX_5V	00000000	Records the maximum input power of the 5V e-fuse after start-up.

VINMIN_12V_1S (23h)

Format: Linear

The VINMIN_12V_1S command records the minimum input voltage of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMIN_12V_1s	00000000	Records the minimum input voltage of the 12V e-fuse in the last 1s.

VINAVG_12V_1S (24h)

Format: Linear

The VINAVG_12V_1S command records the average input voltage of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINAVG_12V_1s	00000000	Records the average input voltage of the 12V e-fuse in the last 1s.

VINMAX_12V_1S (25h)

Format: Linear

The VINMAX_12V_1S command records the maximum input voltage of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMAX_12V_1s	00000000	Records the maximum input voltage of the 12V e-fuse in the last 1s.

VINMIN_12V (26h)

Format: Linear

The VINMIN_12V command records the minimum input voltage of the 12V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMIN_12V	00000000	Records the minimum input voltage of the 12V e-fuse after start-up.

VINMAX_12V (27h)

Format: Linear

The VINMAX_12V command records the maximum input voltage of the 12V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	VINMAX_12V	00000000	Records the maximum input voltage of the 12V e-fuse after start-up.

IINMIN_12V_1S (28h)

Format: Linear

The IINMIN_12V_1S command records the minimum input current of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMIN_12V_1s	00000000	Records the minimum input current of the 12V e-fuse in the last 1s.

IINAVG_12V_1S (29h)

Format: Linear

The IINAVG_12V_1S command records the average input current of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINAVG_12V_1s	00000000	Records the average input current of the 12V e-fuse in the last 1s.

IINMAX_12V_1S (2Ah)

Format: Linear

The IINMAX_12V_1S command records the maximum input current of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMAX_12V_1s	00000000	Records the maximum input current of the 12V e-fuse in the last 1s.

IINMIN_12V (2Bh)

Format: Linear

The IINMIN_12V command records the minimum input voltage of the 12V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMIN_12V	00000000	Records the minimum input voltage of the 12V e-fuse after start-up.

IINMAX_12V (2Ch)

Format: Linear

The IINMAX_12V command records the maximum input voltage of the 12V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	IINMAX_12V	00000000	Records the maximum input voltage of the 12V e-fuse after start-up.

PINMIN_12V_1S (2Dh)

Format: Linear

The PINMIN_12V_1S command records the minimum input power of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMIN_12V_1s	00000000	Records the minimum input power of the 12V e-fuse in the last 1s.

PINAVG_12V_1S (2Eh)

Format: Linear

The PINAVG_12V_1S command records the average input power of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINAVG_12V_1s	00000000	Records the average input power of the 12V e-fuse in the last 1s.

PINMAX_12V_1S (2Fh)

Format: Linear

The PINMAX_12V_1S command records the maximum input power of the 12V e-fuse in the last 1s.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMAX_12V_1s	00000000	Records the minimum input power of the 12V e-fuse in the last 1s.

PINMIN_12V (30h)

Format: Linear

The PINMIN_12V command records the minimum input power of the 12V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMIN_12V	00000000	Records the minimum input power of the 12V e-fuse after start-up.

PINMAX_12V (31h)

Format: Linear

The PINMAX_12V command records the maximum input power of the 12V e-fuse after start-up.

Bits	Access	Bit Name	Default	Description
7:0	RO	PINMAX_12V	00000000	Records the maximum input power of the 12V e-fuse after start-up.

CAP_TEST_CTRL (32h)

Format: Unsigned binary

The CAP_TEST_CTRL command sets the capacitor health test configuration, including CAP_TEST_EN, deep capacitor health test delta voltage, DEEP_EN, and TOOGLE EN.

Bits	Access	Bit Name	Default	Description
6	R/W	CAP_TEST_EN	0	0: Disables capacitor test 1: Enables capacitor test
4	R/W	DV_DEEP	0	Sets the delta V_{STRG} in deep capacitor test mode. 0: 12V 1: 8V
1	R/W	DEEP_EN	0	Enables deep capacitor test mode for the capacitor test. 0: Disabled 1: Enabled
0	R/W	TOGGLE_EN	0	If this bit is enabled, INT1 goes low when discharging the storage capacitor (C_{STRG}) and goes high when C_{STRG} stops boost switching (see Figure 24). 0: Disables toggle; INT1 is not influenced by V_{STRG} discharge 1: Enables toggle; INT1 is low if the PLP stops boost switching

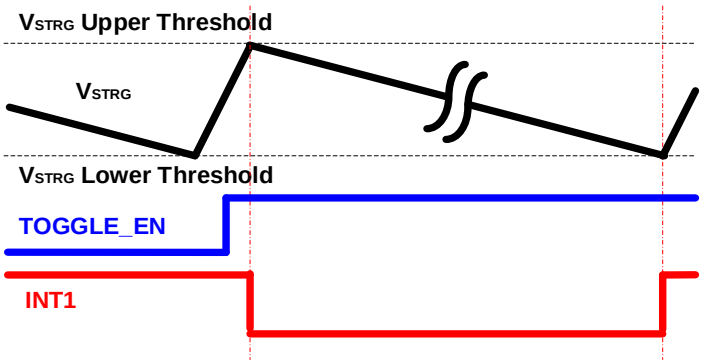


Figure 24: TOGGLE_EN Control

VSTRG1 (33h)

Format: Linear

The VSTRG1 command records the initial V_{STRG} at the beginning of the forced capacitor health test.

Bits	Access	Bit Name	Default	Description
7:0	RO	VSTRG1	00000000	Records the initial V_{STRG} at the beginning of the forced capacitor health test.

VSTRG2 (34h)

Format: Linear

The VSTRG2 command records the final V_{STRG} at the end of the forced capacitor health test.

Bits	Access	Bit Name	Default	Description
7:0	RO	VSTRG2	00000000	Records the final V_{STRG} at the end of the forced capacitor health test.

CAP_TIMER (35h)

Format: Linear

The CAP_TIMER command records the discharge time of the forced capacitor health test.

Bits	Access	Bit Name	Default	Description
7:0	RO	CAP_TIMER	00000000	Records the discharge time of the forced capacitor health test.

CAP_FAIL_TH (36h)

Format: Linear

The CAP_FAIL_TH command sets the failure threshold for the forced capacitor health test.

Bits	Access	Bit Name	Default	Description
7:0	R/W	CAP_FAIL_TH	00000000	Sets the failure threshold of the forced capacitor health test. If CAP_TIMER is below CAP_FAIL_TH, the CAP_ERR bit in the STATUS1 register is set to 1.

STATUS1 (37h)

Format: Unsigned binary

The STATUS1 command reflects over-current (OC), over-voltage (OV), and under-voltage (UV) conditions, as well as the capacitor health test error.

Bits	Access	Bit Name	Default	Description
7	1O	LIM1	0 (INT1)	0: 12V e-fuse current limit is not triggered 1: 12V e-fuse current limit is triggered
6	1O	LIM2	0 (INT1)	0: 5V e-fuse current limit is not triggered 1: 5V e-fuse current limit is triggered
5	1O	OV1	0 (INT1)	0: 12V e-fuse OV clamping is not triggered 1: 12V e-fuse OV clamping is triggered
4	1O	OV2	0 (INT1)	0: 5V e-fuse OV clamping is not triggered 1: 5V e-fuse OV clamping is triggered
3	1O	UV2	0 (INT1)	0: 5V e-fuse under-voltage (UV) does not occur 1: 5V e-fuse UV occurs
2	1O	UV1	0 (INT1)	0: 12V e-fuse UV does not occur 1: 12V e-fuse UV occurs
0	1O	CAP_ERR	0 (INT1)	0: The capacitor test does not detect capacitor failure 1: The capacitor test detects capacitor failure

STATUS2 (38h)

Format: Unsigned binary

The STATUS2 command reflects over-temperature (OT) warning, OT fault, power failure indicator, STRG power good (PG), capacitor health test completion, and PLP release time.

Bits	Access	Bit Name	Default	Description
7	1O	OTW	0 (INT2)	0: Die temperature < 120°C 1: Die temperature > 120°C
6	1O	OT	0 (INT2)	0: E-fuse or die temperature < 150°C 1: E-fuse or die temperature > 150°C
5	1O	PFI	0 (INT2)	0: PFI is low 1: PFI is high
4	1O	PGS	0 (INT2)	0: PGS is high 1: PGS is low
3	1O	CAPTEST_DONE	0 (INT2)	0: The capacitor health test is not done 1: The capacitor health test is done
1	1O	POR	0 (INT2)	0: The PLP release time is not longer than MAX_RLS_TIMER_BCKP 1: The PLP release time is longer than MAX_RLS_TIMER_BCKP

MSK_INT1 (39h)

Format: Unsigned binary

The MSK_INT1 command masks or unmasks OC, OV, and UV conditions, as well as the capacitor health test error reflected on INT1.

Bits	Access	Bit Name	Default	Description
7	R/W	MSK_LIM1	1	0: Not masked 1: Masked
6	R/W	MSK_LIM2	1	0: Not masked 1: Masked
5	R/W	MSK_OV1	1	0: Not masked 1: Masked
4	R/W	MSK_OV2	1	0: Not masked 1: Masked
3	R/W	MSK_UV2	1	0: Not masked 1: Masked
2	R/W	MSK_UV1	1	0: Not masked 1: Masked
0	R/W	MSK_CAP_ERR	1	0: Not masked 1: Masked

MSK_INT2 (3Ah)

Format: Unsigned binary

The MSK_INT2 command masks or unmasks OT warning, OT fault, power failure indicator, STRG PG, capacitor health test completion, and the PLP release time reflected on INT2.

Bits	Access	Bit Name	Default	Description
7	R/W	MSK_OTW	1	0: Not masked 1: Masked
6	R/W	MSK_OT	1	0: Not masked 1: Masked
5	R/W	MSK_PFI	1	0: Not masked 1: Masked
4	R/W	MSK_PGS	1	0: Not masked 1: Masked
3	R/W	MSK_CAPTEST_DONE	1	0: Not masked 1: Masked
1	R/W	MSK_POR	1	0: Not masked 1: Masked

ILIM1 (3Bh)

Format: Linear

The ILIM1 command sets the current limit of the 12V e-fuse.

Bits	Access	Bit Name	Default	Description
4:0	R/W	ILIM1	01011 = 2A	Sets the current limit of the 12V e-fuse. 00001: 1A 00010: 1.1A 00011: 1.2A 00100: 1.3A 00101: 1.4A 00110: 1.5A 00111: 1.6A 01000: 1.7A 01001: 1.8A 01010: 1.9A 01011: 2A 01100: 2.2A 01101: 2.4A 11111: 6A

ILIM2 (3Ch)

Format: Linear

The ILIM2 command sets the current limit of the 5V e-fuse.

Bits	Access	Bit Name	Default	Description
4:0	R/W	ILIM2	01011 = 2A	Sets the current limit of the 5V e-fuse. 00001: 1A 00010: 1.1A 00011:1.2A 00100: 1.3A 00101: 1.4A 00110: 1.5A 00111: 1.6A 01000: 1.7A 01001: 1.8A 01010: 1.9A 01011: 2A 01100: 2.2A 01101: 2.4A 11111: 6A

RLS_UVLO (3Dh)

Format: Linear

The RLS_UVLO command sets the V_{STRG} UVLO falling threshold to stop the PLP buck release.

Bits	Access	Bit Name	Default	Description
7:0	R/W	RLS_UVLO	00110111	Sets the V_{STRG} UVLO falling threshold. If V_{STRG} is below this threshold, then buck release stops. 00110111: 2.640V (min) 11111010: 12.000V (max) Step: 0.048V

CAP_TIMER_DEEP (3Eh)

Format: Linear

The CAP_TIMER_DEEP command records the discharge time of the deep capacitor health test.

Bits	Access	Bit Name	Default	Description
7:0	RO	CAP_TIMER_ DEEP	00000000	Records the discharge time of the deep capacitor health test.

SYS_CTRL2 (41h)

Format: Unsigned binary

The SYS_CTRL2 command sets the e-fuses' turn-on selection, bidirectional power-sharing converter mode, and E-FUSE_RST and ENCH_DISCHRG configuration.

Bits	Access	Bit Name	Default	Description
6	R/W	E-FUSE_ON_CTRL	1	0: 12V and 5V e-fuse turn on separately 1: 12V and 5V e-fuse turn on only if $V_{IN1} > V_{IN1\_UVLO1}$ and $V_{IN2} > V_{IN2\_UVLO2}$
5	R/W	SHARING_MODE	0	0: Bidirectional power-sharing converter operates in buck mode (either standalone or current-sharing mode) 1: Bidirectional power-sharing converter operates in boost mode (only current-sharing mode)
3	R/W	E-FUSE_RST	1	0: When QPOR = 1, the e-fuse turns on automatically if V_{STRG} is discharged to UVLO and VIN recovers 1: When QPOR = 1, even if V_{STRG} is discharged to UVLO and VIN recovers, the e-fuse does not turn on until the EN1 bit is toggled, the EN2 bit is toggled, or the EN pin is toggled
2	R/W	ENCH_DISCHRG	0	0: The RT FET turns on when the forced capacitor test (which requires a password to turn off the RT FET before checking the tantalum leakage resistance 1: The RT FET turns on when the forced capacitor test or ENCH is set to 0

DEEP_CAP_TEST_START_ADC (53h)

Format: Linear

The DEEP_CAP_TEST_START_ADC command records the initial V_{STRG} at the beginning of the deep capacitor health test.

Bits	Access	Bit Name	Default	Description
7:0	RO	DEEP_CAP_TEST_START_ADC	00000000	Records the initial V_{STRG} at the beginning of the deep capacitor health test.

VSTRG1_STORED (54h)

Format: Linear

The VSTRG1_STORED command copies the data in register 33h after the first forced capacitor health test or after detecting the rising edge of register 07h, bit[5].

Bits	Access	Bit Name	Default	Description
7:0	RO	VSTRG1_STORED	00000000	Automatically loads the initial V_{STRG} from register 33h to register 54h after the first forced capacitor health test or after detecting the rising edge of register 07h, bit[5].

VSTRG2_STORED (55h)

Format: Linear

The VSTRG2_STORED command copies the data in register 34h after the first forced capacitor health test or after detecting the rising edge of register 07h, bit[5].

Bits	Access	Bit Name	Default	Description
7:0	RO	VSTRG2_STORED	00000000	Automatically loads the final V_{STRG} from register 34h to register 55h after the first forced capacitor health test or after detecting the rising edge of register 07h, bit[5].

APPLICATION INFORMATION

Setting the Storage Voltage

V_{STRG} is set by the resistor divider connected to the FBS pin (see Figure 25).

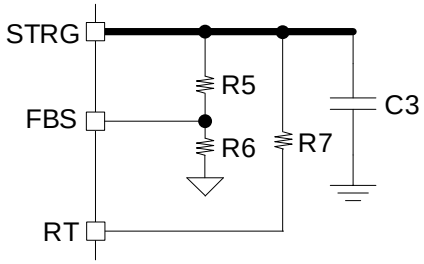


Figure 25: Storage Voltage Feedback Circuit

V_{STRG} can be calculated with Equation (12):

$$V_{STRG} = (1 + \frac{R5}{R6}) \times V_{FBS\_REF} \quad (12)$$

Where V_{FBS_REF} is typically 0.8V, and R5 and R6 are selected based on real application requirements. A low leakage current is typically expected with greater resistances for R5 and R6, which is ideal in most designs.

Table 5 lists the recommended feedback resistances for different V_{STRG} values.

Table 5: FBS Resistances for Different Storage Voltages

V_{STRG} (V)	R5 (kΩ)	R6 (kΩ)
12	140	10
20	240	10
30	365	10

Setting the Regulation Voltage in Buck Release Mode

When the PLP operates in buck release mode, the release voltage (V_{BUS_RLS}) is regulated by the resistor divider connected to the FBR pin (see Figure 26).

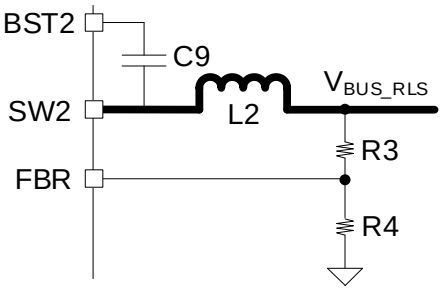


Figure 26: Release Feedback Circuit

V_{BUS_RLS} can be calculated with Equation (13):

$$V_{BUS\_RLS} = (1 + \frac{R3}{R4}) \times V_{REF} \quad (13)$$

Where V_{REF} is typically 0.8V, and the sum of R3 and R4 is recommended to be between 10kΩ and 200kΩ.

Setting the Regulation Voltage for the Power-Sharing Converter in Standalone Buck Mode

When the power-sharing converter operates in standalone buck mode, its output voltage (V_{BUCK}) is regulated by the resistor divider connected to the FB1 pin (see Figure 27).

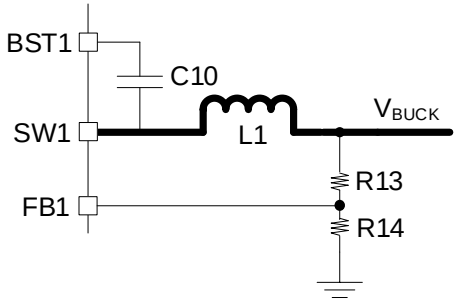


Figure 27: Power-Sharing Converter Feedback Circuit

V_{BUCK} can be calculated with Equation (14):

$$V_{BUCK} = (1 + \frac{R13}{R14}) \times V_{FB1\_REF} \quad (14)$$

Where V_{FB1_REF} is 0.6V by default, and its value can be configured between 400mV and 1.27V via the I^2C. The sum of R13 and R14 is recommended to be between 10kΩ and 200kΩ.

Setting the Threshold Voltage for Power Failures

The V_{B1} and V_{B2} thresholds that trigger buck release mode are set by the resistor dividers connected to the DET1 and DET2 pins (see Figure 28 on page 59).

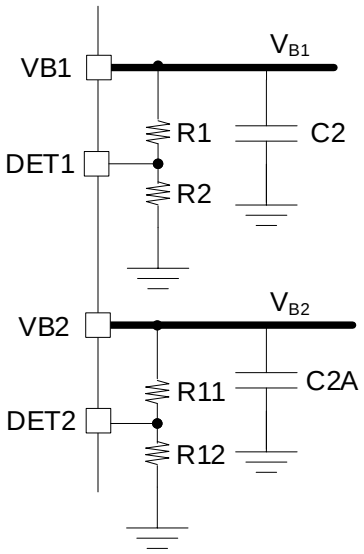


Figure 28: Power Failure Threshold Feedback Circuit

The V_{B1} threshold to trigger power failure (V_{B1_PFI}) can be calculated with Equation (15):

$$V_{B1\_PFI} = (1 + \frac{R1}{R2}) \times V_{DET1\_REF} \quad (15)$$

Where V_{DET1_REF} is typically 0.8V, and the sum of R1 and R2 is recommended to be between 10kΩ and 200kΩ.

The V_{B2} threshold to trigger power failure (V_{B2_PFI}) can be calculated with Equation (16):

$$V_{B2\_PFI} = (1 + \frac{R11}{R12}) \times V_{DET2\_REF} \quad (16)$$

Where V_{DET2_REF} is typically 0.8V, and the sum of R11 and R12 is recommended to be between 10kΩ and 200kΩ.

Setting the VBx Rising Time

Connect a capacitor to the DVDT1 and DVDT2 pins to control the slew rate when V_{B1} or V_{B2} rises during start-up. To calculate the rising time during SS, see Equation (1) and Equation (2) on page 20. Table 6 lists the recommended capacitance for e-fuse 1's SS time (t_{DVDT1}).

Table 6: Soft-Start Time for DVDT1 Capacitance

t_{DVDT1} (ms)	C_{DVDT1} (nF)
3.4	10

.

Table 7 lists the recommended capacitance for e-fuse 2's SS time (t_{DVDT2}).

Table 7: Soft-Start Time for DVDT2 Capacitance

t_{DVDT2} (ms)	C_{DVDT2} (nF)
2.8	10

Selecting the Storage Capacitor

C_{STRG} stores energy during normal operation and releases this energy to VBx during input power loss. General-purpose electrolytic capacitors or low-profile POS capacitors are used for most applications. The capacitor's voltage rating is recommended to exceed the target V_{STRG} by 20%.

Consider the capacitance reduction with the DC voltage offset. Different capacitors have different capacitance derating performances. It is recommended to choose a capacitor with a sufficient voltage rating to guarantee the capacitance.

The required capacitance depends on the length of the dying gasp for a typical application. The required C_{STRG} can be calculated with Equation (17):

$$C_{STRG} = \frac{2 \times V_{BUS\_RLS} \times I_{RLS} \times t_{DASP}}{(V_{STRG})^2 - (V_{BUS\_RLS})^2 \times Eff} \quad (17)$$

Where I_{RLS} is the bus release current when V_{BUS} is regulated at V_{BUS_RLS} in buck release mode, t_{DASP} is the required dying gasp time, and Eff is the energy release efficiency in buck release mode.

C_{STRG} should be selected considering the efficiency in buck release mode. For example, if I_{RLS} is 3A, t_{DASP} is 20ms, V_{STRG} is 28V, V_{BUS_RLS} is 7.5V, and efficiency is 90%, then the required C_{STRG} is 1374μF.

Selecting the Bootstrap (BST), CT1, and CT2 Capacitors

The bootstrap (BST) capacitor (C_{BST}) supplies power to the buck converter's HS-FET. A 0.1μF to 1μF ceramic capacitor is recommended for BST decoupling. Connect a minimum 0.1μF ceramic capacitor between the CT1 and power ground to achieve stable operation in boost-sharing

mode. In buck-sharing mode, CT1 and VB1 can be connected directly. The CT2 capacitor stabilizes the pre-charge loop of the PLP converter. It is recommended to connect a minimum 2.2µF capacitor between the CT2 pin and power ground.

Selecting the RT Resistor for the Capacitor Test

During the capacitor test, the MP5520 discharges C_{STRG} via an external resistor connected to the RT pin and the internal discharge FET. The internal discharge FET is connected between RT and GND with a resistance of about 1Ω.

The discharge peak current should be limited below 500mA via the external resistor. A 1kΩ to 15kΩ discharge resistor is typically recommended.

Selecting the Input Capacitor and TVS Diode

A voltage spike may be observed during the input switches' start-up or fast shutdown. Adding an input capacitor can effectively attenuate the voltage spike. The required capacitance should be determined by the application. Generally, larger capacitances can attenuate voltage spikes more effectively.

However, using larger input capacitance results in higher input inrush current, especially during hot-plug conditions. A minimum 0.1µF capacitor is recommended since higher capacitances may cause inrush current issues.

An efficient solution to mitigate the issues caused by the voltage spike is to add a TVS diode at the input. This also helps limit the inrush current during hot-plug situations.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 29 on page 61 and follow the guidelines below:

1. Connect the high-current paths (VINx, VBx, CTx, SWx, STRG, and PGND) using short, wide, and direct traces.
2. Keep the SW1 and SW2 trace as short as possible, and route them away from the feedback network.
3. Place the decoupling capacitor across VBx and PGND, as close to the device as possible.
4. Place the decoupling capacitor across CT2 and PGND, as close to the device as possible.
5. If using a large-volume capacitor, place a small ≥2.2µF ceramic capacitor as close to CT2 and PGND as possible.
6. Place the decoupling capacitor across VCC and AGND, as close to the device as possible.
7. The feedback resistors should be placed next to FBR, FBS, FB1, and DET.
8. Keep the BST voltage path (BST, C_{BST}, and SW) as short as possible.
9. Connect all signal grounds together, then connect the signal grounds to PGND using a one-point connection.

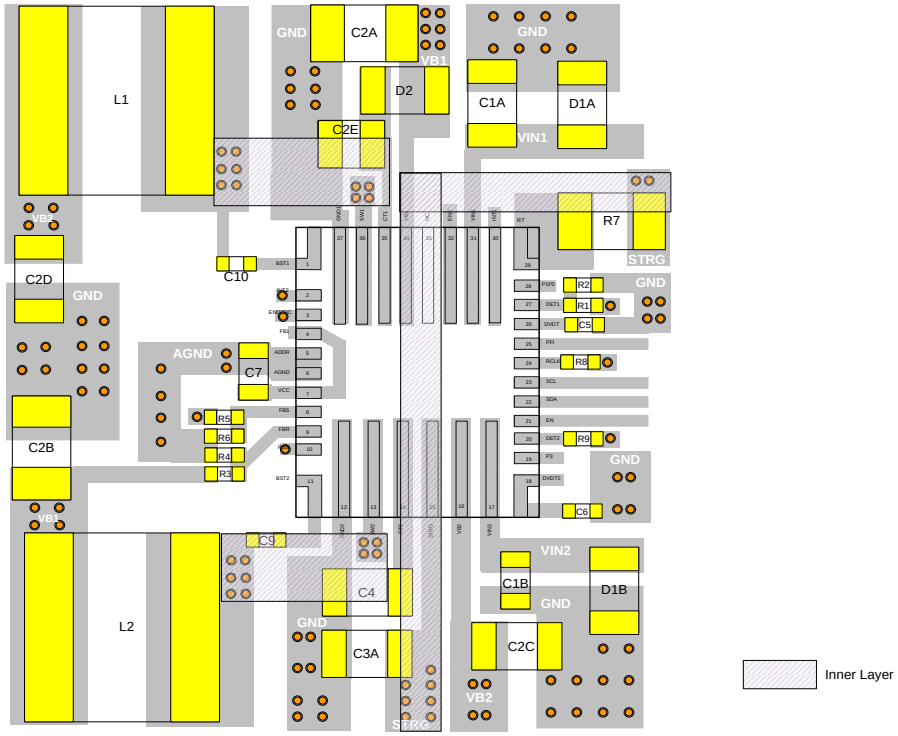


Figure 29: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

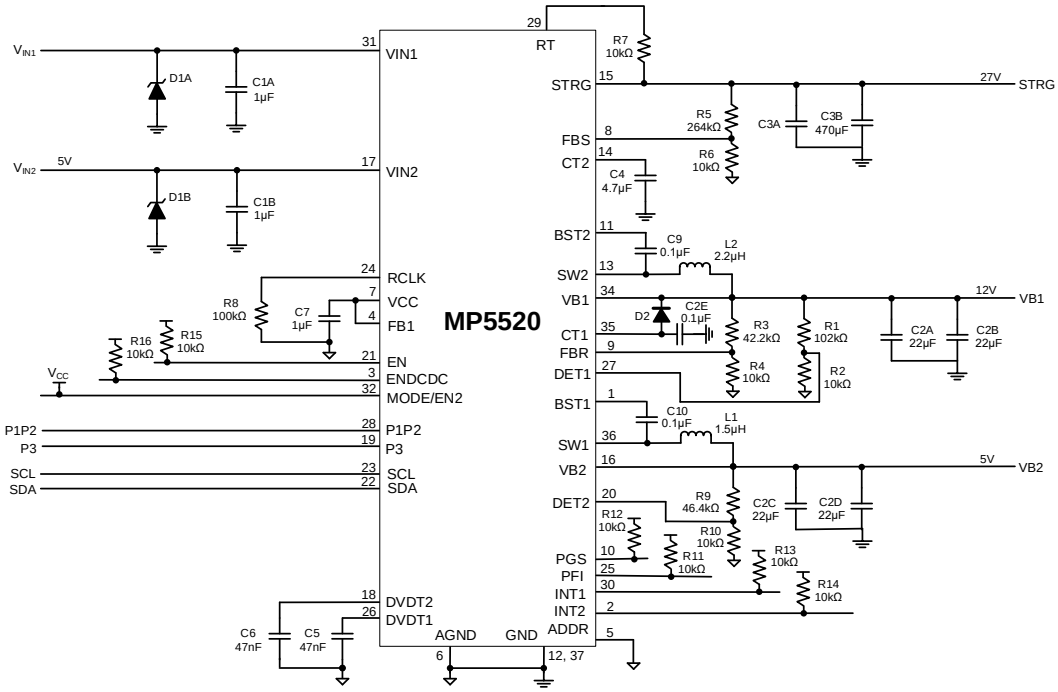


Figure 30: Typical Application Circuit 1

APPENDIX: LOGIC FLOW OF APPLICATION 1

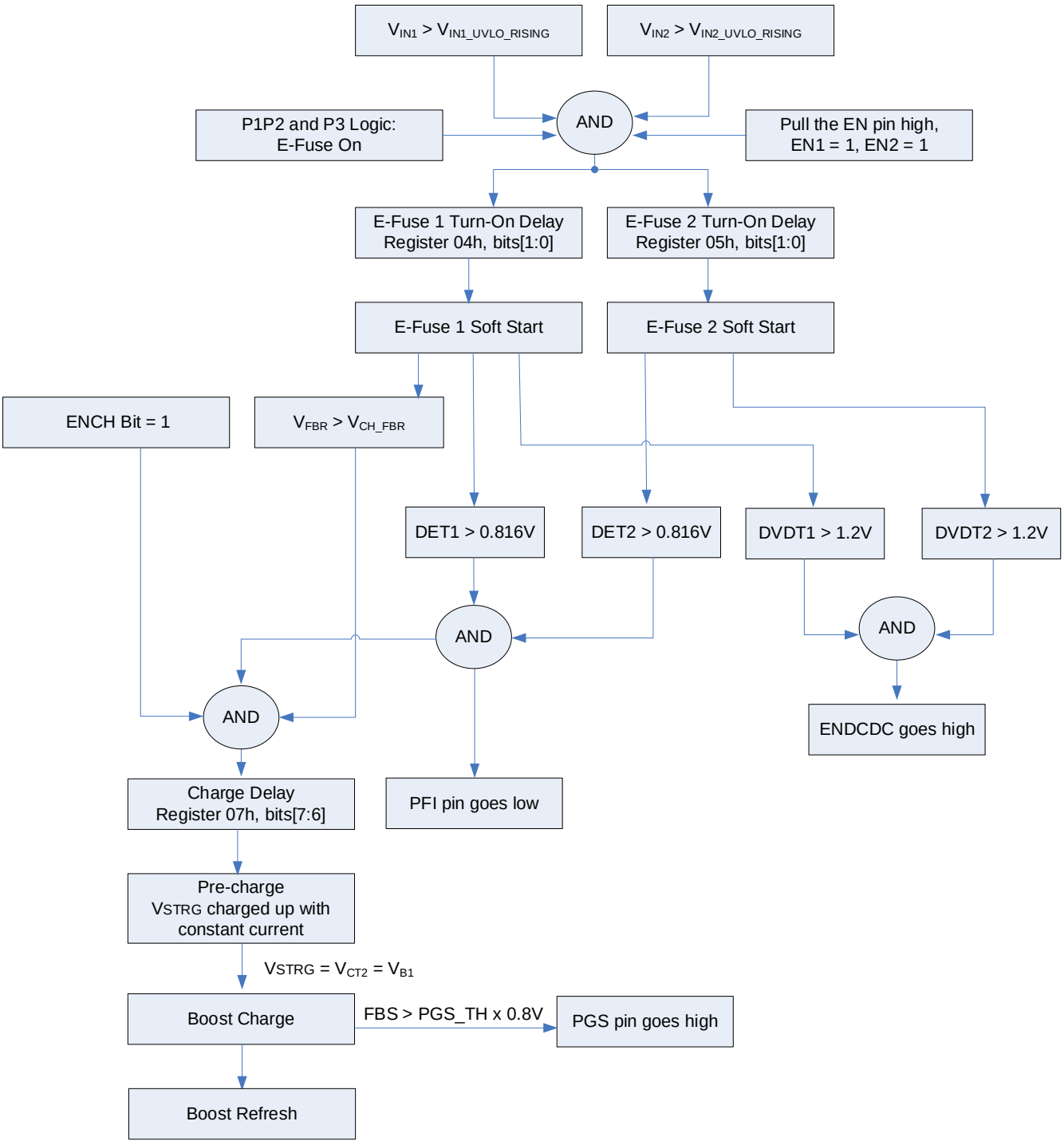


Figure 31: Normal Start-Up

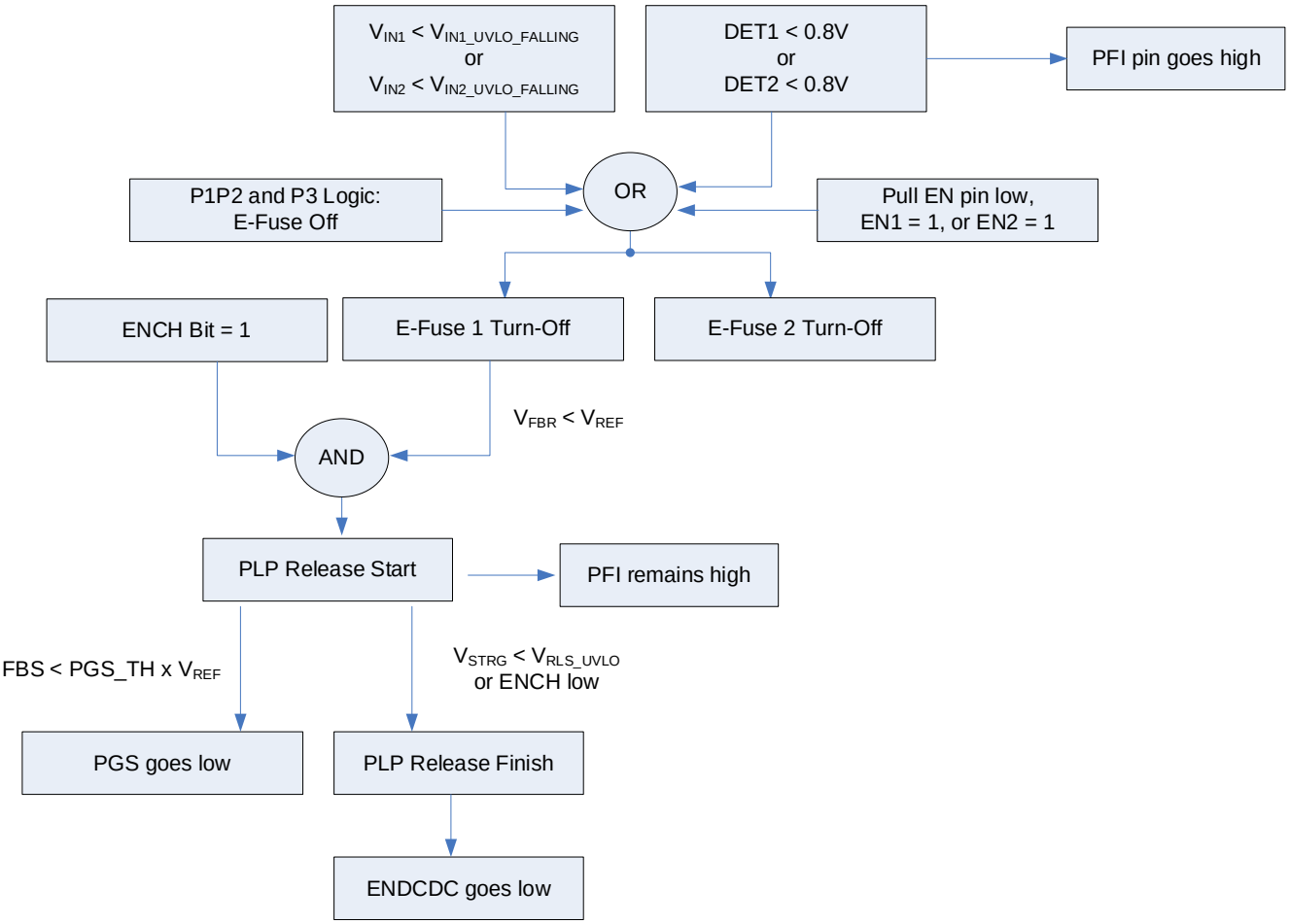


Figure 32: Normal Shutdown

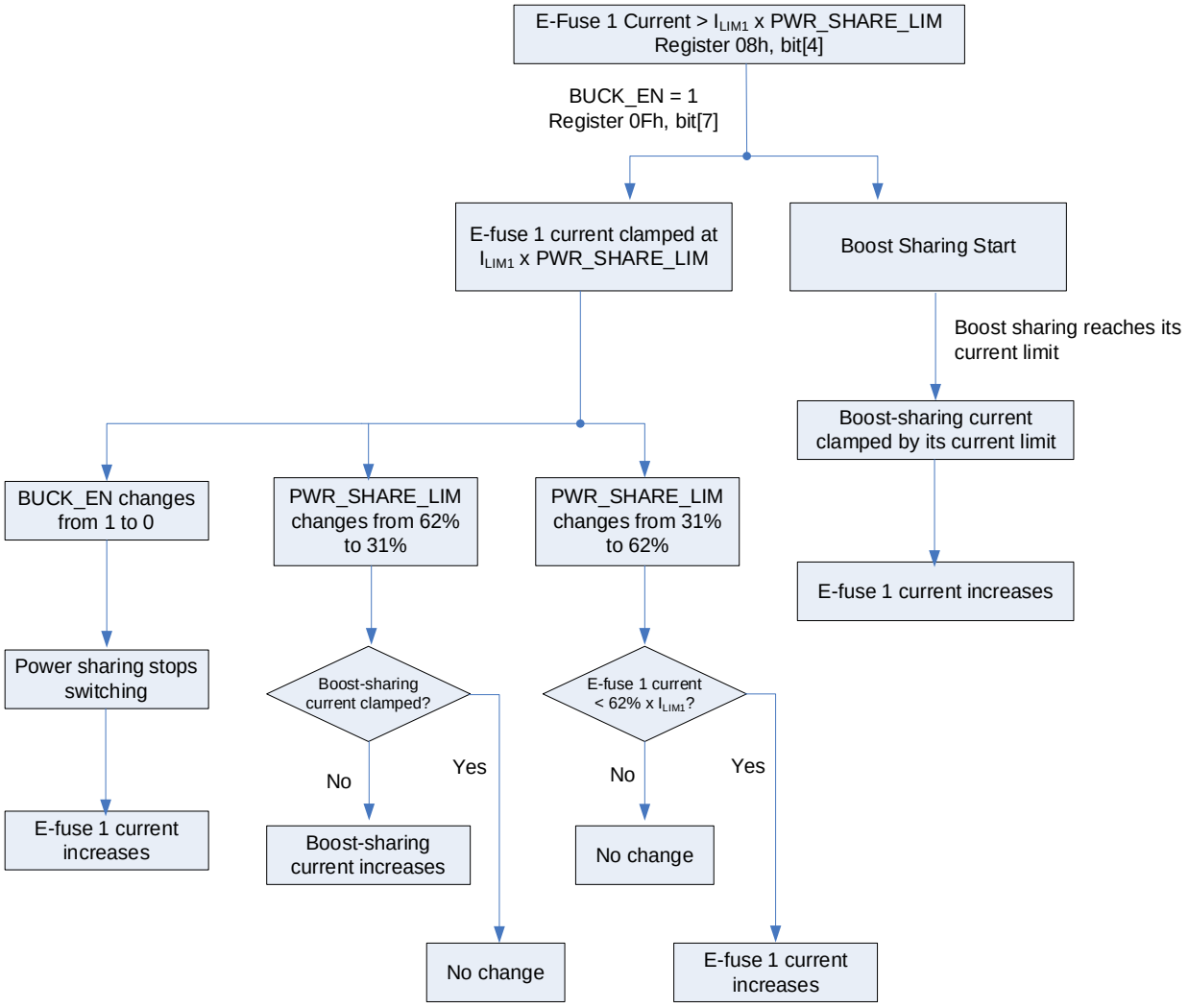


Figure 33: Power Sharing

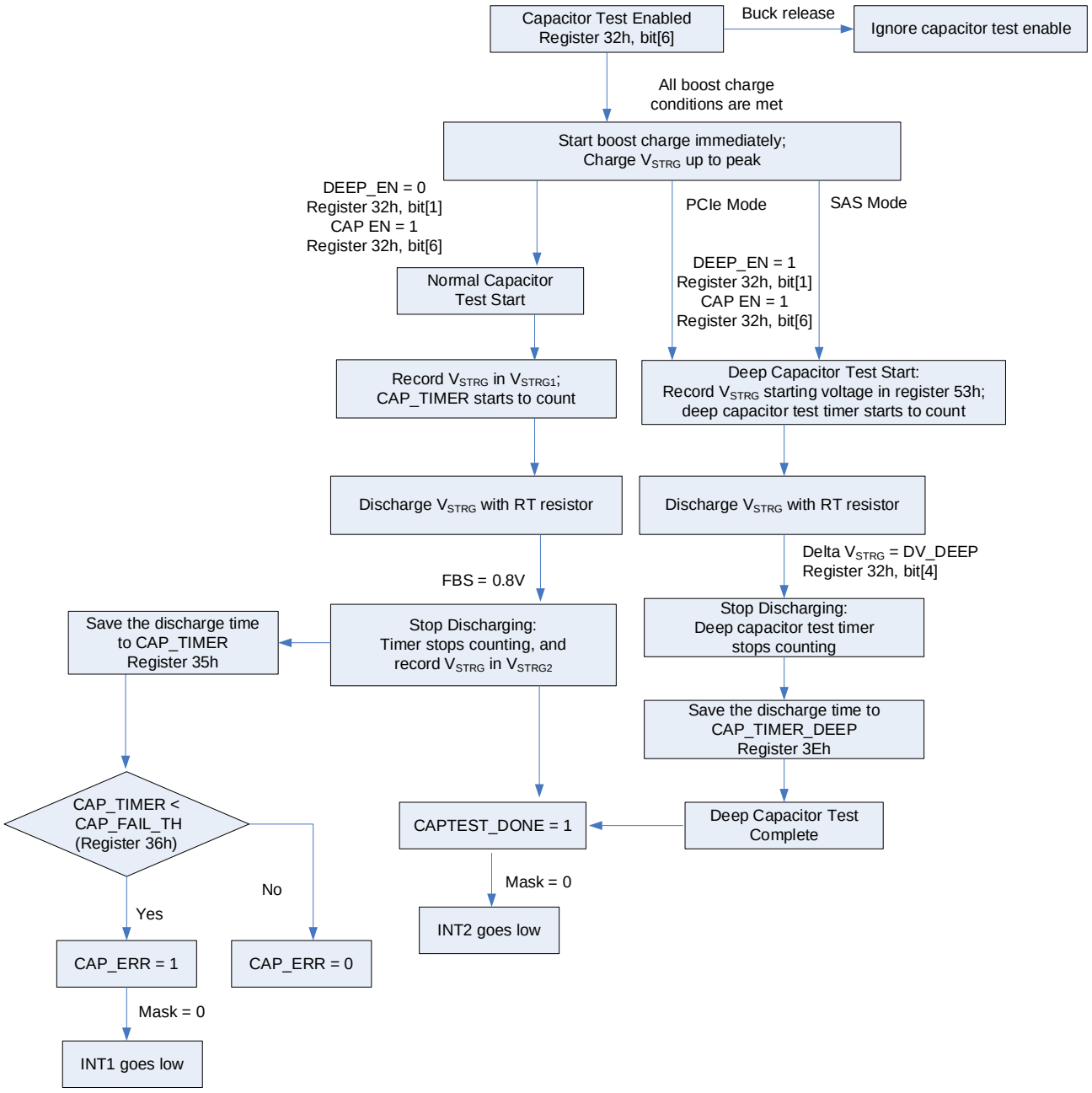


Figure 34: Capacitor Test (14)

Note:

14) Since buck release has the highest priority, if the PLP needs to buck release during the capacitor test, the MP5520 stops the capacitor test immediately.

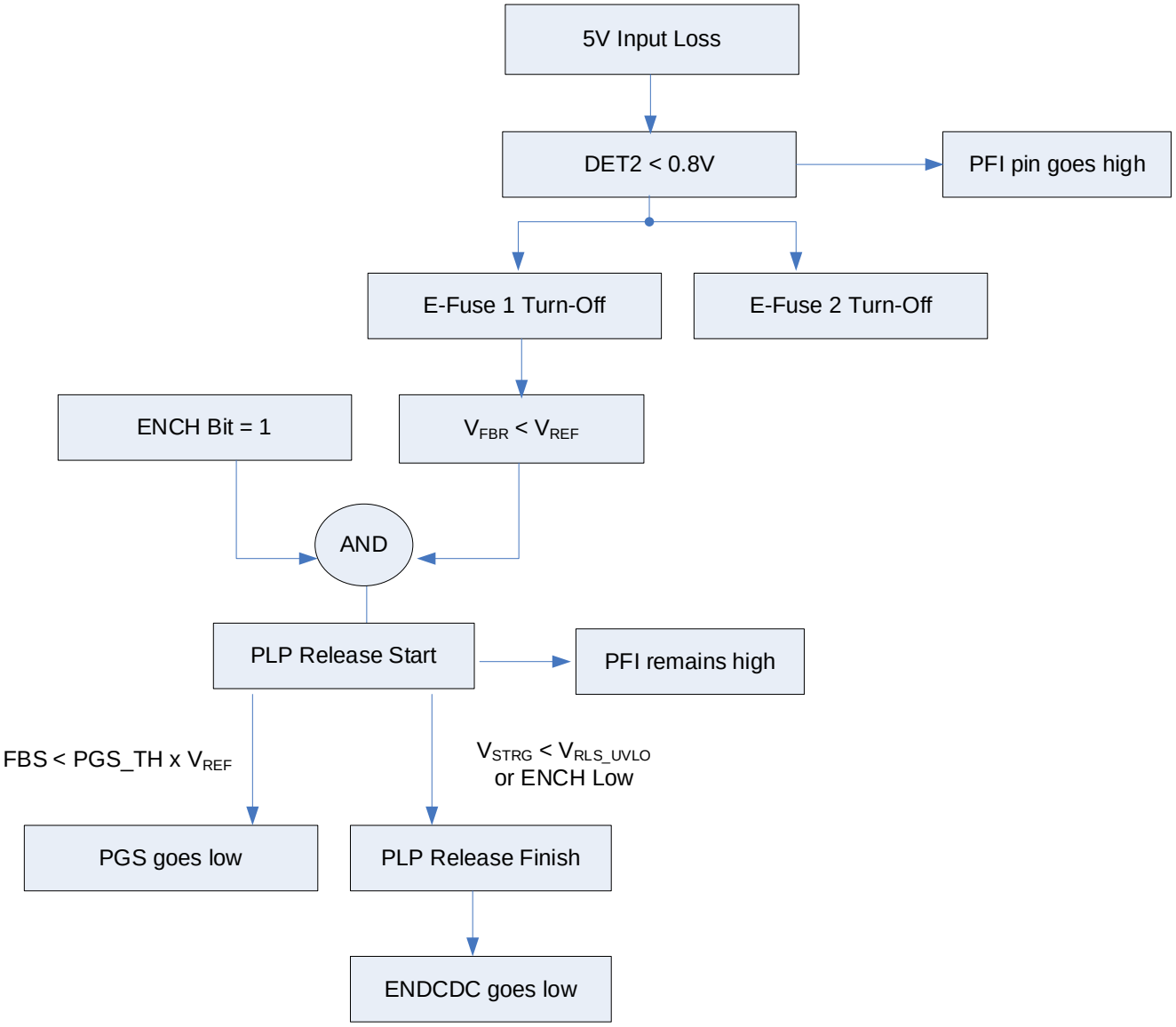


Figure 35: 5V Input Loss

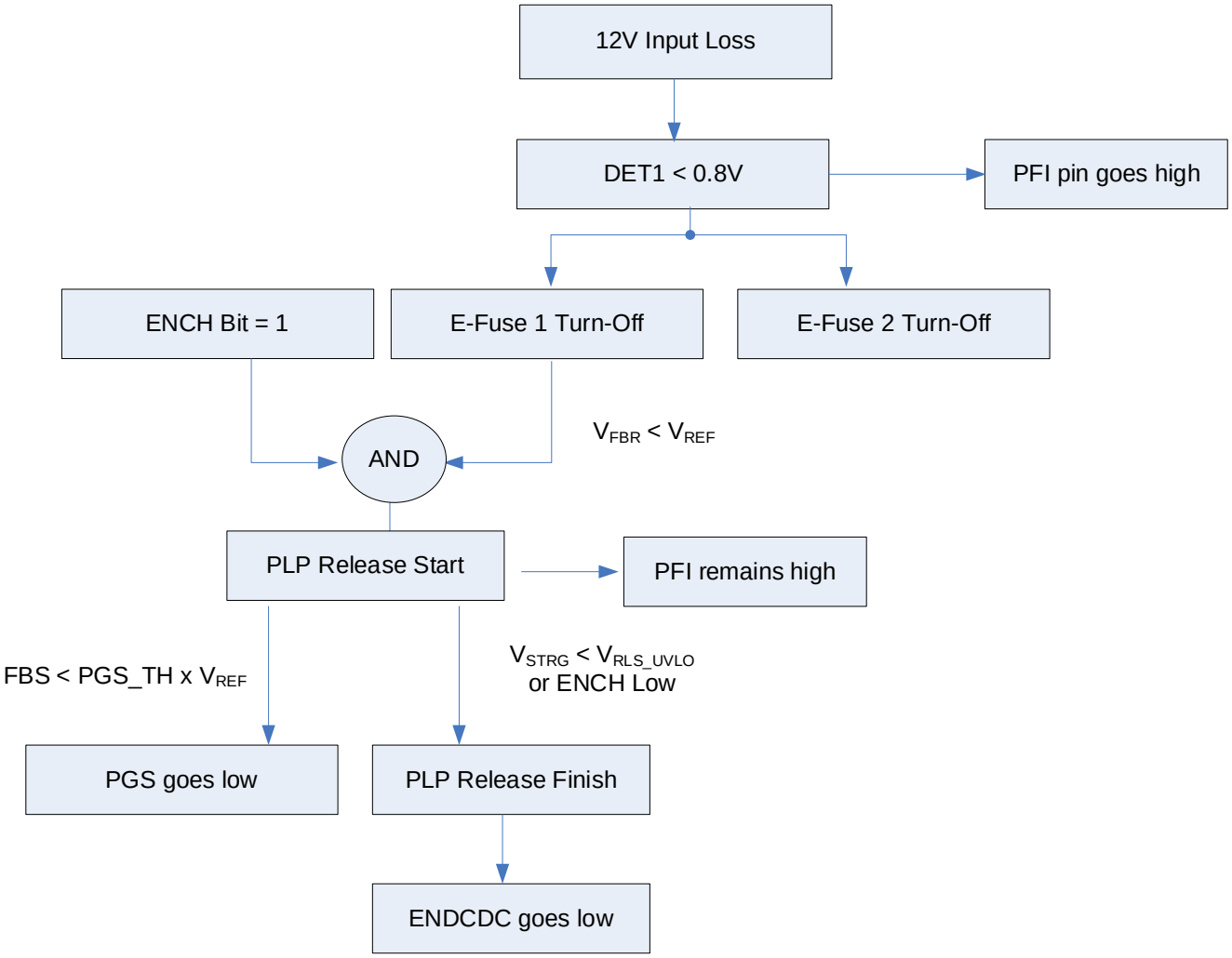


Figure 36: 12V Input Loss

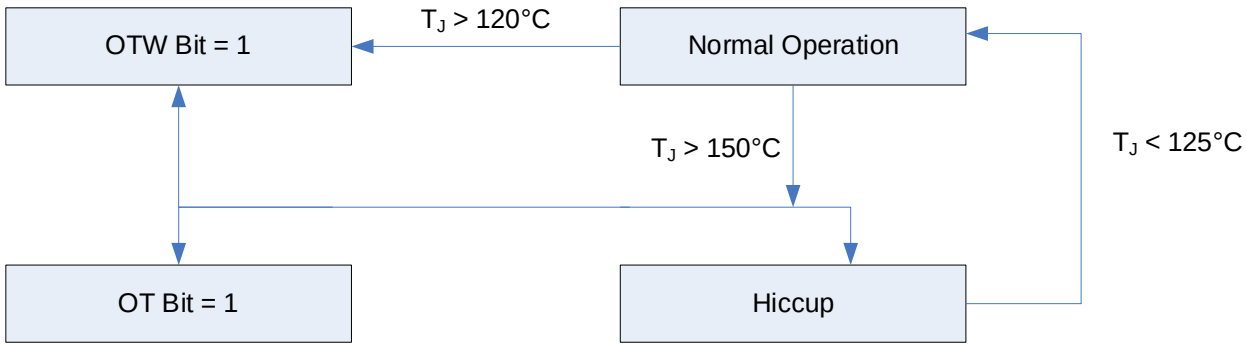


Figure 37: Thermal Shutdown

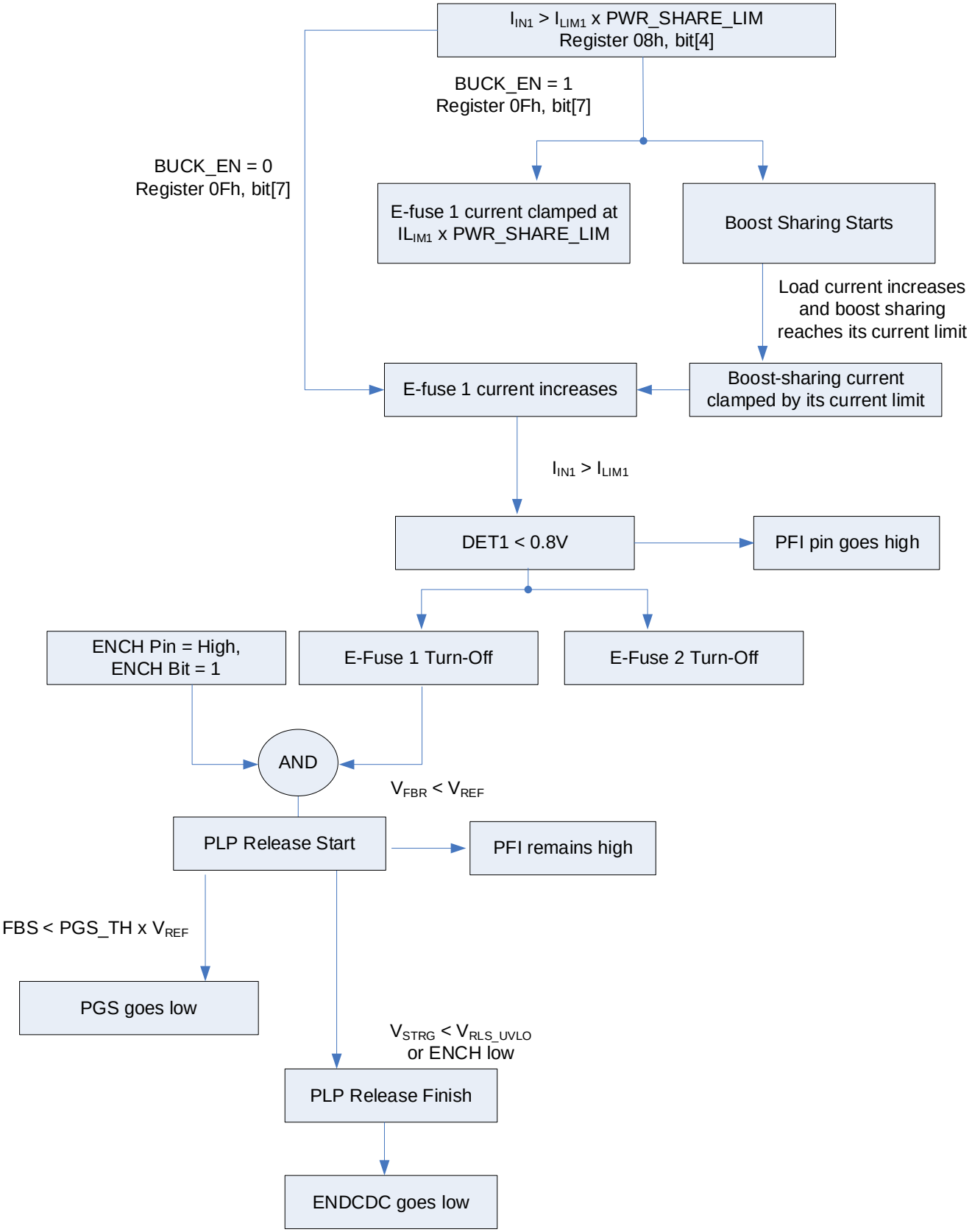


Figure 38: E-Fuse 1 Over-Current (OC) Logic

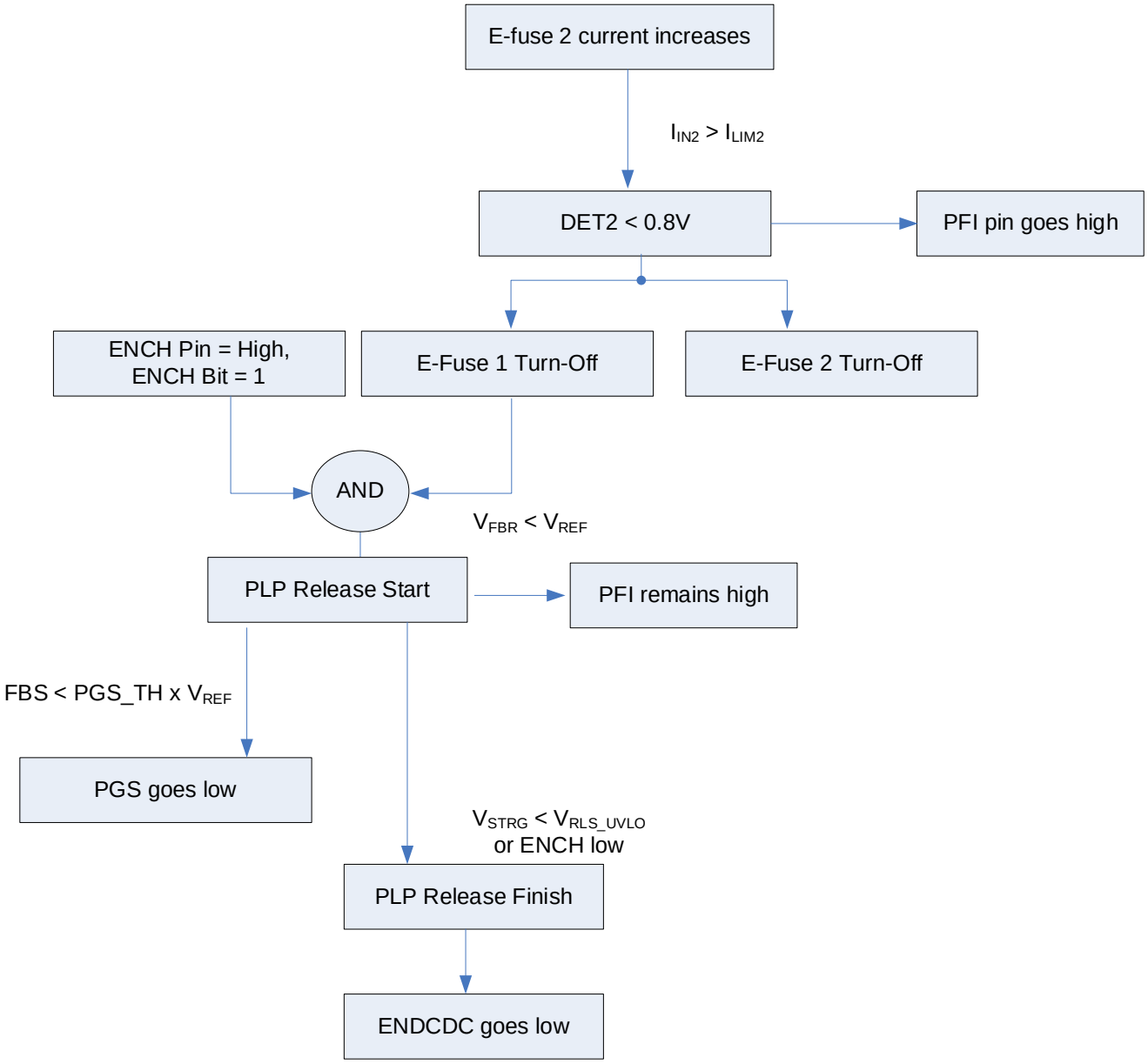


Figure 39: E-Fuse 2 Over-Current (OC) Logic

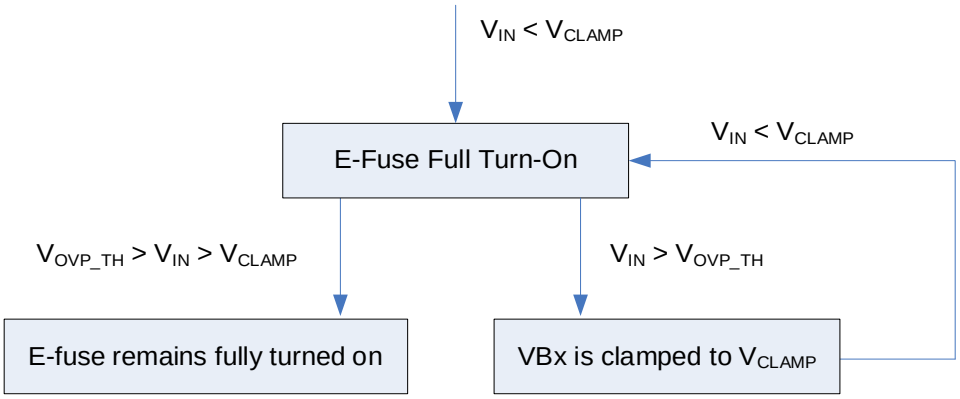


Figure 40: E-Fuse Over-Voltage Protection (OVP)

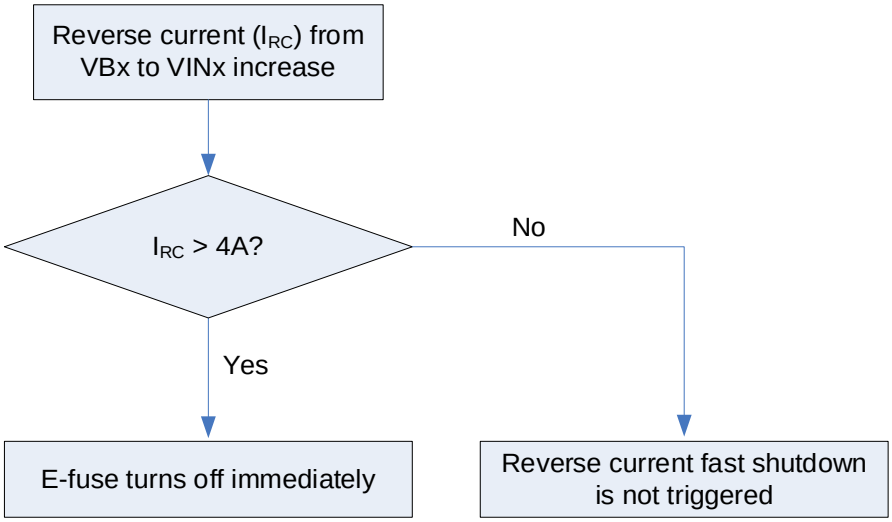


Figure 41: E-Fuse Reverse Current Fast Shutdown

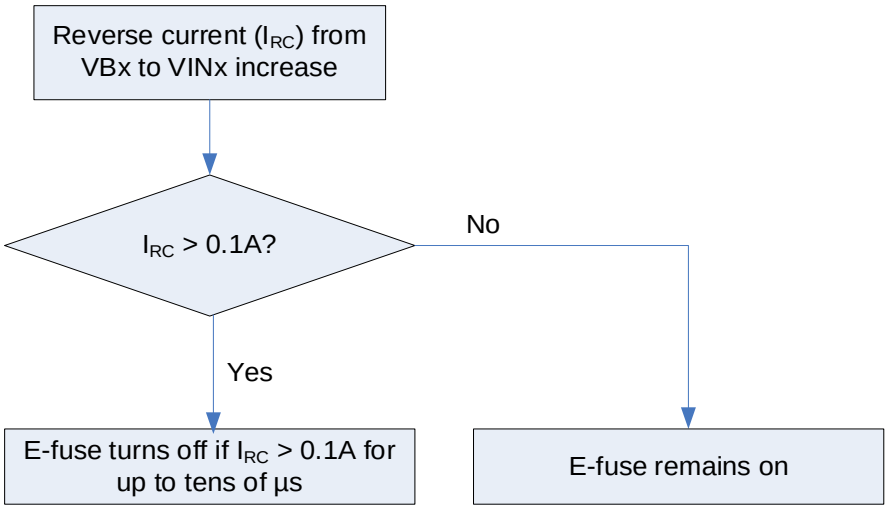
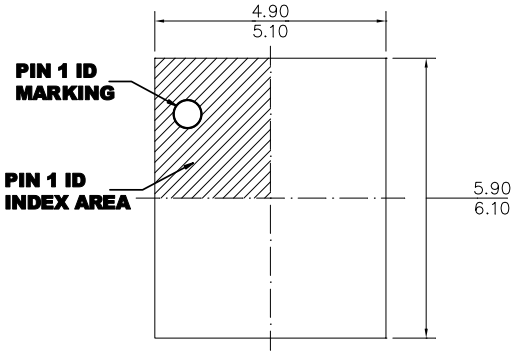


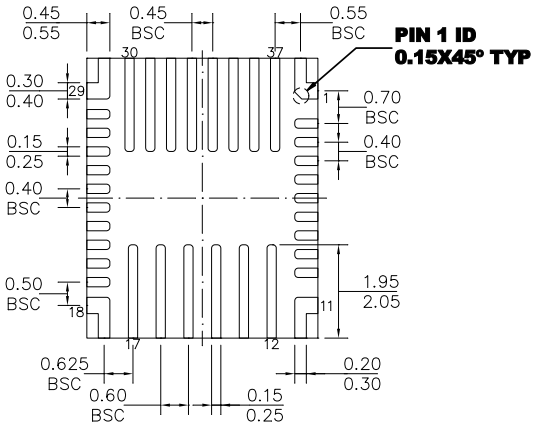
Figure 42: E-Fuse Reverse Current Block

PACKAGE INFORMATION

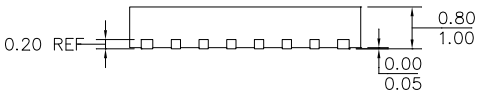
QFN-37 (5mmx6mm)



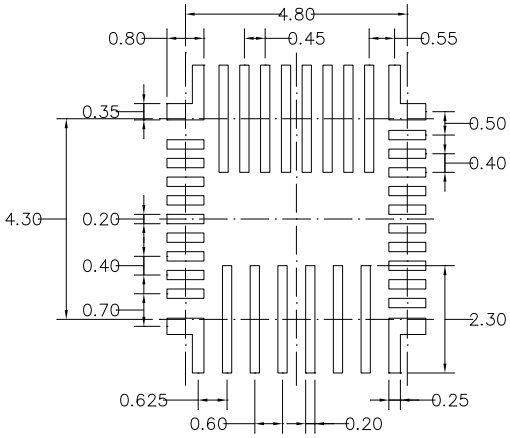
TOP VIEW



BOTTOM VIEW



SIDE VIEW

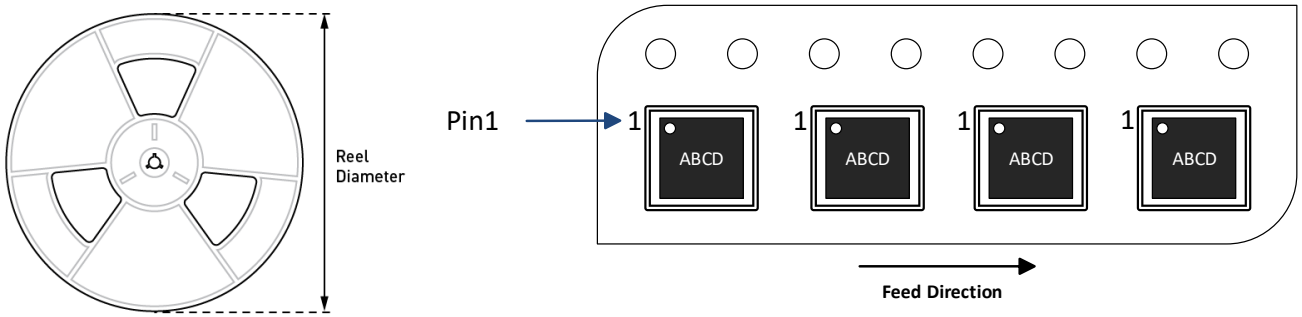


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP5520GQJ-xxxx-Z	QFN-37 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/2/2024	Initial Release	-