MP8004

13W 802.3af PoE Powered Device Interface with Flyback DC/DC Converter

The Future of Analog IC Technology

DESCRIPTION

The MP8004 is an integrated IEEE 802.3af PoE compliant Powered Device (PD) power supply solution. It includes a PD interface and an isolated/non-isolated flyback converter.

The PD interface includes detection and classification modes as well as a 100V output pass device. An inrush current limit is included to charge the input capacitor slowly without interruption due to die heating.

The DC/DC converter includes a 150V power switch and is capable of delivering 13W PoE power with high efficiency. It has an internal soft start and auto-retry. Also, it incorporates over-current, short-circuit, and over-voltage protection. It can also skip cycles to maintain zero load regulation.

The MP8004 supports a front-end solution for PoE-PD application with minimal external components and is available in a thermally enhanced 4mm x 6mm QFN-20 package.

FEATURES

- Meets IEEE 802.3af Specifications
- 100V, 1Ω Integrated Pass Switch
- 420mA DC Input Current Limit
- 150V, 0.45Ω Integrated Switch for Power Converter
- Cycle-by-Cycle Switching Current Limit
- Integrated 100V Start-Up Circuit
- Programmable Switching Frequency
- Duty Cycle Limiting with Line Feed Forward
- Internal Slope Compensation
- OCP, SCP, and OTP
- 4mm x 6mm QFN-20 Package

APPLICATIONS

- VoIP Telephones
- Security Camera Systems
- Wireless Access Points/Wireless LAN
- Small-Cell Base Stations
- Safety Backup Power
- Remote Internet Power

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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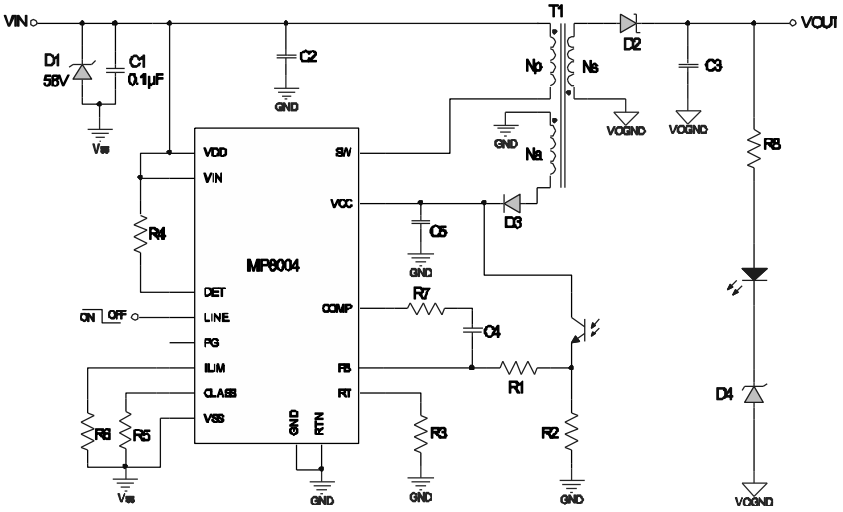
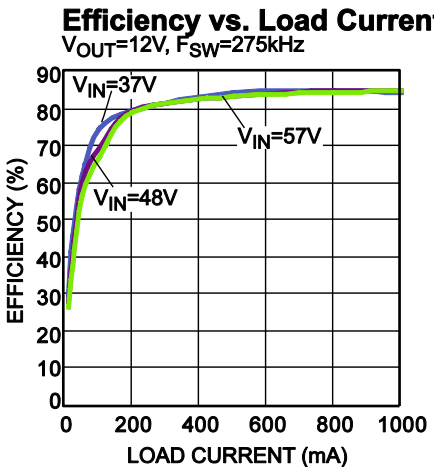
TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8004GQW	QFN-20 (4mmX6mm)	*See Below*

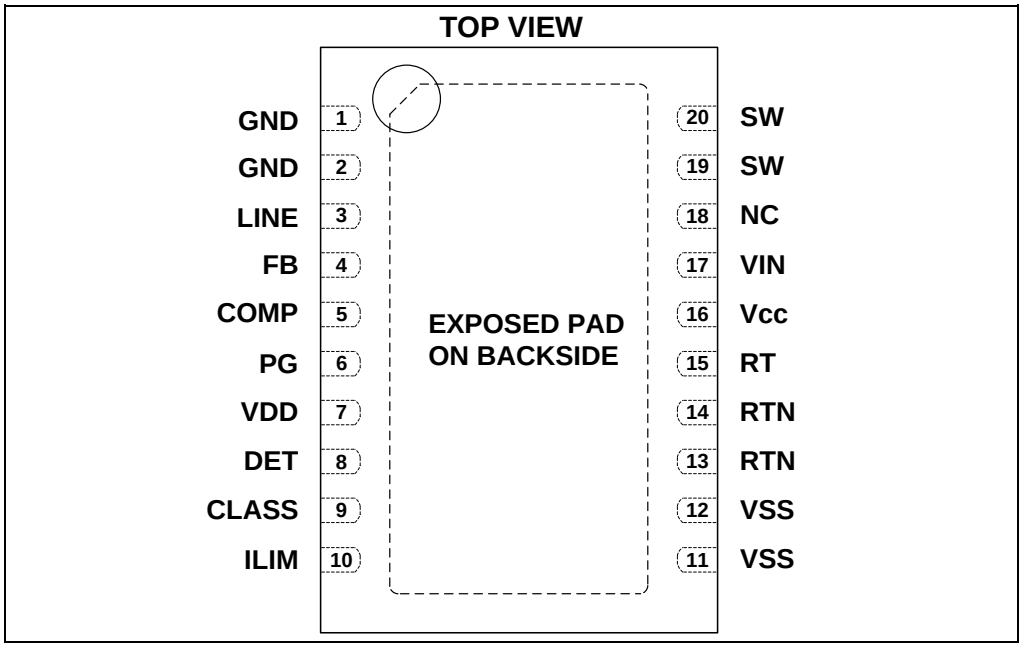
* For Tape & Reel, add suffix –Z (e.g. MP8004GQW–Z)

TOP MARKING

MPSYWW
MP8004
LLLLLL

MPS: MPS prefix:
Y: year code;
WW: week code:
MP8004: part number;
LLLLLL: lot number;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{DD}, V_{IN}, RTN ..... -0.3V to +100V
PG, DET ..... -0.3V to +57V
CLASS ..... -0.3V to +12V
V_{SW} ..... -0.5V to +180V
All other Pins ..... -0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) (2)
.....3.4W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature.....-65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{DD}, V_{IN} ..... 0V to 57V
Supply Voltage V_{CC} ..... 4.5 V to 6V
Switching Voltage V_{SW} ..... -0.5V to +150V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-20 (4mmx6mm) …...…..36…..…8…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD}, CLASS, ILIM and DET voltages are referenced to V_{SS}, and all other pin voltages are referenced to GND, GND and RTN are shorted. V_{DD} – V_{SS} = 48V, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42kΩ, R_{ILIM} = 178kΩ, V_{CC} = 5.0V, V_{LINE} = 1.8V, RT = 20kΩ, T_A = 25°C, unless otherwise noted.

PD Section

Parameter	Symbol	Condition		Min	Typ	Max	Units
Detection							
Detection on	V_{DET_ON}	V_{DD}=V_{RTN}=V_{PG}=1.9V			1.9		V
Detection off	V_{DET_OFF}	V_{DD}=V_{RTN}=V_{PG}=11V			11		V
Detection on/off Hysteresis	V_{DET_H}	Falling below 11V on Threshold			0.2		V
DET Leakage Current	V_{DET_LK}	V_{DET}=V_{VDD}=57V, Measure I_{DET}			0.1	5	μA
Detection Current	I_{DET}	V_{VDD}=V_{RTN} R_{DET}=26.1kΩ, Measure I_{VDD}+I_{RTN}+I_{DET}	V_{DD}= 3V	135	140	145	μA
			V_{DD}= 10.1V	405	420	435	μA
Classification							
V_{CLASS} Output Voltage	V_{CL}	Over a Load Range of 1mA to 41.2 mA		9.6	10	10.4	V
Classification Current	I_{CLASS}	R_{CLASS}=4420Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		2.2	2.4	2.8	mA
		R_{CLASS}=953Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		10.3	10.6	11.3	
		R_{CLASS}=549Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		17.7	18.3	19.5	
		R_{CLASS}=357Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		27.1	28	29.5	
		R_{CLASS}=255Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		38	39.4	41.2	
Classification Lower Threshold	V_{CL_ON}	Regulator Turns on, V_{VDD} Rising		10.2	11.3	13	V
Classification Upper Threshold	V_{CU_OFF}	Regulator Turns off, V_{VDD} Rising		21	21.9	23	V
Classification Hysteresis	V_{CU_H}	Hysteresis			0.4		V
IC Supply Current during Classification	I_{IN_CLASS}	V_{DD} = 17.5V, CLASS Floating, RTN Tied to VSS			160	250	μA
Leakage Current	$I_{LEAKAGE}$	V_{CLASS} = 0 V, V_{VDD} = 57V				1	μA
Pass Device							
On Resistance	$R_{DS(ON)}$	I_{RTN}=300mA			1.0	1.2	Ω
Leakage Current	I_{SW_LK}	V_{RTN}=57V			1	15	μA
Current Limit	I_{LIMIT}	V_{RTN}=1V		380	420	460	mA
Inrush Limit	I_{INRUSH}	V_{RTN}=2V, R_{ILM}=178kΩ		120	150	200	mA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD}, CLASS, ILIM and DET voltages are referenced to V_{SS}, and all other pin voltages are referenced to GND, GND and RTN are shorted. V_{DD} – V_{SS} = 48V, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42kΩ, R_{ILIM} = 178kΩ, V_{CC} = 5.0V, V_{LINE} = 1.8V, RT = 20kΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG						
Latch off Voltage Threshold Rising (5)		V_{RTN} Rising	9.5	10	10.5	V
Latch off Voltage Threshold Falling (5)		V_{RTN} Falling		1.2		V
PG Deglitch (6)		Delay Rising and Falling		345		µs
Output Low Voltage		I_{PG} = 400 µA		0.12	0.4	V
Leakage Current		V_{PG} = 57 V, V_{RTN} = 0 V		0.1	1	µA
UVLO						
Voltage at V_{DD}		V_{DD} Rising (including 1.4V Diode drop)	38	40	42	V
		V_{DD} Falling (including 1.4V Diode drop)	30.2	31.5	32.8	
Thermal Shutdown						
Thermal Shut down Temperature (6)	T_{RISE}	Temperature Rising		125		ºC
Hysteresis (6)	T_{HYS}			20		ºC
Thermal Shut down Counter(5)	T_{COUNT}	Events Prior to Latch off		8		counts
Thermal Counter Reset Voltage(5)	V_{CRST}	Must Drop below Classification Range		10.8		V
Bias Current						
Operating Current	$I_{Q(VDD)}$	V_{DD} = 48V, PG, RTN Floating Measure I_{VDD}		240	450	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{DD}, CLASS, ILIM and DET voltages are referenced to V_{SS}, and all other pin voltages are referenced to GND, GND and RTN are shorted. V_{DD} – V_{SS} = 48V, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42KΩ, R_{ILIM} = 178kΩ, V_{CC} = 5.0V, V_{LINE} = 1.8V, RT = 20k, T_A = 25°C, unless otherwise noted.

DCDC Converter Section

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Quiescent Supply Current	I_{CC}	V_{FB} = 1.3V		1.0	1.5	mA
Line OV Threshold Voltage		V_{CC} = 5.0V, V-Line Rising	2.85	3	3.15	V
Line OV Hysteresis		V_{CC} = 5.0V		300		mV
Line UV Threshold Voltage		V_{CC} = 5.0V, V-Line Rising	1.16	1.21	1.26	V
Line UV Hysteresis		V_{CC} = 5.0V		100		mV
V_{CC} Upper Threshold Voltage			5.6	5.85	6.1	V
V_{CC} Lower Threshold Voltage			4.30	4.50	4.70	V
V_{CC} Over Voltage Threshold Voltage (6)			6.3	6.6	6.9	V
Startup Current	I_{st}	V_{IN} = 48V, V_{CC} = 4.0V		10		mA
Voltage Feedback						
Feedback Voltage	V_{FB}		1.16	1.21	1.26	V
Feedback Input Current	I_{FB}	V_{FB} = 1.2V		50		nA
Error Amplifier Gain Bandwidth (5)	GBW		1			MHz
Error Amplifier DC Gain (5)	A_V		60			dB
Comp Output Source Current	I_{OH}	V_{FB} = 1.0V, V_{COMP} = 0.5V		2		mA
Comp Output Sink Current	I_{OL}	V_{FB} = 1.4V, V_{COMP} = 2.5V		2		mA
Power Device						
Switch-On Resistance	R_{ON}	V_{SW} = 0.1V		0.45		Ω
Switch Leakage Current	I_{LK}	V_{SW} = 150V		1		μA
Current Limit (6)	I_{LIM}			4		A
PWM						
Minimum Oscillating Frequency	F_{MIN}	RT = 100k		55		kHz
Maximum Oscillating Frequency	F_{MAX}	RT = 10k		550		kHz
Thermal Shutdown						
Thermal Shutdown (6)				150		°C
Thermal Shutdown Hysteresis (6)				30		°C

Notes:

5) Guaranteed by design

6) Guaranteed by engineering sample characterization.

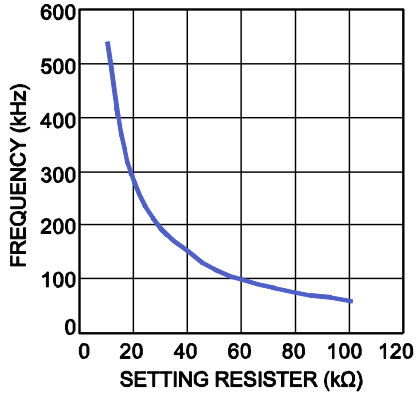
PIN FUNCTIONS

Pin #	Name	Description
1, 2	GND	Ground. DCDC converter power return and reference node.
3	LINE	Input UV/OV Set Point. Short to ground to turn the controller off.
4	FB	Regulation Feedback Input. Inverting input of the error amplifier. The non-inverting is internally connected to 1.21V
5	COMP	Error Amplifier Output.
6	PG	PD Output Power Good Indicator.
7	VDD	Positive Power Supply Terminal.
8	DET	PoE detection resistance pin. Connect 26.1kΩ detection resistor to this pin to compensate IC leakage.
9	CLASS	PoE Classification Resistor Pin.
10	ILIM	PD startup current limit setting pin.
11, 12	VSS	Negative Power Supply Terminal.
13, 14	RTN	Drain of PD pass MOSFET. Connect GND pin to this pin.
15	RT	Oscillator Resistor and Synchronous Clock Pin. Connect an external resistor to GND for oscillator frequency setting. It can be used as a synchronous input from external oscillator clock.
16	Vcc	Supply Bias Voltage for DC converter. A capacitor no less than 1uF is recommended to connect between this pin and GND.
17	VIN	DCDC converter High Voltage Startup Circuit Supply.
18	NC	No Connect.
19, 20	SW	Output Switching Node. High voltage power N-Channel MOSFET drain output.
	EXPOSED PAD	Used to heat sink from the part to the circuit board traces. Must be connected to the GND pins (pin 1,2)

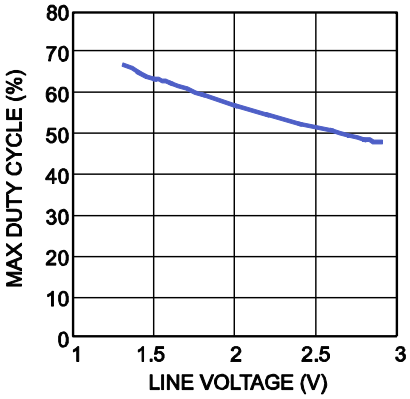
TYPICAL CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

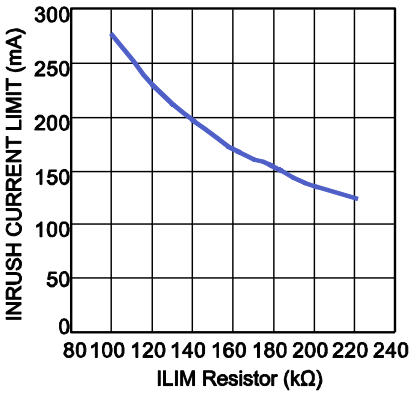
Frequency vs. Setting Resister



DCDC Max Duty Cycle vs. Line Voltage

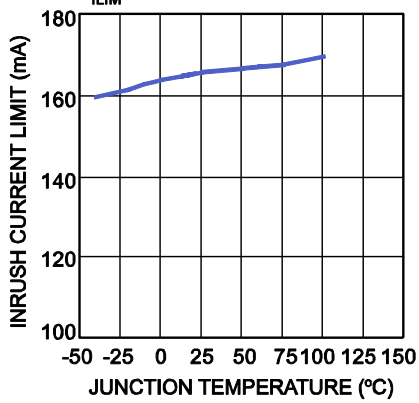


PD Inrush Current Limit vs. Setting Resister

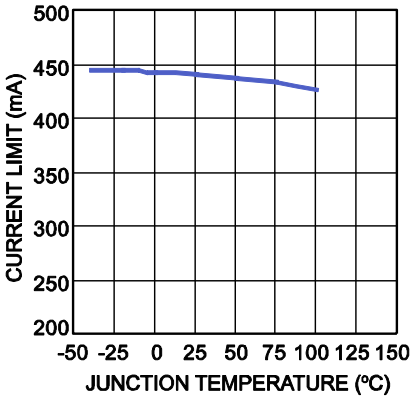


PD Inrush Current Limit vs. Temperature

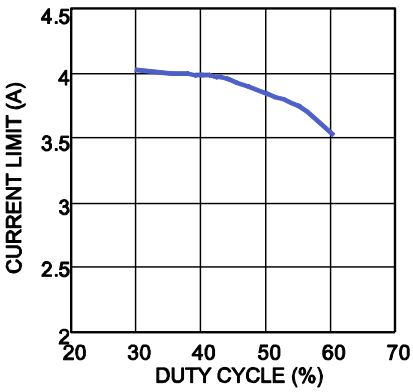
R_{ILIM}=178kΩ



PD Current Limit vs. Temperature

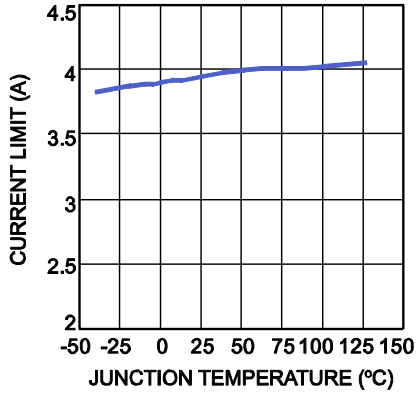


DC Converter Current Limit vs. Duty Cycle



DC Converter Current Limit vs. Temperature

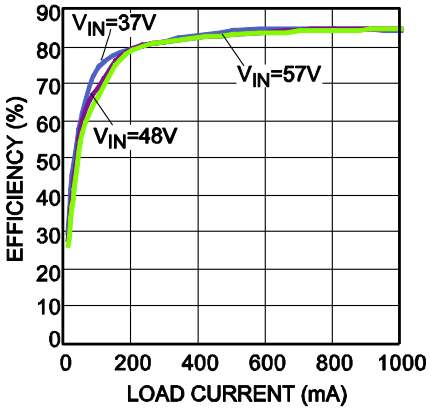
Duty Cycle =35%



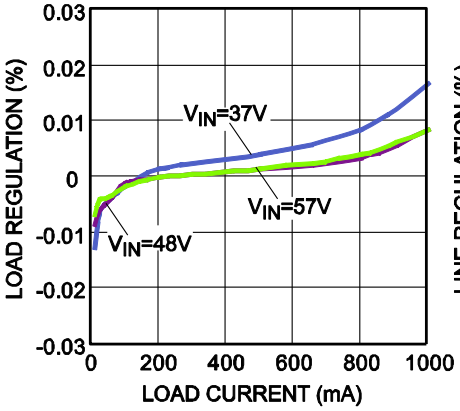
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

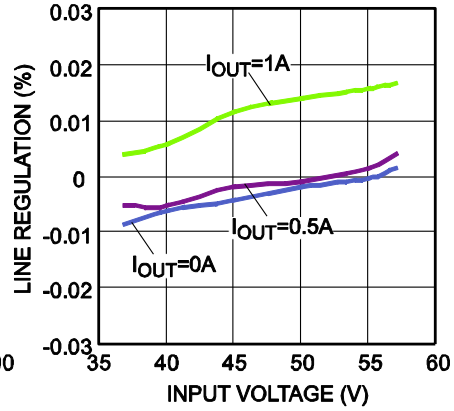
Efficiency vs. Load Current



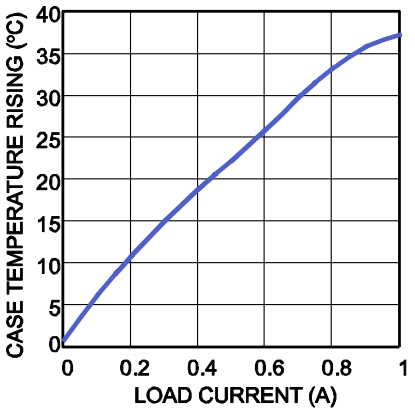
Load Regulation



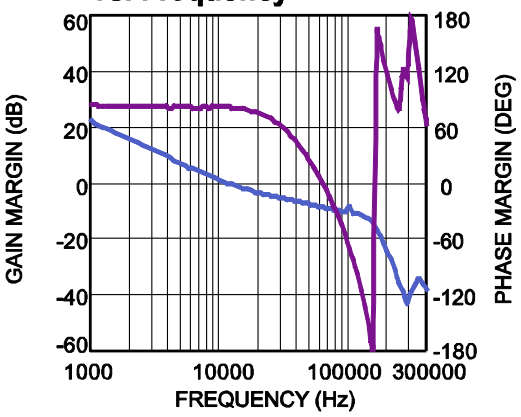
Line Regulation



Case Temperature Rising vs. Load Current



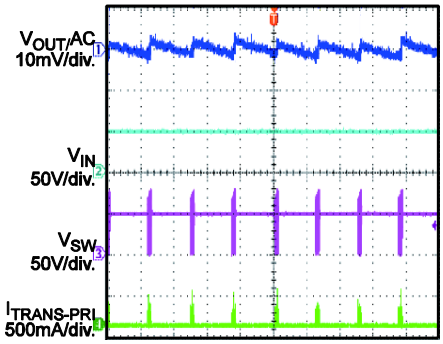
Magnitude and Phase vs. Frequency



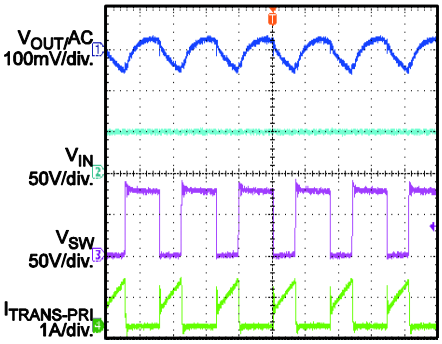
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

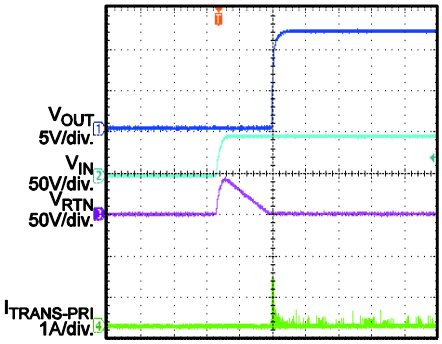
Steady State
I_{OUT} = 0A



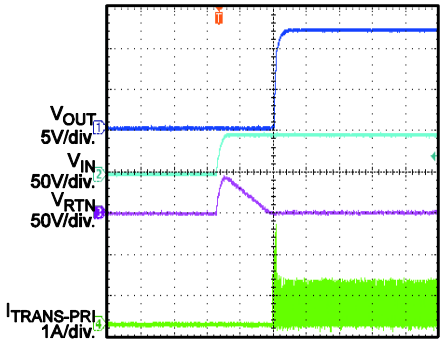
Steady State
I_{OUT} = 1A



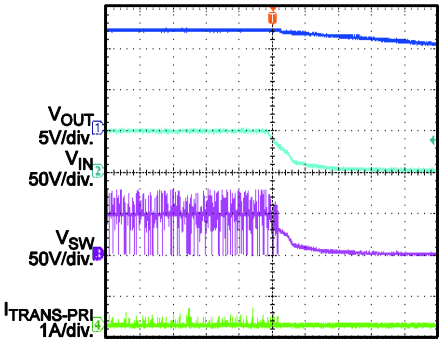
V_{IN} Startup
I_{OUT} = 0A



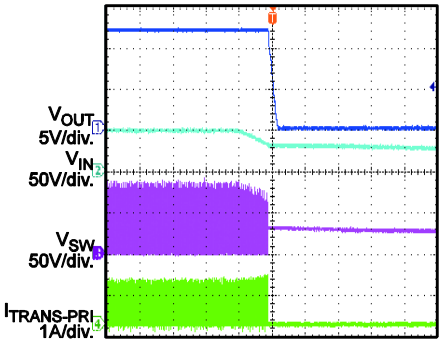
V_{IN} Startup
I_{OUT} = 1A



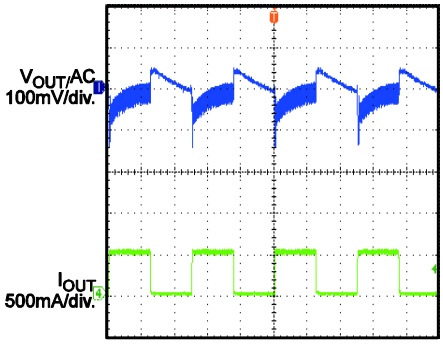
V_{IN} Shutdown
I_{OUT} = 0A



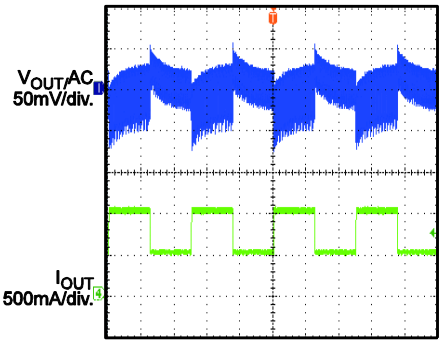
V_{IN} Shutdown
I_{OUT} = 1A



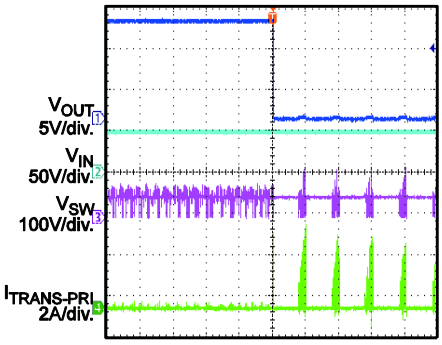
Load Transient
I_{OUT} = 0A->0.5A,
I_{RAMP} = 800mA/µs



Load Transient
I_{OUT} = 0.5A->1A,
I_{RAMP} = 800mA/µs



SCP Entry
I_{OUT} = 0A to short

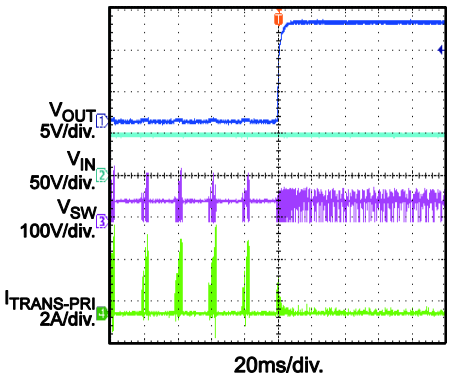


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

SCP Recovery

I_{OUT} = short to 0A



FUNCTION DIAGRAM

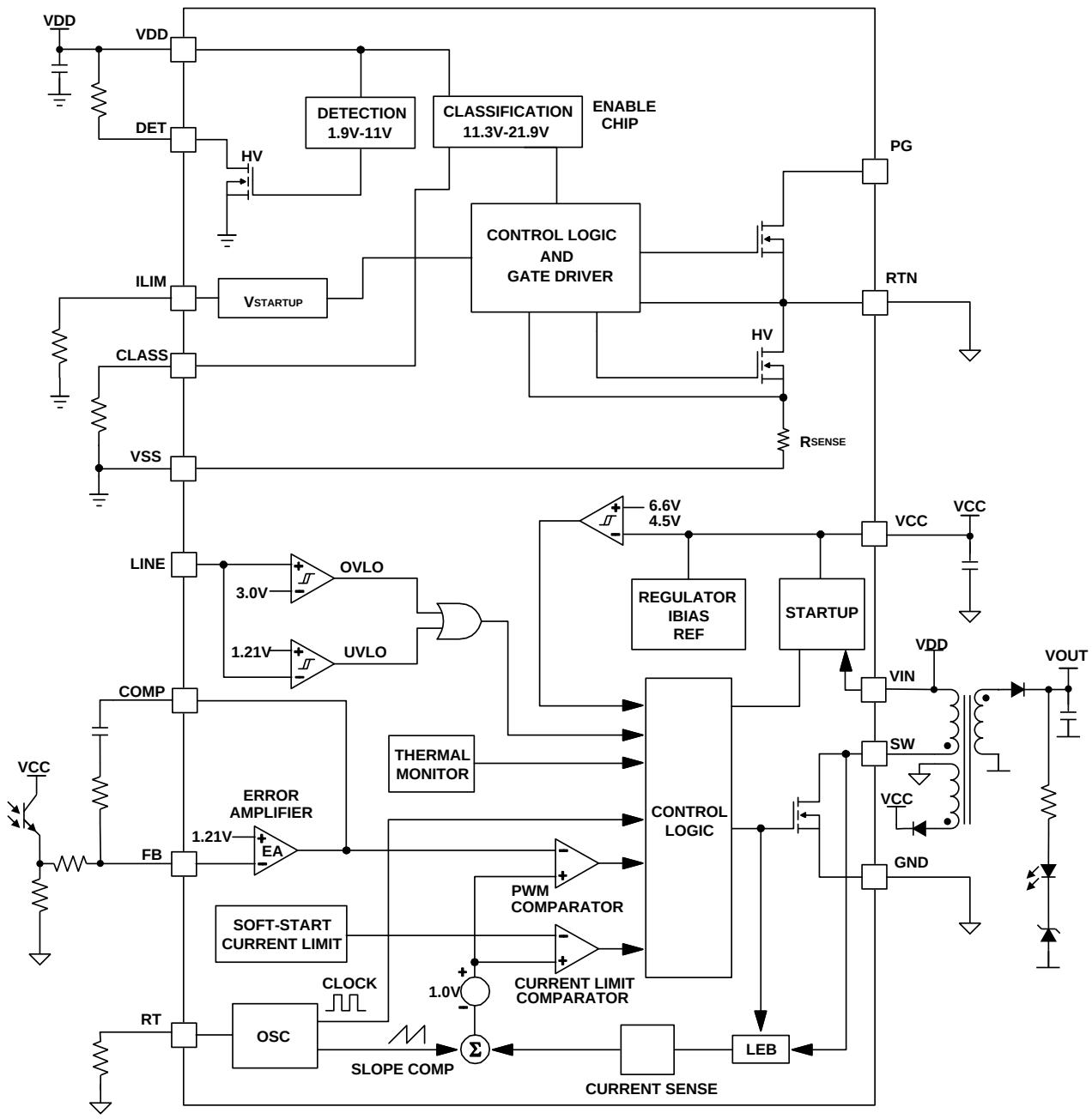


Figure 1: Functional Block Diagram

OPERATION

The MP8004 is one integrated solution of IEEE 802.3af power over Ethernet (PoE) powered device (PD) for up to 13W power application. It includes a PD interface and a flyback converter with internal power switch. Figure 1 shows the function diagram.

Detection

The PD interface operates in the manner described here and in the IEEE 802.3af Specifications. This device (along with the power sourcing element (PSE)) operates as a safety device to supply voltages only when the power sourcing element recognizes a unique, tightly specified resistance at the end of an unknown length of Ethernet cable.

A 26.1kΩ resistance is presented as a load to the PSE in Detection Mode, when the PSE applies two “safe” voltages of less than 10.1V while measuring the change in current drawn in order to determine the load resistance. If the PSE “sees” the correct load, then it may either further increase the applied voltage to enter the “classification” range of operation or switch on the nominal 48V power to the load.

Classification

The classification mode can further specify to the PSE the expected load range of the device under power so that the PSE can intelligently distribute power to as many loads as possible (within its maximum current capabilities). If a classification resistance is not present, the PD load is assumed to be the maximum of approximately 13 Watts. The PSE classification mode is active between 14.5V and 20.5V.

PD Startup

The main power switch will pass a limited current to charge the downstream DC-DC converter’s input capacitor to above 40V. The charging will continue until the controlled current drops below an externally programmed limiting level, depending upon the Rilim current setting resistor. The main pass power switch is internally thermally protected by reducing the output current using a foldback technique. The required power dissipation of the IC drops from the allowed peak value of I_{INRUSH} x 57V to 0.17W ((420mA)^2 x R_{ON}) during the normal operation at turn-on. The minimum allowed capacitance of 5µF will charge in 1.6ms if inrush current is limited at 150mA. A larger capacitor will take a proportionally longer time to charge due to the constant current charging method. If a capacitor is too large that will overheat the part and force it into thermal shutdown. The IC will reattempt charging for a number of cycles but ultimately will be shut down until the input voltage from the PSE is recycled. This is the way the IC protects itself under overload and/or shorted conditions.

DCDC Converter Startup

After PD pass switch turns on, power between Vin and GND is applied, the capacitor at the V_{CC} pin is charged through the VIN pin. When the voltage at the V_{CC} pin crosses 5.85V without fault, the controller is enabled. The V_{CC} pin is then disconnected from the VIN pin and V_{CC} voltage is discharged via the operating current. When V_{CC} drops to 4.5V, the V_{CC} pin is reconnected to the VIN pin and V_{CC} will be recharged. The voltage at the V_{CC} pin repeats this ramp cycle between 4.5V and 5.85V. It is also recommended that the capacitor at V_{CC} pin is no less than 1uF to achieve stable operation. The V_{CC} pin can be powered with a voltage higher than 4.5V from an auxiliary winding to reduce the power dissipated in the internal start-up circuit.

To avoid DCDC converter starts before pass switch is fully turned on, one LINE pin is addressed to enable/disable the startup of DCDC converter. Control LINE pin through PG signal can avoid this DCDC startup inrush current during PD’s charging period.

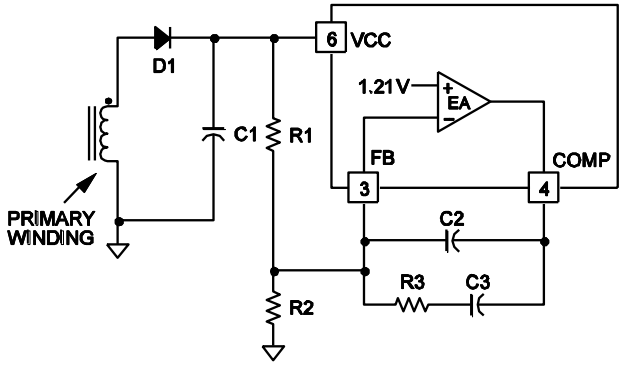
Under-Voltage and Over-Voltage Detection

The DC converter includes a line monitor circuit. Two external resistors form a voltage divider from the Vin voltage to GND pin; its tap connects to the LINE pin. The controller is

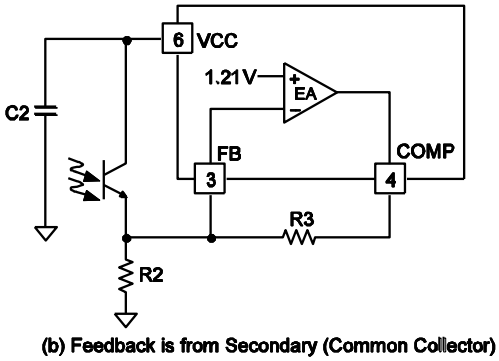
operational when the voltage at the LINE pin is between 1.21V and 3V. When the voltage at the LINE pin goes out of this operating range, the controller is disabled and goes into standby mode. The LINE pin can also be used as a remote enable. Grounding the LINE pin will disable the controller.

Error Amplifier

The converter section includes an error amplifier with its non-inverting input connected to internal 1.21V reference voltage. The regulated voltage is fed back through a resistor network or an optocoupler to the FB pin. Figure 2 shows some common error amplifier configurations.



(a) Using Primary winding to provide feedback



(b) Feedback is from Secondary (Common Collector)

Figure 2—Error Amplifier Configurations

Synchronize Programmable Oscillator

The converter oscillating frequency is set by an external resistor from the RT pin to ground. The value of RT can be estimated from:

$$RT = 10k\Omega \times \frac{550KHz}{f_S}$$

The DCDC converter can be synchronized to an external clock pulse. The frequency of the clock pulse must be higher than the internal oscillator frequency. The clock pulse width should be within 50ns to 150ns. The external clock can be coupled to the RT pin with a 100pF capacitor and a peak level greater than 3.5V

Duty Cycle Limiting with Line Feed Forward

The DCDC converter has a D_{MAX} (maximum duty cycle) limit at 67.5% when the LINE pin voltage is equal to 1.3V. As V_{LINE} increases, D_{MAX} reduces. Maximum duty cycle can be estimated by:

$$D_{MAX} = \left[\frac{2.7V}{2.7V + V_{LINE}}\right] \times 100\%$$

The max duty cycle decreases a little while F_{SW} increases. And in order to have enough margin for transient regulation some duty margin is necessary in application.

Limiting the duty cycle at high line voltage protects against magnetic saturation and minimizes the output sensitivity to line transients.

Converter Auto-Restart

When V_{CC} is biased from an auxiliary winding and an open loop condition occurs, the voltage at the V_{CC} pin increases to 6.6V. When V_{CC} crosses the threshold voltage, the auto-restart circuit turns off the power switch and puts the converter in standby mode. When V_{CC} drops to 4.5V, the startup switch turns on to charge V_{CC} up again. When V_{CC} crosses 5.85V, the switch turns off and the standby current discharges V_{CC} back to 4.5V. After repeating the ramp cycles between the two threshold voltages 15 times, the auto-restart circuit is disabled and the converter begins soft-start again.

Converter over Current Protection

The DCDC converter has cycle-by-cycle over current limit when the internal switch current peak value exceeds the set current limit threshold. Meanwhile, the output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 33% of the FB reference. Once a UV is triggered, the DCDC converter enters hiccup mode to periodically restart the part (the DCDC converter turns off

the switch until Vcc repeats the ramp cycles between 4.5V to 5.85V for 15 times). Thisprotection mode is especially useful when the output is dead-short to ground. The average short circuit input current is greatly reduced to alleviate the thermal issue and protect the regulator. The converter exits the hiccup mode once the over current condition is removed.

Thermal Shutdown

The device has separated thermal monitor circuits for pass through device and switching device. DC converter thermal protection won't affect PD interface and can recover automatically, but PD temperature protection will latch off after a number of restarts.

APPLICATION INFORMATION

COMPONENT SELECTION

Detection Resistor

The PSE applies two “safe” voltages between 2.7V to 10.1V while measuring the current in order to determine the load resistance. The resistance is calculated as a $\Delta V/\Delta I$, with an acceptable range of 23.7kΩ to 26.3kΩ. Use a typical value of 26.1kΩ detection resistor to compensate MP8004 VDD leakage.

Classification Resistor

In order to distribute power to as many loads as possible from PSE, the classification process applies a voltage between 14.5V and 20.5V to the input of the PD, which in turn draws a fixed current set by R(CLASS). An 802.3af PSE measures the PD current to determine which of the five available classes that the PD is signaling. Blew table is the Classification resistance and the PSE output power.

Table 1: CLASSIFICATION - IEEE 802.3af Values

CLASS	PD POWER (W)	RCLASS (Ω)	Class Current (mA)	NOTE
0	0.44 – 12.95	4420	0 - 4	Default class
1	0.44 – 3.84	953	9-12	
2	3.84 – 6.49	549	17 - 20	
3	6.49 – 12.95	357	26 - 30	
4	-	255	36 - 44	Reserved

Setting PD Inrush Current Limit

In order to limit the DCDC input capacitor charging current after PD`s pass switch turns on. There is a resister (R_{LIMIT}) to set the inrush current. The resister can be referred to the TPC curve and use a typical value of 178kΩ to get 150mA inrush current limit.

Switching DC-DC Frequency

The frequency (f_S), has big effects on the selection of the transformer (T1), the output cap, (C3), and the input cap, (C2). The higher the frequency, the smaller the sizes for T1, C3, and C2. However, a higher frequency also leads to higher AC power losses in the power switch, control circuitry, transformer, and in the external interconnection. The general rule states that lower the output power, higher the optimum switching frequency. For general application 200kHz to 300kHz frequency is recommended.

Fundamental Equations

The transformer turns ratio N is defined as:

$$N = \frac{N_P}{N_S}$$

Where N_P and N_S are the number of turns of the primary and secondary side windings, respectively.

The output voltage V_O is estimated to be:

$$V_O = \frac{D}{1-D} \times \frac{V_{IN}}{N}$$

Where D is the duty cycle.

The steady-state drain to source voltage of the primary power switch when it is off is estimated as:

$$V_{DS} = V_{IN} + N \times V_O$$

The steady-state reverse voltage of the Schottky diode D2 is estimated as:

$$V_{D1} = V_O + \frac{V_{IN}}{N}$$

The output current is calculated as:

$$I_O = I_D \times (1-D)$$

Where I_D is the average current through Schottky diode when it is conducting.

The input current is calculated as:

$$I_{IN} = I_S \times D$$

Where I_S is the average current through the primary power switch when it is conducting.

Transformer (Coupled Inductor) Design

1. Transformer Turns Ratio

The transformer turns ratio determines the duty cycle range, selection of the rectifier (D2), primary side peak current, primary snubber loss, and the current as well as voltage stresses on the power switch(S). It also has effects on the selection of C2 and C3. A higher transformer turns ratio (N) means the following:

- Higher Duty Cycle
- Higher voltage stress on S (V_{DS}), but lower voltage stress on D2 (V_{D2}).

- Lower primary side RMS current ($I_{S(RMS)}$), but higher secondary side RMS current ($I_{D2(RMS)}$).
- Use of a smaller input capacitor but bigger output capacitor.
- Lower primary side peak current ($I_{S(PEAK)}$) and lower primary snubber loss.
- Lower main switch (S) turn-on loss

For a 12V power supply design, with V_{IN}=37V~57V, below table shows the voltage stresses of the power switch (S) and the rectifier (D2).

Table 2—Main Switch (S) and Rectifier (D2) Voltage Stress vs. Transformer Turns Ratio

N	D_{MAX}	V_{DS} (V)	V_{DS}/0.9 (V)	V_{D2} (V)	V_{D2}/0.9 (V)
1	0.24	86	96	110	123
2	0.39	101	113	65	72
3	0.49	116	129	50	55
4	0.56	131	146	42	47
5	0.62	146	163	37	42

Note:
The voltage spike due to the leakage inductance of the transformer and device's voltage rating/derating factors were considered. See "Voltage Stress of the Internal Power Switch & External Schottky Diode" and snubber design for more information.

2. Ripple Factor of the Magnetizing Current
The conduction loss in S, D2, the transformer, the snubber, and in the ESR of the input/output capacitors will increase as the ripple of the magnetizing current increases. The ripple factor (K_r) is defined as the ratio of the peak-to-peak ripple current vs. the average current as shown in Figure 3.

$$K_r = \frac{\Delta I_M}{\overline{I_M}}$$

Where I_M can be derived either from input or output current;

$$\overline{I_M} = \frac{I_{IN}}{D} = \frac{I_O}{N \times (1-D)}$$

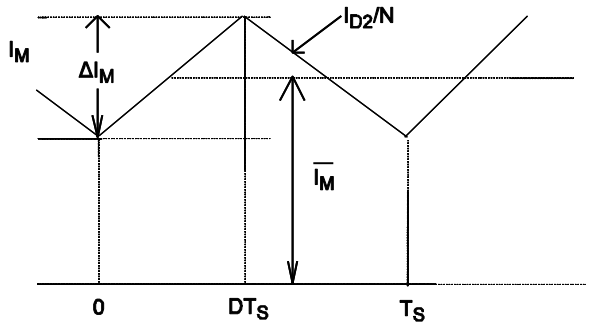


Figure 3—Magnetic Current of Flyback Transformer (Reflected to Primary Side)

The input/output ripple voltage will also increase with a high ripple factor, which makes the filter bigger and more expensive. On the other hand, it can help to minimize the turn-on loss of S and reverse-recovery loss due to D2. With nominal input voltage, K_r can be selected at 60%~120% for most DC-DC converters.

The primary side (or magnetizing) inductance can be determined by:

$$L_F = \frac{V_{IN} \times D \times T_S}{K_r \times \overline{I_M}}$$

3. Core Selection
Pick a core based on experience or through a catalog (Refer to http://www.ferroxcube.com).

Select an ER, EQ, PQ, or RM core to minimize the transformer's leakage inductance.

4. Winding Selection
Solid wire, Litz wire, PCB winding, Flex PCB winding or any combination thereof can be used as transformer winding. For low current applications, solid wire is the most cost effective choice. Consider using several wires in parallel and interleaving the winding structure for better performance of the transformer.

The number of primary turns can be determined by:

$$N_P = \frac{L_F \times I_P}{B_{MAX} \times A_E}$$

Where B_{MAX} is the allowed maximum flux density (usually below 300mT) and A_E is the effective area of the core.

The air gap can be estimated by:

$$Gap = \frac{\mu_0 \times N^2 \times A_E}{L_F}$$

5. Right Half Plane Zero

A Flyback converter operating in continuous mode has a right half plane (RHP) zero. In the frequency domain, this RHP zero adds not only a phase lag to the control characteristics but also increases the gain of the circuit. Typical rule of thumb states that the highest usable loop crossover frequency is limited to one third the value of the RHP zero. The expression for the location of the RHP zero in a continuous mode flyback is given by:

$$f_{RHPZ} = R_{LOAD} \times \frac{(1-D)^2}{2\pi \times L_F \times D} \times N^2$$

Where R_{LOAD} is the load resistance, L_F is the magnetizing inductance on transformer primary side, and N is the transformer's turn ratio.

Reducing the primary inductance increases the RHP zero frequency which results in higher crossover frequency.

Duty Cycle Range

The duty cycle range is determined once N is selected. In general, the optimum operating duty cycle should be smaller for high input/low output than low input/high output applications. Except for high output voltage or wide input range applications, the maximum D usually does not exceed 60%.

Voltage Stress of the Internal Power Switch & External Schottky Diode

For the internal power switch, the voltage stress is given by:

$$V_{DS} = V_{IN} + V_O \times N + V_P$$

Where V_P is a function of L_{LK} (leakage inductrance), f_S, R, C, C_{DS}, V_{IN}, I_O, etc. Please refer to Figure 4. The lower the L_{LK} and Io, the lower the Vp. Smaller R can reduce Vp, but power loss will increase. See Snubber Design for details.

Typically V_P can be selected as 20~40% of (V_{IN}+NV_O).

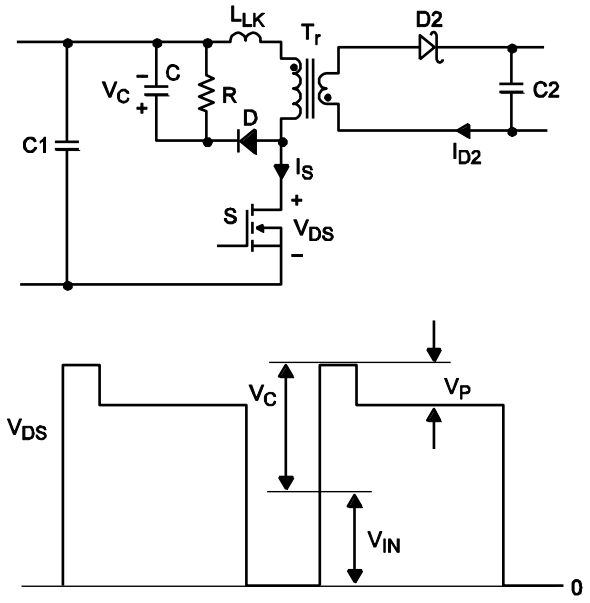


Figure 4—Key Operation Waveform

For the rectifier, D2, the voltage stress is given by:

$$V_{D2} = V_O + \frac{V_{IN}}{N} + V_{PD2}$$

Use of a R-C or R-C-D type snubber circuit for D2 is recommended.

V_{PD2} can be selected as 40~100% of (V_O+V_{IN}/N), thus:

$$V_{DS(MAX)} = K_s \times (V_{IN(MAX)} + NV_O)$$

Where K_S=1.2~1.4, and

$$V_{D2(MAX)} = K_{D2} \cdot (V_O + \frac{V_{IN(MAX)}}{N})$$

Where K_{D2}=1.4~2.

For example,

$$V_{IN(MAX)} = 57V, N = 4, K_S = 1.25, K_{D2} = 1.6, V_O = 12V$$
$$V_{DS} = 1.25 \times (57V + 4 \times 12V) = 131V$$
$$V_{D2} = 1.6 \times (12V + 57V \div 4) = 42V$$

So the power switch rating should be higher than 131V, and the rated voltage for the synchronous rectifier or Schottky diode should be higher than 42V.

Snubber Design (Passive)

Snubber for Power Switch

Figure 5 shows four different ways to clamp the voltage on the power device. RCD type of snubber circuit is widely used in many applications.

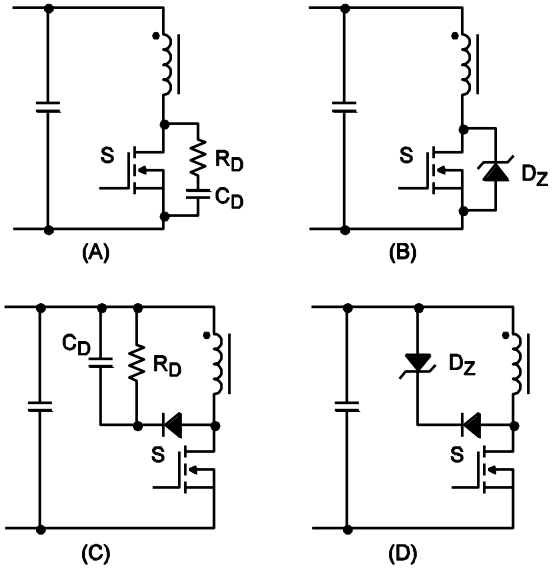


Figure 5—Snubber Designs

RCD Type of Snubber Design Procedure:

1. Setting V_P

Higher V_P means higher voltage stress on the power switch, but lower power loss. Usually, V_P can be set as 20%~40% of (V_{IN}+ NxV$_O$).

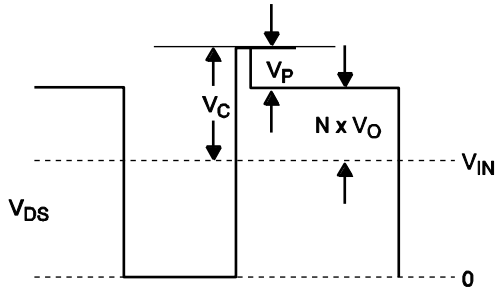


Figure 6—Voltage Waveform of Primary Power Switch Shown in Figure 5

2. Estimated RCD snubber loss is given by:

$$P_{RCD\_LOSS} = P_{LK} \times (1 + \frac{N \times V_O}{V_P})$$

Where:

$$P_{LK} = \frac{1}{2} L_{LK} \times I_P^2 \times f_C$$

P_{LK} is the energy stored in the leakage inductance (L_{LK}), which carries the peak current at the power switch turn-off.

3. Calculate values of the R_D and C_D of RCD snubber by:

$$R_D = \frac{V_P^2}{P_{RCD\_LOSS}}$$

$$R_D \times C_D >> \frac{1}{f_S}$$

Input Capacitor

The input capacitors (C2) are chosen based upon the AC voltage ripple on the input capacitors, RMS current ratings, and voltage rating of the input capacitors.

For a given AC ripple voltage, ΔV_{IN_PP}, C2 can be derived from:

$$C2 = \frac{I_{IN} \times (1-D) \times T_S}{\Delta V_{IN\_PP}}$$

ΔV_{IN_PP} may affect the C2 voltage rating and converter stability. C2 RMS current has to be considered:

$$I_{RMS\_C2} = I_{IN} \times \sqrt{\frac{(1-D)}{D}}$$

C2 has to have enough RMS current rating.

Output Filter

The simplest filter is an output capacitor (C3), whose capacitance is determined by the output ripple requirement.

The current waveform in the output capacitor is mostly in rectangular shape. The full load current is drawn from the capacitors during the primary switch on time. The worse case for the output ripple occurs under low line and full load conditions. The ripple voltage can be estimated by:

$$\Delta V_{O-PP-C} = I_O \times \frac{D}{C3 \times f_S}$$

ESR also needs to be specified for the output capacitors. This is due to the step change in D2 current results in a ripple voltage that is proportional to the ESR. Assuming that the D2 current waveform is in rectangular shape, the ESR requirement is then obtained by given the output ripple voltage.

$$\Delta V_{O-PP\_R_{ESR}} = \frac{I_O \times ESR}{(1-D)}$$

The total ripple voltage can be estimated by:

$$\Delta V_{O-PP} = \Delta V_{O-PP-C} + \Delta V_{O-PP\_ESR}$$

Control Design

Generally, telecom power supplies require the galvanic isolation between a relatively high input voltage and low output voltages. The most widely used devices to transfer signals across the isolation boundary are pulse transformers and optocouplers.

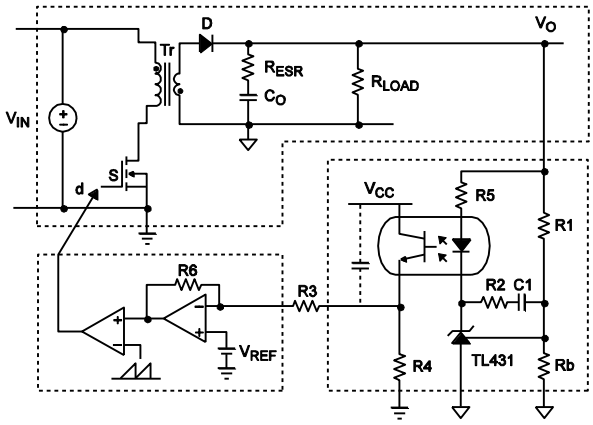


Figure 7—Simplified Circuit of Isolated Power Supply with Optocoupler Feedback

The MP8004 uses current mode control to achieve easy compensation and fast transient response. A type II compensation network which has two poles and one zero is needed to stabilize the system. The practical compensation parameters are provided in the EV8004-QW-00A datasheet.

PCB Layout Guide

High frequency switching regulators require very careful layout for stable operation and low noise. For fly-back topology layout:

1. Keep the input loop as short as possible between input cap, transformer, SW and GND plane for minimal noise and ringing.

2. Keep the output loop between rectifier diode, output cap and transformer as short as possible.

3. The clamp loop circuit between D5, C6, R9 and transformer should be as small as possible

4. The VCC capacitor must be placed close to the VCC pin for best decoupling.

5. The feedback trace should be far away from noise source such as SW.
6. Use single point connection between power GND and signal GND.

7. Thermal pad must be connected to GND plane for heat sink, RTN and GND pins can be connected closely through thermal pad.
Refer to figure 8 for flyback layout, which is referenced to schematic on page 1. For more detail information, refer to flyback EVB datasheet.

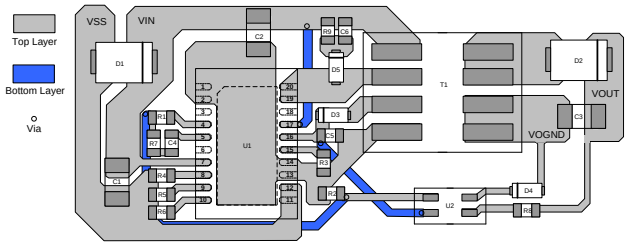


Figure 8—Layout Guide

Design Example

Below is a design example following the application guidelines for the following Specifications:

Table 3: Design Example

Vin	37V-57V (7)
Vout	12V
Iout	1A (7)
Fsw	275KHz

The typical application circuit for VOUT = 12V in Figure 9 shows the detailed application schematic, and it is the basis for the typical performance and circuit waveforms. For more detailed device applications, please refer to the related Evaluation Board Datasheets.

Notes:

7) The load power may not be able to support 12W because standard IEEE802.3af power supplies only 12.95W power input, considering the efficiency, the maximum load power should be limited at about 11W based on 12.95W PoE input. Input Voltage should be higher than 42V for startup, after startup, it can work down to 37V. Meets IEEE 802.3af Specifications.

TYPICAL APPLICATION CIRCUIT

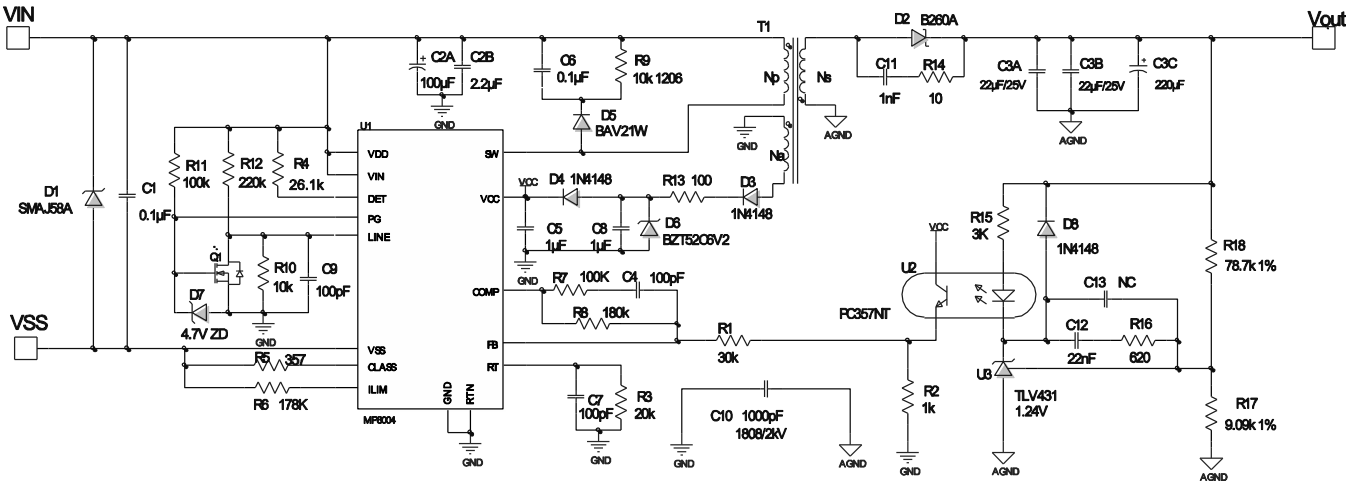
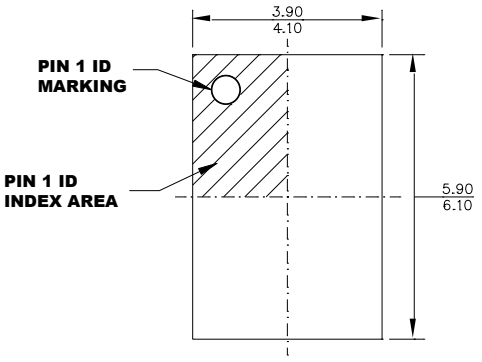


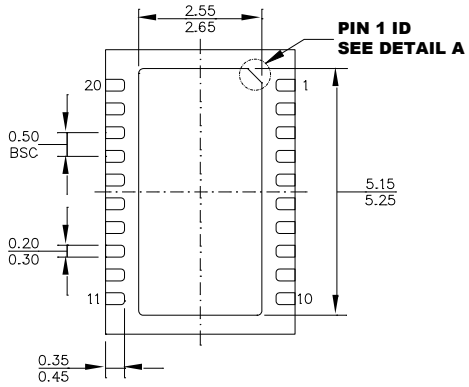
Figure 9: Typical Application Schematic, VIN=37-57V, VOUT=12V@1A [7].

PACKAGE INFORMATION

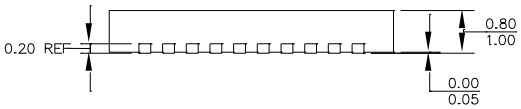
QFN-20 (4mmX6mm)



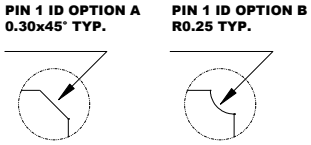
TOP VIEW



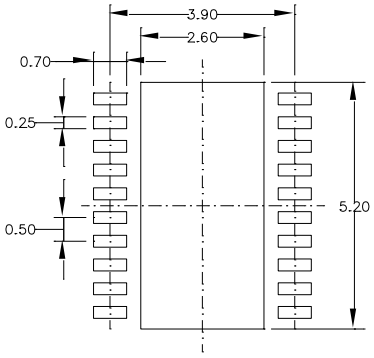
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220, VARIATION VJJE-1.
5) DRAWING IS NOT TO SCALE.