



# MP8009A

**Fully Integrated, 802.3af/at-Compliant,  
PoE PD Interface with Flyback/Forward  
Controller and 32ms Soft-Start Time**

## DESCRIPTION

The MP8009A is an integrated IEEE 802.3af/at-compliant, Power over Ethernet (PoE) powered device (PD) power supply converter. It includes a PD interface and a high-efficiency flyback/forward controller.

The PD interface has all the functions of IEEE 802.3af/at, including detection, single-event and dual-event classification, a 120mA inrush current limit ( $I_{LIMIT\_INRUSH}$ ), a 840mA operational current limit ( $I_{LIMIT}$ ), and a 100V hot-swap MOSFET.

The flyback/forward controller is specifically designed to be cost-effective. It is a space-saving isolated solution with primary-side regulation (PSR) for flyback applications, as well as high-efficiency secondary-side regulation (SSR) for active-clamp forward applications. It can also be used in SSR flyback topologies.

Full protection features include overload protection (OLP), short-circuit protection (SCP), over-voltage protection (OVP), and thermal shutdown. OLP, SCP, and OVP include hiccup mode.

The MP8009A can support a front-end solution for PoE PD applications with a minimal number of external components, and is available in a QFN-28 (4mmx5mm) package.

## FEATURES

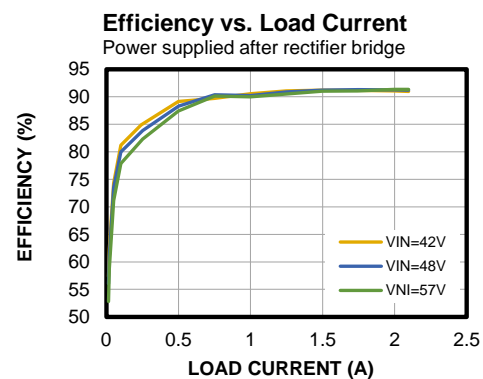
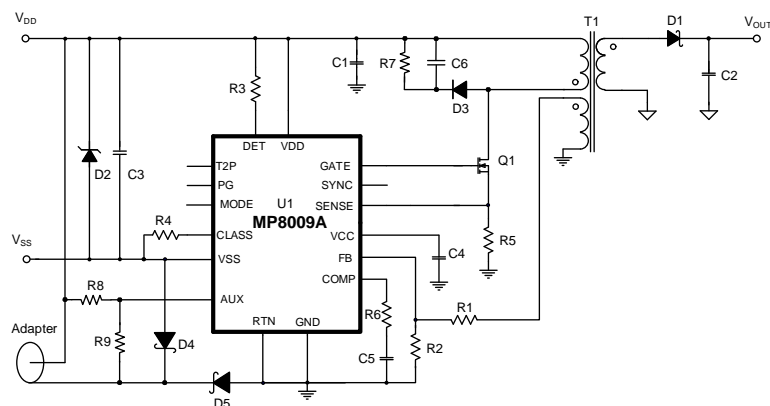
- IEEE 802.3af/at Compliant
- 100V, 0.48Ω Powered Device (PD) Integrated Pass MOSEFT
- 120mA PD Inrush Current ( $I_{LIMIT\_INRUSH}$ )
- 840mA PD Operational Current Limit ( $I_{LIMIT}$ )
- Supports >8.5V Auxiliary Adapter Supply
- Supports Flexible Topology Design:
  - Primary-Side Regulation (PSR) for Flyback Applications
  - Secondary-Side Regulation (SSR) for Flyback Applications
  - SSR for Active-Clamp Forward Applications
- 2A GATE Driver and 0.8A SYNC Driver
- 160mV Switching Current-Sense Limit
- 32ms Soft-Start Time ( $t_{SS}$ )
- 250kHz Fixed Switching Frequency ( $f_{SW}$ )
- Frequency Dithering for EMI Reduction
- Available in a QFN-28 (4mmx5mm) Package

## APPLICATIONS

- IEEE 802.3af/at-Compliant Devices
- Security Cameras
- Video Telephones
- Wireless Local Area Network (WLAN) Access Points
- Internet of Things (IoT) Devices

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## TYPICAL APPLICATION



## ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8009AGV	QFN-28 (4mmx5mm)	See Below	2

\* For Tape & Reel, add suffix -Z (e.g. MP8009AGV-Z).

## TOP MARKING

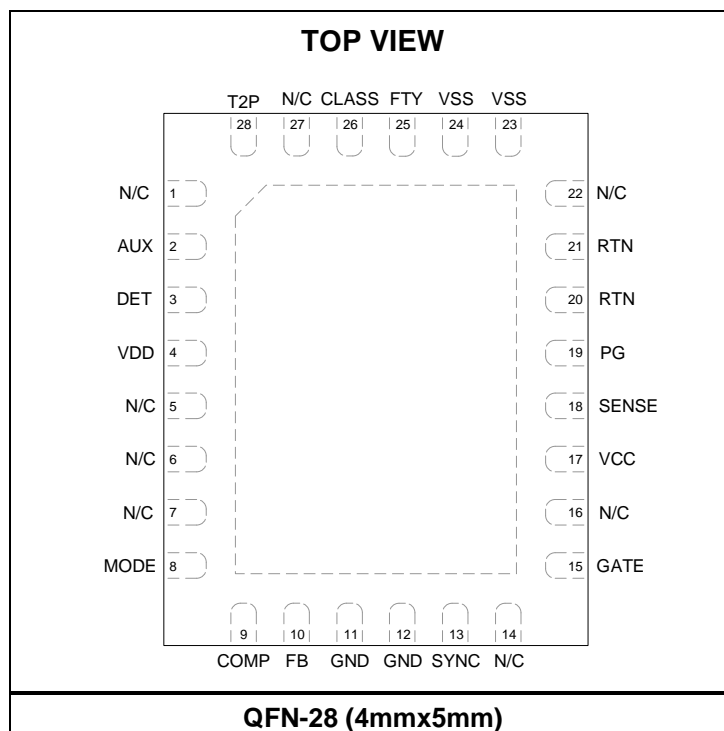
**MPSYWW**

**M8009A**

**LLLLLL**

MPS: MPS prefix  
Y: Year code  
WW: Week code  
M8009A: Part number  
LLLLLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

Pin #	Name	Description
1, 5, 6, 7, 14, 16, 22, 27	NC	<b>Not connected.</b> It is recommended to connect the NC pins to GND.
2	AUX	<b>Auxiliary power input detection.</b> The AUX pin is for auxiliary power applications. Pull AUX 2.3V below the VDD pin voltage ( $V_{DD}$ ) to turn the hot-swap MOSFET off and to disable the classification (CLASS) functions. This forces the T2P and PG pins to be active.
3	DET	<b>Detection.</b> Connect a 24.9k $\Omega$ resistor between the VDD and DET pins for Power over Ethernet (PoE) detection.
4	VDD	<b>Positive power supply terminal for PoE and the controller input power rail.</b>
8	MODE	<b>Primary-side regulation, secondary-side regulation, and dead time selection.</b> Float the MODE pin for primary-side regulation (PSR) applications. Connect the MODE and GND pins via a resistor for secondary-side regulation (SSR) applications. MODE also sets the dead time (DT) between the GATE and SYNC pins. See the Operation Mode Detection section on page 21 for more details.
9	COMP	<b>Loop compensation.</b> The COMP pin functions as the error amplifier (EA) output during PSR. COMP is pulled up to 5V internally via a 10k $\Omega$ resistor during SSR.
10	FB	<b>Output voltage feedback and over-voltage protection monitor.</b> Connect a resistor divider to the sense winding to regulate the output voltage ( $V_{OUT}$ ) during PSR. The internal EA is disabled during SSR. The FB pin detects the over-voltage protection (OVP) signal during both PSR and SSR. Connect the FB and GND pins if the OVP function is not used during SSR.
11, 12	GND	<b>Ground.</b>
13	SYNC	<b>Synchronous MOSFET gate driver.</b>
15	GATE	<b>Main MOSFET gate driver.</b>
17	VCC	<b>DC/DC internal circuit supply.</b> The VCC pin is powered by an internal low-dropout (LDO) regulator via the VDD voltage ( $V_{DD}$ ). Connect a capacitor ( $C_{VCC}$ ) between the VCC and GND pins to bypass the internal regulator. $C_{VCC}$ should be $\geq 1\mu F$ for flyback applications, and 4.7 $\mu F$ for forward applications. VCC can also be powered by an external power source to reduce internal LDO loss.
18	SENSE	<b>Current sense, PSR output voltage compensation, and frequency dithering setting.</b> The SENSE pin is the power current sense. It also sets the $V_{OUT}$ compensation and frequency dithering function via the resistors connected between the SENSE and GND pins ( $R_{REG}$ and $R_{SENSE}$ ). See the Output Voltage Compensation section on page 23 and the Frequency Dithering section on page 24 for more details.
19	PG	<b>PD supply power good indication.</b> The power good (PG) signal enables the DC/DC converter internally. PG is pulled up internally via an internal current source when the PD output is good. Float PG for most applications.
20, 21	RTN	<b>PD hot-swap MOSFET drain.</b> Connect the RTN and GND pins. Connect the exposed thermal pad to the RTN and GND pins to improve thermal dissipation.
23, 24	VSS	<b>PoE input power rail negative power supply terminal.</b>
25	FTY	<b>Factory use only.</b> Connect the VSS and FTY pins.
26	CLASS	<b>Classification.</b> Connect a resistor between the CLASS and VSS pins to configure the classification current ( $I_{CLASS}$ ).
28	T2P	<b>Type-2 power-sourcing equipment indication.</b> The T2P pin is an open-drain output. T2P is pulled down to VSS to indicate the presence of a wall adapter or Type-2 PSE.

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

### Pin Voltages with Respect to VSS

$V_{DD}$ , $V_{RTN}$ , $V_{DET}$ , $V_{T2P}$ , $V_{AUX}$ , $V_{GND}$ .....	-0.3V to +100V
$V_{CLASS}$ , $V_{FTY}$ .....	-0.3V to +6.5V

### Pin Voltages with Respect to GND <sup>(2)</sup>

$V_{DD}$ .....	-0.3V to +100V
$V_{CC}$ , $V_{GATE}$ , $V_{SYNC}$ .....	-0.3V to +18V
$V_{FB}$ .....	-0.5V to +5.5V <sup>(3)</sup>
$V_{MODE}$ , $V_{COMP}$ , $V_{SENSE}$ .....	-0.3V to +5.5V
$V_{PG}$ .....	-0.3V to +6.5V

### Pin Voltages with Respect to VDD

$V_{AUX}$ .....	-6.5V to +0.3V <sup>(4)</sup>
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### Pin Currents

T2P sink current ( $I_{T2P\_SINK}$ ) .....	10mA
PG sink current ( $I_{PG\_SINK}$ ) .....	0.5mA <sup>(5)</sup>
FB sink current ( $I_{FB\_SINK}$ ) .....	±2mA <sup>(3)</sup>
Continuous power dissipation ( $T_A = 25^\circ\text{C}$ )	
QFN-28 (4mmx5mm) .....	3.37W <sup>(6) (7)</sup>
Junction temperature .....	150°C
Lead temperature .....	260°C
Storage temperature .....	-55°C to +150°C

### Recommended Operating Conditions <sup>(8)</sup>

Supply voltage ( $V_{DD}$ ) .....	0V to 57V
$V_{CC}$ , $V_{GATE}$ , $V_{SYNC}$ .....	16V
Maximum $I_{T2P\_SINK}$ .....	5mA
Maximum $I_{PG\_SINK}$ .....	0.4mA <sup>(5)</sup>
Maximum $I_{FB\_SINK}$ .....	±1mA <sup>(3)</sup>
Operating junction temp ( $T_J$ ) ....	-40°C to +125°C

## Thermal Resistance

 $\theta_{JA}$      $\theta_{JC}$ 

QFN-28 (4mmx5mm)

EVL8009A-V-00A <sup>(7)</sup> ..... 37 ..... 2 ..... °C/W

JESD51-7 <sup>(9)</sup> ..... 40 ..... 9 ..... °C/W

### Notes:

- 1) Exceeding these ratings may damage the device.
- 2) Connect the GND and RTN pins.
- 3) FB is clamped internally via an internal circuit. The FB sink/source current should be limited. See the Output Voltage Setting section on page 28 for more details.
- 4) If the voltage between the VDD pin and the adapter ground is high, then ( $V_{AUX} - V_{DD}$ ) may exceed -6.5V. Under these conditions, the current should be limited via an external resistor. See the Wall Adapter Power Detection Circuit section on page 27 for more details.
- 5) If  $V_{PG}$  is pulled above 6.5V externally, then the pull-up current should be limited. See the Power Good (PG) Control section on page 21 for more details.
- 6) The maximum allowable power dissipation is a function of the maximum junction temperature  $T_J$  (MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) = ( $T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the device may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 7) Measured on the EVL8009A-V-00A (139mmx41mm), 2-layer PCB.
- 8) The device is not guaranteed to function outside of its operating conditions.
- 9) The value of  $\theta_{JA}$  given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS (PD INTERFACE)

$V_{DD}$ ,  $V_{CLASS}$ ,  $V_{DET}$ ,  $V_{T2P}$ , and  $V_{RTN}$  are referred to  $V_{SS}$ , all other pin voltages are referred to  $GND$ ,  $GND$  and  $RTN$  are shorted together,  $V_{DD} - V_{SS} = 48V$ ,  $V_{SS} = 0V$ ,  $R_{DET} = 24.9k\Omega$ ,  $R_{CLASS} = 28.7\Omega$ .  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(10)</sup>, typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Detection						
Detection on	V <sub>DET_ON</sub>	V <sub>DD</sub> rising		1.9		V
Detection off	V <sub>DET_OFF</sub>	V <sub>DD</sub> rising		11		V
DET leakage current	V <sub>DET_LKG</sub>	V <sub>DET</sub> = V <sub>DD</sub> = 57V, measure I <sub>DET</sub>		0.1	5	μA
Bias current		V <sub>DD</sub> = 10.1V, DET is floating, not in mark event, measure I <sub>SUPPLY</sub>			12	μA
Detection current	I <sub>DET</sub>	V <sub>DD</sub> = 2.5V, measure I <sub>SUPPLY</sub>	96	99	102	μA
		V <sub>DD</sub> = 10.1V, measure I <sub>SUPPLY</sub>	395	410	425	μA
Classification (CLASS)						
Classification stability timer				90		μs
CLASS voltage	V <sub>CLASS</sub>	13V < V <sub>DD</sub> < 21V, 1mA < I <sub>CLASS</sub> < 42mA	1.1	1.16	1.21	V
Classification current	I <sub>CLASS</sub>	13 ≤ V <sub>DD</sub> ≤ 21V, guaranteed by V <sub>CLASS</sub>				mA
		R <sub>CLASS</sub> = 578Ω, 13V ≤ V <sub>DD</sub> ≤ 21V	1.8	2	2.4	mA
		R <sub>CLASS</sub> = 110Ω, 13V ≤ V <sub>DD</sub> ≤ 21V	9.9	10.55	11.3	mA
		R <sub>CLASS</sub> = 62Ω, 13V ≤ V <sub>DD</sub> ≤ 21V	17.7	18.7	19.8	mA
		R <sub>CLASS</sub> = 41.2Ω, 13V ≤ V <sub>DD</sub> ≤ 21V	26.6	28.15	29.7	mA
		R <sub>CLASS</sub> = 28.7Ω, 13V ≤ V <sub>DD</sub> ≤ 21V	38.2	40.4	42.6	mA
Classification low threshold (CLASS regulator on)	V <sub>CLASS_ON</sub>	Class regulator turns on, V <sub>DD</sub> rising	11.8	12.5	13	V
Classification high threshold (CLASS regulator off)	V <sub>CLASS_OFF</sub>	Class regulator turns off, V <sub>DD</sub> rising	21	22	23	V
Classification low-side (LS) hysteresis	V <sub>CLASS_HYS_LS</sub>			0.8		V
Classification high-side (HS) hysteresis	V <sub>CLASS_HYS_HS</sub>			0.5		V
Mark event reset threshold	V <sub>MARK_RESET</sub>		4.5	5	5.5	V
Max mark event voltage	V <sub>MARK_MAX</sub>		11	11.5	12	V
Mark event current	I <sub>MARK</sub>		0.5	1.5	2	mA
Mark event resistance	R <sub>MARK</sub>	2-point measurement at 7V and 10V			12	kΩ
IC supply current during classification	I <sub>IN_CLASS</sub>	V <sub>DD</sub> = 17.5V, CLASS is floating		220	300	μA
Class leakage current	I <sub>CLASS_LKG</sub>	V <sub>CLASS</sub> = 0V, V <sub>DD</sub> = 57V			1	μA
Powered Device (PD) Under-Voltage Lockout (UVLO) Protection						
VDD UVLO rising threshold	V <sub>DD_UVLO_RISING</sub>		35	37.5	40	V
VDD UVLO falling threshold	V <sub>DD_UVLO_FALLING</sub>		29	31	33	V
VDD UVLO hysteresis	V <sub>DD_UVLO_HYS</sub>		4.9			V
IC operational input current	I <sub>IN</sub>			450		μA

## ELECTRICAL CHARACTERISTICS (PD INTERFACE) (continued)

$V_{DD}$ ,  $V_{CLASS}$ ,  $V_{DET}$ ,  $V_{T2P}$ , and  $V_{RTN}$  are referred to  $V_{SS}$ , all other pin voltages are referred to  $GND$ ,  $GND$  and  $RTN$  are shorted together,  $V_{DD} - V_{SS} = 48V$ ,  $V_{SS} = 0V$ ,  $R_{DET} = 24.9k\Omega$ ,  $R_{CLASS} = 28.7\Omega$ .  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(10)</sup>, typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
<b>Pass Device and Current Limit</b>						
RTN on resistance	$R_{DS(ON)_RTN}$	$I_{RTN} = 600mA$		0.48		$\Omega$
RTN leakage current	$I_{RTN\_LKG}$	$V_{DD} = V_{RTN} = 57V$		1	15	$\mu A$
Current limit	$I_{LIMIT}$	$V_{RTN} = 1V$	720	840	920	mA
Inrush current limit	$I_{LIMIT\_INRUSH}$	$V_{RTN} = 2V$		120		mA
Inrush current termination		$V_{RTN}$ falling		1.2		V
Inrush to operation mode delay	$t_{DELAY}$		80	100		ms
Current foldback threshold		$V_{RTN}$ rising		10		V
Foldback deglitch time		$V_{RTN}$ rising to $I_{INRUSH}$ foldback		1		ms
<b>Type-2 Power-Sourcing Equipment (PSE) Indication (T2P)</b>						
T2P output low voltage		$I_{T2P} = 2mA$ , with respect to $V_{SS}$		0.1	0.3	V
T2P output high leakage current		$V_{T2P} = 48V$			1	$\mu A$
<b>Auxiliary Power Input Detection (AUX)</b>						
AUX high threshold <sup>(11)</sup>		With respect to $V_{DD}$			-2.3	V
AUX low threshold <sup>(11)</sup>		With respect to $V_{DD}$	-0.6			V
AUX leakage current		$V_{DD} - V_{AUX} = 6V$			2	$\mu A$
VDD UVLO rising for adapter power		$V_{DD} - V_{AUX} = 3V$ , $V_{DD} - V_{SS}$ ramps up from low to high until the T2P/PG signal response		7.25	8.5	V
VDD UVLO falling for adapter power		$V_{DD} - V_{AUX} = 3V$ , $V_{DD} - V_{SS}$ ramps down from high to low until T2P/PG signal reset		5		V
<b>Power Good (PG)</b>						
PG output high voltage		PG is floating		5.5		V
Source current capability		PG is logic high, PG is pulled down to 0V		30		$\mu A$
PG pull-down resistance		PG is logic low, PG is pulled up to 1V		715		k $\Omega$
PG rising threshold for DC/DC switching	$V_{PG\_RISING}$	Starts switching	1.93	2	2.07	V
PG hysteresis for DC/DC switching	$V_{PG\_HYS}$	Stops switching		0.2		V
PG high voltage for DC/DC micropower	$V_{PG\_HIGH}$	Start internal logic			1	V
PG low voltage for DC/DC micropower	$V_{PG\_LOW}$	Stop internal logic	0.4			V
PG enable DC/DC delay	$t_{PG}$	PG on to GATE output		500		$\mu s$
<b>PD Thermal Shutdown</b>						
Thermal shutdown threshold <sup>(12)</sup>	$T_{SD\_PD}$			150		$^{\circ}C$
Thermal shutdown hysteresis <sup>(12)</sup>	$T_{HYS\_PD}$			20		$^{\circ}C$



## ELECTRICAL CHARACTERISTICS (CONTROLLER)

$V_{DD}$ ,  $V_{CLASS}$ ,  $V_{DET}$ ,  $V_{T2P}$ , and  $V_{RTN}$  are referred to  $V_{SS}$ , all other pin voltages are referred to  $GND$ ,  $GND$  and  $RTN$  are shorted together,  $V_{DD} - V_{SS} = 48V$ ,  $V_{SS} = 0V$ ,  $R_{DET} = 24.9k\Omega$ ,  $R_{CLASS} = 28.7\Omega$ .  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(10)</sup>, typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply and UVLO Protection						
VDD UVLO rising threshold	V <sub>DD_UVLO_RISING</sub>	V <sub>DD</sub> rising, start charging V <sub>CC</sub>	4.5	5.5	6.5	V
VDD UVLO falling threshold	V <sub>DD_UVLO_FALLING</sub>	V <sub>DD</sub> falling	3.8	4.8	5.8	V
VCC voltage	V <sub>CC</sub>	I <sub>LOAD</sub> = 0mA to 20mA		8.5		V
VCC dropout voltage	V <sub>CC_DROP</sub>	V <sub>DD</sub> = 8V, I <sub>VCC</sub> = 10mA		1.5		V
VCC UVLO rising threshold	V <sub>CC_UVLO_RISING</sub>	V <sub>DD</sub> > V <sub>DD_UVLO_RISING</sub> , V <sub>CC</sub> rising	5.4	5.7	6	V
VCC UVLO falling threshold	V <sub>CC_UVLO_FALLING</sub>	V <sub>DD</sub> > V <sub>DD_UVLO_RISING</sub> , V <sub>CC</sub> falling	5	5.3	5.6	V
Quiescent current	I <sub>Q</sub>	V <sub>FB</sub> = -0.1V; V <sub>SENSE</sub> = 100mV; V <sub>COMP</sub> = 0V; MODE, GATE, and SYNC are floating; I <sub>Q</sub> = I <sub>DD</sub> - I <sub>COMP</sub>		1250		μA
		MODE = 0V, V <sub>COMP</sub> = 0V, I <sub>Q</sub> = I <sub>DD</sub> - I <sub>COMP</sub> GATE and SYNC are floating		900		μA
Voltage Feedback (FB)						
Reference voltage	V <sub>REF</sub>	T <sub>J</sub> = 25°C	1.98	2	2.02	V
		T <sub>J</sub> = -40°C to +125°C	1.97	2	2.03	V
FB current	I <sub>FB</sub>	V <sub>FB</sub> = 2V		10	50	nA
FB OVP threshold	V <sub>OVP_FB</sub>		120	125	130	% of V <sub>REF</sub>
OVP hiccup off time				340		ms
Minimum diode conduction time for FB sample <sup>(13)</sup>	t <sub>SAMPLE</sub>			0.5	0.6	μs
Regulation compensation current into FB		V <sub>SENSE</sub> = 50mV, R <sub>SENSE_GND</sub> = 3.3kΩ <sup>(14)</sup>		2.7		μA
		V <sub>SENSE</sub> = 50mV, R <sub>SENSE_GND</sub> = 6.8kΩ <sup>(14)</sup>		5.4		μA
		V <sub>SENSE</sub> = 50mV, R <sub>SENSE_GND</sub> = 12.7kΩ <sup>(14)</sup>		10.8		μA
Error Amplifier (EA)						
EA transconductance	G <sub>EA</sub>	MODE is floating, V <sub>FB</sub> = V <sub>REF</sub> ± 50mV, V <sub>COMP</sub> = 1.5V		0.59		mA/V
Maximum EA source current	I <sub>EA_SINK_MAX</sub>	MODE is floating, V <sub>COMP</sub> = 1.5V, V <sub>FB</sub> = 1.9V		-110		μA
Maximum EA sink current	I <sub>EA_SOURCE_MAX</sub>	MODE is floating, V <sub>COMP</sub> = 1.5V, V <sub>FB</sub> = 2.1V		110		μA
COMP high voltage	V <sub>COMP</sub>	MODE is floating, V <sub>FB</sub> = 1.9V		4		V
		MODE = 0V, COMP is floating		5		V
COMP internal pull-up resistance		SSR mode		10		kΩ



## ELECTRICAL CHARACTERISTICS (CONTROLLER) (continued)

$V_{DD}$ ,  $V_{CLASS}$ ,  $V_{DET}$ ,  $V_{T2P}$ , and  $V_{RTN}$  are referred to  $V_{SS}$ , all other pin voltages are referred to  $GND$ ,  $GND$  and  $RTN$  are shorted together,  $V_{DD} - V_{SS} = 48V$ ,  $V_{SS} = 0V$ ,  $R_{DET} = 24.9k\Omega$ ,  $R_{CLASS} = 28.7\Omega$ .  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(10)</sup>, typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Soft Start (SS)						
Internal soft-start time	t <sub>SS</sub>	MODE is floating, test FB between 0V and 2V		32		ms
		MODE = 0V, test COMP between 1.5V and 3.5V		40		ms
Current Sense (CS)						
Maximum current limit	I <sub>LIMIT_MAX</sub>		140	160	180	mV
Minimum current limit	I <sub>LIMIT_MIN</sub>	In PSR mode	33	36	39	mV
Short-circuit protection (SCP) threshold			240	300	360	mV
Current leading-edge blanking time	t <sub>LEB</sub>			250		ns
Current-sense amplifier gain	G <sub>CS</sub>			11		V/V
SENSE input bias current		V <sub>SENSE</sub> = 160mV		10	50	nA
Pulse-Width Modulation (PWM) Switching						
Switching frequency	f <sub>SW</sub>		225	250	275	kHz
Minimum foldback frequency in PFM mode		In PSR mode, COMP = 0V		30		kHz
PSR/SSR, Dead Time (DT), Frequency Dithering, and V <sub>OUT</sub> Compensation Selection (MODE and SENSE)						
MODE pin detection current	I <sub>MODE</sub>		35	40	45	μA
SENSE pin detection current	I <sub>SENSE</sub>		90	100	110	μA
MODE pin and SENSE pin detection period	t <sub>MODE</sub> t <sub>SENSE</sub>			200		μs
MODE detection threshold <sup>(15)</sup>	V <sub>MODE</sub>	Voltage level 1 range			0.15	V
		Voltage level 2 range	0.25		0.4	V
		Voltage level 3 range	0.55		0.85	V
		Voltage level 4 range	1.1		1.5	V
		Voltage level 5 range	2.2			V
SENSE detection threshold <sup>(15)</sup>	V <sub>SENSE</sub>	Voltage level 1 range			0.15	V
		Voltage level 2 range	0.25		0.4	V
		Voltage level 3 range	0.55		0.85	V
		Voltage level 4 range	1.1		1.5	V
		Voltage level 5 range	2.2			V
GATE Driver Signal						
GATE driver impedance (source)	I <sub>GATE_SOURCE</sub>	I <sub>GATE</sub> = -20mA		2		Ω
GATE driver impedance (sink)	I <sub>GATE_SINK</sub>	I <sub>GATE</sub> = 20mA		1.7		Ω
GATE source current capability <sup>(12)</sup>		V <sub>CC</sub> = 8.5V, C <sub>GATE</sub> = 10nF, test gate rising speed		2		A
GATE sink current capability <sup>(12)</sup>		V <sub>CC</sub> = 8.5V, C <sub>GATE</sub> = 10nF, test gate falling speed		1.7		A

## ELECTRICAL CHARACTERISTICS (CONTROLLER) (continued)

$V_{DD}$ ,  $V_{CLASS}$ ,  $V_{DET}$ ,  $V_{T2P}$ , and  $V_{RTN}$  are referred to  $V_{SS}$ , all other pin voltages are referred to  $GND$ ,  $GND$  and  $RTN$  are shorted together,  $V_{DD} - V_{SS} = 48V$ ,  $V_{SS} = 0V$ ,  $R_{DET} = 24.9k\Omega$ ,  $R_{CLASS} = 28.7\Omega$ .  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$  <sup>(10)</sup>, typical values are tested at  $T_J = 25^{\circ}C$ , unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
GATE output high voltage	$V_{GATE\_HIGH}$		$V_{CC} - 0.05$			V
GATE output low voltage	$V_{GATE\_LOW}$				0.05	V
Minimum GATE on time	$t_{ON\_MIN\_GATE}$			250		ns
GATE maximum duty cycle	$D_{MAX}$			70		%
<b>SYNC Driver Signal</b>						
SYNC driver impedance (source)	$I_{SYNC}$	$I_{GATE} = -20mA$		5		$\Omega$
SYNC driver impedance (sink)	$I_{SYNC}$	$I_{GATE} = 20mA$		2		$\Omega$
SYNC source current capability <sup>(12)</sup>		$V_{CC} = 8.5V$ , $C_{SYNC} = 10nF$ , test SYNC rising speed		0.8		A
SYNC sink current capability <sup>(12)</sup>		$V_{CC} = 8.5V$ , $C_{SYNC} = 10nF$ , test SYNC falling speed		1.2		A
SYNC output high voltage	$V_{SYNC\_HIGH}$		$V_{CC} - 0.05$			V
SYNC output low voltage	$V_{SYNC\_LOW}$				0.05	V
<b>Protections</b>						
Overload protection (OLP) with hiccup mode on time <sup>(12)</sup>	$t_{ON\_OLP}$			4.8		ms
OLP with hiccup mode off time <sup>(12)</sup>	$t_{OFF\_OLP}$			340		ms
Thermal shutdown threshold <sup>(12)</sup>	$T_{SD}$			150		$^{\circ}C$
Thermal shutdown hysteresis <sup>(12)</sup>	$T_{HYS}$			20		$^{\circ}C$

### Notes:

10) Guaranteed by over-temperature correlation. Not tested in production.

11) If  $(V_{DD} - V_{AUX})$  exceeds 2.3V, then the adapter input is enabled. If  $(V_{DD} - V_{AUX})$  drops below 0.6V, then the PSE input is enabled.

12) Guaranteed by sample characterization. Not tested in production.

13) It is recommended that the output diode conduction time be  $>0.7\mu s$ .

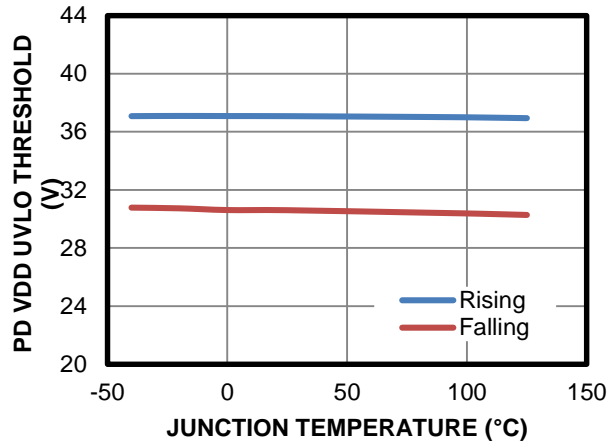
14)  $R_{SENSE\_GND}$  is the resistance from the SENSE pin to  $GND$ . It includes the current-sense resistor ( $R_{SENSE}$ ) connected between the MOSFET source and  $GND$ , as well as the resistor connected between the MOSFET source and the SENSE pin.

15) See Table 2 on page 22 and Table 3 on page 24 for more details on different voltage levels.

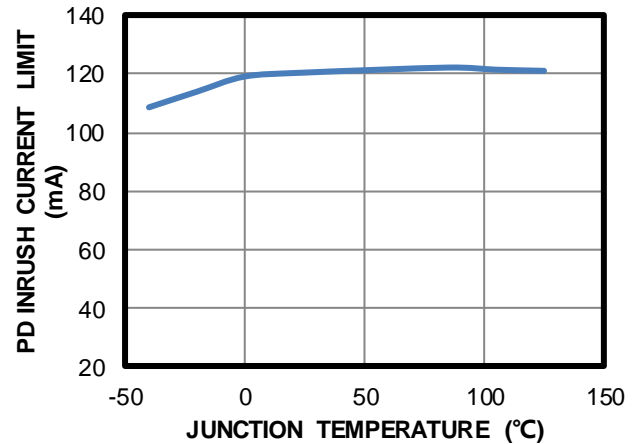
# TYPICAL CHARACTERISTICS

$V_{DD} - V_{SS} = 48V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

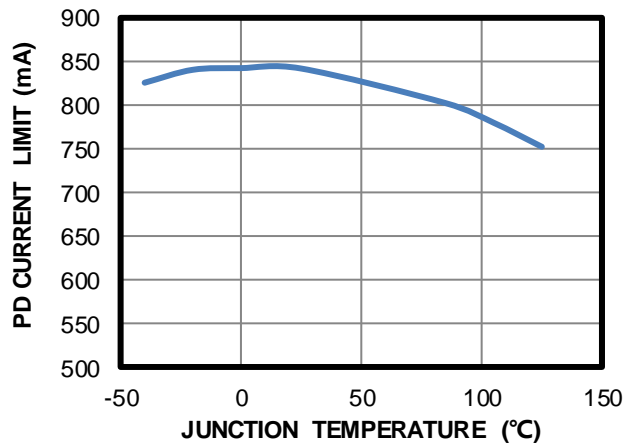
**PD VDD UVLO Threshold vs. Junction Temperature**



**PD Inrush Current Limit vs. Junction Temperature**

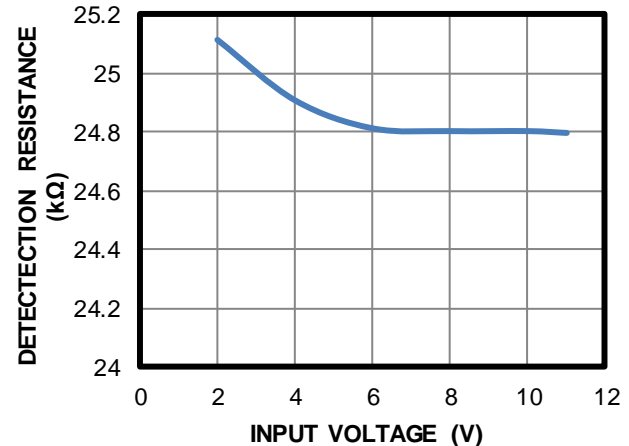


**PD Current Limit vs. Junction Temperature**

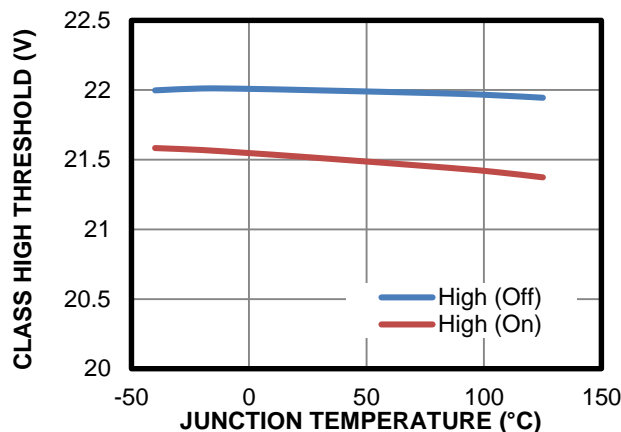


**Detection Resistance vs. Input Voltage**

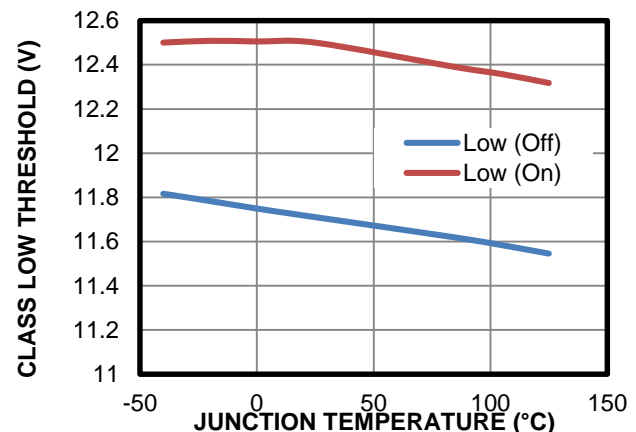
$R_{DET} = 24.9k\Omega$



**CLASS High Threshold vs. Junction Temperature**



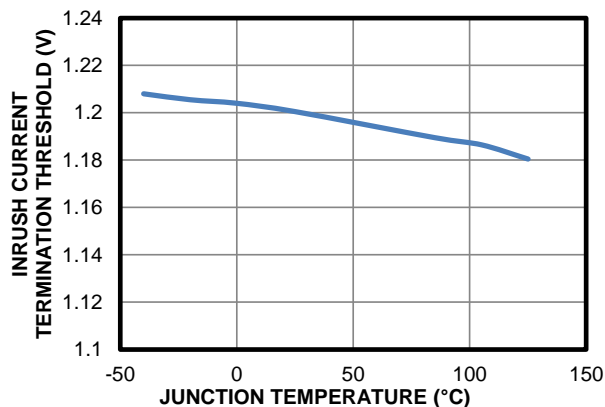
**CLASS Low Threshold vs. Junction Temperature**



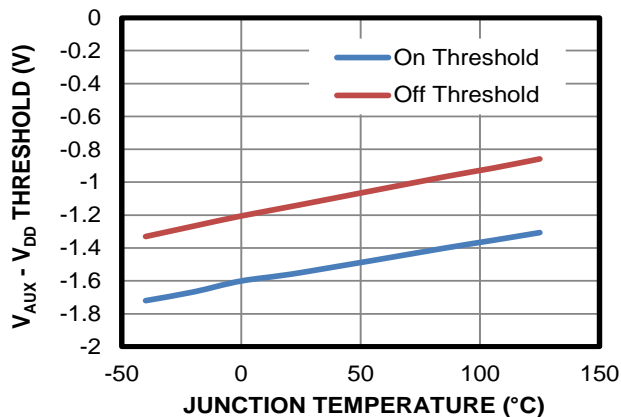
# TYPICAL CHARACTERISTICS (continued)

$V_{DD} - V_{SS} = 48V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

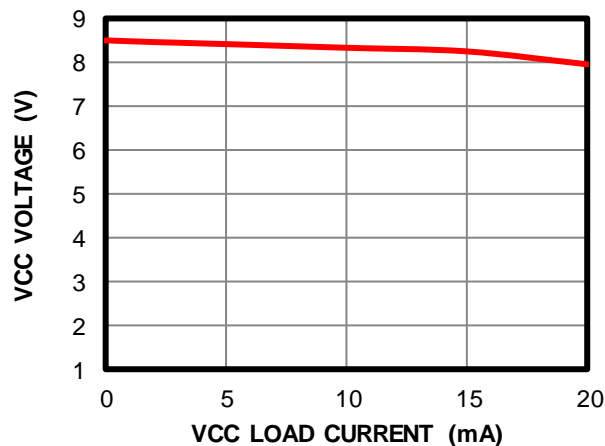
**Inrush Current Termination Threshold vs. Junction Temperature**



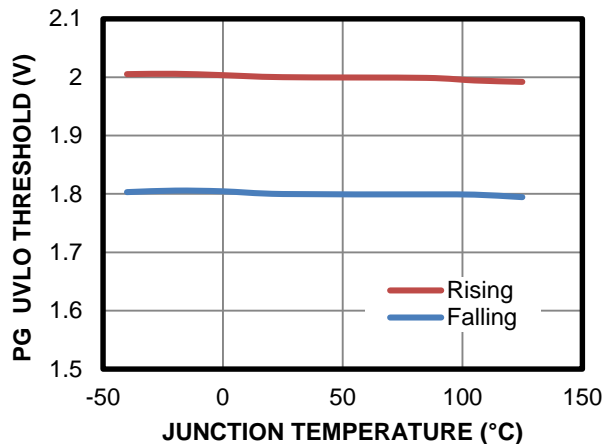
**$V_{AUX} - V_{DD}$  vs. Junction Temperature**



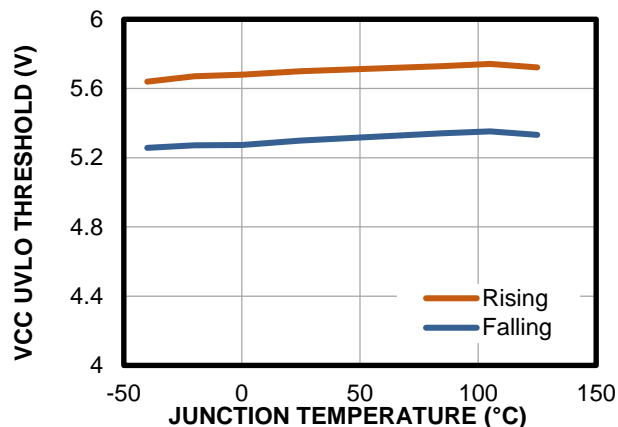
**VCC Load Regulation**



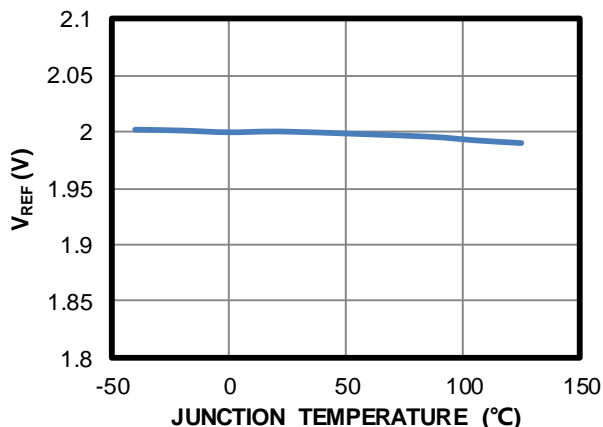
**PG UVLO Threshold vs. Junction Temperature**



**VCC UVLO Threshold vs. Junction Temperature**



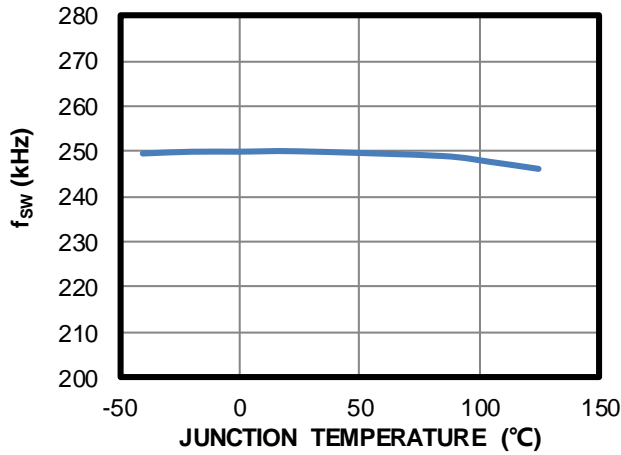
**Reference Voltage vs. Junction Temperature**



# TYPICAL CHARACTERISTICS (continued)

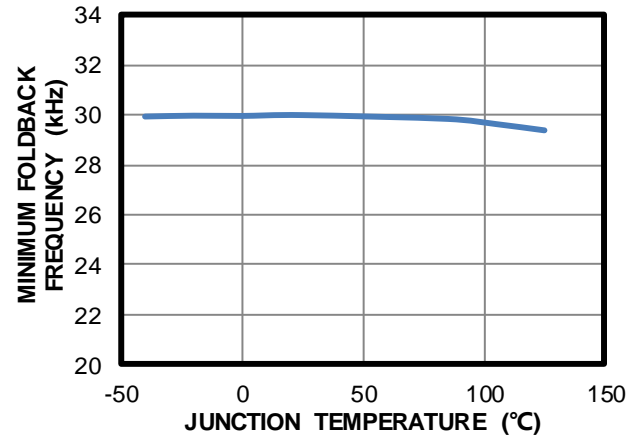
$V_{DD} - V_{SS} = 48V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

Switching Frequency vs. Junction Temperature

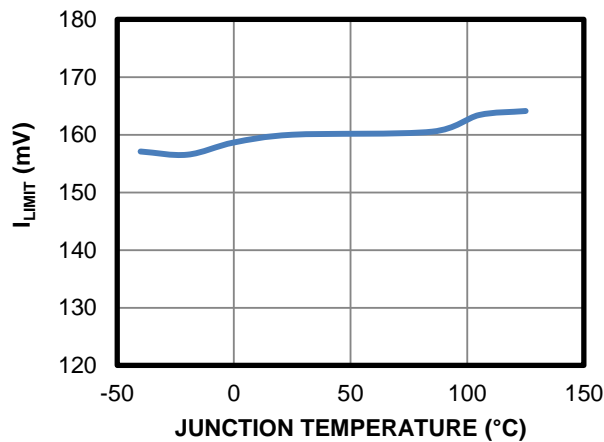


Minimum Foldback Frequency vs. Junction Temperature

PSR mode

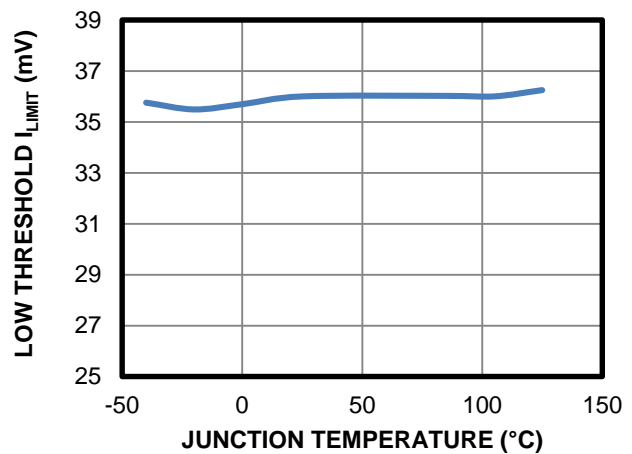


Current Limit vs. Junction Temperature

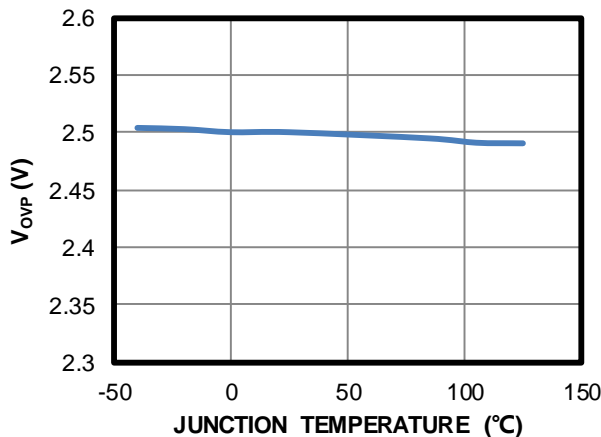


Low Threshold Current Limit vs. Junction Temperature

PSR mode

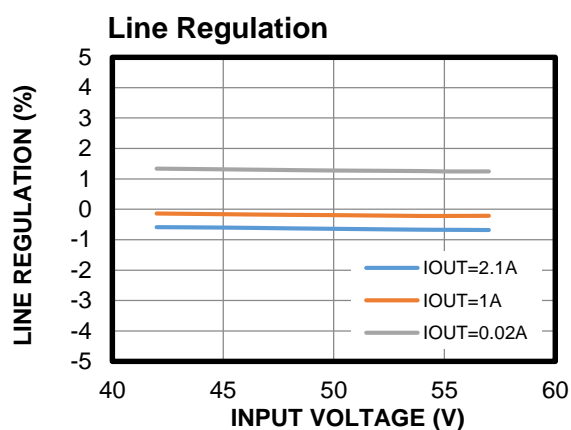
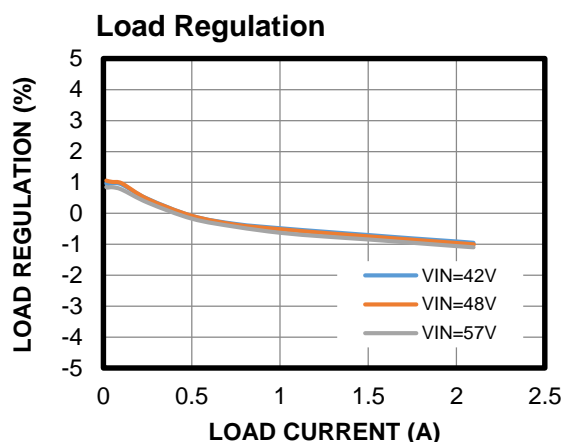
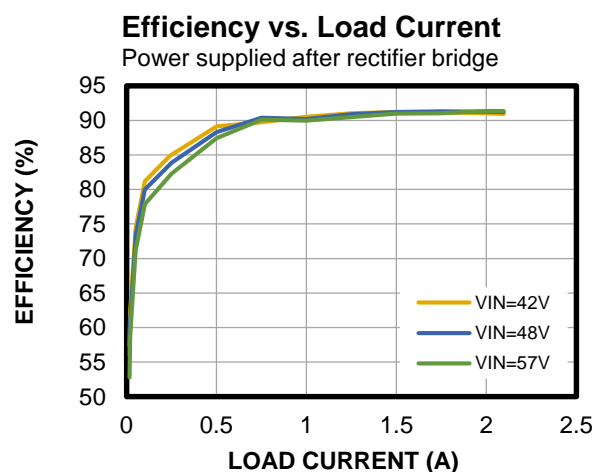


OVP Threshold vs. Junction Temperature



## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} - V_{SS} = 48V$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 2.1A$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

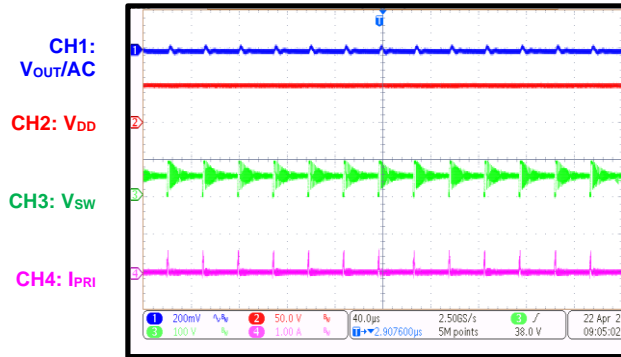


# TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{DD} - V_{SS} = 48V$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 2.1A$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

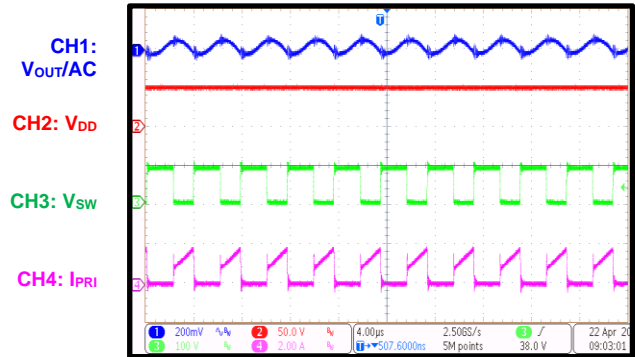
## Steady State

$I_{OUT} = 30mA$



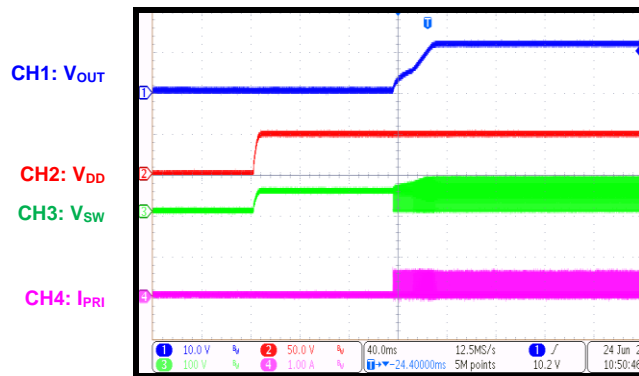
## Steady State

$I_{OUT} = 2.1A$



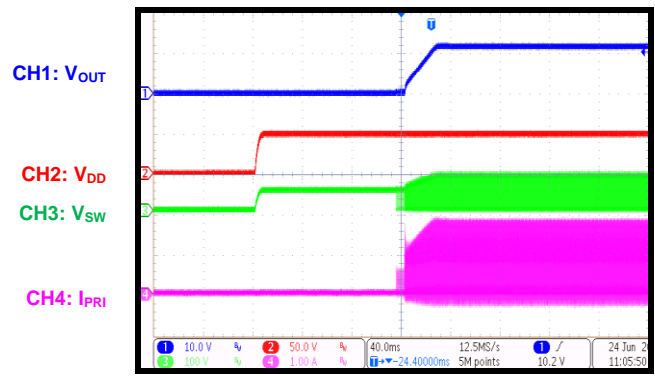
## Start-Up through VDD

$I_{OUT} = 30mA$



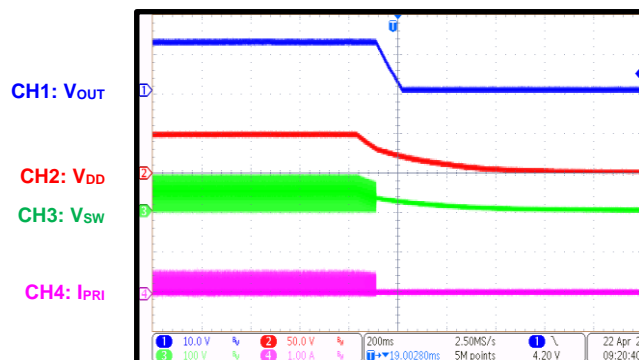
## Start-Up through VDD

$I_{OUT} = 2.1A$



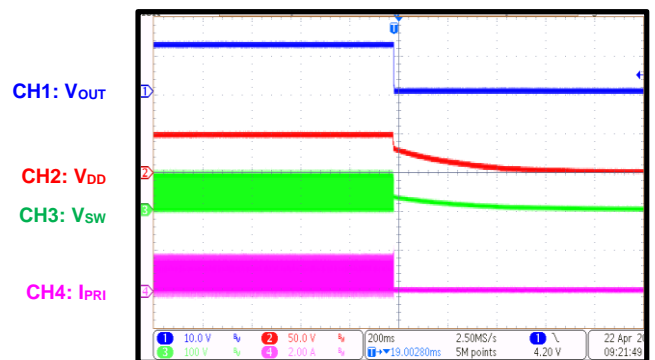
## Shutdown through VDD

$I_{OUT} = 30mA$



## Shutdown through VDD

$I_{OUT} = 2.1A$



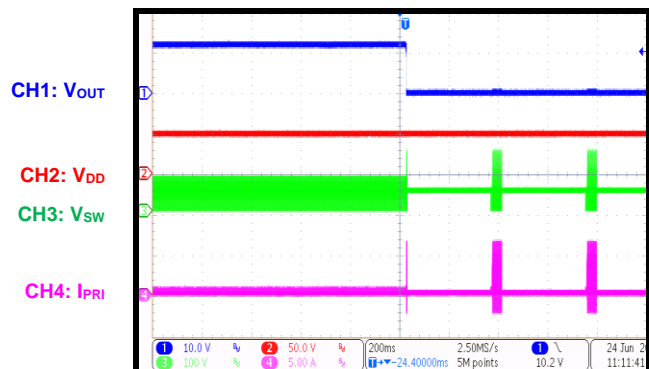


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{DD} - V_{SS} = 48V$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 2.1A$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

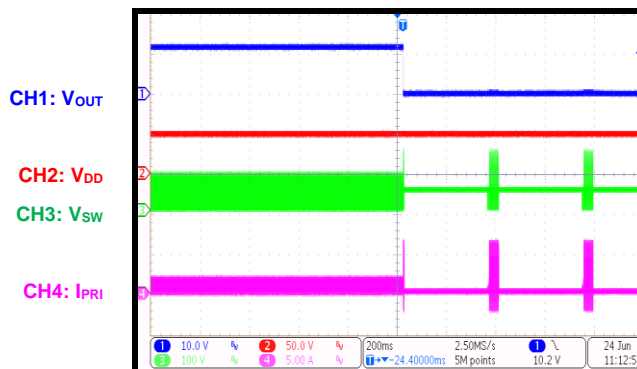
## SCP Entry

$I_{OUT} = 30mA$  to short



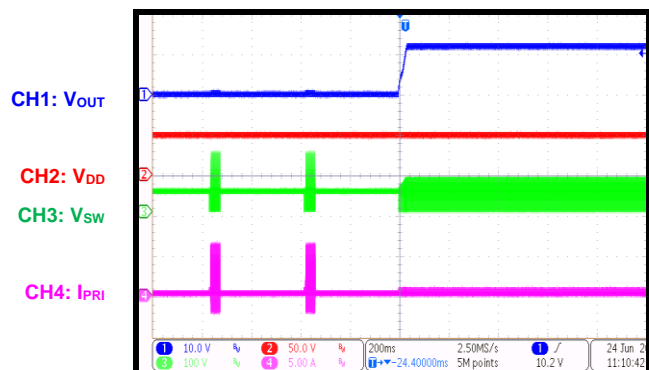
## SCP Entry

$I_{OUT} = 2.1A$  to short



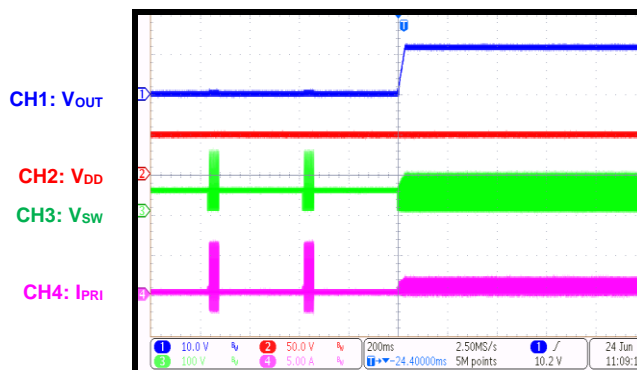
## SCP Recovery

$I_{OUT} =$  short to 30mA



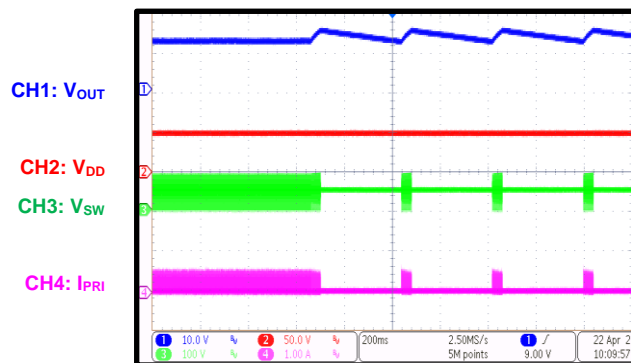
## SCP Recovery

$I_{OUT} =$  short to 2.1A



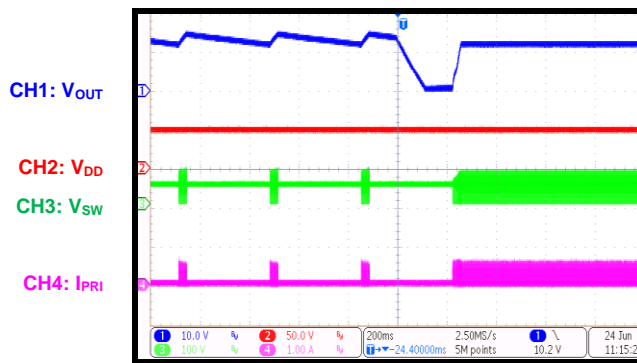
## OVP Entry

$I_{OUT} = 30mA$  to 2mA



## OVP Recovery

$I_{OUT} = 2mA$  to 30mA

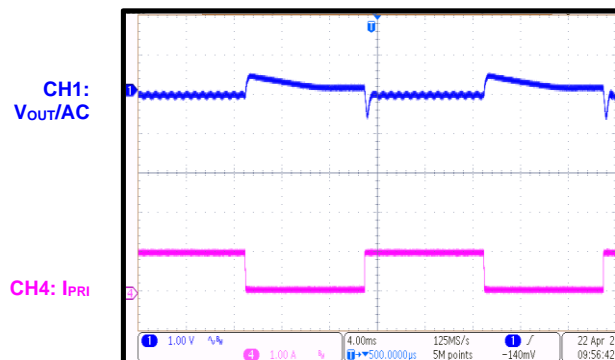


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{DD} - V_{SS} = 48V$ ,  $V_{OUT} = 12V$ ,  $I_{OUT} = 2.1A$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

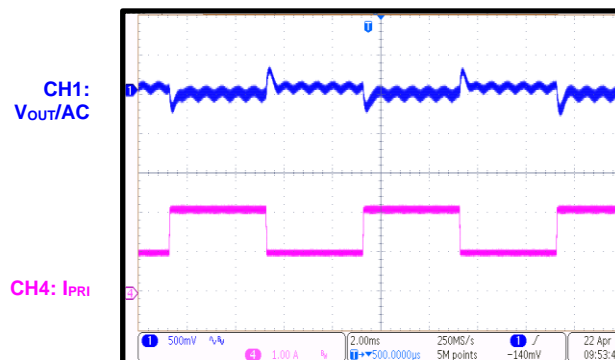
## Load Transient

$I_{OUT} = 30mA$  to  $1A$ ,  $50mA/\mu s$  slew rate



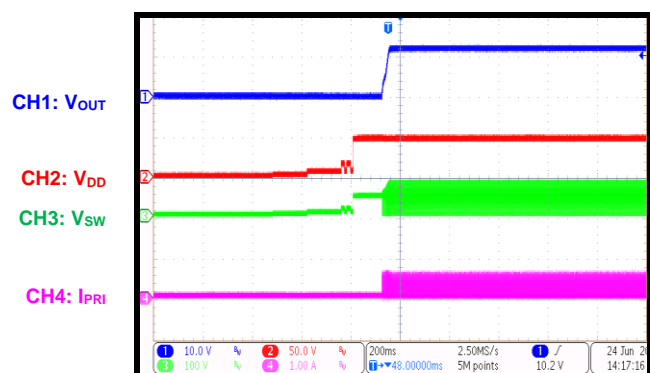
## Load Transient

$I_{OUT} = 1A$  to  $2.1A$ ,  $50mA/\mu s$  slew rate



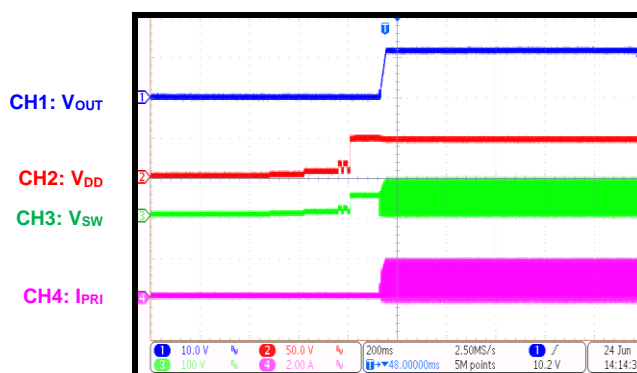
## PSE Start-Up

$I_{OUT} = 30mA$



## PSE Start-Up

$I_{OUT} = 2.1A$



## FUNCTIONAL BLOCK DIAGRAM

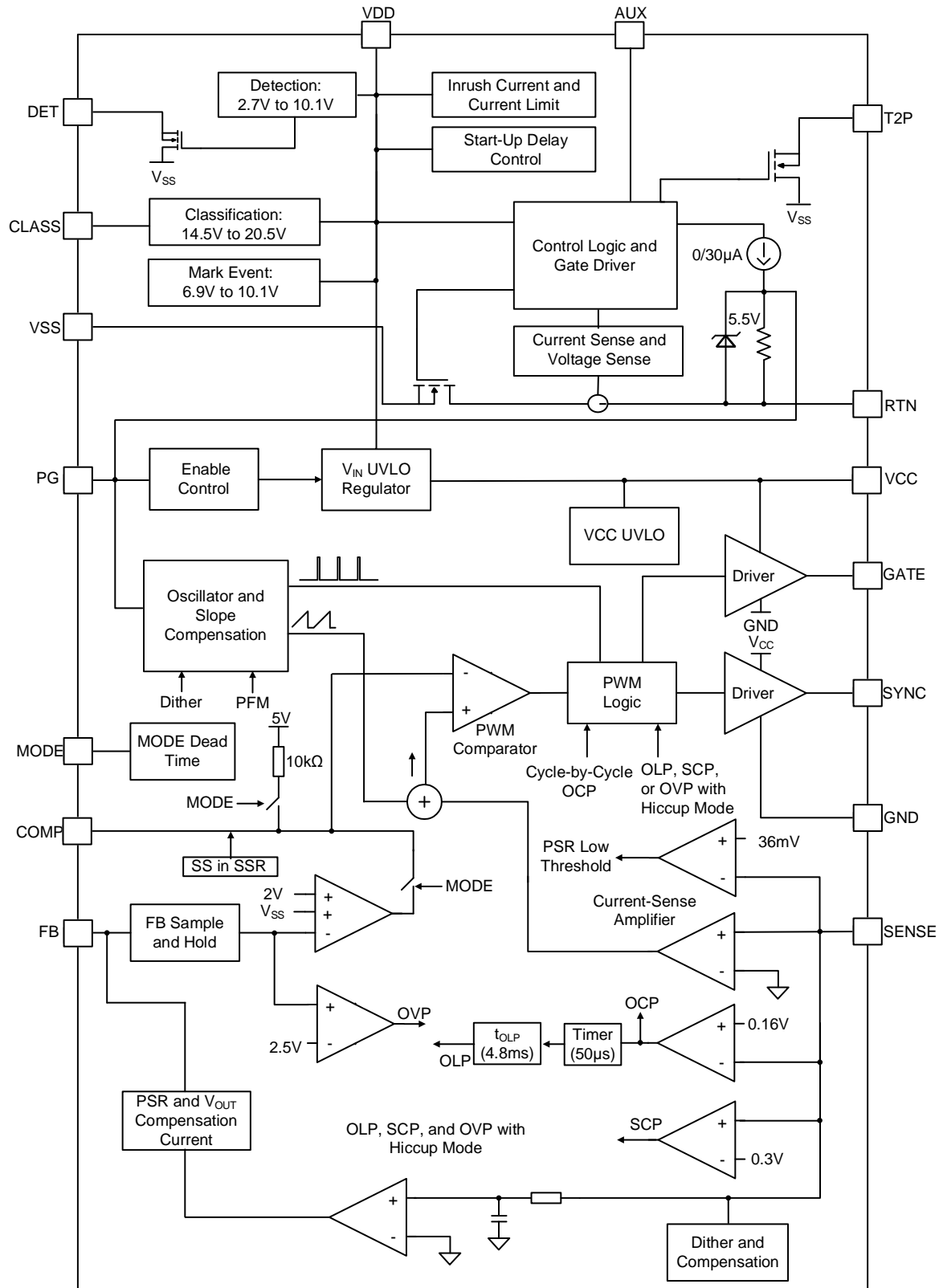
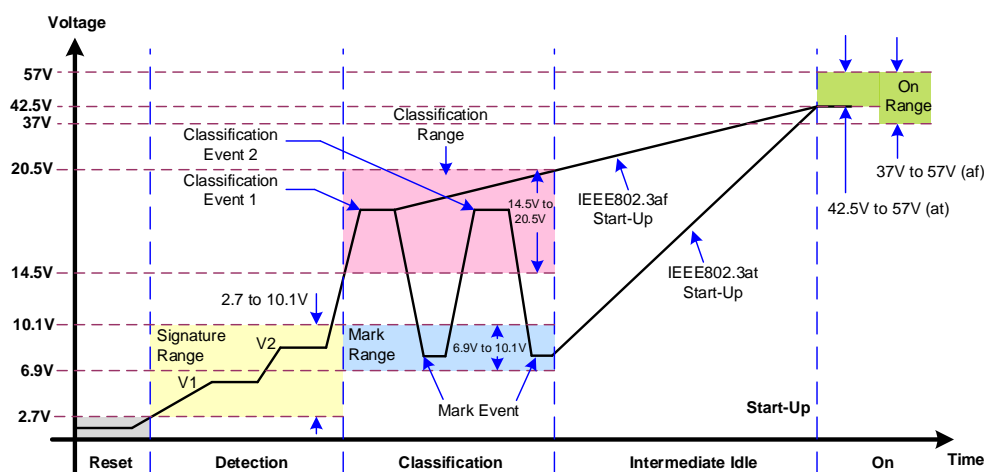


Figure 1: Functional Block Diagram

## OPERATION

Compared to IEEE802.3af, the IEEE802.3at standard establishes a higher power allocation for Power over Ethernet (PoE) while maintaining backward compatibility with existing IEEE 802.3af systems. Power-sourcing equipment (PSE) and powered devices (PD) are distinguished as Type-1 (compliant with IEEE 802.3af power levels) or Type-2 (compliant with IEEE 802.3at power levels). The IEEE 802.3af/at standard establishes a method of communication between PD and PSE with detection, classification, and mark events.

The MP8009A is an integrated PoE solution with an IEEE 802.3af/at PD interface and a peak current-mode flyback controller. Along with the PSE, the MP8009A operates as a safety device. The device supplies voltage only while the PSE recognizes a unique and tightly specified resistance at the end of an unknown length of Ethernet cable. Once it is powered from the PSE, the MP8009A regulates the output voltage ( $V_{OUT}$ ) based on the application circuit setting. Figure 2 shows the typical PD interface power operation sequence.



**Figure 2: PD Interface Power Operation Sequence**

### Detection

In detection mode, a resistor ( $R_{DET}$ ) connected between the DET and VDD pins is presented as a load to the PSE. The PSE applies two “safe” voltages (between 2.7V and 10.1V) to the PD while measuring the change in the drawn current to determine the load resistance. Place a 24.9k $\Omega$  ( $\pm 1\%$ ) resistor between the VDD and DET pins to present a correct signature resistance. The valid signature resistance detected on the power interface (PI) is between 23.7k $\Omega$  and 26.3k $\Omega$ .

The detection resistance detected on the PI is the result of the input bridge resistance that is in series with the VDD load. It is recommended to place a bridge with a Schottky diode after the PI (see the Selecting the Input Bridge section on page 27 for more details).

### Classification

Classification mode specifies the expected load range of the device being powered by the PSE, which allows the PSE to distribute power to as many loads as possible within its maximum current capability. Classification mode is active while the VDD voltage ( $V_{DD}$ ) is between 14.5V and 20.5V. In classification mode, the MP8009A presents a current set via the CLASS resistor ( $R_{CLASS}$ ). Table 1 shows the recommended resistor values for common classification currents.

**Table 1: Recommended Resistor Values for Common Classification Currents**

Class	Max Input Power to PD (W)	$I_{CLASS}$ (mA)	$R_{CLASS}$ ( $\Omega$ )
0	12.95	2	578
1	3.84	10.55	110
2	6.49	18.7	62
3	12.95	28.15	41.2
4	25.5	40.4	28.7

## 2-Event Classification

The MP8009A can be used as a Type-1 PD, with classes 0, 1, 2, and 3 (see Table 1 on page 19). It can also distinguish class 4 with 2-event classification.

In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 2 on page 19 shows an example of 2-event classification. The first classification event occurs once the PSE provides a voltage between 14.5V and 20.5V to the MP8009A, and the MP8009A presents a class-4 load current ( $I_{LOAD}$ ). Then the PSE drops the input voltage ( $V_{IN}$ ) into the marked voltage ( $V_{MARK}$ ) range (between 6.9V and 10.1V) to signal the first mark event. The MP8009A presents a  $I_{LOAD}$  (between 0.5mA to 2mA) in the  $I_{LOAD}$  range.

The PSE repeats this sequence, signaling the second classification and second mark event. Then the PSE applies power to the MP8009A, which charges the DC/DC input capacitor (C1) with a controlled inrush current ( $I_{INRUSH}$ ). Once C1 is fully charged, T2P presents an active-low signal with respect to VSS after the inrush to operation mode delay ( $t_{DELAY}$ ). The T2P output becomes inactive once  $V_{DD}$  drops below the under-voltage lockout (UVLO) protection threshold (see Figure 3).

## PD Interface Under-Voltage Lockout (UVLO) Protection and Current Limit

If the PD is powered by the PSE, and  $V_{DD}$  exceeds the start-up threshold, then the hot-swap MOSFET begins passing a limited  $I_{INRUSH}$  to charge C1. The start-up charge current is about 120mA.

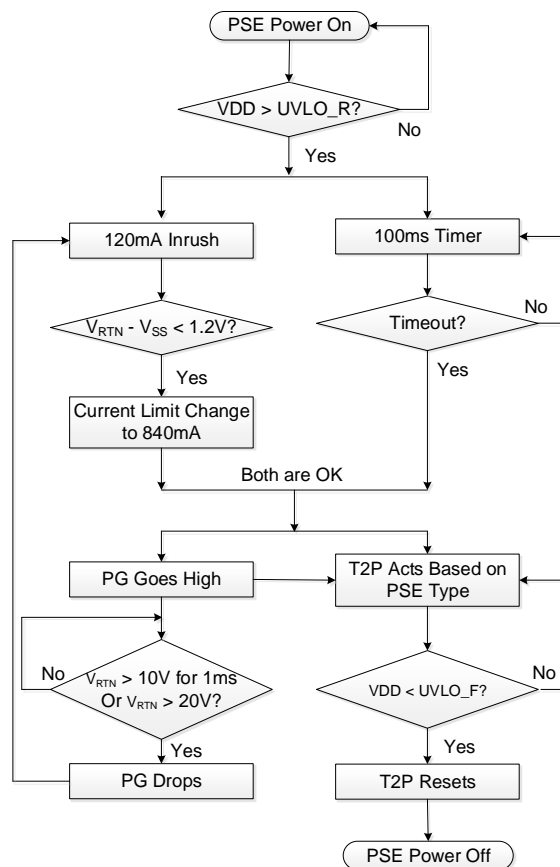
If the RTN voltage drops below 1.2V, then the hot-swap current limit ( $I_{LIMIT}$ ) changes to 840mA. After UVLO is initiated and  $t_{DELAY}$  is complete, the MP8009A asserts the PG signal. The PG signal is pulled high once the hot-swap MOSFET turns on completely. Then PG enables the DC/DC controller.

If ( $V_{DD} - V_{SS}$ ) drops below the UVLO falling threshold, the hot-swap MOSFET is disabled.

If the output current ( $I_{OUT}$ ) overloads, then the internal pass MOSFET  $I_{LIMIT}$  function is enabled, and ( $V_{RTN} - V_{SS}$ ) rises. If  $V_{RTN}$  exceeds 10V for longer than 1ms (or if it exceeds 20V), then

$I_{LIMIT}$  reverts to the inrush value, and the PG voltage ( $V_{PG}$ ) drops low.

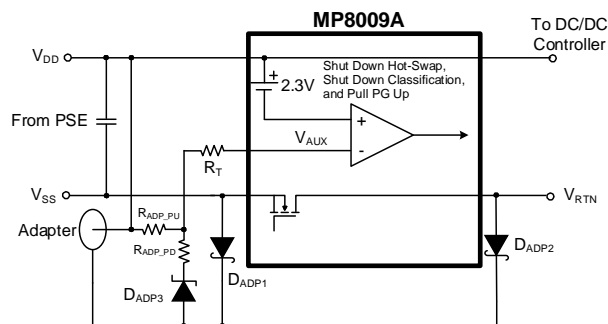
Figure 3 shows the  $I_{LIMIT}$  function, as well as the PG and T2P operation logic during the start-up sequence while the power is supplied via a PSE.



**Figure 3: Start-Up Sequence**

## Wall Adapter Power Detection and Operation

The MP8009A uses wall adapter power detection for applications where an auxiliary power source (e.g. a wall adapter) powers the device (see Figure 4).



**Figure 4: Adapter Power Detection**

Once  $(V_{DD} - V_{SS})$  exceeds 8.5V, the MP8009A enables wall adapter detection. The wall adapter power detection resistor divider is connected between the VDD pin and the negative terminal of the adapter. A Zener diode ( $D_{ADP3}$ ) is added for a more accurate hysteresis. There is a -2.3V reference voltage ( $V_{REF}$ ) between the AUX and VDD pins for adapter detection. The adapter is detected once the AUX voltage ( $V_{AUX}$ ) is triggered. ( $R_{ADP\_PU} + R_{ADP\_PD}$ ) can be calculated with Equation (1):

$$V_{DD} - V_{AUX} = (V_{ADP} - V_{DADP3}) \times \frac{R_{ADP\_PU}}{R_{ADP\_PU} + R_{ADP\_PD}} > 2.3V \quad (1)$$

Where  $V_{ADP}$  is the adapter voltage,  $V_{DADP3}$  is the Zener diode voltage, and ( $R_{ADP\_PU} + R_{ADP\_PD}$ ) is the AUX resistor divider from the adapter power.

If the applied  $V_{ADP}$  exceeds the designed  $V_{ADP}$ , then  $(V_{DD} - V_{AUX})$  is high. If  $(V_{DD} - V_{AUX})$  exceeds 6.5V, then some current may flow out via the AUX pin. Design the external resistor ( $R_{ADP\_PU}$  or  $R_{ADP\_PD}$ ) or a resistor connected between the resistor divider and AUX ( $R_T$ ) to limit the AUX current ( $I_{AUX}$ ). The external resistor limits the current by assuming  $(V_{DD} - V_{AUX})$  is 6.5V (the AUX pin voltage rating) for the calculation. The current flowing out of the AUX pin should be below 3mA.

To ensure that the MP8009A is stable while working with adapter power, place a Schottky diode ( $D_{APD1}$ ) between the negative terminal of the adapter and the VSS voltage ( $V_{SS}$ ).  $D_{APD2}$  can be added to block the reverse current between the adapter and the PSE power source. If a wall adapter is detected, then the internal MOSFET between RTN and VSS turns off, classification current is disabled, and T2P becomes active. The PG signal is active when the adapter power is detected, so that it can enable the downstream DC/DC controller, even if the input hot-swap MOSFET is disabled (see Figure 4).

### Power Good (PG) Control

The PG signal is driven by the internal current source. After  $t_{DELAY}$  starts counting when UVLO is triggered, and RTN drops to 1.2V (or a wall adapter power is detected), the PG signal is pulled high to indicate the power condition.

Then the DC/DC controller is enabled. Figure 3 on page 20 shows the PG logic while the device is powered by the PSE. PG goes high if the adapter is detected under any condition.

PG can be pulled up through external resistor, but the pull-up resistor should be carefully considered to limit the current flowing into the PG pin. An internal Zener diode on the PG pin that clamps  $V_{PG}$  to about 6.5V. Ensure that the current flowing into PG is below 0.4mA.

## DC/DC CONTROLLER OPERATION

### Start-Up and Power Supply

The MP8009A's DC/DC controller features a high-voltage, internal start-up circuit. If the voltage between the VDD and GND pins exceeds 5.5V, then the VCC capacitor ( $C_{VCC}$ ) is charged via the internal LDO. Typically, the VCC voltage ( $V_{CC}$ ) is regulated to 8.5V (if  $V_{DD}$  is sufficiently high), and the VCC UVLO threshold is 5.7V. With the exception of the VCC UVLO threshold, the DC/DC controller has an EN UVLO threshold that is typically 2V. If  $V_{CC}$  is charged above 5.7V and the EN pin is high, then the DC/DC controller starts up.

VCC can be powered from the transformer auxiliary winding to reduce IC power loss after the DC/DC controller starts switching. The auxiliary power should exceed  $V_{CC}$  to override the internal LDO. There is an internal reverse-blocking circuit that allows  $V_{CC}$  to exceed  $V_{DD}$  if VCC has biased power. Due to the pin ratings,  $V_{CC}$  should be  $<16V$ .

If  $V_{DD}$  is below 8.5V and  $V_{CC}$  cannot be regulated to 8.5V, then the internal, high-voltage VCC LDO has a 1.5V voltage drop. This means that the DC/DC controller can operate with an input as low as 8V.

### Operation Mode Detection

After the DC/DC controller is enabled, it outputs a 40μA current to the MODE pin to detect the resistor setting. If the MODE voltage ( $V_{MODE}$ ) exceeds 2.2V, then the controller operates in primary-side regulation (PSR) mode, and the internal error amplifier (EA) is enabled. If the MODE pin is connected to GND via a resistor, the controller operates in secondary-side regulation (SSR) mode.



Table 2 shows the MODE pin configurations.

**Table 2: MODE Pin Configurations**

R <sub>MODE</sub> (kΩ)			Mode	Dead Time (ns)
Min	Typ (1%)	Max		
0	0	3.3	SSR	100
7.32	7.5	8.2	SSR	150
16	16.9	18.7	SSR	200
32.4	32.4	33	SSR	300
64.9	Floating	Floating	PSR	150

In SSR mode, the internal EA is disabled while the COMP voltage ( $V_{COMP}$ ) is pulled up to the internal 5V power source via a 10kΩ resistor. In PSR mode, the  $V_{OUT}$  feedback (FB) signal ( $V_{FB}$ ) is detected by the auxiliary winding via the FB pin. The DC/DC controller reduces the switching frequency ( $f_{SW}$ ), but keeps it above 30kHz under light-load conditions. In SSR mode, the  $V_{FB}$  is detected via the COMP pin, and the controller maintains a fixed  $f_{SW}$ . The peak current ( $I_{PEAK}$ ) can be regulated by  $V_{COMP}$  until it triggers power-save mode (PSM).

Once the controller is enabled, there is a delay time (500μs) before it starts switching. The operation mode, dead time (DT), frequency dithering, and  $V_{OUT}$  compensation settings can be detected by the DC/DC controller during this period (see Table 2, and Table 3 on page 24).

The MODE pin can set the device to PSR or SSR mode. It can also configure the DT between the GATE and SYNC pins.

The MODE detection current lasts about 200μs. Connect a resistor connected between the MODE and GND pins is sufficient. In a noisy environment, connect a capacitor between the MODE and GND pins to provide filtering. Use a ≤100pF capacitor so that  $V_{MODE}$  can rise to a steady state before the DC/DC controller detects it.

### Pulse-Width Modulation (PWM) Mode

The MP8009A DC/DC controller can be set to a flyback or forward topology. In a flyback topology, the external N-channel MOSFET turns on at the beginning of each cycle, forcing the current in the transformer to increase.

The current through the MOSFET can be sensed. If the sum of the SENSE voltage ( $V_{SENSE}$ ) and the slope compensation

signal exceeds the voltage set by  $V_{COMP}$ , then the external MOSFET turns off. The transformer current transmits energy from the primary-side winding to the secondary-side winding, and charges the output capacitor (C2) via the Schottky diode.

The transformer's primary-side current is controlled by  $V_{COMP}$ , which is controlled by the  $V_{FB}$ . This means that  $V_{OUT}$  controls the transformer current to satisfy the load.

In forward topology, the energy is transferred from the primary-side winding to the secondary-side winding once the primary-side N-channel MOSFET turns on. The primary-side  $I_{PEAK}$  is controlled  $V_{COMP}$ , which is controlled by the external shunt voltage regulator integrated circuit (TL431) and optocoupler feedback. See the Voltage Control section to set the  $V_{OUT}$  voltage feedback.

### Voltage Control

#### Primary-Side Regulation (PSR)

Unlike traditional flyback applications with optoisolator feedback, the MP8009A's DC/DC controller can detect the auxiliary winding voltage from the FB pin during the secondary-side output diode conduction period.

If that the secondary-side winding acts as the master, and the auxiliary winding acts as the slave, then the secondary-side diode is conducting.  $V_{FB}$  can be calculated with Equation (2):

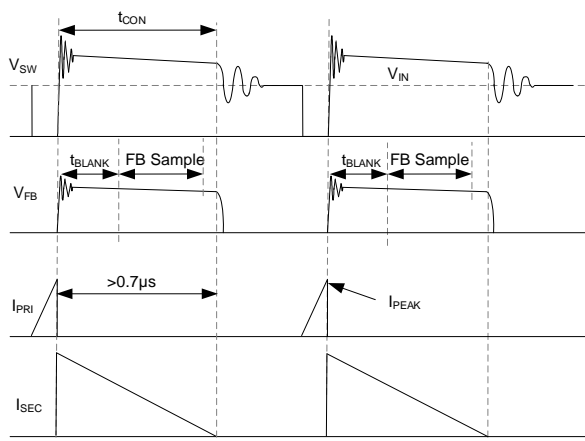
$$V_{FB} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) \times \frac{R_{FBL}}{R_{FBH} + R_{FBL}} \quad (2)$$

Where  $V_{DOF}$  is the output diode forward voltage drop,  $N_A$  is the turn of the auxiliary winding,  $N_S$  is the turn of the secondary-side output winding, and  $(R_{FBH} + R_{FBL})$  is the resistor divider for FB sampling.

The DC/DC controller regulates the primary-side MOSFET switching to ensure that the  $V_{SENSE}$  current signal exceeds 36mV, and starts sampling the auxiliary winding voltage after the power MOSFET turns off. A blanking time (300ns) is inserted to avoid spike ringing due to inductance leakage ( $L_K$ ).

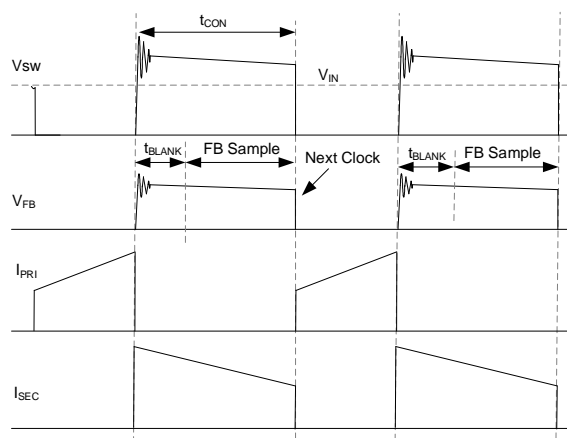
Figure 5 on page 23 shows a FB sample in discontinuous conduction mode (DCM).





**Figure 5: FB Sample in DCM**

Figure 6 shows a FB sample in continuous conduction mode (CCM).



**Figure 6: FB Sample in CCM**

To guarantee a sufficient FB sample period, the output diode current conduction time ( $t_{CON}$ ) at light loads (before the diode current drops to 0A in each cycle) should exceed 600ns. It is recommended that  $t_{CON}$  exceed 700ns, and that  $V_{SENSE\_PK}$  is 33mV. The DC/DC controller GATE signal also provides a minimum off time ( $t_{OFF\_MIN}$ ) (1.2μs). A 70% maximum duty limits  $t_{OFF\_MIN}$  to guarantee a sufficient FB sample time while the DC/DC controller operates with a high duty cycle.

During the FB sensing period,  $V_{FB}$  is sent into the negative input of the EA.  $V_{FB}$  is held until the sensing period is complete. The EA output is generated on the COMP pin. This output controls the transformer  $I_{PEAK}$  to match the output regulation requirement.

## Secondary-Side Regulation (SSR)

The MP8009A's DC/DC controller can also be set to operate in secondary-side regulation (SSR) mode. In SSR mode, the  $V_{OUT}$  signal is fed back to the COMP pin via an optocoupler. The PSR  $V_{FB}$  detection function is disabled, so FB should be connected to GND.

Under light-load conditions, the controller maintains a fixed  $f_{SW}$  in SSR mode. If  $V_{COMP}$  drops, then  $I_{PEAK}$  drops low until it reaches the PSM threshold. The minimum  $I_{LIMIT}$  (36mV) is not available in SSR mode.

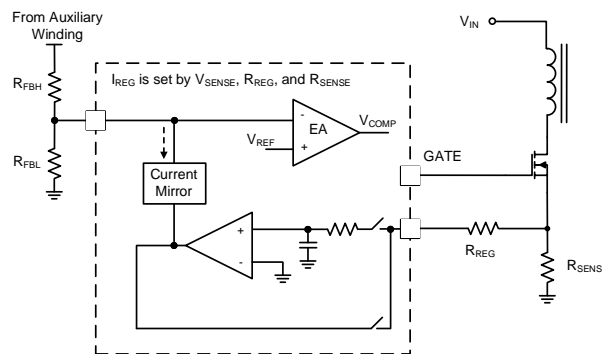
In SSR mode, the DC/DC controller can support both flyback and forward topologies. In PSR mode, it can only support flyback topology.

## Output Voltage Compensation

In PSR mode, the auxiliary winding waveform reflects the secondary-side winding voltage; however,  $V_{OUT}$  differs from the output winding voltage due to the output diode voltage drop and the power-winding resistance. The dropout voltage varies as the conducted current changes.

The resistors connected between the SENSE and GND pins ( $R_{REG}$  and  $R_{SENSE}$ ) set the  $V_{OUT}$  compensation gain while the current varies. The current-sense signal is filtered internally, and controls the FB sink current ( $I_{FB\_SINK}$ ) according to the average SENSE voltage ( $V_{SENSE}$ ).

There are three types of current gains based on the average  $V_{SENSE}$  (see Table 3 on page 24). A sink current on FB leads to a voltage drop on FB's high-side (HS) feedback resistor ( $R_{FBH}$ ), which compensates  $V_{OUT}$  (see Figure 7).



**Figure 7: Output Voltage Compensation**

In SSR mode, this voltage compensation function is disabled.

### Frequency Dithering

The DC/DC controller integrates a frequency dithering circuit to minimize EMI emissions. During steady-state operation,  $f_{SW}$  is fixed internally; however, the frequency dithering circuit is added to the configured frequency with 1.5kHz modulation.

In PSR mode, frequency dithering is fixed at  $\pm 6\%$  of  $f_{SW}$ . In SSR mode, frequency dithering can be configured to be  $\pm 3\%$ ,  $\pm 6\%$ , or  $\pm 9\%$  of  $f_{SW}$  depending on  $R_{REG}$  and  $R_{SENSE}$ .

Table 3 shows the SENSE pin configurations.

**Table 3: SENSE Pin Configurations**

$R_{REG} + R_{SENSE}$ (k $\Omega$ ) <sup>(14)</sup>			PSR Mode		SSR Mode
Min	Typ (1%)	Max	Dither Range (kHz)	$I_{FB} / V_{SENSE}$ Ratio ( $\mu A/mV$ )	Dither Range (kHz)
0	0	1.3	0	0	0
3	3.3	3.6	$\pm 15$	0.054	$\pm 7.5$
6.2	6.8	7.5	$\pm 15$	0.108	$\pm 15$
12.7	12.7	13	$\pm 15$	0.216	$\pm 22.5$
24.9	25.5	28	$\pm 15$	0	$\pm 22.5$

The SENSE pin detection current lasts about 200 $\mu s$  after start-up. Two resistors ( $R_{REG}$  and  $R_{SENSE}$ ) connected between the SENSE and GND pins is typically sufficient. In a noisy environment, connect a capacitor between the SENSE and GND pins to provide filtering.

### Current Sense and Over-Current Protection (OCP)

The MP8009A's DC/DC controller is a peak current-mode flyback/forward controller. The current through the external MOSFET can be sensed via a sensing resistor connected in series with the MOSFET source. The voltage sensed on the SENSE pin is then amplified and fed to the high-speed current comparator for current mode control. The current comparator takes this sensed voltage (and the slope compensation) as one of its inputs, and compares it to the COMP voltage ( $V_{COMP}$ ). If the amplified current signal exceeds  $V_{COMP}$ , then

the comparator outputs low, and the power MOSFET turns off.

If  $V_{SENSE}$  exceeds the  $I_{LIMIT}$  threshold (typically 160mV), then the controller turns off the GATE output for that cycle. The output remains off until the internal oscillator starts the next cycle and senses the current again. Cycle-by-cycle current limiting limits the MOSFET's current.

### Error Amplifier (EA)

In PSR mode, the DC/DC controller senses the FB voltage ( $V_{FB}$ ) during the flyback period with a pulsed FB signal. Then the FB signal is held and fed into the error amplifier (EA). The EA regulates  $V_{COMP}$  based on  $V_{FB}$ . Then  $V_{COMP}$  controls the peak transformer current to regulate  $V_{OUT}$ .

In SSR mode, the internal EA is disabled and the COMP pin is pulled up via an internal resistor. An external optocoupler can be connected to the COMP pin for  $V_{OUT}$  signal feedback.

### Light-Load Operation

In PSR mode,  $V_{COMP}$  decreases to regulate the lower peak transformer current under light-load conditions. If the sensed  $I_{PEAK}$  signal is below 36mV, then the controller does not reduce the transformer current, and instead reduces  $f_{SW}$ . As a result, the transferred energy decreases and  $V_{OUT}$  is regulated.

The DC/DC controller limits the minimum  $f_{SW}$  above 30kHz in PSR mode under light-load conditions. This helps the MP8009A detect  $V_{OUT}$  with a 30kHz  $f_{SW}$  and avoid audible noise. This minimum  $f_{SW}$  requires some load to maintain  $V_{OUT}$ ; otherwise,  $V_{OUT}$  can rise and trigger over-voltage protection (OVP).

In SSR mode, the DC/DC controller maintains a fixed  $f_{SW}$  under light-load conditions.  $V_{COMP}$  continues to drop until it reaches the power-save mode (PSM) threshold.

### Over-Voltage Protection (OVP)

The DC/DC controller provides OVP. If  $V_{FB}$  exceeds 125% of  $V_{REF}$ , then the controller shuts off the gate driving signal and enters hiccup mode. The controller restarts after 340ms. If the over-voltage (OV) fault is removed, then the part resumes normal operation. Connect the FB

and GND pins if the OVP function is not used.

To avoid mistripping OVP due to the oscillation of  $L_K$  and parasitic capacitance, OVP sampling has a blanking time.

### Overload Protection (OLP)

The DC/DC controller limits  $I_{PEAK}$  cycle by cycle for over-current protection (OCP). If the load continues increasing after triggering the switching OCP, then  $V_{OUT}$  decreases and  $I_{PEAK}$  triggers OCP each cycle.

The DC/DC controller sets overload detection by monitoring  $V_{SENSE}$ . Once the internal soft start finishes, overload protection (OLP) is enabled. If an OCP signal is detected for longer than 4.8ms, the controller turns off the GATE driver. After a delay time (340ms), the controller starts up again.

A one-shot on-timer (50 $\mu$ s) is activated during OLP. It remains active for 50 $\mu$ s after an OCP pulse. This means that if there is an OCP pulse in a 50 $\mu$ s period, then the controller triggers OCP. If the condition is removed within 4.75ms, then the DC/DC controller resumes normal operation.

### Short-Circuit Protection (SCP)

If the output is shorted to ground, then OCP is triggered. The current is limited cycle by cycle, and OLP may also be triggered.

If  $I_{PEAK}$  cannot be limited by  $V_{SENSE}$  (160mV) in each cycle due to the minimum gate on time ( $t_{ON\_MIN\_GATE}$ ), then the current can become very high and saturate the transformer. If the monitored  $V_{SENSE}$  exceeds 300mV, then the GATE pin turns off and the part enters hiccup mode with a 340ms off time ( $t_{OFF}$ ).

If the short circuit is removed, then  $V_{OUT}$  recovers after the next restart cycle with a delay time (340ms).

### Soft Start (SS)

The DC/DC controller provides soft start (SS) by charging an internal capacitor with a current source. During the soft-start period,  $V_{SS}$  ramps up slowly. If a commanded shutdown occurs, a thermal shutdown occurs, or protection function is triggered, then the soft-start capacitor ( $C_{SS}$ ) is discharged completely.

In PSR mode,  $V_{SS}$  is clamped at the FB

reference voltage. The FB reference soft-start time ( $t_{SS}$ ) is set by  $V_{SS}$  (between 0V and 2V).

In SSR mode,  $V_{SS}$  is clamped at  $V_{COMP}$  until  $V_{COMP}$  reaches the switching current.

### Minimum On Time

The transformer parasitic capacitance and the gate driver signal induce a current spike on  $R_{SENSE}$  while the power MOSFET turns on. The controller uses a leading-edge blanking time (250ns) to avoid terminating the switching pulse. During this blanking period, the current-sense comparator is disabled, and the gate driver remains on.

### Gate Driver

The DC/DC controller integrates a high-current gate driver for the primary-side N-channel MOSFET. The high-current gate driver provides strong driving capability and benefits from MOSFET selection. If the external MOSFET ( $Q_G$ ) is low, then the switching speed should be low to reduce EMI. It is recommended that the series resistance be  $>5\Omega$ .

The controller also integrates a SYNC driver pin to turn the synchronous driver on and off. Pull SYNC high to turn the synchronous driver off; pull SYNC low to turn it on. Figure 8 shows the phase and DT relationship between the GATE and SYNC drivers.

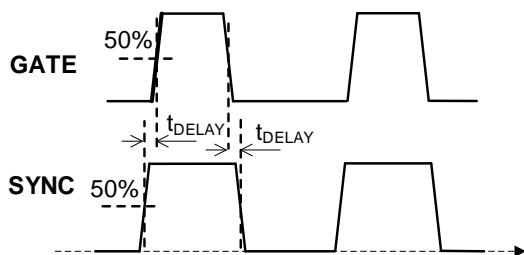


Figure 8: GATE and SYNC Driver

If the IC turns off due to UVLO protection or another protection, both the GATE and SYNC pins are pulled low.

### Transformer Inductance Considerations

In PSR mode, the DC/DC controller samples  $V_{OUT}$  during the flyback time, so the secondary diode conduction time (with a minimum  $I_{PEAK}$  controlled by the 33mV minimum current-sense limit) should be longer than 0.7 $\mu$ s. The transformer inductance can be estimated with Equation (3):

$$L_{PRI} \geq (V_{OUT} + V_{DOF}) \times \frac{N_p}{N_s} \times 0.7\mu s \times \frac{R_{SENSE}}{33mV} \quad (3)$$

Where  $L_{PRI}$  is the transformer's primary inductance, and  $V_{DOF}$  is the output rectifier diode's forward voltage drop.

In SSR mode, there is no inductance limit, but it is recommended to set  $I_{PEAK}$  high enough to avoid triggering PSM logic. If the system is designed for CCM, PSM may cause a higher  $V_{OUT}$  ripple, especially in synchronous mode forward topology.

### Over-Temperature Protection (OTP)

Thermal shutdown is employed to prevent the chip from operating at exceedingly high temperatures. The MP8009A has a separate temperature-monitoring circuit for the PD and the DC/DC power controller. The controller's thermal protection does not affect the PD interface, but the PD temperature protection turns off both the PD and the controller. Once the temperature drops below the falling threshold, then the MP8009A starts up and resumes normal operation.

## APPLICATION INFORMATION

### Selecting the Detection Resistor ( $R_{DET}$ )

In detection mode, a resistor should be connected between the DET and VDD pins to act as a load for the PSE. The resistance is calculated by  $\Delta V / \Delta I$ , and should be between 23.7k $\Omega$  and 26.3k $\Omega$ . Use a typical value of 24.9k $\Omega$  for the detection resistor.

### Selecting the Input Bridge

For the input bridge after the power interface (PI), it is recommended to bridge with Schottky diodes to reduce resistance for the detection function and to increase power conduction during steady state (see Figure 19 on page 36).

If a bridge with PN junction diodes must be used, the detection resistor ( $R_{DET}$ ) should be connected between the VDD and VSS pins (see Figure 20 on page 37). In this case, float the DET pin.

### Selecting the Classification Resistor ( $R_{CLASS}$ )

To distribute power to as many loads as possible from the PSE, place a resistor between the CLASS and VSS pins to classify the PD power level (which draws a fixed current set by  $R_{CLASS}$ ). Table 1 on page 19 shows how to select  $R_{CLASS}$  to supply power to the PD. The typical CLASS voltage ( $V_{CLASS}$ ) in the classification range is 1.16V. It produces 47mW of power loss on  $R_{CLASS}$ , even under class-4 conditions.

### Selecting the TVS Protection Diode

To limit the input transient voltage within the absolute maximum ratings, a transient voltage suppressor (TVS) diode should be placed across the rectified voltage ( $V_{DD} - V_{SS}$ ). An SMAJ58A or equivalent diode is recommended for general indoor applications. Outdoor transient levels or other special applications require additional protection.

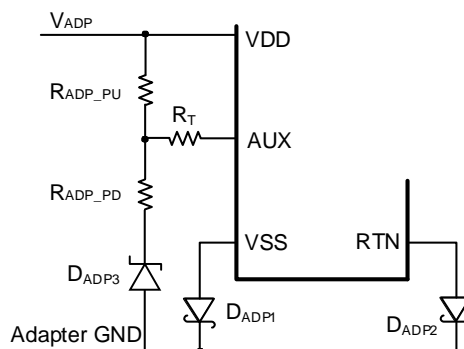
### Selecting the PD Input Capacitor

A 0.05 $\mu$ F to 0.12 $\mu$ F input bypass capacitor (from VDD to VSS) is required to meet IEEE 802.3at/af specifications. It is recommended to use a 0.1 $\mu$ F, 100V ceramic capacitor.

### Wall Adapter Power Detection Circuit

For the best wall adapter power detection while an auxiliary power source powers the device,

the resistor divider ( $R_{ADP\_PU} + R_{ADP\_PD}$ ) and the diode ( $D_{ADP3}$ ) should be selected according to Equation (1) on page 21 (see Figure 9).



**Figure 9: Wall Adapter Detection Circuit**

Choose  $R_{ADP\_PU}$  to be about 3k $\Omega$  to balance the power loss and the  $D_{ADP1} / D_{ADP2}$  leakage current discharge. A resistor ( $R_T$ ) limits the AUX current below 3mA when  $V_{ADP}$  is high. The minimum  $R_T$  value can be estimated with Equation (4):

$$R_T(k\Omega) = \frac{(V_{ADP} - V_{DADP3}) \times R_{ADP\_PU} - 6.5}{R_{ADP\_PU} + R_{ADP\_PD} \times 3} \quad (4)$$

It is recommended to have  $D_{ADP1}$  Schottky diode with a 100V voltage rating and small package size (e.g. BAT46W). The voltage rating of  $D_{ADP2}$  should be  $\geq 100V$ , and the current rating should exceed the input current ( $I_{IN}$ ). A low voltage drop Schottky diode (e.g. STPS2H100) is recommended to reduce conduction power loss.

### Power Good (PG) Indication Setting

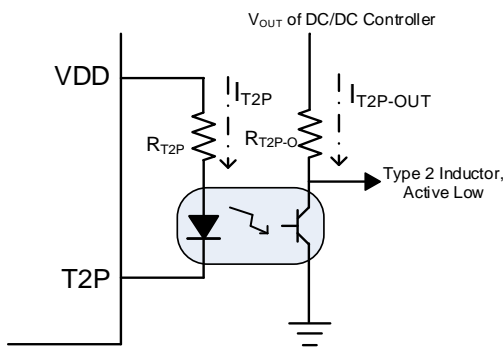
The MP8009A integrates provides power good (PG) indication. If the PG logic is high, then PG is pulled high via an internal pull-up current source. This allows the device to enable the DC/DC controller without an external pull-up circuit. If PG is in a logic low state, then the internal pull-up current is disabled, and PG is pulled low via an internal resistor.

### T2P Indication Connection

The T2P pin is an active-low, open-drain output that indicates whether a Type-2 PSE or a wall adapter is connected. An optocoupler can interface the T2P pin to the circuitry on the



secondary side of the converter (see Figure 10).



**Figure 10: T2P Indicator Circuit**

It is recommended to use a high-gain optocoupler and a high-impedance receiver (e.g. CMOS).

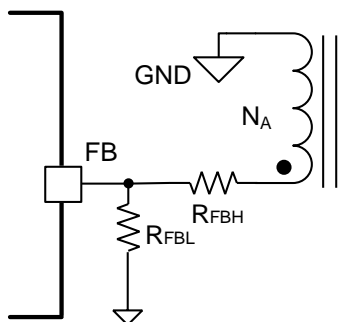
Consider the T2P sink current (typically 2mA), the T2P output low voltage (0.1V), and the diode forward voltage drop in design. Choose  $R_{T2P}$  to be 23.7kΩ to match the 48V input. If the the DC/DC controller's  $V_{OUT}$  is 12V, then  $R_{T2P-O}$  should be 20kΩ (based on the CRT), even if it varies with temperature, LED biased current, and aging.

If an LED can light up from VDD to T2P to indicate whether a Type-2 PSE is available, then  $R_{T2P}$  can have a higher resistance to match the LED's maximum current and to reduce power loss.

### Output Voltage Setting

In the MP8009A's DC/DC controller, there are two feedback modes: primary-side regulation (PSR) and secondary-side regulation (SSR).

In PSR mode, the converter detects the auxiliary winding voltage from the FB pin. The resistor divider ( $R_{FBH} + R_{FBL}$ ) is used for feedback sampling (see Figure 11).



**Figure 11: FB Sampling in PSR Mode**

If the primary-side power MOSFET is off, then the auxiliary winding voltage is proportional to the output winding. Then  $V_{OUT}$  can be estimated with Equation (5):

$$V_{OUT} = \frac{V_{REF} \times (R_{FBH} + R_{FBL})}{R_{FBL}} \times \frac{N_S}{N_A} - V_{DOF} \quad (5)$$

Where  $N_S$  is the transformer's number of secondary-side winding turns,  $N_A$  is the transformer's number of auxiliary winding turns,  $V_{DOF}$  is the output rectifier diode forward drop, and  $V_{REF}$  is the reference voltage on the FB pin.

If the main power MOSFET is on, then the auxiliary winding voltage is negative and  $V_{FB}$  is limited by the internal circuit. Then the current flowing out of the FB pin can be calculated with Equation (6):

$$I_{FB} = \frac{1}{R_{FBH}} \times \left( \frac{V_{IN} \times N_A}{N_P} \right) \quad (6)$$

$R_{FBH}$  should high enough to limit the negative FB current to below 1mA. Due to FB's parasitic capacitance, choose  $R_{FBH}$  to be <100kΩ.

In SSR mode,  $V_{OUT}$  is set via TL431. If TL431's  $V_{REF}$  is 2.5V, and the expected  $V_{OUT}$  is 12V, then the upper and lower divider resistor ratio is 3.8. TL431 generates an amplified signal to control the DC/DC controller's COMP pin via an optocoupler (e.g. PC357). COMP controls the current, and  $V_{OUT}$  is regulated based on the feedback signal.

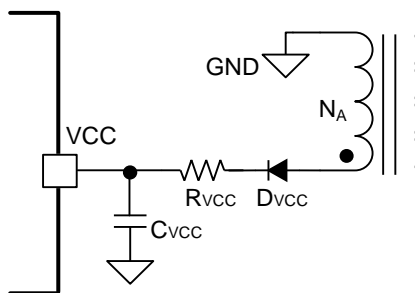
### Operation Mode Setting

Once enabled, the DC/DC controller outputs a current (40μA) to the MODE pin to detect the MODE resistance. If  $V_{MODE}$  exceeds 2.2V, then the controller operates in PSR mode; otherwise, it operates in SSR mode. The MODE pin can configure the DT between the GATE and SYNC pins (see Table 2 on page 22).

### VCC Power Supply Setting

$V_{CC}$  is regulated by the internal LDO via VDD.  $V_{CC}$  is typically regulated at 8.5V. Connect a decoupling capacitor between the VCC and GND pins.

In flyback mode, choose  $C_{VCC}$  to be  $\geq 1\mu F$ .  $V_{CC}$  can also be powered by the transformer auxiliary winding to reduce high-voltage LDO power loss (see Figure 12 on page 29).



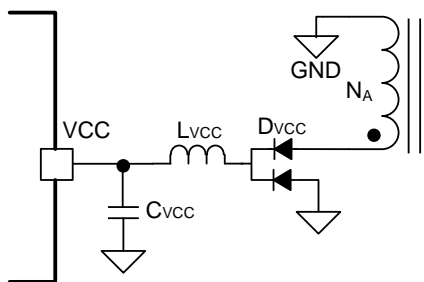
**Figure 12: V<sub>CC</sub> from the N<sub>A</sub> Winding in Flyback Application**

The auxiliary winding supply voltage (V<sub>CC</sub>) can be estimated with Equation (7):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{DOF}) - V_{DVCCF} \quad (7)$$

Where V<sub>DVCCF</sub> is the D<sub>VCC</sub> voltage drop from the auxiliary winding.

In forward mode, choose C<sub>VCC</sub> to be  $\geq 4.7\mu\text{F}$ . V<sub>CC</sub> can also be powered by the transformer auxiliary winding (see Figure 13).



**Figure 13: V<sub>CC</sub> from N<sub>A</sub> Winding in Forward Application**

The auxiliary winding supply voltage (V<sub>CC</sub>) can be calculated with Equation (8):

$$V_{CC} = \frac{N_A}{N_S} \times V_{OUT} \quad (8)$$

V<sub>CC</sub> should be below 16V.

### Output Voltage Compensation Setting and Frequency Dithering Setting

The SENSE pin can set the V<sub>OUT</sub> and frequency dithering function. Once enabled, the DC/DC controller outputs a current (100μA) to the SENSE pin to detect the SENSE resistance. The controller determines the compensation type and the frequency dithering type based on the resistance (see Table 3 on page 24). V<sub>OUT</sub> compensation can only be enabled in PSR mode.

### Selecting the Current-Sense Resistor (R<sub>SENSE</sub>)

The MP8009A's DC/DC controller is a peak-current-mode flyback/forward controller. The current through the external MOSFET can be sensed via a sensing resistor. If the voltage sensed on the SENSE pin exceeds the current-limit threshold voltage (typically 160mV), the controller turns off the GATE output for that cycle.

To avoid reaching the current limit, the voltage on the sensing resistor (R<sub>SENSE</sub>) should be below 80% of the current limit voltage (160mV). R<sub>SENSE</sub> can be estimated with Equation (9):

$$R_{SENSE} = \frac{0.8 \times 160\text{mV}}{I_{PEAK}} \quad (9)$$

Where I<sub>PEAK</sub> is the primary-side peak current.

### Selecting the Power MOSFET

The controller can drive a wide variety of N-channel power MOSFETs. The critical parameters to select the MOSFET are the maximum drain-to-source voltage (V<sub>DS\_MAX</sub>), the maximum current (I<sub>D\_MAX</sub>), the on resistance (R<sub>DS(ON)</sub>), the total gate charge (Q<sub>G</sub>), and the turn-on threshold (V<sub>TH</sub>).

In flyback applications, the off-state voltage across the MOSFET (V<sub>MOSFET</sub>) can be calculated with Equation (10):

$$V_{MOSFET} = V_{IN} + N \times V_{OUT} \quad (10)$$

Consider the voltage spike while the MOSFET turns off. V<sub>DS\_MAX</sub> should exceed 1.5 times the calculated voltage.

In forward applications, V<sub>MOSFET</sub> can be calculated with Equation (11):

$$V_{MOSFET} = \frac{D \times V_{IN}}{1 - D} + V_{IN} \quad (11)$$

Where D is the duty cycle, and the maximum duty cycle is limited at about 70%.

The maximum current through the power MOSFET occurs while V<sub>IN</sub> is at its minimum and the output power is at its maximum. The current rating of the MOSFET should exceed 1.5 times RMS current (I<sub>RMS</sub>) rating.

The on resistance of the MOSFET determines the conduction loss.



$Q_G$  is important in MOSFET selection because it determines the commutation time. A high  $Q_G$  results in high switching loss, while a low  $Q_G$  can result in a fast turn-on/off speed. The turn-on/off speed determines the voltage spike on the MOSFET.

$V_{TH}$  is also important in MOSFET selection. GATE is powered by VCC; therefore,  $V_{TH}$  should be below  $V_{CC}$ .

### Selecting the Flyback Transformer

A transformer is an important component in a flyback converter, as it determines the duty cycle,  $I_{PEAK}$ , efficiency, MOSFET, and output diode rating. A good transformer should consider the winding ratio, primary-side inductance, saturation current,  $L_K$ , current rating, and core selection.

The transformer winding ratio is important because it determines the duty cycle. The duty cycle (D) can be calculated with Equation (12):

$$D = \frac{N \times V_{OUT}}{N \times V_{OUT} + V_{IN}} \quad (12)$$

Where N is the transformer's primary-side winding to output winding ratio.

A duty cycle of about 45% is recommended for most applications.

The primary-side inductance affects the  $I_{IN}$  ripple ratio factor. A higher-value inductor results in a larger transformer size and higher cost. A lower-value inductor results in a high switching  $I_{PEAK}$  and  $I_{RMS}$ , which can reduce efficiency. Choose a primary-side inductor to set the  $I_{IN}$  ratio factor between 30% and 50%. The primary-side inductance ( $L_P$ ) can be calculated with Equation (13):

$$L_P = \frac{V_{IN} \times D^2}{2 \times n \times I_{IN} \times f_{SW}} \quad (13)$$

Where n is the current ripple ratio.

Calculate  $L_P$  based on the minimum  $V_{IN}$  condition.

The transformer should have a high enough saturation current to support the switching  $I_{PEAK}$ ; otherwise, the transformer inductance can decrease significantly.  $R_{SENSE}$  limits the switching  $I_{PEAK}$ .

The energy stored in  $L_K$  cannot couple to the secondary side. This causes a high voltage spike as the MOSFET turns off. This decreases efficiency and increases stress on the MOSFET. Typically, the transformer  $L_K$  should be below 3% of the transformer inductance.

The current rating counts  $I_{RMS}$ , which allows current to flow through each winding. The current density should be controlled; otherwise, it can lead to increased resistor power loss.

### Diode Conduction Time Setting for PSR Flyback Applications

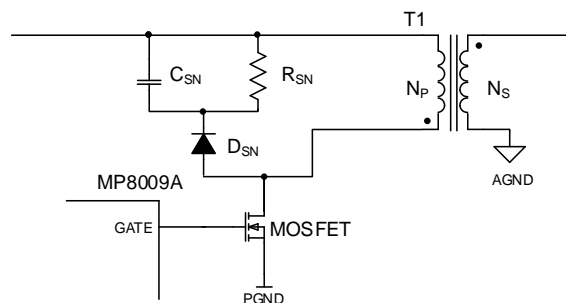
In PSR mode, the controller samples the auxiliary-winding voltage after the primary-side power MOSFET turns off. A blanking time (300ns) reduces spike ringing due to  $L_K$ . To guarantee a sufficient FB sample period, the output diode current conduction time ( $t_{CON}$ ) under light-load conditions should be >600ns. Design the transformer to ensure that  $t_{CON} > 700ns$ , and that  $V_{SENSE\_PK}$  is 33mV.  $t_{CON}$  can be calculated with Equation (14):

$$t_{CON} = \frac{33mV \times L_P \times N_S}{R_{SENSE} \times N_P \times (V_{OUT} + V_{DOF})} \geq 700ns \quad (14)$$

Where  $V_{DOF}$  is the output diode's forward voltage drop.

### Selecting the RCD Snubber for Flyback Applications

The transformer's  $L_K$  can cause spikes and excessive ringing on the MOSFET drain voltage waveform. An RCD snubber circuit limits the MOSFET voltage spike (see Figure 14).



**Figure 14: RCD Snubber Circuit**

The power dissipation in the snubber circuit ( $P_{SN}$ ) can be estimated with Equation (15):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{PEAK}^2 \times f_{SW} \quad (15)$$

Where  $I_{PEAK}$  is the peak switching current.

$R_{SN}$  consumes the  $L_K$  power loss.  $R_{SN}$  can be calculated with Equation (16):

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}} \quad (16)$$

Where  $V_{SN}$  is the expected snubber voltage on the snubber capacitor ( $C_{SN}$ ).

$C_{SN}$  can be designed to achieve an appropriate voltage ripple on the snubber. The snubber voltage ripple can ( $\Delta V_{SN}$ ) can be estimated with Equation (17):

$$\Delta V_{SN} = \frac{V_{SN}}{R_{SN} \times C_{SN} \times f_{SW}} \quad (17)$$

A 15% ripple is acceptable, typically.

### Selecting the Output Diode for Flyback Applications

The flyback output rectifier diode supplies current to the output capacitor while the primary-side MOSFET is off. Use a Schottky diode to reduce losses due to the diode's forward voltage and recovery time. The diode should be rated for a reverse-voltage 1.5 times the calculated value. The diode voltage ( $V_{DIODE}$ ) can be estimated with Equation (18):

$$V_{DIODE} = \frac{V_{IN}}{N} + V_{OUT} \quad (18)$$

The average current rating should exceed the maximum  $I_{LOAD}$ . The  $I_{PEAK}$  rating should exceed the output winding  $I_{PEAK}$ . It is recommended to add an RC snubber circuit for the output diode.

### Selecting the Transformer for Forward Applications

The forward transformer transfers energy to the output while the power MOSFET is on. Its key parameters are the winding ratio, primary-side winding turns, current rating, and core selection. The transformer winding ratio determines the duty cycle. The duty cycle ( $D$ ) can be calculated with Equation (19):

$$D = \frac{V_{OUT} \times N}{V_{IN}} \quad (19)$$

Where  $N$  is the transformer's primary-side winding to output winding ratio. A 45% duty

cycle is recommended for most applications.

If the power MOSFET is on, then the transformer transfers energy to the output, and  $V_{IN}$  generates an exciting current in the transformer. There should be sufficient primary-side winding to prevent the transformer from saturating. The peak exciting current ( $I_{EXC}$ ) can be estimated with Equation (20):

$$I_{EXC} = \frac{V_{OUT} \times N}{2 \times L_P \times f_{SW}} \quad (20)$$

Where  $L_P$  is the primary inductance.

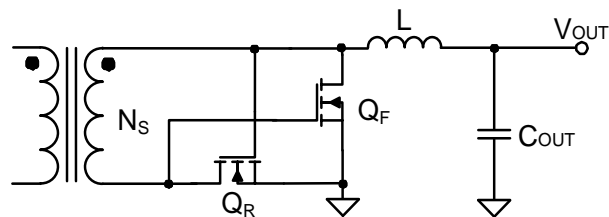
When using  $I_{EXC}$  to calculate the primary winding, ensure that there are sufficient margins for extreme conditions (e.g. load transient and OCP). The current rating is dependent on the maximum  $I_{RMS}$ , which flows through each winding. The current density should be controlled to high resistive power loss.

### Selecting the Synchronous MOSFET for Forward Applications

The MP8009A's DC/DC controller supports active-clamp forward applications. The active clamp P-channel MOSFET should have the same maximum voltage as the main power MOSFET. Its maximum current should exceed the exciting  $I_{PEAK}$  and  $I_{RMS}$ .

### Selecting the Output MOSFET for Forward Applications

The forward output requires two diodes to conduct the current. If higher efficiency is required, then the diodes can be replaced with MOSFETs (see Figure 15).



**Figure 15: Forward Output MOSFET**

The MOSFET voltage rating should exceed its  $V_{DS\_MAX}$ . The  $Q_R$   $V_{DS\_MAX}$  ( $V_R$ ) can be calculated with Equation (21):

$$V_R = \frac{D \times V_{IN}}{N \times (1 - D)} \quad (21)$$

The  $Q_F V_{DS\_MAX}$  ( $V_F$ ) can be calculated with Equation (22):

$$V_F = \frac{V_{IN}}{N} \quad (22)$$

Where  $N$  is the transformer's primary winding to output winding ratio, and  $D$  is the primary MOSFET's duty cycle. Ensure that there is some margin.

The MOSFET current rating should exceed its maximum  $I_{RMS}$  and maximum  $I_{PEAK}$ . The  $Q_R I_{RMS}$  ( $I_R$ ) can be estimated with Equation (23):

$$I_R = I_{OUT} \times \sqrt{D} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{I_{PP}}{I_{OUT}}\right)^2} \quad (23)$$

The  $Q_F I_{RMS}$  ( $I_F$ ) can be calculated with Equation (24):

$$I_F = I_{OUT} \times \sqrt{1-D} \times \sqrt{1 + \frac{1}{3} \times \left(\frac{I_{PP}}{I_{OUT}}\right)^2} \quad (24)$$

Where  $I_{PP}$  is the inductor's peak-to-peak current.

The  $Q_R$  MOSFET's gate driver voltage is equal to  $V_F$ . The  $Q_F$  MOSFET's gate driver voltage is equal to  $V_R$ . If the driver voltage exceeds each MOSFET's maximum gate voltage, then a clamp circuit is required. The MOSFET turn-on resistance determines the conduction loss, while  $Q_G$  determines the driver circuit loss. These values should be low enough to provide high efficiency and lower rising temperatures.

### Selecting the Output Inductor for Forward Applications

The output inductor used for forward applications supplies constant current to the output load, while the main power MOSFET is on. A larger-value inductor results in less ripple current and a lower output voltage ripple ( $\Delta V_{OUT}$ ); however, a larger-value inductor has a larger physical size, higher series resistance, and lower saturation current. A good rule to determine the inductance is to allow the peak-to-peak inductor ripple current ( $\Delta I_L$ ) be between 30% and 50% of the maximum  $I_{OUT}$ . The inductance ( $L$ ) can be calculated by with Equation (25):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT} \times N}{V_{IN}}\right) \quad (25)$$

Choose an inductor that does not saturate under the maximum peak inductor current ( $I_L$ ).

### Selecting the Input Capacitor ( $C_{IN}$ )

An input capacitor ( $C_{IN}$ ) is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to minimize noise on the IC. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors can also be used. For ceramic capacitors, the capacitance dominates the input voltage ripple ( $\Delta V_{IN}$ ) at the  $f_{SW}$ .

In flyback mode,  $\Delta V_{IN}$  can be estimated with Equation (26):

$$\Delta V_{IN} = I_{IN} \times \frac{V_{IN}}{f_{SW} \times C_{IN} \times (N \times V_{OUT} + V_{IN})} \quad (26)$$

In forward mode,  $\Delta V_{IN}$  can be estimated with Equation (27):

$$\Delta V_{IN} = \frac{I_{IN}}{f_{SW} \times C_{IN}} \times \left(1 - \frac{V_{OUT} \times N}{V_{IN}}\right) \quad (27)$$

### Selecting the Output Capacitor ( $C_{OUT}$ )

The output capacitor ( $C_{OUT}$ ) maintains the DC  $V_{OUT}$ . For the best results, use ceramic capacitors or low-ESR capacitors to minimize  $\Delta V_{OUT}$ .

When using ceramic capacitors, the capacitance dominates  $\Delta V_{OUT}$  at  $f_{SW}$ .

In flyback mode,  $\Delta V_{OUT}$  can be estimated with Equation (28):

$$\Delta V_{OUT} = \frac{N \times V_{OUT}}{(V_{IN} + N \times V_{OUT}) \times f_{SW}} \times \frac{I_{OUT}}{C_{OUT}} \quad (28)$$

If  $\Delta V_{OUT}$  is too high, a  $\pi$  filter is required. Choose the inductor to be between 0.1 $\mu$ H and 0.47 $\mu$ H.

In forward mode,  $\Delta V_{OUT}$  can be estimated with Equation (29):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT} \times N}{V_{IN}}\right) \quad (29)$$

## Design Examples

Table 4 shows a design example for a PSR flyback topology for the specifications below.

**Table 4: PSR Flyback Design Example**

<b>PoE Input</b>	36V to 57V
<b>V<sub>OUT</sub></b>	12V
<b>I<sub>OUT</sub></b>	2.1A

For the detailed application schematic, see Figure 19 on page 36. For more device applications, refer to the related evaluation board datasheet.

Table 5 shows a design example for forward applications.

**Table 5: SSR Forward Design Example**

<b>PoE Input</b>	36V to 57V
<b>Adapter Input</b>	48V
<b>V<sub>OUT</sub></b>	5V
<b>I<sub>OUT</sub></b>	4.8A

For the detailed application schematic, see Figure 21 on page 38. For more detailed device applications, refer to the related evaluation board datasheet.

## PCB Layout Guidelines

Efficient layout of the PoE front-end and high-frequency switching power supply is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 16, Figure 17, and Figure 18, and follow the guidelines below:

### PD Interface Circuit

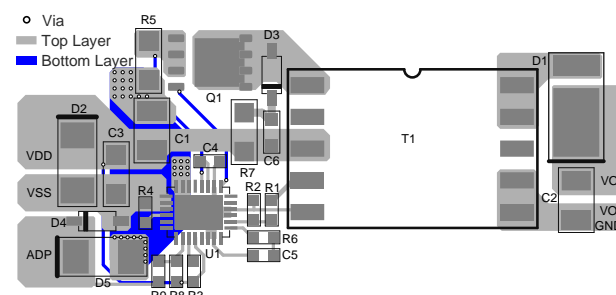
All component placements must follow the power flowing between RJ-45, the Ethernet transformer, the diode bridges, the TVS to 0.1μF capacitor, and the DC/DC converter input bulk capacitor. The spacing between VDD and VSS must comply with safety standards (e.g. IEC60950).

1. Keep all of the leads as short as possible using wide power traces.
2. Place the PD interface circuit ground planes so that they are referenced to VSS.
3. Place the switching converter ground planes so that they are referenced to RTN/GND.
4. Connect the exposed pad and GND. Do not connect the exposed pad to VSS.
5. Place the AUX resistor divider close to AUX if adapter power detection is enabled.

### Flyback Topology

1. To reduce noise and ringing, keep the input loop between the input bulk capacitor, transformer, MOSFET, sense resistor, and GND plane as short as possible.
2. Keep the output loop between the rectifier diode, output capacitor, and transformer as short as possible.
3. Keep the clamp loop circuit between D3, C6, and the transformer as short as possible.
4. Place the VCC capacitor close to the VCC and GND pins for the best decoupling.
5. Route the feedback trace away from noisy nodes, such as the switching node.
6. Place the COMP components close to the COMP pin.
7. Connect the power GND and signal GND using a single-point connection.

Figure 16 shows the recommended flyback layout for primary-side regulation. See the Typical Application section on page 2 for more details.

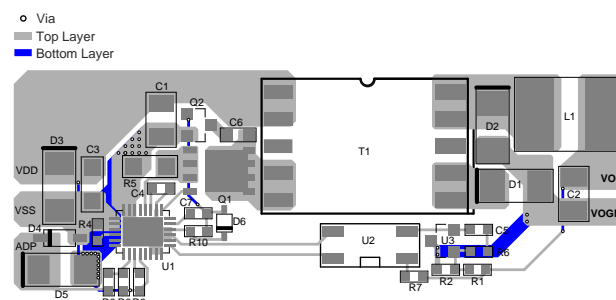


**Figure 16: Recommended PCB Layout for Flyback Topology**

### Forward Topology

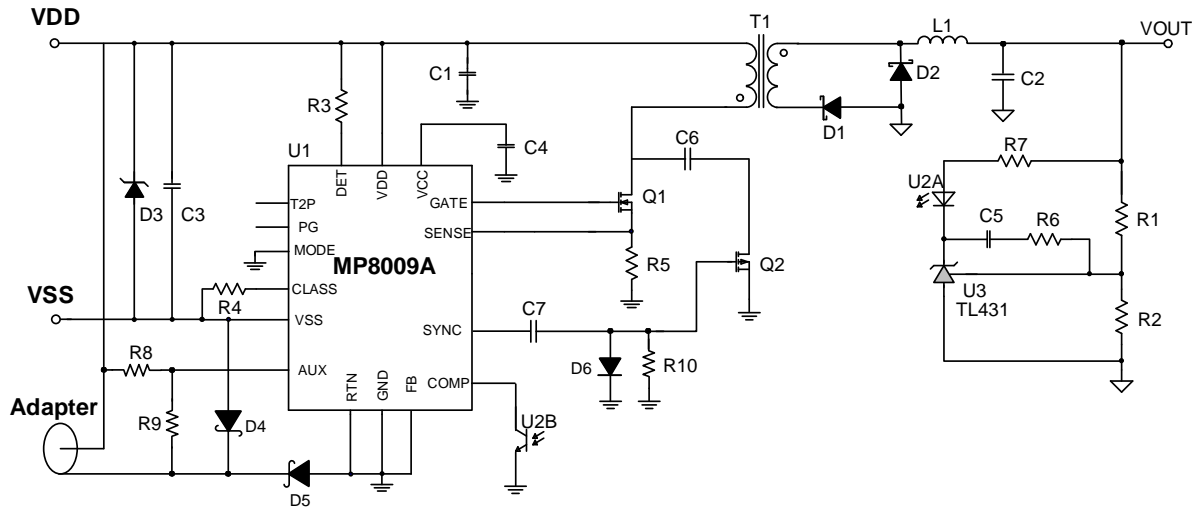
1. To reduce noise and ringing, keep the input loop between the input capacitor, transformer, Q1, and sense resistor as short as possible.
2. To reduce noise and ringing, keep the active-clamp loop between the input capacitor, transformer, C6, and Q2 as short as possible.
3. Keep the output high-frequency current loop between the transformers, D1, and D2 as short as possible.
4. Place the VCC capacitor close to the VCC and GND pins for the best decoupling.
5. Route the COMP feedback trace away from noisy nodes, such as the switching node.
6. Connect the power GND and signal GND using a single-point connection.

Figure 17 shows the recommended forward layout. For more details, refer to the related evaluation board datasheet.



**Figure 17: Recommended PCB Layout for Forward Topology**

Figure 18 shows the recommended schematic for a forward layout.



**Figure 18: Forward Layout Schematic**

# TYPICAL APPLICATION CIRCUITS

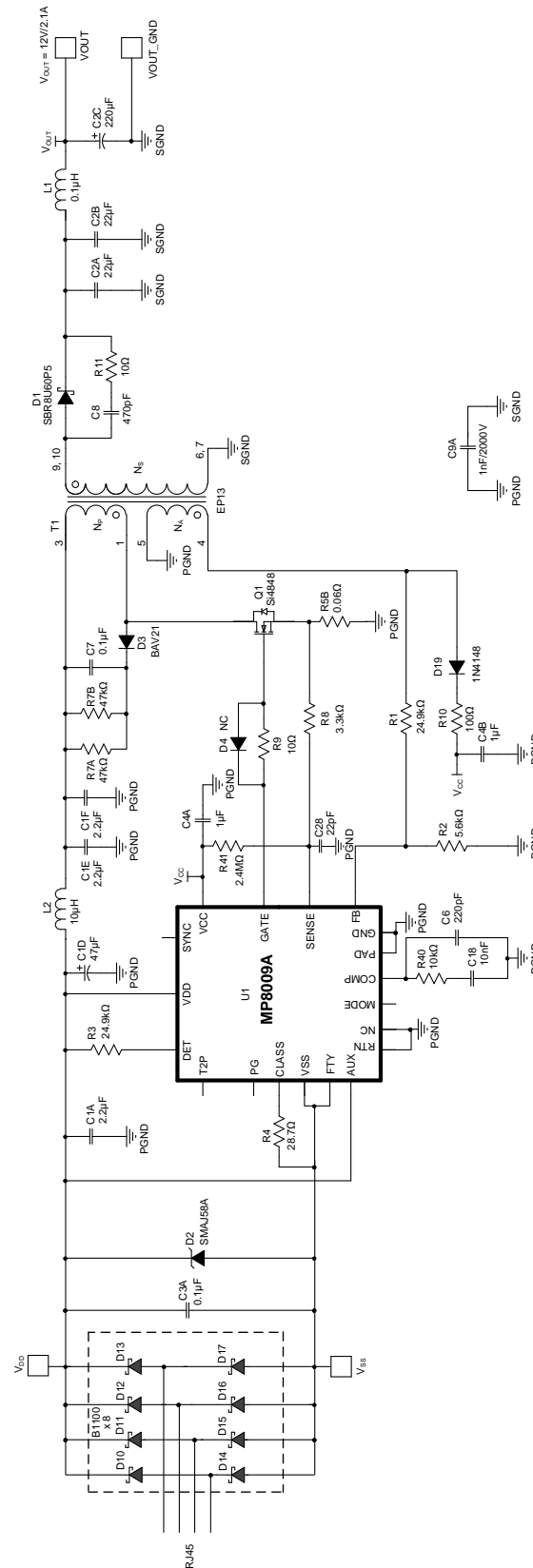
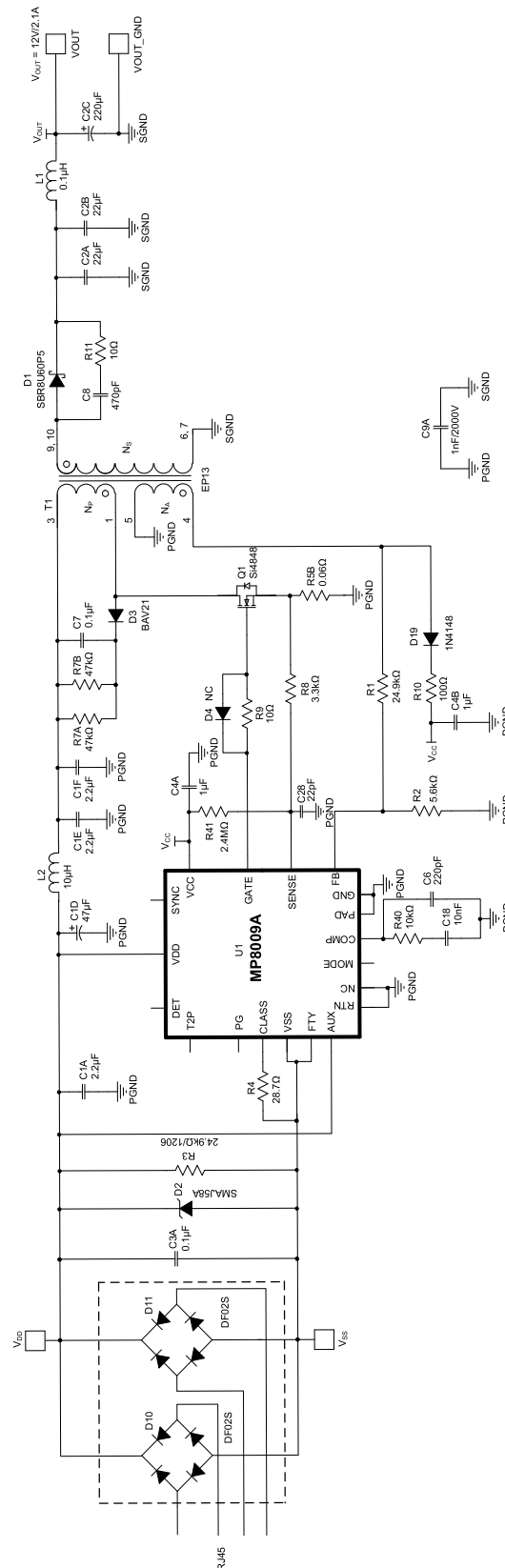


Figure 19: Typical Application Circuit with Schottky Diode Input Bridge



## TYPICAL APPLICATION CIRCUITS *(continued)*



**Figure 20: Typical Application Circuit with PN Junction Diode Input Bridge**

## TYPICAL APPLICATION CIRCUITS (continued)

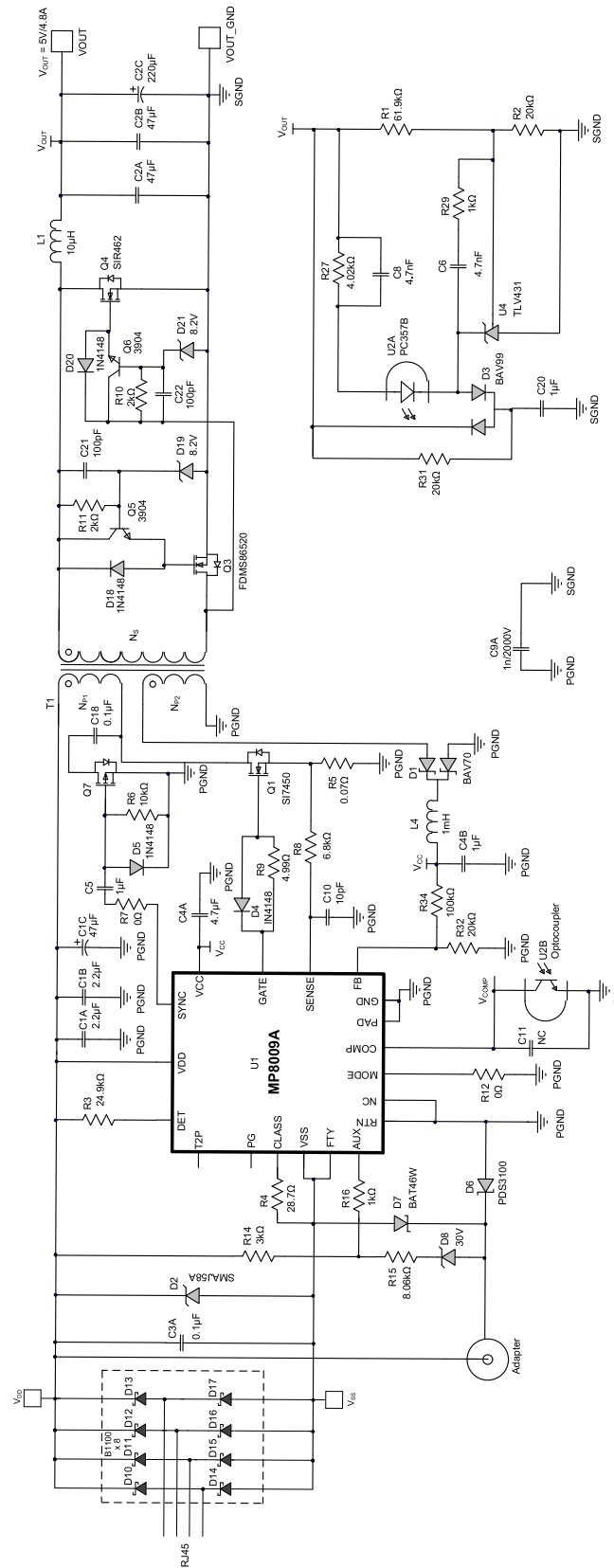
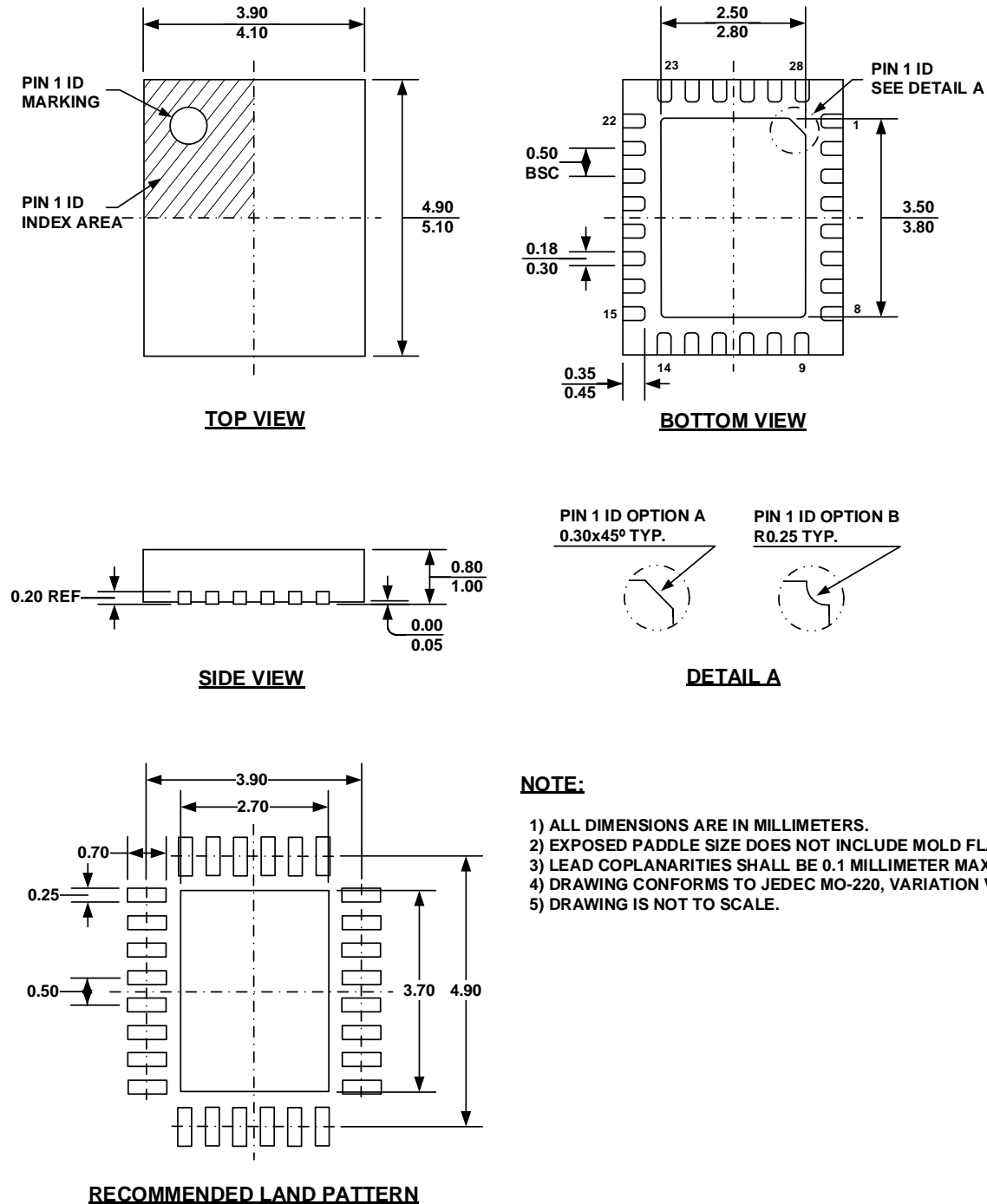


Figure 21: Typical Application Circuit for Forward Topology with PoE or 48V Adapter Input

# PACKAGE INFORMATION

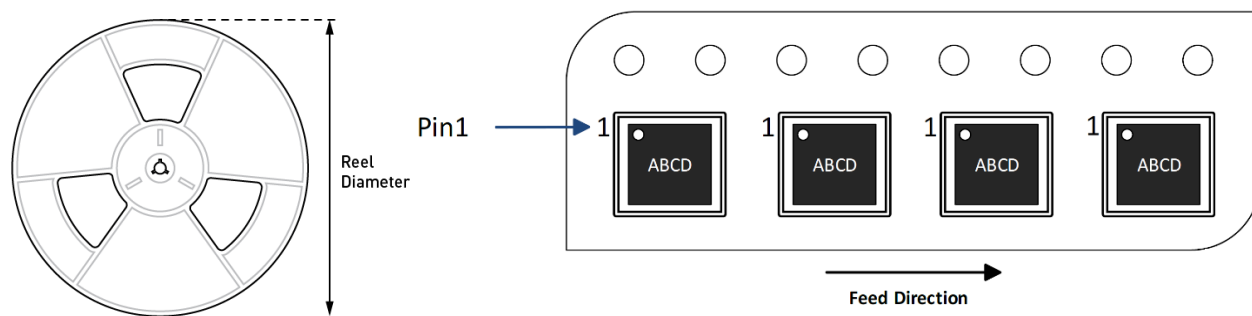
## QFN-28 (4mmx5mm)



### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITIES SHALL BE 0.1 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
- 5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8009AGV-Z	QFN-28 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/25/2022	Initial Release	-

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