MP8125

550mA, 8-14V Input, LNB Power Supply and Control Voltage Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP8125 is a voltage regulator designed to provide efficient, low noise power to the Satellite receiver's RF LNB (Low Noise Block) converter via coaxial cable through a DiSEqC 1.x compatible link that receives instructions from a dedicated controller.

The MP8125 integrates a current mode boost regulator followed by a tracking linear regulator. The boost regulator provides a clean and quiet power source that will not contaminate the low noise RF signal down converted to the receiver. The tracking linear regulator protects the output against overload or short.

The MP8125 provides a number of features described in the European EUTELSAT specification (DiSEqC) including: voltage selection of horizontal or vertical polarization directions of LNB and a selectable V_{OUT} compensation for voltage drop on the long coaxial cable. In accordance with DiSEqC standard, a tone signal of 22kHz is generated by an internal oscillator and can be activated or deactivated onto output by EXTM pin.

The MP8125 is available in thermally enhanced TSSOP16 and 24-pin QFN (4 x 4mm) packages.

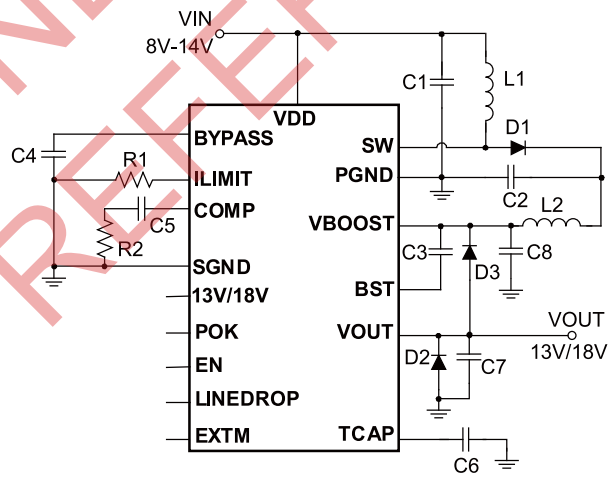
FEATURES

- DiSEqC 1.x Compatibility
- Up to 550mA Output Current
- 8V to 14V Input Voltage
- Boost Converter with Internal Switch
- Low Noise LDO Output
- Built-in 22kHz Tone Signal Generator
- Programmable Current Limit
- 1V Line Drop Compensation
- Adjustable Soft-start Time
- POK Indicator
- Short Circuit Protection
- Over Temperature Protection
- TSSOP16 Exposed Pad and 24-pin QFN (4 x 4mm) Packages

APPLICATIONS

- LNB Power Supply and Control for Satellite Set Top Boxes

TYPICAL APPLICATION

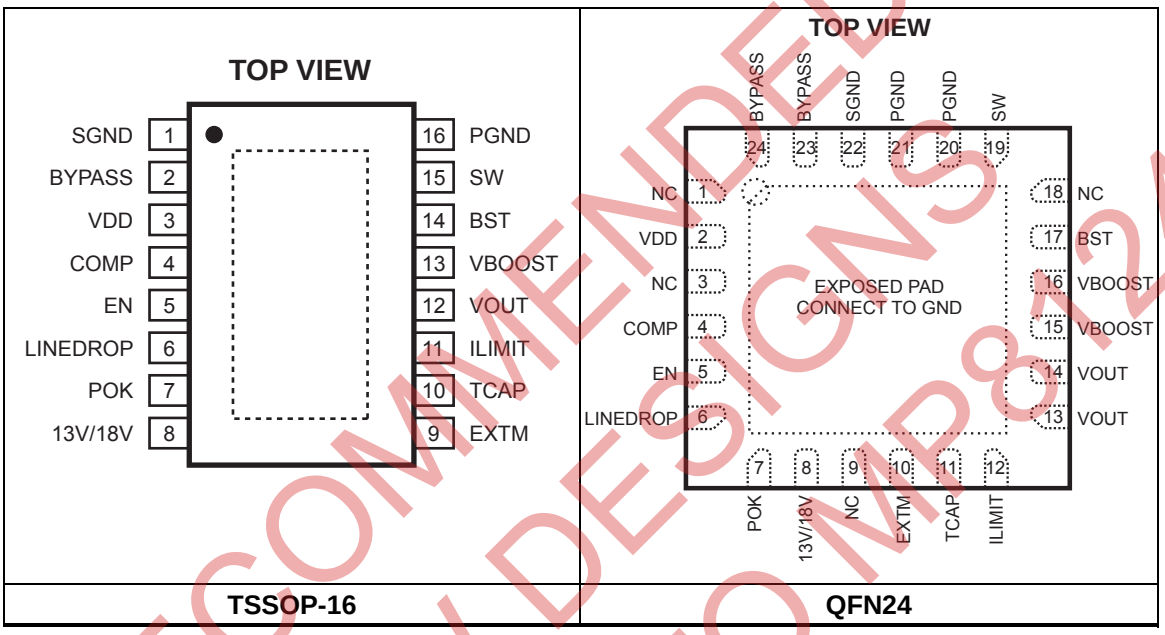


ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP8125EF*	TSSOP-16	MP8125	-20°C to +85°C
MP8125DR	QFN24(4x4mm)	MP8125	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP8125EF–Z).
For RoHS compliant packaging, add suffix –LF (e.g. MP8125EF–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

VDD .....-0.3V to 16V
VOUT, SW, VBOOST .....-0.3V to 25V
BST ..... V_{SW} +7V
All Other Pins .....-0.3V to 6.5 V
Continuous Power Dissipation.....(T_A=+25°C) (2)
TSSOP-16.....2.8W
QFN24(4x4mm).....2.9W
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to 150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....8V to 14V
Output Voltage V_{OUT}..... 13V/14V/18V/19V
Maximum Junction Temp. (T_J).....+125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP-16.....45 .....8.... °C/W
QFN24(4x4mm) .....42 .....9.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer PCB

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
General						
Input Voltage Range	V_{IN}		8	12	14	V
Input Supply Current (5)	I_{IN}	EN=High, no load		5		mA
Under Voltage Lockout	UVLO	V_{IN} rising	7		8	V
UVLO Hysteresis				350		mV
EN Input Logic Threshold	V_{EN_High}	V_{EN} rising			2	V
	V_{EN_Low}	V_{EN} falling	0.8			V
13V/18V Input Logic Threshold	$V_{13/18\_High}$	$V_{13V/18V}$ rising			2	V
	$V_{13/18\_Low}$	$V_{13V/18V}$ falling	0.8			V
LINEDROP Input Logic Threshold	V_{LD_High}	$V_{LINEDROP}$ rising			2	V
	V_{LD_Low}	$V_{LINEDROP}$ falling	0.8			V
TCAP pin current	I_{CHA}	TCAP capacitor charging		7		µA
Output Backward Leakage Current (6)	I_{BKLK}	EN=Low, V_{OUT} is clamped to 24V, VBOOST is float		0.7	1	mA
Voltage on BYPASS pin	V_{BYP}			5		V
SWITCHING REGULATOR						
Boost Switch On Resistance (5)	R_{DSON}	I_{OUT} =500mA		500		mΩ
Boost Frequency				352		kHz
LINEAR REGULATOR						
Dropout Voltage (5)		V_{BOOST}-V_{OUT}, I_{OUT}=500mA		0.9		V
OUTPUT						
Output Voltage	V_{OUT}	LINEDROP=Low, 13V/18V=Low, I_{OUT} =10-100mA	12.8	13.2	13.6	V
		LINEDROP=Low, 13V/18V=High, I_{OUT} =10-100mA	17.6	18.14	18.7	V
		LINEDROP=High, 13V/18V=Low, I_{OUT} =10-100mA	13.72	14.2	14.58	V
		LINEDROP=High, 13V/18V=High, I_{OUT} =10-100mA	18.57	19.14	19.73	V
Output Line Regulation		8V≤V_{IN}≤14V; I_{OUT}=100mA		4	40	mV
Output Load Regulation (5)		10mA≤I_{OUT}≤500mA, 13V/18V=Low		20		mV
		10mA≤I_{OUT}≤500mA, 13V/18V=High		30		mV

ELECTRICAL CHARACTERISTICS (*continued*)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
TONE Signal						
Tone Signal Frequency	f_{TONE}	T_A = 25°C	20	22	24	kHz
EXTM Input Logic Threshold	V_{EXTM_High}	V_{EXTM} rising			2	V
	V_{EXTM_Low}	V_{EXTM} falling	0.8			V
Delay Time of Tone Signal Activated or Deactivated (5)	t_{DELAY}	Delay time after EXTM goes high or low		$\frac{1.5}{f_{TONE}}$		
Peak-to-Peak Amplitude	V_{PP}	I_{LOAD} = 0 to 100mA	0.55	0.65	0.9	V
Rise and Fall Time		R_L=1kΩ, C_L=0.1μF		8		μs
Over-Current Protection						
Output Current Limit	I_{LIMIT}	R_{LIMIT}=10kΩ	600	850	1100	mA
Dynamic Overload Protection Off Time	T_{OFF}	Time of attempt to restart		2		s
Dynamic Overload Protection On Time	T_{ON}	Time to onset of shutdown		50		ms
POK						
POK Upper Trip Threshold (5)		V_{FB} with Respect to Nominal		12		%
POK Lower Trip Threshold		V_{FB} with Respect to Nominal		-12		%
POK Output Lower Voltage		I_{SINK} = 5mA			0.3	V
Thermal Protection						
Over Temperature Shutdown (5)				150		°C
OTP Hysteresis				20		°C

Note:
5) Guaranteed by design.
6) Shall withstand the back voltage for an indefinite period of time. On removal of the fault condition the device returns to normal operation

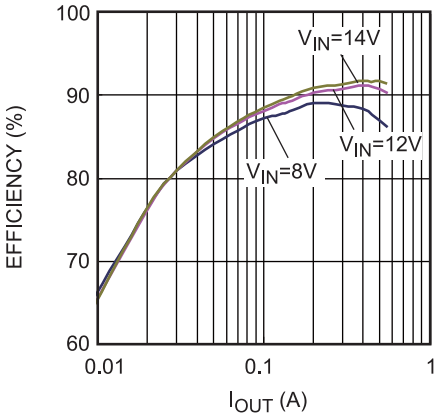
PIN FUNCTIONS

Pin # TSSOP-16	Pin # QFN24	Name	Description
1	22	SGND	Analog ground.
2	23, 24	BYPASS	Connect a bypass capacitor for the internal regulator.
3	2	VDD	Input supply pin.
4	4	COMP	Compensation pin for Boost regulator (47nF & 19.6kΩ is suggested).
5	5	EN	Regulator On/Off Control Input. When this pin is low, the output is disabled. A high level at EN turns on the converter. Connect EN to the input source (through a 100kΩ pull-up resistor if VIN > 6V) for automatic startup. EN cannot be left floating.
6	6	LINEDROP	This pin provides selectable V_{OUT} compensation for voltage drop on the long coaxial cable. When the LINEDROP is high, the LDO output is 1V increased. LINEDROP cannot be left floating.
7	7	POK	Power OK. A high output indicates that LDO output is within ±12% of nominal value. A low output means that LDO output is outside this window.
8	8	13V/18V	Select 13V or 18V for output voltage. High level for 18V while low level for 13V. This pin cannot be left floating.
9	10	EXTM	External modulation input for 22kHz signaling. A high level at EXTM turns on 22kHz signal and a low level disables it. EXTM cannot be left floating.
10	11	TCAP	Internal voltage reference for LDO output, A soft-start capacitor can be connected to this pin to set rise time of the output voltage. The capacitor should be very close to this pin and SGND, and the route should keeps far away from any noise like SW copper.
11	12	ILIMIT	The ILIMIT is used to set the value of the output current limit of LDO. A resistor from ILIMIT to GND programs the limit.
12	13, 14	VOUT	Output voltage.
13	15, 16	VBOOST	Input of the internal LDO.
14	17	BST	Supply for the internal LDO driver.
15	19	SW	SW is the drain of the internal MOSFET switch of Boost stage. Connect the power inductor and output rectifier to SW.
16	20, 21	PGND	Power ground.
	1, 3, 9, 18	NC	Not Connect.

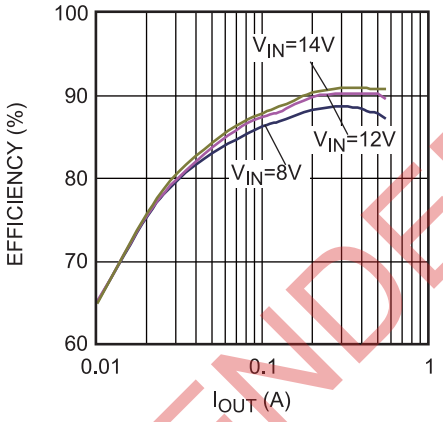
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the DESIGN EXAMPLE section.
V_{IN} =12V, $V_{LINEDROP}$=5V, V_{EXTM}=0V, T_A = +25ºC, unless otherwise noted.

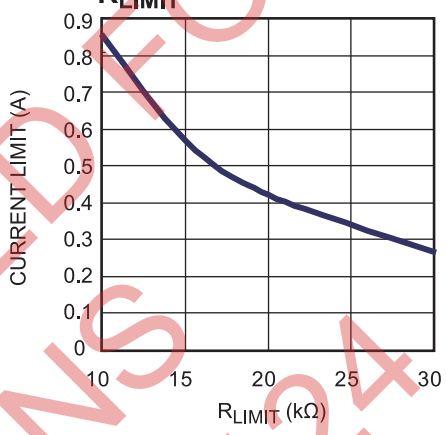
Efficiency Curve @ V_{OUT}=19V



Efficiency Curve @ V_{OUT}=14V



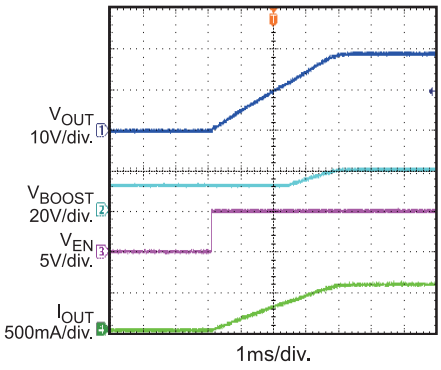
Current Limit vs. R_{LIMIT}



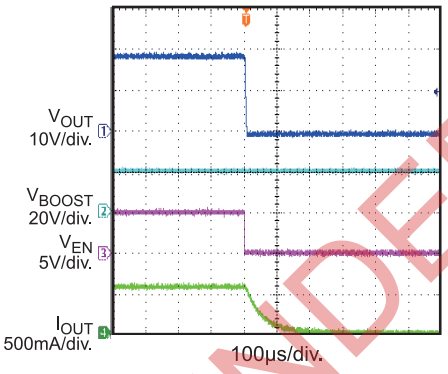
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the DESIGN EXAMPLE section.
V_{IN} =12V, $V_{LINEDROP}$=5V, V_{EXTM}=0V, I_{OUT}=0.55A, T_A = +25°C, unless otherwise noted.

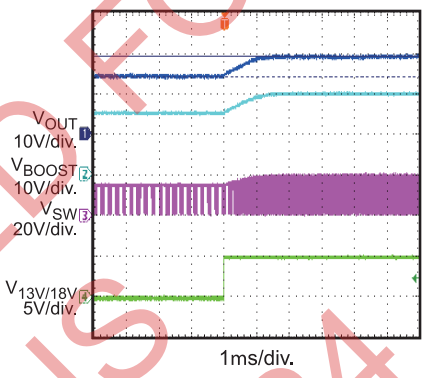
EN Startup



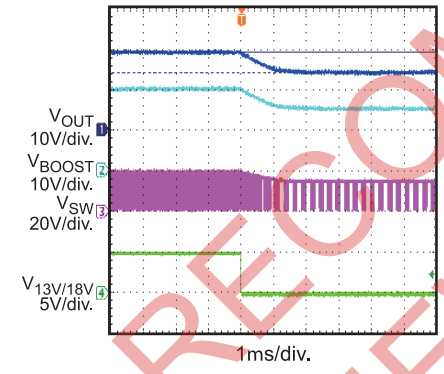
EN Shutdown



13V to 18V Switching

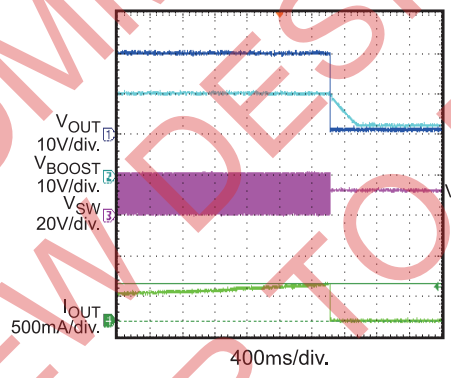


18V to 13V Switching



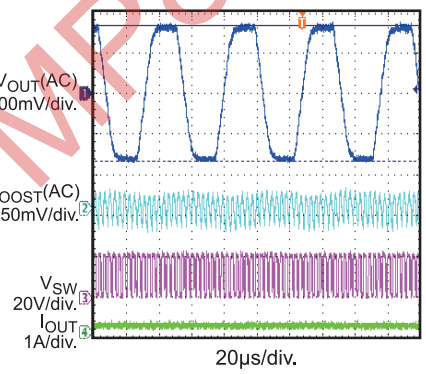
Current Limit Protection

R_{LIMIT} = 20kΩ

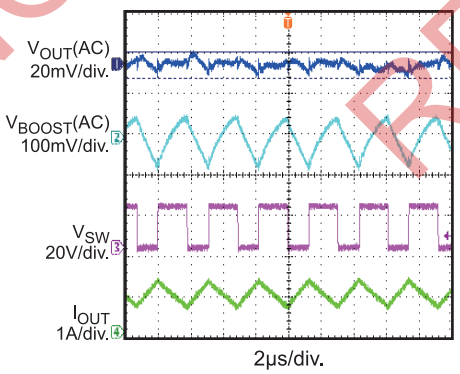


22kHz Tone Signal

V_{EXTM} = 5V, I_{OUT} = 0.1A



Output Ripple



BLOCK DIAGRAM

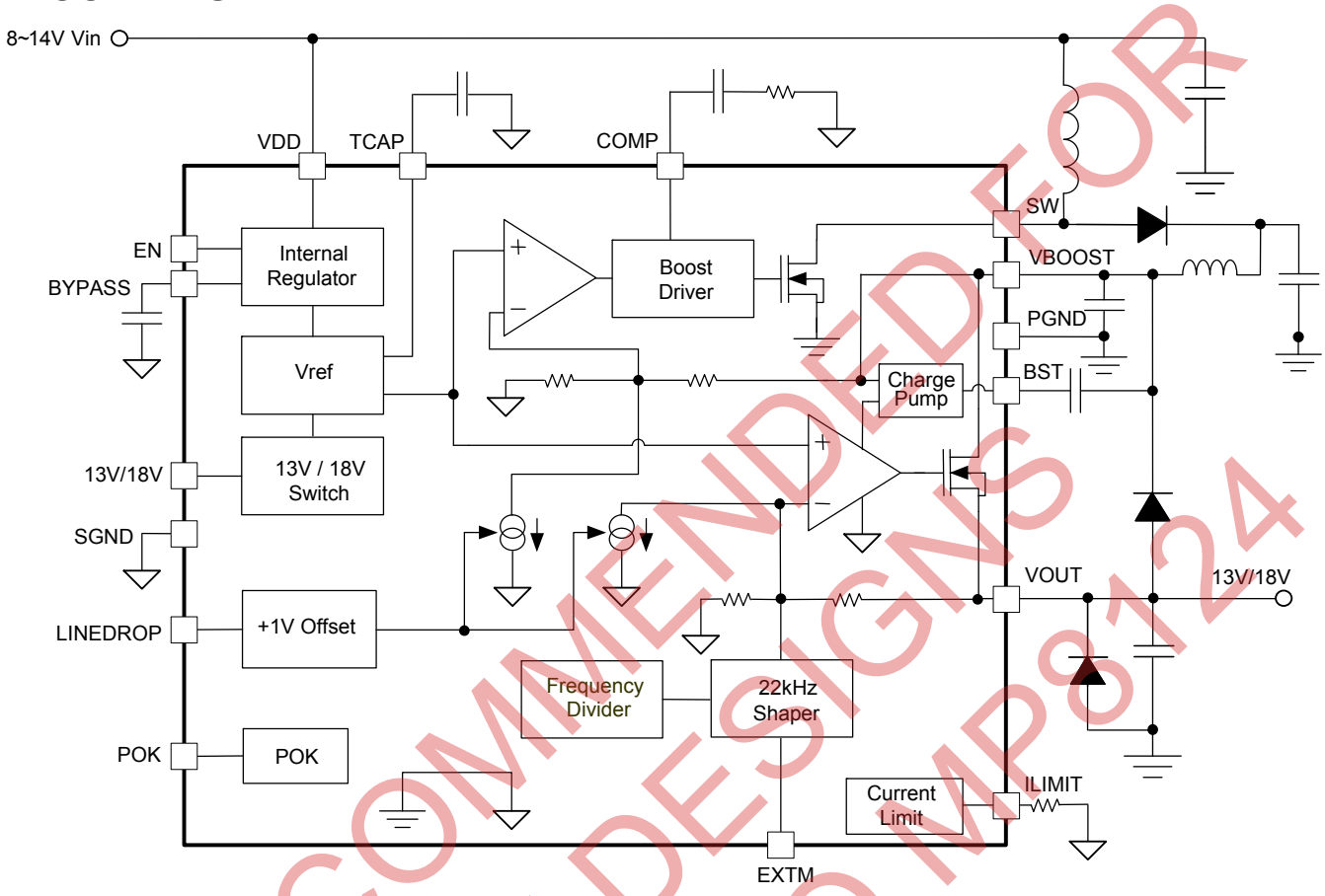


Figure 1—Internal Function Block Diagram

OPERATION

The MP8125 is a single output voltage regulator for providing both supply voltage and control signal from satellite set-top box modules to LNB (low noise block) of the antenna port.

The MP8125 has an integrated boost converter that, from a single supply source between 8V and 14V, generates the voltage to enable the linear post-regulator to work at a minimum dissipated power.

Boost Converter/Linear Regulator

The boost converter is a fixed frequency, non-synchronous voltage regulator with peak current mode control. The operating frequency is 352kHz typically, which is 16 times the 22kHz internal tone frequency.

To reduce power dissipation, the boost converter operates in a pulse-skipping mode at light load.

The output voltage of boost converter tracks the requested output voltage to allow the linear regulator to work with minimum drop-out voltage.

13V/18V Switching

With the logic input pin 13V/18V, the output voltage can be set to 13V or 18V to select different polarization directions of LNB. A logic high level on this pin will set the output to 18V while a low level set it to 13V.

LINEDROP Control

In order to compensate the excess of voltage drop along the coaxial cable, a voltage compensation function is integrated. If set a high level on LINEDROP pin, the output voltage can be increased by 1 V. A low level will disable the function.

Soft Start

Soft start is implemented via external capacitor (C_{SS}). With the required slew rate (k) of the output voltage, the value of C_{SS} can be obtained using the following formula:

$$C_{SS} = (15 \times I_{CHA}) / k$$

Where I_{CHA} is 7 μA typ.

Current Limit

The output current is limited dynamically and the threshold can be programmed by an external resistor connected to the ILIMIT pin according to the following formula:

$$I_{LIMIT} = 8500 / R_{LIMIT}$$

When an overload is detected, the output current will be regulated at the current limit level for 50 ms. After this time period, if the overload is still detected, the output will be shut down for 2s before the output is resumed.

For the boost converter, it integrates cycle-by-cycle over current limit function, which can guarantee the part works with full load.

Power Good (POK)

POK is connected to an internally open-drain device. When output voltage is out of +/- 12% of normal value, POK will be pulled down. Otherwise, it will be pulled high.

Tone Generation

In accordance with DiSEqC standards, a tone signal of 22kHz is generated by an internal oscillator and activated/deactivated by EXTM pin. A high level on EXTM activates the internal tone signal and modulates it onto the output to provide the LNB control information. A low level will deactivate the 22kHz signal.

The tone signal will be activated or deactivated onto the output within 1.5 periods after EXTM goes high or low. Please refer to the Figure 2 (T is the period of tone signal.).

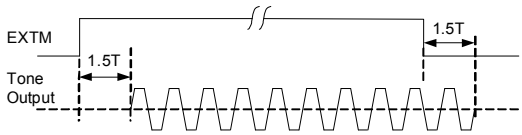


Figure 2—Tone Signal on Output

Thermal Protection

When the junction temperature exceeds +150°C, the part will be shut down. Once the junction temperature is cooled enough, typically 130°C, the part will re-start automatically.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Input Capacitor

The input capacitor (C1) is required to maintain the DC input voltage. Ceramic capacitors with low ESR/ESL types are recommended. The input voltage ripple can be estimated by the below formula. Typically, a 10μF X7R ceramic capacitor is recommended.

$$\Delta V_{IN} = \frac{V_{IN}}{8f_s^2 \cdot L \cdot C1} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Setting the Output Capacitor of Boost Converter

The output current to the step-up converter is discontinuous, therefore a capacitor is essential to supply the AC current to the load. Use low ESR capacitors for the best performance. The output voltage ripple can be estimated by the below formula.

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot R_L \cdot C2} \cdot \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Where R_L is the value of load resistor.

Ceramic capacitors with X7R dielectrics are highly recommended because of their low ESR and small temperature coefficient. Typically, a 22μF X7R ceramic capacitor is recommended.

Selecting the Inductor of Boost Converter

An inductor with a DC current rating of at least 25% higher than the maximum load current is recommended. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{IN}(V_{OUT} - V_{IN})}{f_s \cdot V_{OUT} \cdot \Delta I_L}$$

Where ΔI_L is the inductor ripple current. Choose inductor ripple current to be approximately 30% of the maximum load current.

Selecting the Rectifier Diode of Boost Converter

The high switching frequency demands high-speed rectifiers. Schottky diodes are recommended for most applications because of the fast recovery time and low forward voltage. Typically, a 2A Schottky diode is recommended for the boost converter.

DESIGN EXAMPLE

Below is a design example following the application guidelines for the specifications:

V_{IN}	12V
V_{OUT}	19V

The detailed application schematic is shown in Figure 3. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheet.

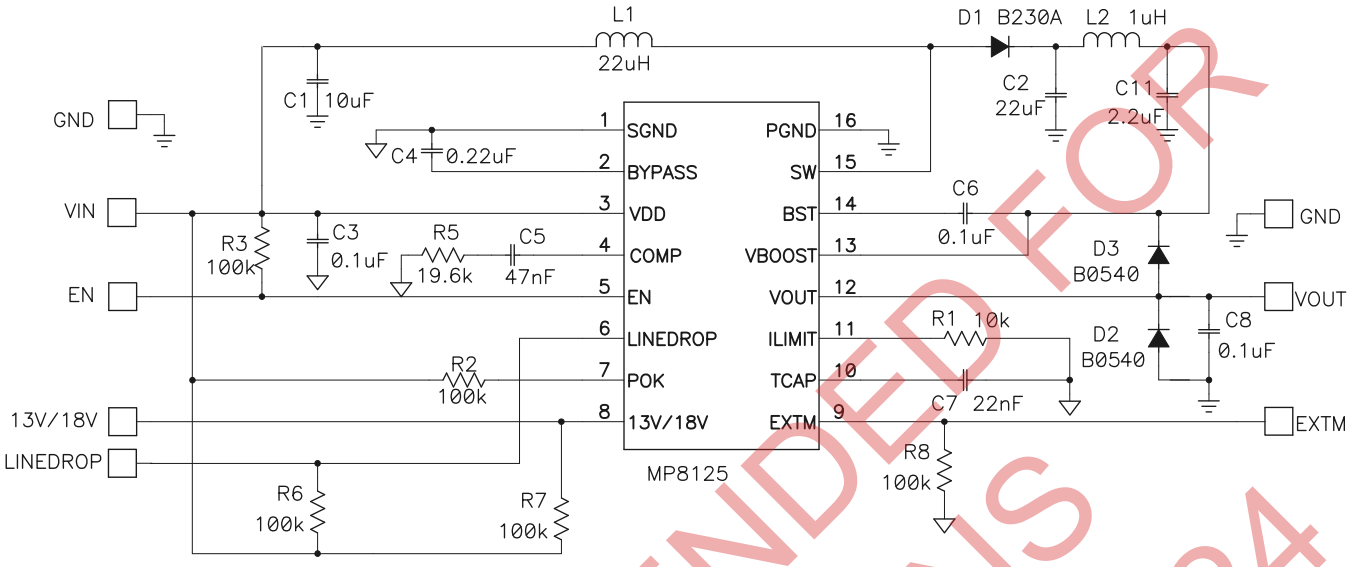
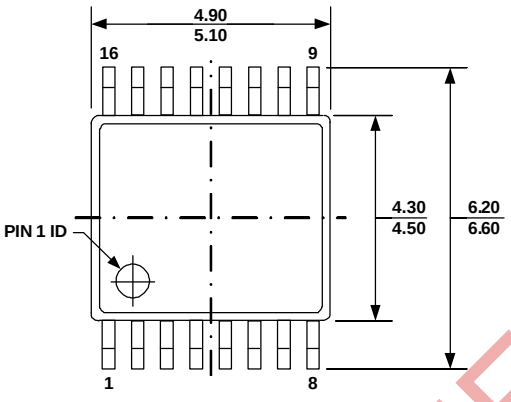


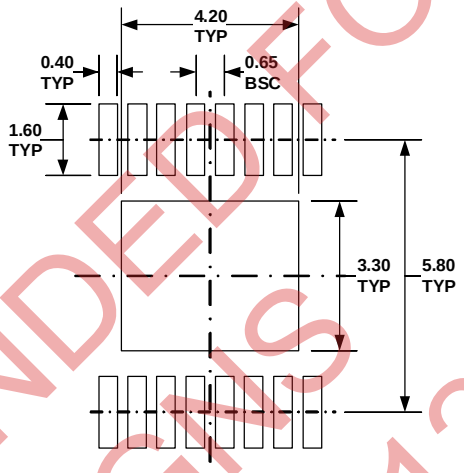
Figure 3—Detailed Application Schematic

PACKAGE INFORMATION

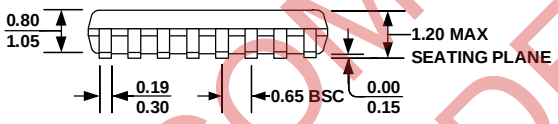
TSSOP16



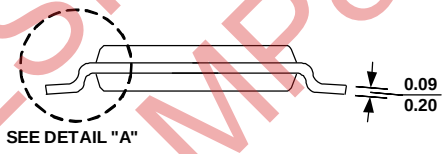
TOP VIEW



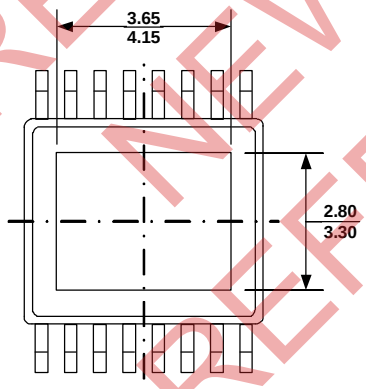
RECOMMENDED LAND PATTERN



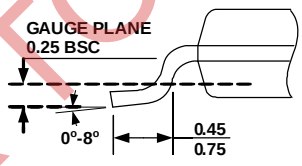
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

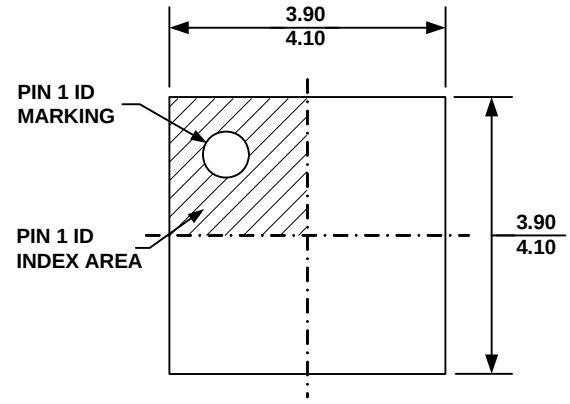


DETAIL "A"

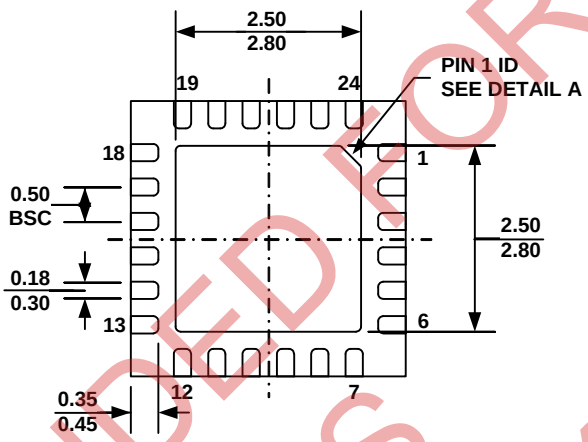
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6) DRAWING IS NOT TO SCALE

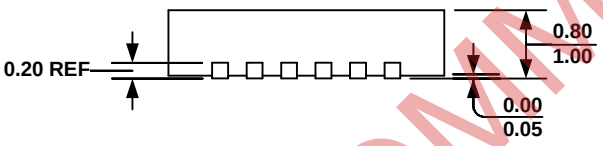
QFN24 (4X4mm)



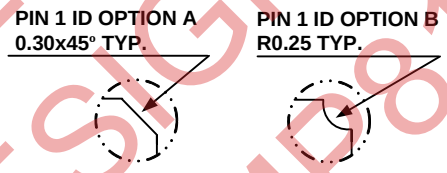
TOP VIEW



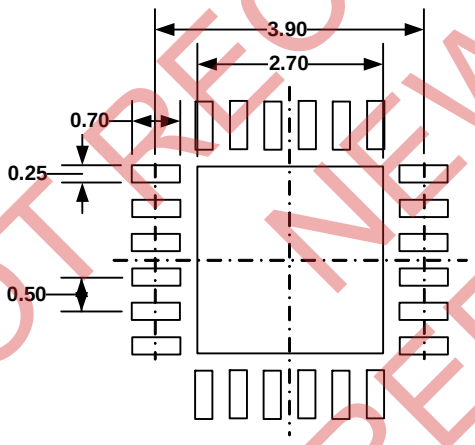
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGGD.
5) DRAWING IS NOT TO SCALE.