MP8772

12A, 17V, 700kHz Synchronous Step-down Converter with PG and External Soft Start in 3x3mm QFN package

DESCRIPTION

The MP8772 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP8772 offers a very compact solution that achieves 12A of continuous output current with excellent load and line regulation over a wide input range. The MP8772 uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP8772 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-16 (3mmx3mm) package.

FEATURES

- Output Adjustable from 0.6V
- Wide 3V to 17V Operating Input Range
- 12A Output Current
- 16mΩ/5.5mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 100μA Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Fixed 700kHz Switching Frequency
- External Programmable Soft Start-Up Time
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purpose

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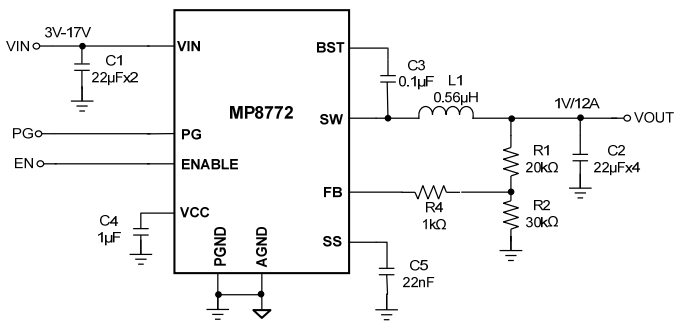
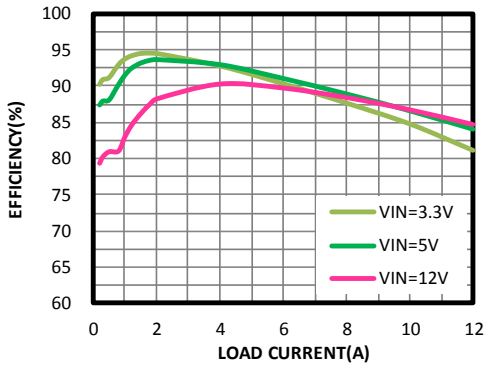
TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.56μH, DCR = 1.5mΩ



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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8772GQ	QFN-16 (3mmx3mm)	*See Below*

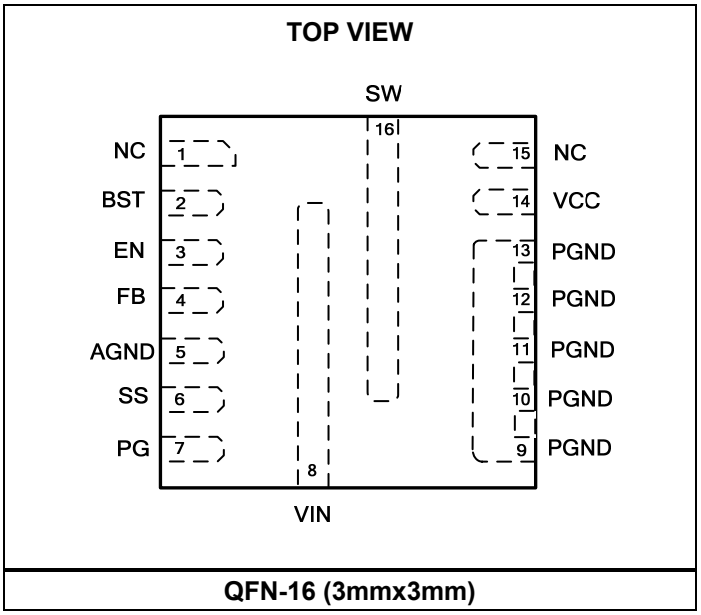
* For Tape & Reel, add suffix –Z (e.g.: MP8772GQ–Z)

TOP MARKING

BABY
LLL

BAB: Product code of MP8772GQ
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



QFN-16 (3mmx3mm)

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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} ..... -0.3V to +20V
V_{SW} ..... -0.3V (-5V < 10ns) to V_{IN} + 0.7V (23V < 10ns)
V_{BST} ..... V_{SW} + 4V
V_{EN} ..... V_{IN}
All other pins ..... -0.3V to +4V
Continuous power dissipation (T_A = +25°C) (2) 3.2W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to 125°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3V to 17V
Output voltage (V_{OUT}) ..... 0.6V to V_{IN} * D_{MAX} or 12V max
Operating junction temp. (T_J) .... -40°C to +125°C

Thermal Resistance	θ_{JA}	θ_{JC}	
QFN-16 (3mmx3mm)			
EV8772-Q-00A(4)	38	10	°C/W
JESD51-7 (5)	50	12	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation on EV8772-Q-00A board at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV8772-Q-00A, 4-layer PCB.
5) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		17	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			5	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	μA
MOSFET						
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		16		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		5.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 17V, T_J = 25°C			1	μA
Current Limit and ZCD						
Valley current limit	I_{LIMIT_VY}		12	14		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
ZCD	I_{ZCD}			200		mA
Switching Frequency and Minimum On/Off Timer						
Switching frequency	Fs		600	700	800	kHz
Minimum on time (7)	$T_{On\ MIN}$			50		ns
Minimum off time (7)	$T_{Off\ MIN}$			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	μA
Enable and UVLO						
EN rising threshold	$V_{EN\ RISING}$		1.1	1.25	1.4	V
EN falling threshold	$V_{EN\ FALLING}$		0.9	1	1.1	V
EN pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.6	2.8	3.0	V
VCC under-voltage lockout threshold	VCC_{HYS}			350		mV
VCC regulator	V_{CC}			3.4		V
VCC load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%

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ELECTRICAL CHARACTERISTICS (6) *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power good UV rising threshold	$PGUV_{vth_Hi}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{vth_Lo}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{vth_Hi}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{vth_Lo}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{Td}	Both edge		50		µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	µA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD-HYS}			20		°C

NOTES:

6) Guaranteed by over-temperature correlation, not tested in production.

7) Guaranteed by design and characterization test.

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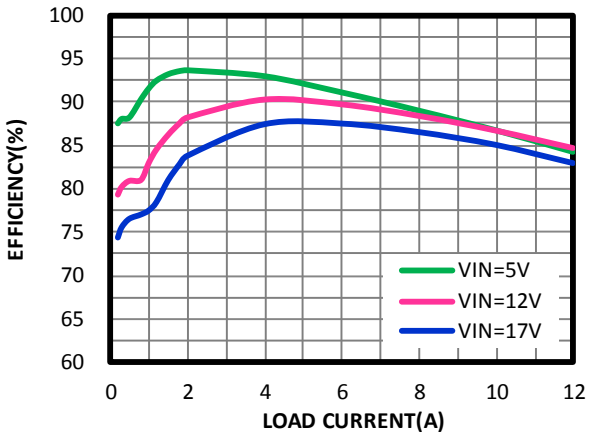
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

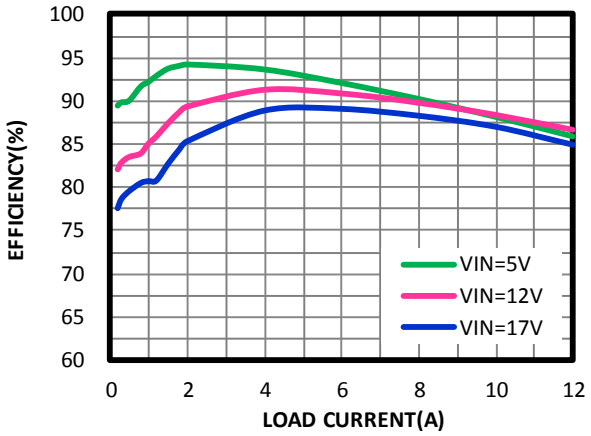
Efficiency vs. Load Current

V_{OUT} = 1V, L = 0.56µH, DCR = 1.5mΩ



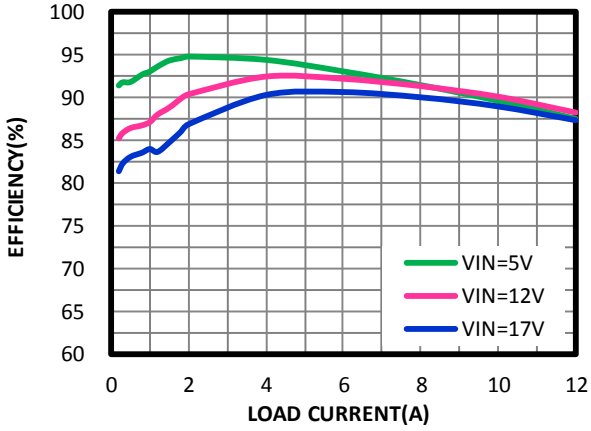
Efficiency vs. Load Current

V_{OUT} = 1.2V, L = 0.56µH, DCR = 1.5mΩ



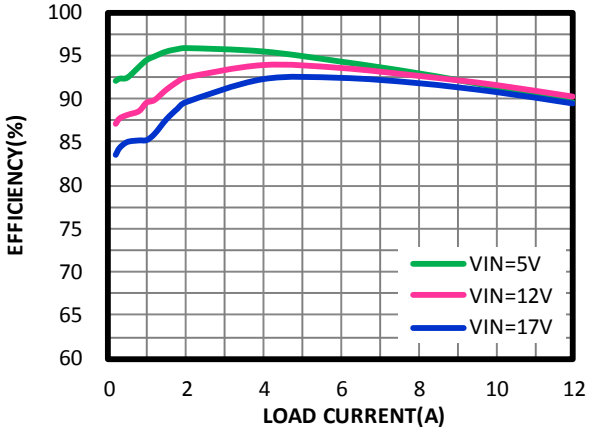
Efficiency vs. Load Current

V_{OUT} = 1.5V, L = 0.56µH, DCR = 1.5mΩ



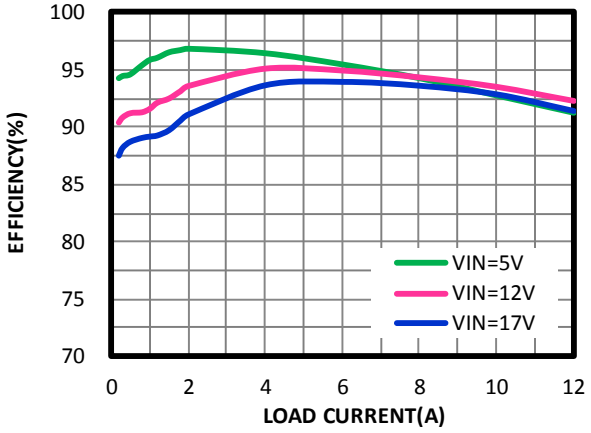
Efficiency vs. Load Current

V_{OUT} = 1.8V, L = 0.82µH, DCR = 0.9mΩ



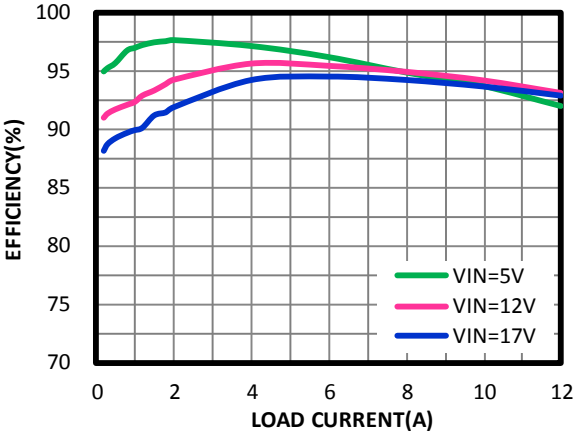
Efficiency vs. Load Current

V_{OUT} = 2.5V, L = 0.82µH, DCR = 0.9mΩ



Efficiency vs. Load Current

V_{OUT} = 3.3V, L = 1µH, DCR = 1.35mΩ



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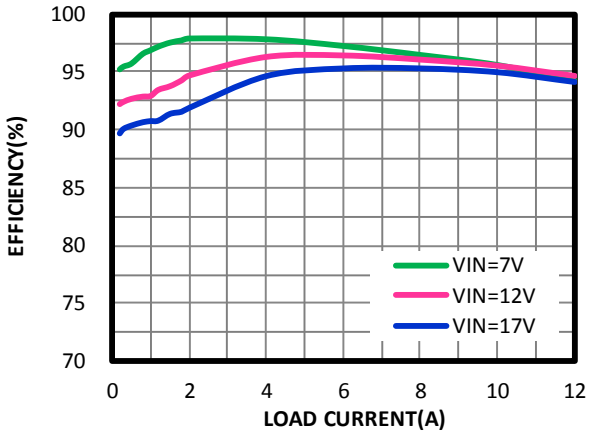
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

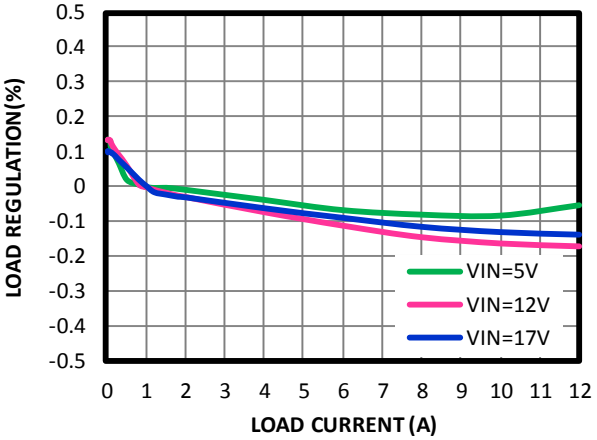
Efficiency vs. Load Current

V_{OUT} = 5V, L = 1.2µH, DCR = 1.8mΩ



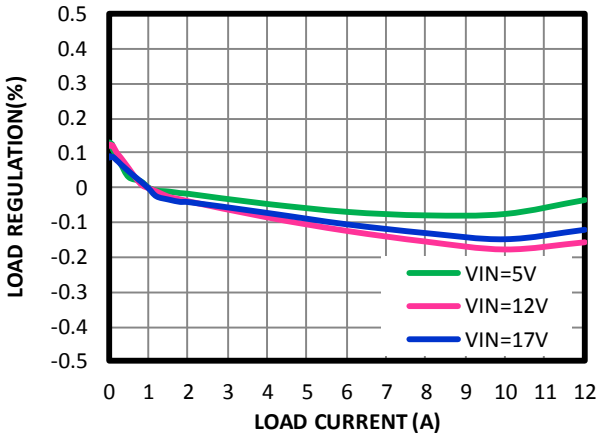
Load Regulation vs. Load Current

V_{OUT} = 1V



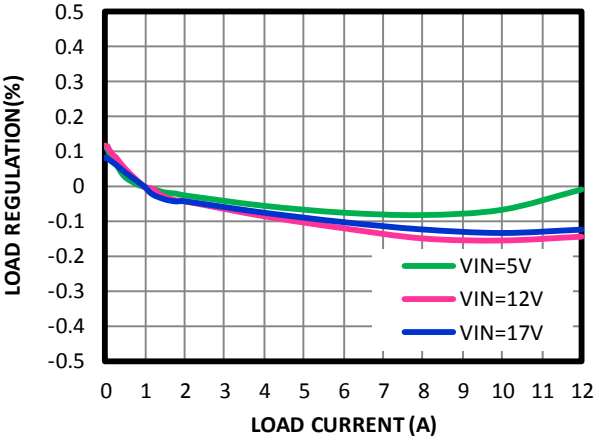
Load Regulation vs. Load Current

V_{OUT} = 1.2V



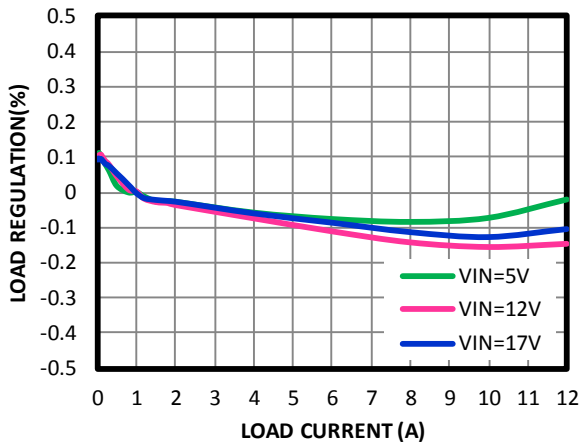
Load Regulation vs. Load Current

V_{OUT} = 1.5V



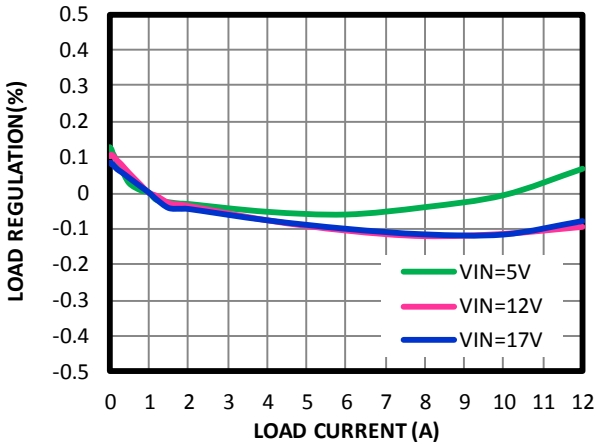
Load Regulation vs. Load Current

V_{OUT} = 1.8V



Load Regulation vs. Load Current

V_{OUT} = 2.5V



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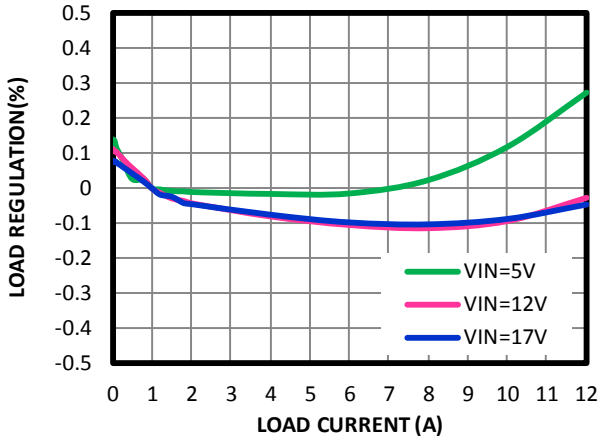
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

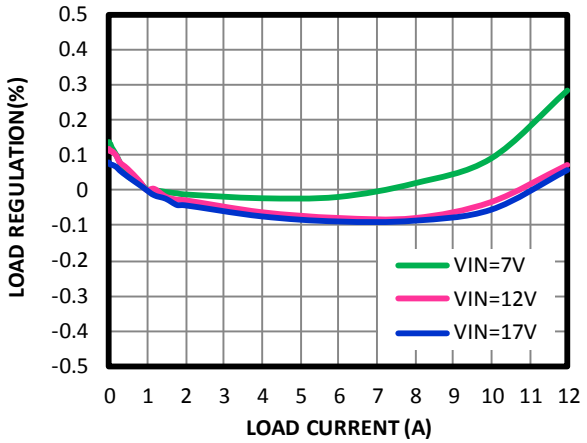
Load Regulation vs. Load Current

V_{OUT} = 3.3V

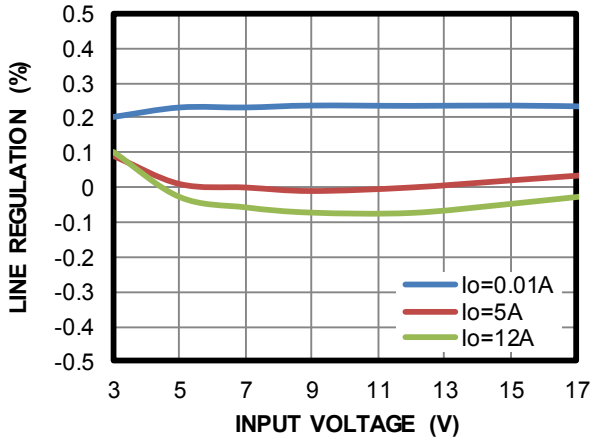


Load Regulation vs. Load Current

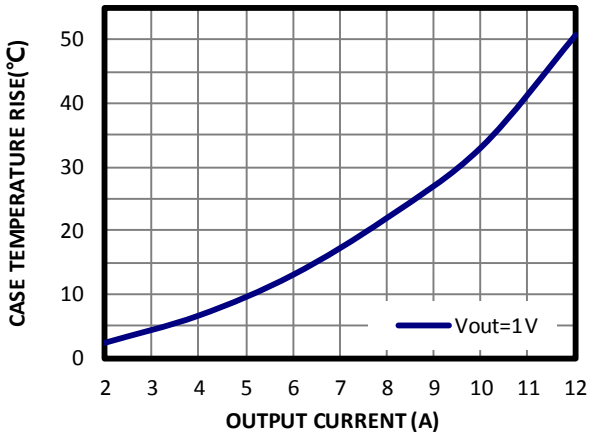
V_{OUT} = 5V



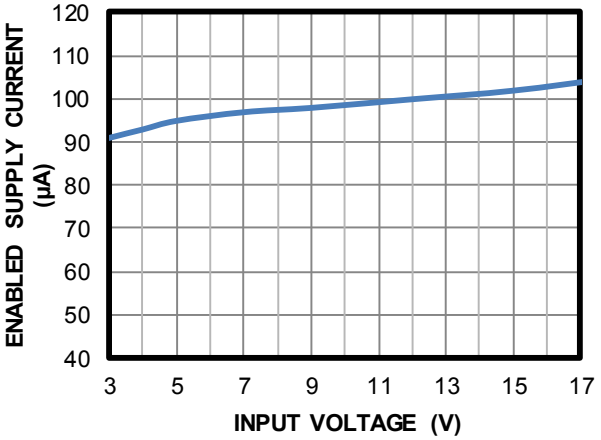
Line Regulation vs. Input Voltage



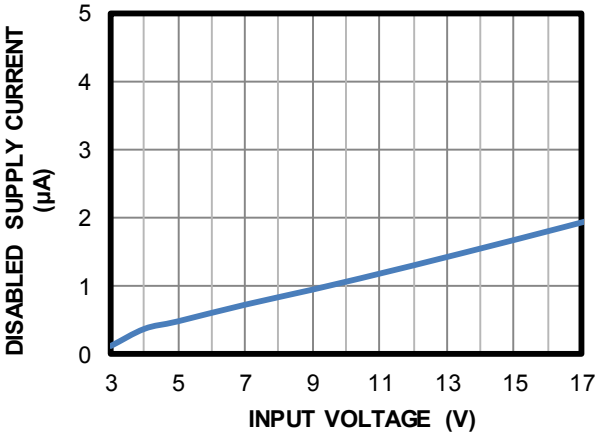
Case Temperature Rise vs. Output Current



Enabled Supply Current vs. Input Voltage



Disabled Supply Current vs. Input Voltage



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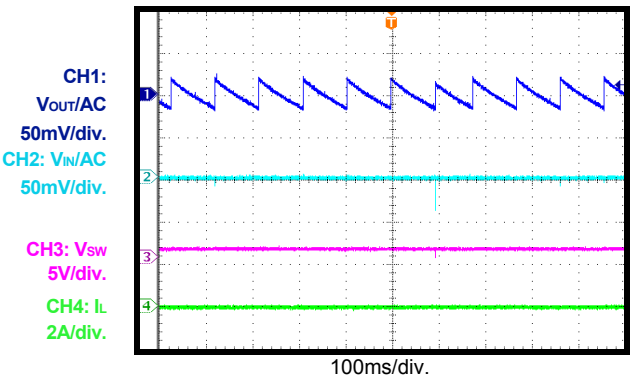
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

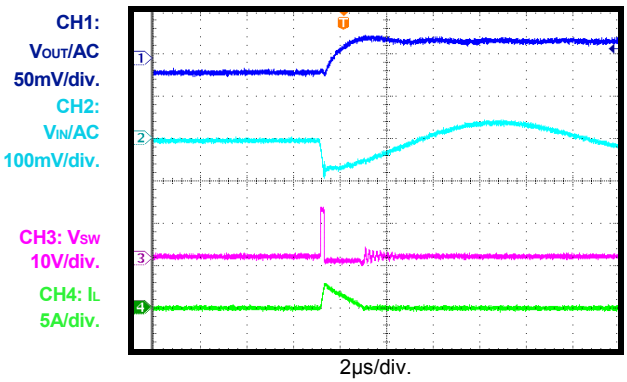
Input/Output Ripple

I_{OUT} = 0A



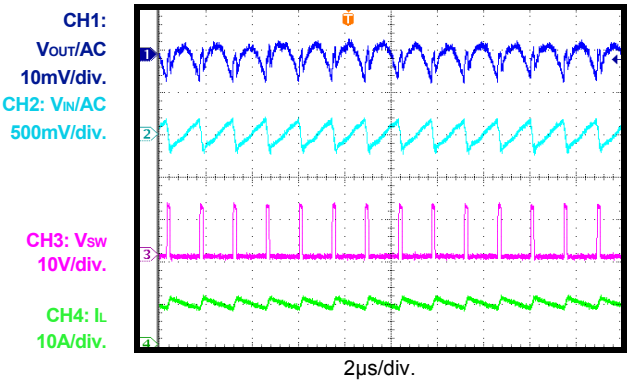
Input/Output Ripple

I_{OUT} = 0A



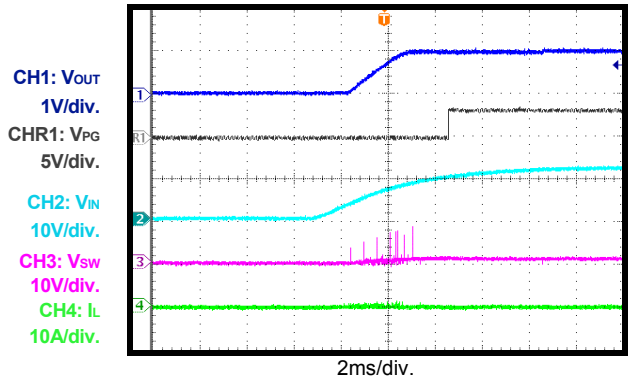
Input/Output Ripple

I_{OUT} = 12A



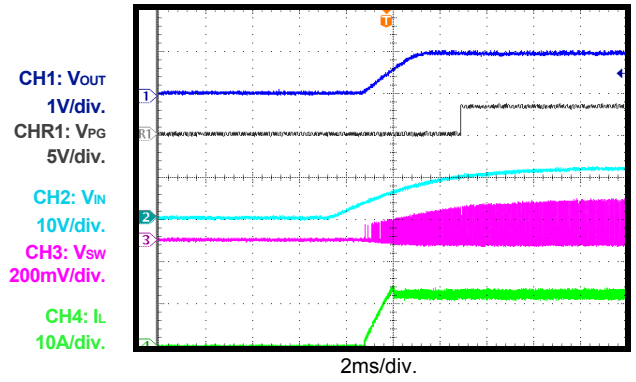
Start-Up through Input Voltage

I_{OUT} = 0A



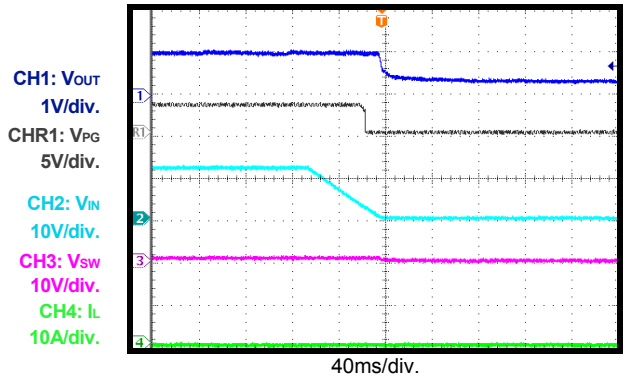
Start-Up through Input Voltage

I_{OUT} = 12A



Shutdown through Input Voltage

I_{OUT} = 0A



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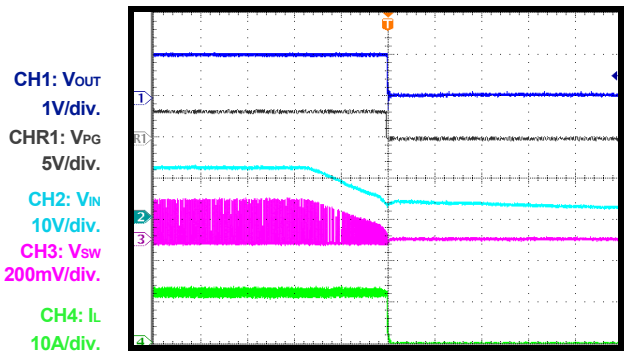
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

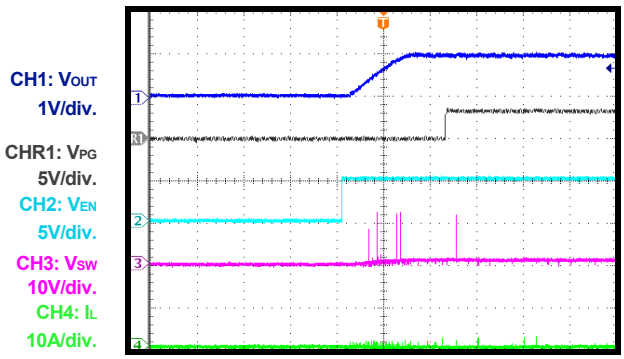
Shutdown through Input Voltage

I_{OUT} = 12A



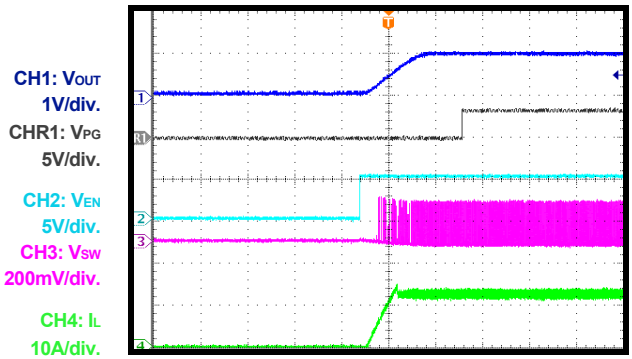
Start-Up through EN

I_{OUT} = 0A



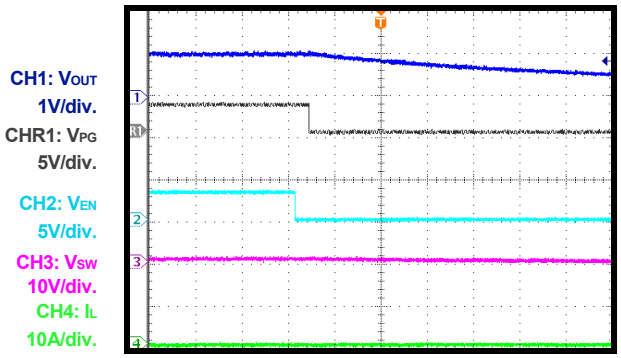
Start-Up through EN

I_{OUT} = 12A



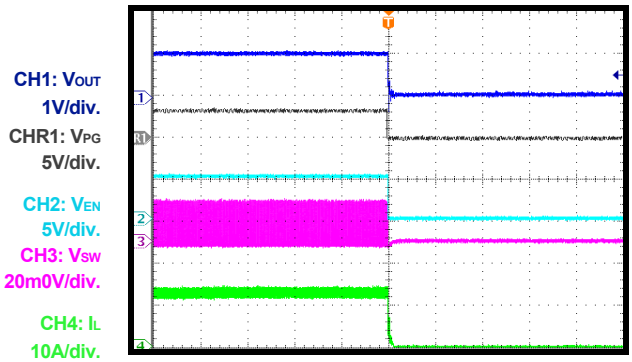
Shutdown through EN

I_{OUT} = 0A



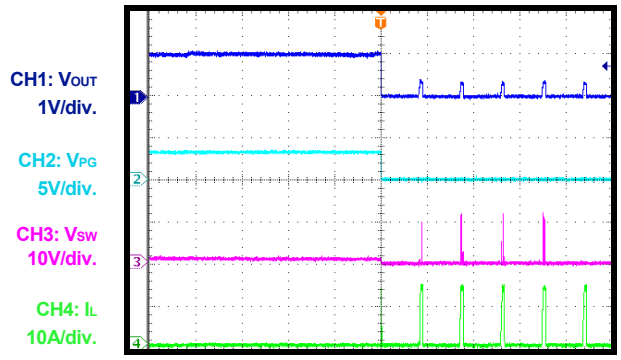
Shutdown through EN

I_{OUT} = 12A



Short-Circuit Protection Entry

I_{OUT} = 0A



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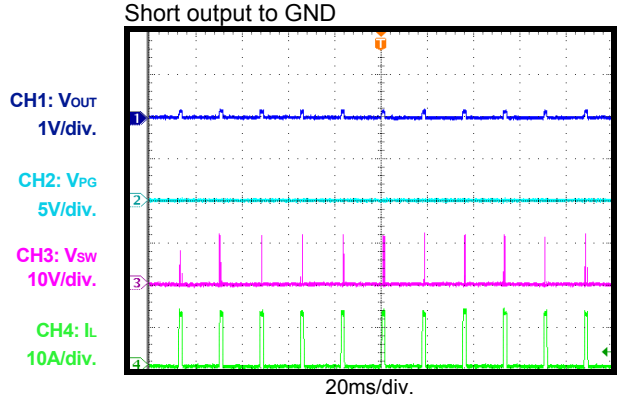
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1V, L = 0.56µH, T_A = 25°C, unless otherwise noted.

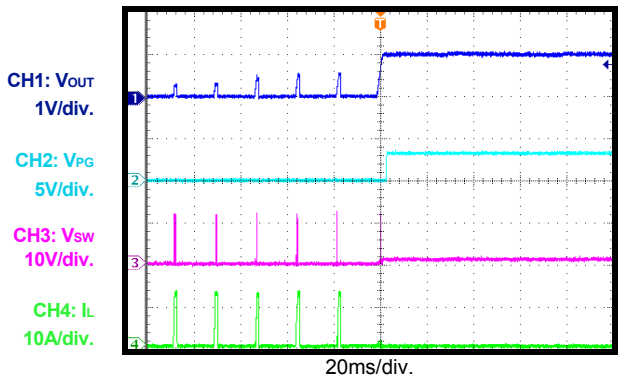
Short-Circuit Protection Steady State

Short output to GND



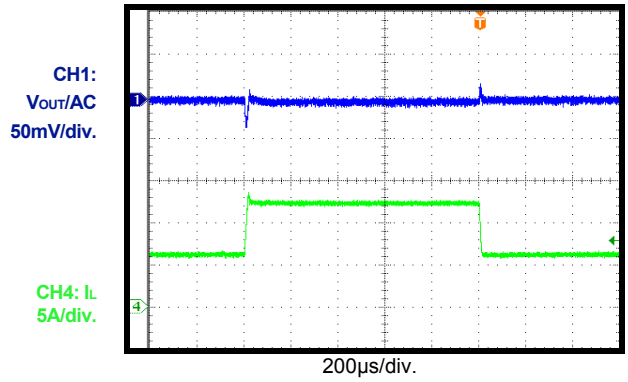
Short-Circuit Protection Recovery

I_{OUT} = 0A



Load Transient

I_{OUT} = 6 - 12A



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PIN FUNCTIONS

Package Pin #	Name	Description
1, 15	NC	**No connection.** NC must be left floating.
2	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. A BST resistor less than 4.7Ω is recommended.
3	EN	**Enable.** Pull EN high to enable the MP8772. When floating, EN is pulled down to GND and disabled by an internal 1.2MΩ resistor.
4	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider connected between the output and GND.
5	AGND	**Signal ground.** AGND is not connected to the system ground internally. Ensure that AGND is connected to the system ground in the PCB layout.
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid inrush current at start-up.
7	PG	**Power good output.** The output of PG is an open drain. PG changes state if UVP, OCP, OTP, or OV occurs.
8	VIN	**Supply voltage.** The MP8772 operates from a 3 - 17V input rail. A capacitor (C1) is needed to decouple the input rail. Use a wide PCB trace to make the connection.
9 - 13	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during the PCB layout. PGND is recommended to be connected to GND with coppers and vias.
14	VCC	**Internal bias supply output.** Decouple VCC with a 1μF capacitor. Place the VCC capacitor close to VCC and GND.
16	SW	**Switch output.** Connect SW with a wide PCB trace.

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BLOCK DIAGRAM

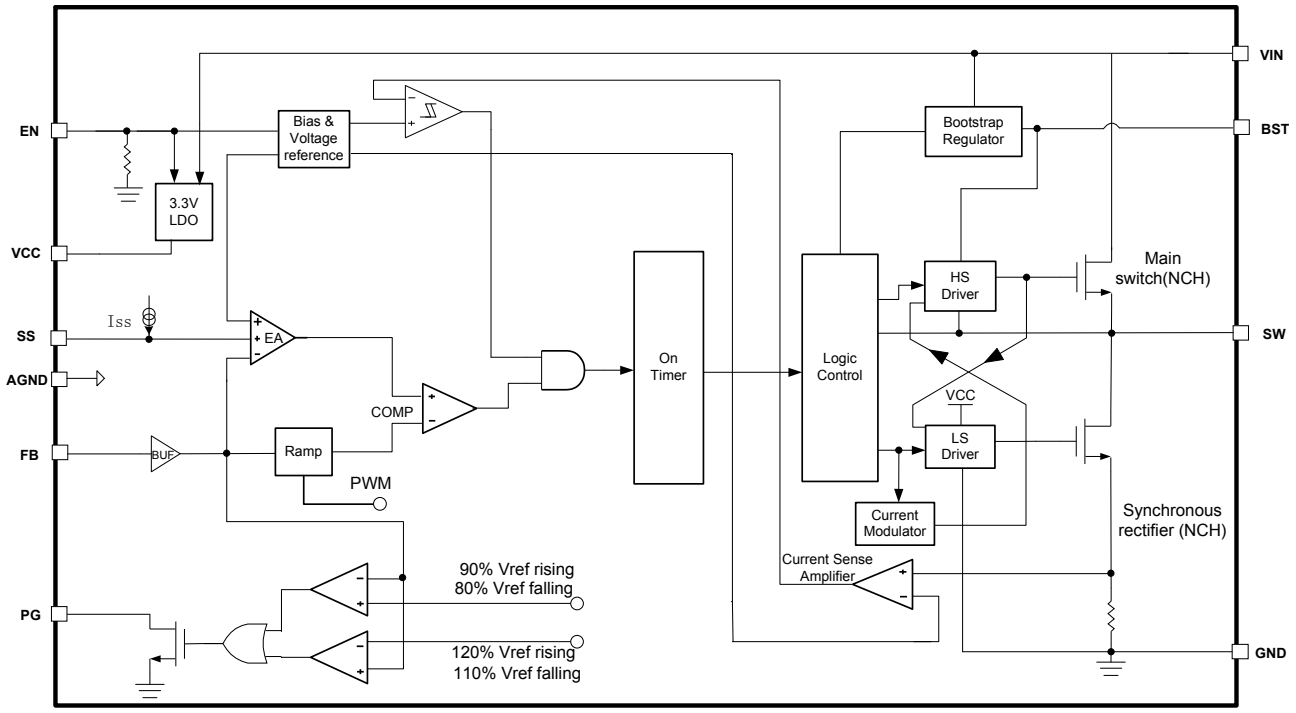

Figure 1: Functional Block Diagram

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OPERATION

The MP8772 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. Figure 2 shows the simplified ramp compensation block in the MP8772. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

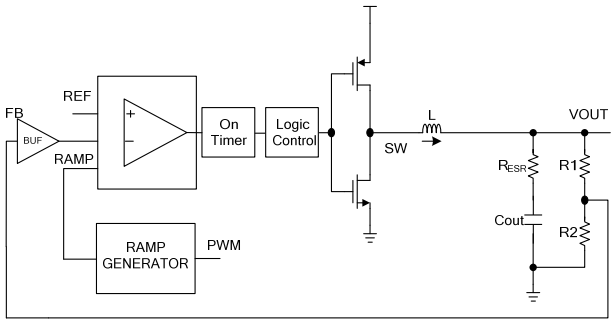

Figure 2: Simplified Ramp Compensation Block

Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 3). When V_{FB} is below the error amplifier output voltage (V_{EAO}), the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period.

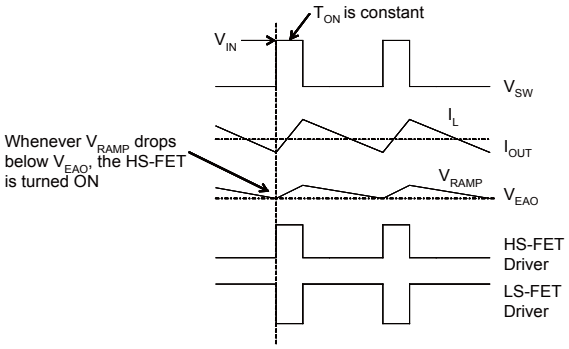

Figure 3: Heavy-Load Operation

In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

Light-Load Operation

When the MP8772 works in pulse-frequency modulation (PFM) during light-load operation, the MP8772 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the LS-FET driver goes into tri-state (Hi-Z) (see Figure 4). Therefore, the output capacitors discharge slowly to GND through the LS-FET, R1, and R2. This operation improves device efficiency greatly when the output current is low.

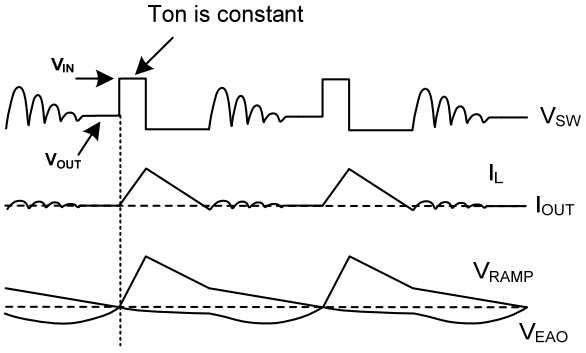

Figure 4: Light-Load Operation

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Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does during heavy-load conditions. The HS-FET turn-on frequency is a function of the output current. As the output current increases, the current modulator regulation time period becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches the critical level when the current modulator time is zero and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

VCC Regulator

The 3.4V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 3.4V, the output of the regulator is in full regulation. When V_{IN} falls below 3.4V, the output of the regulator decreases following V_{IN}. A 1µF decoupling ceramic capacitor is needed at VCC.

Enable (EN)

EN is a digital control pin that turns the regulator on and off. Drive EN above 1.25V to turn on the regulator. Drive EN below 1V to turn off the regulator. When floating, EN is pulled down to GND by an internal 1.2MΩ resistor. EN can be connected to V_{IN} directly and supports a 17V input range.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8772 UVLO comparator monitors the output voltage of the internal regulator (VCC). The VCC UVLO rising threshold is about 2.8V, while its falling threshold is 2.45V.

When the input voltage is higher than the UVLO rising threshold voltage, the MP8772 powers up. The MP8772 shuts off when the input voltage is lower than the UVLO falling threshold voltage. This is a non-latch protection.

Soft Start (SS)

The MP8772 employs a soft start (SS) mechanism to ensure smooth output ramping during power-up. When EN goes high, an internal current source (6µA) charges up the SS capacitor. The SS capacitor voltage takes over V_{REF} to the PWM comparator. The output voltage ramps up smoothly with the SS voltage (V_{SS}). If V_{SS} rises above V_{REF}, it continues to ramp up until V_{REF} takes over. At this point, the soft start finishes, and the device enters steady-state operation.

The SS capacitor value can be determined with Equation (2):

$$C_{ss}(nF) = 0.83 \times \frac{T_{ss}(ms) \times I_{ss}(uA)}{V_{REF}(V)} \quad (2)$$

If the output capacitance is large, it is not recommended to set the SS time too short; otherwise, the current limit can be reached easily during SS. SS cap less than 4.7nF should be avoid.

Power Good (PG) Indicator

PG is the open drain of a MOSFET that connects to VCC or another voltage source through a resistor (e.g.: 100kΩ). The MOSFET turns on with the application of an input voltage, so PG is pulled to GND before SS is ready. After V_{FB} reaches 90% of V_{REF}, PG is pulled high after a 50µs delay. When V_{FB} drops to 80% of V_{REF}, PG is pulled low.

When UVLO or over-temperature protection (OTP) occurs, PG is pulled low immediately. When an over-current (OC) condition occurs, PG is pulled low when V_{FB} drops below 80% of V_{REF} after a 0.05ms delay. When an over-voltage (OV) condition occurs, PG is pulled low when V_{FB} rises above 120% of V_{REF} after a 0.05ms delay. If V_{FB} falls below 110% of V_{REF}, PG is pulled high after a 0.05ms delay.

If the input supply fails to power the MP8772, PG is clamped low, even though PG is tied to an external DC source through a pull-up resistor. The relationship between the PG voltage and the pull-up current is shown in Figure 5.

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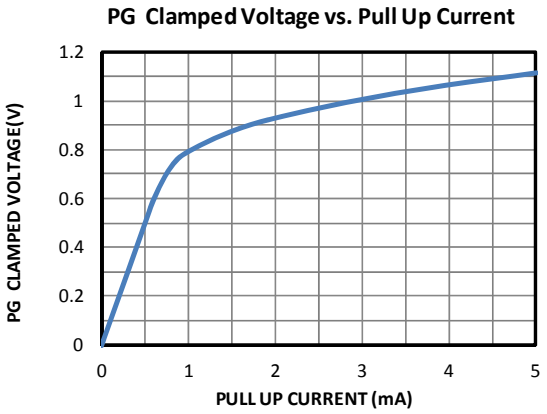

Figure 5: PG Clamped Voltage vs. Pull-Up Current

Over-Current Protection (OCP) and Short-Circuit Protection (SCP)

The MP8772 has a valley-limit control. The LS-FET monitors the current flowing through the LS-FET. The HS-FET waits until the valley current limit is removed before turning on again. Meanwhile, the output voltage drops until V_{FB} is below the under-voltage (UV) threshold (typically 50% below the reference). Once UV is triggered, the MP8772 enters hiccup mode to restart the part periodically.

During over-current protection (OCP), the device attempts to recover from the over-current fault with hiccup mode. This means that the chip disables the output power stage, discharges the soft-start capacitor, and attempts to soft start again automatically. If the over-current condition still remains after the soft start ends, the device repeats this operation cycle until the over-current condition disappears, and then the output rises back to the regulation level. OCP is a non-latch protection.

Pre-Bias Start-Up

The MP8772 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft-start capacitor is charged as well. If the BST voltage exceeds its rising threshold voltage and the soft-start capacitor voltage exceeds the sensed output voltage at FB, the part begins working normally.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection with a rising threshold of 1.7V and a hysteresis of 150mV. V_{IN} regulates the bootstrap capacitor voltage internally through D1, M1, R4, C4, Lo, and Co (see Figure 6). If V_{IN} - V_{SW} exceeds 5V, U2 regulates M1 to maintain a 3.3V BST voltage across C4. The BST resistor (R4) is recommended to be less than 4.7Ω.

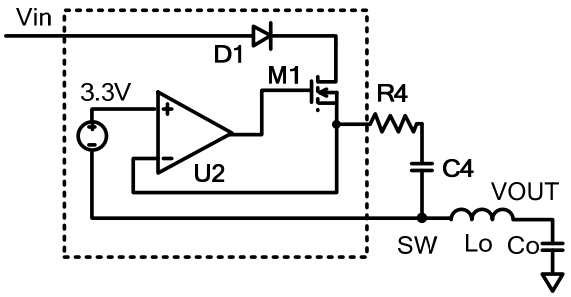

Figure 6: Internal Bootstrap Charger

Start-Up and Shutdown Circuit

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuits.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. The shutdown procedure starts by blocking the signaling path initially to avoid any fault triggering. The internal supply rail is then pulled down.

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APPLICATION INFORMATION

Setting the Output Voltage

An external resistor divider is used to set the output voltage. First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, while a large R2 makes FB noise-sensitive. R2 is recommended to be between 2 - 100kΩ. Typically, set the current through R2 to be below 250μA for a good balance between system stability and no-load loss. Then determine R1 with Equation (3):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (3)$$

The feedback circuit is shown in Figure 7.

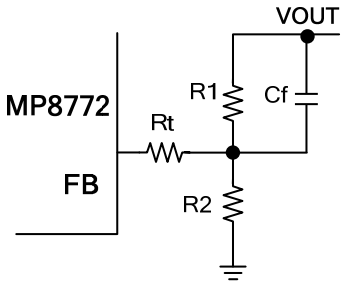

Figure 7: Feedback Network

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	Cf (pF)	Rt (kΩ)
1.0	20	30	0.56	56	1
1.2	20	20	0.56	56	1
1.5	20	13	0.56	56	1
1.8	20	10	0.82	56	1
2.5	20	6.34	0.82	56	1
3.3	20	4.42	1	56	1
5	20	2.7	1.2	56	1

Selecting the Inductor

An inductor is necessary for supplying constant current to the output load while being driven by the switched input voltage. A larger-value inductor results in less ripple current and a lower output ripple voltage but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30 - 40% of the maximum output current, and ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (4):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated with Equation (5):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (6):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose an input capacitor that meets the specification.

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The input voltage ripple can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (9):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (9)$$

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (10)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

The output voltage ripple caused by the ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through a resistor (R_{RAMP}) and a capacitor (Cr).

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (12)$$

Besides considering the output ripple, choosing a larger output capacitor can also result in a better load transient response. Be sure to consider the maximum output capacitor limitation in the design application. If the output capacitor value is too high, the output voltage cannot reach the design value during the soft-start time and fails to regulate.

The maximum output capacitor value (C_{o_max}) can be limited approximately with Equation (13):

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (13)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

PCB Layout Guidelines

Efficient PCB layout of the switching power supplies is critical for stable operation. A poor layout design can result in poor line or load regulation and stability issues. For better performance, it is recommended to use a four-layer boards (two middle layers are GND). For best results, refer to Figure 8 and follow the guidelines below.

1. Place the high-current paths (GND, VIN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitor as close to VIN and GND as possible.
3. Place a VCC decoupling capacitor close to the device.
4. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
5. Place the external feedback resistors next to FB.
6. Keep the switching node (SW) short and away from the feedback network.

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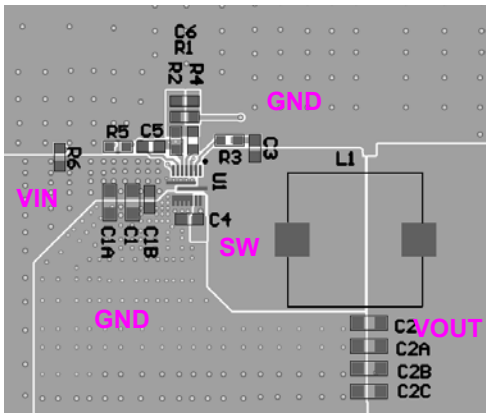
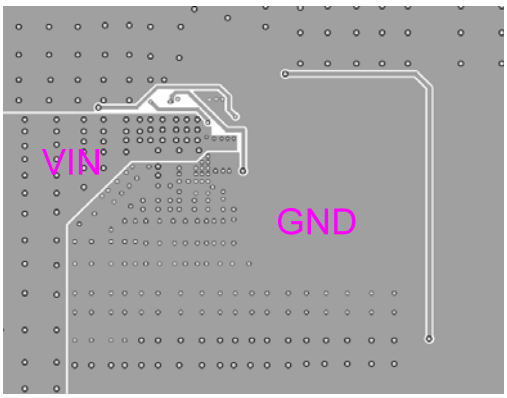


Top Layer



Bottom Layer

Figure 8: Recommended Layout

Design Example

Table 2 shows a design example when ceramic capacitors are applied.

Table 2: Design Example

V_{IN}	12V
V_{OUT}	1V
I_{OUT}	12A

The detailed application schematics are shown in Figure 9 through Figure 15. The typical performance and waveforms are shown in the Typical Characteristics section. For more devices applications, please refer to the related evaluation board datasheet.

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TYPICAL APPLICATION CIRCUITS

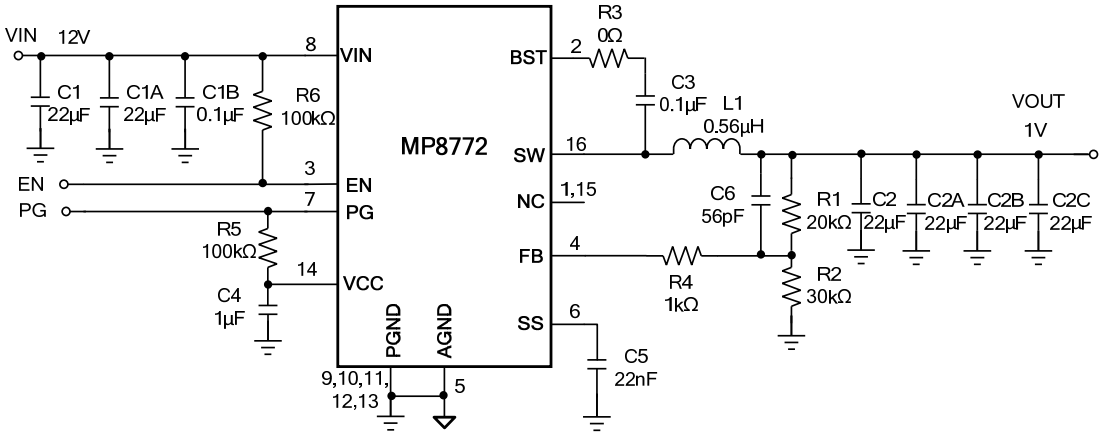

Figure 9: V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A (8)

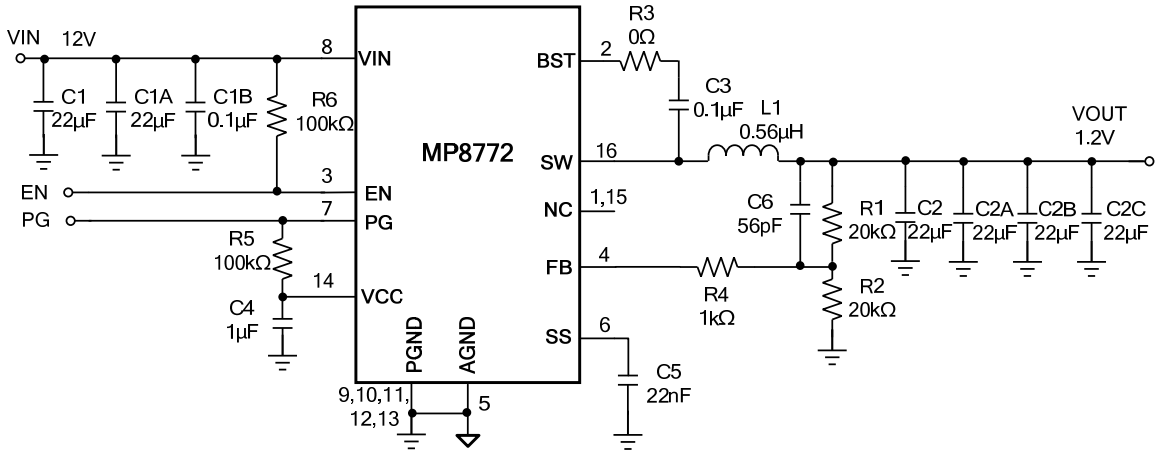

Figure 10: V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 12A (8)

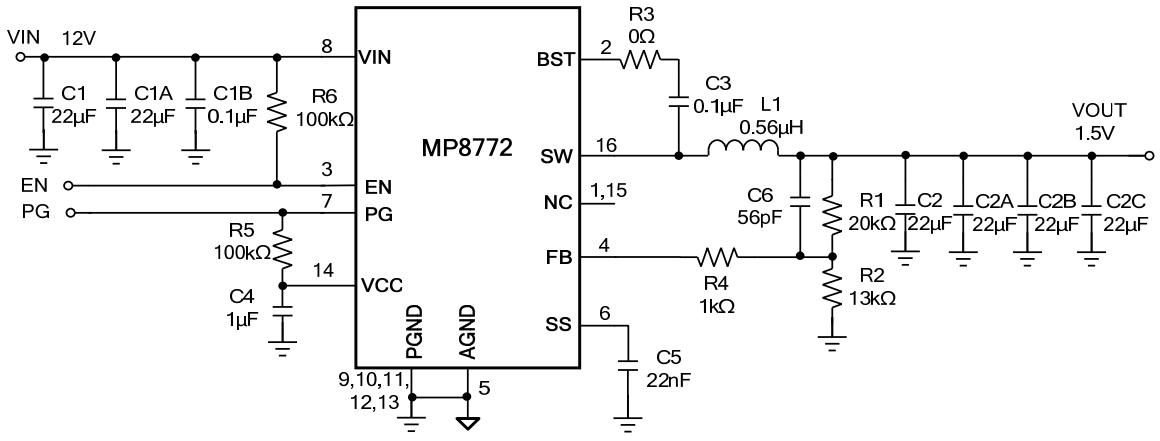

Figure 11: V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 12A (8)

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TYPICAL APPLICATION CIRCUITS *(continued)*

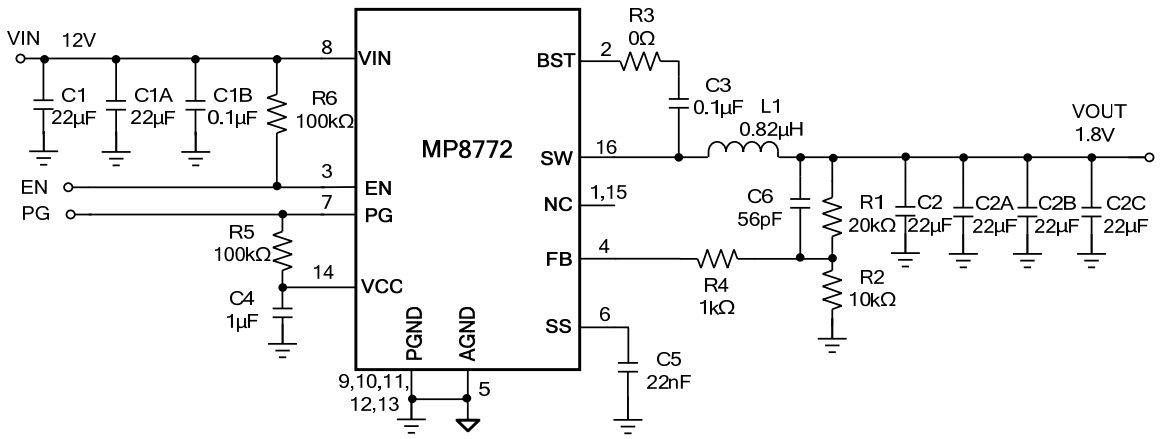

Figure 12: V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} = 12A (8)

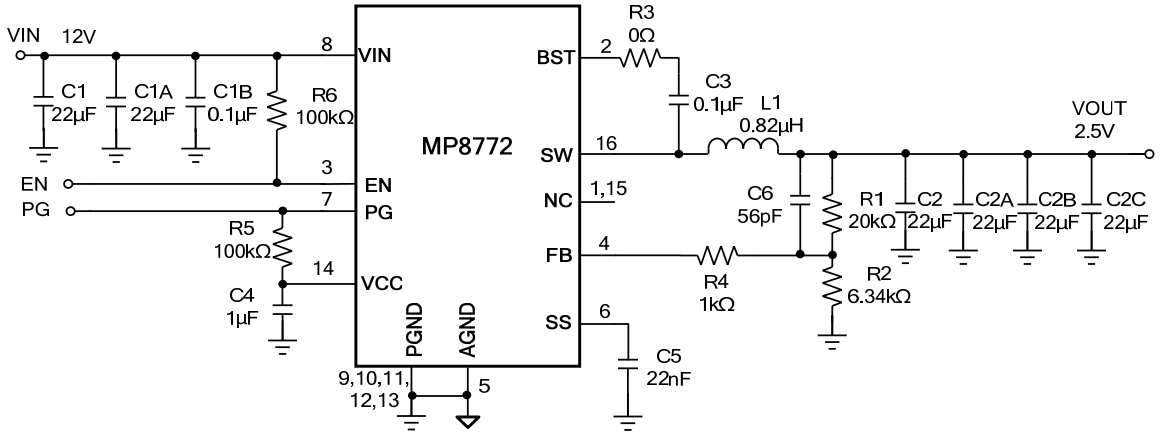

Figure 13: V_{IN} = 12V, V_{OUT} = 2.5V, I_{OUT} = 12A (8)

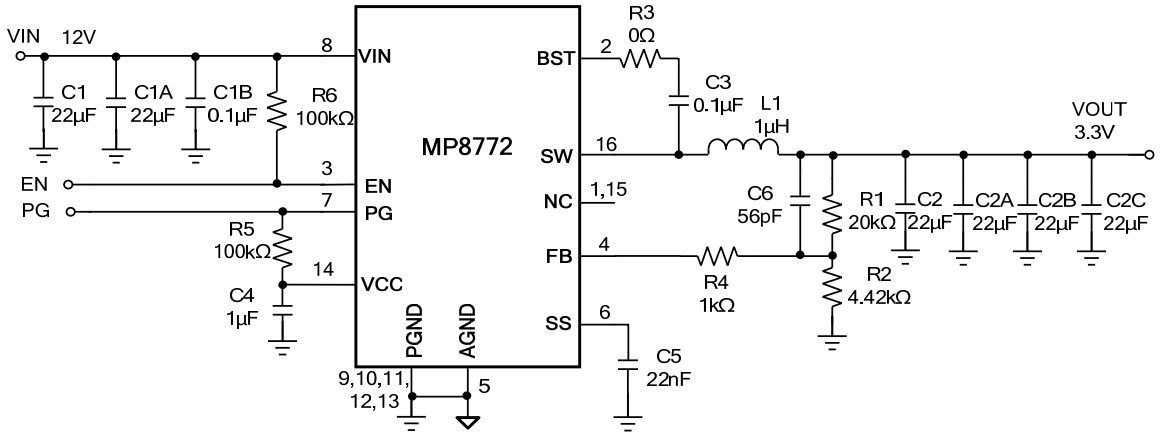

Figure 14: V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 12A (8)

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TYPICAL APPLICATION CIRCUITS *(continued)*

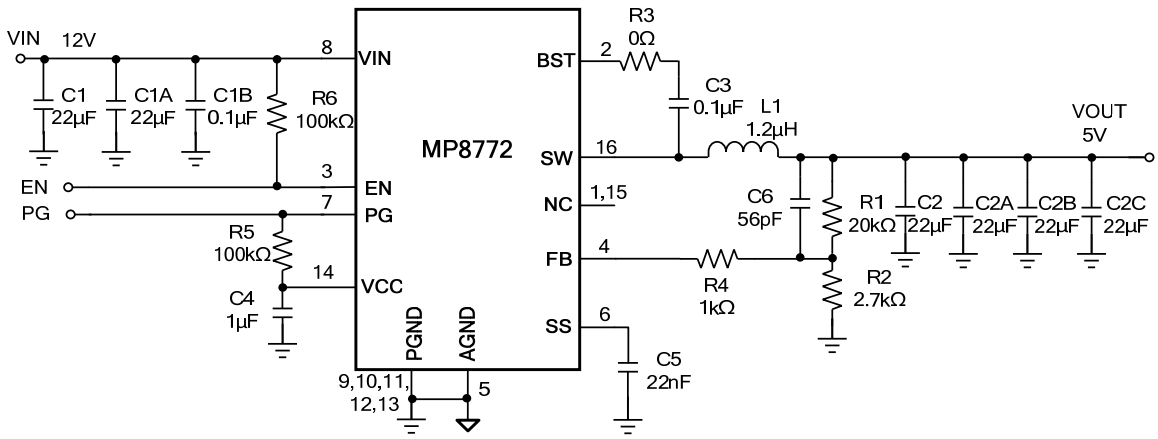

Figure 15: V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 12A (8)

NOTE:

8) When V_{IN} is low, refer to the Selecting the Input Capacitor section on page 17.

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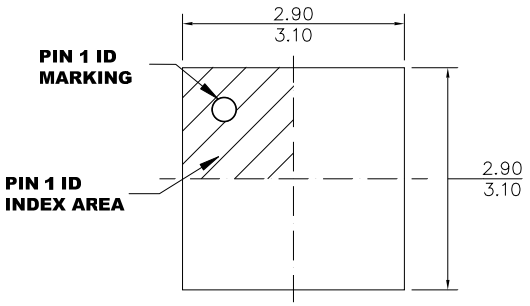
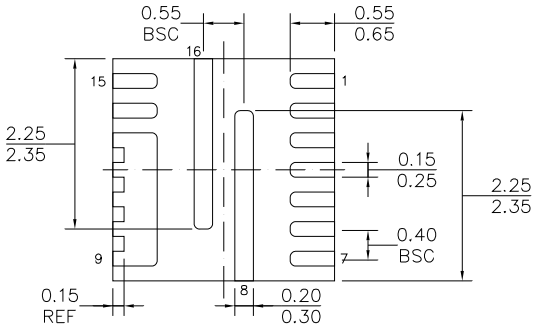
PACKAGE INFORMATION

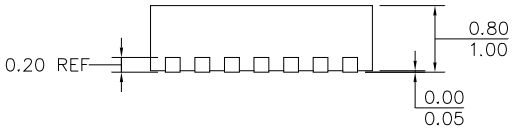
QFN-16 (3mmx3mm)



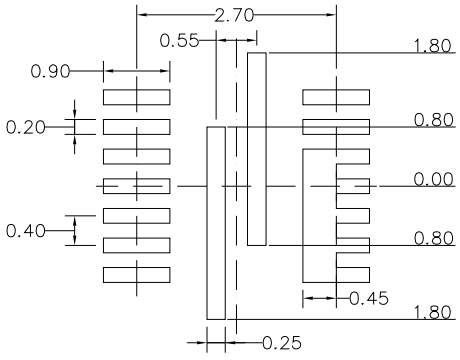
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

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