MP8792

16V, 12A, Synchronous Step-Down Converter with Adjustable Current Limit, Configurable Frequency, and Voltage Tracking

DESCRIPTION

The MP8792 is a fully integrated, high-frequency, synchronous buck converter. It offers a compact solution to achieve up to 12A of output current over a wide input supply range with excellent load and line regulation. The MP8792 operates at high efficiency over a wide output current load range.

The MP8792 adopts internally compensated constant-on-time (COT) control to provide fast transient response and ease loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz with MODE configuration, allowing the MP8792's frequency to remain constant regardless of the input or output voltages.

The output voltage start-up ramp is controlled by an internal 1ms timer. It can be increased by adding a capacitor on TRK/REF. An open-drain power good (PG) signal indicates whether the output is within its nominal voltage range. The PGOOD pin is clamped to about 0.7V by an external pull-up voltage when the input supply fails to power the MP8792.

Fully integrated protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP8792 requires a minimal number of readily available, standard external components. It is available in a QFN (3mmx4mm) package.

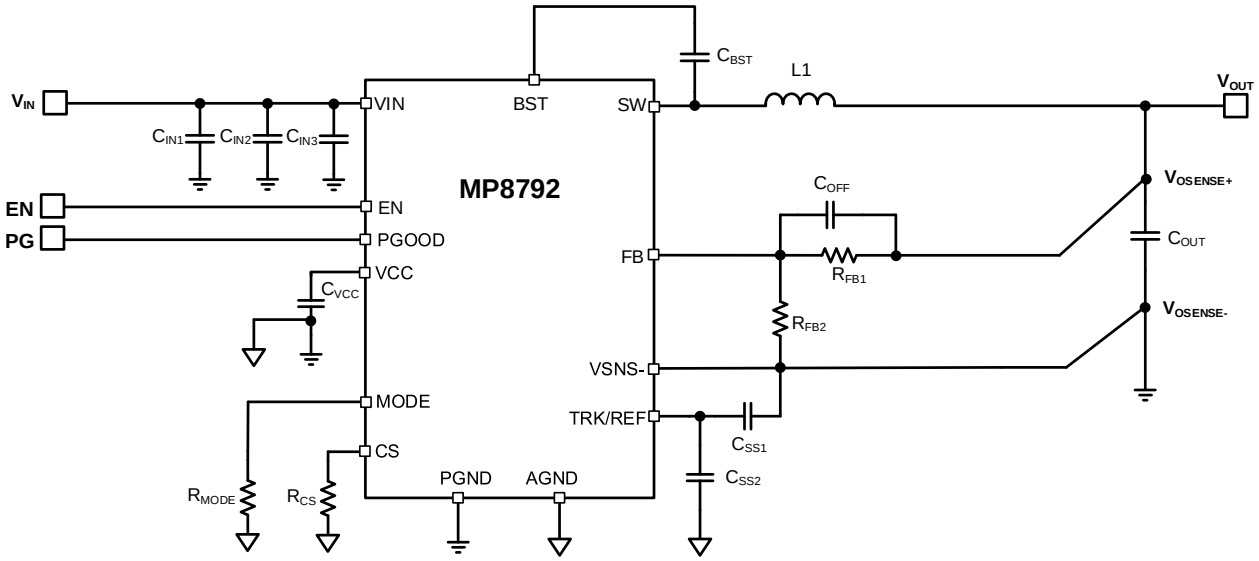
FEATURES

- Wide Input Voltage Range from 2.7V
  - 2.7V to 16V with External 3.3V VCC Bias
  - 4V to 16V with Internal VCC Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- Configurable Accurate Current Limit Level
- 12A Output Current
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Adaptive COT for Ultra-Fast Transient Response
- Stable with Zero-ESR Output Capacitor
- 0.5% Reference Voltage across a 0°C to 70°C Junction Temperature Range
- 1% Reference Voltage across a -40°C to +125°C Junction Temperature Range
- Selectable Pulse Skip or Forced CCM Operation
- Excellent Load Regulation
- Output Voltage Tracking
- Output Voltage Discharge
- PGOOD Active Clamped at Low Level during Power Failure
- Programmable Soft-Start Time from 1ms
- Pre-Biased Start-Up
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVP, OVP, UVLO, and Thermal Shutdown
- Output Adjustable from 0.6V to 90% of V_{IN}, up to 5.5V Max
- Available in a QFN (3mmx4mm) Package
- The MPL-AY1265 Inductor Series Matches Best Performance

APPLICATIONS

- FPGAs, High-Definition TVs, and Monitors
- Communication Systems
- General Power Distribution Systems

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP8792GLE	QFN-21 (3mmx4mm)	*See Below*	1

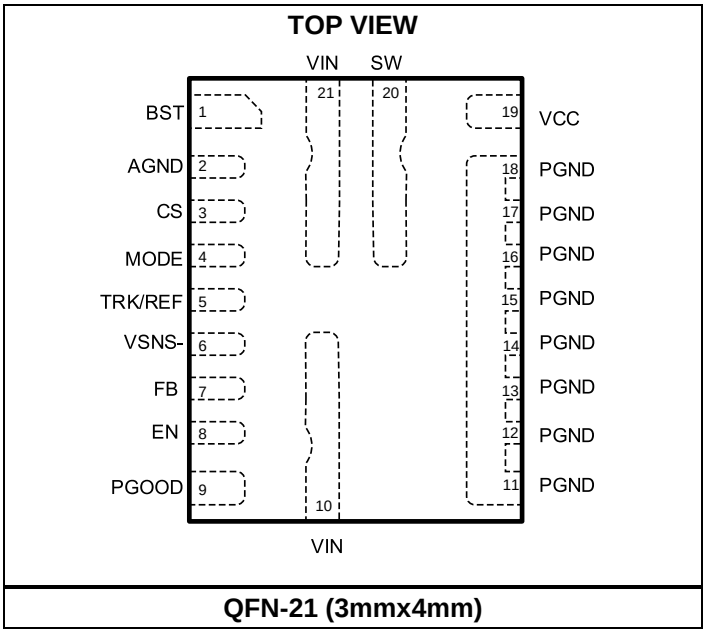
* For Tape & Reel, add suffix –Z (e.g. MP8792GLE–Z).

TOP MARKING

MPYW
8792
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
8792: First four digits of the part number
LLL: Lot number
E: Package prefix

PACKAGE REFERENCE



QFN-21 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap**. Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
2	AGND	**Analog ground.** Select AGND as the control circuit reference point.
3	CS	**Current limit.** Connect a resistor to ground to set the current limit trip point.
4	MODE	**Operation mode selection**. Program MODE to select CCM, pulse skip mode, and the operating switching frequency. See Table 1 on page 14 for additional details.
5	TRK/REF	**External tracking voltage input.** The output voltage tracks this input signal. Decouple TRK/REF with a ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. The capacitance determines the soft-start time. See Equation 2 on page 14 for additional details.
6	VSNS-	**Differential remote-sense negative input.** Connect VSNS- directly to the negative side of the voltage sense point. Short to GND if remote sense is not used.
7	FB	**Feedback (differential remote-sense positive input).** An external resistor divider from the output to VSNS- (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Avoid placing vias on the FB traces.
8	EN	**Enable.** EN is an input signal that turns the regulator on or off. Drive EN high to turn the regulator on; drive EN low to turn it off. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
9	PGOOD	**Power good output.** This is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate if the output voltage is within regulation. There is a delay of about 1ms from when the FB voltage becomes greater than or equal to 92.5% of the reference voltage and the time PGOOD pulls high.
10, 21	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are required to decouple the input rail. Use wide PCB traces to make the connection.
11–18	PGND	**System ground.** PGND is the reference ground of the regulated output voltage, and it should be considered while designing the PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The driver and control circuits are powered from this voltage. Decouple VCC with a minimum 1µF ceramic capacitor, placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on time of the PWM duty cycle. The inductor current drives SW low during the off time. Use wide PCB traces to make the connection.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
$V_{SW (DC)}$ ..... -0.3V to V_{IN} + 0.3V
V_{SW} (25ns) (2) ..... -3V to +25V
V_{SW} (25ns) ..... -5V to +25V
V_{BST} ..... V_{SW} + 4V
V_{CC}, EN 4.5V
All other pins ..... -0.3V to +4.3V
Junction temperature ..... 170°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +170°C

ESD Rating

Human body model (HBM) 2000V
Charged device model (CDM) 750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
$V_{IN(DC)}$ - $V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
$V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
External VCC bias (V_{CC_EXT}) ..... 3.12V to 3.6V
Maximum output current (I_{OUT_MAX}) 12A
Maximum output current limit (I_{OC_MAX}) 16A
Maximum peak inductor current (I_{L_PEAK}) 18A
EN voltage (V_{EN}) 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance	***θ_{JA}***	***θ_{JC}***	
QFN-21 (3mmx4mm)			
EVL8792-LE-00A (5)	29	4	°C/W
JESD51-7 (6)	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured by using differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) The voltage rating can be in the range of -3V to +23V for a period of 25ns or shorter with a maximum repetition rate of 1000kHz when the input voltage is 16V.
5) Measured on EVL8792-LE-00A, 4-layer PCB, 78mmx81mm.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		10	20	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 0.62V		650	850	μA
MOSFET						
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
HS on state resistance	$R_{DS\_ON\_HS}$	V_{EN} = 2V at 25°C		13.3		mΩ
LS on state resistance	$R_{DS\_ON\_LS}$	V_{EN} = 2V at 25°C		3.8		mΩ
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS}/I_{OUT}	I_{OUT} ≥ 2A	18	20	22	μA/A
Low-side negative current limit	I_{LIM_NEG}			-9		A
Negative current limit time out (7)	t_{NCL_Timer}			200		ns
Switching Frequency						
Switching frequency	f_{SW}	MODE = GND, I_{OUT} = 0A, V_{OUT} = 1V, T_J = 25°C	480	600	720	kHZ
		MODE = 30.1kΩ, I_{OUT} = 0A, V_{OUT} = 1V, T_J = 25°C	680	800	920	kHZ
		MODE = 60.4kΩ, I_{OUT} = 0A, V_{OUT} = 1V, T_J = 25°C	850	1000	1150	kHZ
Minimum on time (7)	t_{ON_MIN}	V_{FB} = 500mV			50	ns
Minimum off time (7)	t_{OFF_MIN}	V_{FB} = 500mV			180	ns
Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft Start						
Feedback voltage	V_{REF}	T_J = -40°C to +125°C	594	600	606	mV
		T_J = 0°C to 70°C	597	600	603	mV
TRK/REF sourcing current	I_{TRACK_Source}	$V_{TRK/REF}$ = 0V		42		μA
TRK/REF sinking current	I_{TRACK_Sink}	$V_{TRK/REF}$ = 1V		12		μA
Soft-start time	t_{SS}	C_{TRACK} = 1nF, T_J = 25°C	0.75	1	1.25	ms
Error Amplifier						
Error amplifier offset	V_{OS}		-3	0	+3	mV
Feedback current	I_{FB}	V_{FB} = REF		50	100	nA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
Enable input rising threshold	VIH_{EN}		1.17	1.22	1.27	V
Enable hysteresis	V_{EN-HYS}			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge FET	R_{ON_DISCH}			80	150	Ω
VIN UVLO						
VIN under-voltage lockout rising threshold	VIN_{Vth_Rise}	V_{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout falling threshold	VIN_{Vth_Fall}		1.55	1.85	2.15	V
VCC Regulator						
VCC under-voltage lockout rising threshold	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout falling threshold	VCC_{vth_Fall}		2.35	2.5	2.65	V
VCC regulator	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		I_{CC} = 25mA		0.5		%
Power Good						
Power good high threshold	$PG_{Vth\_Hi\_Rise}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
	$PG_{Vth\_Hi\_Fall}$	FB from low to high	102%	105%	108%	V_{REF}
Power good low threshold	$PG_{Vth\_Lo\_Rise}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth\_Lo\_Fall}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low-to-high delay	PG_{Td}	T_J = 25°C	0.63	0.9	1.17	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	μA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, Pull PGOOD up to 3.3V through a 100kΩ resistor at 25°C		650	800	mV
	V_{OL_10}	V_{IN} = 0V, Pull PGOOD up to 3.3V through a 10kΩ resistor at 25°C		750	900	mV
Thermal Protection						
Thermal shutdown (7)	T_{SD}			160		°C
Thermal shutdown hysteresis (7)				30		°C

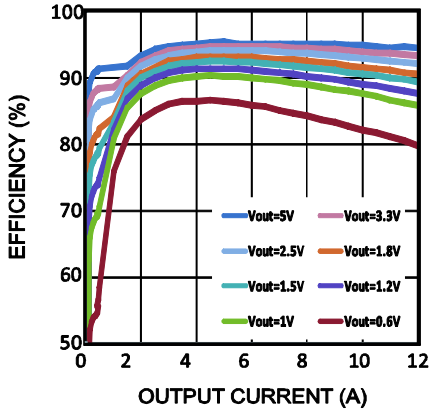
Note:

7) Guaranteed by design.

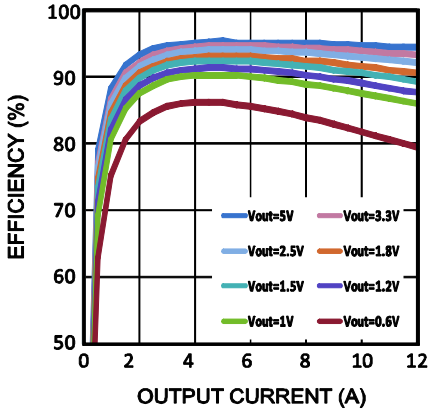
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2 V, f_{SW} = 800kHz, unless otherwise noted.

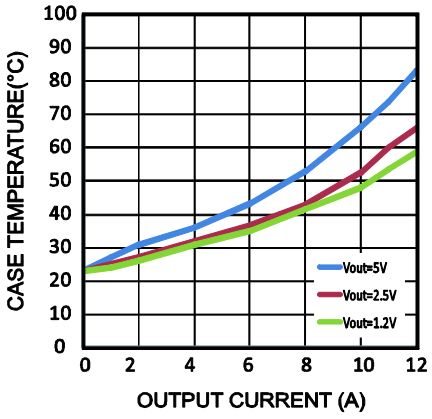
Efficiency
Pulse Skip, 1.1µH, 800kHz



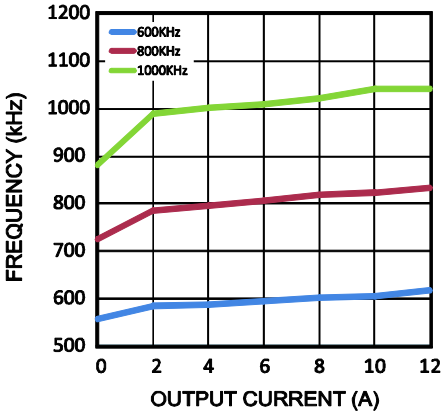
Efficiency
Forced CCM, 1.1µH, 800kHz



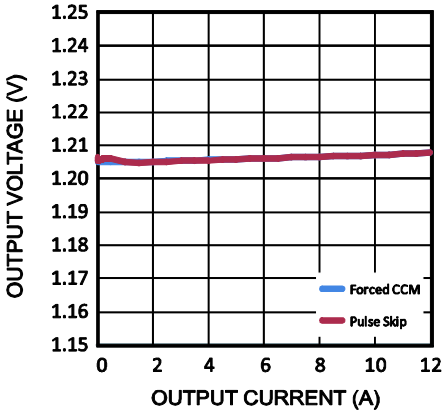
Thermal Results
800kHz



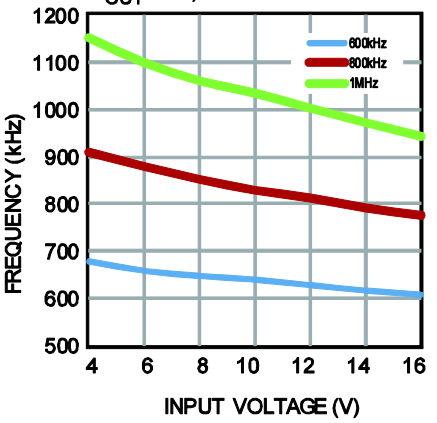
Switching Frequency vs. Output Current
Forced CCM



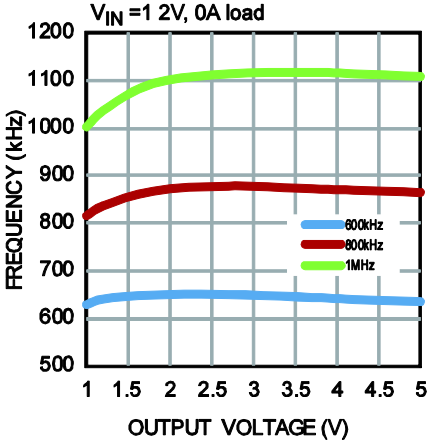
Output Voltage Load Regulation



Switching Frequency vs. Input Voltage
V_{OUT} = 1V, 0A load



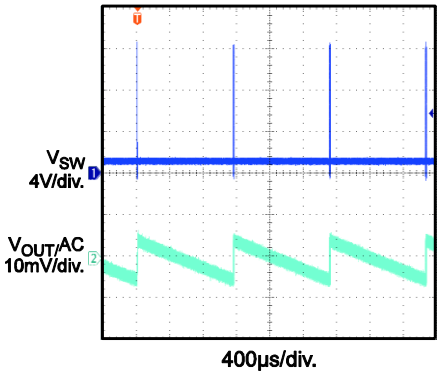
Switching Frequency vs. Output Voltage
V_{IN} =1 2V, 0A load



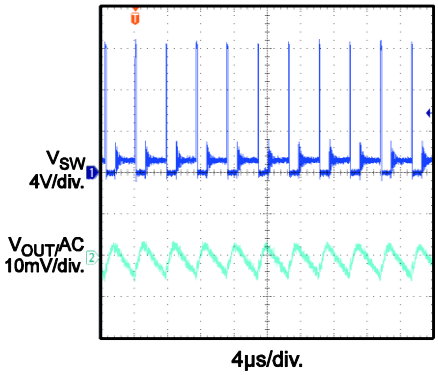
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

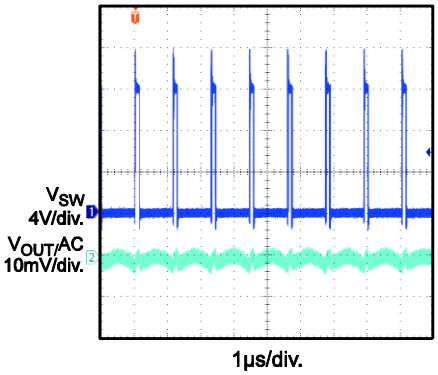
Steady State
I_{OUT} = 0A, pulse skip



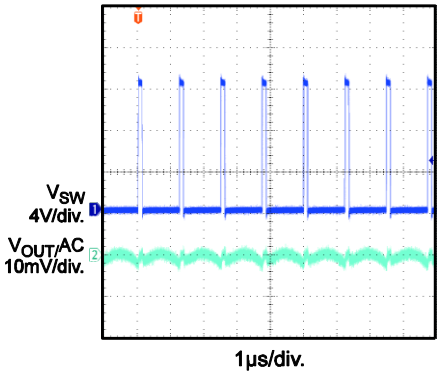
Steady State
I_{OUT} = 0.5A, pulse skip



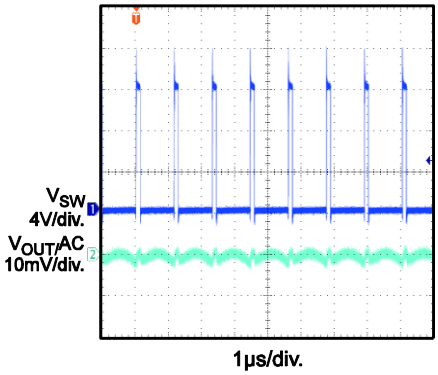
Steady State
I_{OUT} = 12A, pulse skip



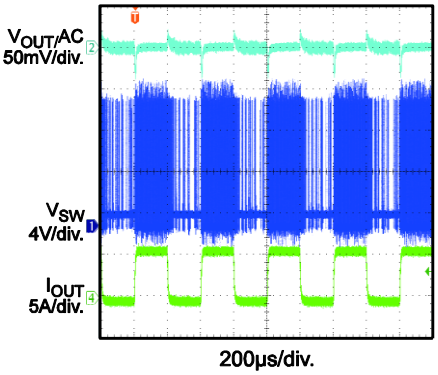
Steady State
I_{OUT} = 0A, forced CCM



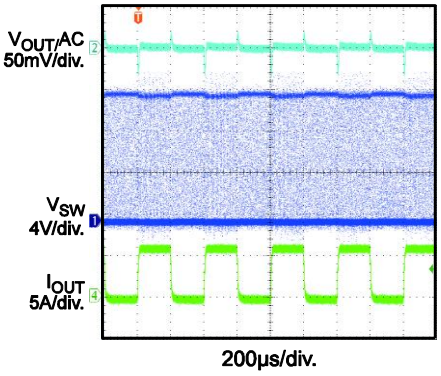
Steady State
I_{OUT} = 12A, forced CCM



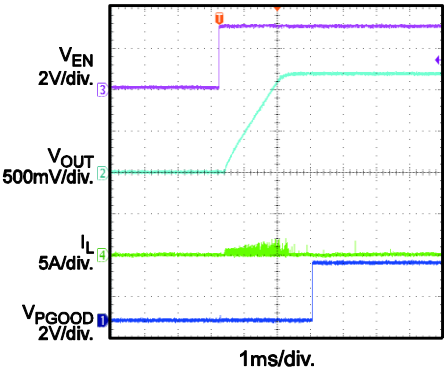
Load Transient
I_{OUT} = 0A to 6A, pulse skip



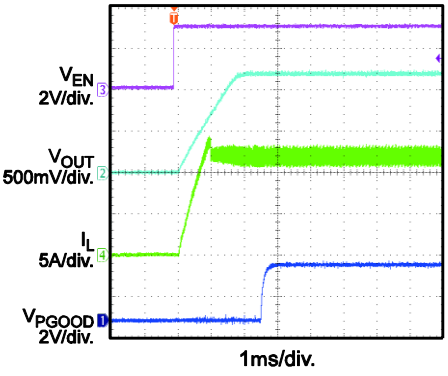
Load Transient
I_{OUT} = 0A to 6A, forced CCM



Start-Up through EN
I_{OUT} = 0A, pulse skip



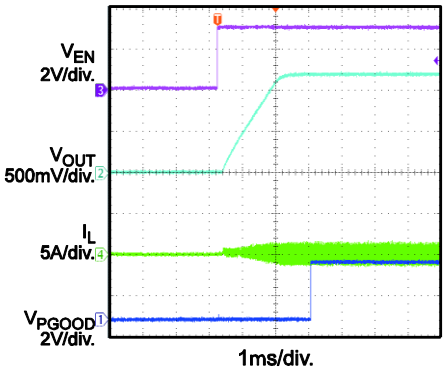
Start-Up through EN
I_{OUT} = 12A, pulse skip



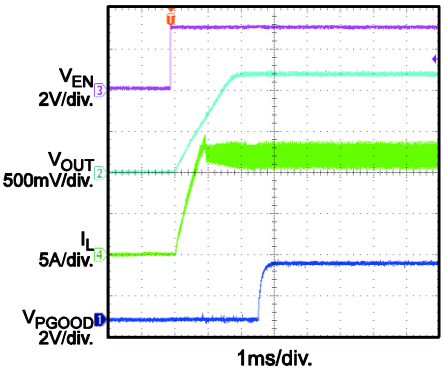
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

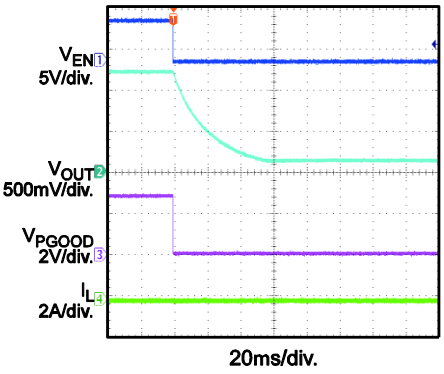
Start-Up through EN
I_{OUT} = 0A, forced CCM



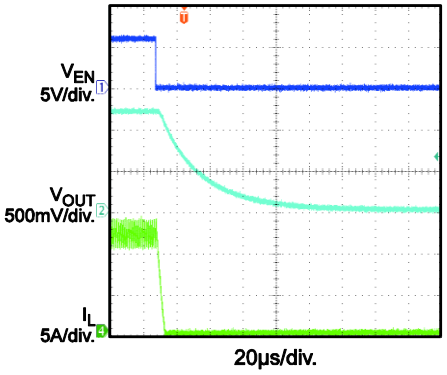
Start-Up through EN
I_{OUT} = 12A, forced CCM



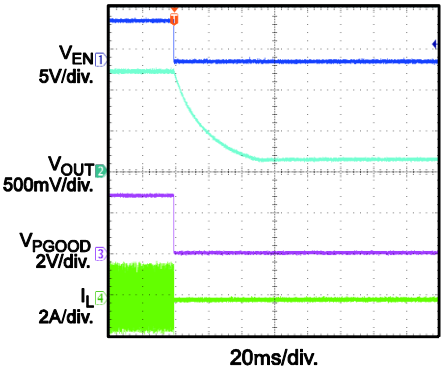
Shutdown through EN
I_{OUT} = 0A, pulse skip



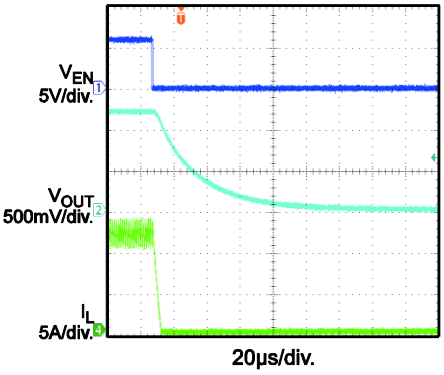
Shutdown through EN
I_{OUT} = 12A, pulse skip



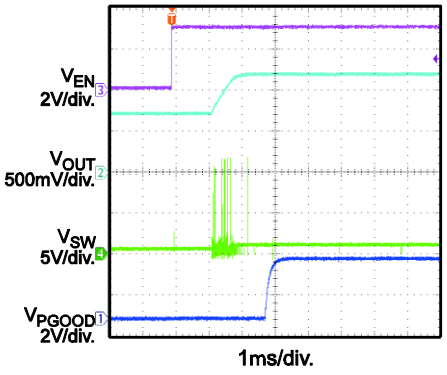
Shutdown through EN
I_{OUT} = 0A, forced CCM



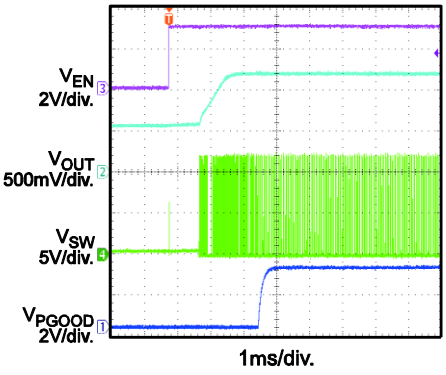
Shutdown through EN
I_{OUT} = 12A, forced CCM



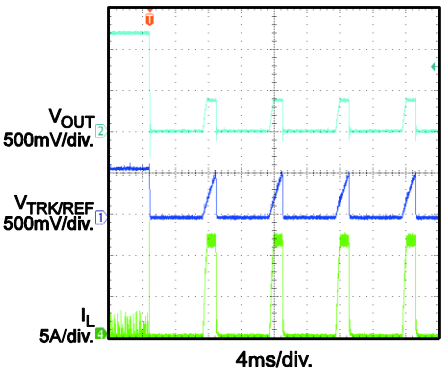
Pre-Biased Start-Up
Pulse skip



Pre-Biased Start-Up
Forced CCM



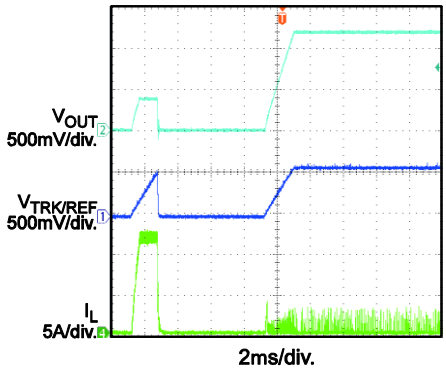
Over-Current Protection Entry



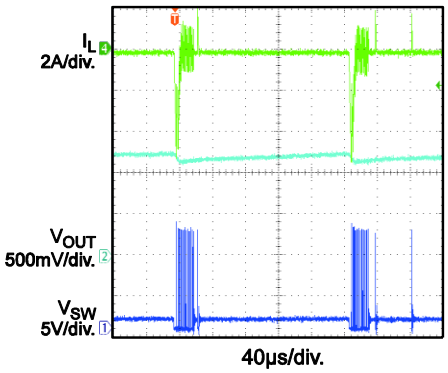
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1.2V, F_S = 800kHz unless otherwise noted.

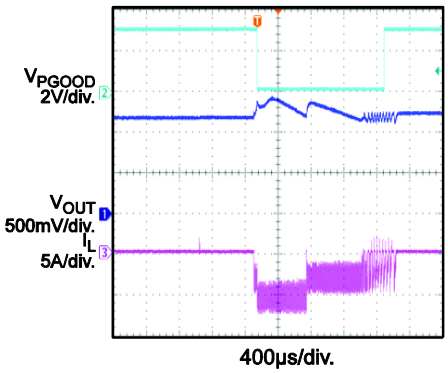
Over-Current Protection Recovery



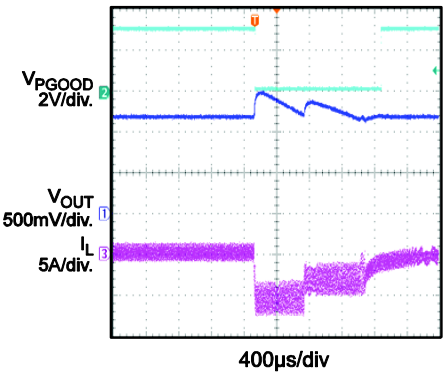
OSM Operation
Pulse skip mode



Over-Voltage Protection
Pulse skip mode



Over-Voltage Protection
Forced CCM



FUNCTIONAL BLOCK DIAGRAM

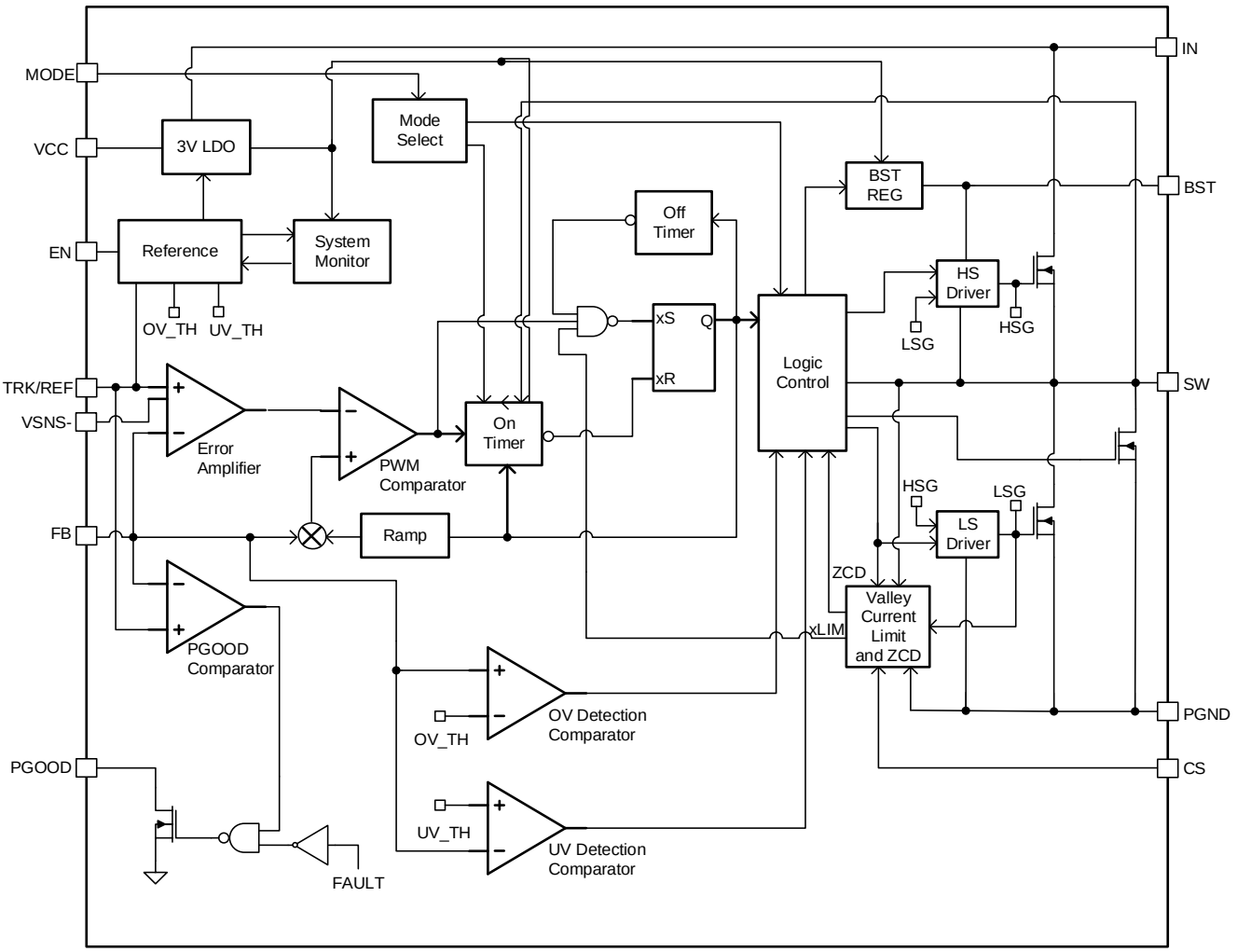


Figure 1: Functional Block Diagram

OPERATION

Constant-On-Time (COT) Control

The MP8792 employs constant-on-time (COT) control to achieve fast load transient response. Figure 2 shows the details of the MP8792's control stage.

The operational amplifier (AMP) corrects any voltage errors between the feedback voltage (V_{FB}) and the reference voltage (V_{REF}). The MP8792 can use AMP to provide excellent load regulation over the whole load range in either forced continuous conduction mode (CCM) or pulse skip mode.

The dedicated VSNS- pin provides differential output voltage remote sensing. The pair of remote-sense traces should be kept at low impedance for optimal performance.

The MP8792 has internal ramp compensation, and it supports a low-ESR MLCC output capacitor solution. The adaptive internal ramp is optimized so that the MP8792 remains stable in the whole operating input/output voltage range with proper design of the output L/C filter.

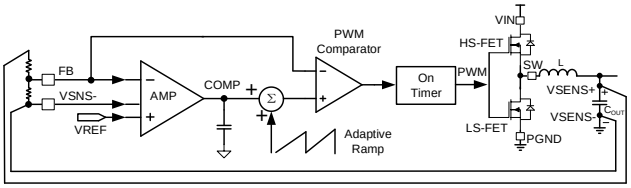


Figure 2: COT Control

PWM Operation

Figure 3 shows the generation of the pulse-width modulation (PWM) signal. AMP corrects any error between V_{FB} and V_{REF}, and generates a smooth DC voltage (COMP). The internal ramp is superimposed onto COMP. The superimposed COMP is compared with the FB signal. When V_{FB} drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) turns on.

The HS-FET remains on for a fixed on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on time elapses, the HS-FET turns off. It turns on again when V_{FB} drops below the superimposed COMP. By repeating this operation, the MP8792 regulates the output voltage.

To minimize conduction loss, the integrated low-side MOSFET (LS-FET) turns on when the HS-FET is off. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off period and the LS-FET on period, or vice versa.

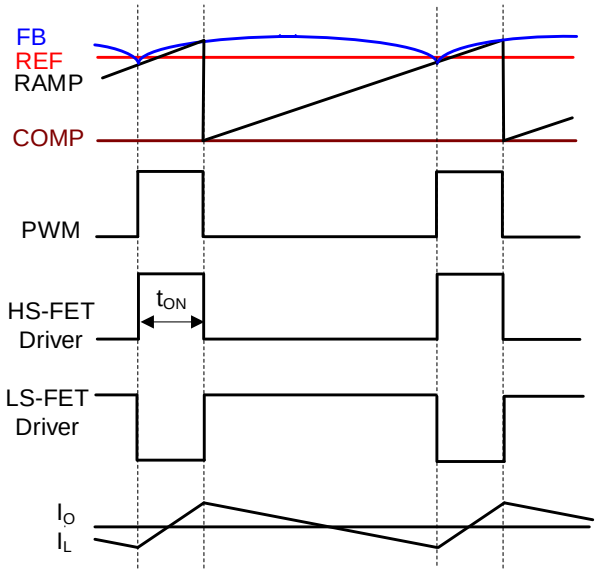


Figure 3: Heavy-Load Operation (PWM)

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above 0A (see Figure 2). The MP8792 can also be configured to operate in forced CCM operation when the output current is low (see the Mode Selection section on page 14 for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), so the output ripple remains constant throughout the load range.

Pulse Skip Operation

Under light-load conditions, the MP8792 can be configured to work in pulse skip mode to optimize efficiency. When the load decreases, the inductor current also decreases. Once the inductor current reaches zero, the part transitions from CCM to pulse skip mode if the MP8792 is configured to do so (see the Mode Selection section on page 14 for details).

Figure 4 shows pulse skip mode operation under light-load conditions. When V_{FB} drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero.

During pulse skip mode, V_{FB} does not reach the superimposed COMP when the inductor current approaches zero. The LS-FET driver switches to tri-state (HI-Z) when the inductor current reaches zero.

A current modulator controls the LS-FET and limits the inductor current to below -1mA. This allows the output capacitors to discharge slowly to PGND through the LS-FET. Under light-load conditions, the HS-FET does not turn on as frequently in pulse skip mode as it does in forced CCM. As a result, the efficiency in pulse skip mode is improved compared to forced CCM operation.

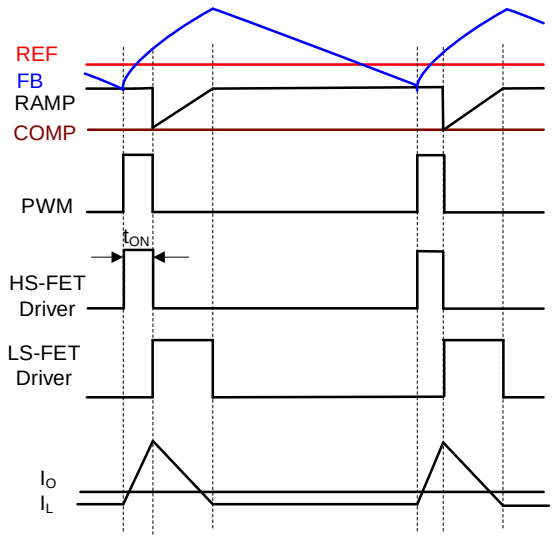


Figure 4: Pulse Skip at Light-Load

As the output current increases from light load, the time period during which the current modulator regulates becomes shorter. The HS-FET turns on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be calculated with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (1)$$

Where f_{SW} is the switching frequency.

The MP8792 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MP8792 can be configured to operate in forced CCM, even under light-load conditions (see Table 1).

Mode Selection

The MP8792 provides both forced CCM operation and pulse skip mode operation under light-load conditions. The MP8792 has three options for switching frequency: 600kHz, 800kHz, and 1000kHz. The operation mode and switching frequency are selected by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: Mode Selection

Mode	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
243kΩ (±20%) to GND	Pulse skip	800kHz
121kΩ (±20%) to GND	Pulse skip	1000kHz
GND	Forced CCM	600kHz
30.1kΩ (±20%) to GND	Forced CCM	800kHz
60.4kΩ (±20%) to GND	Forced CCM	1000kHz

Soft Start (SS)

The minimum soft-start time is 1ms; it can be increased by adding a soft-start capacitor between TRK/REF and VSNS-.

The total SS capacitor value can be estimated with Equation (2):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times 36\mu A}{0.6(V)} \quad (2)$$

Output Voltage Tracking and Reference

The MP8792 provides an analog input pin (TRK/REF) to track another power supply or accept an external reference. When an external voltage signal is connected to TRK/REF, it acts as a reference for the MP8792 output voltage. V_{FB} follows this external voltage signal, and the soft-start settings are ignored. The TRK/REF

input signal ranges from 0.3V to 1.4V. During initial start-up, TRK/REF must reach 600mV to ensure proper operation. After that, it can be set to any value between 0.3V and 1.4V.

Pre-Biased Start-Up

The MP8792 has been designed for a monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the high-side and low-side MOSFETs until the voltage on the TRK/REF capacitor exceeds the sensed output voltage at FB. If the BST voltage (from BST to SW) is below 2.3V before the TRK/REF voltage reaches the pre-biased FB level, the LS-FET turns on to allow the BST voltage to be charged through VCC. The LS-FET turns on for narrow pulses, so the drop in the pre-biased level is negligible.

Output Voltage Discharge

When the MP8792 is disabled through EN, it enables output voltage discharge mode. This causes both the HS-FET and LS-FET to latch off. A discharge FET connected between SW and PGND turns on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once V_{FB} drops below 10% of V_{REF}, the discharge FET turns off.

Current Sense and Over-Current Protection (OCP)

The MP8792 features an on-die current sense (CS) and a configurable positive current limit threshold.

The current limit is active when the MP8792 is enabled. When the LS-FET is on, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, V_{CS} is proportional to the SW current cycle by cycle. The HS-FET turns on only when V_{CS} drops below the internal over-current protection (OCP) voltage threshold (V_{LIM}) while the LS-FET is on to limit the SW valley current cycle by cycle.

Calculate the current limit threshold setting from RCS with Equation (3):

$$R_{CS}(\Omega) = \frac{V_{LIM}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_{SW}})} \quad (3)$$

Where, V_{LIM} = 1.2V, G_{CS} = 20μA/A, and I_{LIM} is the desired output current limit (in A).

OCP hiccup mode is active 3ms after the MP8792 is enabled. Once OCP hiccup is active, if the MP8792 detects an over-current condition for 31 consecutive cycles, or if V_{FB} drops below the under-voltage protection (UVP) threshold, the device enters hiccup mode. In hiccup mode, the MP8792 latches off the HS-FET immediately, and latches off the LS-FET after zero-current cross detection (ZCD). Meanwhile, the TRK/REF capacitor is also discharged. After about 11ms, the MP8792 automatically tries to soft start.

If the over-current condition remains after 3ms of running, the MP8792 repeats this operation cycle until the over-current condition disappears. Then the output voltage smoothly rises back to the regulation level.

Negative Inductor Current limit

When the LS-FET detects a -9A current, the part turns off the LS-FET for 200ns to limit the negative current.

Output Sinking Mode (OSM)

The MP8792 employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When V_{FB} exceeds 104% of V_{REF} but is below the OVP threshold, it triggers OSM. During OSM, the LS-FET remains on until it reaches the -5.5A negative current limit. Upon reaching -5.5A, the LS-FET turns off for 200ns; the HS-FET turns on during this period. After 200ns, the LS-FET turns on again. The MP8792 maintains this operation until V_{FB} drops below 102% of V_{REF}. Once it does, the MP8792 exits OSM after 15 consecutive cycles of forced CCM.

Over-Voltage Protection (OVP)

The MP8792 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides hiccup over-voltage protection (OVP).

If V_{FB} exceeds 116% of V_{REF}, it triggers OVP. The LS-FET remains on until it reaches the low-side negative current limit (NOCP). Once it reaches NOCP, the LS-FET turns off for 200ns; the HS-FET turns on during this period.

After 200ns, the LS-FET turns on again. The MP8792 repeats this operation to discharge the over-voltage on the output. The device exits this mode when V_{FB} drops below 105% of V_{REF}.

Over-Temperature Protection (OTP)

The MP8792 has over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off and discharges the TRK/REF capacitors. This is a non-latch protection. There is about 30°C hysteresis. Once the junction temperature drops to about 130°C, a soft start is initiated. The OTP function is effective once the MP8792 is enabled.

Output Voltage Setting and Remote Output Voltage Sensing

First, choose a value for R1. Then R2 can be calculated with Equation (4):

$$R_2(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_1(k\Omega) \quad (4)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is recommended in parallel with R1. R1 and C_{FF} add an extra zero frequency (f_Z) to the system, which improves loop response. R1 and C_{FF} are selected so that the zero frequency formed by R1 and C_{FF} is between 20kHz and 60kHz. The extra zero frequency can be estimated with Equation (5):

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}} \quad (5)$$

Power Good (PGOOD)

The MP8792 has a power good (PGOOD) output. PGOOD is the open drain of a MOSFET. Connect PGOOD to VCC or another external voltage source (below 3.6V) through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PGOOD is pulled to GND before TRK/REF is ready. After V_{FB} reaches 92.5% of V_{REF} and a .08ms delay, PGOOD is pulled high.

When V_{FB} drops to 80% of V_{REF} or exceeds 116% of the nominal V_{REF}, PGOOD is latched low. PGOOD can only be pulled high again after a new soft start.

If the input supply fails to power the MP8792, PGOOD is clamped low even though PGOOD is tied to an external DC source through a pull-up resistor. Figure 5 shows the relationship between the PGOOD voltage and the pull-up current.

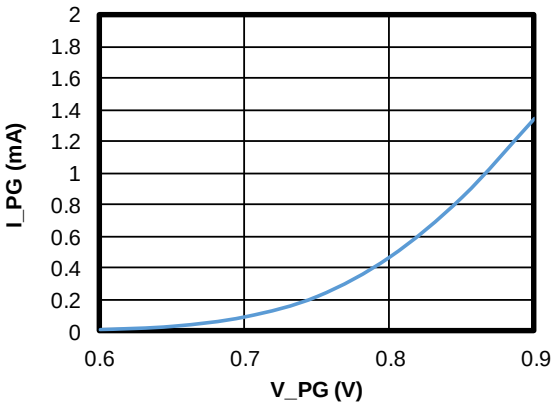


Figure 5: PGOOD Clamped Voltage vs. Pull-Up Current

EN Configuration

The MP8792 turns on when EN goes high, and it turns off when EN goes low. Do not float EN. EN can be driven by an analog or digital control logic signal to enable or disable the device.

The MP8792 provides accurate EN thresholds, so a resistor divider from VIN to AGND can program the input voltage at which the MP8792 is enabled. This is highly recommended for an application where there is no dedicated EN control logic signal, to avoid possible UVLO bouncing during start-up and shutdown. The resistor divider values can be calculated with Equation (6):

$$V_{IN\_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (6)$$

Where VIH_{EN} is typically 1.22V. R_{UP} and R_{DOWN} should be chosen so that V_{EN} does not exceed 3.6V when V_{IN} reaches its maximum value.

EN can be directly connected to VIN through a pull-up resistor (R_{UP}). R_{UP} should be chosen so that the maximum current going to EN is 50μA. R_{UP} can be estimated with Equation (7):

$$R_{UP}(k\Omega) = \frac{VIN_{MAX}(V)}{0.05(mA)} \quad (7)$$

APPLICATION INFORMATION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors for optimal performance. While designing the PCB layout, place the input capacitors as close to IN as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R and X7R ceramic dielectrics because they are fairly stable over a wide temperature range, and they offer low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs when $V_{IN} = 2V_{OUT}$, calculated with Equation (11):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (11)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors.

Estimate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (12)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

The ESR dominates the switching frequency impedance for the POSCAP capacitors. For simplification, the output ripple can be calculated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

Selecting the Inductor

The inductor supplies constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage. However, it has a larger physical size, a higher series resistance, and a lower saturation current. It is usually recommended to select an inductor value that allows the inductor peak-to-peak ripple current to be 30% to 40% of the maximum switch current limit. Design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value using Equation (15):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (16):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists our power inductor recommendations. Select a part number based on your design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AY1265	0.47µH	MPS

Visit MonolithicPower.com under Products > Inductors for more information.

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Place major MLCC capacitors on the same layer as the MP8792.
3. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
4. For the QFN-21 package, a 0402 capacitor with a minimum 1µF value is required.
5. Place the 0402 capacitor on the right side of the IC.
6. Extend VIN to the right side and connect it to the 0402 capacitor.
7. Place at least two 20/10 mil vias on the ground side of the capacitor to the inner solid ground plane.
8. Place as many PGND vias as possible close to PGND, to minimize parasitic impedance and thermal resistance.
9. Place the VCC decoupling capacitor close to the device.
10. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
11. Place the BST capacitor as close to BST and SW as possible. Use traces (with a width of 20 mil or wider) to route the path. It is recommended to use a bootstrap capacitor between 0.1µF and 1µF.
12. Place the REF capacitor close to TRK/REF to VSNS-.
13. If a via must be placed on the PGOOD pad, place it at least 10mm away from the positive side of the first input decoupling capacitor, close to the IC.

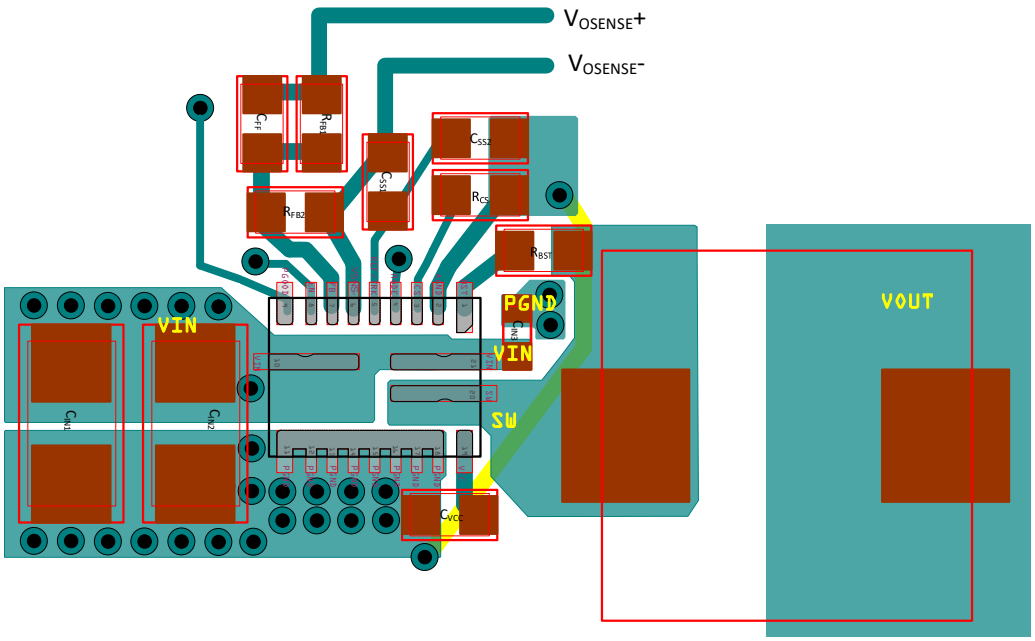
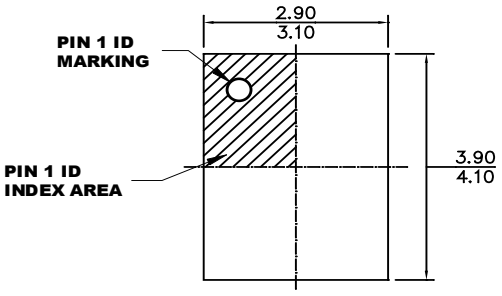


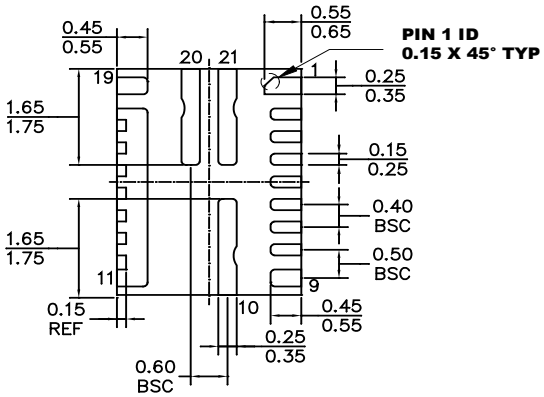
Figure 6: Recommended PCB Layout (QFN-21)

PACKAGE INFORMATION

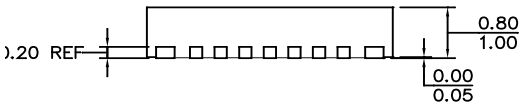
QFN-21 (3mmx4mm)



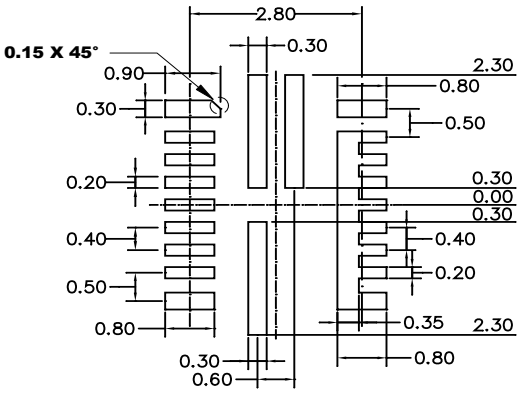
TOP VIEW



BOTTOM VIEW



SIDE VIEW

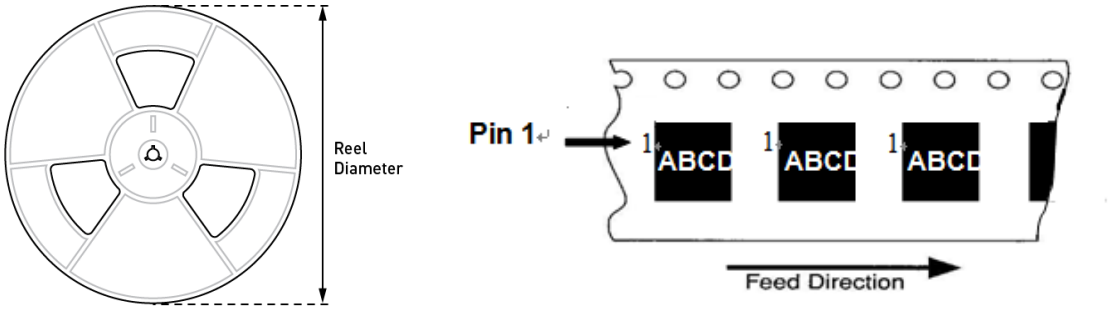


RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PINS 1, 9, 10, 11, 19, 20, AND 21 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8792GLE	QFN-21 (3mmx4mm)	5000	N/A	13in	12mm	8mm