# MP8886

## 45V Input, Dual 3A/Single 6A Output, Digital, Configurable, Synchronous Buck Converter

## DESCRIPTION

The MP8886 is a 45V input, dual-phase, dual-output, high-efficiency, synchronous step-down converter with a PMBus control interface and multiple-time programmable (MTP) memory. The device can achieve up to 3A of continuous output current ($I_{OUT}$) for two channels or up to 6A of continuous $I_{OUT}$ for a single channel, with excellent load and line regulation across a wide input voltage ($V_{IN}$) range.

The output voltage ($V_{OUT}$) can be controlled on the fly via the PMBus serial interface. $V_{OUT}$ can be set between 0.6V and 24V. The voltage transition rate, switching frequency ($f_{SW}$), and power saving modes can also be configured via the PMBus interface.

Peak current mode control provides fast transient response and eases loop stabilization. Full protection features include $V_{IN}$ under-voltage lockout (UVLO) protection, over-voltage protection (OVP), over-current protection (OCP), and thermal shutdown.

The MP8886's MTP memory provides flexible configuration options. The device can be paralleled with up to four phases, and it has an automatic phase shift function for applications with a higher $I_{OUT}$. The integrated, internal high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively) provide high efficiency without the use of an external Schottky diode.

With internal compensation and a feedback divider, the MP8886 offers a very compact solution with a minimal number of readily available, standard external components. The MP8886 is available in a TQFN-26 (5mmx5mm) package.

## FEATURES

- Wide 4V to 45V Input Voltage ($V_{IN}$) Range
- Wide 0.6V to 24V Output Voltage ($V_{OUT}$) Range
- Output Current ($I_{OUT}$) Range:
  - Dual Output: Up to 3A
  - Dual-Phase, Single Output: Up to 6A
  - Dual-Phase, Single Inductor: Up to 6A
  - Multiple Paralleled ICs: Up to 36A
- 150kHz to 2.2MHz Configurable $f_{SW}$ Synchronized to an External Clock
- Internal 62mΩ/34mΩ Low $R_{DS(ON)}$ MOSFETs
- Frequency Spread Spectrum (FSS) for Reduced EMI
- Output OVP, UVP, OCP, and Thermal Shutdown
- Low-Dropout (LDO) Mode
- Telemetry Readback for $V_{IN}$, $V_{OUT}$, Input Current ($I_{IN}$), $I_{OUT}$, Temperature, and Faults
- Configurable via the MTP:
  - $V_{OUT}$
  - $f_{SW}$
  - Compensation Network
  - Output OCP, OVP, and UVP Thresholds
  - Input OVP and UVLO Thresholds
  - Selectable Advanced Asynchronous Modulation (AAM) Mode and Forced Continuous Conduction Mode (FCCM)
- CRC Protection for MTP Integrity
- Available in a TQFN-26 (5mmx5mm) Package

MPL Optimized Performance with MPS MPL-AY6050 Inductor Series

## APPLICATIONS

- DC/DC Power Systems
- USB Power Delivery (PD) and USB Type-C Applications

# TYPICAL APPLICATION

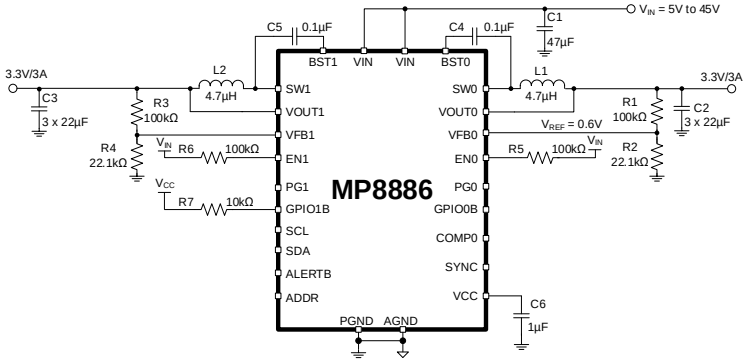
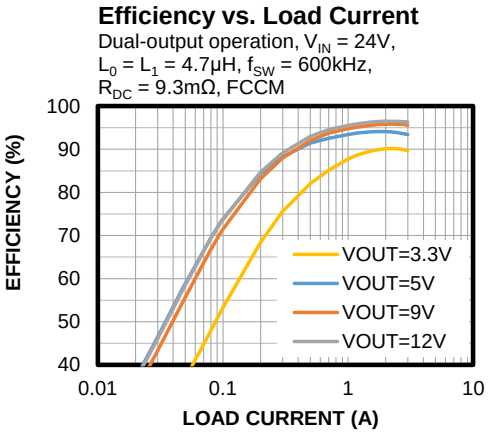



**Figure 1: Dual-Output Operation**



## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP8886GUT-0000 | TQFN-26 (5mmx5mm) | *See Below* | 1 |
| MP8886GUT-0002 | TQFN-26 (5mmx5mm) | *See Below* | |
| MP8886GUT-xxxx** | TQFN-26 (5mmx5mm) | *See Below* | |
| EVKT-MP8886 | Evaluation kit | - | - |

*For Tape & Reel, add suffix -Z (e.g. MP8886GUT-xxxx-Z).

** "xxxx" is the configuration code identifier for the register settings stored in the multiple-time programmable (MTP) memory, which can be configured by the user. Each "x" can be a hexadecimal value between 0 and F. "0000" is the default code when using an internal feedback divider, and "0002" is the default code when using an external feedback divider. For custom configurations, contact an MPS FAE to create a unique code.

## TOP MARKING (MP8886GUT)

MPSYYWW
MP8886
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP8886: Part number
LLLLLLL: Lot number

## EVALUATION KIT EVKT-MP8886

EVKT-MP8886 kit contents (1) (items below can be ordered separately):

| # | Part Number | Item | Quantity |
|---|---|---|---|
| 1 | EVL8886-U-00A | MP8886 evaluation board | 1 |
| 2 | EVKT-USBI2C-02 | Includes one USB-to-I²C communication interface device, one USB cable, and one ribbon cable | 1 |
| 3 | MP8886GUT-0000 | The MP8886, which can be configured via the MTP | 2 |
| 4 | Online resources | Include MPS's Virtual Bench Pro 4.0 | - |

**Order directly from MonolithicPower.com or our distributors.**

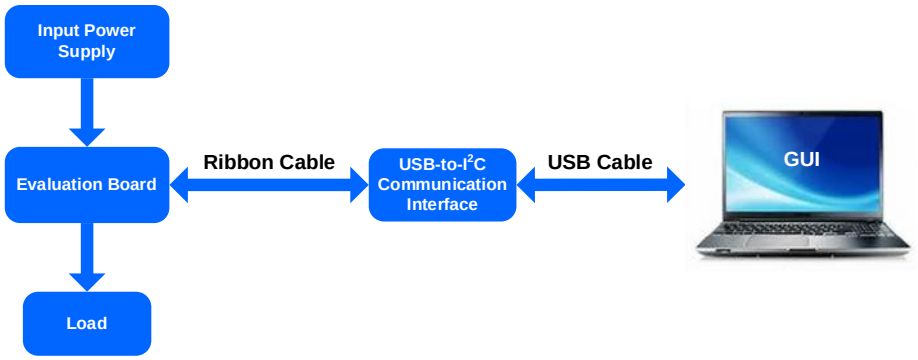


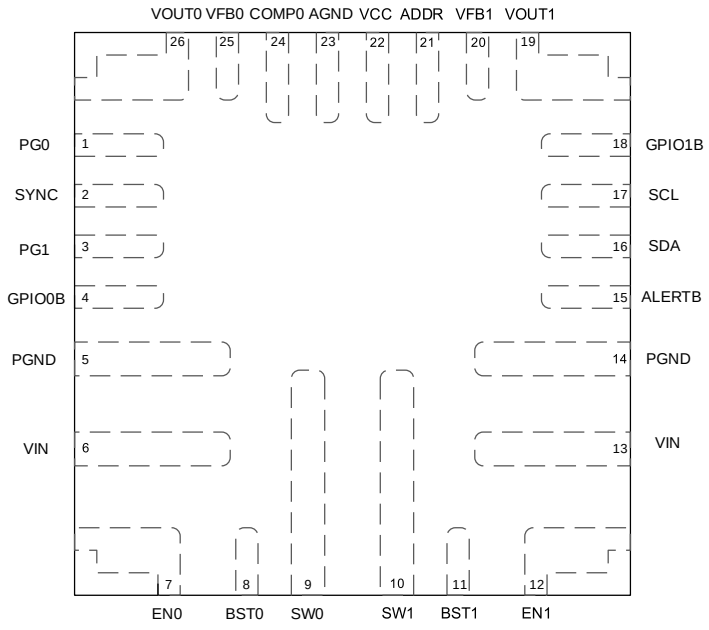

**Figure 2: Evaluation Kit Set-Up**

**Note:**

1) $V_{IN}$ should exceed 7V when using the MTP. To use the evaluation kit, download the GUI from the MPS website or contact an MPS FAE.

# PACKAGE REFERENCE

**TOP VIEW**




**TQFN-26 (5mmx5mm)**

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | PG0 | **Channel 0 power good indication.** If output over-voltage protection (OVP) or under-voltage protection (UVP) is triggered on channel 0, the PG0 pin is pulled low. PG0 is an open-drain output that requires an external pull-up resistor. Connect PG0 to AGND or float PG0 if not used. |
| 2 | SYNC | **Synchronized to external clock signal.** The SYNC pin can be configured as a synchronous input or output via the PMBus. |
| 3 | PG1 | **Channel 1 power good indication.** If output OVP or UVP is triggered on channel 1, the PG1 pin is pulled low. PG1 is an open-drain output that requires an external pull-up resistor. Connect PG1 to AGND or float PG1 if not used. |
| 4 | GPIO0B | **Channel 0 general I/O port.** The GPIO0B pin can be set as a digital output for fault indication. If input OVP, output OVP, output UVP, over-current protection (OCP), or thermal shutdown is triggered on channel 0, GPIO0B is pulled low. Connect GPIO0B to AGND or float GPIO0B if not used. See the General I/O Ports (GPIO) section on page 20 for more information. |
| 5, 14 | PGND | **Power ground.** The PGND pin is the reference ground of the regulated output voltage ($V_{OUT}$). Connect PGND to larger copper areas at the negative terminals of the input and output capacitors. |
| 6, 13 | VIN | **Input voltage.** The VIN pin supplies all power to the converter. Place a decoupling capacitor between VIN and PGND. Place this capacitor as close as possible to the IC to reduce switching spikes. Make the VIN connection using a wide PCB trace. |
| 7 | EN0 | **Channel 0 enable.** Pull the EN0 pin high to turn channel 0 on; pull EN0 low to turn it off. Do not float EN0. |
| 8 | BST0 | **Channel 0 bootstrap.** Connect a capacitor between the SW0 and BST0 pins to form a floating supply across the high-side MOSFET (HS-FET) driver. |
| 9 | SW0 | **Channel 0 switch output.** Make the connection between the SW0 pin and the inductor using a wide PCB trace. |
| 10 | SW1 | **Channel 1 switch output.** Make the connection between the SW1 pin and the inductor using a wide PCB trace. |
| 11 | BST1 | **Channel 1 bootstrap.** Connect a capacitor between the SW1 and BST1 pins to form a floating supply across the HS-FET driver. |
| 12 | EN1 | **Channel 1 enable.** Pull the EN1 pin high to turn channel 1 on; pull EN1 low to turn it off. Do not float EN1. |
| 15 | ALERTB | **Alert output.** If a fault or warning is indicated by STATUS_WORD (79h), the ALERTB pin is pulled low. ALERTB is an open-drain output that requires an external pull-up resistor. Connect ALERTB to AGND or float ALERTB if not used. |
| 16 | SDA | **PMBus serial data.** Pull the SDA pin up to the VCC voltage ($V_{CC}$) if not used. |
| 17 | SCL | **PMBus serial clock.** Pull the SCL pin up to $V_{CC}$ if not used. |
| 18 | GPIO1B | **Channel 1 general I/O port.** The GPIO1B pin can be set as a digital output for fault indication or as an analog input. When set as a digital output, input OVP, output OVP, output UVP, OCP, or thermal shutdown is triggered on channel 1, GPIO1B pulls low. When set as an analog input, GPIO1B sets the operation mode via a resistor connected to AGND. Connect GPIO1B to AGND or float GPIO1B if not used. See the General I/O Ports (GPIO) section on page 20 for more information. |
| 19 | VOUT1 | **Channel 1 sense input.** Connect the VOUT1 pin to the channel 1 $V_{OUT}$. VOUT1 is also used for the $V_{OUT}$ bias input. See the Internal Regulator section on page 19 for more information. |
| 20 | VFB1 | **Channel 1 feedback voltage input for external feedback divider mode.** Connect VFB1 to a voltage divider to set the initial $V_{OUT}$ for external feedback divider mode. Float VFB1 or connect VB1 to AGND for internal feedback divider mode. |

## PIN FUNCTIONS *(continued)*

| Pin # | Name | Description |
|---|---|---|
| 21 | ADDR | **PMBus address setting.** The ADDR pin sets the lower 3 bits of the PMBus address via a resistor connected to AGND (see Table 2 on page 24). |
| 22 | VCC | **Internal 4.9V LDO regulator output.** Decouple the VCC pin using a 1µF capacitor. |
| 23 | AGND | **Analog ground.** The AGND pin is the ground for the internal logic and signal circuit. AGND is not internally connected to PGND. Ensure that AGND is connected to PGND in the PCB layout. |
| 24 | COMP0 | **Compensation for parallel operation.** For applications with multiple ICs, connect the COMP0 pins of all ICs together. Float COMP0 for applications with a single IC. |
| 25 | VFB0 | **Channel 0 feedback voltage input for external feedback divider mode.** Connect the VFB0 pin to a voltage divider to set the initial $V_{OUnT}$ for external feedback divider mode. VFB0 should be floating or connected to GND in internal feedback divider mode. |
| 26 | VOUT0 | **Channel 0 sense input.** Connect the VOUT0 pin to the channel 0 $V_{OUT}$. VOUT0 is also used for the $V_{OUT}$ bias input. See the Internal Regulator section on page 19 for more information. |

## ABSOLUTE MAXIMUM RATINGS (2)

$V_{IN}$ ..... -0.3V to +48V
$V_{SWx}$ ..... -0.3V (-5V for <10ns) to $V_{IN}$ + 0.3V (+49V for <10ns)
$V_{ENx}$ ..... -0.3V to +45V
$V_{BSTx}$ ..... $V_{SW}$ + 5.5V
$V_{CC}$ ..... -0.3V to +5.5V
$V_{OUTx}$ ..... 0V to 28V
$V_{COMP0}$ ..... -0.3V to +5V
$V_{PG0}$ ..... -0.3V to +5.2V
All other pins ..... -0.3V to +5.5V
Continuous power dissipation ($T_A$ = 25°C) (3)
TQFN-26 (5mmx5mm) ..... 5.43W
Junction temperature ($T_J$) ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

### *ESD Ratings* (4)

Human body model (HBM) ..... ±2kV
Charged-device model (CDM) ..... ±750V

### *Recommended Operating Conditions* (5)

Input voltage ($V_{IN}$) ..... 4V to 45V
Output voltage ($V_{OUT}$) ..... 0.6V to 24V
Operating junction temp ($T_J$) .... -40°C to +125°C

### *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

| | | |
|---|---|---|
| EVL8886-U-00A (6) | 23 | 3 °C/W |
| JESD51-7 (7) | 34.9 | 3.1 °C/W |

**Notes:**

2) Exceeding these ratings may damage the device.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the converter may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) HBM is per JEDEC specification JESD22-A114; CDM is per JEDEC specification JESD22-C101. JEDEC document JEP155 states that a 500V HBM allows for safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that a 250V CDM allows for safe manufacturing with a standard ESD control process.
5) The device is not guaranteed to function outside of its operating conditions.
6) Measured on the EVL8886-U-00A, 4-layer PCB.
7) Measured on a JESD51-7, 4-layer PCB. The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C, typical values are tested at $T_J$ = 25°C (8), unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input voltage ($V_{IN}$) under-voltage lockout (UVLO) rising threshold | $V_{IN\_UVLO\_RISING}$ | 35h = 0x29 | 4.24 | 4.44 | 4.64 | V |
| | | 35h = 0x47 | 7.5 | 7.7 | 7.9 | V |
| $V_{IN}$ UVLO falling threshold | $V_{IN\_UVLO\_FALLING}$ | 36h = 0x26 | 3.9 | 4.1 | 4.3 | V |
| | | 36h = 0x44 | 7.13 | 7.33 | 7.53 | V |
| VIN quiescent current | $I_Q$ | $V_{OUT}$ = 5V, the VO_BIAS bit is enabled, no load | | 12 | | µA |
| | | $V_{FB}$ > $V_{REF}$, the VO_BIAS bit is disabled, no load | | 150 | 250 | µA |
| VIN shutdown current | $I_{SD}$ | $V_{EN}$ = 0V | | | 5 | µA |
| Output voltage | $V_{OUT}$ | 21h = 0x226; D2h, bits[2:0] = 0b010; $T_J$ = 25°C | 3.28 | 3.3 | 3.32 | V |
| | | 21h = 0x226; D2h, bits[2:0] = 0b010; $T_J$ = -40°C to +125°C | 3.21 | 3.3 | 3.39 | V |
| | | 21h = 0x341; D2h, bits[2:0] = 0b010; $T_J$ = 25°C | 4.96 | 5 | 5.04 | V |
| | | 21h = 0x341; D2h, bits[2:0] = 0b010; $T_J$ = -40°C to +125°C | 4.9 | 5 | 5.1 | V |
| | | 21h = 0x3E8; D2h, bits[2:0] = 0b011; $T_J$ = 25°C | 11.76 | 11.96 | 12.16 | V |
| | | 21h = 0x3E8, D2h, bits[2:0] = 0b011; $T_J$ = -40°C to +125°C | 11.72 | 11.96 | 12.2 | V |
| | | 21h = 0x3E8; D2h, bits[2:0] = 0b100; $T_J$ = 25°C | 23.2 | 23.8 | 24.4 | V |
| | | 21h = 0x3E8; D2h, bits[2:0] = 0b100; $T_J$ = -40°C to +125°C | 23.1 | 23.8 | 24.5 | V |
| Default switching frequency | $f_{SW}$ | D4h, bits[2:0] = 3b'011 | 500 | 600 | 700 | kHz |
| SYNC frequency range (9) | $f_{SYNC}$ | Sync clock set range | 150 | | 2200 | kHz |
| SYNC voltage ($V_{SYNC}$) high threshold | $V_{SYNC\_HIGH}$ | | 1.7 | | | V |
| $V_{SYNC}$ low threshold | $V_{SYNC\_LOW}$ | | | | 0.4 | V |
| Minimum on time (9) | $t_{ON\_MIN}$ | Peak current mode | | 100 | | ns |
| Minimum off time (9) | $t_{OFF\_MIN}$ | | | 130 | | ns |
| High-side MOSFET (HS-FET) on resistance per channel | $R_{DS(ON)\_HS}$ | $V_{BST}$ - $V_{SW}$ = 5V | | 62 | 120 | mΩ |
| Low-side MOSFET (LS-FET) on resistance per channel | $R_{DS(ON)\_LS}$ | | | 34 | 70 | mΩ |
| Switch leakage current | $I_{SW\_LKG}$ | $V_{SW}$ = 45V, $T_J$ = 25°C | | | 5 | µA |
| Default soft-start time | $t_{SS}$ | 61h = 0x00 | 0.45 | 0.7 | 0.95 | ms |
| EN voltage ($V_{EN}$) rising threshold | $V_{EN\_RISING}$ | | 1 | 1.2 | 1.4 | V |
| $V_{EN}$ hysteresis | $V_{EN\_HYS}$ | | | 430 | | mV |

## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C, typical values are tested at $T_J$ = 25°C (9), unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Default PG0 upper rising threshold | $V_{PG0\_UP\_RISING}$ | E3h, bit[0] = 0b0 | 112 | 117 | 122 | % of $V_{OUT0}$ |
| Default PG1 upper rising threshold | $V_{PG1\_UP\_RISING}$ | E3h, bit[0] = 0b0 | 110 | 115 | 120 | % of $V_{OUT1}$ |
| PGx upper rising threshold hysteresis | $V_{PGx\_UP\_HYS}$ | D9h, bit[1] = 0b1 | | 10 | | % of $V_{OUT}$ |
| | | D9h, bit[1] = 0b0 | | 5 | | % of $V_{OUT}$ |
| Default PG0 lower rising threshold | $V_{PG0\_LOW\_RISING}$ | E5h, bit[0] = 0b1 | 89 | 92 | 95 | % of $V_{OUT0}$ |
| Default PG1 lower rising threshold | $V_{PG1\_LOW\_RISING}$ | E5h, bit[0] = 0b1 | 81 | 85 | 89 | % of $V_{OUT1}$ |
| PGx lower rising threshold hysteresis | $V_{PGX\_LOW\_HYS}$ | D9h, bit[0] = 0b1 | | 10 | | % of $V_{OUT}$ |
| | | D9h, bit[0] = 0b0 | | 5 | | % of $V_{OUT}$ |
| PGx output low voltage | $V_{PGX\_LOW}$ | $I_{SINK}$ = 1mA | | | 0.3 | V |
| PGx deglitch timer (9) | $t_{PGX\_DEGLITCH}$ | Rising | | 20 | | µs |
| | | Falling | | 12 | | µs |
| VCC regulator voltage | $V_{CC}$ | $I_{CC}$ = 0mA | 4.7 | 4.9 | 5.1 | V |
| VCC regulation | | $I_{VCC}$ = 5mA | | 0.5 | 1 | % |
| Default peak current limit ($I_{LIMIT}$) | $I_{LIMIT\_PEAK}$ | E0h, bits[6:4] = 3b'101 | 3.3 | 6 | 8.7 | A |
| Default valley $I_{LIMIT}$ | $I_{LIMIT\_VALLEY}$ | E0h, bits[2:0] = 3b'011 | 3 | 5 | 7 | A |
| Input over-voltage protection (OVP) threshold | $V_{IN\_OVP}$ | 55h = 0x14E | 34 | 36 | 38 | V |
| Input OVP hysteresis | $V_{IN\_OVP\_HYS}$ | D9h, bit[3] = 0b0 | | 1.2 | | V |
| | | D9h, bit[3] = 0b1 | | 2.2 | | V |
| Default thermal shutdown (9) | $T_{SD}$ | E7h = 0x96 | | 150 | | °C |
| Default thermal shutdown hysteresis (10) | $T_{SD\_HYS}$ | D9h, bit[4] = 0 | | 25 | | °C |
| **PMBus DC Characteristics (SDA, SCL)** | | | | | | |
| Input high voltage | $V_{IH}$ | | 2.1 | | | V |
| Input low voltage | $V_{IL}$ | | | | 0.8 | V |
| Output low voltage (9) | $V_{OL}$ | $I_{SINK}$ = 1mA | | | 0.4 | V |
| Input leakage current | $I_{LKG}$ | SDA, SCL pulled up with 3.3V | -10 | | +10 | µA |
| SDA and SCL pin capacitance (9) | $C_{PIN}$ | | | | 400 | pF |

## ELECTRICAL CHARACTERISTICS *(continued)*

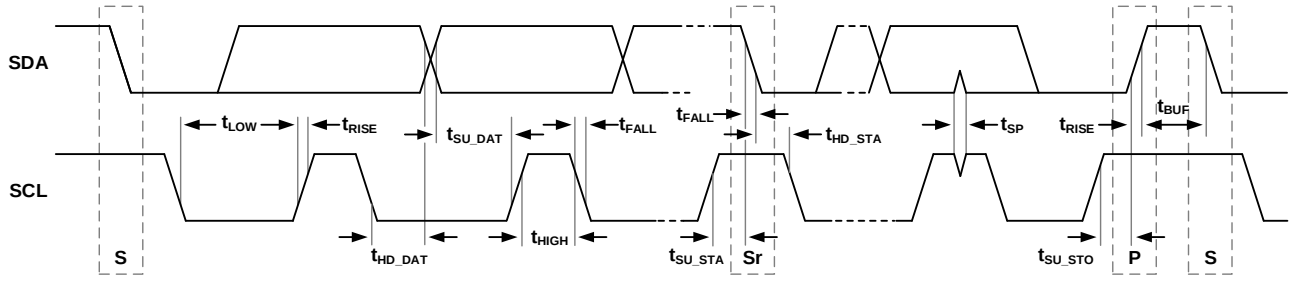
**$V_{IN}$ = 12V, $V_{EN}$ = 2V, $T_J$ = -40°C to +125°C, typical values are tested at $T_J$ = 25°C (9), unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **PMBus Timing Characteristics** | | | | | | |
| SCL clock frequency (9) | $f_{SCL}$ | | | 400 | 1000 | kHz |
| Bus free time between a start and a stop condition (9) | $t_{BUF}$ | | 160 | | | ns |
| Holding time for start command (9) | $t_{HD\_STA}$ | | 160 | | | ns |
| Set-up time for a repeated start command (9) | $t_{SU\_STA}$ | | 160 | | | ns |
| Set-up time for a stop command (9) | $t_{SU\_STO}$ | | 160 | | | ns |
| Data hold time (9) | $t_{HD\_DAT}$ | | | 60 | | ns |
| Data set-up time (9) | $t_{SU\_DAT}$ | | 10 | | | ns |
| Clock low timeout (9) | $t_{LOW\_TO}$ | | 25 | | 35 | ms |
| Clock low period (9) | $t_{LOW}$ | | 160 | | | ns |
| Clock high period (9) | $t_{HIGH}$ | | 60 | | | ns |
| SCL and SDA fall time (9) | $t_{FALL}$ | | 10 | | 300 | ns |
| SCL and SDA rise time (9) | $t_{RISE}$ | | 10 | | 300 | ns |

**Notes:**

8) Tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.
9) Derived by design and characterization. Not tested in production.

## PMBUS-COMPATIBLE INTERFACE TIMING DIAGRAM




**S = Start Condition**
**Sr = Repeated Start Condition**
**P = Stop Condition**

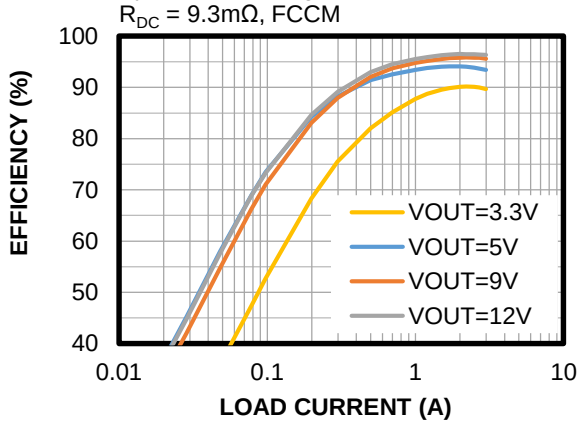
**Figure 2: PMBus-Compatible Interface Timing Diagram**

## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 24V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $T_A$ = 25°C, tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.**

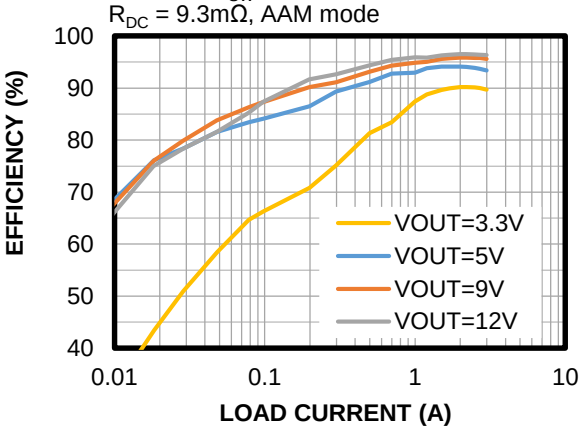
### Efficiency vs. Load Current

Dual-output operation, $V_{IN}$ = 24V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $R_{DC}$ = 9.3mΩ, FCCM



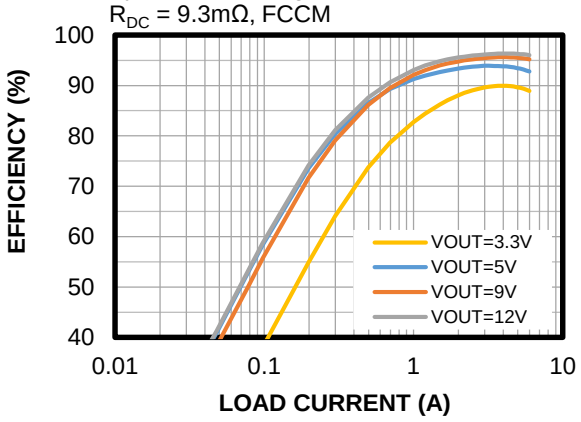

### Efficiency vs. Load Current

Dual-output operation, only one channel is operating, $f_{SW}$ = 600kHz, $R_{DC}$ = 9.3mΩ, AAM mode



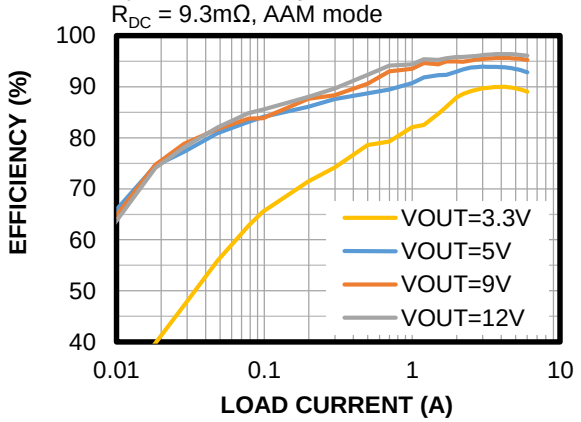

### Efficiency vs. Load Current

Dual-phase, single-output operation, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $R_{DC}$ = 9.3mΩ, FCCM



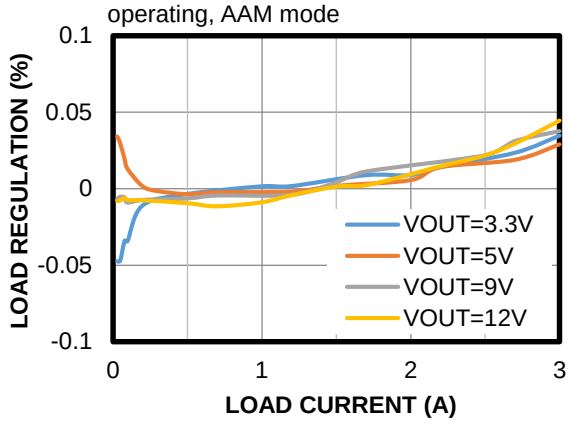

### Efficiency vs. Load Current

Dual-phase, single-output operation, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $R_{DC}$ = 9.3mΩ, AAM mode



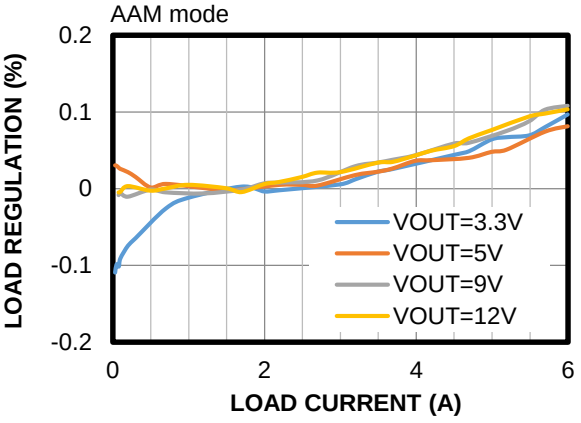

### Load Regulation

Dual-output operation, only one channel is operating, AAM mode




### Load Regulation

Dual-phase, single-output operation, AAM mode

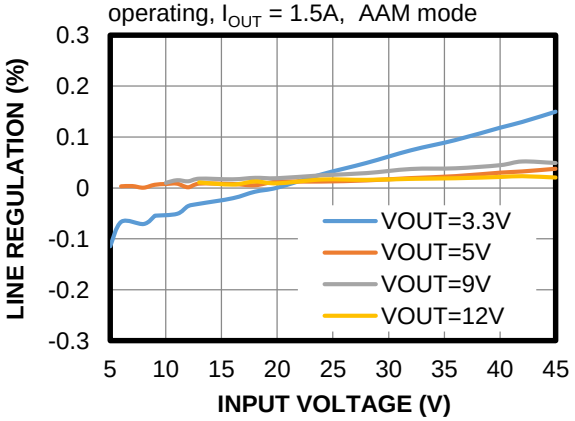


## TYPICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 24V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $T_A$ = 25°C, tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.**

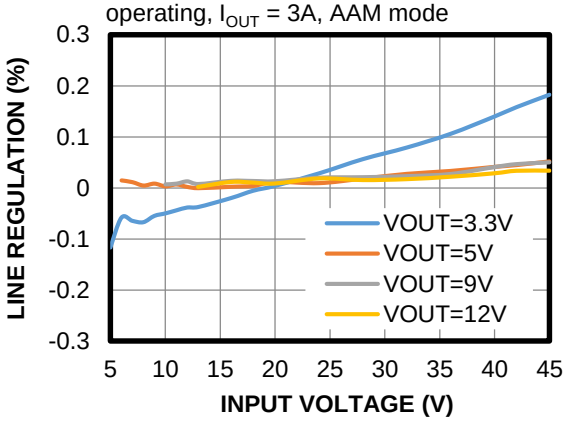
**Line Regulation**

Dual-output operation, only one channel is operating, $I_{OUT}$ = 1.5A, AAM mode




**Line Regulation**

Dual-output operation, only one channel is operating, $I_{OUT}$ = 3A, AAM mode

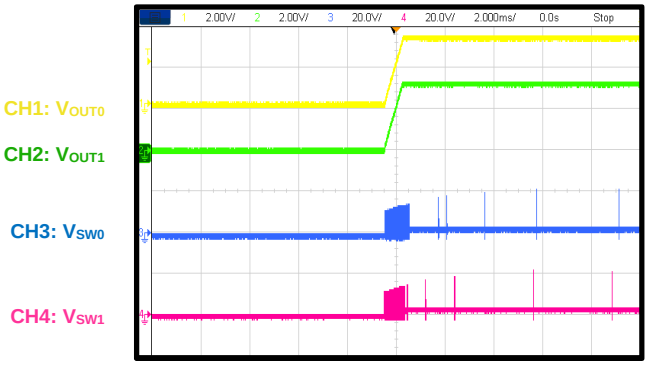


## TYPICAL PERFORMANCE CHARACTERISTICS

**Performance waveforms are tested on the evaluation board. $V_{IN}$ = 24V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $T_A$ = 25°C, tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.**

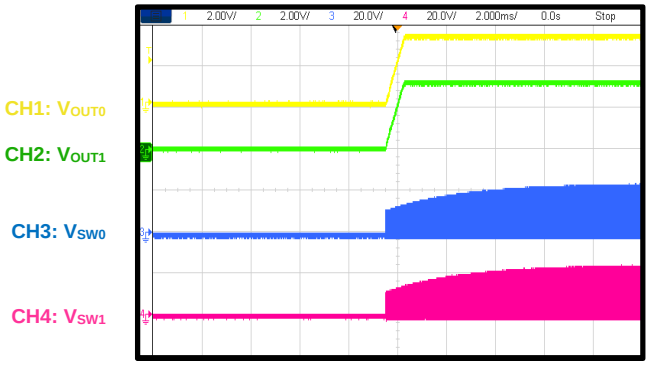
### Start-Up through VIN

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 0A



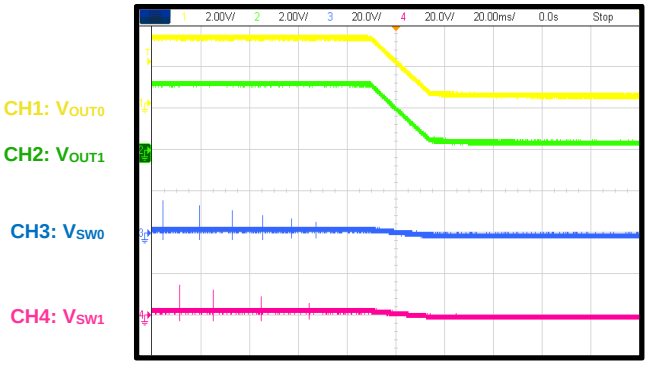

### Start-Up through VIN

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 3A



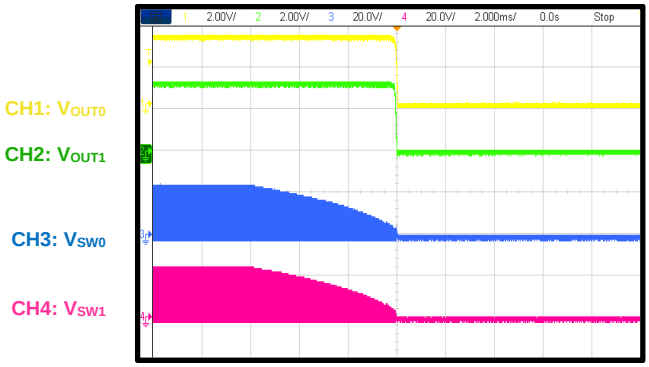

### Shutdown through VIN

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 0A



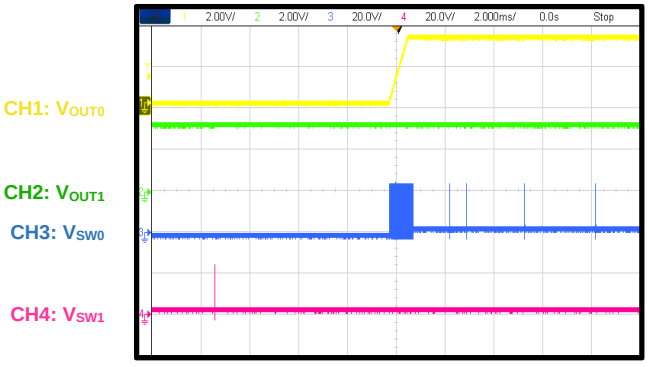

### Shutdown through VIN

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 3A



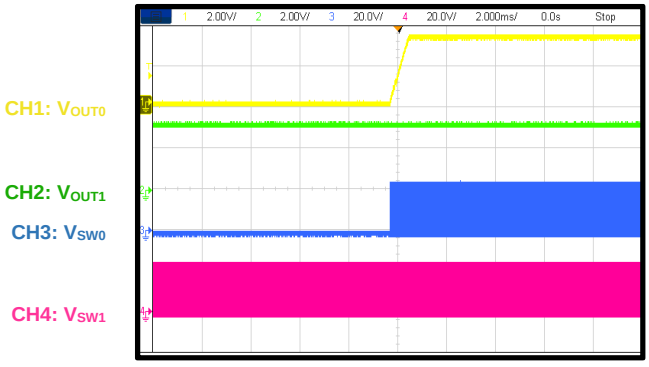

### Start-Up through EN

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 0A. EN1 is high, EN0 turns on




### Start-Up through EN

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 3A. EN1 is high, EN0 turns on

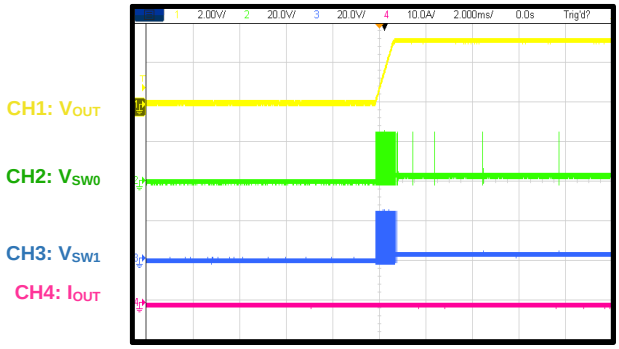


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board. $V_{IN}$ = 24V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $T_A$ = 25°C, tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.**

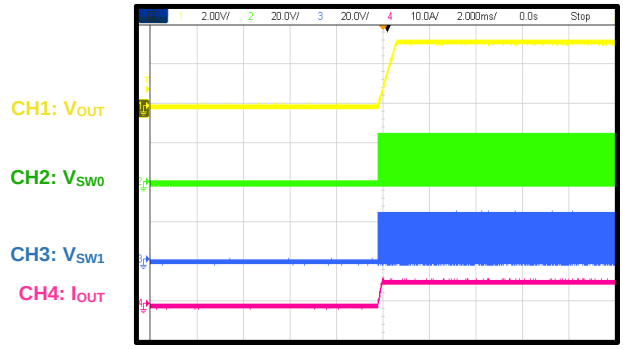
### Start-Up through EN

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 0A, EN1 is high or low,
EN0 turns on



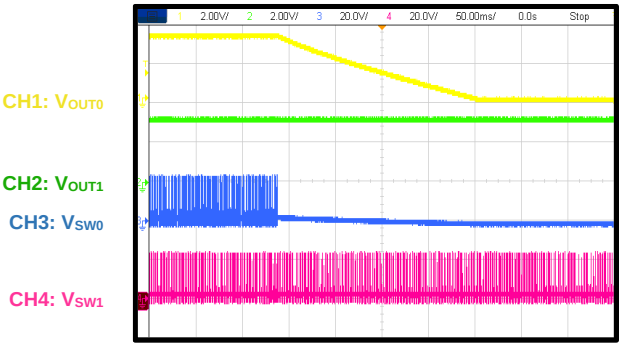

### Start-Up through EN

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A, EN1 is high or low,
EN0 turns on



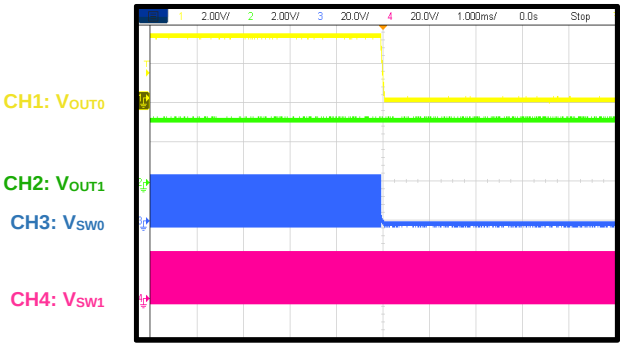

### Shutdown through EN

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V,
$I_{OUT0}$ = $I_{OUT1}$ = 0A, EN1 is high, EN0 turns off



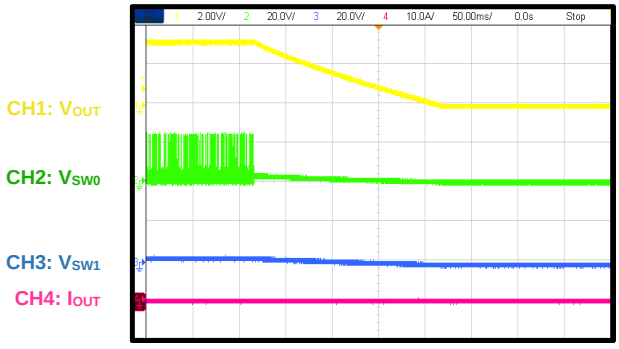

### Shutdown through EN

Dual output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V,
$I_{OUT0}$ = $I_{OUT1}$ = 3A, EN1 is high, EN0 turns off



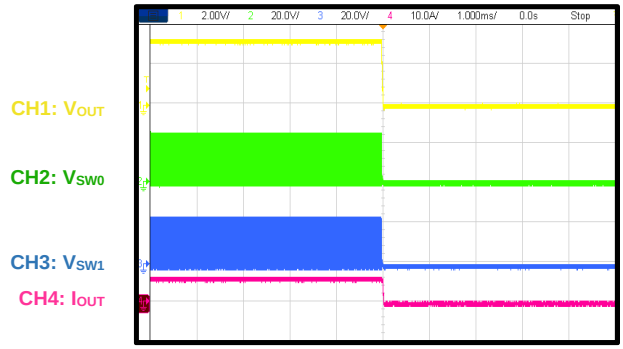

### Shutdown through EN

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 0A. EN1 is high or low,
EN0 turns off




### EN Shutdown

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A, EN1 is high or low,
EN0 turns off

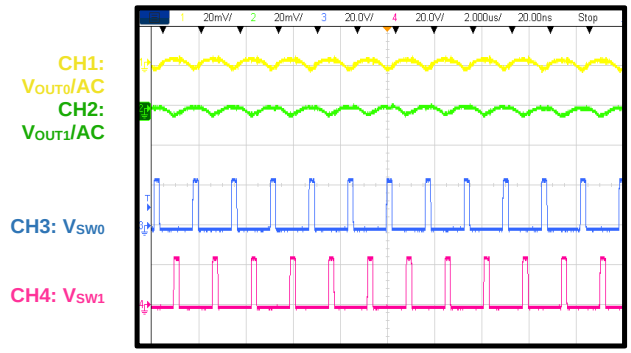


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board. $V_{IN}$ = 24V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $T_A$ = 25°C, tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.**

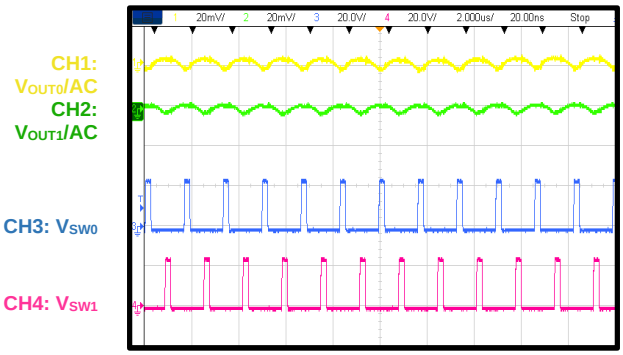
### Steady State

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 1.5A



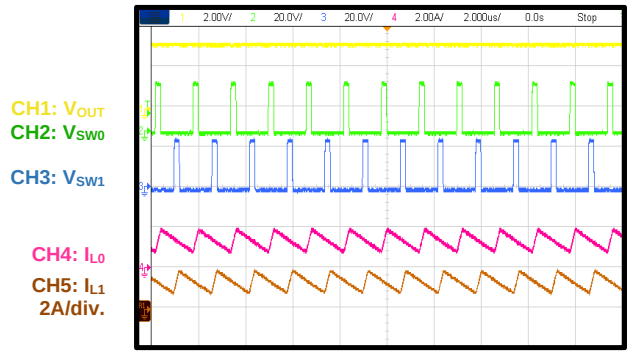

### Steady State

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 3A



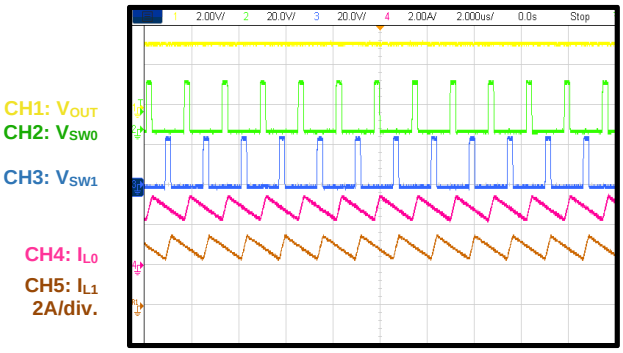

### Steady State

Dual-phase, single-output operation, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 3A



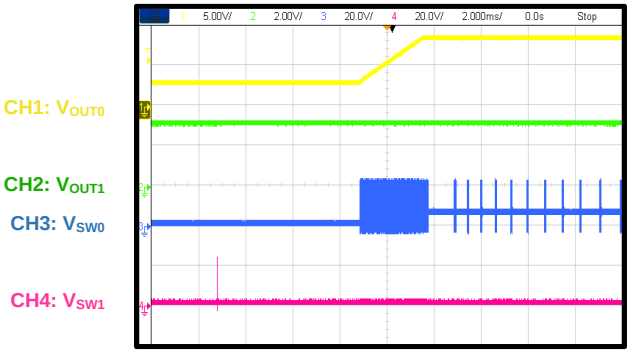

### Steady State

Dual-phase, single-output operation, $V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A



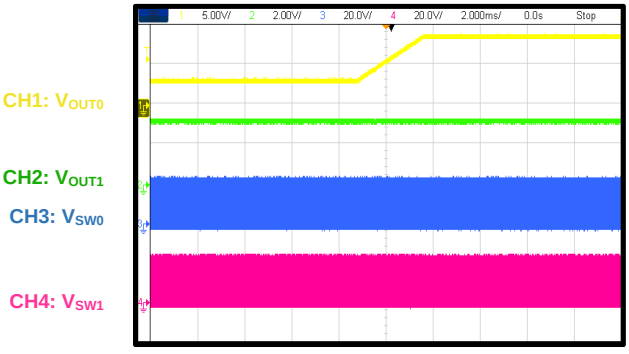

### PMBus VID

Dual-output operation, $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 0A, $V_{OUT0}$ = 3.3V to 9V




### PMBus VID

Dual-output operation, $V_{OUT1}$ = 3.3V, $I_{OUT0}$ = $I_{OUT1}$ = 3A, $V_{OUT0}$ = 3.3V to 9V

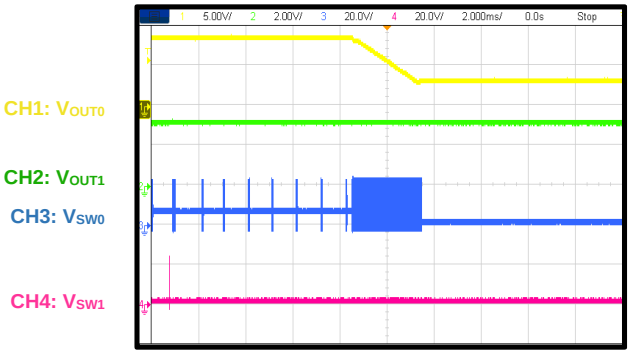


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board. $V_{IN}$ = 24V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $T_A$ = 25°C, tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.**

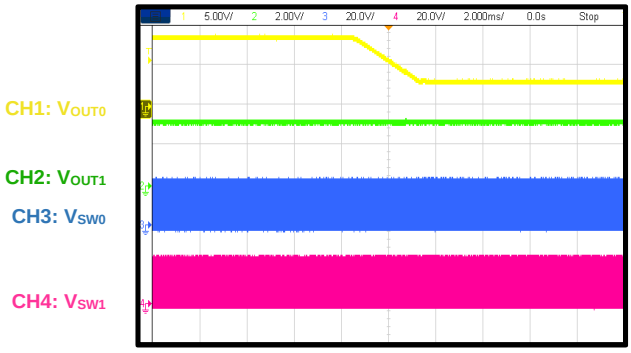
### PMBus VID

Dual-output operation, $V_{OUT1}$ = 3.3V,
$I_{OUT0}$ = $I_{OUT1}$ = 0A, $V_{OUT0}$ = 9V to 3.3V



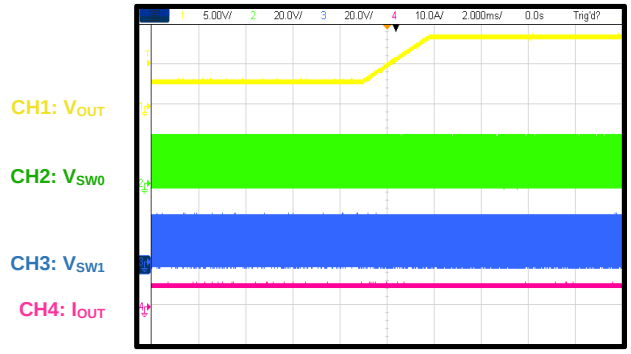

### PMBus VID

Dual-output operation, $V_{OUT1}$ = 3.3V,
$I_{OUT0}$ = $I_{OUT1}$ = 3A, $V_{OUT0}$ = 9V to 3.3V



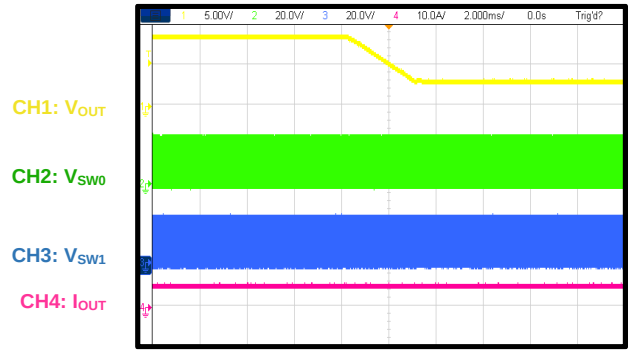

### PMBus VID

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A, $V_{OUT}$ = 3.3V to 9V



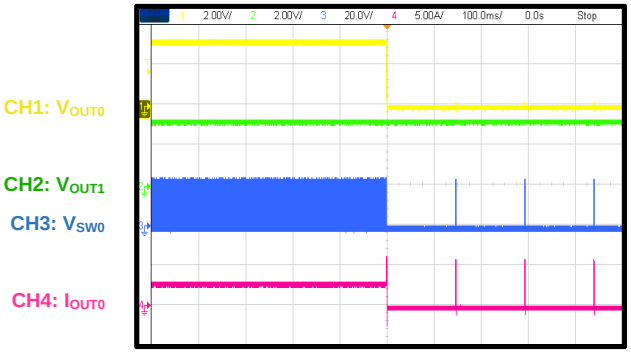

### PMBus VID

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A, $V_{OUT}$ = 9V to 3.3V



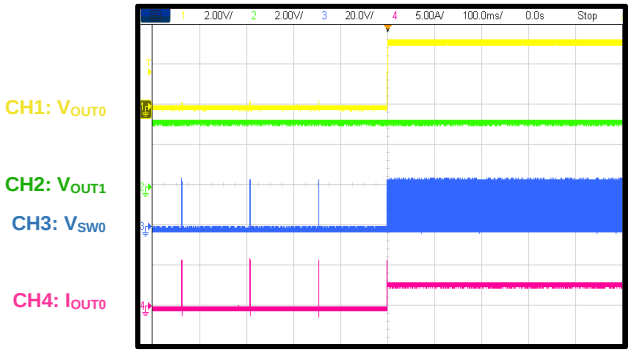

### SCP Entry

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V,
$I_{OUT0}$ = $I_{OUT1}$ = 3A, channel 0 SCP




### SCP Recovery

Dual output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V,
$I_{OUT0}$ = $I_{OUT1}$ = 3A, channel 0 SCP

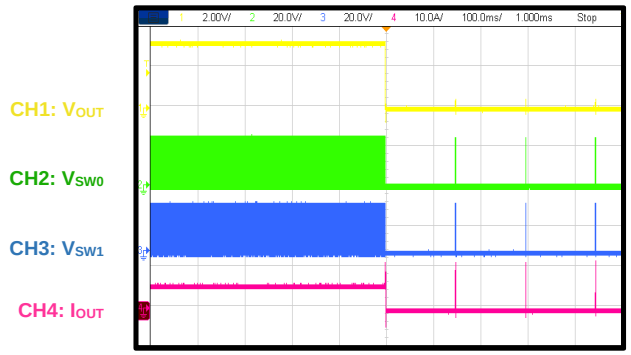


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**Performance waveforms are tested on the evaluation board. $V_{IN}$ = 24V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $L_0$ = $L_1$ = 4.7µH, $f_{SW}$ = 600kHz, $T_A$ = 25°C, tested with the default version of the MP8886 (MP8886GUT-0000), unless otherwise noted.**

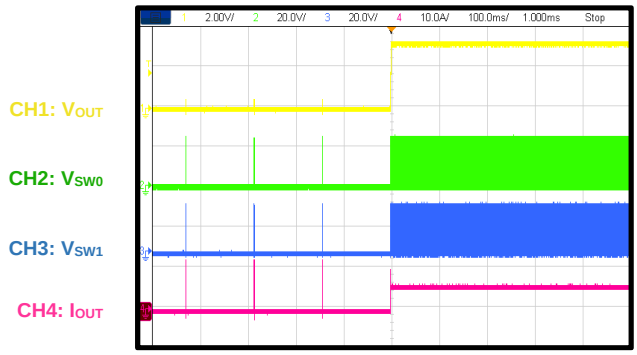
### SCP Entry

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A



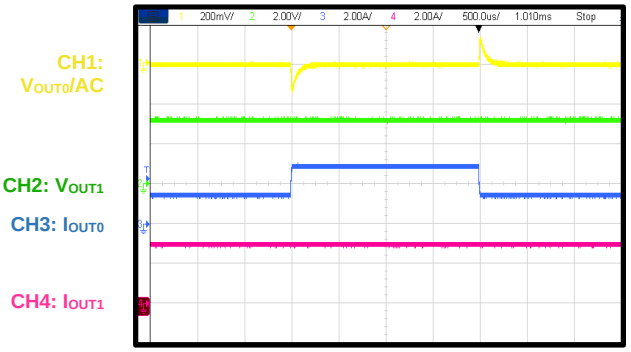

### SCP Recovery

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 6A



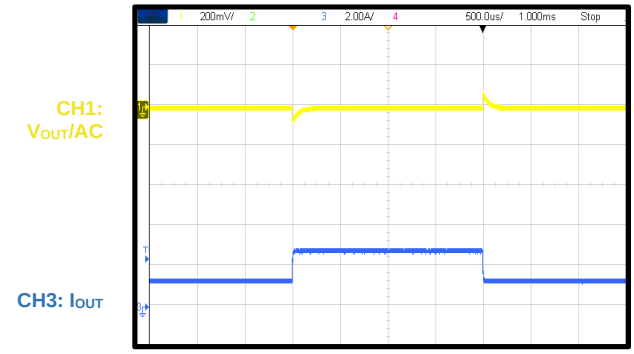

### Load Transient Response

Dual-output operation, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V, $I_{OUT1}$ = 3A, $I_{OUT0}$ = 1.5A to 3A, e-load transient slew rate = 2.5A/µs, $C_{OUT}$ = 3 x 22µF



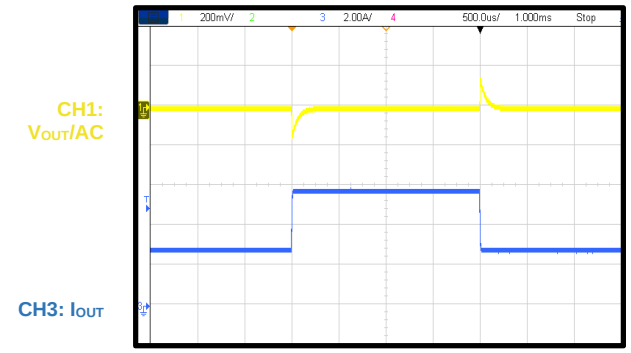

### Load Transient Response

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 1.5A to 3A, e-load transient slew rate = 2.5A/µs, $C_{OUT}$ = 3 x 22µF




### Load Transient Response

Dual-phase, single-output operation,
$V_{OUT}$ = 3.3V, $I_{OUT}$ = 3A to 6A, e-load 2.5A/µs,
$C_{OUT}$ = 3 x 22µF



## FUNCTIONAL BLOCK DIAGRAM

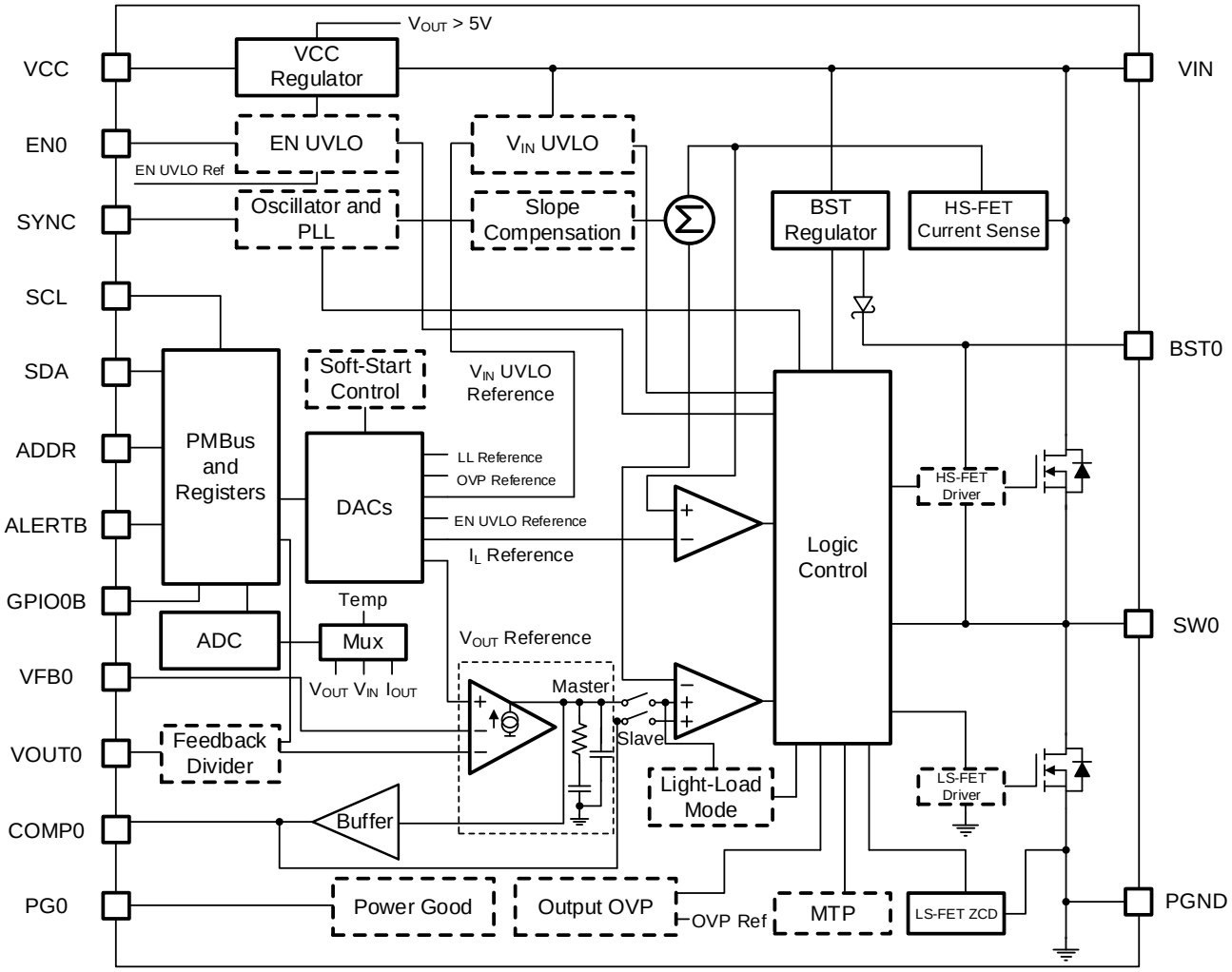



**Figure 3: Functional Block Diagram (Channel 0)**

# OPERATION

The MP8886 is a high-frequency, synchronous step-down converter with built-in high-side and low-side power MOSFETs (HS-FETs and LS-FETs, respectively). The device has a wide input voltage ($V_{IN}$) range, and it can achieve up to 3A of continuous output current ($I_{OUT}$) per channel, or it can be paralleled for up to 6A of continuous $I_{OUT}$. The MP8886 has excellent load and line regulation across the entire -40°C to +125°C junction temperature ($T_J$) range. Multiple MP8886s can also be paralleled for a higher load current capability.

### Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MP8886 operates in fixed-frequency, peak current control mode to regulate the output voltage ($V_{OUT}$). An internal clock initiates the pulse-width modulation (PWM) cycle. At the rising edge of the clock, the HS-FET turns on, and the inductor current ($I_L$) rises linearly to provide energy to the load.

The HS-FET remains on until its current reaches the comparator voltage ($V_{COMP}$), which is the output of the internal error amplifier (EA). $V_{COMP}$ is determined by the difference between the feedback voltage ($V_{FB}$) and the internal, high-precision reference voltage ($V_{REF}$). $V_{COMP}$ determines how much energy should be transferred to the load. $V_{COMP}$ is greater at higher load currents. To adjust $V_{OUT}$, both the feedback divider ratio and the internal $V_{REF}$ can be adjusted via the PMBus.

If the HS-FET turns off, the LS-FET turns on and remains on until the next clock starts. During this period, $I_L$ flows through the LS-FET. To avoid shoot-through, a dead time (DT) is inserted to prevent the HS-FET and LS-FET from turning on at the same time.

If the HS-FET current ($I_{HS}$) does not reach the value set by $V_{COMP}$ in one PWM period, then it remains on until $I_{HS}$ reaches the peak current limit ($I_{LIMIT\_PEAK}$), saving a turn-off operation. See the Over-Current Protection (OCP) section on page 20 for more details.

### Selectable Advanced Asynchronous Modulation (AAM) Mode or Forced Continuous Conduction Mode (FCCM)

At light loads, the MP8886 can operate in advanced asynchronous modulation (AAM) mode and forced continuous conduction mode (FCCM). The mode can be selected via the PMBus. AAM mode optimizes efficiency during light-load or no-load conditions. FCCM maintains a constant switching frequency ($f_{SW}$) and smaller $V_{OUT}$ ripple, but it is less efficient under light loads.

If AAM mode is enabled, the MP8886 enters discontinuous conduction mode (DCM) as $I_L$ approaches 0A. As the load decreases further or if there is no load, the peak $I_L$ ($I_{L\_PEAK}$) drops below the AAM mode peak current threshold set via the PMBus. Then the MP8886 enters AAM mode while consuming a very low quiescent current ($I_Q$) to further improve light-load efficiency.

In AAM mode, the internal clock is blocked, and the MP8886 skips some pulses. If $V_{FB}$ drops below $V_{REF}$, $V_{COMP}$ ramps up until $I_{L\_PEAK}$ exceeds the AAM mode threshold. Then the internal clock is reset, and the crossover time is used as the benchmark for the next clock. This control scheme improves efficiency by scaling down $f_{SW}$ to reduce switching and gate driver losses.

As $I_{OUT}$ increases from light loads, $V_{COMP}$ and $f_{SW}$ also increase. If $I_{OUT}$ exceeds the critical level set by $V_{COMP}$, the MP8886 resumes fixed-frequency PWM control in discontinuous conduction mode (DCM) or FCCM.

In FCCM, the MP8886 operates in fixed-frequency, peak current control mode to regulate $V_{OUT}$, regardless of $I_{OUT}$.

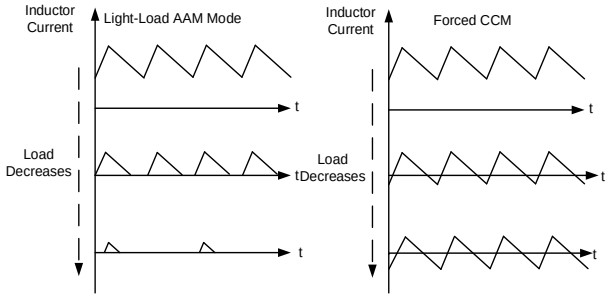



**Figure 4: AAM Mode and FCCM**

### Internal Regulator

A 4.9V internal regulator powers most of the internal circuitry. This regulator takes $V_{IN}$ and operates across the entire $V_{IN}$ range. If $V_{IN}$ exceeds 4.9V, the regulator's output is in full regulation. Lower $V_{IN}$ values result in lower $V_{OUT}$ values. The regulator is enabled once $V_{IN}$ exceeds its under-voltage lockout (UVLO) threshold and either EN0 or EN1 is high. Once both EN0 and EN1 are pulled low, the internal VCC regulator is disabled to reduce power dissipation.

To improve thermal performance, the $V_{OUT}$-biased function can be enabled via the PMBus (MFR_VOUT_CTRL). If $V_{OUTx}$ exceeds 4.8V, VCC and the internal circuitry are powered by $V_{OUTx}$. $V_{OUTx}$ can supply VCC via the VOUTx pin. The MP8886 selects the supply channel automatically, according to $V_{OUT}$ and the operation mode.

### Enable (EN) Control

ENx is a digital control pin that turns the converter on and off. Pull EN0 high to turn channel 0 on; pull EN0 low to turn it off. Pull EN1 high to turn channel 1 on; pull EN1 low to turn it off. If both EN0 and EN1 are pulled low, VCC, the digital clock, and most of the internal circuitry are turned off to reduce current consumption. ENx can tolerate high voltages, and it can be pulled up to VIN.

### Switching Frequency ($f_{SW}$)

The MP8886 has a configurable $f_{SW}$ that can be set between 150kHz and 2.2MHz via the PMBus. The default $f_{SW}$ is 600kHz. $f_{SW}$ can also be set by a logic-level synchronizing signal via the SYNC pin.

### Synchronous Input and Output

The SYNC pin can be configured as a synchronous input or output via the PMBus. When operating as a synchronous input (SYNC in), the internal $f_{SW}$ can be synchronized by an external clock via the SYNC pin. The MFR_PHASE_CTRL register sets the phase shift between the external SYNC in signal and the internal oscillator clock to 0° or 180°.

At start-up, the MP8886 operates at an internal set frequency, then quickly synchronizes to the external clock once soft start (SS) is complete. Ensure that the high amplitude of the SYNC clock exceeds 1.7V and the low amplitude is below 0.4V to drive the internal logic. The recommended external SYNC frequency ($f_{SYNC}$) is between 150kHz and 2.2MHz.

When there is a SYNC clock, the MP8886 operates in FCCM with a fixed frequency. It is recommended that the clock pulses are >200ns.

When the SYNC pin operates as a synchronous output (SYNC out), the device outputs a clock based on the internal oscillator. The SYNC pin does not need to be externally pulled up when operating as SYNC out.

When multiple devices are operating in parallel, the SYNC pins of all the devices should be connected together. The master device should be configured as the SYNC output, and the slave devices should automatically be configured as SYNC in.

### $V_{IN}$ Under-Voltage Lockout (UVLO) Protection

The MP8886 features $V_{IN}$ UVLO to ensure there is reliable output power. If either EN0 or EN1 is active, the MP8886 starts up once $V_{IN}$ exceeds its UVLO rising threshold. The device shuts down when $V_{IN}$ drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. UVLO is a non-latch protection. The $V_{IN}$ UVLO threshold can be configured via the PMBus.

### Soft Start (SS)

To avoid overshoot during start-up, the MP8886 has built-in soft start (SS), which ramps up $V_{OUT}$ with a controlled slew rate. Once the device starts up, the internal circuitry generates a soft-start voltage ($V_{SS}$) that ramps up slowly. If $V_{SS}$ is below the internal $V_{REF}$, then $V_{SS}$ overrides $V_{REF}$ as the EA reference. If $V_{SS}$ exceeds $V_{REF}$, then $V_{REF}$ acts as the reference. At this point, SS completes and the MP8886 enters steady state operation.

The soft-start time ($t_{SS}$) can be configured via the PMBus. If the output is shorted to PGND, $V_{FB}$ is pulled low, and $V_{SS}$ is discharged. The MP8886 initiates another SS once it returns to a normal state.

### Pre-Biased Start-Up

If $V_{FB}$ exceeds $V_{SS}$ during start-up, this means that the output has a pre-biased voltage. Neither the HS-FET nor LS-FET turn on until $V_{SS}$ exceeds $V_{FB}$.

### Power Good (PG) Indication

The MP8886 has power good (PG) indication (PG0 for channel 0 and PG1 for channel 1). The PGx pin is an open-drain output that should be pulled up to a voltage source via a resistor (e.g. 100kΩ). When $V_{IN}$ is present, the MOSFET turns on so that PGx is pulled down to AGND before SS is ready. Once $V_{OUT}$ is outside of its rated voltage range, PGx pulls low to indicate a failure output status. When $V_{OUT}$ is within the rated voltage range, PGx pulls high after a delay (typically 20μs). The PG threshold and hysteresis can be configured via the PMBus.

In applications with multiple phases or devices, only the master device's PG0 pin indicates the PG status.

### General I/O Ports (GPIO)

The MP8886 has two general I/O ports (GPIO0B and GPIO1B). Each GPIO pin can be set as an analog input or digital output via MFR_GPIO_MODE (DCh). When GPIOxB is set as a digital output, it is an open drain that should be pulled up to a voltage source via a resistor (e.g. 100kΩ).

When GPIO0B is set as an analog input, it is a high impedance input with no specific function. When GPIO0B is set as a digital output, it operates as a fault indicator that pulls down if $V_{IN}$ over-voltage protection (OVP), $V_{OUT}$ OVP, $V_{OUT}$ under-voltage protection (UVP), OCP, or thermal shutdown is triggered on channel 0. The MFR_GPIO_CTRL register determines which events control GPIO0B. Connect GPIO0B to AGND or float GPIO0B if it is not used, regardless of whether it is set as an input or output.

When GPIO1B is set as an analog input, it sets the converter's operation mode (see the Operation Mode Selection section on page 23 for more details). When GPIO1B is set as a digital output, it operates as a fault indicator that is pulled down if $V_{IN}$ OVP, $V_{OUT}$ OVP, $V_{OUT}$ UVP, OCP, or thermal shutdown is triggered on channel 1. The MFR_GPIO_CTRL register determines which events control GPIO1B. Set GPIO1B as a digital output, and connect GPIO1B to AGND or float GPIO1B if not used.

### Over-Current Protection (OCP)

The MP8886 has cycle-by-cycle OCP. $I_L$ is monitored while the HS-FET is on. Once $I_{L\_PEAK}$ exceeds $I_{LIMIT\_PEAK}$, the HS-FET turns off; the LS-FET turns on to discharge the energy, and $I_L$ decreases. The HS-FET does not turn on again until $I_L$ drops below the valley current limit ($I_{LIMIT\_VALLEY}$). This prevents $I_L$ from rising and damaging the components. $I_{LIMIT\_PEAK}$ and $I_{LIMIT\_VALLEY}$ can be configured via the PMBus.

When $I_L$ exceeds $I_{LIMIT\_VALLEY}$, the OCP timer starts. If the OCP timer reaches 32 consecutive cycles, OCP is triggered. As $I_L$ reaches $I_{LIMIT\_PEAK}$ during each OCP timer cycle, short-circuit protection (SCP) with hiccup mode is triggered.

### Short-Circuit Protection (SCP)

If a short circuit occurs, the MP8886 immediately reaches its current limit ($I_{LIMIT}$) and $V_{OUT}$ drops to its UVP threshold (90% of $V_{OUT}$ by default). The device considers this an output dead short, which immediately triggers SCP. There are three SCP fault response modes that can be selected via the PMBus: hiccup (default), current limit only, and latch-off.

In hiccup mode, the MP8886 disables the output and resets $V_{SS}$, then initiates a new SS. The hiccup time can be configured via the PMBus. If the short remains after SS completes, then the device repeats this operation until the short is removed, and the output returns to its regulation level. Hiccup mode greatly reduces the average short-circuit current by periodically restarting the part to alleviate thermal issues and protect the converter.

In current limit only mode, the MP8886 continues to operate while maintaining $I_{OUT}$ at the value set by MFR_OC_FAULT_LIMIT (E0h).

In latch-off mode, the MP8886 turns off until the power on VIN is cycled or the device is enabled again.

### Over-Voltage Protection (OVP)

The MP8886 monitors $V_{FB}$ to detect output over-voltage (OV) conditions. When $V_{OUT}$ exceeds the OVP threshold, OVP is triggered.

There are three OVP fault response modes that can be selected via the PMBus: discharge (default), ignore, and latch-off. In discharge mode, the LS-FET turns on to discharge the output until the current reaches the negative $I_{LIMIT}$. In ignore mode, the MP8886 takes no action and continues to operate without interruption. In latch-off mode, the MP8886 turns off until the power on VIN is cycled or the device is enabled again.

The MP8886 also has optional $V_{IN}$ OVP. The $V_{IN}$ OVP threshold can be set via the PMBus. If $V_{IN}$ exceeds its OVP threshold, the MP8886 stops switching. $V_{IN}$ OVP is a non-latch protection. The device resumes normal operation once the $V_{IN}$ OV condition is removed.

### Thermal Shutdown

The MP8886 monitors the IC temperature internally to prevent the device from operating at exceedingly high temperatures. If the junction temperature ($T_J$) exceeds the thermal shutdown rising threshold, the device shuts down. Thermal shutdown is a non-latch protection. Once $T_J$ drops below the thermal shutdown falling threshold, the device initiates a new SS to resume normal operation. The thermal shutdown threshold and hysteresis can be set via the PMBus.

### Floating Driver and Bootstrap (BST) Charging

An external bootstrap (BST) capacitor ($C_{BST}$) powers the floating HS-FET driver. The floating driver has its own UVLO protection, with a 2.6V rising threshold and 200mV hysteresis. When the difference between the BST voltage ($V_{BST}$) and SW voltage ($V_{SW}$) ($V_{BST}$ - $V_{SW}$) is below the internal 4.9V BST regulator voltage, a P-channel MOSFET pass transistor (M1 in Figure 5) connected between VIN and BST turns on to charge the $C_{BST}$ while LS-FET is on. If ($V_{BST}$ - $V_{SW}$) exceeds 4.9V, the BST comparator (U1 in Figure 5) regulates M1 to maintain a 4.9V $V_{BST}$ across $C_{BST}$. The external circuit should have enough voltage headroom to accommodate charging.

When ($V_{BST}$ - $V_{SW}$) drops below the UVLO threshold, the HS-FET turns off, and the LS-FET turns on for its minimum on time ($t_{ON\_MIN}$) to conduct and refresh the charge on $C_{BST}$.

At higher duty cycles, the internal charging circuit may not have sufficient voltage and time to charge $C_{BST}$. Add external circuitry to ensure that $V_{BST}$ is within its normal operating range. Figure 5 shows the internal BST charging circuit.

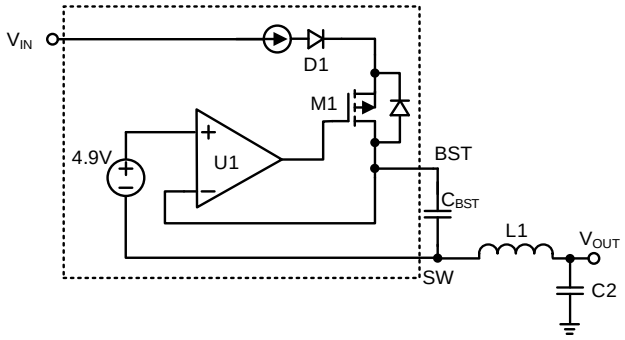



**Figure 5: Internal BST Charging Circuit**

### Low-Dropout Mode

To improve dropout, the MP8886 is designed to operate at close to 100% duty cycle when ($V_{BST}$ - $V_{SW}$) exceeds the UVLO threshold.

If $V_{IN}$ drops, the HS-FET remains on and operates at close to 100% duty cycle to maintain output regulation until ($V_{BST}$ - $V_{SW}$) drops below the UVLO threshold. Since the supply current sourced from $C_{BST}$ is low, the BST charge does not refresh often, and the HS-FET remains on for more switching cycles. This keeps the switching regulator's effective duty cycle high. The effective maximum duty cycle for a single channel is 98% on the evaluation board.

The effective duty cycle during low dropout is primarily determined by the voltage drop across the power MOSFET, inductor resistance, and PCB resistance.

### Operation with a Single Device

There are three operation options for applications with a single device: dual-output operation; 2-phase, single-output operation; and single-phase, 6A operation. See the Operation Mode Selection section on page 23 for more details.

Figure 6 on page 22 shows dual-output operation. With dual-output operation, channel 0 and channel 2 are independent, and their outputs can be set independently.

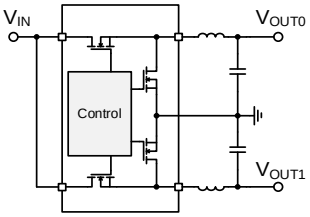



**Figure 6: Single Device with Dual Outputs**

Figure 7 shows dual-phase, single-output operation. In this scenario, channel 0 and channel 1 are paralleled and can achieve up to 6A of $I_{OUT}$. Channel 0 and channel 1 are automatically interleaved with a 180° phase shift to reduce $V_{OUT}$ ripple.

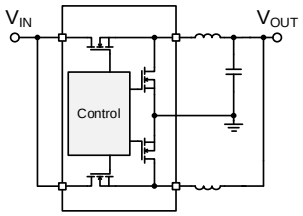



**Figure 7: Single Device with Two Phases and a Single Output**

Figure 8 shows single-phase, 6A operation. In this scenario, channel 0 and channel 1's switching nodes are connected together externally. The two channels work in parallel with one inductor to achieve 6A of $I_{OUT}$.

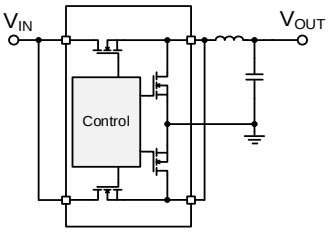



**Figure 8: Single Device with Dual Outputs**

Figure 17 and Figure 18 on page 54, and Figure 19 on page 55 show the typical application circuits for different output and phase operations.

### Operation with Multiple Devices

Multiple MP8886s can operate in parallel for applications with a higher $I_{OUT}$. When multiple ICs are paralleled, one IC is set as the master device, while the others are set as slave devices. See the Operation Mode Selection section on page 23 for more details. Up to two ICs (four phases) can be paralleled, with an automatically interleaved 90° phase shift. If there is more than one slave device, the slave devices all have the same phase shift.

In applications with more than one IC, connect the COMP0 pins of all the ICs together. Connect all of the SYNC pins together as well. For the master chip, the SYNC pin should be set as SYNC out. For the slave devices, the SYNC pin should be set as SYNC in. The SYNC pin does not need to be pulled up externally. If using the internal feedback divider, float the VFBx pin or connect VFBx to AGND. If using the external feedback divider, all of the VFBx pins should be connected together and configured by one feedback divider. All devices should be set to the same frequency via MFR_FREQUENCY_SWITCH (D4h).

Figure 9 shows two paralleled ICs operating with an internal feedback divider.

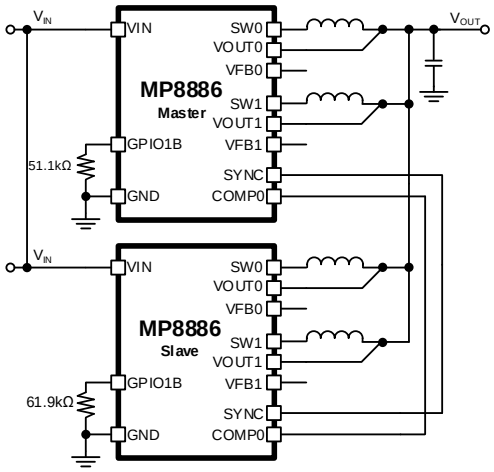



**Figure 9: Two Paralleled Devices with GPIO1B Configuration and an Internal Feedback Divider**

Figure 10 shows the two paralleled devices with an external feedback divider.

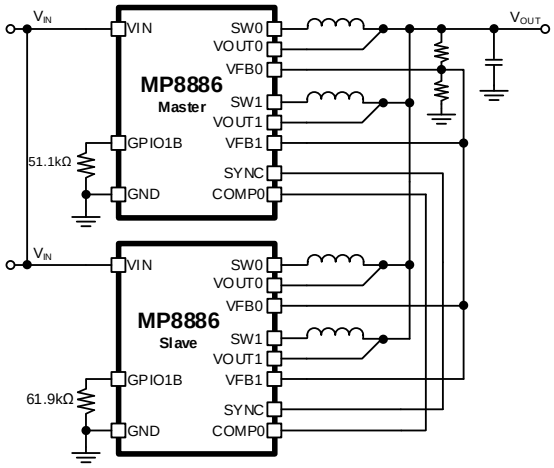



**Figure 10: Two Paralleled Devices with GPIO1B Configuration and an External Feedback Divider**

### Operation Mode Selection

The MP8886 has different operation modes for applications with single and multiple devices. The operation mode can be selected via the multiple-time programmable (MTP) memory or GPIO1B.

When MFR_PWR_STAGE_SET (EAh), bit[3] is set to 0, the operation mode is set by GPIO1B during start-up. Connect GPIO1B to VCC or AGND via a resistor to set the operation mode. GPIO1B should be set as an analog input in MFR_GPIO_MODE for this purpose. Table 1 shows the GPIO1B configurations for the different operation modes.

**Table 1: GPIO1B Configurations for Different Operation Modes**

| R1 (1%) | R2 (1%) | Application | Mode |
|---|---|---|---|
| 10kΩ | NS | Single IC | Dual output |
| NS | 10kΩ | | Single-phase, 6A output |
| NS | 30.1kΩ | | Dual-phase, single output |
| NS | 51.1kΩ | Multiple ICs | Master |
| NS | 61.9kΩ | | Slave |

Figure 11 shows the operation mode selection via GPIO1B.

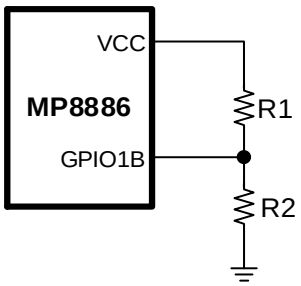



**Figure 11: Operation Mode Selection via GPIO1B**

When MFR_PWR_STAGE_SET (EAh), bit[3] is set to 1, the operation mode is set via the MTP. See the MFR_PWR_STAGE_SET (EAh) section on page 46 for more details.

### PMBus Control and Default Output Voltage

Once the MP8886 is enabled, $V_{IN}$ exceeds its UVLO threshold, EN is pulled high, and OPERATION (01h), bit[7] is set to 1, the device starts up with the default $V_{OUT}$. $V_{OUT}$ is determined by the PMBus once the PMBus receives a valid $V_{OUT}$.

$V_{OUT}$ is set by adjusting the internal $V_{REF}$ and output feedback divider ratio. See the VOUT_COMMAND (21h) section on page 29h and the MFR_VOUT_CTRL (D2h) section on page 37 for more details.

### Cyclical Redundancy Check (CRC) Protection

The MTP's integrity is checked after a power cycle is reset. Each time the MTP contents are read, the MP8886 initiates a cyclic redundancy check (CRC). If a CRC error occurs, the registers attempt to read the contents again. If the error occurs again, the CML bits of the STATUS_BYTE and STATUS_WORD commands are set, and the ALERTB pin is pulled low.

# PMBUS INTERFACE

## PMBus Serial Interface

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled up to a bus voltage ($V_{BUS}$) externally while they are idle. While the lines are connected, a master device generates the SCL signal and device address, and arranges the communication sequence. The MP8886 is a PMBus slave device that supports two fast modes: 400kHz and 1000kHz. The PMBus interface adds flexibility to the power supply solution.

## Slave Address

Set a unique address for each slave device that is connected to the same PMBus. The ADDR pin configures the lower 3 bits of the PMBus address. Table 2 shows the different ADDR resistor ($R_{ADDR}$) values for the lower 3 bits. If the ADDR pin is floating, the address for the lower 3 bits is 111.

**Table 2: PMBus Lower 3 Bits Address**

| $R_{ADDR}$ (kΩ) (1%) | Lower 3 Bits of the Slave Address |
|---|---|
| 0 | 000 |
| 30.9 | 001 |
| 51.1 | 010 |
| 68.1 | 011 |
| 86.6 | 100 |
| 105 | 101 |
| 124 | 110 |
| 210 | 111 |

The higher 4 bits of the PMBus address are set via the MFR_ADDRESS (0xD0) register. These bits range between 0000 and 1111. By default, the higher 4 bits are 0000. In addition, MFR_RAIL_ADDRESS (E8h) can set the PMBus address digitally.

## Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and end of the PMBus transfer. A start command (S) is defined as the SDA signal transitioning from high to low while SCL is high. The stop command (P) is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 12 on page 25).

The master then generates the SCL clocks and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge (ACK) bit.

## PMBus Update Sequence

The MP8886 requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MP8886. The device performs an update on the falling edge of the LSB byte.

## PMBus Message Format

Figure 13 on page 25 shows the PMBus message format. The white cells indicate that the bus host is actively driving the bus. The gray cells indicate that the MP8886 is driving the bus. Additional components are defined below:

- S = Start command
- Sr = Repeated start command
- P = Stop command
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

“A” represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is active high (logic 1), indicated by $\overline{A}$.

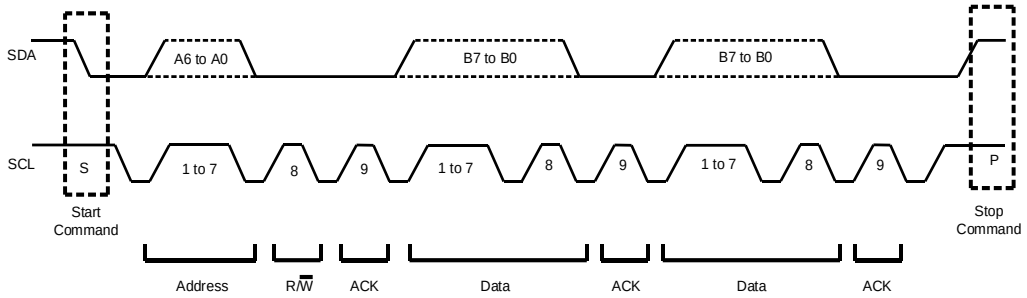



**Figure 12: Data Transfer across the PMBus**

**a) Send Byte**

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | P |

**b) Receive Byte**

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | Slave Address | Rd | A | Command Code | A | P |

**c) Write Byte**

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Data Byte | A | P |

**d) Write Word**

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Data Byte Low | A | Data Byte High | A | P |

**e) Read Byte**

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte | $\overline{A}$ | P |

**f) Read Word**

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte Low | A |

| 8 | 1 | 1 |
|---|---|---|
| Data Byte High | $\overline{A}$ | P |

**Figure 13: PMBus Message Format**

## SUPPORTED PMBUS COMMANDS

| Command Code | Command Name | Type | Bytes | Page 0 (Channel 0) | Page 1 (Channel 1) |
|---|---|---|---|---|---|
| 00h | PAGE | R/W | 1 | ✓ | ✓ |
| 01h | OPEARTION | R/W | 1 | ✓ | ✓ |
| 03h | CLEAR_FAULTS | Send | 0 | ✓ | ✓ |
| 10h | WRITE_PROTECT | R/W | 1 | ✓ | ✓ |
| 15h | STORE_USER_ALL | Send | 0 | ✓ | ✓ |
| 16h | RESTORE_USER_ALL | Send | 0 | ✓ | ✓ |
| 21h | VOUT_COMMAND | R/W | 2 | ✓ | ✓ |
| 24h | VOUT_MAX | R/W | 2 | ✓ | ✓ |
| 25h | VOUT_MARGIN_HIGH | R/W | 2 | ✓ | ✓ |
| 26h | VOUT_MARGIN_LOW | R/W | 2 | ✓ | ✓ |
| 35h | VIN_ON | R/W | 2 | ✓ | ✓ |
| 36h | VIN_OFF | R/W | 2 | ✓ | ✓ |
| 55h | VIN_OV_FAULT_LIMIT | R/W | 2 | ✓ | ✓ |
| 60h | TON_DELAY | R/W | 2 | ✓ | ✓ |
| 61h | TON_RISE | R/W | 2 | ✓ | ✓ |
| 64h | TOFF_DELAY | R/W | 2 | ✓ | ✓ |
| 65h | TOFF_FALL | R/W | 2 | ✓ | ✓ |
| 78h | STATUS_BYTE | R | 1 | ✓ | ✓ |
| 79h | STATUS_WORD | R | 2 | ✓ | ✓ |
| 7Ah | STATUS_VOUT | R | 1 | ✓ | ✓ |
| 7Bh | STATUS_IOUT | R | 1 | ✓ | ✓ |
| 7Ch | STATUS_INPUT | R | 1 | ✓ | ✓ |
| 7Eh | STATUS_CML | R | 1 | ✓ | ✓ |
| 88h | READ_VIN | R | 2 | ✓ | ✓ |
| 89h | READ_IIN | R | 2 | ✓ | ✓ |
| 8Bh | READ_VOUT | R | 2 | ✓ | ✓ |
| 8Ch | READ_IOUT | R | 2 | ✓ | ✓ |
| 8Dh | READ_TEMPERATURE | R | 2 | ✓ | ✓ |
| D0h | MFR_ADDRESS | R/W | 1 | ✓ | - |
| D1h | MFR_DITHER_CTRL | R/W | 1 | ✓ | - |
| D2h | MFR_VOUT_CTRL | R/W | 1 | ✓ | ✓ |
| D3h | MFR_VOUT_TRAN_RATE | R/W | 1 | ✓ | ✓ |
| D4h | MFR_FREQ_SWITCH | R/W | 1 | ✓ | - |
| D5h | MFR_PHASE_CTRL | R/W | 1 | ✓ | - |
| D6h | MFR_COMP1_CTRL | R/W | 1 | ✓ | ✓ |
| D7h | MFR_COMP2_CTRL | R/W | 1 | ✓ | ✓ |
| D8h | MFR_SLOPE_CTRL | R/W | 1 | ✓ | ✓ |
| D9h | MFR_HYS_CTRL | R/W | 1 | ✓ | ✓ |
| DAh | MFR_PWM_CTRL | R/W | 1 | ✓ | ✓ |
| DBh | MFR_GPIO_CTRL | R/W | 1 | ✓ | ✓ |
| DCh | MFR_GPIO_MODE | R/W | 1 | ✓ | ✓ |
| DDh | MFR_PRODUCT_ID | R/W | 1 | ✓ | - |
| DEh | MFR_PRODUCT_VERSION | R/W | 1 | ✓ | - |
| E0h | MFR_OC_FAULT_LIMIT | R/W | 1 | ✓ | ✓ |
| E1h | MFR_OC_RESPONSE | R/W | 1 | ✓ | ✓ |
| E2h | MFR_VIN_OV_FAULT_RESPONSE | R/W | 1 | ✓ | ✓ |
| E3h | MFR_VOUT_OV_ FAULT_LIMIT | R/W | 1 | ✓ | ✓ |
| E4h | MFR_VOUT_OV_AULT_RESPONSE | R/W | 1 | ✓ | ✓ |

## SUPPORTED PMBUS COMMANDS *(continued)*

| Command Code | Command Name | Type | Bytes | Page 0 (Channel 0) | Page 1 (Channel 1) |
|---|---|---|---|---|---|
| E5h | MFR_VOUT_UV_ FAULT_LIMIT | R/W | 1 | ✓ | ✓ |
| E6h | MFR_VOUT_UV_AULT_RESPONSE | R/W | 1 | ✓ | ✓ |
| E7h | MFR_OT_FAULT_LIMIT | R/W | 1 | ✓ | - |
| E8h | MFR_RAIL_ADDRESS | R/W | 1 | ✓ | - |
| E9h | MFR_LIGHT_CTRL | R/W | 1 | ✓ | ✓ |
| EAh | MFR_PWR_STAGE_SET | R/W | 1 | ✓ | - |

# REGISTER MAP (10)

## PAGE (00h)

**Format:** Unsigned binary

The PAGE command determines whether the PMBus command operates on channel 0 or channel 1. When bit[0] = 0, channel 0 is selected, and the PMBus command operates on channel 0. When bit[0] = 1, channel 1 is selected, and the PMBus command operates on channel 1. For more details on which PMBus command can support channel 0 or channel 1, see the Supported PMBus Commands section starting on page 26.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:1 | R | RESERVED | 7’b 0000000 | Reserved. |
| 0 | R/W | PAGE | 1’b0 | Selects whether the PMBus command operates on channel 0 or channel 1.<br>0: Chanel 0 is selected for the PMBus command<br>1: Chanel 1 is selected for the PMBus command |

## OPEARTION (01h)

**Format:** Unsigned binary

The OPERATION command controls some behaviors. Bit[7] controls when the DC/DC converter turns on and off. This means that the MP8886’s output can be turned on and off under host control via the PMBus. Bit[6] controls the shutdown behavior. If the PMBus device output is on (bit[7] = 1), then bits[5:4] control the basic source of the $V_{OUT}$ command.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R/W | OPERATION | 4’b1000 | Selects the operation mode.<br>4’b00xx: The converter turns off immediately without a configurable delay or fall time ($t_{FALL}$)<br>4’b01xx: The converter initiates a soft shutdown with a configurable delay (set by TOFF_DELAY) and $t_{FALL}$ (set by TOFF_FALL)<br>4’b1000: The converter is on with a normal output (set by VOUT_COMMAND)<br>4’b 1001: The converter is on with a low output (set by VOUT_MARGIN_LOW)<br>4b’1010: The converter is on with a high output (set by VOUT_MARGIN_HIGH)<br>“x” means not applicable. |
| 3:0 | R | RESERVED | 4’b0000 | Reserved. |

## CLEAR_FAULTS (03h)

**Format:** Unsigned binary

The CLEAR_FAULTS command clears any fault bits that have been set. This command clears all bits in all status registers simultaneously. If a fault is still present once the bit is cleared, the fault bit is set again immediately. This command is write-only. There is no data byte for this command. Faults on channel 0 and channel 1 should be cleared separately.

**Note:**

10) All default values are based on the default configuration code (MP8886GUT-0000).

### WRITE_PROTECT (10h)

**Format:** Unsigned binary

The WRITE_PROTECT command controls writing to the MP8886. This command provides protection against accidental writes. This write protection controls all registers, including channel 0 and channel 1.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R/W | WRITE_PROTECT | 4’b0000 | Selects the write protection settings.<br>4’b1000: All writes are disabled except writes to the WRITE_PROTECT command<br>4’b0100: All writes are disabled except writes to the WRITE_PROTECT, OPERATION, and PAGE commands<br>4’b0010: All writes are disabled except writes to the WRITE_PROTECT, OPERATION, PAGE, and VOUT_COMMAND commands<br>4’b0000: Enables all writes to all commands |
| 3:0 | R | RESERVED | 4’b0000 | Reserved. |

### STORE_USER_ALL (15h)

**Format:** Unsigned binary

The STORE_USER_ALL command saves the register values to the MTP. STORE_USER_ALL instructs the PMBus device to copy the entire contents of the operating memory to the corresponding locations in the MTP (the non-volatile user store memory). Any items in the operating memory that do not have corresponding locations in the MTP are ignored.

The MP8886 automatically turns EN off, then writes all of the data from the converter’s memory map to the internal MTP. After the device has completed writing to the MTP, it restarts with the new configuration data from the MTP. This process starts once the MP8886 receives a STORE_USER_ALL command from the PMBus interface.

The MTP can be configured an unlimited number of times. To configure the MTP successfully, $V_{IN}$ must exceed 7V.

This command has no data bytes. This command is write-only.

### RESTORE_USER_ALL (16h)

**Format:** Unsigned binary

The RESTORE_USER_ALL command loads the MTP values to the registers. RESTORE_USER_ALL instructs the PMBus device to copy the entire contents of the user store (MTP) to the matching locations in the operating memory (PMBus register). The values in the operating memory are overwritten by the value retrieved from the user store. Any items in the user store that do not have corresponding locations in the operating memory are ignored.

RESTORE_USER_ALL can be used even when the device is not configured for the MTP. While restoring the MTP data to the user memory, the device executes a CRC calculation and compares the calculation with the stored CRC check result in the MTP cell. The MTP value is restored to the operating memory once these values match.

The output turns off first during this operation. After MTP configuration is complete, the output turns on again with the new configuration data from the MTP.

This command has no data bytes. This command is write-only.

### VOUT_COMMAND (21h)

**Format:** Direct

The VOUT_COMMAND command sets $V_{REF}$, which can be used to calculate $V_{OUT}$.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:10 | R/W | RESERVED | 6'b000000 | Reserved. |
| 9:0 | R/W | VOUT_COMMAND | 10'b1000100110 | Sets $V_{REF}$. |

$V_{OUT}$ is determined by $V_{REF}$ and the feedback divider ratio. $V_{OUT}$ can be estimated with Equation (1):

$$V_{OUT}\ (V) = 0.0015 \times (X / \text{Feedback Divider Ratio}) \quad (1)$$

Where *X* is the 10-bit, unsigned binary integer of VOUT_COMMAND, bits[9:0] (1.5mV per LSB).

There is an external feedback divider ratio (see Figure 15 on page 51). The internal feedback divider ratio is selected via MFR_VOUT_CTRL, while the external divider ratio can be calculated with Equation (2):

$$\text{External Feedback Divider Ratio} = R2 / (R1 + R2) \quad (2)$$

In external feedback divider mode, the external resistor divider sets $V_{OUT}$. When using an external feedback divider, the internal feedback divider ratio should be set to 1:16. In internal feedback divider mode, the internal feedback divider ratio is selected by MFR_VOUT_CTRL (D2h) (see Table 3).

**Table 3: Internal Feedback Divider Ratio**

| MFR_VOUT_CTRL, Bits[2:0] | Internal Feedback Divider Ratio | $V_{OUT}$ Range |
|---|---|---|
| 000 | 1:1 | 0.6V to 1.5345V |
| 001 | 1:2 | 0.6V to 3.069V |
| 010 | 1:4 | 0.6V to 6.138V |
| 011 | 1:8 | 1.2V to 12.276V |
| 100 | 1:16 | 2.4V to 24.552V |

### VOUT_MAX (24h)

**Format:** Direct

The VOUT_MAX command sets the $V_{REF}$ upper threshold, which limits $V_{OUT}$. This command limits $V_{OUT}$, which prevents a user from unintentionally setting $V_{OUT}$ too high.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:10 | R/W | RESERVED | 6'b000000 | Reserved. |
| 9:0 | R/W | VOUT_MAX | 10'b1111111111 | Sets the maximum $V_{REF}$. |

The maximum $V_{OUT}$ ($V_{OUT\_MAX}$) limit is determined by the maximum $V_{REF}$ and feedback divider ratio. $V_{OUT\_MAX}$ can be estimated with Equation (2):

$$V_{OUT\_MAX}\ (V) = 0.0015 \times (X / \text{Feedback Divider Ratio}) \quad (2)$$

Where *X* is the 10-bit, unsigned binary integer of VOUT_MAX, bits[9:0] (1.5mV per LSB).

There is an external feedback divider ratio (see Figure 15 on page 51). The internal feedback divider ratio is selected via MFR_VOUT_CTRL, while the external divider ratio can be calculated with Equation (2).

### VOUT_MARGIN_HIGH (25h)

**Format:** Direct

The VOUT_MARGIN_HIGH command stores $V_{REF}$ in response to the margin high action in OPERATION (01h).

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:10 | R/W | RESERVED | 6'b000000 | Reserved. |
| 9:0 | R/W | VOUT_MARGIN_HIGH | 10'b1001010010 | Sets the margin high $V_{REF}$. |

The margin high $V_{OUT}$ ($V_{OUT\_MARGIN\_HIGH}$) is determined by the margin high $V_{REF}$ and the feedback divider ratio. $V_{OUT\_MARGIN\_HIGH}$ can be calculated with Equation (3):

$$V_{OUT\_MARGIN\_HIGH}\ (V) = 0.0015 \times (X / \text{Feedback Divider Ratio}) \quad (3)$$

Where *X* is the 10-bit, unsigned binary integer of VOUT_MARGIN_HIGH, bits[9:0] (1.5mV per LSB).

There is an external feedback divider ratio (see Figure 15 on page 51). The internal feedback divider ratio is selected via MFR_VOUT_CTRL, while the external divider ratio can be calculated with Equation (2) on page 30.

### VOUT_MARGIN_LOW (26h)

**Format:** Direct

The VOUT_MARGIN_LOW command stores $V_{REF}$ in response to the margin low action in OPERATION (01h).

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:10 | R/W | RESERVED | 6'b000000 | Reserved. |
| 9:0 | R/W | VOUT_MARGIN_LOW | 10'b0111111010 | Sets the margin low $V_{REF}$. |

The margin low $V_{OUT}$ ($V_{OUT\_MARGIN\_LOW}$) is determined by the margin low $V_{REF}$ and the feedback divider ratio. $V_{OUT\_MARGIN\_LOW}$ can be estimated with Equation (4):

$$V_{OUT\_MARGIN\_LOW}\ (V) = 0.0015 \times (X / \text{Feedback Divider Ratio}) \quad (4)$$

Where *X* is the 10-bit, unsigned binary integer of VOUT_MARGIN_LOW, bits[9:0] (1.5mV per LSB).

There is an external feedback divider ratio (see Figure 15 on page 51). The internal feedback divider ratio is selected via MFR_VOUT_CTRL, while the external divider ratio can be calculated with Equation (2) on page 30.

### VIN_ON (35h)

**Format:** Direct

The VIN_ON command sets the $V_{IN}$ UVLO rising threshold via the PMBus. Channel 0's VIN_ON has a higher priority than channel 1's VIN_ON. If $V_{IN}$ is below channel 0's VIN_ON, both channel 0 and channel 1 do not turn on.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:9 | R/W | RESERVED | 7'b0000000 | Reserved. |
| 8:0 | R/W | VIN_ON | 9'b000100100 | Sets the $V_{IN}$ UVLO rising threshold. 108mV/LSB. |

If the VIN_ON value is below the value set by register 1Dh, the $V_{IN}$ UVLO rising threshold is 3.1V. If the VIN_ON value exceeds the value set by register 1Dh, the $V_{IN}$ UVLO rising threshold is set by VIN_ON.

### VIN_OFF (36h)

**Format:** Direct

The VIN_OFF command sets the $V_{IN}$ UVLO falling threshold via the PMBus. Channel 0's VIN_OFF has a higher priority than channel 1's VIN_OFF. If $V_{IN}$ is below channel 0's VIN_OFF, both channel 0 and channel 1 turn off.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:9 | R/W | RESERVED | 7'b0000000 | Reserved. |
| 8:0 | R/W | VIN_OFF | 9'b000100010 | Sets the $V_{IN}$ UVLO falling threshold. 108mV/LSB. |

If the VIN_OFF value is below the value set by register 1Bh, the $V_{IN}$ UVLO falling threshold is 2.9V. If the VIN_OFF value exceeds the value set by register 1Bh, the $V_{IN}$ UVLO falling threshold is set by VIN_OFF.

### VIN_OV_FAULT_LIMIT (55h)

**Format:** Direct

The VIN_OV_FAULT_LIMIT command sets the $V_{IN}$ OVP rising threshold.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:9 | R/W | RESERVED | 7'b0000000 | Reserved. |
| 8:0 | R/W | VIN_OV_FAULT_LIMIT | 9'b111010110 | Sets the $V_{IN}$ OVP rising threshold. 108mV/LSB. |

### TON_DELAY (60h)

**Format:** Direct

The TON_DELAY command sets the delay time from when EN turns on to when $V_{OUT}$ starts rising. TON_DELAY is valid when the EN pin is on and the PMBus commands the device on.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:7 | R/W | RESERVED | 9'b000000000 | Reserved. |
| 6:0 | R/W | TON_DELAY | 7'b0000000 | Sets the output EN delay time. 1ms/LSB. |

### TON_RISE (61h)

Format: Direct

The TON_RISE command sets the period when $V_{OUT}$ rises from 10% to 90% of its target voltage (i.e. the output rise time).

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:5 | R/W | RESERVED | 11'b00000000000 | Reserved. |
| 4:0 | R/W | TON_RISE | 5'b00001 | Sets the output rise time. 1ms/LSB. |

### TOFF_DELAY (64h)

**Format:** Direct

The TOFF_DELAY command sets the delay time from when EN turns off to when $V_{OUT}$ starts falling. TOFF_DELAY is valid when the PMBus receives an off command. When the EN pin turns off, the output drops immediately.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:7 | R/W | RESERVED | 9'b000000000 | Reserved. |
| 6:0 | R/W | TOFF_DELAY | 7'b0000000 | Sets the output disable delay. 1ms/LSB. |

### TOFF_FALL (65h)

**Format:** Direct

The TOFF_FALL command sets the period when $V_{OUT}$ drops from 90% to 10% of its target voltage (i.e. the output fall time).

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:5 | R/W | RESERVED | 11'b00000000000 | Reserved. |
| 4:0 | R/W | TOFF_FALL | 5'b00001 | Sets the output fall time. 1ms/LSB. |

### STATUS_BYTE (78h)

**Format:** Unsigned binary

The STATUS_BYTE command indicates the MP8886's state. Once a fault is removed, the bit is cleared. To clear the latched fault bits, issue a CLEAR_FAULTS command.

| Bits | Access | Bit Name | Behavior | Default | Description |
|---|---|---|---|---|---|
| 7 | R | BUSY | Live | 1'b0 | Indicates whether a fault has occurred when the device is busy and unable to respond. |
| 6 | R | OFF | Live | 1'b0 | This bit asserts if the device is not providing power to the output, regardless of the reason (even if the device is not enabled). |
| 5 | R | VOUT_OV_FAULT | Latch | 1'b0 | Indicates whether an output over-voltage (OV) fault has occurred. |
| 4 | R | IOUT_OC_FAULT | Latch | 1'b0 | Indicates whether an output over-current (OC) fault has occurred. |
| 3 | R | VIN_UV_FAULT | Latch | 1'b0 | Indicates whether an input under-voltage (UV) fault has occurred. |
| 2 | R | TEMPERATURE | Latch | 1'b0 | Indicates whether a temperature fault or warning has occurred. |
| 1 | R | CML | Latch | 1'b0 | Indicates whether a communications, memory, or logic fault has occurred. |
| 0 | R | RESERVED | N/A | 1'b0 | Reserved. |

### STATUS_WORD (79h)

**Format:** Unsigned binary

The STATUS_WORD indicates the MP8886's state. Once a fault is removed, the bit is cleared. To clear the latched fault bits, issue a CLEAR_FAULTS (03h) command.

| Bits | Access | Bit Name | Behavior | Default | Description |
|---|---|---|---|---|---|
| 15 | R | VOUT | Latch | 1'b0 | Indicates whether a $V_{OUT}$ fault or warning has occurred. |
| 14 | R | IOUT/POUT | Latch | 1'b0 | Indicates whether an $I_{OUT}$ or output power ($P_{OUT}$) fault or warning has occurred. |
| 13 | R | INPUT | Latch | 1'b0 | Indicates whether a $V_{IN}$, input current ($I_{IN}$), or input power ($P_{IN}$) fault or warning has occurred. |
| 12 | R | RESERVED | N/A | 1'b0 | Reserved. |
| 11 | R | PG_STATUS | Live | 1'b0 | Returns the POWER_GOOD signal. If this bit is set to 0, an output is present. |
| 10:8 | R | RESERVED | N/A | 3'b000 | Reserved. |
| 7 | R | BUSY | Live | 1'b0 | Indicates whether a fault has been declared while the device was busy and unable to respond. |

| | | | | | |
|---|---|---|---|---|---|
| 6 | R | OFF | Live | 1’b0 | This bit asserts if the device is not providing power to the output, regardless of the reason (even if the device is not enabled). |
| 5 | R | VOUT_OV_FAULT | Latch | 1’b0 | Indicates whether an output over-voltage (OV) fault has occurred. |
| 4 | R | IOUT_OC_FAULT | Latch | 1’b0 | Indicates whether an output over-current (OC) fault has occurred. |
| 3 | R | VIN_UV_FAULT | Latch | 1’b0 | Indicates whether an input under-voltage (UV) fault has occurred. |
| 2 | R | TEMPERATURE | Latch | 1’b0 | Indicates whether a temperature fault or warning has occurred. |
| 1 | R | CML | Latch | 1’b0 | Indicates whether a communications, memory, or logic fault has occurred. |
| 0 | R | RESERVED | N/A | 1’b0 | Reserved. |

### STATUS_VOUT (7Ah)

**Format:** Unsigned binary

The STATUS_VOUT command indicates the device’s $V_{OUT}$ status. To clear the bits in this register, issue a CLEAR_FAULTS (03h) command.

| Bits | Access | Bit Name | Behavior | Default | Description |
|---|---|---|---|---|---|
| 7 | R | VOUT_OV_FAULT | Live | 1’b0 | Indicates whether an output over-voltage (OV) fault has occurred. |
| 6:5 | R | RESERVED | Live | 2’b00 | Reserved. |
| 4 | R | VOUT_UV_FAULT | Latch | 1’b0 | Indicates whether an output under-voltage (UV) fault has occurred. |
| 3:0 | R | RESERVED | Latch | 4’b0000 | Reserved. |

### STATUS_INPUT (7Ch)

**Format:** Unsigned binary

The STATUS_INPUT command indicates the device’s $V_{IN}$ status. To clear the bits in this register, issue a CLEAR_FAULTS (03h) command.

| Bits | Access | Bit Name | Behavior | Default | Description |
|---|---|---|---|---|---|
| 7 | R | VOUT_OV_FAULT | Live | 1’b0 | Indicates whether an input over-voltage (OV) fault has occurred. |
| 6:5 | R | RESERVED | Live | 2’b00 | Reserved. |
| 4 | R | VOUT_UV_FAULT | Latch | 1’b0 | Indicates whether an input under-voltage (UV) fault has occurred. |
| 3:0 | R | RESERVED | Latch | 4’b0000 | Reserved. |

### STATUS_CML (7Eh)

**Format:** Unsigned binary

The STATUS_CML command indicates the device’s PMBus command status. To clear the bits in this register, issue a CLEAR_FAULTS (03h) command.

| Bits | Access | Bit Name | Behavior | Default | Description |
|---|---|---|---|---|---|
| 7 | R | INVALID_ COMMAND | Latch | 1’b0 | Indicates whether an invalid command has been received by the PMBus. |

| | | | | | |
|---|---|---|---|---|---|
| 6 | R | INVALID_DATA | Latch | 1’b0 | Indicates whether an invalid data has been received by the PMBus. |
| 5 | R | PEC_FAIL | Latch | 1’b0 | Indicates whether a PMBus package error check (PEC) has failed. |
| 4 | R | MEMORY_FAULT | Latch | 1’b0 | Indicates whether a memory fault has been detected (e.g. the memory’s CRC does not match the initial CRC value). |
| 3:2 | R | RESERVED | N/A | 2’b00 | Reserved. |
| 1 | R | COMMUNICATION_ FAULT | Latch | 1’b0 | Indicates whether a communication fault (other than the faults listed in this table) has occurred. |
| 0 | R | RESERVED | N/A | 1’b0 | Reserved. |

**READ_VIN (88h)**

**Format:** Direct

The READ_VIN command returns the measured $V_{IN}$.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:9 | R | RESERVED | 7’b0000000 | Reserved. |
| 8:0 | R | READ_VIN | 9’b000000000 | Returns the measured $V_{IN}$. 108mV/LSB. |

$V_{IN}$ can be calculated with Equation (5):

$$V_{IN}\ (V) = 0.108 \times (X) \quad (5)$$

Where *X* is the 9-bit, unsigned binary integer of READ_VIN, bits[8:0] (108mV per LSB).

It is recommended to read this result more than five times, and then take the average value to improve accuracy.

**READ_IIN (89h)**

**Format:** Direct

The READ_IIN command returns the measured $I_{IN}$.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:9 | R | RESERVED | 7’b0000000 | Reserved. |
| 8:0 | R | READ_IIN | 9’b000000000 | Returns the measured $I_{IN}$. 15mA/LSB. |

$I_{IN}$ can be calculated with Equation (6):

$$I_{IN}\ (A) = 0.015 \times (X) \quad (6)$$

Where *X* is the 9-bit, unsigned binary integer of READ_IIN, bits[8:0] (15mA per LSB).

It is recommended to read this result more than five times, and then take the average value to improve accuracy.

**READ_VOUT (8Bh)**

**Format:** Direct

The READ_VOUT command returns the $V_{FB}$.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:9 | R | RESERVED | 7’b0000000 | Reserved. |
| 8:0 | R | READ_VOUT | 9’b000000000 | Returns the measured $V_{FB}$. 3mV/LSB. |

$V_{OUT}$ is determined by $V_{FB}$ and the feedback divider ratio. $V_{OUT}$ can be estimated with Equation (7):

$$V_{OUT}\ (V) = 0.003 \times (X / \text{Feedback Divider Ratio}) \quad (7)$$

Where *X* is the 9-bit, unsigned binary integer of READ_VOUT, bits[8:0] (3mV per LSB).

There is an external feedback divider ratio (see Figure 15 on page 51). The internal feedback divider ratio is selected via MFR_VOUT_CTRL, while the external divider ratio can be calculated with Equation (2) on page 30.

It is recommended to read this result more than five times, and then take the average value to improve accuracy.

### READ_IOUT (8Ch)

**Format:** Direct

The READ_IOUT command returns the measured $I_{OUT}$.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:9 | R | RESERVED | 7'b0000000 | Reserved. |
| 8:0 | R | READ_IOUT | 9'b000000000 | Returns the measured $I_{OUT}$. 15mA/LSB. |

$I_{IN}$ can be calculated with Equation (8):

$$I_{IN}\ (A) = 0.015 \times (X) \quad (8)$$

Where *X* is the 9-bit, unsigned binary integer of READ_IOUT, bits[8:0] (15mA per LSB).

It is recommended to read this result more than five times, and then take the average value to improve accuracy.

### READ_TEMPERATURE (8Dh)

**Format:** Direct

The READ_TEMPERATURE command returns the measured IC junction temperature ($T_J$). This value is also used for over-temperature (OT) warning and fault detection.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 15:10 | R | RESERVED | 6'b000000 | Reserved. |
| 9:0 | R | READ_TEMPERATURE | 10'b0000000000 | Returns the measured $T_J$. 1°C /LSB. |

### MFR_ADDRESS (D0h)

**Format:** Unsigned binary

The MFR_ADDRESS command sets the 4 higher bits of the 7-bit PMBus address.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R/W | RESERVED | 4'b0000 | Reserved. |
| 3:0 | R/W | MFR_ADDRESS | 4'b0000 | Sets the 4 higher bits of the 7-bit PMBus address. The 3 lower bits are set by the ADDR pin (see Table 2 on page 24). |

### MFR_DITHER_CTRL (D1h)

**Format:** Unsigned binary

The MFR_DITHER_CTRL command controls the frequency dithering function. Frequency dithering reduces peak emissions at a specific frequency.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7 | R/W | DITHER_ ENABLE/ DISABLE | 1'b0 | Enables frequency dithering.<br>0: Disabled<br>1: Enabled |
| 6:3 | R/W | DITHER_CYCLE | 4b'0000 | Sets the dither cycle.<br>Bits / Dither Cycle / Bits / Dither Cycle<br>0000 2kHz 1000 18kHz<br>0001 4kHz 1001 20kHz<br>0010 6kHz 1010 22kHz<br>0011 8kHz 1011 24kHz<br>0100 10kHz 1100 26kHz<br>0101 12kHz 1101 28kHz<br>0110 14kHz 1110 30kHz<br>0111 16kHz 1111 32kHz |
| 2:0 | R/W | DITHER_RANGE | 3b'000 | Sets the dither range.<br>Bits / Dither Range / Bits / Dither Range<br>000 $f_{SW}$ + 2kHz to $f_{SW}$ + 9kHz 100 $f_{SW}$ + 18kHz to $f_{SW}$ + 81kHz<br>001 $f_{SW}$ + 6kHz to $f_{SW}$ + 27kHz 101 $f_{SW}$ + 22kHz to $f_{SW}$ + 99kHz<br>010 $f_{SW}$ + 10kHz to $f_{SW}$ + 45kHz 110 $f_{SW}$ + 26kHz to $f_{SW}$ + 117kHz<br>011 $f_{SW}$ + 14kHz to $f_{SW}$ + 63kHz 111 $f_{SW}$ + 30kHz to $f_{SW}$ + 135kHz |

### MFR_VOUT_CTRL (D2h)

Format: Unsigned binary

The MFR_VOUT_CTRL command sets the $V_{OUT}$ feedback behavior. MFR_VOUT_CTRL selects feedback divider mode, the feedback divider ratio, and the VCC bias supply function.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:5 | R/W | RESERVED | 3'b000 | Reserved. |
| 4 | R/W | VOUT_SET_ MODE | 1'b1 | Selects the feedback divider mode.<br>0: External feedback divider mode. When using an external feedback divider, bits[2:0] of this command should be set to 100<br>1: Internal feedback divider mode |
| 3 | R/W | VOBIAS_EN | 1'b1 | Enables the $V_{OUT}$ bias. If enabled, VCC can be supplied via the VOUT pin if $V_{OUT}$ exceeds 4.8V. Channel 0's VOBIAS_EN bit controls the $V_{OUT}$ bias function. Channel 1 does not have this control bit.<br>0: Disabled<br>1: Enabled |
| 2:0 | R/W | FEEDBACK_ DIVIDER_RATIO | 3'b010 | These bits set the feedback divider ratio. Before configuring these bits, disable the DC/DC converter using register 01h.<br>Bits / Divider Ratio / $V_{OUT}$ Range<br>000 1:1 0.6V to 1.5345V<br>001 1:2 0.6V to 3.069V<br>010 1:4 0.6V to 6.138V<br>011 1:8 1.2V to 12.276V<br>100 1:16 2.4V to 24.552V |

### MFR_VOUT_TRANSITION_RATE (D3h)

Format: Unsigned binary

The MFR_VOUT_TRANSITION_RATE command sets the $V_{OUT}$ transition rate while adjusting $V_{OUT}$ via the PMBus.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:3 | R/W | RESERVED | 5'b00000 | Reserved. |
| 2:0 | R/W | OUTPUT_VOLTAGE_ TRANSITION_RATE | 3'b100 | Sets the $V_{OUT}$ transition rate. This selection only works once soft start completes. The rising and falling transition rates are the same. |

| Bits | $V_{OUT}$ Slew Rate |
|---|---|
| 000 | 0.1V/ms |
| 001 | 0.25V/ms |
| 010 | 0.5V/ms |
| 011 | 1V/ms |
| 100 | 2V/ms |

When using the internal feedback divider, the $V_{OUT}$ transition rate is the set by MFR_VOUT_CTRL, bits[2:0], regardless of the feedback ratio. When using an external feedback divider, MFR_VOUT_CTRL, bits[2:0] is set to 100, and the $V_{OUT}$ transition rate ($V_{OUT\_TRANSITION\_RATE}$) can be estimated with Equation (9):

$$V_{OUT\_TRANSITION\_RATE}\ (V) = X / 16 / (\text{Feedback Divider Ratio}) \quad (9)$$

Where *X* is the set value in bits[2:0].

The external divider ratio can be calculated with Equation (2) on page 30.

### MFR_FREQUENCY_SWITCH (D4h)

**Format:** Unsigned binary

The MFR_FREQUENCY_SWITCH command sets channel 0 and channel 1's $f_{SW}$.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:3 | R/W | RESERVED | 5'b00000 | Reserved. |
| 2:0 | R/W | SWITCHING_ FREQUENCY_SET | 3'b011 | Sets $f_{SW}$. |

| Bits | $f_{SW}$ | Bits | $f_{SW}$ |
|---|---|---|---|
| 000 | 150kHz | 100 | 800kHz |
| 001 | 200kHz | 101 | 1000kHz |
| 010 | 400kHz | 110 | 1500kHz |
| 011 | 600kHz | 111 | 2200kHz |

### MFR_PHASE_CTRL (D5h)

**Format:** Unsigned binary

The MFR_PHASE_CTRL command sets the SYNC pin's behavior.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:5 | R/W | RESERVED | 3'b000 | Reserved. |
| 4 | R/W | SYNC_IN_PHASE_ SHIFT | 1'b0 | Sets the phase shift between the external SYNC in signal and the internal oscillator.<br>0: 0°<br>1: 180° |
| 3:1 | R/W | RESERVED | 3'b000 | Reserved. |

| | | | | |
|---|---|---|---|---|
| 0 | R/W | SYNC_IN/OUT | 1’b0 | Determines whether the SYNC pin operates as a SYNC in or SYNC out.<br>0: SYNC out<br>1: SYNC in |

### MFR_COMP1_CTRL (D6h)

**Format:** Unsigned binary

The MFR_COMP1_CTRL command sets the compensation network parameters. See Figure 14 on page 40 for more details regarding the compensation network.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7 | R/W | RESERVED | 1’b0 | Reserved. |
| 6:4 | R/W | CTH | 3’b100 | Sets the configurable CTH that adjusts the compensation capacitor. 10pF/LSB, 20pF offset.<br>Bits / Value / Bits / Value<br>000 / 20pF / 100 / 60pF<br>001 / 30pF / 101 / 70pF<br>010 / 40pF / 110 / 80pF<br>011 / 50pF / 111 / 90pF |
| 3:2 | R/W | RESERVED | 2’b00 | Reserved. |
| 1:0 | R/W | CTHP | 2’b00 | Sets the configurable CTHP that adjusts the high-frequency compensation capacitor.<br>Bits: 00 / 01 / 10 / 11<br>Value: 0.1pF / 0.3pF / 0.6pF / 0.9pF |

### MFR_COMP2_CTRL (D7h)

**Format:** Unsigned binary

The MFR_COMP2_CTRL command sets the compensation network parameters. See Figure 14 on page 40 for more details regarding the compensation network.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R/W | GM | 4’b0010 | Sets the configurable error amplifier (EA) gain.<br>Bits / Value / Bits / Value<br>0000 / 25.0μA/V / 1000 / 5.0μA/V<br>0001 / 16.7μA/V / 1001 / 4.5μA/V<br>0010 / 12.5μA/V / 1010 / 4.2μA/V<br>0011 / 10.0μA/V / 1011 / 3.8μA/V<br>0100 / 8.3μA/V / 1100 / 3.6μA/V<br>0101 / 7.1μA/V / 1101 / 3.3μA/V<br>0110 / 6.3μA/V / 1110 / 3.1μA/V<br>0111 / 5.6μA/V / 1111 / 2.9μA/V |
| 3:0 | R/W | RTH | 4’b1010 | Sets the configurable RTH that adjusts the compensation resistor. 80kΩ/LSB, 200kΩ offset.<br>Bits / Value / Bits / Value<br>0000 / 200kΩ / 1000 / 840kΩ<br>0001 / 280kΩ / 1001 / 920kΩ<br>0010 / 360kΩ / 1010 / 1000kΩ<br>0011 / 440kΩ / 1011 / 1080kΩ<br>0100 / 520kΩ / 1100 / 1160kΩ<br>0101 / 600kΩ / 1101 / 1240kΩ<br>0110 / 680kΩ / 1110 / 1320kΩ<br>0111 / 760kΩ / 1111 / 1400kΩ |

### MFR_SLOPE_CTRL (D8h)

**Format:** Unsigned binary

The MFR_COMP_CTRL command sets the slope compensation.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R/W | RESERVED | 4’b0000 | Reserved. |
| 3:0 | R/W | SLOP_COMP | 4’b0000 | Sets the configurable slop compensation rate. |

| Bits | Value | Bits | Value |
|---|---|---|---|
| 0000 | 1.83 x $f_{SW}$ x 1e-6 | 1000 | 1.83 x $f_{SW}$ x 1e-6 |
| 0001 | 1.65 x $f_{SW}$ x 1e-6 | 1001 | 2 x $f_{SW}$ x 1e-6 |
| 0010 | 1.5 x $f_{SW}$ x 1e-6 | 1010 | 2.3 x $f_{SW}$ x 1e-6 |
| 0011 | 1.375 x $f_{SW}$ x 1e-6 | 1011 | 2.75 x $f_{SW}$ x 1e-6 |
| 0100 | 1.27 x $f_{SW}$ x 1e-6 | 1100 | 3.3 x $f_{SW}$ x 1e-6 |
| 0101 | 1.2 x $f_{SW}$ x 1e-6 | 1101 | 4.125 x $f_{SW}$ x 1e-6 |
| 0110 | 1.1 x $f_{SW}$ x 1e-6 | 1110 | 5.5 x $f_{SW}$ x 1e-6 |
| 0111 | $f_{SW}$ x 1e-6 | 1111 | 8.25 x $f_{SW}$ x 1e-6 |

Figure 14 shows the compensation network.

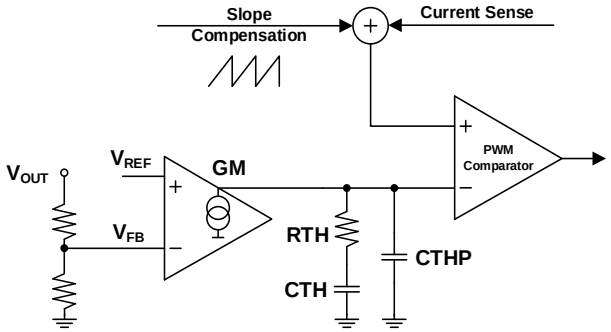



**Figure 14: Compensation Network**

### FR_HYS_CTRL (D9h)

**Format:** Unsigned binary

The MFR_HYS_CTRL command sets the hysteresis values.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:5 | R/W | RESERVED | 3’b000 | Reserved. |
| 4 | R/W | OVER_ TEMPERATURE_ HYSTERESIS | 1’b0 | Sets the thermal shutdown hysteresis.<br>0: 25°C<br>1: 50°C |
| 3 | R/W | VIN_OVER_ VOLTAGE_ HYSTERESIS | 1’b0 | Sets the $V_{IN}$ over-voltage protection (OVP) hysteresis.<br>0: 1.2V<br>1: 2.2V |
| 2 | R/W | RESERVED | 1’b0 | Reserved. |
| 1 | R/W | VOUT_OV_ HYSTERESIS | 1’b0 | Sets the $V_{OUT}$ OVP hysteresis.<br>0: 5% of $V_{OUT}$<br>1: 10% of $V_{OUT}$ |
| 0 | R/W | VOUT_UV_ HYSTERESIS | 1’b0 | Sets the $V_{OUT}$ under-voltage protection (UVP) hysteresis.<br>0: 5% of $V_{OUT}$<br>1: 10% of $V_{OUT}$ |

### MFR_PWM_CTRL (DAh)

**Format:** Unsigned binary

The MFR_PWM_CTRL command sets the switching rising and falling slew rates.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:6 | R/W | RESERVED | 2'b00 | Reserved. |
| 5:4 | R/W | SWITCHING_ RISING_ SLEW_RATE | 2'b01 | Sets the switching rising slew rate.<br>**Bits** 00 01 10 11<br>**Slew Rate** 2V/ns 4V/ns 6V/ns 8V/ns |
| 3:2 | R/W | RESERVED | 2'b00 | Reserved. |
| 1:0 | R/W | SWITCHING_ FALLING_ SLEW_RATE | 2'b01 | Sets the switching falling slew rate.<br>**Bits** 00 01 10 11<br>**Slew Rate** 2V/ns 4V/ns 6V/ns 8V/ns |

### MFR_GPIO_CTRL (DBh)

**Format:** Unsigned binary

The MFR_GPIO_CTRL command determines the GPIO pin behavior when set as a digital output. The GPIO pin is pulled down to indicate faults that are enabled via MFR_GPIO_CTRL. On Page 0, MFR_GPIO_CTRL sets the GPIO0B behavior for channel 0. On Page 1, MFR_GPIO_CTRL sets the GPIO1B behavior for channel 1.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:5 | R/W | RESERVED | 3'b000 | Reserved. |
| 4 | R/W | VIN_OVER_ VOLTAGE_ INDICATE | 1'b0 | Enables GPIO $V_{IN}$ over-voltage (OV) fault indication.<br>0: Disabled<br>1: Enabled |
| 3 | R/W | OVER_ TEMPERATURE_ INDICATE | 1'b0 | Enables GPIO over-temperature (OT) fault indication.<br>0: Disabled<br>1: Enabled |
| 2 | R/W | VOUT_UNDER_ VOLTAGE_ INDICATE | 1'b0 | Enables GPIO $V_{OUT}$ under-voltage (UV) fault indication.<br>0: Disabled<br>1: Enabled |
| 1 | R/W | VOUT_OVER_ VOLTAGE_ INDICATE | 1'b0 | Enables GPIO $V_{OUT}$ OV fault indication.<br>0: Disabled<br>1: Enabled |
| 0 | R/W | OVER_CURRENT_ INDICATE | 1'b0 | Enables GPIO $V_{OUT}$ over-current (OC) fault indication.<br>0: Disabled<br>1: Enabled |

### MFR_GPIO_MODE (DCh)

**Format:** Unsigned binary

The MFR_GPIO_CTRL command sets the GPIO mode. On Page 0, MFR_GPIO_CTRL sets GPIO0B's mode. On Page 1, MFR_GPIO_CTRL sets GPIO1B's mode.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:1 | R/W | RESERVED | 7'b0000000 | Reserved. |

| | | | | |
|---|---|---|---|---|
| 0 | R/W | GPIO_MODE | 1’b0 | Sets the GPIO mode. See the General I/O Ports (GPIO) section on page 20 for more details.<br>0: Analog input<br>1: Digital output |

### MFR_PRODUCT_ID (DDh)

**Format:** Unsigned binary

The MFR_PRODUCT_ID command indicates the product suffix number. This command is for manufacturer use only.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R | RESERVED | 4’b0000 | Reserved. |
| 3:0 | R/W | ID | 4’b0000 | Manufacturer use only. |

### MFR_PRODUCT_VERSION (DEh)

**Format:** Unsigned binary

The MFR_PRODUCT_VERSION command indicates the configuration revision number. This command is for manufacturer use only.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R | RESERVED | 4’b0000 | Reserved. |
| 3:0 | R/W | PRODUCT_ VERSION | 4’b0000 | Manufacturer use only. |

### MFR_OC_FAULT_LIMIT (E0h)

**Format:** Unsigned binary

The MFR_OC_FAULT_LIMIT command sets current limits.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>7</td><td>R/W</td><td>RESERVED</td><td>1’b0</td><td>Reserved.</td></tr>
<tr><td>6:4</td><td>R/W</td><td>PEAK_CURRENT_ LIMIT</td><td>3’b101</td><td>Sets the peak $I_{LIMIT}$.
<table>
<tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr>
<tr><td>000</td><td>1A</td><td>100</td><td>5A</td></tr>
<tr><td>001</td><td>2A</td><td>101</td><td>6A</td></tr>
<tr><td>010</td><td>3A</td><td>110</td><td>7A</td></tr>
<tr><td>011</td><td>4A</td><td>111</td><td>8A</td></tr>
</table></td></tr>
<tr><td>3</td><td>R/W</td><td>RESERVED</td><td>1’b0</td><td>Reserved.</td></tr>
<tr><td>2:0</td><td>R/W</td><td>VALLEY_CURRENT_ LIMIT</td><td>3’b011</td><td>Sets the valley $I_{LIMIT}$.
<table>
<tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr>
<tr><td>000</td><td>2A</td><td>100</td><td>6A</td></tr>
<tr><td>001</td><td>3A</td><td>101</td><td>7A</td></tr>
<tr><td>010</td><td>4A</td><td>110</td><td>8A</td></tr>
<tr><td>011</td><td>5A</td><td>111</td><td>9A</td></tr>
</table></td></tr>
</table>

### MFR_OC_RESPONSE (E1h)

**Format:** Unsigned binary

The MFR_OC_RESPONSE command sets the basic functions for when an over-current (OC) fault occurs.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:6 | R/W | OC_RESPONSE_MODE | 2'b10 | Sets the output OC fault response.<br>00: Current limit only. The device continues to operate while maintaining the output current at the value set by MFR_OC_FAULT_LIMIT<br>01: Deglitch off. The device continues to maintain the current set by MFR_OC_FAULT_LIMIT for the delay time according to bits[2:0] of this command. If the fault condition is still present at the end of the delay time, the device responds according to bit[5] of this command<br>10: The device shuts down immediately, and responds according to bit[5] of this command |
| 5 | R/W | RETRY_SETTING | 1'b1 | These bits set the output OC fault response behavior.<br>0: Latch-off. The device does not retry until the power is cycled or the device is enabled again<br>1: Hiccup. The device attempts to restart continuously. The retry interval is determined by bits[4:3] of this command |
| 4:3 | R/W | RETRY_INTERVAL | 2'b11 | Sets the retry interval.<br>**Bits** 00 01 10 11<br>**Retry Interval** 20ms 50ms 100ms 150ms |
| 2:0 | R/W | DELAY_TIME | 3'b100 | Sets the delay time after an OC fault has occurred.<br>**Bits** **Value** **Bits** **Value**<br>000 10µs 100 50µs<br>001 20µs 101 60µs<br>010 30µs 110 70µs<br>011 40µs 111 80µs |

### MFR_VIN_OV_FAULT_RESPONSE (E2h)

**Format:** Unsigned binary

The MFR_VIN_OV_FAULT_RESPONSE command sets the basic functions for when an input over-voltage (OV) fault occurs.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:6 | R/W | VIN_OV_FAULT_RESPONSE_MODE | 2'b10 | Sets the $V_{IN}$ OV fault response.<br>00: Ignore. The device takes no action and continues to operate without interruption<br>01: Not supported<br>10: The device shuts down immediately and responds according to bit[5] of this command |
| 5 | R/W | RETRY_SETTING | 1'b1 | Sets the $V_{OUT}$ behavior after the $V_{IN}$ OV fault is removed.<br>0: The device does not attempt to restart<br>1: The device attempts to restart continuously. The retry interval is determined by bits[4:3] of this command |
| 4:3 | R/W | RETRY_INTERVAL | 2'b00 | Sets the retry interval.<br>**Bits** 00 01 10 11<br>**Retry Interval** 20ms 50ms 100ms 150ms |
| 2:0 | R/W | RESERVED | 3'b000 | Reserved. |

### MFR_VOUT_OV_FAULT_LIMIT (E3h)

**Format:** Unsigned binary

The MFR_VOUT_OV_FAULT_LIMIT command sets the $V_{OUT}$ over-voltage protection (OVP) threshold.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:1 | R/W | RESERVED | 7'b0000000 | Reserved. |
| 0 | R/W | VOUT_OV_FAULT_LIMIT | 1'b0 | Sets the $V_{OUT}$ OVP threshold.<br>0: 15% of $V_{OUT}$<br>1: 20% of $V_{OUT}$ |

### MFR_VOUT_OV_FAULT_RESPONSE (E4h)

**Format:** Unsigned binary

The MFR_VOUT_OV_FAULT_RESPONSE command sets the basic functions for when an output over-voltage (OV) fault occurs.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>7:6</td><td>R/W</td><td>VOUT_OV_FAULT_RESPONSE_MODE</td><td>2'b11</td><td>Sets the $V_{OUT}$ OV fault response.<br>00: Ignore. The device takes no action and continues to operate without interruption<br>01: Deglitch off. The device continues to operate for the delay time specified in bits[2:0] of this command. If the fault condition is still present at the end of the delay time, the device responds according to bit[5] of this command<br>10: The device shuts down immediately and responds according to bit[5] of this command<br>11: Discharge mode. The LS-FET turns on to discharge the output until the current reaches the negative current limit</td></tr>
<tr><td>5</td><td>R/W</td><td>RETRY_SETTING</td><td>1'b0</td><td>Sets the $V_{OUT}$ OV fault response behavior.<br>0: Latch-off. The device does not retry until the power is cycled or the device is enabled again<br>1: Hiccup. The device attempts to restart continuously. The retry interval is determined by bits[4:3] of this command</td></tr>
<tr><td>4:3</td><td>R/W</td><td>RETRY_INTERVAL</td><td>2'b00</td><td>Sets the retry interval.
<table>
<tr><th>Bits</th><td>00</td><td>01</td><td>10</td><td>11</td></tr>
<tr><th>Retry Interval</th><td>20ms</td><td>50ms</td><td>100ms</td><td>150ms</td></tr>
</table></td></tr>
<tr><td>2:0</td><td>R/W</td><td>DELAY_TIME</td><td>3'b000</td><td>Sets the delay time after an OV fault has occurred.
<table>
<tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr>
<tr><td>000</td><td>10µs</td><td>100</td><td>50µs</td></tr>
<tr><td>001</td><td>20µs</td><td>101</td><td>60µs</td></tr>
<tr><td>010</td><td>30µs</td><td>110</td><td>70µs</td></tr>
<tr><td>011</td><td>40µs</td><td>111</td><td>80µs</td></tr>
</table></td></tr>
</table>

### MFR_VOUT_UV_FAULT_LIMIT (E5h)

**Format:** Unsigned binary

The MFR_VOUT_UV_FAULT_LIMIT command sets the $V_{OUT}$ UVP threshold.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:1 | R/W | RESERVED | 7'b0000000 | Reserved. |
| 0 | R/W | VOUT_UV_FAULT_LIMIT | 1'b1 | This bit sets the $V_{OUT}$ UVP threshold.<br>0: -15% of $V_{OUT}$<br>1: -10% of $V_{OUT}$ |

### MFR_VOUT_UV_FAULT_RESPONSE (E6h)

**Format:** Unsigned binary

The MFR_VOUT_OV_FAULT_RESPONSE command sets the basic functions for when an output under-voltage (UV) fault occurs.

<table>
<tr><th>Bits</th><th>Access</th><th>Bit Name</th><th>Default</th><th>Description</th></tr>
<tr><td>7:6</td><td>R/W</td><td>VOUT_UV_FAULT_<br>RESPONSE_MODE</td><td>10</td><td>Sets the $V_{OUT}$ UV fault response.<br><br>00: Ignore. The device takes no action and continues to operate without interruption<br>01: Deglitch off. The device continues to operate for the delay time specified in bits[2:0] of this command. If the fault condition is still present at the end of the delay time, the device responds according to bit[5] of this command<br>10: The device shuts down immediately and responds according to bit[5] of this command</td></tr>
<tr><td>5</td><td>R/W</td><td>RETRY_SETTING</td><td>1</td><td>Sets the $V_{OUT}$ UV fault response behavior.<br><br>0: Latch-off. The device does not retry until the power is cycled or the device is enabled again<br>1: Hiccup. The device attempts to restart continuously. The retry interval is determined by bits[4:3] of this command</td></tr>
<tr><td>4:3</td><td>R/W</td><td>RETRY_INTERVAL</td><td>11</td><td>Sets the retry interval.<br><table><tr><th>Bits</th><td>00</td><td>01</td><td>10</td><td>11</td></tr><tr><th>Retry Interval</th><td>20ms</td><td>50ms</td><td>100ms</td><td>150ms</td></tr></table></td></tr>
<tr><td>2:0</td><td>R/W</td><td>DELAY_TIME</td><td>100</td><td>Sets the delay time after a UV fault has occurred.<br><table><tr><th>Bits</th><th>Value</th><th>Bits</th><th>Value</th></tr><tr><td>000</td><td>10µs</td><td>100</td><td>50µs</td></tr><tr><td>001</td><td>20µs</td><td>101</td><td>60µs</td></tr><tr><td>010</td><td>30µs</td><td>110</td><td>70µs</td></tr><tr><td>011</td><td>40µs</td><td>111</td><td>80µs</td></tr></table></td></tr>
</table>

### MFR_OT_FAULT_LIMIT (E7h)

**Format:** Unsigned binary

The MFR_OT_FAULT_LIMIT command sets the thermal shutdown threshold.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:0 | R/W | MFR_OT_FAULT_<br>LIMIT | 8’b10010110 | Sets the thermal shutdown threshold. 1°C/LSB. |

### MFR_RAIL_ADDRESS (E8h)

**Format:** Unsigned binary

The MFR_RAIL_ADDRESS command determines the rail address. When the rail address is enabled (bit[7] = 1), the second $I^2C$ slave address, which is set by bits[6:0], is active. Both the original $I^2C$ address and this rail address can be used to communicate with the MP8886.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7 | R/W | ENABLE | 1’b0 | Enables the rail address.<br><br>0: Disabled<br>1: Enabled |
| 6:0 | R/W | ADDRESS | 7’b0000000 | Sets the 7-bit PMBus address. |

### MFR_LIGHT_CTRL (E9h)

**Format:** Unsigned binary

The MFR_LIGHT_CTRL command sets the PWM operation mode and the AAM mode threshold to decrease $f_{SW}$ or skip the switching pulse.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7 | R/W | PWM_MODE | 1'b0 | Selects the PWM operation mode (AAM mode or FCCM).<br>0: AAM mode<br>1: FCCM |
| 6:3 | R/W | AAM_THRESHOLD_FOR_EXTENDING_FREQUENCY | 4'b0001 | Sets the AAM mode threshold, where $f_{SW}$ starts to decrease.<br>Bits / Value / Bits / Value<br>0000 350mA 1000 750mA<br>0001 400mA 1001 800mA<br>0010 450mA 1010 850mA<br>0011 500mA 1011 900mA<br>0100 550mA 1100 950mA<br>0101 600mA 1101 1000mA<br>0110 650mA 1110 1050mA<br>0111 700mA 1111 1100mA |
| 2:0 | R/W | AAM_THRESHOLD_FOR_BLANKING_CLOCK | 3'b001 | Sets the AAM mode threshold, where the switching pulse can be skipped.<br>Bits / Value / Bits / Value<br>000 200mA 100 600mA<br>001 300mA 101 700mA<br>010 400mA 110 800mA<br>011 500mA 111 900mA |

### MFR_PWR_STAGE_SET (EAh)

**Format:** Unsigned binary

The MFR_PWR_STAGE_SET command determines whether the MP8886's operation mode is set by the GPIO1B pin or the MTP.

| Bits | Access | Bit Name | Default | Description |
|---|---|---|---|---|
| 7:4 | R/W | RESERVED | 3'b000 | Reserved. |
| 3 | R/W | POWER_STAGE_CONTROL | 1'b0 | Determines whether the operation mode is set by the GPIO1B pin or the MTP (register EAh, bits[2:0]). See the Operation Mode Selection section on page 23 for more details.<br>0: The GPIO1B pin sets the operation mode<br>1: The MTP sets the operation mode according to bits[2:0] of this command |
| 2:0 | R/W | POWER_STAGE_MODE | 3'b000 | Sets the power stage mode for up to 4-phase operation.<br>Application / Bits / Operation Mode<br>Single IC 000 Single-phase, 6A operation<br>Single IC 001 Dual-phase, single-output operation<br>Single IC 111 Dual-output operation<br>Multiple ICs 010 Master of multiple ICs<br>Multiple ICs 011 Slave of multiple ICs<br>- 101 Reserved |

## DEFAULT MTP CONFIGURATIONS

Table 4 shows the default MTP configurations for the MP8886GUT-0000.

**Table 4: MP8886GUT-0000 Default MTP Configurations**

| Items | Channel 0 | Channel 1 |
|---|---|---|
| VOUT_SET_MODE | Internal feedback divider mode | Internal feedback divider mode |
| MFR_VOUT_CTRL | 1:4, 0.6V to 6.138V | 1:4, 0.6V to 6.138V |
| OUTPUT_VOLTAGE | 3.3V | 3.3V |
| OUTPUT_INITIAL_STATE | On | On |
| PWM_MODE | AAM mode | AAM mode |
| TON_RISE | 1ms | 1ms |
| TOFF_FALL | 1ms | 1ms |
| PEAK_CURRENT_LIMIT | 6A | 6A |
| VALLEY_CURRENT_LIMIT | 5A | 5A |
| OCP_RESPONSE_MODE | Hiccup mode | Hiccup mode |
| SWITCHING_FREQUENCY_SET | 600kHz | |
| OPERATION_MODE_SET | GPIO1B set | |
| PMBUS_ADDRESS | 0x00 with $R_{ADDR}$ = 0Ω | |
| MTP_CONFIGURE_CODE | 0x0000 | |

Table 5 shows the default register values for the MP8886GUT-0000.

**Table 5: MP8886GUT-0000 Default Register Values**

| Suffix Code | Page | Register | Hex Value | Suffix Code | Page | Register | Hex Value |
|---|---|---|---|---|---|---|---|
| 0000 | 0 | 01 | 80 | 0000 | 0 | E7 | 96 |
| 0000 | 0 | 21 | 226 | 0000 | 0 | E8 | 0 |
| 0000 | 0 | 24 | 3FF | 0000 | 0 | E9 | 9 |
| 0000 | 0 | 25 | 252 | 0000 | 0 | EA | 0 |
| 0000 | 0 | 26 | 1FA | 0000 | 1 | 01 | 80 |
| 0000 | 0 | 35 | 24 | 0000 | 1 | 21 | 226 |
| 0000 | 0 | 36 | 22 | 0000 | 1 | 24 | 3FF |
| 0000 | 0 | 55 | 1D6 | 0000 | 1 | 25 | 252 |
| 0000 | 0 | 60 | 0 | 0000 | 1 | 26 | 1FA |
| 0000 | 0 | 61 | 1 | 0000 | 1 | 35 | 24 |
| 0000 | 0 | 64 | 0 | 0000 | 1 | 36 | 22 |
| 0000 | 0 | 65 | 1 | 0000 | 1 | 55 | 1D6 |
| 0000 | 0 | D0 | 0 | 0000 | 1 | 60 | 0 |
| 0000 | 0 | D1 | 0 | 0000 | 1 | 61 | 1 |
| 0000 | 0 | D2 | 1A | 0000 | 1 | 64 | 0 |
| 0000 | 0 | D3 | 4 | 0000 | 1 | 65 | 1 |
| 0000 | 0 | D4 | 3 | 0000 | 1 | D2 | 1A |
| 0000 | 0 | D5 | 0 | 0000 | 1 | D3 | 4 |
| 0000 | 0 | D6 | 40 | 0000 | 1 | D6 | 40 |
| 0000 | 0 | D7 | 2A | 0000 | 1 | D7 | 2A |
| 0000 | 0 | D8 | 0 | 0000 | 1 | D8 | 0 |
| 0000 | 0 | D9 | 0 | 0000 | 1 | D9 | 0 |
| 0000 | 0 | DA | 11 | 0000 | 1 | DA | 11 |
| 0000 | 0 | DB | 0 | 0000 | 1 | DB | 0 |
| 0000 | 0 | DC | 0 | 0000 | 1 | DC | 0 |
| 0000 | 0 | DD | 0 | 0000 | 1 | E0 | 53 |
| 0000 | 0 | DE | 0 | 0000 | 1 | E1 | BC |
| 0000 | 0 | E0 | 53 | 0000 | 1 | E2 | A0 |
| 0000 | 0 | E1 | BC | 0000 | 1 | E3 | 0 |
| 0000 | 0 | E2 | A0 | 0000 | 1 | E4 | C0 |
| 0000 | 0 | E3 | 0 | 0000 | 1 | E5 | 1 |
| 0000 | 0 | E4 | C0 | 0000 | 1 | E6 | BC |
| 0000 | 0 | E5 | 1 | 0000 | 1 | E9 | 9 |
| 0000 | 0 | E6 | BC | - | - | - | - |

Table 6 shows the default MTP configurations for the MP8886GUT-0002.

**Table 6: MP8886GUT-0002 Default MTP Configurations**

| Items | Channel 0 | Channel 1 |
|---|---|---|
| VOUT_SET_MODE | External feedback divider mode | External feedback divider mode |
| MFR_VOUT_CTRL | 1:16, 0.6V to 24.552V | 1:16, 0.6V to 24.552V |
| REFRENCE_VOLTAGE | 0.6V | 0.6V |
| OUTPUT_INITIAL_STATE | On | On |
| PWM_MODE | AAM mode | AAM mode |
| TON_RISE | 1ms | 1ms |
| TOFF_FALL | 1ms | 1ms |
| PEAK_CURRENT_LIMIT | 6A | 6A |
| VALLEY_CURRENT_LIMIT | 5A | 5A |
| OCP_RESPONSE_MODE | Hiccup mode | Hiccup mode |
| SWITCHING_FREQUENCY_SET | 600kHz | |
| OPERATION MODE SET | GPIO1B set | |
| PMBUS_ADDRESS | 0x00 with $R_{ADDR}$ = 0Ω | |
| MTP_CONFIGURE_CODE | 0x0002 | |

Table 7 shows the default register values for the MP8886GUT-0002.

**Table 7: MP8886GUT-0002 Default Register Values**

| Suffix Code | Page | Register | Hex Value | Suffix Code | Page | Register | Hex Value |
|---|---|---|---|---|---|---|---|
| 0002 | 0 | 01 | 80 | 0002 | 0 | E7 | 96 |
| 0002 | 0 | 21 | 190 | 0002 | 0 | E8 | 0 |
| 0002 | 0 | 24 | 3FF | 0002 | 0 | E9 | 9 |
| 0002 | 0 | 25 | 252 | 0002 | 0 | EA | 0 |
| 0002 | 0 | 26 | 1FA | 0002 | 1 | 01 | 80 |
| 0002 | 0 | 35 | 24 | 0002 | 1 | 21 | 190 |
| 0002 | 0 | 36 | 22 | 0002 | 1 | 24 | 3FF |
| 0002 | 0 | 55 | 1D6 | 0002 | 1 | 25 | 252 |
| 0002 | 0 | 60 | 0 | 0002 | 1 | 26 | 1FA |
| 0002 | 0 | 61 | 1 | 0002 | 1 | 35 | 24 |
| 0002 | 0 | 64 | 0 | 0002 | 1 | 36 | 22 |
| 0002 | 0 | 65 | 1 | 0002 | 1 | 55 | 1D6 |
| 0002 | 0 | D0 | 0 | 0002 | 1 | 60 | 0 |
| 0002 | 0 | D1 | 0 | 0002 | 1 | 61 | 1 |
| 0002 | 0 | D2 | C | 0002 | 1 | 64 | 0 |
| 0002 | 0 | D3 | 4 | 0002 | 1 | 65 | 1 |
| 0002 | 0 | D4 | 3 | 0002 | 1 | D2 | C |
| 0002 | 0 | D5 | 0 | 0002 | 1 | D3 | 4 |
| 0002 | 0 | D6 | 40 | 0002 | 1 | D6 | 40 |
| 0002 | 0 | D7 | 2A | 0002 | 1 | D7 | 2A |
| 0002 | 0 | D8 | 0 | 0002 | 1 | D8 | 0 |
| 0002 | 0 | D9 | 0 | 0002 | 1 | D9 | 0 |
| 0002 | 0 | DA | 11 | 0002 | 1 | DA | 11 |
| 0002 | 0 | DB | 0 | 0002 | 1 | DB | 0 |
| 0002 | 0 | DC | 0 | 0002 | 1 | DC | 0 |
| 0002 | 0 | DD | 2 | 0002 | 1 | E0 | 53 |
| 0002 | 0 | DE | 0 | 0002 | 1 | E1 | BC |
| 0002 | 0 | E0 | 53 | 0002 | 1 | E2 | A0 |
| 0002 | 0 | E1 | BC | 0002 | 1 | E3 | 0 |
| 0002 | 0 | E2 | A0 | 0002 | 1 | E4 | C0 |
| 0002 | 0 | E3 | 0 | 0002 | 1 | E5 | 1 |
| 0002 | 0 | E4 | C0 | 0002 | 1 | E6 | BC |
| 0002 | 0 | E5 | 1 | 0002 | 1 | E9 | 9 |
| 0002 | 0 | E6 | BC | - | - | - | - |

# APPLICATION INFORMATION

## Setting the Output Voltage

The MP8886 has two modes to set the output voltage: internal feedback divider mode and external feedback divider mode.

VOUT_COMMAND sets the feedback reference voltage with 1.5mV/LSB and a maximum value of 1.5345V. $V_{OUT}$ is determined by the reference voltage and FB divider ratio. In internal feedback divider mode, the internal FB divider ratio is set by MFR_VOUT_CTRL (0xD2) (see Table 8)

**Table 8: Internal Feedback Divider Mode**

| MFR_VOUT_CTRL, Bits[2:0] | Internal FB Divider Ratio (11) | Output Range |
|---|---|---|
| 000 | 1:1, range 1 | 0.6V to 1.5345V |
| 001 | 1:2, range 2 | 0.6V to 3.069V |
| 010 | 1:4, range 3 | 0.6V to 6.138V |
| 011 | 1:8, range 4 | 1.2V to 12.276V |
| 100 | 1:16, range 5 | 2.4V to 24.552V |

**Note:**

11) The internal divider ratio is defined as R2 / (R1 + R2).

In external feedback divider mode, the external resistor divider sets $V_{OUT}$. In addition, the internal FB divider ratio should be set to 1:16 when using the external divider. It is recommended to choose a resistor between 10kΩ and 100kΩ for R2. R1 can be calculated with Equation (10):

$$R1 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R2 \quad (10)$$

Figure 15 shows the external feedback circuit.

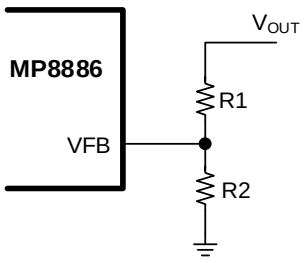



**Figure 15: Feedback Network**

## Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Place the input capacitor as close to the VIN pin as possible.

Since $C_{IN}$ absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (11):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (11)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (12):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (12)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor determines the input voltage ripple. Select an input capacitor that meets the input voltage ripple requirement in the system. The input voltage ripple can be estimated with Equation (13):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

The worst-case condition occurs at $V_{IN} = 2 \times V_{OUT}$, calculated with Equation (14):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (14)$$

## Selecting the Output Capacitor

The output capacitor must maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (15):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (15)$$

For ceramic capacitors, the capacitance dominates the impedance at $f_{SW}$ and causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (16):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

When using capacitors with a higher ESR (e.g. and electrolytic capacitor), the ESR dominates the impedance at $f_{SW}$. The output voltage ripple can be determined by the ESR values. For simplification, the output ripple can be estimated with Equation (17):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (17)$$

Larger-value output capacitors reduce output voltage ripple and improve load transient response. However, the maximum output capacitance limit should be also considered in design application. If the output capacitor value is too large, the output voltage cannot reach the target value during soft start, and then it fails to regulate. The maximum output capacitor ($C_{O\_MAX}$) can be calculated with Equation (18):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times t_{ss} / V_{OUT} \quad (18)$$

Where $I_{LIM\_AVG}$ is the average start-up current during soft start, and $t_{SS}$ is the soft-start time.

### Selecting the Inductor

**MPL Optimized Performance with MPS Inductor MPL1050 Series**

The inductor supplies constant current to the output load while being driven by the high-frequency SW node voltage.

A larger-value inductor results in less ripple current and lower output voltage ripple, but also has a larger physical size, higher series resistance, and lower saturation current.

A good rule to determine the inductance value is to allow the peak-to-peak ripple current in the inductor to be 30% to 60% of the maximum output load current. The inductance value can be estimated with Equation (19):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (19)$$

Where $\Delta I_L$ is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (20):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 9 lists our power inductor recommendations. Select a part number based on your design requirements.

**Table 9: Power Inductor Selection**

| Part Number | Inductor Value | Manufacturer |
|---|---|---|
| MPL-AY1050-4R7 | 4.7μH | MPS |

Visit Monolithicpower.com under Products > Inductors for more information

## PCB Layout Guidelines

An optimized PCB layout is critical for reliable operation. For the best results, refer to Figure 16 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
3. Route the high-current paths (PGND, IN, and OUT) using short and wide traces.
4. Place as many PGND vias as possible close to the PGND pin to reduce parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the VCC and AGND pins.
6. Connect the AGND and PGND pins at the VCC capacitor's ground point.
7. Place the BST capacitor as close to the BST and SW pins as possible.
8. Place the external feedback resistors close to the VFB pin.
9. Avoid routing sensitive traces close to the input plane and SW node.

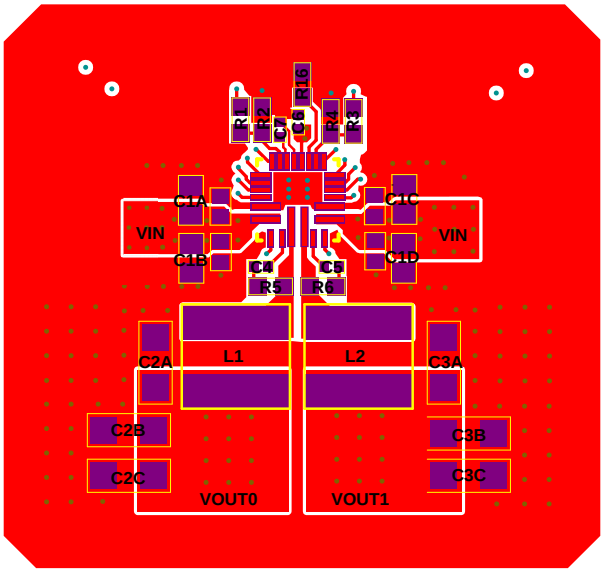



**Figure 16: Recommended PCB Layout (Placement and Top Layer)**

# TYPICAL APPLICATION CIRCUITS

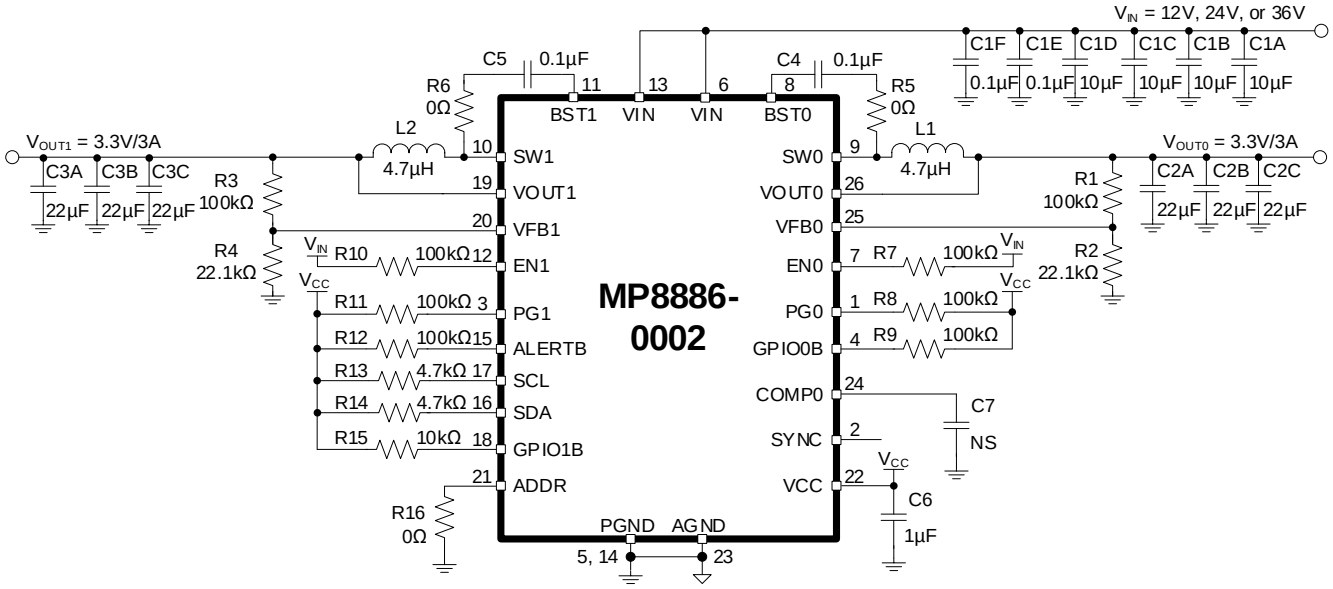



**Figure 17: Typical Application Circuit with Dual Outputs and an External Feedback Divider (MP8886-0002, $V_{IN}$ = 12V, 24V, or 36V, $V_{OUT0}$ = $V_{OUT1}$ = 3.3V/3A)**

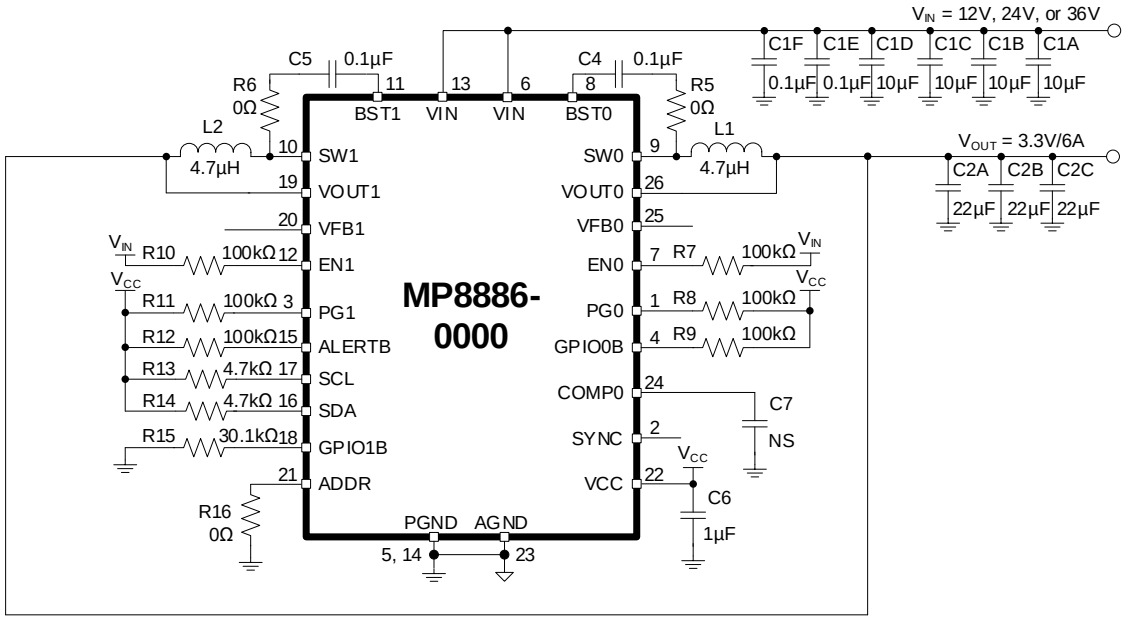



**Figure 18: Typical Application Circuit with 2 Phases, a Single Output, and an Internal Feedback Divider (MP8886-0000, $V_{IN}$ = 12V, 24V, or 36V, $V_{OUT}$ = 3.3V/6A)**

## TYPICAL APPLICATION CIRCUITS *(continued)*

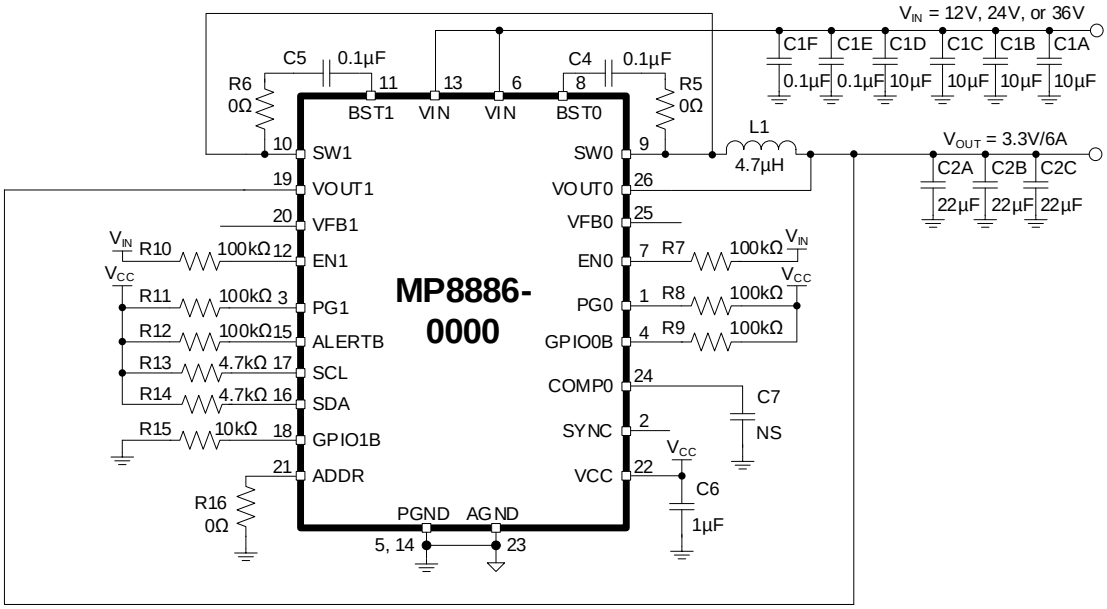



**Figure 19: Typical Application Circuit with 1 Phase, 6A Output, and an Internal Feedback Divider (MP8886-0000, $V_{IN}$ = 12V, 24V, or 36V, $V_{OUT}$ = 3.3V/6A)**

## TYPICAL APPLICATION CIRCUITS *(continued)*

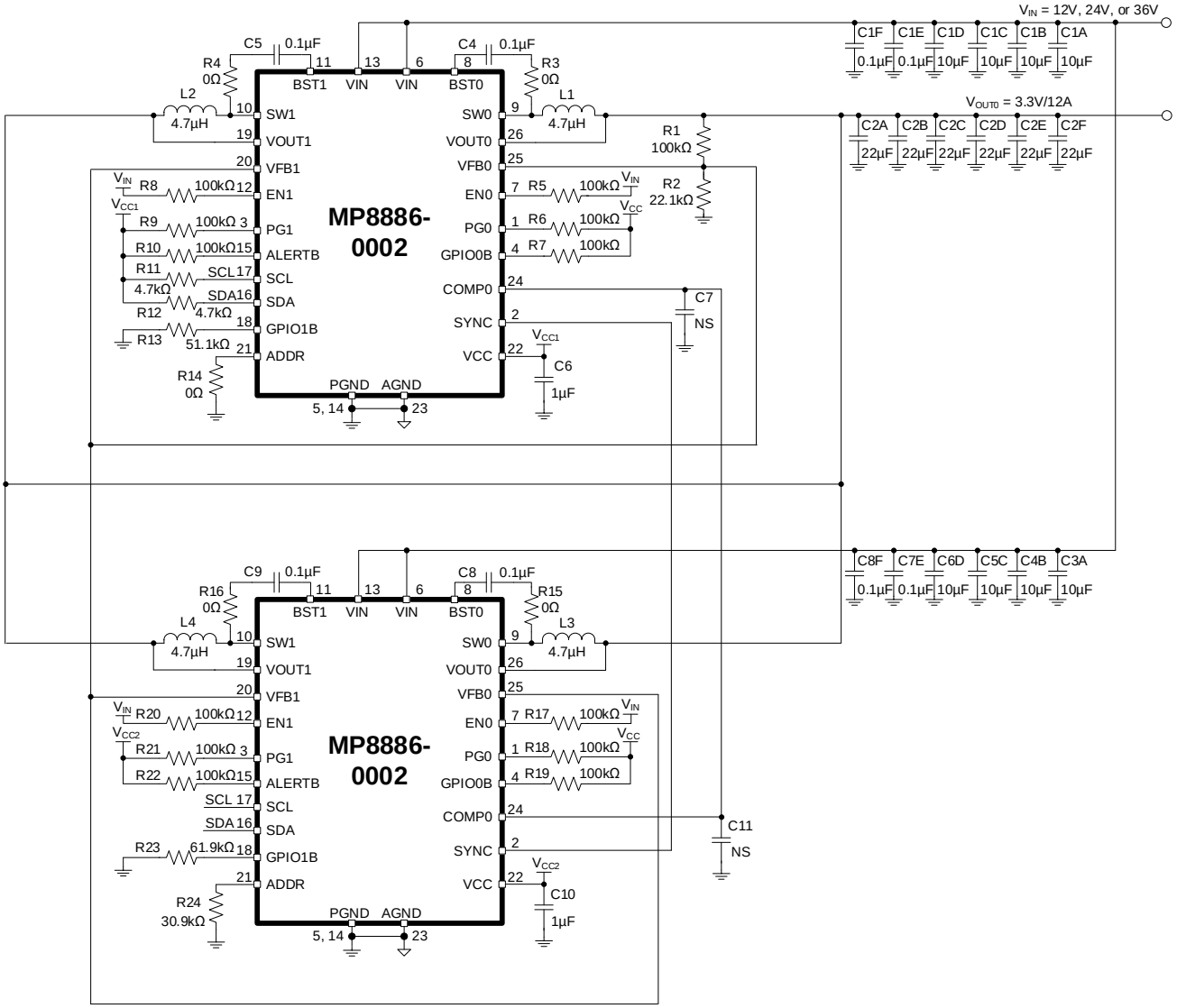
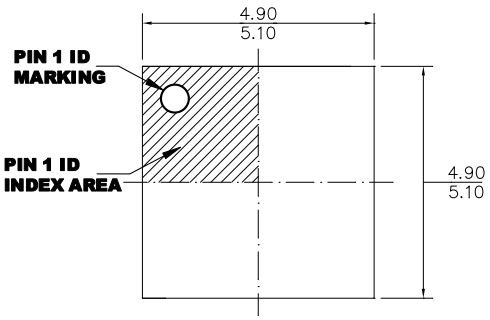


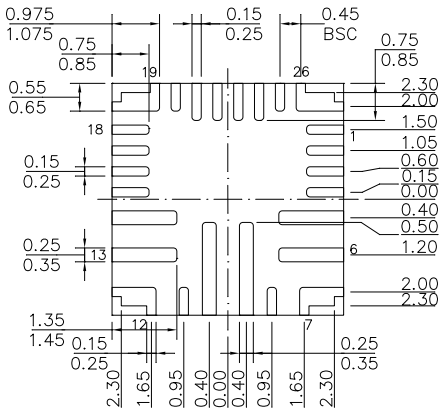

**Figure 20: Typical Application Circuit with 2 Paralleled Devices, 4 Phases, 12A Output, and an External Output Voltage Divider (MP8886-0002, $V_{IN}$ = 12V, 24V, or 36V, $V_{OUT}$ = 3.3V/12A)**

# PACKAGE INFORMATION

## TQFN-26 (5mmx5mm)

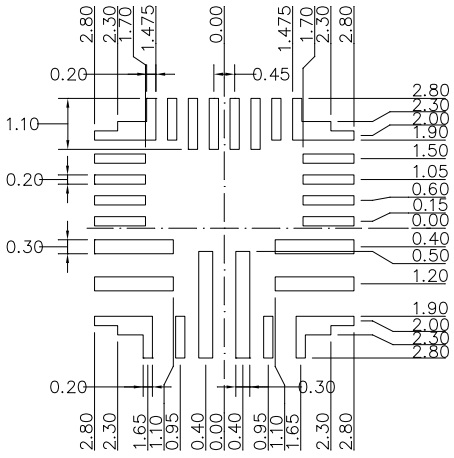



**TOP VIEW**




**BOTTOM VIEW**


**SIDE VIEW**

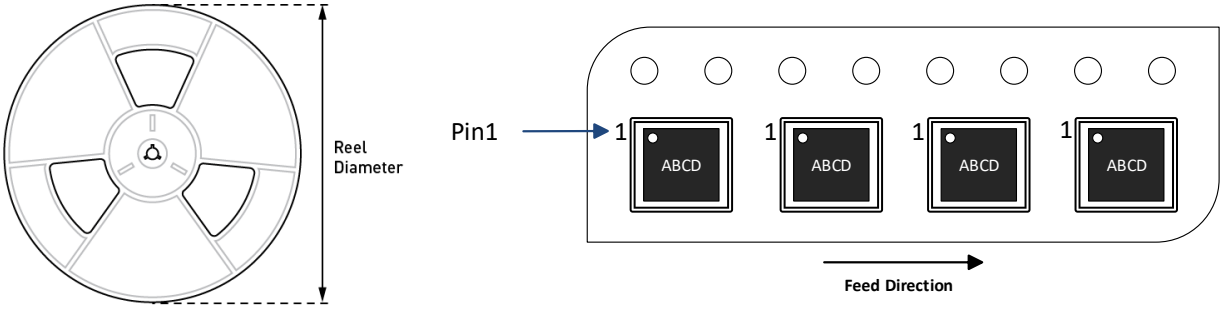



**RECOMMENDED LAND PATTERN**

**NOTE:**

**1) LAND PATTERNS OF PIN 5 AND PIN 6, AND PIN 13 AND PIN 14 HAVE THE SAME LENGTH AND WIDTH.**
**2) LAND PATTERNS OF PIN 9 AND PIN 10 HAVE THE SAME LENGTH AND WIDTH.**
**3) ALL DIMENSIONS ARE IN MILLIMETERS.**
**4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.**
**5) REFERENCEIS MO-220.**
**6) DRAWING IS NOT TO SCALE.**

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Quantity/ Tray | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|---|
| MP8886GUT-0000-Z | TQFN-26 (5mmx5mm) | 5000 | N/A | N/A | 13in | 12mm | 8mm |
| MP8886GUT-0002-Z | | | | | | | |
| MP8886GUT-xxxx-Z | | | | | | | |

## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 2/29/2024 | Initial Release | - |