MPM3690-50D

16V, 50A, High-Efficiency DC/DC Power Module with PMBus

DESCRIPTION

The MPM3690-50D is a 50A, fully integrated power module with a PMBus interface. It integrates a monolithic DC/DC converter, power inductor, and other passive components. The MPM3690-50D offers a complete power solution with excellent line and load regulation across a wide input voltage (V_{IN}) range and load range.

The device integrates two interleaved phases in a single molded power module. The device adopts MPS's proprietary, multi-phase constant-on-time (MCOT) control scheme, which provides ultra-fast transient response, simple loop compensation, and minimizes the output capacitance. The PMBus interface provides module configurations and monitors key parameters.

Full protection functions include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPM3690-50D is available in a BGA (16mmx16mmx5.18mm) package.

FEATURES

- 3V to 16V Input Voltage (V_{IN}) Range with External 3.3V V_{CC} Bias
- 4V to 16V V_{IN} Range with Internal V_{CC} Bias
- 0.5V to 3.6V Output Voltage (V_{OUT}) Range
- 50A Continuous Current for Up to 1.8V Output
- V_{OUT} Remote Sense
- ±1% Reference Voltage Accuracy (-40°C to +125°C)
- PMBus 1.3 Compliant
- Telemetry Read Back Including V_{IN}, V_{OUT}, Output Current (I_{OUT}), Temperature, and Faults
- Configurable via the PMBus:
  - V_{OUT}
  - Soft-Start Time (t_{SS})
  - Over-Current (OC), Over-Temperature (OT), Over-Voltage (OV), Under-Voltage (UV), and Under-Voltage Lockout (UVLO) Limits
  - Pulse-Width Modulation (PWM) Mode
  - Switching Frequency (f_{SW})
- Available in a BGA (16mmx16mmx5.18mm) Package

APPLICATIONS

- Telecom and Networking Equipment
- Industrial Equipment
- FPGA and ASIC Power Systems

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TYPICAL APPLICATION

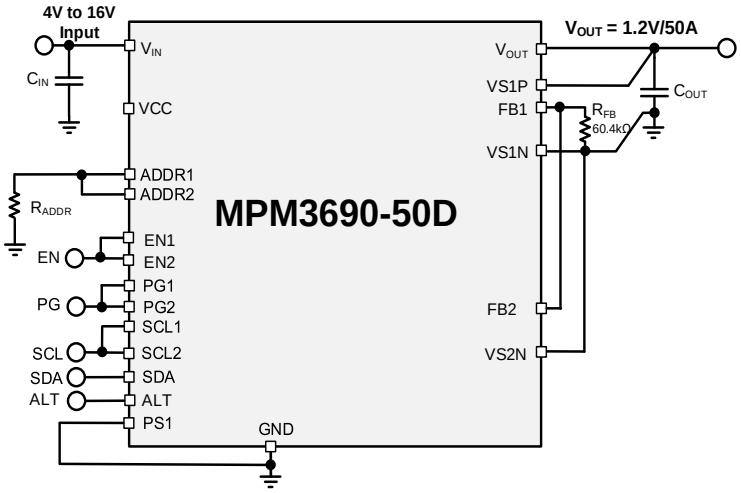
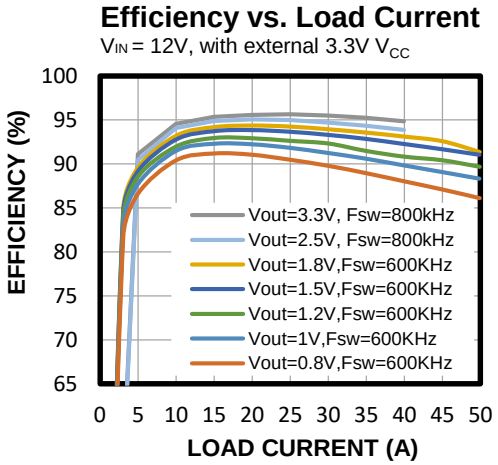


Figure 1: Interleaved Operation (1.2V, 50A)



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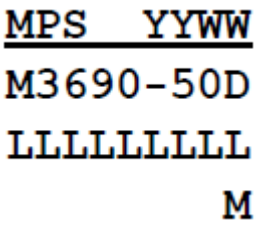
ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MPM3690GBF-50D-xxxx**	BGA (16mmx16mmx5.18mm)	*See Below*	3
MPM3690GBF-50D-0001	BGA (16mmx16mmx5.18mm)	*See Below*	3
MPM3690GBF-50D-2222	BGA (16mmx16mmx5.18mm)	*See Below*	3

* For Tray, add suffix -T (e.g. MPM3690GBF-50D-xxxx-T).

** The 4-digit suffix code “xxxx” is the configuration identifier for the register settings stored in the multiple-time programmable (MTP) memory. The default configuration codes are “0001” and “2222”. For customized configurations, contact an MPS FAE to assign a 4-digit suffix code.

TOP MARKING (MPM3690GBF-50D)



MPS: MPS prefix
YY: Year code
WW: Week code
M3690-50D: Part number
LLLLLLLLL: Lot number
M: Module

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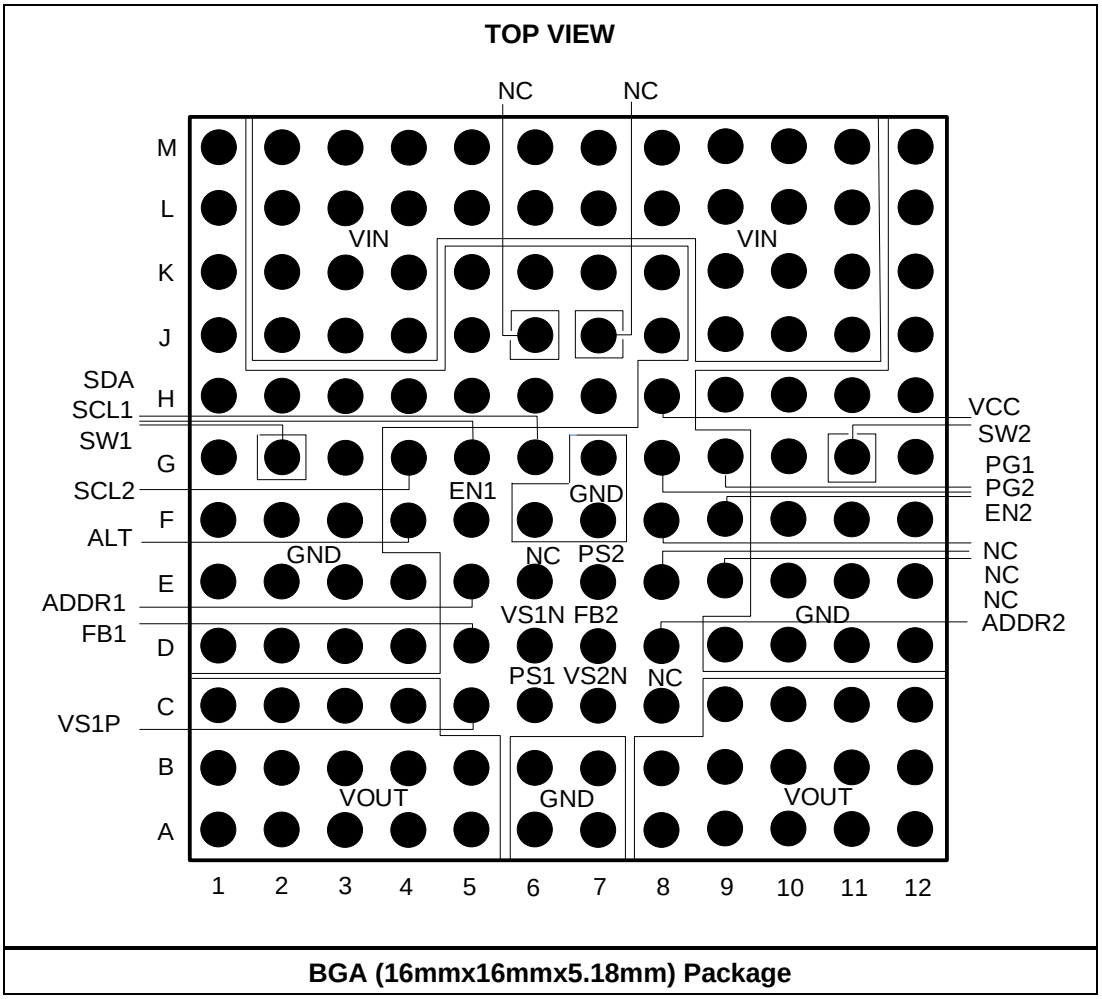
PACKAGE REFERENCE



BGA (16mmx16mmx5.18mm) Package

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PIN FUNCTIONS

Pin Number	Name	Description
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C1 C2, C3, C4, A8, A9, A10, A11, A12, B8, B9, B10, B11, B12, C9, C10, C11, C12	VOUT	**Power output.** The VOUT pins are power output pins
A6, A7, B6, B7, D1, D2, D3, D4, D9, D10, D11, D12, E1, E2, E3, E4, E10, E11, E12, F1, F2, F3, F6, F7, F10, F11, F12, G1, G3, G7, G10, G12, H1, H2, H3, H4, H5, H6, H7, H9, H10, H11, H12, J1, J5, J8, J12, K1, K5, K6, K7, K8, K12, L1, L12, M1, M12	GND	**Power ground.** GND is the ground of the regulated output voltage.
C5	VS1P	**Positive input of the remote sense amplifier.** Connect the VS1P pin to the remote sense point of the output voltage.
D6, C7	VS1N, VS2N	**Negative input of the remote sense amplifier.** Connect these pins to the remote sense point of the output GND to enable the remote sense. Connect VS1N and VS2N together.
C6, E7	PS1, PS2	**Phase-shedding.** With a proper PMBus setting, pull PS2 high to enable the slave phase. Pull PS2 low to disable the slave phase. Connect PS1 to GND.
D5, D7	FB1, FB2	**Feedback voltage.** Connect a resistor between FB1 and VS1N to configure the output voltage. FB1 is connected to VS1P with a 60.4kΩ resistor. Connect the FB1 and FB2 pins together.
E5, D8	ADDR1, ADDR2	**PMBus slave address setting pin.** Connect the ADDR1 and ADDR2 pins together. Connect a resistor from ADDR to GND to set the address of this device.
G5, G4	SCL1, SCL2	**PMBus serial clock.** Connect the SCL1 and SCL2 pins together.
C8, E6, E8, E9, F8, J6, J7	NC	**No connection (internally floated).** Float these pins**.**
F4	ALT	**PMBus alert.** The ALT pin is an active low, open-drain output. A pull-up resistor must be connected from ALT to a 3.3V rail.
F5, F9	EN1, EN2	**Converter control.** EN is a digital input that turns the regulator on or off. Drive EN high to turn the regulator on; drive it low to turn it off. Do not float this pin. Connect the EN1 and EN2 pins together.
G2, G11	SW1, SW2	**Switching nodes.** Float these pins.
G6	SDA	**PMBus serial data.**
G9, G8	PG1, PG2	**Power good outputs.** The output of the PG pins are open drains. Pull the PG pins high with a pull-up resistor. Connect the PG1 and PG2 pins together.
H8	VCC	**Output of the internal power supply.** Float the VCC pin or connect it to the external 3.3V power supply to improve efficiency.
M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, L2, L3, L4, L5, L6, L7, L8, L9, L10, L11, J2, J3, J4, J9, J10, J11, K2, K3, K4, K9, K10, K11	VIN	**Supply voltage.** Connect the input voltage between these pins and the GND pins.

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PIN MAP

Table 1: Pin Map for Pins A1~F12

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
A1	VOUT	B1	VOUT	C1	VOUT	D1	GND	E1	GND	F1	GND
A2	VOUT	B2	VOUT	C2	VOUT	D2	GND	E2	GND	F2	GND
A3	VOUT	B3	VOUT	C3	VOUT	D3	GND	E3	GND	F3	GND
A4	VOUT	B4	VOUT	C4	VOUT	D4	GND	E4	GND	F4	ALT
A5	VOUT	B5	VOUT	C5	VS1P	D5	FB1	E5	ADDR1	F5	EN1
A6	GND	B6	GND	C6	PS1	D6	VS1N	E6	NC	F6	GND
A7	GND	B7	GND	C7	VS2N	D7	FB2	E7	PS2	F7	GND
A8	VOUT	B8	VOUT	C8	NC	D8	ADDR2	E8	NC	F8	NC
A9	VOUT	B9	VOUT	C9	VOUT	D9	GND	E9	NC	F9	EN2
A10	VOUT	B10	VOUT	C10	VOUT	D10	GND	E10	GND	F10	GND
A11	VOUT	B11	VOUT	C11	VOUT	D11	GND	E11	GND	F11	GND
A12	VOUT	B12	VOUT	C12	VOUT	D12	GND	E12	GND	F12	GND

Table 2: Pin Map for Pins G1~M12

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	VIN	K2	VIN	L2	VIN	M2	VIN
G3	GND	H3	GND	J3	VIN	K3	VIN	L3	VIN	M3	VIN
G4	SCL2	H4	GND	J4	VIN	K4	VIN	L4	VIN	M4	VIN
G5	SCL1	H5	GND	J5	GND	K5	GND	L5	VIN	M5	VIN
G6	SDA	H6	GND	J6	NC	K6	GND	L6	VIN	M6	VIN
G7	GND	H7	GND	J7	NC	K7	GND	L7	VIN	M7	VIN
G8	PG2	H8	VCC	J8	GND	K8	GND	L8	VIN	M8	VIN
G9	PG1	H9	GND	J9	VIN	K9	VIN	L9	VIN	M9	VIN
G10	GND	H10	GND	J10	VIN	K10	VIN	L10	VIN	M10	VIN
G11	SW2	H11	GND	J11	VIN	K11	VIN	L11	VIN	M11	VIN
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{OUT} 6.5V
$V_{SW1/2}$ (DC) .....-0.3V to +18.3V
V_{CC} 4.5V
V_{CC} (1s) (2) 6V
All other pins .....-0.3V to +4.3V
All other pins (1s) (2) 6V
Continuous power dissipation (T_A = 25°C) (3) 18.59W
Junction temperature .....170°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +170°C

ESD Ratings

Human body model (HBM) ..... ±1000V
Charged device model (CDM)..... ±2000V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) .....4V to 16V
Supply voltage (V_{IN}) (5).....3V to 16V
Output voltage (V_{OUT}).....0.5V to 3.6V
CTRL, PG .....-0.3V to +3.6V
Other digital pins.....-0.3V to +3.6V
External V_{CC} bias .....3V to 3.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (6)

	θ_{JA}	θ_{JC}	
EVM3690-50D-BF-00A	7.8	4.1	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Voltage rating during MTP programming.
3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) An external 3.3V V_{CC} bias is required. Writing to the MTP is not supported with an external 3.3V V_{CC} bias.
6) Measured on the EVM3690-50D-BF-00A: a 4-layer PCB, 10cmx10cm.

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ELECTRICAL CHARACTERISTICS

Typical value is tested at T_J = 25°C, V_{IN} = 12V, min and max values at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input Voltage (V_{IN}) Supply Current						
Supply current (quiescent)	I_{IN}	V_{EN} = 0V		5	8	mA
V_{IN}						
Input voltage range	V_{IN}	Internal V_{CC}	4		16	V
		With external 3.3V V_{CC}	3		16	V
Output Voltage (V_{OUT}) (7)						
Output voltage range (7)	V_{OUT_RANGE}		0.5		3.6V	V
Load regulation (7)	$V_{OUT_DC_LOAD}$	I_{OUT} from 0A to 50A		±0.5%		V_{OUT}
Line regulation (7)	$V_{OUT_DC_LINE}$	V_{IN} from 4V to 16V, I_{OUT} = 50A		±0.5%		V_{OUT}
Output Current (I_{OUT}) Limit						
Individual valley current limit	I_{LIM}	Individual phase current limit, D7h, bits[4:0] = 5b'10010		27		A
Min individual valley current limit configurable value (7)		Individual phase current limit		3		A
Max individual valley current limit configurable value (7)		Individual phase current limit		27		A
Individual low-side negative current limit in over-voltage protection (OVP)	$I_{LIM_NEG_OVP}$	Individual phase current limit		-13		A
Frequency and Timer						
Switching frequency	f_{SW}	Individual phase		600		kHz
Minimum on time (7)	t_{ON_MIN}	f_{SW} = 1000kHz, V_{OUT} = 0.6V		50		ns
Minimum off time (7)	t_{OFF_MIN}	FB = 480mV		220		ns
Output OVP and Under-Voltage Protection (UVP)						
OVP threshold	V_{OVP}	D4h, bits[1:0] = 00	111%	115%	119%	V_{REF}
UVP threshold	V_{UVP}	D9h, bits[3:2] = 10	75%	79%	83%	V_{REF}
Max configurable OVP threshold	V_{OVP_MAX}	D4h, bits[1:0] = 11	126%	130%	134%	V_{REF}
Min configurable OVP threshold	V_{OVP_MIN}	D4h, bits[1:0] = 00	111%	115%	119%	V_{REF}
Max configurable UVP threshold	V_{UVP_MAX}	D9h, bits[3:2] = 11	80%	84%	88%	V_{REF}
Min configurable UVP threshold	V_{UVP_MIN}	D9h, bits[3:2] = 00	65%	69%	73%	V_{REF}
Enable (EN)						
Input high voltage	V_{IH_EN}		2.2			V
Input low voltage	V_{IL_EN}				1.20	V
Analog-to-Digital Converter (ADC) (7)						
Voltage range			0		1.28	V
ADC resolution				10		bits
DNL				1		LSB
Sample rate				3		kHz
Feedback (FB) Voltage						
Range			450	600	672	mV

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical value is tested at T_J = 25°C, V_{IN} = 12V, min and max values at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback accuracy	V_{FB}		594	600	606	mV
Resolution		Per LSB		2		mV
Feedback voltage with margin high (7)	$V_{FB_MG_HIGH}$			672		mV
Feedback voltage with margin low (7)	$V_{FB_MG_LOW}$			450		mV
Soft Start and Turn On/Off Delay						
Soft-start time (8)	t_{SS}	61h, bits[2:0] = 3b'001		2		ms
Turn-on delay	t_{ON_DELAY}	60h, bits[7:0] = 0x00h		0		ms
Turn-off delay	t_{OFF_DELAY}	64h, bits[7:0] = 0x00h		0		ms
Error Amplifier (EA)						
Feedback current	I_{FB}	V_{FB} = V_{REF} (V_{FB} is the difference between VOSNS+ and VOSNS-)		50	100	nA
Soft Shutdown						
Soft shutdown discharge FET	R_{ON_DISCH}	Individual phase		60		Ω
Under-Voltage Lockout (UVLO)						
VCC UVLO rising threshold	VCC_{VTH}		2.6	2.75	2.9	V
VCC UVLO hysteresis	VCC_{HYS}			300		mV
Min input configurable turn-on voltage	$V_{IN_ON_MIN}$	V_{CC} = 3.3V	2.65	2.9	3.1	V
Max input configurable turn-on voltage	$V_{IN_ON_MAX}$		16	16.5	17	V
Min input configurable turn-off voltage	$V_{IN_OFF_MIN}$	V_{CC} = 3.3V		2.75		V
Max input configurable turn-off voltage	$V_{IN_OFF_MAX}$			15.75		V
Power Good (PG)						
PG high threshold	PG_{VTH_HI}	V_{FB} from low to high, D9h, bits[1:0] = 01		94%		V_{REF}
PG low threshold	PG_{VTH_LO}	V_{FB} from high to low, D9h, bits[3:2] = 10		79%		V_{REF}
PG low-to-high delay	t_{PGTD}	D1h, bits[5:2] = 0000		2		ms
PG sink current capability	V_{PG}	I_{PG} = 10mA			0.3	V
PG leakage current	I_{PG_LEAK}	V_{PG} = 3V		1.5		µA
PG low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PG up to 3.3V through a 100kΩ resistor, T_J = 25°C		600	720	mV
	V_{OL_10}	V_{IN} =0V, pull PG up to 3.3V through a 10kΩ resistor, T_J = 25°C		700	820	

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ELECTRICAL CHARACTERISTICS *(continued)*

Typical value is tested at T_J = 25°C, V_{IN} = 12V, min and max values at T_J = -40°C to +125°C (7), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Thermal Protection (TP)						
TP fault rising threshold (7)	T_{SD_RISE}	4Fh = 0x96h		150		°C
TP fault falling threshold (7)	T_{SD_FALL}	4Fh = 0x96h, D6h, bits[2:1] = 01		125		°C
TP warning rising threshold (7)	T_{WARN_RISE}	51h = 0082h		130		°C
TP warning falling threshold (7)	T_{WARN_FALL}	51h = 0082h, D6h, bits[2:1] = 01		105		°C
Min TP warning temperature (7)	$T_{SD_WARN_MIN}$			35		°C
Max TP warning temperature (7)	$T_{SD_WARN_MAX}$			160		°C
Monitoring Parameters						
Output voltage monitor accuracy (7)		V_{OUT} = 0.6V	0.588	0.6	0.612	V
Input voltage monitor accuracy			11.76	12	12.24	V
PMBus DC Characteristics (SDA, SCL, ALERT, CTRL) (7)						
Input high voltage	V_{IH}		2.1			V
Input low voltage	V_{IL}				0.8	V
Output low voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Input leakage current	I_{LEAK}	SDA, SCL, ALERT = 3.3V	-10		+10	µA
Maximum voltage (SDA, SCL, ALERT)	V_{MAX}	Transient voltage including ringing	-0.3	+3.3	+3.6	V
Pin capacitance on SDA,SCL	C_{PIN}				10	pF
PMBus Timing Characteristics (7)						
Min operating frequency				10		kHz
Max operating frequency				1000		kHz
Bus free time		Between a stop and start condition	4.7			µs
Holding time			4			µs
Repeated start condition set-up time			4.7			µs
Stop condition set-up time			4			µs
Data hold time			300			ns
Data set-up time			250			ns
Clock low timeout			25		35	ms
Clock low period			4.7			µs
Clock high period			4		50	µs
Clock/data falling time					300	ns
Clock/data rising time					1000	ns

Notes:

7) Guaranteed by sample characterization.
8) Guaranteed by sample characterization. Not tested in production. The parameter is tested during parameters characterization.

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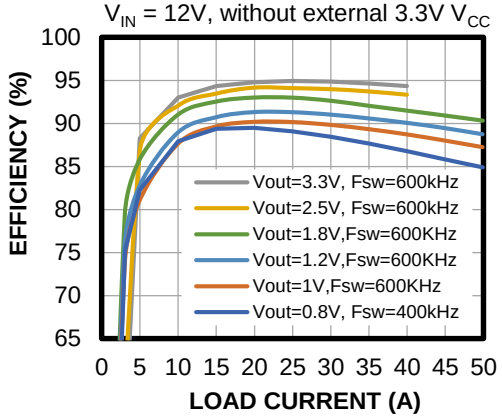
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz, C_{OUT} = 16 x 47µF + 2 x 220µF POSCAP, FCCM, T_A = 25°C, unless otherwise noted.

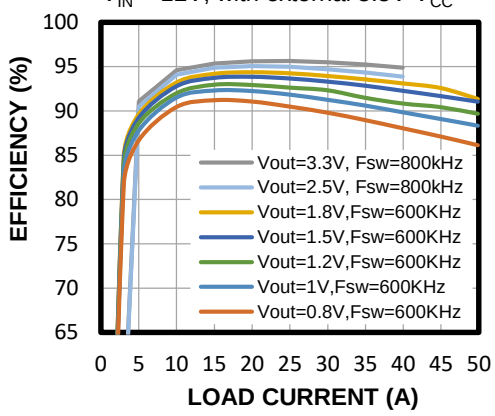
Efficiency vs. Load Current

V_{IN} = 12V, without external 3.3V V_{CC}

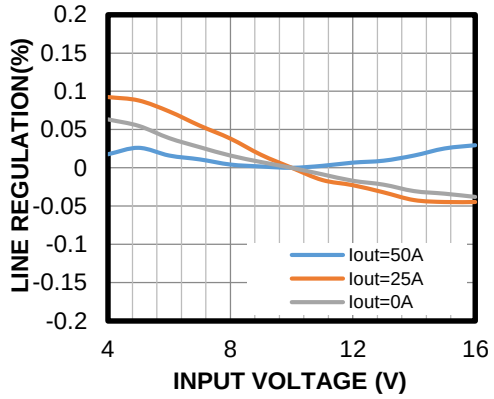


Efficiency vs. Load Current

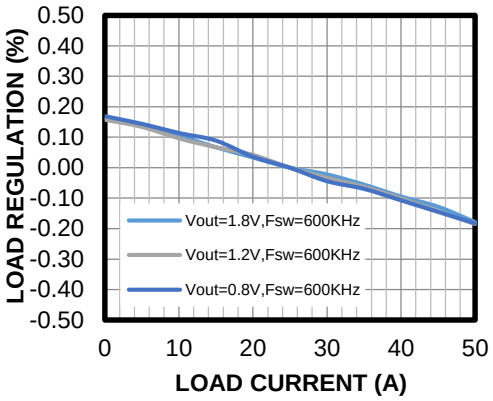
V_{IN} = 12V, with external 3.3V V_{CC}



Line Regulation

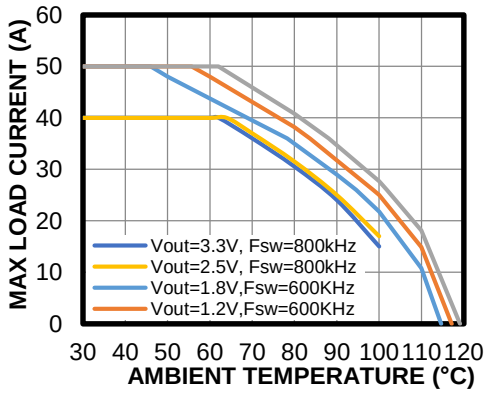


Load Regulation



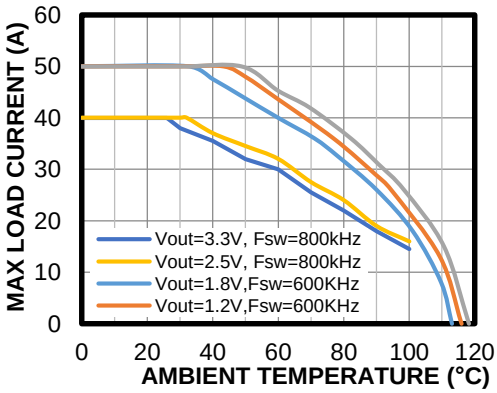
Thermal Derating

With airflow



Thermal Derating

No airflow



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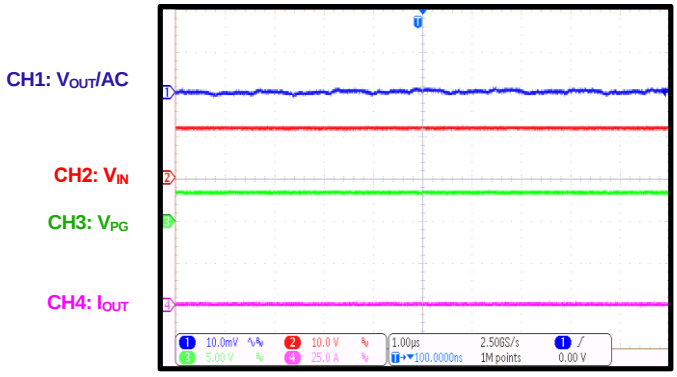
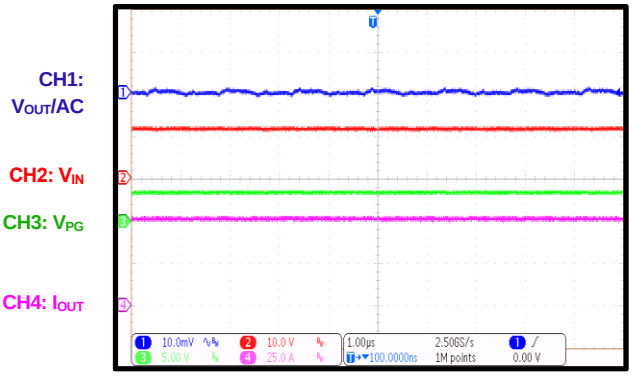
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz, C_{OUT} = 16 x 47µF + 2 x 220µF POSCAP, FCCM, T_A = 25°C, unless otherwise noted.

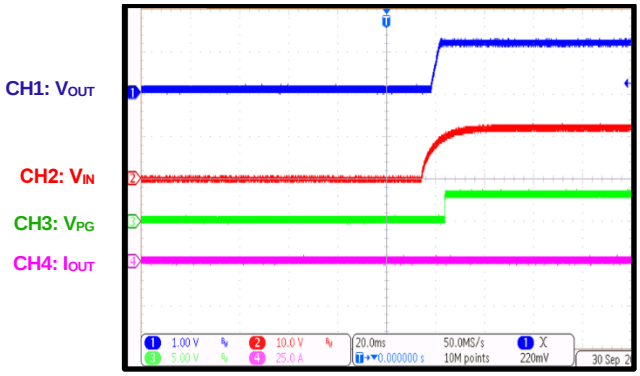
Output Voltage Ripple
I_{OUT} = 0A



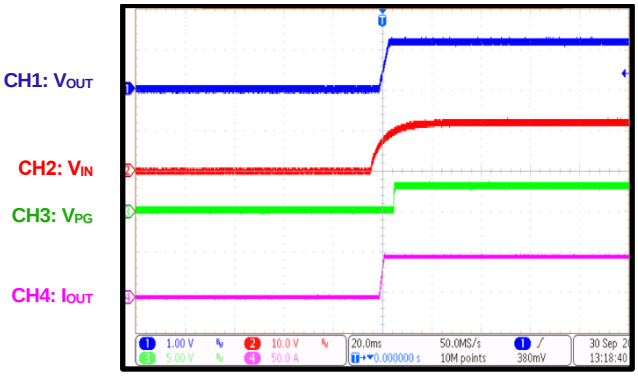
Output Voltage Ripple
I_{OUT} = 50A



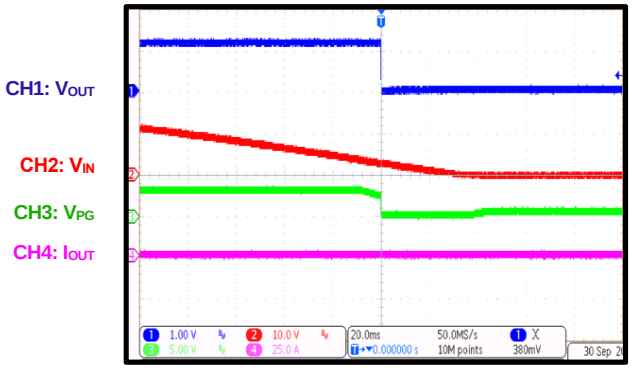
Start-Up through VIN
I_{OUT} = 0A



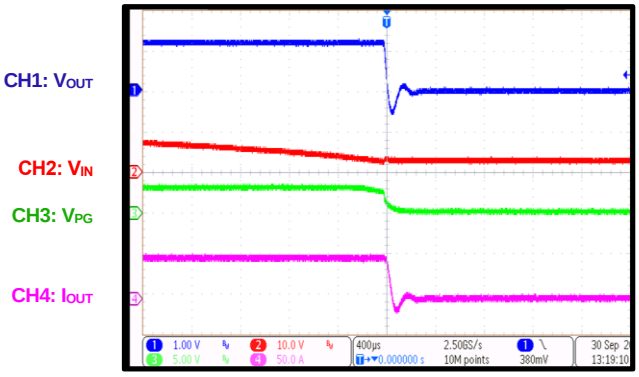
Start-Up through VIN
I_{OUT} = 50A



Shutdown through VIN
I_{OUT} = 0A



Shutdown through VIN
I_{OUT} = 50A



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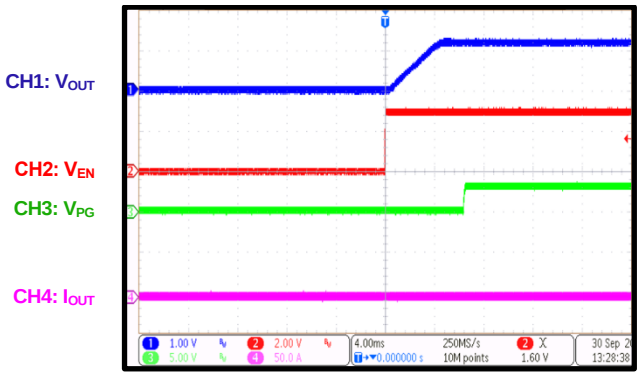
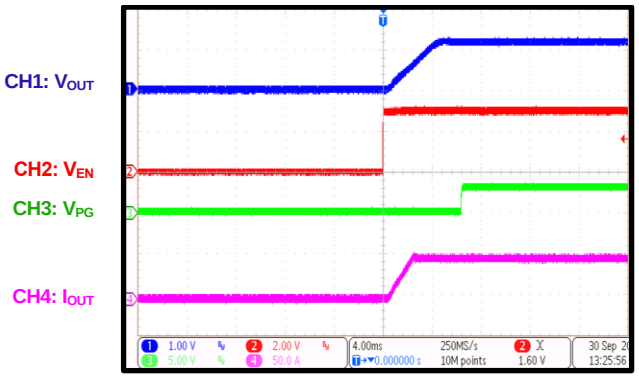
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz, C_{OUT} = 16 x 47µF + 2 x 220µF POSCAP, FCCM, T_A = 25°C, unless otherwise noted.

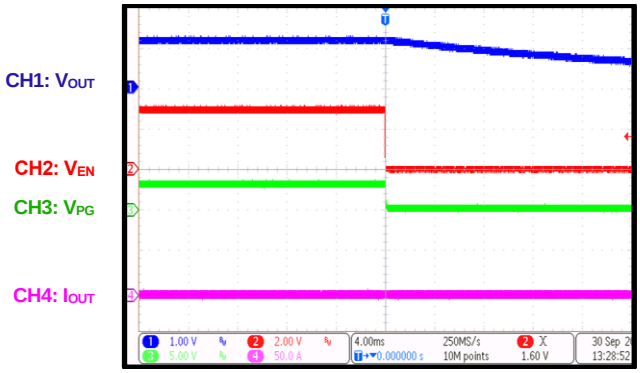
Start-Up through EN
I_{OUT} = 0A



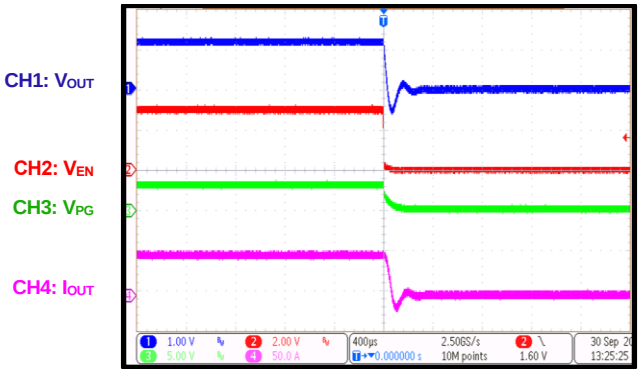
Start-Up through EN
I_{OUT} = 50A



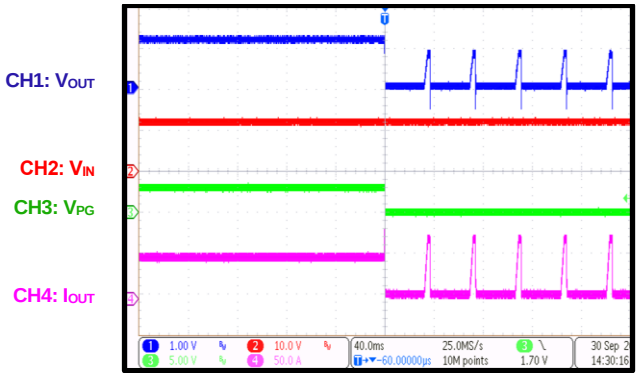
Shutdown through EN
I_{OUT} = 0A



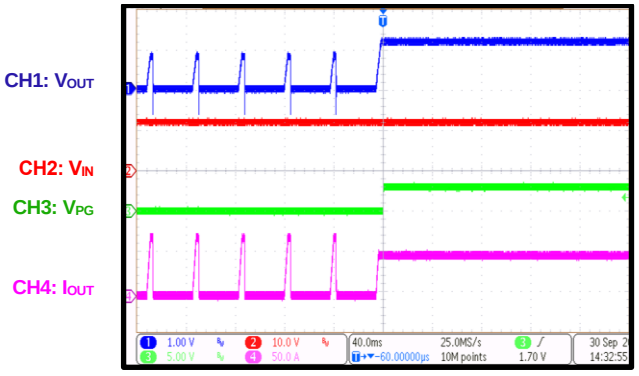
Shutdown through EN
I_{OUT} = 50A



SCP Entry
I_{OUT} = 50A



SCP Recovery
I_{OUT} = 50A



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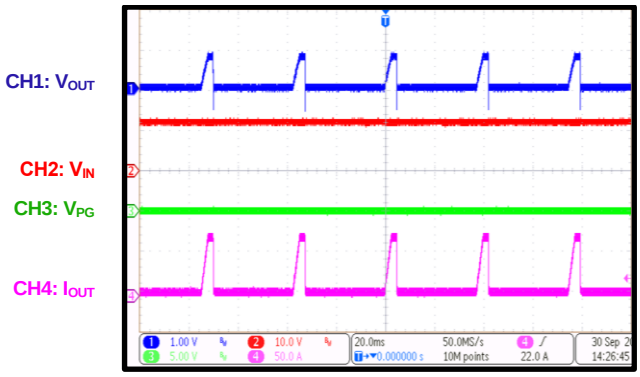
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

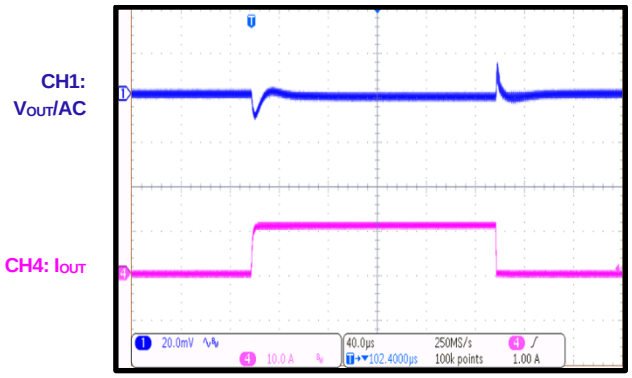
V_{IN} = 12V, V_{OUT} = 1.2V, f_{SW} = 600kHz, C_{OUT} = 16 x 47µF + 2 x 220µF POSCAP, FCCM, T_A = 25°C, unless otherwise noted.

SCP Steady State



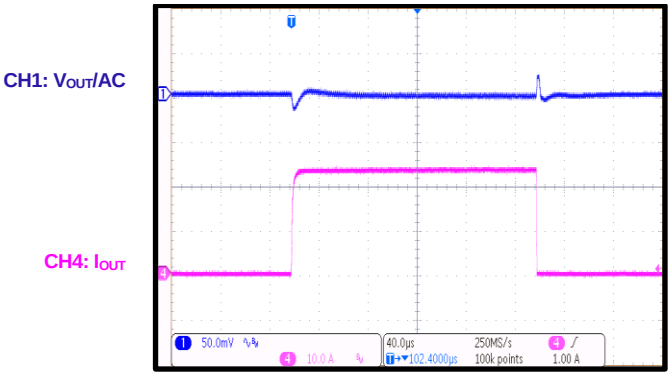
Load Transient Response

Load step = 0A to 12.5A, 10A/µs, ramp = 15mV



Load Transient Response

Load step = 0A to 25A, 10A/µs, ramp = 15mV



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FUNCTIONAL BLOCK DIAGRAM

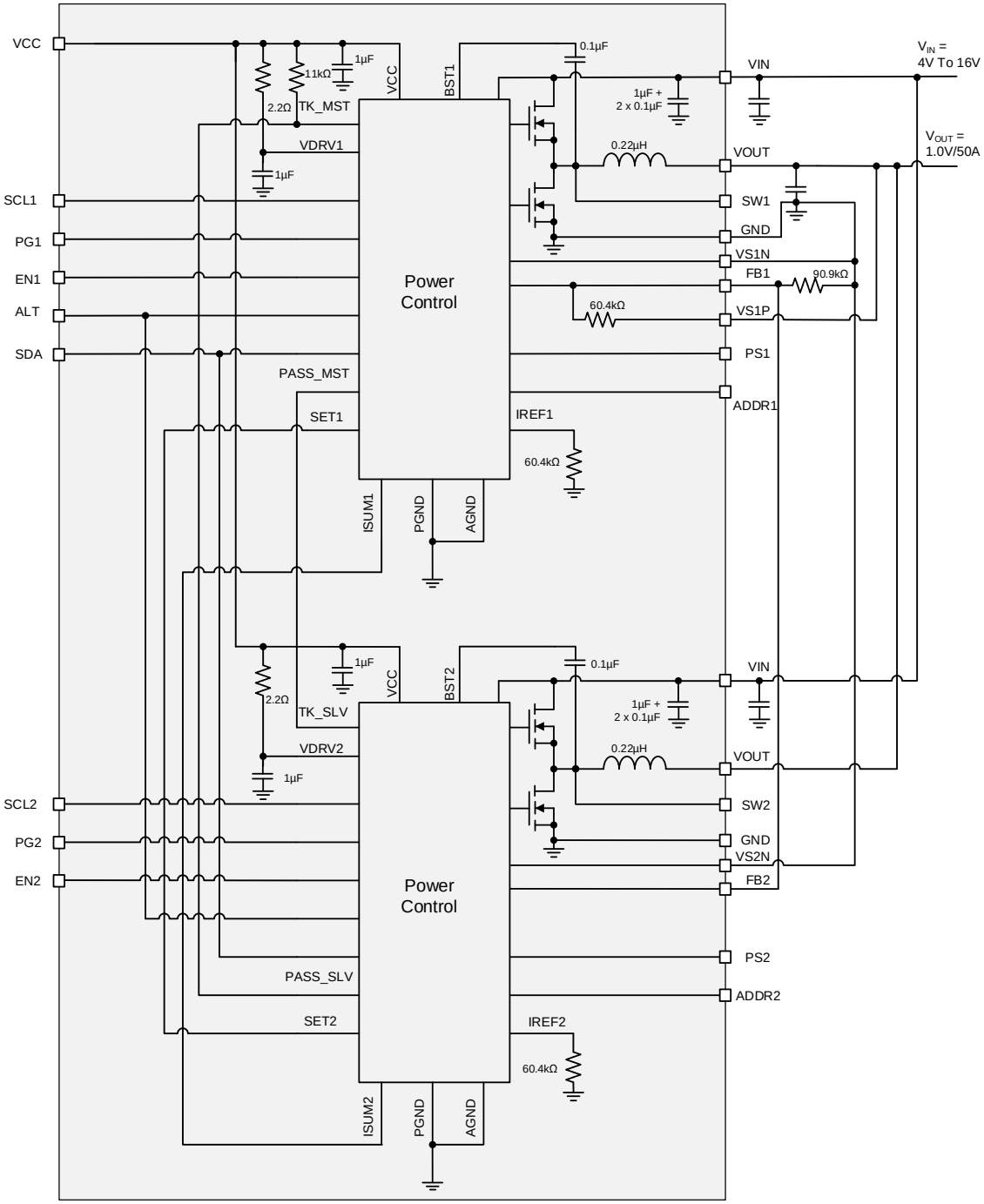

Figure 2: Functional Block Diagram

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OPERATION

Multi-Phase Constant-On-Time (MCOT) Operation

The MPM3690-50D is a fully integrated power module with up to 50A of continuous output current (I_{OUT}) on a BGA (16mmx16mmx5.18mm) package. The MPM3690-50D employs a constant-on-time control scheme to provide a fast transient response.

Multi-Phase Operation

The MPM3690-50D adopts multi-phase constant-on-time (MCOT) control. The control scheme configures the two ICs in the module for master and slave functionality.

MCOT Operation (Master)

The master phase performs the following functions:

- Accepts both write and read commands through the PMBus from a host.
- Generates the SET signals.
- Manages start-up, shutdown, and all protections.
- Monitors for any fault alerts from the slave phases through the PG pin.
- Starts the first on pulse.
- Starts the on pulse when receiving RUN and SET signals.
- Determines the on pulse width of its own phase based on the per-phase and total current.
- Sends the PASS/TAKE signal.

MCOT Operation (Slave)

The slave phase performs the following functions:

- Accepts write commands through the PMBus from a host.
- Takes the SET signal from the master.
- Sends over-voltage (OV), under-voltage (UV), and over-temperature (OT) alerts to the master through the PG pin.
- Starts the on pulse when receiving RUN and SET signals.
- Determines the on pulse width of its own phase based on the per-phase and total current.

MCOT control enables the MPM3690-50D to respond to a load step transient much faster than traditional current mode control schemes. When a load step occurs, the FB signal is below the internal reference; therefore, the SET signal is generated more frequently than it would be during steady state to respond to the load transient. Depending on the load transient step size and slew rate, the SET signal can be generated with a minimum 50ns interval (i.e. the next phase can be turned on as fast as 50ns after the previous phase to provide ultra-fast load transient response).

RAMP Compensation

The MPM3690-50D provides internal RAMP compensation to generate stable operation with zero-ESR ceramic output capacitors.

A triangular RAMP signal is generated internally, and is superimposed on the internal FB signal. This signal starts to rise once RAMP and the internal FB drop below the reference signal, and a SET pulse is generated. The RAMP signal's rising time is fixed. The RAMP compensation amplitude can be selected via register D0h, bits[3:1] to support a wide range of operation configurations.

There is a tradeoff between stability and load transient response. A larger RAMP signal provides higher stability but slower load transient response, and vice versa. Select the RAMP compensation value based on the target design for each application.

Mode Selection

The MPM3690-50D provides both forced continuous conduction mode (FCCM) and pulse-skip operation under light-load conditions. There are four available switching frequencies. The operation mode under light-load conditions and the switching frequency can be selected via the PMBus.

Soft Start (SS)

The soft-start time (t_{SS}) time can be set via register 61h. The minimum t_{SS} is 1ms, though it can also be set to 2ms, 4ms, 8ms, and 16ms.

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Output Voltage Discharge

When the MPM3690-50D is disabled through EN, it enables output voltage (V_{OUT}) discharge. Both the high-side MOSFET (HS-FET) and the low-side MOSFET (LS-FET) latch off. A discharge MOSFET connected between SW and GND turns on to discharge V_{OUT}. The typical on resistance of this MOSFET is about 60Ω. Once the FB voltage (V_{FB}) drops below 10% of the reference voltage (V_{REF}), the discharge MOSFET turns off.

Inductor Valley Over-Current Protection (OCP)

The MPM3690-50D features on-die current sensing and a configurable inductor valley current limit threshold. The inductor valley over-current (OC) limit can be configured via register D7h, which sets the per-phase inductor valley current limit for both single-phase and multi-phase operation. While the LS-FET is on, the inductor current is sensed and monitored cycle-by-cycle. The HS-FET can only turn on if an OC condition is not detected while the LS-FET is on.

The inductor current is limited cycle-by-cycle. If an OC condition is detected for 31 consecutive cycles, OCP is triggered. In addition, if V_{OUT} drops below the under-voltage protection (UVP) threshold, the MPM3690-50D enters OCP immediately.

Once OCP is triggered, the MPM3690-50D either enters hiccup mode or latch-off mode, depending on the register setting. After the MPM3690-50D latches off, power must be recycled on VCC or CTRL to re-enable the device.

Negative Inductor Current limit

When the LS-FET detects a negative current below the limit (-13A), the part turns off the LS-FET for a certain period of time to limit the negative current. This period is set via PMBus command D5h, bit[3].

Under-Voltage Protection (UVP)

The MPM3690-50D monitors V_{OUT} through the VOSNS+ pin and VOSNS- pin. UVP is triggered if V_{FB} drops below the UVP threshold. After UVP is triggered, the MPM3690-50D enters either hiccup mode or latch-off mode, depending on the register setting. After the MPM3690-50D latches off, power must be recycled on VCC or CTRL to re-enable the device.

Over-Voltage Protection (OVP)

Over-voltage protection (OVP) is triggered if V_{FB} exceeds the OVP threshold. See the MFR_OVP_NOCP_SET (D5h) section on page 37 for more details.

Over-Temperature Protection (OTP)

The MPM3690-50D provides over-temperature protection (OTP). The IC internally monitors the junction temperature. If the junction temperature exceeds the threshold, the converter shuts off.

After OTP is triggered, the device either enters hiccup mode or latches off. If the device latches off, cycle the power on VCC or EN to enable the part again.

Feedback (FB) Circuit

For the MPM3690-50D, connect a resistor between FB1 to VS1N to set V_{OUT} and tie FB1 to FB2. A 60.4kΩ resistor is connected between FB1 and VS1P. Figure 3 shows the block diagram for the feedback network.

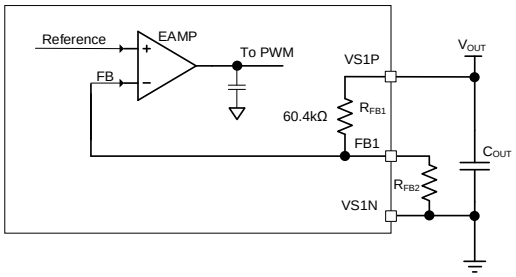

Figure 3: Feedback Circuit

V_{OUT} can be calculated with Equation (1):

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{FB1}}{R_{FB2}}) \quad (1)$$

Where V_{REF} is the reference voltage (0.6V), and R_{FB1} = 60.4kΩ.

Power Good (PG)

The MPM3690-50D has a power good (PG) output for each channel. The PG pin is the open drain of a MOSFET. Connect it to VCC or an external voltage source that is below 3.6V through a pull-up resistor (typically 100kΩ). After applying V_{IN}, the MOSFET turns on so that the PG pin is pulled to GND before soft start (SS) is ready. After V_{FB} reaches the threshold, the PG pin is pulled high after a delay. The delay can be

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selected via PMBus command MFR_CTRL_VOUT.

If the device encounters any fault (UVP, OVP, OTP, and UVLO), the PG pin latches low. After the PG pin latches low, it cannot be pulled high again until a new SS is initialized.

If the input supply fails to power the MPM3690-50D, the PG pin clamps low even though PG is tied to an external DC source through a pull-up resistor. Figure 4 shows the relationship between the PG voltage and the pull-up current.

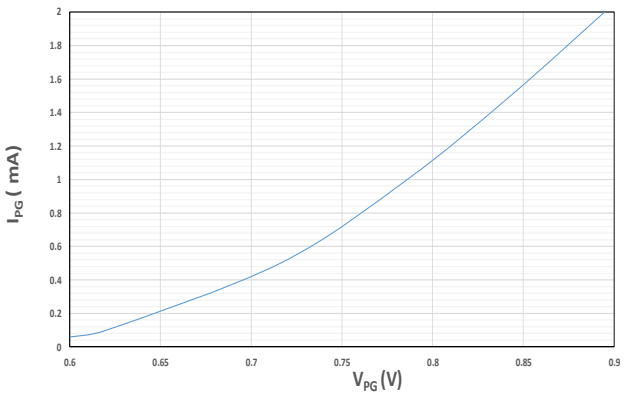

Figure 4: PG Current vs. PG Voltage

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PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open standard, power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional, serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled up to a bus voltage when they are in an idle state. When connecting to the lines, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPM3690-50D is a PMBus slave device that supports both standard mode (100kHz) and fast mode (400kHz and 1000KHz).

Slave Address

A unique address should be set for each slave device that is connected to the same PMBus. The ADDR pin configures the MPM3690-50D's address. There is a 10μA current flowing out of the ADDR pin. Connect a resistor between the ADDR pin and GND to set the ADDR voltage. The internal analog-to-digital converter (ADC) converts the pin voltage of the ADDR pin to set the PMBus address. A maximum of 16 addresses can be set by the ADDR pin. Table 2 shows the PMBus address for different resistors.

The MFR_ADDR_PMBUS (D3h) register can digitally set the PMBus address.

For multi-phase configurations, the slave phases can share the same address as the master, or they can have different addresses, depending on the application needs.

Table 2: PMBus Address vs. ADDR Resistor

R_{ADDR} (kΩ)	Slave Address
2.49	30h
7.5	31h
12.4	32h
17.4	33h
22.6	34h
27.4	35h
32.4	36h
37.4	37h
42.2	38h
47.5	39h
100	3Fh

The slave phases can only accept write commands, and they cannot accept read commands from the PMBus master. The master phase can accept both write and read commands from the PMBus master.

Start and Stop Commands

The start and stop commands are signaled by the master device, which signifies the beginning and the end of the PMBus transfer. The start command is defined as the SDA signal transitioning from high to low while the SCL line is high. The stop command is defined as the SDA signal transitioning from low to high while the SCL line is high (see Figure).

The master generates the SCL clocks, and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

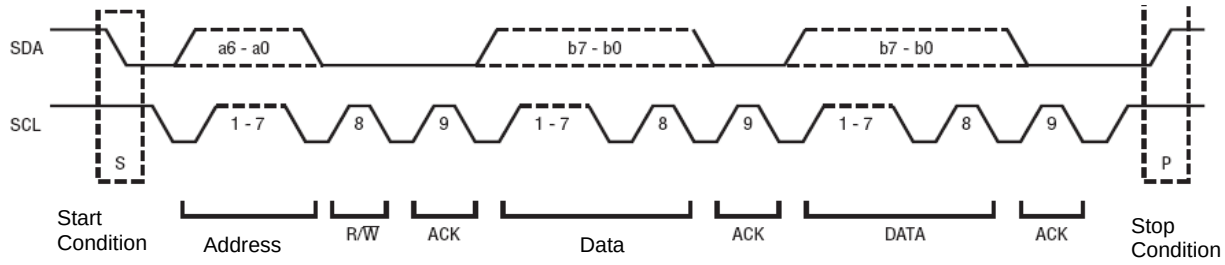

Figure 5: Data Transfer Across the PMBus

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PMBus Update Sequence

The MPM3690-50D requires a start command, a valid PMBus address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPM3690-50D acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPM3690-50D. The MPM3690-50D performs an update on the falling edge of the LSB byte.

Protocol Usage

All PMBus transactions on the MPM3690-50D are done using defined bus protocols. The following protocols are implemented:

- Send byte with PEC
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC
- Block read with PEC

PMBus Bus Message Format

Figure 6 on page 21 shows the PMBus message format. Unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the MPM3690-50D is driving the bus. The symbols for Figure 6 are defined below:

- S = start condition
- Sr = repeated start condition
- P = stop condition
- R = read bit
- $\overline{W}$ = write bit
- A = acknowledge bit (0)
- $\overline{A}$ = acknowledge bit (1)

A represents the ACK bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is logic 1, indicated by $\overline{A}$.

Packet Error Checking (PEC)

The MPM3690-50D PMBus interface supports the use of the packet error checking (PEC) byte. The PEC byte is transmitted by the MPM3690-50D during a read transaction or sent by the bus host to the MPM3690-50D during a write transaction.

The PEC byte is used by the bus host or the MPM3690-50D to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the MPM3690-50D determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag. Within a group command, the host can choose whether to send a PEC byte as part of the message to the MPM3690-50D.

PMBus Alert Response Address (ARA)

The PMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices that needs to communicate. A host typically uses a hardware interrupt pin to monitor the PMBus ALERT pins of a number of devices. When the host interrupt occurs, the host issues a message on the bus using the PMBus receive byte or receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have a PMBus alert signal return their own 7-bit address as the 7MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active PMBus alert signal, and attempt to communicate with the host. In this scenario, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus alert signal. If the host sees that the PMBus alert signal is still low, it continues to read addresses until all devices that need to communicate have successfully transmitted their addresses.

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a) Send Byte and Send Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	PEC	A	P

b) Receive Byte and Receive Byte with PEC

1	7	1	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	8	1	1
S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

c) Write Byte and Write Byte with PEC

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	PEC	A	P

d) Write Word and Write Word with PEC

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

1	7	1	1	8	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	PEC	A	P

e) Read Byte and Read Byte with PEC

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	P

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	PEC	A	P

f) Read Word and Read Word with PEC

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	A	P

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	8	1	1
Data Byte High	A	PEC	A	P

g) Block Read with PEC

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count = N	A	...

8	1	8	1	...	8	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	P

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Byte Count = N	A	...

8	1	8	1	...	8	1	8	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	PEC	A	P

Figure 6: PMBus Message Format

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Data and Numerical Formats

The MPM3690-50D uses a direct format internally to represent real-world values such as voltage, current, power, and temperature.

All numbers with no suffix in this document are decimals, unless explicitly designated otherwise.

Numbers in binary format are indicated by the prefix “n’b”, where n is the binary count. For example, 5’b01010 indicates a 5-bit binary data. And the data is 01010.

The suffix “h” indicates a hexadecimal format, which is generally used for the register address number in this document.

The symbol “0x” indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number whose hexadecimal value is A3.

PMBus Communication Failure

A data transmission fault occurs when the data is not properly transferred between the devices. There are several data transmission faults as listed below:

- Sending too little data
- Reading too little data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

PMBus Reporting and Status Monitoring

The MPM3690-50D supports real-time monitoring for certain operation parameters and statuses via the PMBus interface (see Table 3).

Table 3: PMBus Monitored Parameters and Statuses

Parameter/Status	PMBus
V_{OUT}	1.25mV/LSB
I_{OUT}	31.25mA/62.5mA/LSB
Temperature	1°C/LSB
V_{IN}	25mV/LSB
V_{IN} over-voltage (OV)	✓
V_{IN} under-voltage (UV)	✓
V_{IN} OV warning	✓
V_{IN} UV warning	✓
V_{OUT} OV	✓
V_{OUT} UV	✓
Over-temperature (OT)	✓
OT warning	✓
V_{OUT} over-current (OC)	✓
V_{OUT} OC warning	✓

MTP Configurations

The MPM3690-50D has built-in multiple-time programmable (MTP) memory to store the user configurations. The standard command STORE_USER_ALL (15h) is not supported by this device. The MTP can be configured through the following command combination:

- E7h (2000h)
- E7h (1000h)
- E7h (4000h)

For the MPM3690-50D’s GUI, the above commands are integrated and named (STORE_USER_ALL (15h). This means that the MPS GUI supports a 15h command.

When the MTP is being configure, the VCC voltage (V_{CC}) may be as high as 5V. Exercise caution if VCC is connected to circuits that cannot support such a high voltage. There must be a time delay (about 1s) between two commands.

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REGISTER MAP

Code	Name	Type	Bytes	Default Value	MTP?
01h	OPERATION	R/W w/ PEC	1	0x80	Yes
02h	ON_OFF_CONFIG	R/W w/ PEC	1	0x1e	Yes
03h	CLEAR_FAULTS	Send byte w/ PEC	0	-	-
10h	WRITE_PROTECT	R/W w/ PEC	1	0x00	Yes
15h	STORE_USER_ALL	Send byte w/ PEC	0	-	-
16h	RESTORE_USER_ALL	Send byte w/ PEC	0	-	-
19h	CAPABILITY	R w/ PEC	1	0xB0	-
20h	VOUT_MODE	R w/ PEC	1	0x40	-
21h	VOUT_COMMAND	R/W w/ PEC	2	0x0258 (1.2V)	Yes
24h	VOUT_MAX	R/W w/ PEC	2	0x0BB8 (6V)	Yes
25h	VOUT_MARGIN_HIGH	R/W w/ PEC	2	0x02A0 (1.344V)	Yes
26h	VOUT_MARGIN_LOW	R/W w/ PEC	2	0x0200 (1.024V)	Yes
29h	VOUT_SCALE_LOOP	R/W w/ PEC	2	0x01F4 (0.5)	Yes
2Bh	VOUT_MIN	R/W w/ PEC	2	0x00FA (0.5V)	Yes
35h	VIN_ON	R/W w/ PEC	2	0x0010 (4V)	Yes
36h	VIN_OFF	R/W w/ PEC	2	0x000B (2.75V)	Yes
4Fh	OT_FAULT_LIMIT	R/W w/ PEC	2	0x00A0 (160°C)	Yes
51h	OT_WARN_LIMIT	R/W w/ PEC	2	0x008C (140°C)	Yes
55h	VIN_OV_FAULT_LIMIT	R/W w/ PEC	2	0x0024 (18V)	Yes
57h	VIN_OV_WARN_LIMIT	R/W w/ PEC	2	0x0020 (16V)	Yes
58h	VIN_UV_WARN_LIMIT	R/W w/ PEC	2	0x0001 (0.25V)	Yes
60h	TON_DELAY	R/W w/ PEC	2	0x0000 (0ms)	Yes
61h	TON_RISE	R/W w/ PEC	2	0x0002 (4ms)	Yes
64h	TOFF_DELAY	R/W w/ PEC	2	0x0000 (0ms)	Yes
78h	STATUS_BYTE	R w/ PEC	1	-	-
79h	STATUS_WORD	R w/ PEC	2	-	-
7Ah	STATUS_VOUT	R w/ PEC	1	-	-
7Bh	STATUS_IOUT	R w/ PEC	1	-	-
7Ch	STATUS_INPUT	R w/ PEC	1	-	-
7Dh	STATUS_TEMPERATURE	R w/ PEC	1	-	-
7Eh	STATUS_CML	R w/ PEC	1	-	-
88h	READ_VIN	R w/ PEC	2	-	-
8Bh	READ_VOUT	R w/ PEC	2	-	-
8Ch	READ_IOUT	R w/ PEC	2	-	-
8Dh	READ_TEMPERATURE_1	R w/ PEC	2	-	-

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REGISTER MAP *(continued)*

Code	Name	Type	Bytes	Default Value	MTP?
D0h	MFR_CTRL_COMP	R/W w/ PEC	1	0x0D	Yes
D1h	MFR_CTRL_VOUT	R/W w/ PEC	1	0x00	Yes
D2h	MFR_CTRL_OPS	R/W w/ PEC	1	0x03	Yes
D3h	MFR_ADDR_PMBUS	R/W w/ PEC	1	0x30	Yes
D4h	MFR_VOUT_FAULT_LIMIT	R/W w/ PEC	1	0x03	Yes
D5h	MFR_OVP_NOCP_SET	R/W w/ PEC	1	0x02	Yes
D6h	MFR_OT_OC_SET	R/W w/ PEC	1	0x09	Yes
D7h	MFR_OC_PHASE_LIMIT	R/W w/ PEC	1	0x11 (51A total, 25.5A per phase)	Yes
D9h	MFR_PGOOD_ON_OFF_LIMIT	R/W w/ PEC	1	0x00	Yes
DAh	MFR_VOUT_STEP	R/W w/ PEC	1	0x04	Yes
EAh	MFR_CTRL	R/W w/ PEC	2	0x08	Yes

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REGISTER DESCRIPTION

OPERATION (01h)

Format: Unsigned binary

The OPERATION command is a paged register. It turns the converter output on/off in conjunction with input from the CTRL pin, sets the output voltage to the upper or lower margin voltages. The device stays in the commanded operating mode until a subsequent OPERATION command is received, or a change in the state of the CTRL pin instructs the converter to change to another mode. This command also re-enables the converter after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown does not clear any fault registers.

Bits	Access	Bit Name	Description
7:2	R/W	OPERATION	Selects the operation mode. 6’b 00xx xx: Hi-Z shutdown 6’b 01xx xx: Soft shutdown 6’b 1000 xx: Normal on 6’b 1001 01: Margin low (ignore fault) 6’b 1001 10: Margin low (act on fault) 6’b 1010 01: Margin high (ignore fault) 6’b 1010 10: Margin high (act on fault) “x” means not applicable.
1:0	R	RESERVED	Reserved.

ON_OFF_CONFIG (02h)

Format: Unsigned binary

The ON_OFF_CONFIG command configures the combination of the CTRL pin input and the PMBus commands that are required to turn the converter on and off. This includes how the converter responds when V_{IN} is applied.

Bits	Access	Bit Name	Description
7:5	R	RESERVED	Reserved.
4	R/W	PON	1’b0: The converter turns on any time V_{IN} is present, regardless of state of the CTRL pin 1’b1: The converter does not turn on until commanded by the CTRL pin and OPERATION command
3	R/W	OP	1’b0: The converter ignores the “on” bit in the OPERATION command from the PMBus 1’b1: The converter responds to the “on” bit in the OPERATION command from the PMBus
2	R/W	EN	1’b0: The converter ignores the CTRL pin (on/off controlled only by the OPERATION command) 1’b1: The converter requires CTRL pin assertion to power up. Depending on the bit[3] of this command, the OPERATION command may also be required to instruct the converter to start up
1	R/W	POL	This function is disabled. 1’b0: Active low (pull the CTRL pin low to start the converter) 1’b1: Active high (pull the CTRL pin high to start the converter)
0	R	DLY	Reserved.

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CLEAR_FAULTS (03h)

The CLEAR_FAULTS command resets all stored warning and fault flags. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the ALT# signal may not be cleared, or it re-asserts almost immediately. Issuing a CLEAR_FAULTS command does not cause the converter to restart in the event of a fault-related shutdown. Instead, an OPERATION command must be issued after the fault condition is cleared. This command uses the PMBus to send a byte protocol.

WRITE_PROTECT (10h)

The WRITE_PROTECT command controls writing to the converter. The intent of this command is to provide protection against accident changes. It is not intended to provide protection against deliberate changes to the converter's configuration or operation. All the supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

Bits	Access	Bit Name	Description
7:5	R/W	WRITE_PROTECT	3'b 000: Enable writes to all commands 3'b 001: Disable all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands 3'b 010: Disable all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands 3'b 100: Disable all writes except to the WRITE_PROTECT command
4:0	R	RESERVED	Reserved.

STORE_USER_ALL (15h)

The STORE_USER_ALL command writes all the data from the registers to the internal MTPs. This process operates when the MPM3690-50D receives a STORE_USER_ALL command from the PMBus interface. Currently, the MPM3690-50D does not support the standard 15h command. However, it can accept a 15h command from the MPS GUI. See the MTP Configurations section on page 22 for additional details. Table 4 shows the registers that can be stored in STORE_USER_ALL.

Table 4: Registers Stored in STORE_USER_ALL

Registers Stored in STORE_USER_ALL	
OPERATION (01h)	VIN_UV_WARN_LIMIT (58h)
ON_OFF_CONFIG (02h)	TON_DELAY (60h)
WRITE_PROTECT (10h)	TON_RISE (61h)
VOUT_COMMAND (21h)	TOFF_DELAY (64h)
VOUT_MAX (24h)	MFR_CTRL_COMP (D0h)
VOUT_MARGIN_HIGH (25h)	MFR_CTRL_VOUT (D1h)
VOUT_MARGIN_LOW (26h)	MFR_CTRL_OPS (D2h)
VOUT_SCALE_LOOP (29h)	MFR_ADDR_PMBUS (D3h)
VOUT_MIN (2Bh)	MFR_VOUT_FAULT_LIMIT (D4h)
VIN_ON (35h)	MFR_OVP_NOCP_SET (D5h)
VIN_OFF (36h)	MFR_OT_OC_SET (D6h)
OT_FAULT_LIMIT (4Fh)	MFR_OC_PHASE_LIMIT (D7h)
OT_WARN_LIMIT (51h)	MFR_PGOOD_ON_OFF (D9h)
VIN_OV_FAULT_LIMIT (55h)	MFR_VOUT_STEP (DAh)
VIN_OV_WARN_LIMIT (57h)	MFR_CTRL (EAh)

RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the MPM3690-50D to copy all content of the MTP values to the matching locations in the registers. The values in the registers are overwritten by the value retrieved from the MTP. Any items in the MTPs that do not have matching locations in the operating memory are ignored.

The RESTORE_USER_ALL command can be used while the device operates. The RESTORE_USER_ALL command can be used, but the MPM3690-50D may respond to the copying

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operation with unpredictable or dangerous results.

This command is write-only.

CAPABILITY (19h)

Format: Unsigned binary

The CAPABILITY command returns information about the PMBus functions supported by the MPM3690-50D. This command can be read with the PMBus read byte protocol.

Bits	Access	Bit Name	Description
7	R	PEC	1'b1: PEC is supported
6:5	R	MAXIMUM_BUS_ SPEED	2'b 00: The maximum supported bus speed is 100kHz 2'b 01: The maximum supported bus speed is 1MHz 2'b 10: The maximum supported bus speed is 400kHz 2'b 11: Reserved
4:0	R	RESERVED	Reserved.

VOUT_MODE (20h)

The VOUT_MODE command sets and reads the output voltage. The 3 most significant bits are used to determine the data format (only a direct format is supported by the MPM3690-50D), and the remaining 5 bits represent the exponent used in the output voltage read/write commands.

VOUT_COMMAND (21h)

Format: Direct

The VOUT_COMMAND sets V_{OUT}. The VOUT_COMMAND and the VOUT_SCALE_LOOP determine the feedback reference voltage (VOUT_COMMAND x VOUT_SCALE_LOOP).

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Reserved.
11:0	R/W	VOUT_COMMAND	12'b: 2mV/LSB

The value is unsigned and 1LSB = 2mV.

The V_{OUT} command accuracy is 2mV/K, where K is the SCALE_LOOP value. The default value is 1.2V.

VOUT_MAX (24h)

Format: Direct

The VOUT_MAX command sets an upper limit on the V_{OUT} that the converter can command, regardless of any other commands or combinations. This command provides a safeguard against a user accidentally setting V_{OUT} to a possibly destructive level. It is not the primary output over-voltage protection (OVP).

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Reserved.
11:0	R/W	VOUT_MAX	12'b: 2mV/LSB

If an attempt is made to configure V_{OUT} above the limit set by this command, the device responds in the following way:

- The commanded output voltage is set to VOUT_MAX.
- The V_{OUT} bit is set in STATUS_WORD.
- The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register.
- The device notifies the host.

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The value is unsigned and 1LSB = 2mV. The maximum value for VOUT_MAX is 6V, and the default value is 6V.

VOUT_MARGIN_HIGH (25h)

Format: Direct

The VOUT_MARGIN_HIGH command sets the voltage unit to which the output changes when the OPERATION command is set to margin high.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Reserved.
11:0	R/W	VOUT_MARGIN_HIGH	12'b: 2mV/LSB

The value is unsigned and 1LSB = 2mV.

VOUT_MARGIN_LOW (26h)

Format: Direct

The VOUT_MARGIN_LOW command sets the voltage unit to which the output changes when the OPERATION command is set to margin low.

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Reserved.
11:0	R/W	VOUT_MARGIN_LOW	12'b: 2mV/LSB

The value is unsigned and 1LSB = 2mV.

VOUT_SCALE_LOOP (29h)

Format: Direct

The VOUT_SCALE_LOOP command sets the feedback resistor divider ratio, which equals V_{FB} / V_{OUT}. Regardless of the external or internal feedback resistor divider, VOUT_SCALE_LOOP should match the value of the actual feedback resistor divider.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Reserved.
9:0	R/W	VOUT_MAX	10'b: 0.001/LSB

The value is unsigned and 1LSB = 0.001. The default value is 0.5.

VOUT_MIN (2Bh)

Format: Direct

The VOUT_MIN command sets a lower limit on the V_{OUT} that the converter can command, regardless of any other commands or combinations. This command provides a safeguard against a user accidentally setting V_{OUT} to a possibly destructive level. It is not the primary output over-voltage protection (OVP).

Bits	Access	Bit Name	Description
15:12	R	RESERVED	Reserved.
11:0	R/W	VOUT_MIN	12'b: 2mV/LSB

If an attempt is made to configure V_{OUT} below the limit set by this command, the device responds in the following way:

- The commanded V_{OUT} is set to VOUT_MIN.
- The V_{OUT} bit is set in STATUS_WORD.
- The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register.

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- The device notifies the host.

The minimum value of VOUT_MIN is 0.5V. The value is unsigned and 1LSB = 2mV. The default value is 0.5V.

VIN_ON (35h)

Format: Direct

The VIN_ON command sets the value of V_{IN} (in V) at which the converter should turn on, if all other required start-up conditions are met. VIN_ON should always be set above VIN_OFF, with a sufficient margin so that there is no bouncing between VIN_ON and VIN_OFF during power conversion.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	Reserved.
5:0	R/W	VOUT_ON	6'b: 250mV/LSB

The value is unsigned and 1LSB = 250mV. The default value is 4V.

VIN_OFF (36h)

Format: Direct

The VIN_OFF command sets the value of V_{IN} (in V) at which the converter should shut down once operation has started. VIN_OFF can be set between 2.75V and 14.75V, with a 0.25V increment. VIN_OFF should always be below VIN_ON with enough margin, with a sufficient margin so that there is no bouncing between VIN_ON and VIN_OFF during power conversion.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	Reserved.
5:0	R/W	VOUT_OFF	6'b: 250mV/LSB

The value is unsigned and 1LSB = 250mV. The default value is 2.75V.

OT_FAULT_LIMIT (4Fh)

Format: Direct

The OT_FAULT_LIMIT command configures or reads the threshold for over-temperature (OT) fault detection. If the measured temperature exceeds this value, an OT fault is triggered. The MPM3690-50D's response depends on the MFR_OT_OC_SET (D6h) register. Meanwhile, the OT fault flags are set in the STATUS BYTE (78h) and STATUS_WORD (79h) registers, and the ALT# signal asserts.

Once the measured temperature falls below the value in this register, the converter turns back on with the OPERATION command when the part works in latch-off mode. The minimum temperature fault detection time should be shorter than 20ms. The temperature ranges between 0°C and 255°C.

In retry mode, the device automatically retries when the temperature drops 20°C below (set by register D6h) the value set by OT_FAULT_LIMIT.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Reserved.
7:0	R/W	VOUT_ON	8'b: 1°C/LSB

The value is unsigned and 1LSB = 1°C. The default value is 00A0h, which corresponds to 160°C.

The OT_FAULT_LIMIT setting value should be below 160°C. If OT_FAULT_LIMIT exceeds 160°C, the register value is ignored, and the MPM3690-50D initiates thermal shutdown when the junction temperature reaches 160°C. Table 5 on page 30 shows the relationship between the direct value and the real-word value.

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Table 5: OT_FAULT_TIME

Direct Value	Real-World Value (°C)
0000 0000	0
0000 0001	1
1111 1111	255

OT_WARN_LIMIT (51h)

Format: Direct

The OT_WARN_LIMIT command configures or reads the threshold for the OT warning detection. If the sensed temperature exceeds this value, an OT warning is triggered, the OT warning flags are set in the STATUS BYTE (78h) and STATUS_WORD (79h) registers, and the ALT# signal asserts. The minimum temperature warning detection time should be shorter than 20ms.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Reserved.
7:0	R/W	VOUT_ON	8'b: 1°C /LSB

The value is unsigned and 1LSB = 1°C. The default value is 008Ch, which corresponds with 140°C. The OT_WARN_LIMIT setting value should be below 160°C. The relationship between the direct value and the real-word value are the same as OT_FAULT_LIMIT.

VIN_OV_FAULT_LIMIT (55h)

Format: Direct

The VIN_OV_FAULT_LIMIT command configures or reads the threshold for V_{IN} over-voltage (OV) fault detection. If the measured value of V_{IN} rises above the value in this register, the V_{IN} OV fault flags are set in the respective registers. Meanwhile, the MPM3690-50D's power stage is disabled. When V_{IN} drops below VIN_OV_FAULT_LIMIT, the MPM3690-50D is re-enabled.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	Reserved.
5:0	R/W	VIN_OV_FAULT_LIMIT	6'b: 500mV/LSB

The value is unsigned and 1LSB = 500mV. The default value is 24h, which corresponds with 18V.

The set VIN_OV_FAULT_LIMIT value should not exceed 18V.

VIN_OV_WARN_LIMIT (57h)

Format: Direct

The VIN_OV_WARN_LIMIT command configures or reads the threshold for V_{IN} OV warning detection. If the measured value of V_{IN} exceeds the value in this register, the V_{IN} OV warning flags are set in the respective registers, and the ALT# signal asserts.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	Reserved.
5:0	R/W	VIN_OV_WARN_LIMIT	6'b: 500mV/LSB

The value is unsigned and 1LSB = 500mV. The default value is 20h, which corresponds with 16V.

The set VIN_OV_WARN_LIMIT value should not exceed 18V.

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VIN_UV_WARN_LIMIT (58h)

Format: Direct

The VIN_UV_WARN_LIMIT command configures or reads the threshold for V_{IN} under-voltage (UV) fault detection. If the measured value of V_{IN} falls below the value in this register, the V_{IN} UV warning flags are set in the respective registers, and the ALT# signal asserts.

Bits	Access	Bit Name	Description
15:6	R	RESERVED	Reserved.
5:0	R/W	VIN_UV_WARN_LIMIT	6'b: 250mV/LSB

The value is unsigned and 1LSB = 250mV. The default value is 01h. The set VIN_UV_WARN_LIMIT value should not exceed 3.3V.

TON_DELAY (60h)

Format: Direct

The TON_DELAY command sets the time (in ms) from when a start condition is received (as configured by the ON_OFF_CONFIG command) until V_{OUT} starts to rise.

Bits	Access	Bit Name	Description
15:8	R	RESERVED	Reserved.
7:0	R/W	TON_DELAY	8'b: 4ms/LSB

The value is unsigned and 1LSB = 4ms. The maximum value is 60h = FFh (1020ms). The default value is 0ms.

TON_RISE (61h)

Format: Direct

The TON_RISE command sets the soft-start time (t_{SS}, in ms) from when the output starts to rise until the voltage has reached the regulation point.

Bits	Access	Bit Name	Description
15:3	R	RESERVED	Reserved.
2:0	R/W	TON_RISE	3'b 000: 1ms 3'b 001: 2ms 3'b 010: 4ms 3'b 011: 8ms 3'b 100 and up: 16ms

The default value for t_{SS} is 02h (4ms).

STATUS BYTE (78h)

The STATUS_BYTE command returns the value of a number of flags indicating the state of the MPM3690-50D. Access to this command should use the read byte protocol. To clear the bits in this register, the underlying fault should be removed, and a CLEAR_FAULTS command should be issued.

Bits	Name	Behavior	Default	Description
7	RESERVED	N/A	0	Always read as 0
6	OFF	R (Live)	0	1'b 0: Part enabled 1'b 1: Part disabled. This can be triggered from a V_{IN} under-voltage (UV) or over-voltage (OV) fault, or an OPERATION off command
5	VOUT_OV	R (Latched)	0	1'b 0: No output OV fault has occurred 1'b 1: An output OV fault has occurred

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4	IOUT_OC_FAULT	R (Latched)	0	1'b 0: No over-current (OC) fault has been detected 1'b 1: An OC fault has been detected
3	VIN_UV	R (Latched)	0	1'b 0: No V_{IN} UV fault has been detected 1'b 1: A V_{IN} UV fault has been detected
2	OT_FAULT_WARN	R (Latched)	0	1'b 0: No over-temperature (OT) warning or fault has been detected 1'b 1: An OT warning or fault has been detected
1	CUMM_ERROR	R (Latched)	0	1'b 0: No communication error has been detected 1'b 1: A communication error has been detected
0	NONE_OF_THE_ ABOVE	R (Latched)	0	1'b 0: No other fault or warning has occurred 1'b 1: A fault or warning not listed in bits[7:1] has occurred

STATUS_WORD (79h)

The STATUS_WORD command returns the value of a number of flags indicating the state of the MPM3690-50D. To clear the bits in this register, the underlying fault should be removed, and a CLEAR_FAULTS command should be issued.

Bits	Name	Behavior	Default	Description
15	VOUT_STATUS	R (Latched)	0	1'b 0: No output fault or warning has occurred 1'b 1: An output fault or warning has occurred
14	IOUT_STATUS	R (Latched)	0	1'b 0: No I_{OUT} fault has occurred 1'b 1: An I_{OUT} fault has occurred
13	VIN_STATUS	R (Latched)	0	1'b 0: No V_{IN} fault has occurred 1'b 1: A V_{IN} fault has occurred. When V_{IN} starts up, the initial flag is set to 1 before V_{IN} reaches the under-voltage lockout (UVLO) threshold. It clears once V_{IN} reaches the UVLO threshold
12	MFR_STATUS	R	0	Always read as 0.
11	POWER_GOOD#	R (Live)	0	1'b 0: The power good signal is asserted 1'b 1: No power good signal is asserted
10	RESERVED	R	0	Always read as 0.
9	RESERVED	R	0	Always read as 0.
8	UNKNOWN	R (Latched)	0	1'b 0: No other fault has occurred 1'b 1: A fault type not specified in bits[15:1] of STATUS_WORD has been detected
Low Byte	STATUS_BYTE	R	-	STATUS_BYTE is the lower byte of STATUS_WORD.

STATUS_VOUT (7Ah)

The STATUS_VOUT command returns 1 data byte with information regarding the MPM3690-50D.

Bits	Name	Behavior	Default	Description
7	VOUT_OV_FAULT	R (Latched)	0	1'b 0: No output over-voltage (OV) fault has occurred 1'b 1: An output OV fault has occurred
6	RESERVED	R	0	Always read as 0.
5	RESERVED	R	0	Always read as 0.
4	VOUT_UV_FAULT	R (Latched)	0	1'b 0 No output under-voltage (UV) fault has occurred 1'b 1 An output UV fault has occurred

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3	VOUT_MAX_MIN	R (Latched)	0	1'b 0: No VOUT_MAX, VOUT_MIN warning has been detected 1'b 1: An attempt has been made to set V_{OUT} to exceed VOUT_MAX or to be below VOUT_MIN
2	RESERVED	R	0	Always read as 0.
1	RESERVED	R	0	Always read as 0.
0	UNKNOWN	R (Latched)	0	1'b 0: No other fault has occurred 1'b 1: A fault type not specified in bits[15:1] of STATUS_WORD has been detected

STATUS_IOUT (7Bh)

Format: Unsigned binary

The STATUS_IOUT command returns the flags indicating the I_{OUT} status for the MPM3690-50D.

Bits	Name	Behavior	Default	Description
7	IOUT_OC	R (Latched)	0	1'b 0: No I_{OUT} over-current (OC) fault has occurred 1'b 1: An I_{OUT} OC fault has occurred
6	IOUT_OC_ &VOUT_UV	R (Latched)	0	1'b 0: No I_{OUT} OC and V_{OUT} under-voltage (UV) fault has occurred 1'b 1: An I_{OUT} OC and V_{OUT} UV fault has occurred
5	IOUT_OC_ WARNING	R (Latched)	0	1'b 0: No I_{OUT} OC warning has occurred 1'b 1: I_{OUT} OC warning has occurred
4:0	RESERVED	R	0	Reserved.

STATUS_INPUT (7Ch)

The STATUS_INPUT command returns the value of flags indicating the V_{IN} status of the MPM3690-50D. To clear the bits in this register, the underlying fault or warning should be removed, and a CLEAR_FAULTS command should be issued.

Bits	Name	Behavior	Default	Description
7	VIN_OV_FAULT	R (Latched)	0	1'b 0: No over-voltage (OV) condition has been detected on the VIN pin 1'b 1: An OV condition has been detected on the VIN pin
6	VIN_OV_WARN	R (Latched)	0	1'b 0: No V_{IN} OV condition has occurred 1'b 1: A V_{IN} OV condition has occurred
5	VIN_UV_WARN	R (Latched)	0	1'b 0: V_{IN} does not exceed VIN_UV_WARN_LIMIT (58h) 1'b 1: V_{IN} exceeds VIN_UV_WARN_LIMIT (58h)
4	VIN_UV_FAULT	R (Latched)	0	1'b 0: V_{IN} exceeds VIN_OFF (36h) 1'b 1 V_{IN} is below VIN_OFF (36h)
3:0	RESERVED	R	0	Always read as 0000.

STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns the value of flags indicating over-temperature (OT) faults or warnings. To clear the bits in this register, the underlying fault should be removed, and a CLEAR_FAULTS command should be issued.

Bits	Name	Behavior	Default	Description
7	OT_FAULT	R (Latched)	0	1'b 0: No over-temperature (OT) fault has occurred 1'b 1: An OT fault has occurred

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6	OT_WARNING	R (Latched)	0	1'b 1: No OT warning has occurred 1'b 1: An OT warning has occurred
5:0	RESERVED	R	0	Always read as 0.

STATUS_CML (7Eh)

Format: Unsigned binary

The STATUS_CML command returns the flags indicating command or data faults.

Bits	Name	Behavior	Default	Description
7	INVALID/ UNSUPPORTED_ COMMAND	R (Latched)	0	1'b 0: No invalid/unsupported command has been received 1'b 1: An invalid/unsupported command has been received
6	INVALID/ UNSUPPORTED_ DATA	R (Latched)	0	1'b 0: No invalid/unsupported data has been received 1'b 1: Invalid/unsupported data has been received
5	RESERVED	R	0	Always read as 0.
4	MEMORY_FAULT	R (Latched)	0	1'b 0: No memory fault has occurred 1'b 1: A memory fault has occurred
3	RESERVED	R	0	Always read as 0.
2	RESERVED	R	0	Always read as 0.
1	OTHER_FAULT	R (Latched)	0	1'b 0: No other fault has occurred 1'b 1: Other fault has occurred
0	MEMORY_BUSY	R (Latched)	0	1'b 0: No memory busy fault has occurred 1'b 1: A memory busy fault has occurred

READ_VIN (88h)

Format: Direct

The READ_VIN command returns the 10-bit measured value of the input voltage (V_{IN}).

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Reserved.
9:0	R	READ_VIN	10'b: 25mV/LSB

READ_VOUT (8Bh)

Format: Direct

The READ_VOUT command returns the 13-bit measured value of the output voltage (V_{OUT}).

Bits	Access	Bit Name	Description
15:13	R	RESERVED	Reserved.
12:0	R	READ_VOUT	13'b: 1.25mV/LSB

READ_IOUT (8Ch)

Format: Direct

The READ_IOUT command returns the 14-bit measured value of the output current (I_{OUT}).

Bits	Access	Bit Name	Description
15:14	R	RESERVED	Reserved.
13:0	R	READ_IOUT	14'b: 62.5mV/LSB or 31.25mV/LSB, as determined by EAh, bit[4]

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READ_TEMPERATURE_1 (8Dh)

Format: Direct

The READ_TEMPERATURE_1 command returns the internally sensed temperature. This internal value is also used for over-temperature (OT) fault and warning detection. It ranges between -40°C to +215°C.

Bits	Access	Bit Name	Description
15:10	R	RESERVED	Reserved.
9	R/W	SIGN	1'b 0: Positive sign 1'b 1: Negative sign
8:0	R	READ_TEMPERATURE	9'b: 1˚C/LSB

READ_TEMPERATURE is a 2-byte, two's complement integer. Bit[9] is the signed bit.

Table 6 shows the relationship between the direct value and the real-word value.

Table 6: READ_TEMPERATURE Values

Sign	Direct Value	Real-World Value (°C)
0	0 0000 0000	0
0	0 0000 0001	+1
0	1 1111 1111	+511
1	0 0000 0001	-511
1	1 1111 1111	-1

MFR_CTRL_COMP (D0h)

The MFR_CTRL_COMP command adjusts loop compensation for the MPM3690-50D.

Bits	Access	Bit Name	Default	Description
7:5	R/W	RESERVED	4'b 0000	Reserved.
4	R/W	CFF	1'b 0	Sets the feed-forward capacitance when the internal feedback resistor divider is selected. 1'b 0: 20pF 1'b 1: 50pF
3:1	R/W	RAMP	3'b 110	Sets the internal ramp compensation to stabilize the loop. Ensure that the actual RAMP amplitude is related to EAh, bit[3]. See the MFR_CTRL (EAh) section on page 38 for more details. 3'b 000: 8.6mV RAMP 3'b 001: 15mV RAMP 3'b 010: 27mV RAMP 3'b 011: 45mV RAMP 3'b 100: 13mV RAMP 3'b 101: 23mV RAMP 3'b 110: 41mV RAMP 3'b 111: 68mV RAMP
0	R/W	SLAVE_FAULT_ DETECTION	1'b 1	Enables the slave-phase fault detection function through the PG pin. 1'b 0: Enabled 1'b 1: Disabled

MFR_CTRL_VOUT (D1h)

The MFR_CTRL_VOUT command adjusts V_{OUT} and the PG delay.

Bits	Access	Bit Name	Default	Description
7	R/W	RESERVED	1'b 0	Reserved.
6	R/W	VOUT_ DISCHARGE	1'b 0	1'b 1: Output voltage discharges at CTRL low 1'b 0: There is no active output voltage discharge

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5:2	R/W	PG_DELAY	4'b 0000	Sets the PG delay. 4'b 0000: 2ms 4'b 0001: 3ms …… 4'b 1110: 16ms 4'b 1111: 1ms
1:0	R/W	VO_RANGE	2'b 00	2'b 00: External voltage divider: V_{REF} = 0.5V to 0.672V 2'b 01: Internal voltage divider: V_{REF} / V_{OUT} = 1:2, V_{OUT} = 0.4V to 1.344V 2'b 10: Internal voltage divider: V_{REF} / V_{OUT} = 1:4, V_{OUT} = 0.7V to 2.688V 2'b 11: Internal voltage divider: V_{REF} / V_{OUT} = 1:8, V_{OUT} = 1.3V to 5.376V

MFR_CTRL_OPS (D2h)

The MFR_CTRL_OPS command sets the switching frequency (f_{SW}) and light-load operation mode.

Bits	Access	Name	Default	Description
7:3	R	RESERVED	5'b 00000	Reserved.
2:1	R/W	SWITCHING_ FREQUENCY	2'b 01	2'b 00: Sets f_{SW} to 400kHz 2'b 01: Sets f_{SW} to 600kHz 2'b 10: Sets f_{SW} to 800kHz 2'b 11: Sets f_{SW} to 1000kHz
0	R/W	SKIP_CCM(SYNC)	1'b 1	1'b 0: Pulse-skip mode under light loads 1'b 1: FCCM under light loads

MFR_ADDR_PMBUS (D3h)

Format: Direct

The MFR_ADDR_PMBUS command sets the address for the master and slave, which can be determined by the ADDR pin or bits[6:0] of this command.

Bits	Access	Name	Default	Description
7	R/W	ENABLE_BIT	1'b 0	1'b 1: The address is determined by MFR_ADDR_PMBUS, bits[6:0] 1'b 0: The address is determined by ADDR pin.
6:0	R/W	ADDRESS	7'b 1010000	Sets the address value if MFR_ADDR_PMBUS, bit[7] is set to 1.

MFR_VOUT_FAULT_LIMIT (D4h)

This MFR_VOUT_FAULT_LIMIT command sets the thresholds for over-voltage protection (OVP). The OVP threshold are relative to the reference voltage (V_{REF}).

Bits	Access	Name	Default	Description
7:4	R	RESERVED	4'b 0000	Reserved.
3:2	R/W	OV_EXIT_TH	2'b 01	2'b 00: 10% of V_{REF} 2'b 01: 50% of V_{REF} 2'b 10: 80% of V_{REF} 2'b 11: 102.5% of V_{REF}
1:0	R/W	OV_ENTER_TH	2'b 01	2'b 00: 115% of V_{REF} 2'b 01: 120% of V_{REF} 2'b 10: 125% of V_{REF} 2'b 11: 130% of V_{REF}

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MFR_OVP_NOCP_SET (D5h)

The MFR_OVP_NOCP_SET command sets the responses for V_{OUT} OVP.

Bits	Access	Name	Default	Description
7:4	R	RESERVED	4'b 0000	Reserved.
3	R/W	DELAY_NOCP	1'b 0	1'b 0: 100ns delay after NOCP 1'b 1: Reserved
2	N/A	RESERVED	N/A	Reserved.
1:0	R/W	VOUT_OV_ RESPONSE	2'b 10	2'b 00: Latch-off with V_{OUT} discharge 2'b 01: Latch-off without V_{OUT} discharge in DCM 2'b 10: Hiccup mode with V_{OUT} discharge 2'b 11: Hiccup mode without V_{OUT} discharge in DCM

MFR_VOUT_OVP_NOCP_SET, bits[1:0] tells the converter what action to take in response to an output OV fault. These options are described in greater details below.

- Latch-off with output discharge: If the device reaches the OV entry threshold, the LS-FET turns on until it reaches NOCP. Then the LS-FET turns off for a fixed time before turning on again. The device operates in this way until V_{FB} drops below the OVP exit threshold set by register D4h, bits[3:2], then the LS-FET turns off. If V_{FB} rises above the OV entry threshold again, the LS-FET turns on again to discharge V_{OUT}. The converter does not attempt to restart until the power is cycled on VIN, VCC, or CTRL.
- Latch-off without output discharge (only effective in DCM): If the device reaches the OV entry threshold, the LS-FET turns on. When the inductor current reaches zero, the converter enters Hi-Z mode (output disabled). The converter stops discharging V_{OUT}. The converter does not attempt to restart until the power is cycled on VIN, VCC, or CTRL.
- Hiccup mode with output discharge: If the device reaches the OV entry threshold, the LS-FET turns on until it reaches NOCP. Then the LS-FET turns off for a fixed time before turning on again. The device operates in this way until V_{FB} drops below the OVP exit threshold set by register D4h, bits[3:2], and then the LS-FET turns off. A new soft start is initiated.
- Hiccup mode without output discharge: If the device reaches the OV entry threshold, the LS-FET turns on until it reaches NOCP. Then the device initiates a new soft start.

If this fault occurs, the device performs the following actions:

- Sets the VOUT_OV bit in the STATUS_BYTE.
- Sets the V_{OUT} bit in the STATUS_WORD.
- Sets the V_{OUT} OV fault bit in the STATUS_VOUT command.
- Notifies the host by asserting ALERT pin.

MFR_OT_OC_SET (D6h)

This MFR_OT_OC_SET command sets the responses of over-current protection (OCP) and what kind of action to take in response to an over-temperature fault. It is a 1-byte command.

Bits	Access	Name	Default	Description
7:4	R	RESERVED	4'b 0000	Reserved
3	R/W	OC_RESPONSE	1'b 1	1'b 0: Latch-off 1'b 1: Retry
2:1	R/W	OT_HYST	2'b 00	2'b 00: 20°C 2'b 01: 25°C 2'b 10: 30°C 2'b 11: 35°C

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0	R/W	OT_RESPONSE	1'b 0	1'b 0: Latch-off 1'b 1: Retry after the temperature drops by the value set by bits[2:1] of this command

MFR_OC_PHASE_LIMIT (D7h)

The MFR_OC_PHASE_LIMIT command sets the inductor valley current limit of each individual phase. This is a cycle-by-cycle current limit. After 31 consecutive cycles of OC, it triggers OCP. It's a 1 byte command.

Bits	Access	Name	Default	Description
7:5	R	RESERVED	3'b 000	Reserved
4:0	R/W	OC_LIMIT	5'b 10010	Current limit. 1.5A/LSB.

The value is unsigned and 1LSB = 1.5A. The default value is 25.5A per-phase, for a total of 50A.

MFR_PGOOD_ON_OFF_LIMIT (D9h)

The MFR_PGOOD_ON_OFF_LIMIT command sets the thresholds for PGOOD on and off.

Bits	Access	Name	Default	Description
7:4	R	RESERVED	4'b 0000	Reserved.
3:2	R/W	PG_OFF	2'b 00	2'b 00:69% of V_{REF} 2'b 01:74% of V_{REF} 2'b 10:79% of V_{REF} 2'b 11:84% of V_{REF}
1:0	R/W	PG_ON	2'b 00	2'b 00:90% of V_{REF} 2'b 01:92.5% of V_{REF} 2'b 10:95% of V_{REF} 2'b 11:97.5% of V_{REF}

D9h, bits[3:2] sets the under-voltage protection (UVP) threshold. When V_{FB} drops below the PG_OFF level, the MPM3690-50D enters UVP. The devices responds to UVP similar to the OCP response.

Any fault condition pulls PG low.

MFR_VOUT_STEP (DAh)

The MFR_VOUT_STEP command sets the slew rate of the V_{OUT} transition after soft start finishes. It does not determine the V_{OUT} slew rate during soft start.

Bits	Access	Name	Default	Description
7:4	R	RESERVED	4'b 0000	Reserved.
3:0	R/W	VOUT_STEP	4'b 0100	0000: 20µs/2mV 1LSB = 2.5µs/2mV. The maximum VOUT_STEP is 40µs/2mV when bits[3:0] = 4b'1000. If bits[3:0] exceeds 4b'1000, VOUT_STEP is 30µs/2mV.

The default value of DAh is 0x04.When the value of DAh exceeds 0x08, the slew rate stays at 30µs/2mV.

MFR_CTRL (EAh)

The MFR_CTRL command enables certain functions. Bit[9] and bit[3] are user accessible for the MFR_CTRL (EAh). The other bits are reserved for manufacturer use only.

Bits	Access	Name	Default	Description
15:10	R	RESERVED	-	For manufacturer use only.
9	R/W	OSM	1'b 0	1'b 0: Enable output sink mode (OSM) 1'b 1: Disable OSM

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8:5	R	RESERVED	-	For manufacturer use only.
4	R/W	OUTPUT_ CURRENT_READ-BACK_RESOLUTION	1’b 0	For manufacturer use only. Selects the accuracy of the output current. For the default code “0001”, this bit is set to 0; for the “2222” code, this bit is set to 1. 1’b 0: 62.5mA/LSB 1’b 1: 31.25mA/LSB
3:0	R	RESERVED	-	Bit[3] chooses single-phase or multi-phase operation. The selection of this bit affects the actual RAMP amplitude selected via register D0h, bits[3:1]. See the MFR_CTRL_COMP (D0h) section on page 35 for more details. For manufacturer use only

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APPLICATION INFORMATION

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with temperature. Use ceramic capacitors with X5R and X7R dielectrics because they are fairly stable across a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (2):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (3):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (3)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter's input voltage ripple. Select a capacitor value that meets the input voltage ripple requirements.

Estimate the input voltage ripple with Equation (4):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, estimated with Equation (5):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (5)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. The output voltage ripple can be calculated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (6)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. This means that the output voltage ripple dominates the output capacitance. For simplification, estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

When using capacitors with a larger ESR (e.g. POSCAP and OSCON) the ESR dominates the impedance at the switching frequency. In this scenario, the output voltage ripple is determined by the ESR values. For simplification, the output ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

Low-V_{IN} Applications

For low-V_{IN} applications (3V < V_{IN} < 4V), an external V_{CC} biased power supply is required. The external V_{CC} bias must exceed 2.9V, which is the V_{CC} UVLO rising threshold maximum value.

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PCB Layout Guidelines

For the best results, refer to Figure 7 and follow the guidelines below.

VIN

1. Place sufficient decoupling capacitors as close as possible to the VIN and GND pins.
2. Place sufficient GND vias around the GND pad of the decoupling capacitors.
3. Avoid placing sensitive signal traces close to the input copper plane and/or vias without sufficient ground shielding.
4. Use a minimum of four 22µF/25V ceramic capacitors at the input channel to provide sufficient decoupling.

VOUT

1. Connect all VOUT pins together on a copper plane.
2. Place sufficient vias near the VOUT pads to provide a current path with minimal parasitic impedance.

GND

1. Connect all GND pins of the module on a copper plane.
2. Place sufficient vias close to the GND pins to provide a current return path with minimal thermal resistance and parasitic impedance.

VS1P and VS1N

1. Connect FB1 to FB2, then connect VS1N to VS2N.
2. Route VS1P and VS1N as differential signals.
3. Avoid routing VS1P and VS1N traces close to the input plane and high-speed signals.

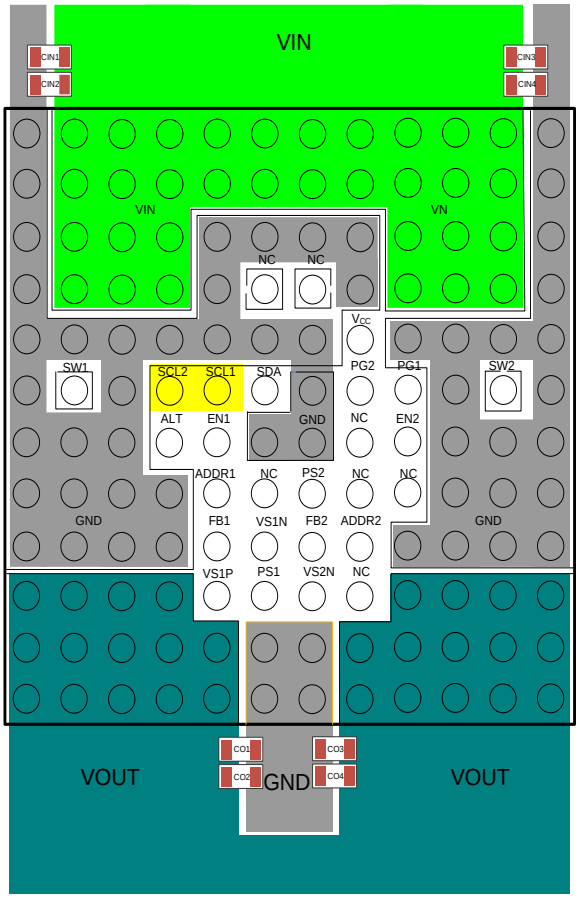

Figure 7: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

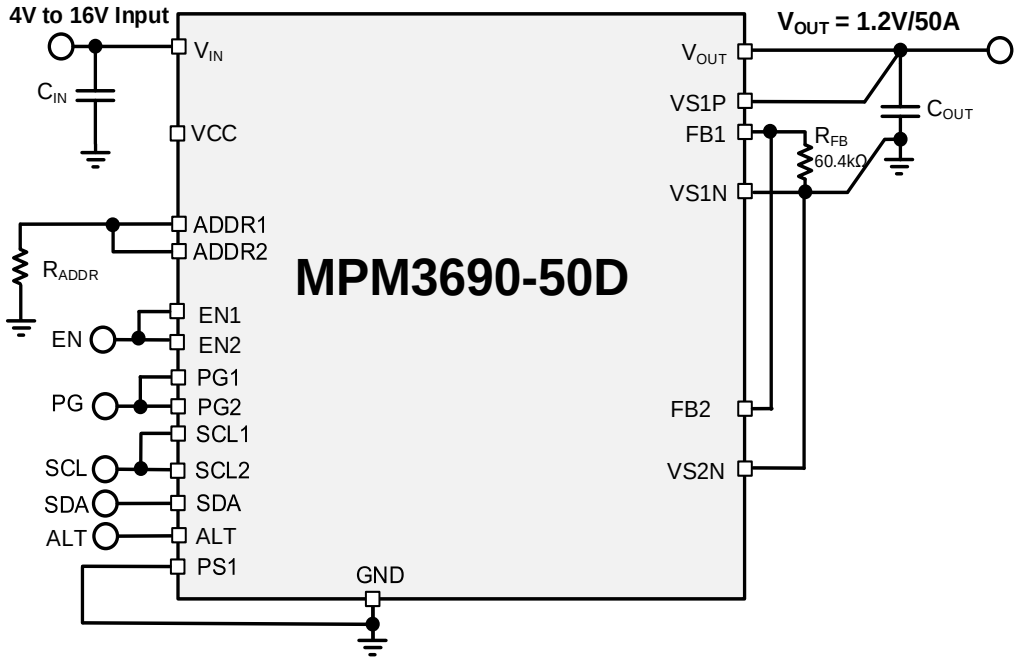

Figure 8: Typical Application Circuit with Interleaved Operation (1.2V at 50A with Remote Sense)

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MPM3690GBF-50D-0001 CONFIGURATION CODES

Table 7: -0001 Suffix Code Configurations

Items	Channel 1
Output voltage set method	External divider
FB voltage	0.6V
Soft-start delay time	4ms
Individual valley current limit	25.5A
Light-load mode	FCCM
Individual switching frequency	600kHz
RAMP	41mV
UVLO rising	4V
UVLO falling	2.75V
OT fault limit	160°C
OT warning limit	140°C
VIN_OV_FAULT_LIMIT	18V
Output current read back resolution	62.5mA/LSB

Table 8: -0001 Suffix Register Values

Register	Hex Value	Register	Hex Value
01	80	60	0
02	1E	61	2
10	0	64	0
21	258	D0	D
24	BB8	D1	0
25	2A0	D2	3
26	200	D3	0
29	1F4	D4	3
2b	FA	D5	2
35	10	D6	9
36	B	D7	11
4F	A0	D8	0
51	8C	D9	0
55	24	DA	4
57	20	EA	8
58	1	-	-

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MPM3690GBF-50D-2222 CONFIGURATION CODES

Table 9: -2222 Suffix Code Configurations

Items	Channel 1
Output voltage set method	External divider
FB voltage	0.6V
Soft-start delay time	4ms
Individual valley current limit	25.5A
Light-load mode	FCCM
Individual switching frequency	600kHz
RAMP	41mV
UVLO rising	4V
UVLO falling	2.75V
OT fault limit	160°C
OT warning limit	140°C
VIN_OV_FAULT_LIMIT	18V
Output current read back resolution	31.25mA/LSB

Table 10: -2222 Suffix Register Values

Register	Hex Value	Register	Hex Value
01	80	60	0
02	1E	61	2
10	0	64	0
21	258	D0	D
24	BB8	D1	40
25	2A0	D2	3
26	200	D3	30
29	1F4	D4	3
2b	FA	D5	2
35	10	D6	9
36	B	D7	11
4F	A0	D8	0
51	8C	D9	0
55	24	DA	4
57	20	EA	18
58	1	-	-

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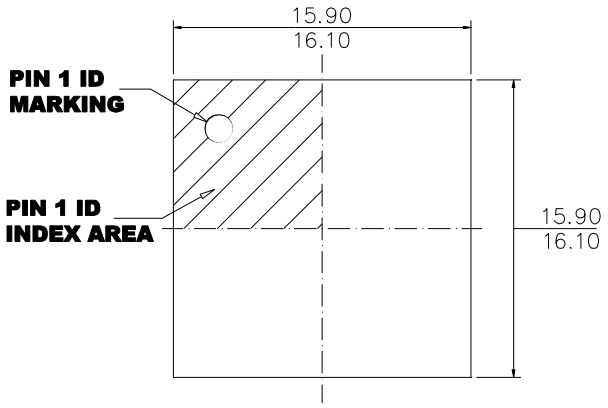
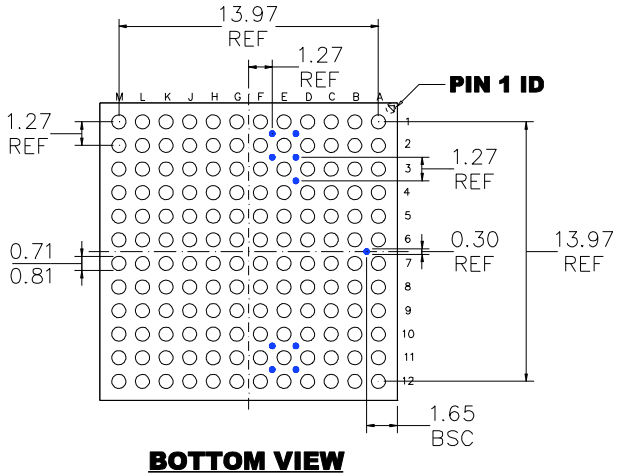
PACKAGE INFORMATION

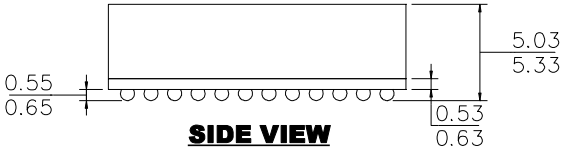
BGA (16mmx16mmx5.18mm)



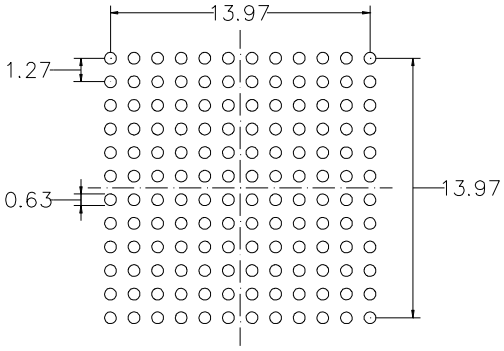
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) THE SOLID BLUE CIRCLES REPRESENT TEST PADS WITHOUT SOLDER BALL.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-275A.
5) DRAWING IS NOT TO SCALE.

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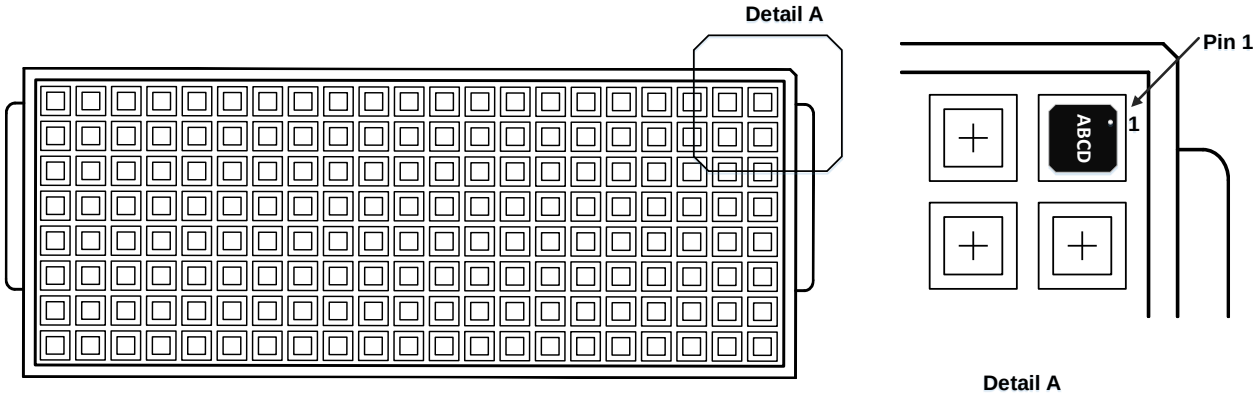
CARRIER INFORMATION (9)



Part Number	Package Description	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3690GBF-50D-xxxx-T	BGA (16mmx16mmx5.18mm)	N/A	90	N/A	N/A	N/A

Note:

9) This is a schematic diagram of the tray. Different packages correspond to different trays, each with a different length, width, and height.

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/16/2023	Initial Release	-

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