MPQ2946

Digital, 8-Phase Controller with Three Rails, AEC-Q100 Qualified

DESCRIPTION

The MPQ2946 is a digital, three-rail, multi-phase controller for autonomous driving applications. It can work with MPS's Intelli-Phase™ products to complete the multi-phase voltage regulator (VR) solution with minimal external components. The device can be configured for up to 8 phases between three rails.

The on-chip, multiple-time programmable (MTP) memory stores and restores device configurations. Device configurations and fault parameters can be configured or monitored via the digital interface. The MPQ2946 can monitor and report the output current (I_{OUT}) through the Intelli-Phase™ current-sense (CS) output.

The MPQ2946 is based on unique, digital, multi-phase nonlinear control to provide fast transient response to a load step with minimal output capacitors. With only one power loop control method for both the steady state and load transient response, power loop compensation is simple to configure.

The MPQ2946 is available in a TQFN-48 (7mmx7mm) package. It is available in AEC-Q100 Grade 1.

FEATURES

- 3-Rail, Up to 8-Phase Digital Pulse-Width Modulation (PWM) Controller
- Digital Interface for Configuring and Monitoring
- Built-In Multiple-Time Programmable (MTP) Memory to Store Custom Configurations
- Automatic Loop Compensation
- Automatic Phase-Shedding (APS) with and without Discontinuous Conduction Mode (DCM) to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing
- Input Voltage (V_{IN}) and Output Voltage (V_{OUT}) Monitoring
- Output Current (I_{OUT}) Monitoring
- Regulator Temperature Monitoring
- Under-Voltage Lockout (UVLO), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection (OCP), and Over-Temperature Protection (OTP)
- Cyclic Redundancy Check (CRC) for MTP Transformation
- Separate Enable (EN) for Each Rail
- Digital, Configurable Load Line
- Available in a TQFN-48 (6mmx6mm) Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Autonomous Driving Systems-on-Chip (SoCs)
- Infotainment Systems

TYPICAL APPLICATION

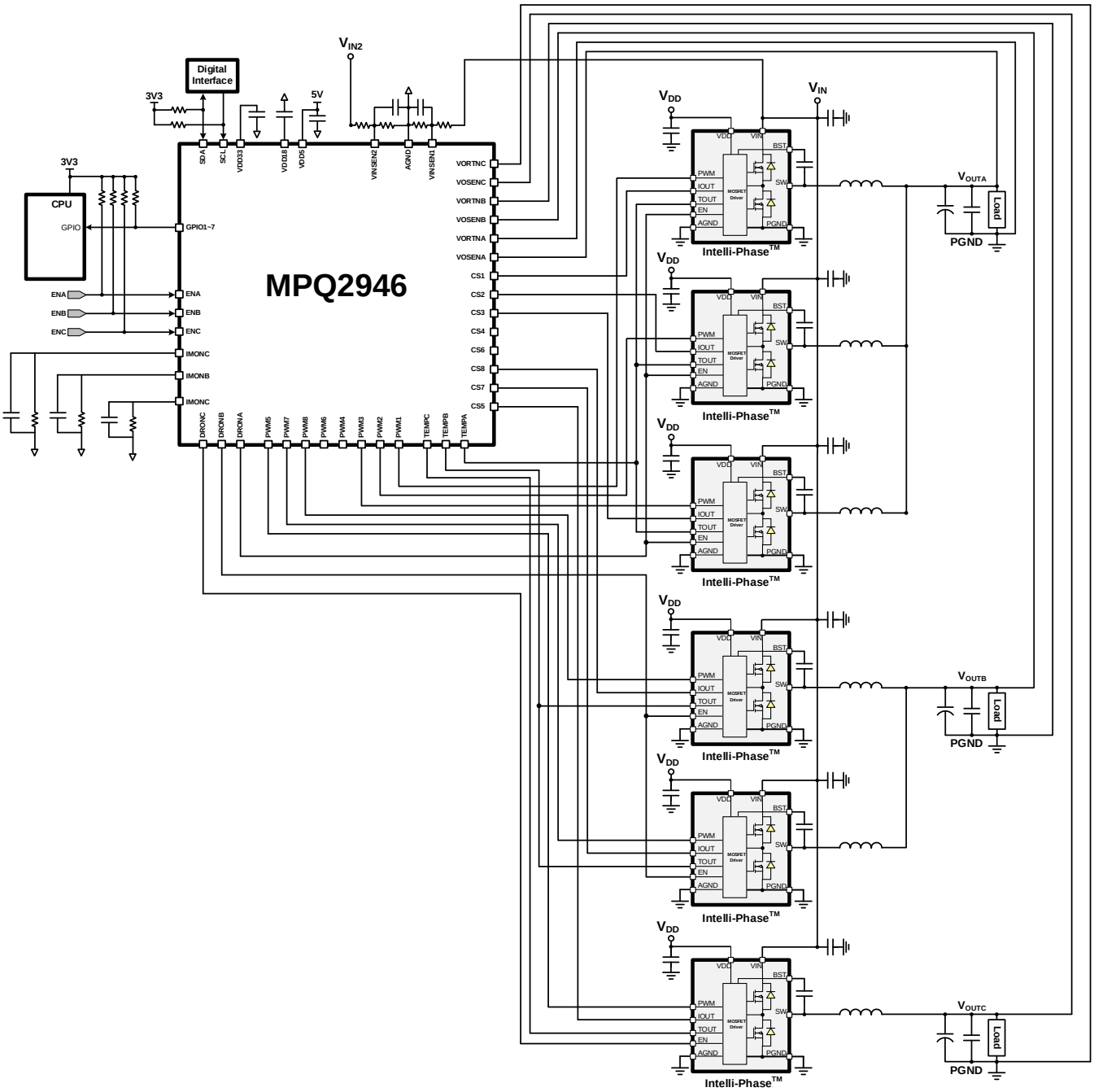


Figure 1: 3 + 2 + 1 Configuration

ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ2946GQNTE-xxxx-AEC1**	TQFN-48 (7mmx7mm)	*See Below*

* For Tape & Reel, add suffix-Z (e.g. MPQ2946GQNTE-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier for the register settings stored in the internal non-volatile memory (NVM). Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

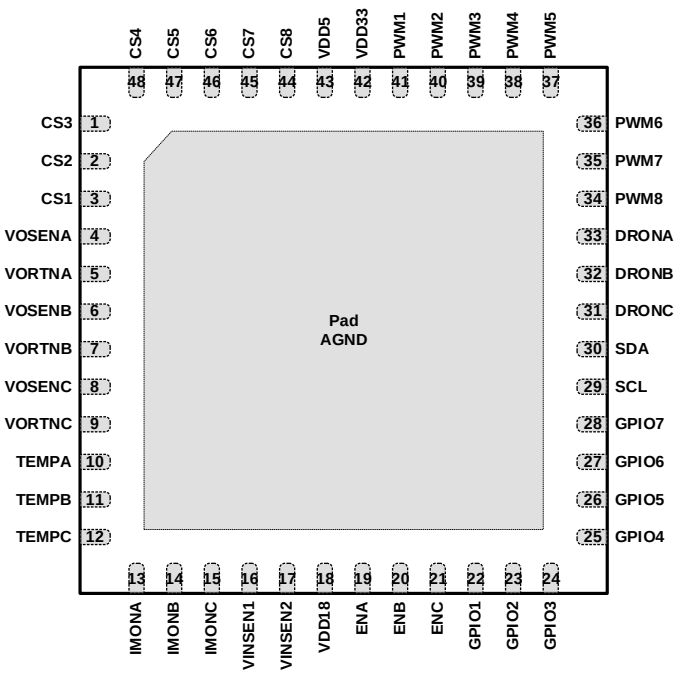
TOP MARKING

MPSYYWW
MP2946
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP2946: Part number
LLLLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE

TOP VIEW



TQFN-48 (7mmx7mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	CS3	A [I]	**Phase 3 current-sense input.** Float the CS pin of any unused phase(s).
2	CS2	A [I]	**Phase 2 current-sense input.** Float the CS pin of any unused phase(s).
3	CS1	A [I]	**Phase 1 current-sense input.** Float the CS pin of any unused phase(s).
4	VOSENA	A [I]	**Positive remote voltage sense input for rail A.** Connect this pin directly to the VR's output voltage at the load. Route this pin differentially with VORTNA. Ground this pin if rail A is not used.
5	VORTNA	A [I]	**Remote voltage-sensing return input for rail A.** Connect this pin directly to ground at the load. Route this pin differentially with VOSENA.
6	VOSENB	A [I]	**Positive remote voltage sense input for rail B.** Connect this pin directly to the VR's output voltage at the load. Route this pin differentially with VORTNB. Ground this pin if rail B is not used.
7	VORTNB	A [I]	**Remote voltage-sensing return input for rail B.** Connect this pin directly to ground at the load. Route this pin differentially with VOSENB.
8	VOSENC	A [I]	**Positive remote voltage sense input for rail C.** Connect this pin directly to the VR's output voltage at the load. Route this pin differentially with VORTNC. Ground this pin if rail C is not used.
9	VORTNC	A [I]	**Remote voltage-sensing return input for rail C.** Connect this pin directly to ground at the load. Route this pin differentially with VOSENC.
10	TEMPA	A [I]	**Analog signal from rail A of the VR to the controller.** This pin's signal indicates the power stage temperature. Connect all Intelli-Phase's™ temperature reporting pins for rail A together to produce the maximum junction temperature, then connect them to the controller's TEMPA pin. Ground this pin if it is not used.
11	TEMPB	A [I]	**Analog signal from rail B of the VR to the controller.** This pin's signal indicates the power stage temperature. Connect all Intelli-Phase's™ temperature reporting pins for rail B together to produce the maximum junction temperature, then connect them to the controller's TEMPB pin. Ground this pin if it is not used.
12	TEMPC	A [I]	**Analog signal from rail C of the VR to the controller.** This pin's signal indicates the power stage temperature. Connect all Intelli-Phase's™ temperature reporting pins for rail C together to produce the maximum junction temperature, then connect them to the controller's TEMPC pin. Ground this pin if it is not used.
13	IMONA	A [I/O]	**Analog total load current signal for the VR's rail A.** The IMONA pin sources a current proportional to the sensed total load current for rail A. Connect an external resistor from IMONA to AGND to configure the gain. Ground this pin if rail A is not used.
14	IMONB	A [I/O]	**Analog total load current signal for the VR's rail B.** The IMONB pin sources a current proportional to the sensed total load current for rail B. Connect an external resistor from IMONB to AGND to configure the gain. Ground this pin if rail B is not used.
15	IMONC	A [I/O]	**Analog total load current signal for the VR's rail C.** The IMONC pin sources a current proportional to the sensed total load current for rail C. Connect an external resistor from IMONC to AGND to configure the gain. Ground this pin if rail C is not used.
16	VINSEN1	A [I]	**Input voltage sense.** Connect VINSEN1 to the first input (VIN1) through a resistor divider. Each rail can be assigned to either VINSEN1 or VINSEN2.
17	VINSEN2	A [I]	**Input voltage sense.** Connect VINSEN2 to the second input (VIN2) through a resistor divider. Each rail can be assigned to either VINSEN1 or VINSEN2.
18	VDD18	A [I/O]	**1.8V LDO output for internal digital power supply.** Connect a 1µF bypass capacitor from VDD18 to AGND.

PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
19	ENA	D [I]	**Enable control for rail A.**
20	ENB	D [I]	**Enable control for rail B.**
21	ENC	D [I]	**Enable control for rail C.**
22	GPIO1	D [O]	**General-purpose output.** The GPIOx pins can be configured for the following pin functions: FAULT: Open-drain output that signals when a fault occurs. Can be separate for each rail. VRRDY: Open-drain output that signals when the output voltage (V_{OUT}) is outside of the proper operating range. Can be separate for each rail. ALERT: Open-drain output that asserts during VID changes. ALERT de-asserts when VID is done changing. Can be separate for each rail. VOUT_ALT: Open-drain output that signals when V_{OUT} exceeds the configured VOUT_ALT threshold. Can be separate for each rail. IOUT_ALT: Open-drain output that signals when the output current (I_{OUT}) exceeds the configured IOUT_ALT threshold. Can be separate for each rail. VR_HOT: Open-drain output that signals when the monitored temperature exceeds the configured VRHOT temperature threshold. Can be separate for each rail.
23	GPIO2	D [O]	
24	GPIO3	D [O]	
25	GPIO4	D [O]	
26	GPIO5	D [O]	
27	GPIO6	D [O]	
28	GPIO7	D [O]	
29	SCL	D [I]	**Source synchronous clock from another digital interface.**
30	SDA	D [I/O]	**Data signal between VR controller and another digital interface.**
31	DRONC	D [O]	**Digital output to enable or disable rail C's Intelli-Phase™.**
32	DRONB	D [O]	**Digital output to enable or disable rail B's Intelli-Phase™.**
33	DRONA	D [O]	**Digital output to enable or disable rail A's Intelli-Phase™.**
34	PWM8	D [O]	**Tri-state logic-level pulse-width modulation (PWM) outputs.** Each output is connected to the input of Intelli-Phase's™ PWM pin. The logic levels are 0V for low logic and 3.3V for high logic. The output is set to tri-state to shut down the Intelli-Phase's™ high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET).
35	PWM7	D [O]	
36	PWM6	D [O]	
37	PWM5	D [O]	
38	PWM4	D [O]	
39	PWM3	D [O]	
40	PWM2	D [O]	
41	PWM1	D [O]	
42	VDD33	A [I/O]	**3.3V LDO output for internal power supply.** Connect a 4.7µF bypass capacitor to ground.
43	VDD5	A [I]	**5V power supply input.** Place a 4.7Ω resistor in series with the 5V supply line, then connect a 4.7µF bypass capacitor from VDD5 to ground, placed close to the VDD5 pin.
44	CS8	A [I]	**Phase 8 current-sense input.** Float the CS pin of any unused phase(s).
45	CS7	A [I]	**Phase 7 current-sense input.** Float the CS pin of any unused phase(s).
46	CS6	A [I]	**Phase 6 current-sense input.** Float the CS pin of any unused phase(s).
47	CS5	A [I]	**Phase 5 current-sense input.** Float the CS pin of any unused phase(s).
48	CS4	A [I]	**Phase 4 current-sense input.** Float the CS pin of any unused phase(s).
PAD	AGND	A [I/O]	**Analog ground.**

ABSOLUTE MAXIMUM RATINGS (1)

VDD5 .....-0.3V to +6V
VDD33 .....-0.3V to +4V
VDD18 .....-0.3V to +2.2V
VORTNA/B/C.....-0.3V to +0.3V
AGND .....-0.3V to +0.3V
VINSEN1/2, IMONA/B/C…… .....-0.3V to 2.2V
PWM1 to PWM8, DRONA/B/C, GPIO1-7, SDA, SCL, ENA/B/C .....-0.3V to +4V
All other pins.....-0.3V to +6V
Junction temperature (T_J) .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

Recommended Operating Conditions (2)

VDD5.....……..4.5V to 5.5V
Operating junction temp (T_J).....-40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

TQFN-48 (7mmx7mm) .....4.7…11.3…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on a JESD51-7, 6-layer PCB.