MPQ2967

Dual-Rail, Digital, 4-Phase Controller with PMBus Interface, AEC-Q100 Qualified

DESCRIPTION

The MPQ2967 is a digital, dual-rail, multi-phase controller for autonomous driving applications. It can work with MPS's Intelli-Phase™ products to complete the multi-phase voltage regulator (VR) solution with minimal external components. The device can be configured for up to 4 phases between two rails.

The on-chip, multiple-time programmable (MTP) memory stores and restores device configurations. Device configurations and fault parameters can be configured or monitored via the PMBus interface. The MPQ2967 can monitor and report the output current (I_{OUT}) through the Intelli-Phase™ current-sense (CS) output.

The MPQ2967 is based on unique, digital, multi-phase nonlinear control to provide fast transient response to a load step with minimal output capacitors. With only one power loop control method for both the steady state and load transient response, power loop compensation is simple to configure.

The MPQ2967 is available in a TQFN-40 (6mmx6mm) package.

FEATURES

- Dual-Rail, Up to 4-Phase Digital PWM Controller
- PMBus Compliant for Configuring and Monitoring
- PWMVID Interface Compliant
- Built-In Multiple-Time Programmable (MTP) Memory to Store Custom Configurations
- Automatic Loop Compensation
- Automatic Phase-Shedding (APS) with and without Discontinuous Conduction Mode (DCM) to Improve Overall Efficiency
- Phase-to-Phase Active Current Balancing
- Input Voltage (V_{IN}) and Output Voltage (V_{OUT}) Monitoring
- Output Current (I_{OUT}) Monitoring
- Regulator Temperature Monitoring
- Under-Voltage Lockout (UVLO), Over-Voltage Protection (OVP), Under-Voltage Protection (UVP), Over-Current Protection (OCP), Over-Temperature Protection (OTP), and Reverse-Voltage Protection (RVP)
- Cyclic Redundancy Check (CRC) and Error Correction Code (ECC) for MTP Transformation
- Packet Error Checking (PEC) for PMBus Communication
- Separate EN for Each Rail
- Digital, Configurable Load Line
- Available in a TQFN-40 (6mmx6mm) Package
- Available in AEC-Q100 Grade 1

MPSafe™ Developed for Functional Safety Applications: ISO 26262 Compliant

APPLICATIONS

- Autonomous Driving System-On-Chips (SoCs)
- Infotainment Systems

TYPICAL APPLICATION

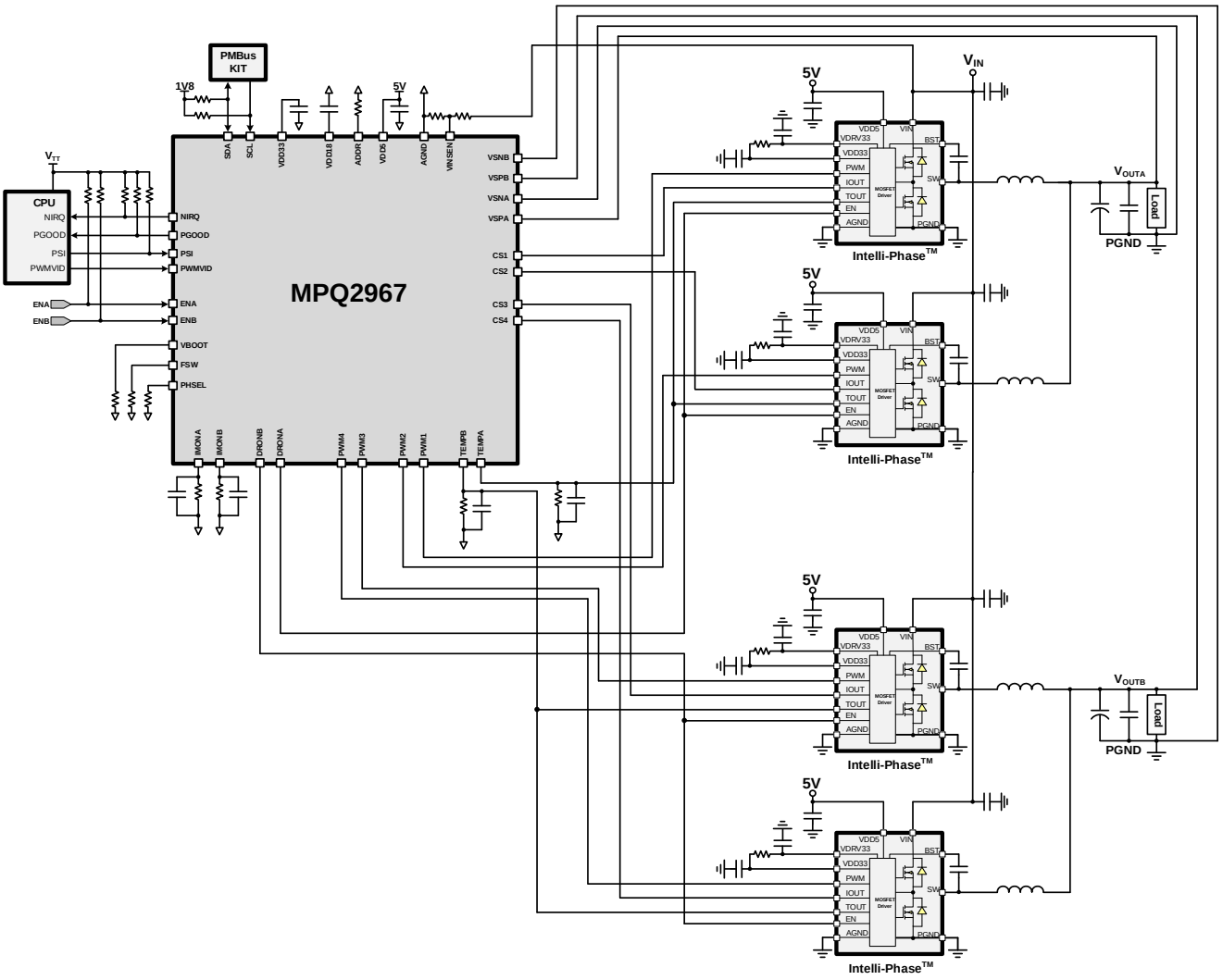


Figure 1: Typical Application Circuit for 2 + 2 Solution

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ2967GQKTE-xxxx-AEC1**	TQFN-40 (6mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MPQ2967GQKTE-xxxx-AEC1-Z).

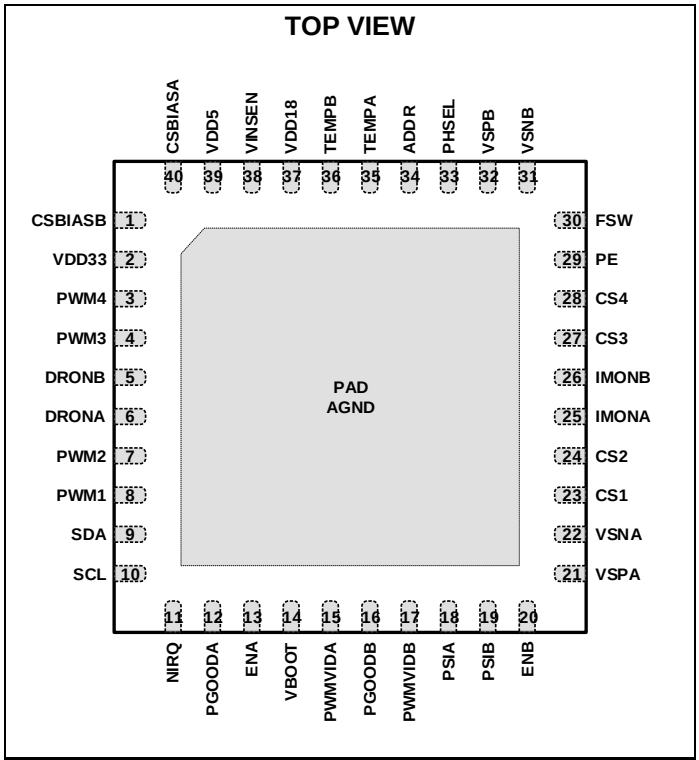
** “xxxx” is the configuration code identifier for the register settings stored in the internal non-volatile memory (NVM). Each “x” can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

TOP MARKING

MPSYYWW
MP2967
LLLLLLLLL
E

MPS: MPS prefix
YY: Year code
WW: Week code
MP2967: Part number
LLLLLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



TQFN-40 (6mmx6mm)

PIN FUNCTIONS

Pin #	Name	I/O	Description
1	CSBIASB	A [I]	**Biased voltage for IMON on rail B.** If the CSBIASB pin is not required, it should not have a connection.
2	VDD33	A [I/O]	**3.3V LDO output for the internal power supply.** Connect a 4.7µF bypass capacitor from the VDD33 pin to the ground.
3	PWM4	D [O]	**Tri-state PWM output for phase 4.**
4	PWM3	D [O]	**Tri-state PWM output for phase 3.**
5	DRONB	D [O]	**Digital output to indicate to the Intelli-Phase™ whether to enable or enter low-power mode for rail B.**
6	DRONA	D [O]	**Digital output to indicate to the Intelli-Phase™ whether to enable or enter low-power mode for rail A.**
7	PWM2	D [O]	**Tri-state PWM output for phase 2.**
8	PWM1	D [O]	**Tri-state PWM output for phase 1.**
9	SDA	D [I/O]	**Data signal between the PMBus controller and voltage regulator (VR) controller.**
10	SCL	D [I]	**Source synchronous clock from the PMBus controller.**
11	NIRQ	D [O]	**Fault interrupt output.**
12	PGOODA	D [O]	**Power good output for rail A.**
13	ENA	D [I]	**Enable control for rail A.**
14	VBOOT	A [I]	**Boot voltage strap for rail A and rail B.**
15	PWMVIDA	D [I]	**PWMVID input for rail A.**
16	PGOODB	D [O]	**Power good output for rail B.**
17	PWMVIDB	D [I]	**PWMVID input for rail B.**
18	PSIA	D [I]	**Power-saving input for rail A.**
19	PSIB	D [I]	**Power-saving input for rail B.**
20	ENB	D [I]	**Enable control for rail B.**
21	VSPA	A [I]	**Positive remote voltage sense input for rail A.** Directly connect the VSPA pin to the VR's output voltage at the load. Differentially route VSPA with VSNA.
22	VSNA	A [I]	**Remote voltage sensing return input for rail A.** Directly connect the VSNA pin to ground at the load. Differentially route VSNA with VSPA.
23	CS1	A [I]	**Current-sense input for phase 1.** Float the CS pin of any unused phase(s).
24	CS2	A [I]	**Current-sense input for phase 2.** Float the CS pin of any unused phase(s).
25	IMONA	A [I/O]	**Analog total load current signal of rail A.** The IMONA pin sources a current proportional to the sensed total load current of rail A. Connect an external resistor from IMONA to AGND to configure the gain.
26	IMONB	A [I/O]	**Analog total load current signal of rail B.** The IMONB pin sources a current proportional to the sensed total load current of rail B. Connect an external resistor from IMONB to AGND to configure the gain.
27	CS3	A [I]	**Current-sense input for phase 3.** Float the CS pin of any unused phase(s).
28	CS4	A [I]	**Current-sense input for phase 4.** Float the CS pin of any unused phase(s).
29	PE	D [I]	**Program enable.** The PE pin is the program enable input for MTP configurations.
30	FSW	A [I]	**Strap for switching frequency (f_{SW}) selection.**
31	VSNB	A [I]	**Remote voltage sensing return input for rail B.** Directly connect the VSNB pin to ground at the load. Differentially route VSNB with VSPB.

PIN FUNCTIONS *(continued)*

Pin #	Name	I/O	Description
32	VSPB	A [I]	**Positive remote voltage sense input for rail B.** Directly connect the VSPB pin to the VR's output voltage at the load. Differentially route VSPB with VSNB.
33	PHSEL	A [I]	**Strap for phase configuration selection.**
34	ADDR	A [I]	**Strap for PMBus address selection.**
35	TEMPA	A [I]	**Analog signal from the VR's rail A to the VID controller.** The TEMPA pin indicates the power stage temperature. Connect the TOUT/FLT pin of each Intelli-Phase™ on rail A together to produce the maximum junction temperature, then connect these pins to the controller's TEMPA pin.
36	TEMPB	A [I]	**Analog signal from the VR's rail B to the VID controller.** The TEMPB pin indicates the power stage temperature. Connect the TOUT/FLT pin of each Intelli-Phase™ on rail B together to produce the maximum junction temperature, then connect these pins to the controller's TEMPB pin.
37	VDD18	A [I/O]	**1.8V LDO output for the internal digital power supply.** Connect a 1µF bypass capacitor from the VDD18 pin to AGND.
38	VINSEN	A [I]	**Input voltage sense.** Connect the VINSEN pin to VIN through a 1/16 divider network.
39	VDD5	A [I]	**5V power supply input.** Connect a 4.7µF bypass capacitor from the VDD5 pin to the ground.
40	CSBIASA	A [I]	**Biased voltage for IMON on rail A.** If the CSBIASA pin is not required, it should not have a connection.
PAD	AGND	A [I/O]	**Analog ground.**