MPQ5029-C

USB Charging Port Controller with Current-Limit Switch, Supporting CDP, DCP, and QC3.0 Modes, AEC-Q100 Qualified

DESCRIPTION

The MPQ5029-C is a fully integrated, USB Type-C port controller, which is also compatible with a legacy Type-A port. It integrates a low-$R_{DS(ON)}$ USB current-limit switch and charging port identification circuit. The MPQ5029-C supports 3A of continuous output current.

The MPQ5029-C supports charging downstream port (CDP) mode, dedicated charging port (DCP) schemes for battery charging specification (BC1.2), divider mode, 1.2V/1.2V mode, and quick-charge specification (QC3.0) without the need for external user interaction. The MPQ5029-C can also support Type-C 5V @ 3A DFP mode.

Full protection features include hiccup current limiting, input over-voltage protection (OVP), thermal shutdown (TSD), and short-to-battery protection.

The MPQ5029-C requires a minimal number of readily available, standard external components to complete the USB switch and charging mode auto-detection solution. The MPQ5029-C is available in a QFN-14 (2mmx3mm) package.

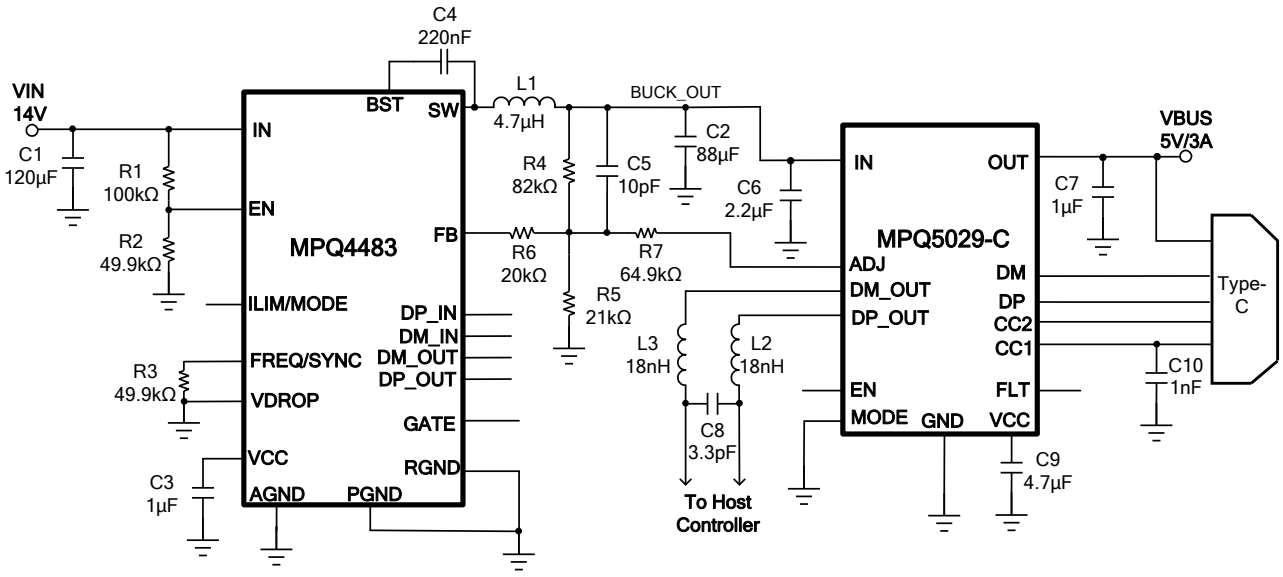
FEATURES

- Up to 22V Voltage Rating for Input and Output
- Supports BC1.2 CDP Mode
- Supports 5V DCP schemes for BC1.2, Divider Mode, 1.2V/1.2V Mode
- Supports QC3.0 (3.6V to 12V Output) Mode
- Supports Type-C 5V @ 3A DFP Mode
- I/O Pins (DP, DM, CC1, and CC2) Support Short-to-Battery Protection
- OUT Short-to-Battery Protection when V_{BUS} Is Enabled
- Line Drop Compensation for 5V Output
- 25mΩ Low $R_{DS(ON)}$ Power MOSFET
- MODE Pin to Program Charging Mode
- Intelligent Load Shedding vs. Temperature Function
- Fault Indication for Over-Current, Input OVP, Thermal Shutdown, and Short-to-Battery Fault
- OCP, OVP, and OTP Protections
- Input Over-Voltage Discharge
- ±8kV HBM ESD Rating CC1, CC2, and OUT to GND
- ±2.5kV HBM ESD Rating DM, DP to GND
- 1W VCONN Power Supply
- Available in a QFN-14 (2mmx3mm) Package with Wettable Flanks
- Available in AEC-Q100 Grade 1

APPLICATIONS

- USB Charging Downstream Ports (CDP)
- USB Type-C Port
- Dedicate Charging Port (DCP)
- USB Hub

TYPICAL APPLICATION



Type-C Port with USB2.0 CDP Mode Application

ORDERING INFORMATION

Part Number*	Package	Top Marking
MPQ5029GD-C-AEC1	QFN-14 (2mmx3mm)	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MPQ5029GD-C-AEC1–Z).

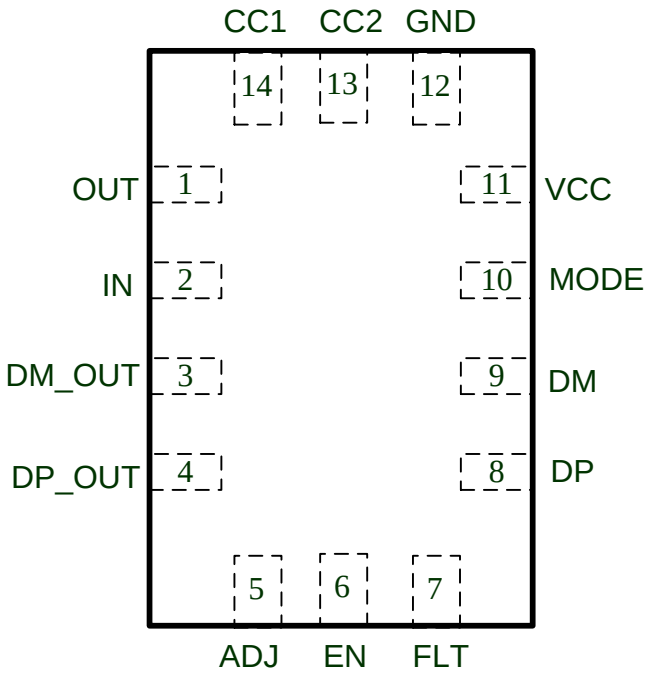
TOP MARKING

BDP
YWW
LLL

BDP: Product code of MPQ5029GD-C-AEC1
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE

TOP VIEW



QFN-14 (2mmx3mm) with Wettable Flanks

PIN FUNCTIONS

Pin #	Name	Description
1	OUT	**Output of USB current-limit switch.**
2	IN	**Supply voltage.** The MPQ5029-C can operate with a 5V typical input voltage for Type-C and USB2.0 applications, or a 3.6V to 12V input voltage for QC3.0 applications.
3	DM_OUT	**D- data line to USB host controller.**
4	DP_OUT	**D+ data line to USB host controller.**
5	ADJ	**Output voltage adjustment pin.** ADJ sinks a current from the upstream DC/DC converter's FB pin to ground to regulate the DC/DC converter's output voltage. ADJ also provides line drop compensation.
6	EN	**Enable control pin.** Apply a logic high voltage to EN to enable the IC. Pull EN to logic low to disable the IC. EN has an internal 7μA auto-pull-up current to the internal 3.5V power supply.
7	FLT	**Fault indication. Open drain.**
8	DP	**D+ data line to USB connector.** DP is the input/output used for handshaking with portable devices.
9	DM	**D- data line to USB connector.** DM is the input/output used for handshaking with portable devices.
10	MODE	**MPQ5029-C charging mode selection.** Connect MODE to VCC, float MODE, or short MODE to ground to select three different modes. VCC: DCP mode and enable QC3.0 Float: DCP mode and disable QC3.0 GND: CDP mode
11	VCC	**Internal 3.5V LDO output.** Bypass VCC with a 4.7μF ceramic capacitor.
12	GND	**Ground pin.**
13	CC2	**Configuration channel.** CC2 is used to detect connections and configure the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.
14	CC1	**Configuration channel.** CC1 is used to detect connections and configure the interface across the USB Type-C cables and connectors. Once a connection is established, CC1 or CC2 is reassigned to provide power over the VCONN pin of the plug.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +24V
Output voltage (V_{OUT}).....-0.3V to +24V
CC1, CC2, DM, DP .....-0.3V to +24V
DM_OUT, DP_OUT, VCC.....-0.3V to +4.5V
EN pin ..... -0.3V to +4V or 250µA for >4V
All other pins .....-0.3V to +4V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = +25°C) (2)
..... 3.29W

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 5V or 3.6V - 12V (QC3.0) (4)
Output voltage (V_{OUT}).....follows with V_{IN}
Output current (I_{OUT})..... up to 3A
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (5)	θ_{JA}	θ_{JC}	
QFN-14 (2mmx3mm)			
EVQ5029-C-GD-00C (5)	38	12	°C/W
JESD51-7 (6)	70	15	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Measured on an EVQ5029-C-GD-00C, 4-layer PCB, 50mmx50mm, 2oz outer layer and 1oz inner layer copper.
3) The device is not guaranteed to function outside of its operating conditions.
4) For lower V_{IN} applications, see the Operation section on page 17.
5) Measured on an EVQ5029-C-GD-00C, 4-layer PCB, 50mmx50mm, 2oz outer layer and 1oz inner layer copper.
6) Measured on a JESD51-7, 4-layer PCB. The value of θ_{JA} given in this table is only valid for comparison with other packages, and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40°C to 125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO1}	ADJ starts to work	2.7	3.0	3.3	V
UVLO hysteresis	$V_{UVLOHYS1}$			100		mV
Second V_{IN} under-voltage lockout rising threshold	V_{IN_UVLO2}	Power MOSFET Turn-on	2.9	3.1	3.3	V
Second UVLO hysteresis	$V_{UVLOHYS2}$			200		mV
EN rising threshold	V_{EN_R}		1.9	2.0	2.1	V
EN hysteresis	V_{EN_F}			100		mV
EN auto pull-up current	I_{EN_UP}		3.5	7.0	10.5	µA
VCC voltage	V_{VCC}	5mA	3.3	3.5	3.7	V
Shutdown current	I_{Q_STD}	EN = 0		22	40	µA
Supply current	I_Q	V_{IN} = 5V, Type-C detach mode		175	225	µA
		V_{IN} = 5V, no load, CC1 = 5.1kΩ, not including CC1 pull-up current		230	300	
MODE logic high voltage	V_{Mode_H}		2			V
MODE float voltage	V_{Mode_F}		1.15		1.95	V
MODE logic low voltage	V_{Mode_L}				0.7	V
USB Power FET						
On resistance	R_{DSON}	V_{IN} = 5V		25	45	mΩ
Input discharge resistance	R_{DIS_IN}		150	200	250	Ω
Soft-start time	T_{SS}	V_{IN} = 5V, no load	250	500	750	µs
Current Limit Set						
USB current limit	I_{LIMIT1}	Type-C mode, room temperature	3.10	3.65	4.20	A
	I_{LIMIT2}	Type-A mode, room temperature	2.45	2.85	3.25	A
Output Voltage Control						
Default V_{IN} voltage	V_{IN_Def}	I_{OUT} = 0A, full temperature	-3%	5.1	+3%	V
Line drop compensation	$V_{IN\_5\_C}$	I_{OUT} = 3A		285	400	mV
Protection						
V_{IN} OVP threshold	V_{OVP1}	Mode = float or GND, V_{IN} = 5V	5.60	5.95	6.30	V
	V_{OVP2}	Mode = VCC, V_{IN} = 5V	5.50	5.75	6.00	V
V_{IN} OVP recovery threshold	$V_{OV\_Recovery}$	Reset mode to 5V default	5.20	5.45	5.70	V
DM, DP pins OVP rising	$V_{OV\_DM\_DP}$		3.7	4.0	4.3	V
DM, DP pins OVP hysteresis	$V_{OV\_DM\_DP\_HYS}$			130		mV
OCP hiccup mode on time	T_{HIC_ON}			2		ms
OCP hiccup mode off time	T_{HIC_OFF}			2		s
Shutdown temperature (7)	T_{STD}			150		°C
Hysteresis (7)	T_{HYS}			25		°C

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
FLT output low voltage	V_{FLT_Low}	Sink 1mA			150	mV
FLT leakage	I_{FLT_LKG}	V_{FAULT} = 4V			1	μA
BC1.2 DCP Short Mode						
DP/DM short resistance	R_{DP/DM_Short}	V_{DP} = 0.8V, I_{DM} = 1mA			40	Ω
		V_{DP} = 0.8V, I_{DM} = 1mA, full temperature			45	Ω
1.2V/1.2V Mode						
DP/DM output voltage	$V_{DP/DM\_1.2V}$		1.1	1.2	1.3	V
DP/DM output impedance	$R_{DP/DM\_1.2V}$		200	300	400	kΩ
Divider Mode						
DP/DM output voltage	$V_{DP/DM}$	V_{IN} = V_{OUT} = 5V	2.50	2.70	2.85	V
DP/DM output impedance	$R_{DP/DM}$		20	26	32	kΩ
Quick Charge 3.0 Mode						
Data detect voltage	V_{DAT_REF}		0.25	0.30	0.40	V
Output voltage select reference	V_{SEL_REF}		1.8	2.0	2.2	V
DP output impendence	R_{DP_QC}		300	400	1500	kΩ
DM output impendence	R_{DM_QC}		13	20	27	kΩ
DM low glitch time (7)	T_{Glitch_DM}			10		ms
DP high glitch time	T_{Glitch_DP}		800	1200	1600	ms
Output voltage change glitch time	$T_{Glitch\_V\_Change}$		20	40	60	ms
Bus voltage step	$V_{BUS\_CONT\_STEP}$		150	200	250	mV
Time for V_{BUS} to discharge to 5V when DP < 0.6V (7)	T_{V_UNPLUG}				500	ms
USB Type-C 5V/3A Mode – Both CC1 and CC2 Pins						
CC resistor to disable Type-C mode	R_A	CC1 pin	90		100	kΩ
CC voltage to enable V_{CONN}	V_{Ra}				0.75	V
CC voltage to enable V_{BUS}	V_{Rd}	Use 0.8V and 2.6V as threshold	0.85		2.45	V
CC detach threshold	V_{OPEN}	Use 2.6V as threshold	2.75			V
CC voltage at 5.1kΩ Rd	V_{CC_Rd}	CC pin pull-down by 5.1kΩ	1.310	1.683	2.040	V
CC voltage falling debounce timer	$T_{CC\_debounce}$	V_{BUS} enable deglitch	100	130	200	ms
CC voltage rising debounce timer	$T_{PD\_debounce}$	V_{BUS} disable deglitch	10	15	20	ms

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, T_J = -40°C to 125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{CONN} output power	P_{VCONN}	V_{CONN} comes from MPQ5029-C input with some series resistance	1			W
V_{BUS} to ground impedance	R_{BUS}	Type-C detach, after output discharge turn-off	72.4			kΩ
CDP MODE						
DM CDP output voltage	V_{DM_SRC}	V_{DP} = 0.6V	0.50	0.64	0.70	V
V_{DM_SRC} impedance	R_{VDM_SRC}	VDM output 0.64V		0.3	0.5	kΩ
		Sink 20mA		1		kΩ
DP rising lower window threshold for V_{DM_SRC} activation	V_{DAT_REF}	50mV hysteresis	0.340	0.375	0.410	V
DP rising upper window threshold for V_{DM_SRC} de-activation	V_{LGC_SRC}	100mV hysteresis	0.78	0.83	0.88	V
V_{DM_SRC} on/off deglitch time	$V_{DM\_SRC\_Degh}$			5		ms
RDP_Down	R_{DP_Down}		14.25	19.50	24.80	kΩ
DP/DM switch on resistance	$R_{ON\_DP/DM}$			4	7	Ω
DP to DP_OUT SW on capacitor (7)	C_{DP}	Same for DM switch		9		pF
3dB bandwidth of analog data SW (7)	f_{BW}		500			MHz

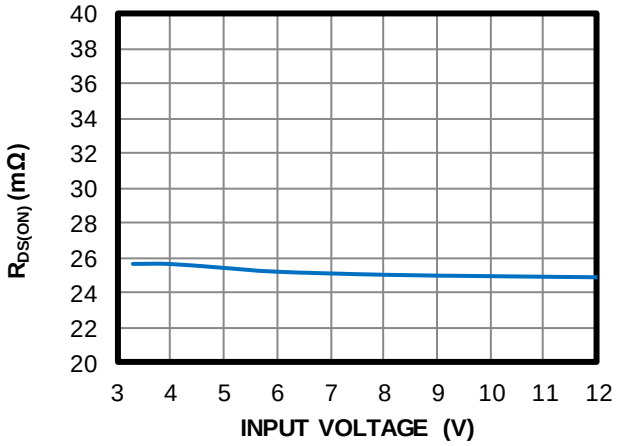
Note:

7) Guaranteed by engineering sample characterization.

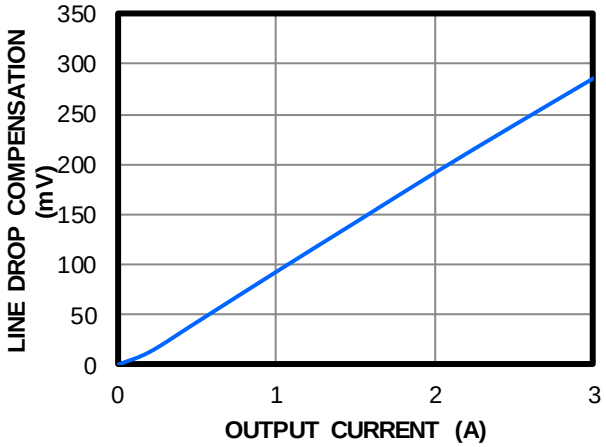
TYPICAL CHARACTERISTICS

V_{IN} = 5V, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

$R_{DS(ON)}$ vs. Input Voltage



Line Drop Compensation vs. Output Current

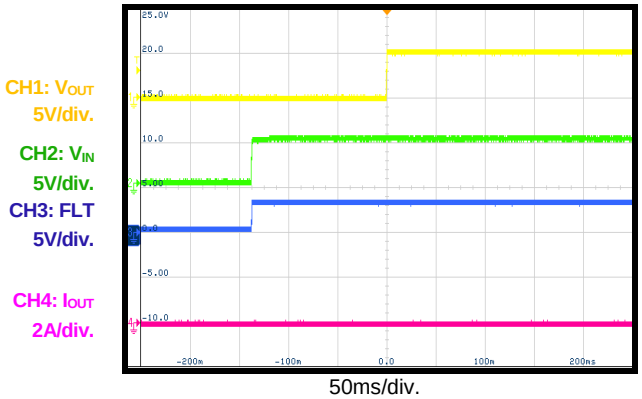


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, T_A = 25°C, Type-C mode, CC1 pull-down by 5.1kΩ resistor, unless otherwise noted. Connect the MPQ5029-C input V_{IN} to the MPQ4483 output. System_V_{IN} = 14V is the input of the MPQ4483.

Start-Up through Input Voltage

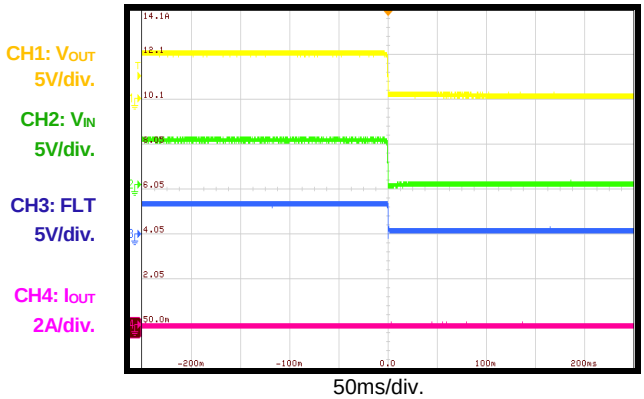
I_{OUT} = 0A



50ms/div.

Shutdown through Input Voltage

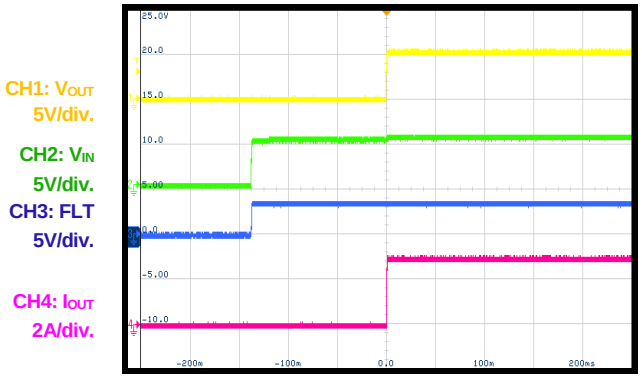
I_{OUT} = 0A



50ms/div.

Start-Up through Input Voltage

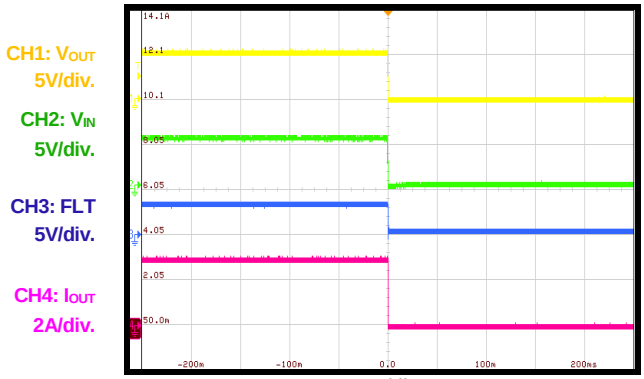
I_{OUT} = 3A



50ms/div.

Shutdown through Input Voltage

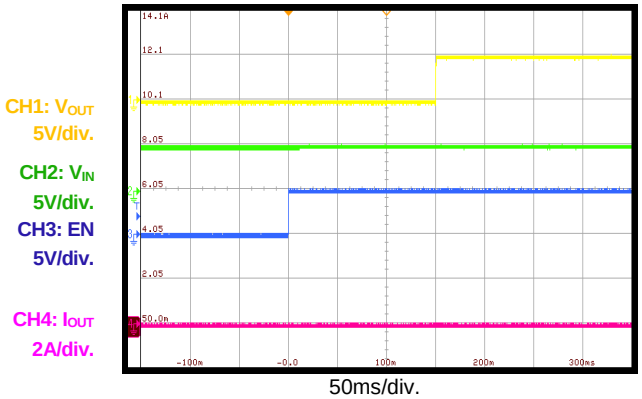
I_{OUT} = 3A



50ms/div.

EN Start-Up

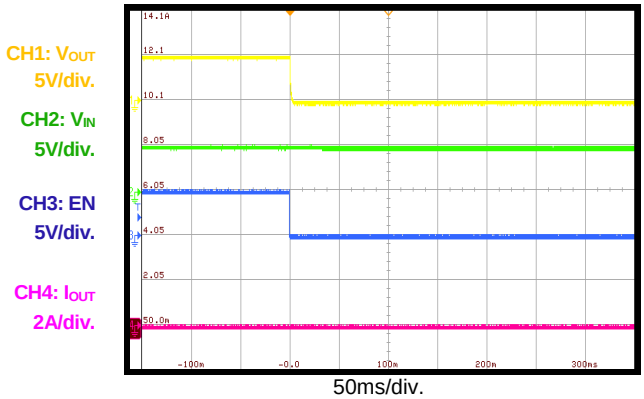
I_{OUT} = 0A



50ms/div.

EN Shutdown

I_{OUT} = 0A



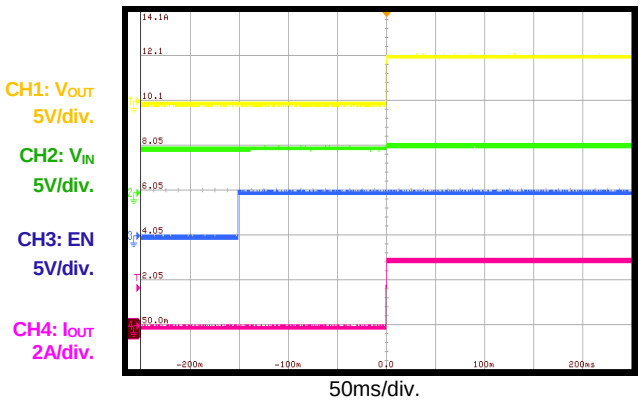
50ms/div.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, T_A = 25°C, Type-C mode, CC1 pull-down by 5.1kΩ resistor, unless otherwise noted. Connect the MPQ5029-C input V_{IN} to the MPQ4483 output. System_V_{IN} = 14V is the input of the MPQ4483.

EN Start-Up

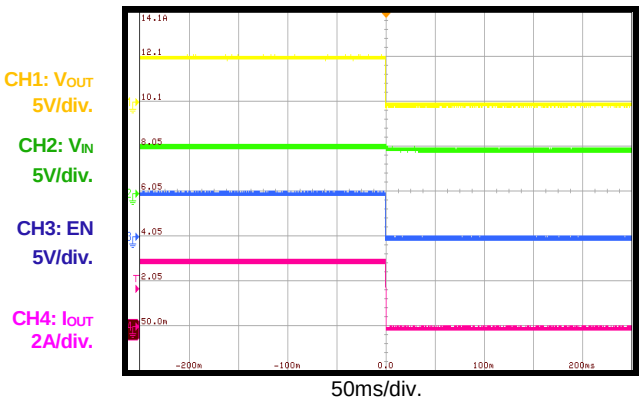
I_{OUT} = 3A



50ms/div.

EN Shutdown

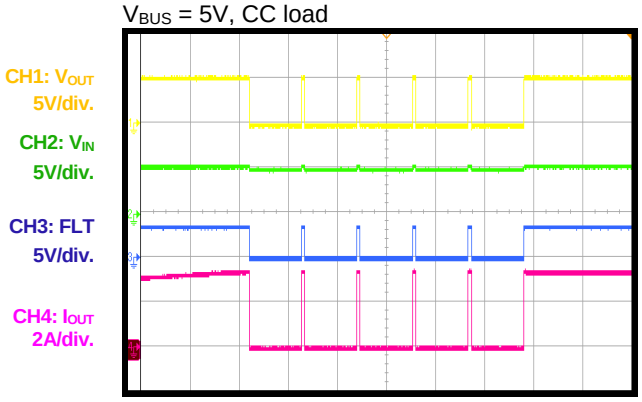
I_{OUT} = 3A



50ms/div.

Over-Current Protection Entry and Recovery

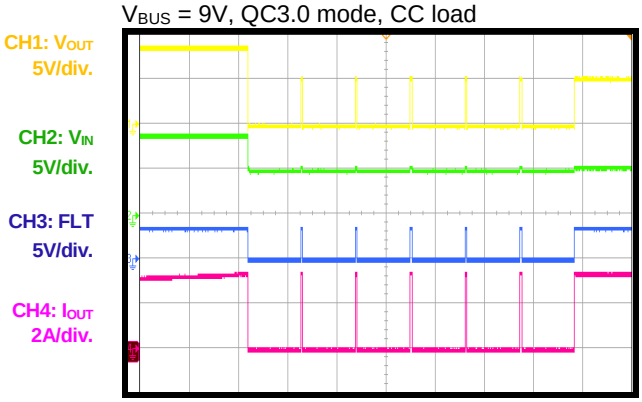
V_{BUS} = 5V, CC load



2s/div.

Over-Current Protection Entry and Recovery

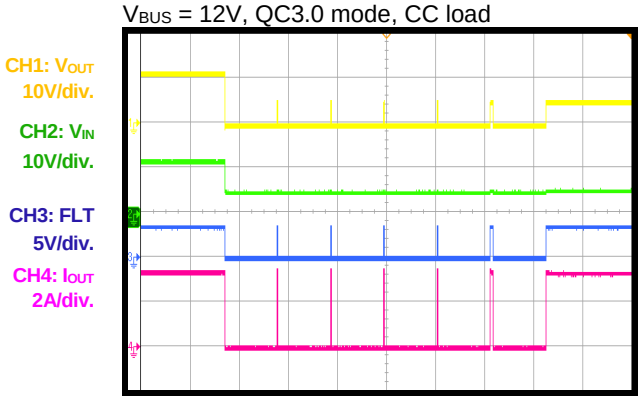
V_{BUS} = 9V, QC3.0 mode, CC load



2s/div.

Over-Current Protection Entry and Recovery

V_{BUS} = 12V, QC3.0 mode, CC load



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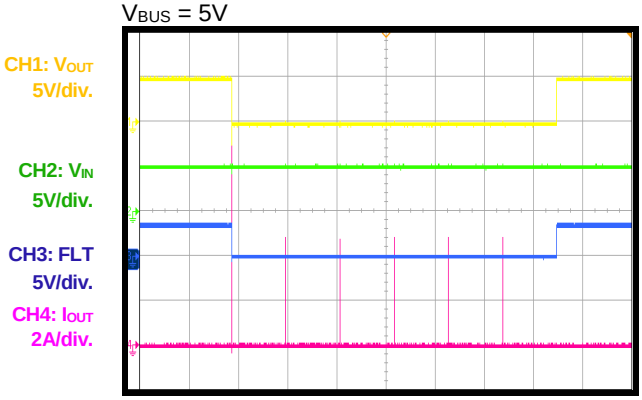
Short-Circuit Protection Entry and Recovery

V_{BUS} = 5V



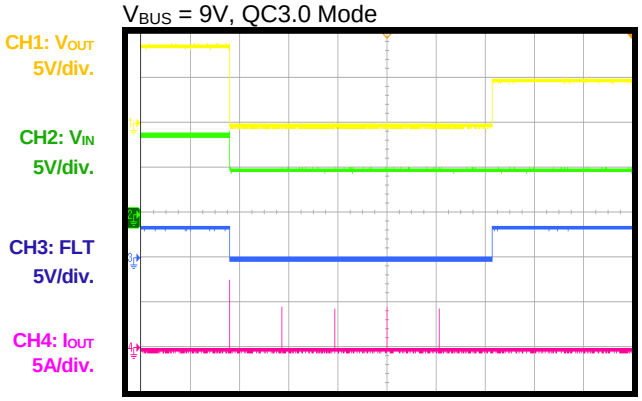
2s/div.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, T_A = 25°C, Type-C mode, CC1 pull-down by 5.1kΩ resistor, unless otherwise noted. Connect the MPQ5029-C input V_{IN} to the MPQ4483 output. System_V_{IN} = 14V is the input of the MPQ4483.

Short-Circuit Protection Entry and Recovery

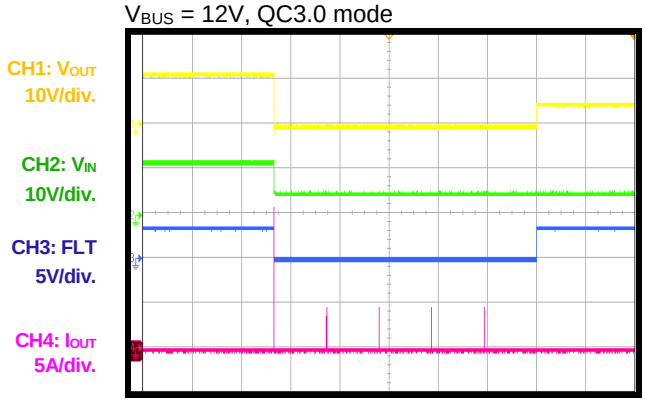
V_{BUS} = 9V, QC3.0 Mode



2s/div.

Short-Circuit Protection Entry and Recovery

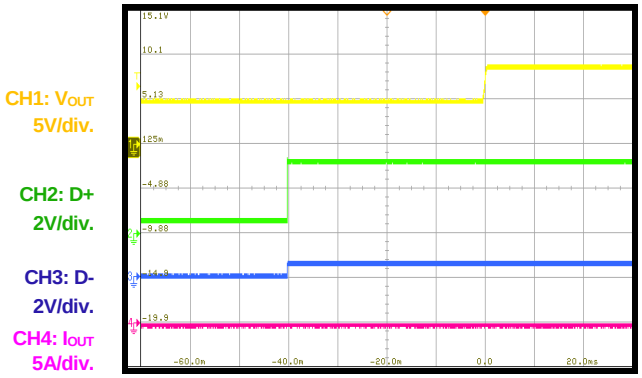
V_{BUS} = 12V, QC3.0 mode



2s/div.

Mode Transition from 5V to 9V

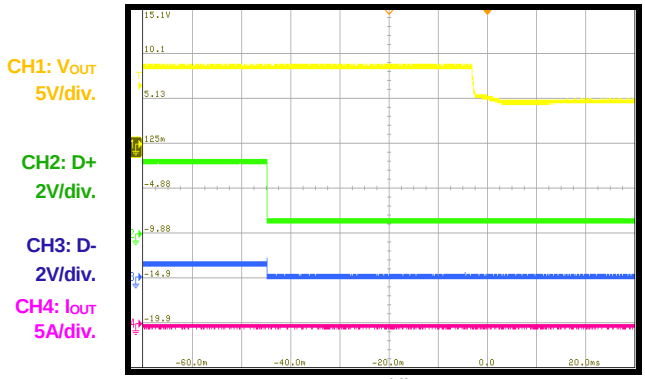
I_{OUT} = 0A, from QC 2.0_5V to 9V



10ms/div.

Mode Transition from 9V to 5V

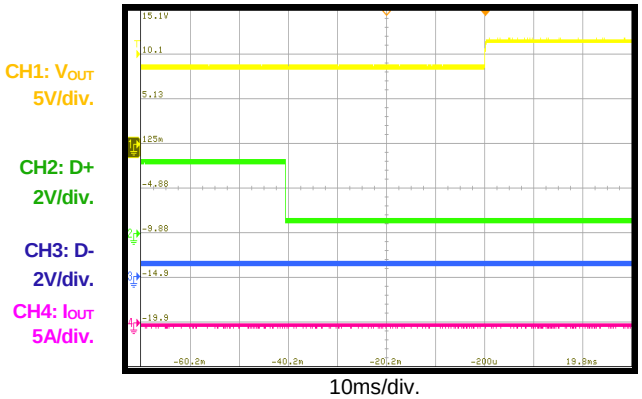
I_{OUT} = 0A, from QC 2.0_9V to 5V



10ms/div.

Mode Transition from 9V to 12V

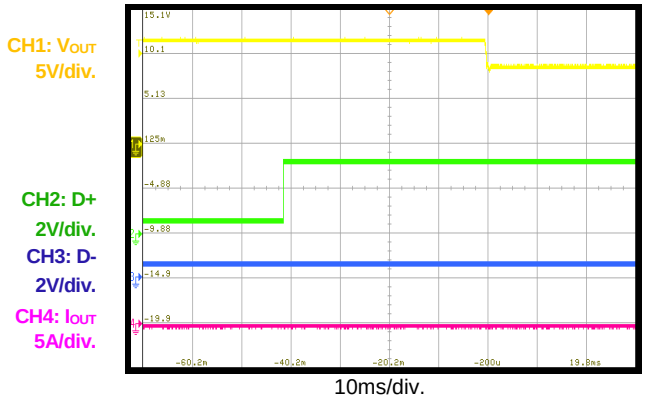
I_{OUT} = 0A, from QC 2.0_9V to 12V



10ms/div.

Mode Transition from 12V to 9V

I_{OUT} = 0A, from QC 2.0_12V to 9V



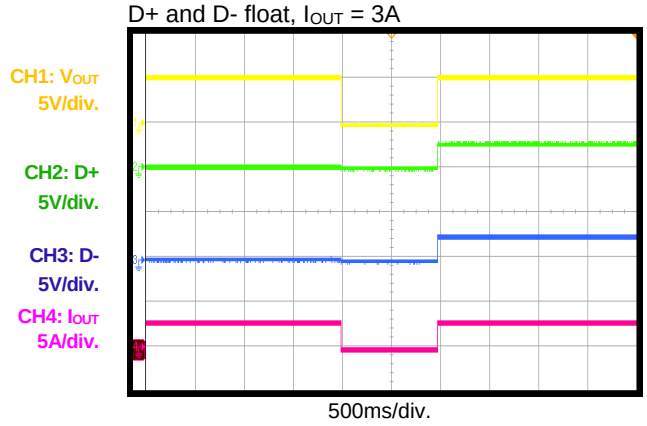
10ms/div.

TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, T_A = 25°C, Type-C mode, CC1 pull-down by 5.1kΩ resistor, unless otherwise noted. Connect the MPQ5029-C input V_{IN} to the MPQ4483 output. System_V_{IN} = 14V is the input of the MPQ4483.

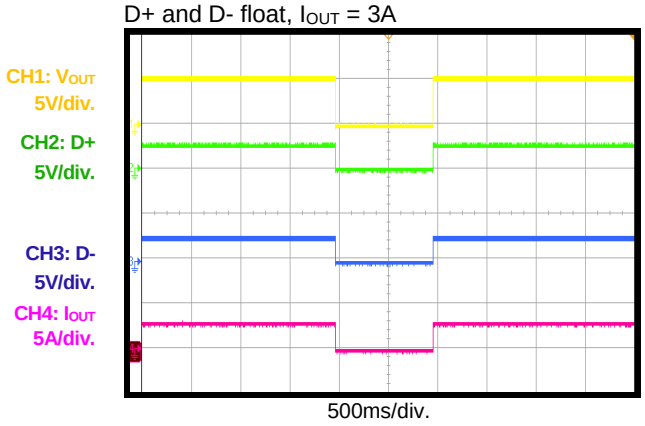
MODE Pin Changes from GND to Float

D+ and D- float, I_{OUT} = 3A



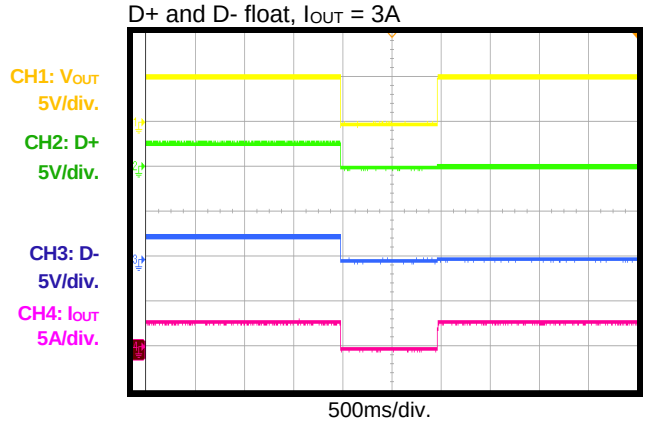
MODE Pin Changes from Float to VCC

D+ and D- float, I_{OUT} = 3A



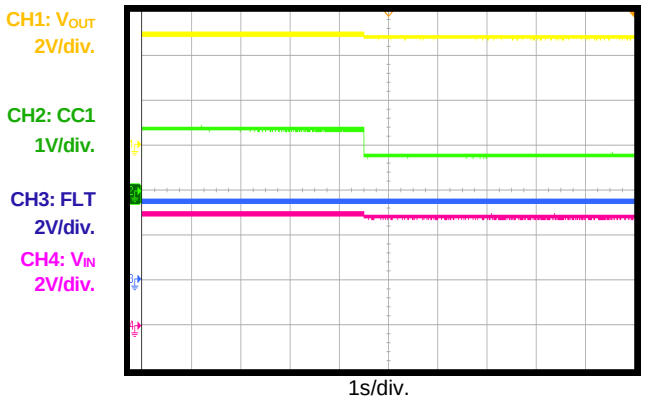
MODE Pin Changes from VCC to GND

D+ and D- float, I_{OUT} = 3A



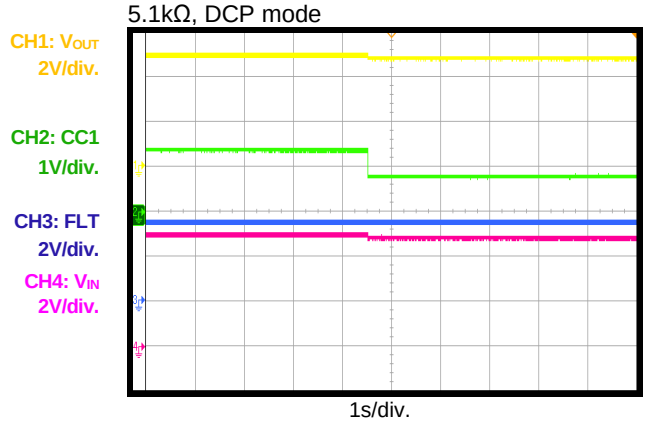
Load Shedding Entry

Buck output set to 4.9V, V_{BUS} = 5V, CC1 = 5.1kΩ, CDP mode



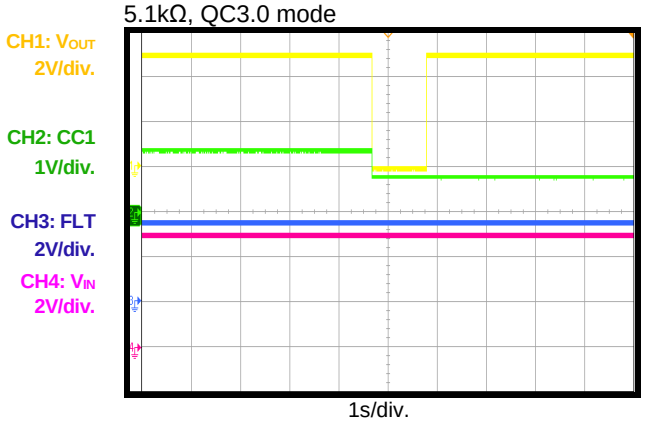
Load Shedding Entry

Buck output set to 4.9V, V_{BUS} = 5V, CC1 = 5.1kΩ, DCP mode



Load Shedding Entry

Buck output set to 3.6V, V_{BUS} = 5V, CC1 = 5.1kΩ, QC3.0 mode

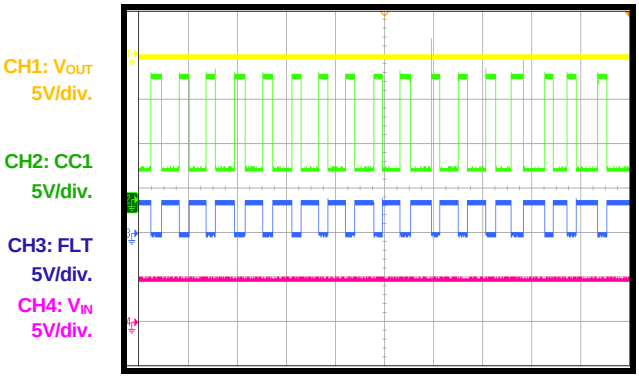


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, T_A = 25°C, Type-C mode, CC1 pull-down by 5.1kΩ resistor, unless otherwise noted. Connect the MPQ5029-C input V_{IN} to the MPQ4483 output. System_V_{IN} = 14V is the input of the MPQ4483.

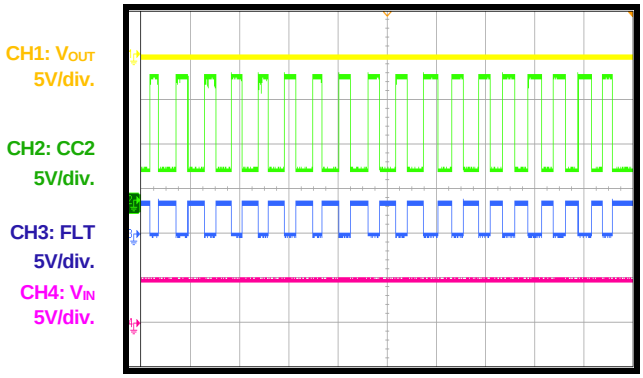
CC1 Short to Battery

$V_{BATTERY}$ = 14V, CC2 float



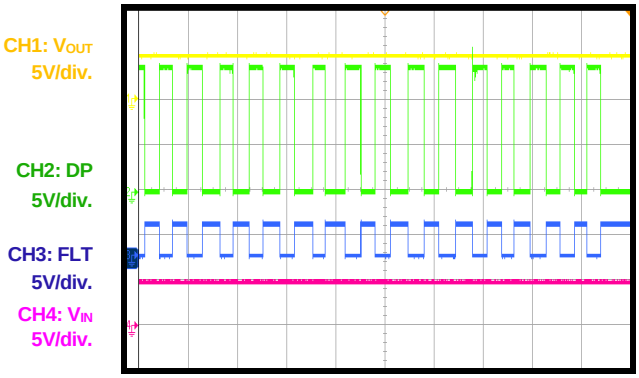
CC2 Short to Battery

$V_{BATTERY}$ = 14V, CC1 float



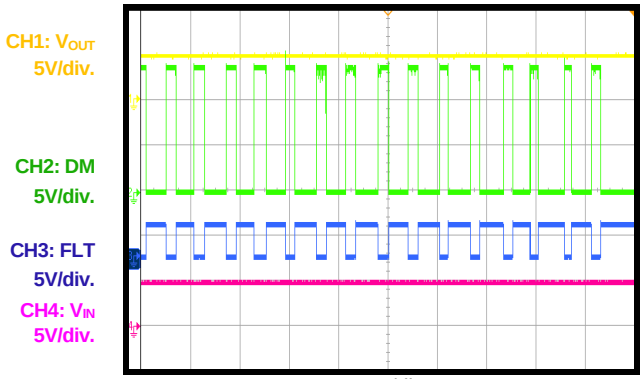
DP Short to Battery

$V_{BATTERY}$ = 14V, CC1 = 5.1kΩ, GND mode



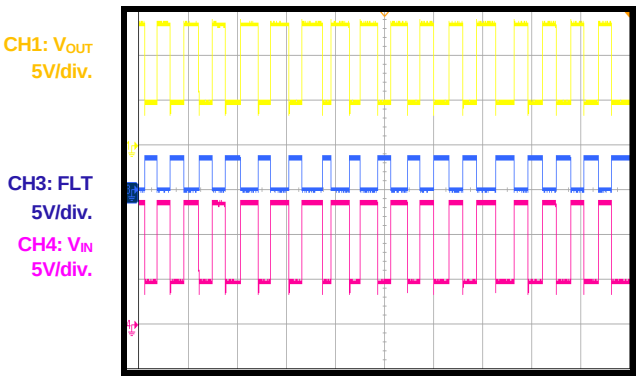
DM Short to Battery

$V_{BATTERY}$ = 14V, CC1 = 5.1kΩ, GND mode



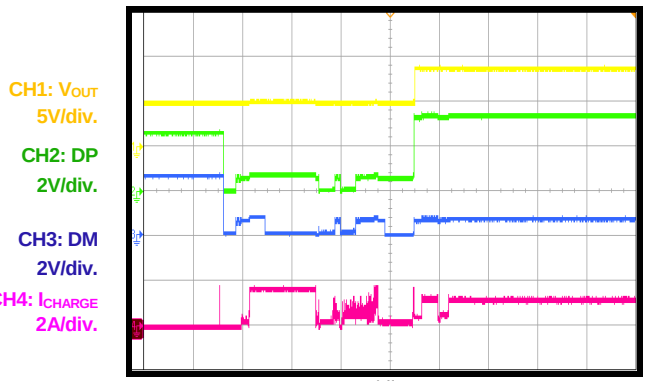
VOUT Short to Battery

$V_{BATTERY}$ = 14V, CC1 = 5.1kΩ



QC 3.0 Device Charging Test

Mobile phone plug-in

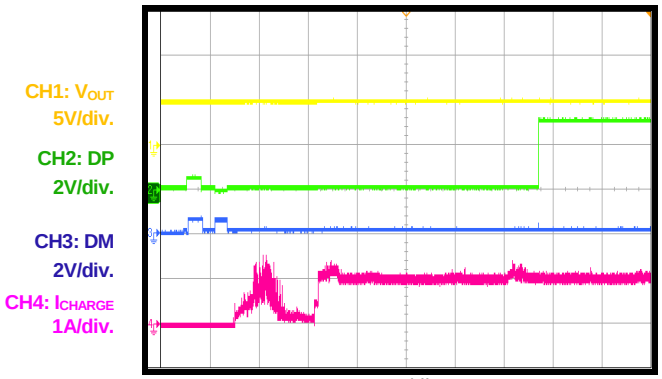


TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 5V, T_A = 25°C, Type-C mode, CC1 pull-down by 5.1kΩ resistor, unless otherwise noted. Connect the MPQ5029-C input V_{IN} to the MPQ4483 output. System_V_{IN} = 14V is the input of the MPQ4483.

CDP Mode Detection

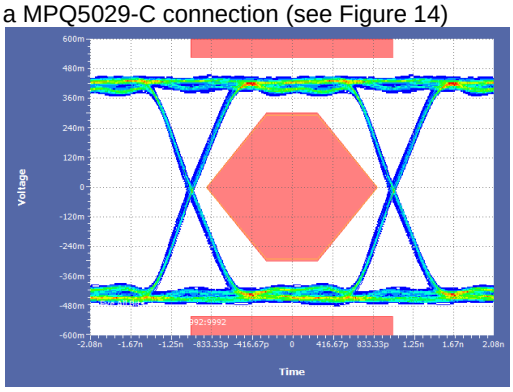
Mobile phone plug-in



200ms/div.

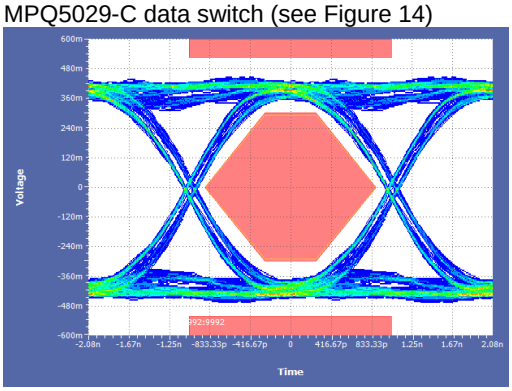
Eye Diagram

Measured on an EVB by a 50cm cable, without a MPQ5029-C connection (see Figure 14)



Eye Diagram

Measured on an EVB by a 50cm cable, with a MPQ5029-C data switch (see Figure 14)



FUNCTIONAL BLOCK DIAGRAM

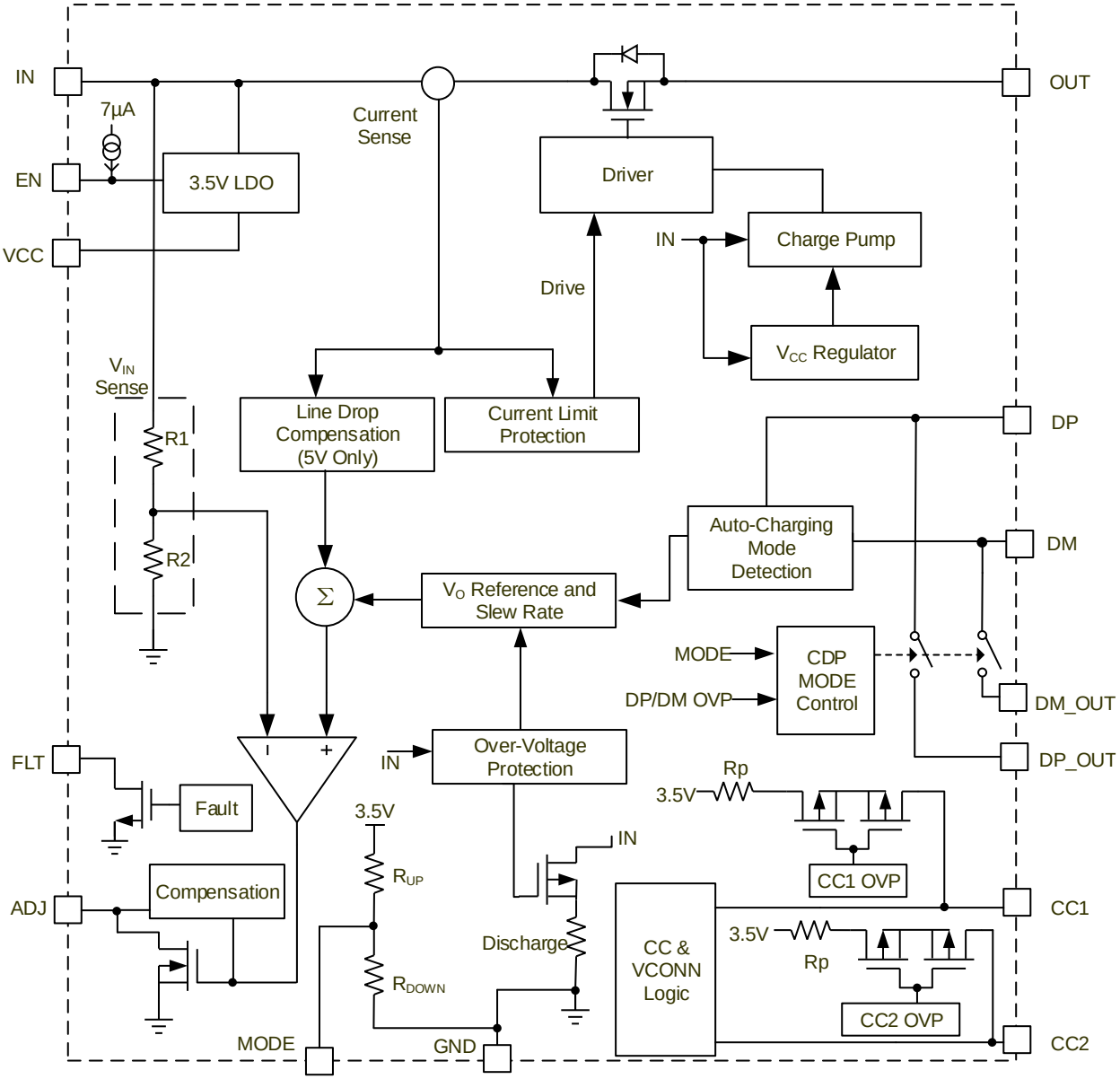


Figure 1: Functional Block Diagram

OPERATION

The MPQ5029-C integrates a USB current limit switch and charging port identification circuits. It achieves 3A of continuous output current over a wide input supply range.

The MPQ5029-C supports quick-charge specification (QC3.0), and is compatible with QC2.0. The MPQ5029-C also supports CDP and DCP schemes for battery-charging specification (BC1.2), divider mode, and 1.2V/1.2V mode without the need for external user interaction.

The MPQ5029-C also supports Type-C 5V @ 3A DFP mode.

The part provides line drop compensation for a 5V output. Full protection features include hiccup current limiting, input over-voltage protection (OVP), thermal shutdown, and short-to-battery protection.

Operation Supply Voltage

The MPQ5029-C has a two-stage input voltage threshold. The first threshold is about 3V, and the second threshold is the under-voltage lockout (UVLO) of the power MOSFET. When V_{IN} is higher than the first threshold, the MPQ5029-C's ADJ block turns on, which sinks a current to adjust the upstream regulator's output to an accurate 5.1V (typical). After this process, the MPQ5029-C enables the power MOSFET and enters a fully working state.

Under Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MPQ5029-C's second UVLO comparator monitors the input voltage. Once the input voltage is higher than the second UVLO threshold (about 3.1V), the power MOSFET turns on at a controlled slew rate after a fixed delay.

Internal Soft Start (SS)

The internal soft start prevents inrush current and keeps the output voltage from overshooting during start-up.

Enable Control (EN)

The MPQ5029-C has an enable control pin (EN). The MPQ5029-C has an internal 7μA pull-up current that allows EN to be floated for auto-start-up. Pull EN high or float EN to enable the IC. Pull EN low to disable the IC.

Apply a mid-level voltage (0.8V to 1.8V) to EN to force the chip to enter client mode. In client mode, the USB switch is off, but the DP/DM high speed data switch is on.

EN is clamped internally using a 4V Zener diode (see Figure 2). When connecting the EN to >4V VIN through a pull-up resistor, limit the EN input current to less than 250μA. Connecting EN directly to a voltage source without a pull-up resistor requires limiting the voltage amplitude to less than 4V.

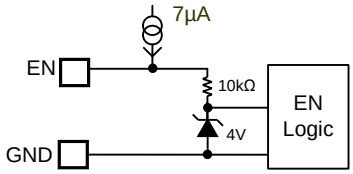


Figure 2: Zener Diode between EN and GND

QC Mode Voltage Transition – Class A

If the downstream device of the MPQ5029-C supports QC specification, the device can support output voltages higher than 5V via DM and DP communication. If a higher USB output voltage is required, use the ADJ pin. Typically, ADJ is connected to the FB pin of the upstream voltage converter. After the handshake, the MPQ5029-C sinks a controlled ADJ current gradually to adjust V_{OUT} to 9V, 12V, or any other voltage (e.g. 200mV). Because of the MPQ5029-C's smart controller mode, only one ADJ pin is needed to set different high-voltage values and meet the QC specification. The output voltage transition is smooth with no undershoot or overshoot (see Figure 3 and Table 1).

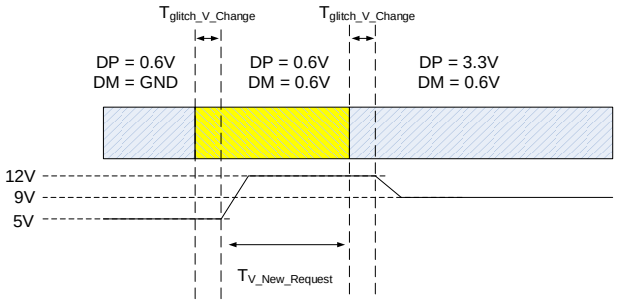


Figure 3: QC Mode Transition

Table 1: QC Mode Definition

Portable Device		USB Output Voltage
DP	DM	
0.6V	0.6V	12V
3.3V	0.6V	9V
0.6V	3.3V	3.6V to 12V/200mV step according to QC3.0
3.3V	3.3V	No action
0.6V	GND	5V

When the downstream device is removed, V_{OUT} returns to the default 5V automatically. The input-to-ground discharge resistor helps perform this procedure quickly.

Line Drop Compensation

The MPQ5029-C can compensate for an output voltage drop, such as high resistance caused by a long trace, to maintain a fairly constant 5V load-side voltage. The line drop compensation is only active at 5V V_{IN}, and increases the input voltage by 285mV at 3A output current (see Figure 4).

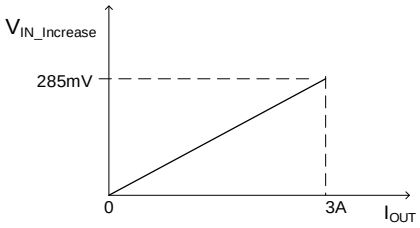


Figure 4: Line Drop Compensation

The line drop compensation is realized through ADJ. The ADJ voltage (V_{ADJ}) sinks a controlled current slowly. The line drop compensation amplitude increases linearly as the load current increases.

In no-load condition, if the input voltage is lower than the typical 5.1V, ADJ sinks a current to regulate the upstream regulator's output voltage to 5.1V. If the input voltage is higher than 5.1V, the MPQ5029-C no longer regulates the input voltage. For a quick load transient response, configure R1/R2 to allow the default output voltage to be less than 5.1V, maintaining that ADJ works continuously.

Figure 5 shows typical ADJ configuration. The ADJ sink current capability is 500μA. ADJ requires a feedback current through R1 of less than 500μA. Calculate R1 with Equation (1):

$$R1(k\Omega) > \frac{\Delta V(V)}{0.5} \quad (1)$$

Where ΔV is the maximum line drop compensation value plus the difference in voltage between 5.1V and the buck voltage.

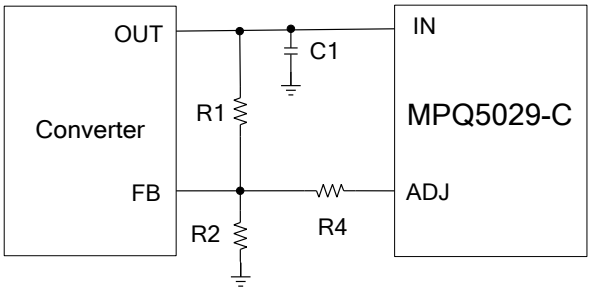


Figure 5: ADJ Configuration

There is another V_{ADJ} configuration to limit the maximum output voltage by inserting a resistor (R4) between FB and V_{ADJ}. With R4, the maximum output voltage can be limited with Equation (2):

$$V_{OUT\_Max}(V) = \frac{R_1 + R_2 // R_4}{R_2 // R_4} \times V_{FB}(V) \quad (2)$$

After adding R4, the maximum ADJ sink current is limited with Equation (3):

$$I_{ADJ\_Max}(\mu A) = \frac{V_{FB} - V_{OFFSET}(mV)}{R_4(k\Omega)} \quad (3)$$

Where V_{OFFSET} is about 100mV.

Input Over-Voltage and Discharge

To protect the downstream device over-voltage, the MPQ5029-C provides an input OVP discharge function. Because the MPQ5029-C supports QC3.0 protocol, it has a dynamic over-voltage protection threshold.

An accurate and fast comparator monitors the over-voltage condition of the input. If the input voltage rises above the threshold, the power MOSFET remains on, while the input-to-ground discharge path is active. When the input voltage falls below the typical 5.45V, the MPQ5029-C exits OVP mode.

The input-to-ground discharge resistance is always active during high-to-low voltage change mode. This resistance is disabled when FB is less than 108% of V_{REF} with a 20ms delay and

OV is removed (see Figure 6).

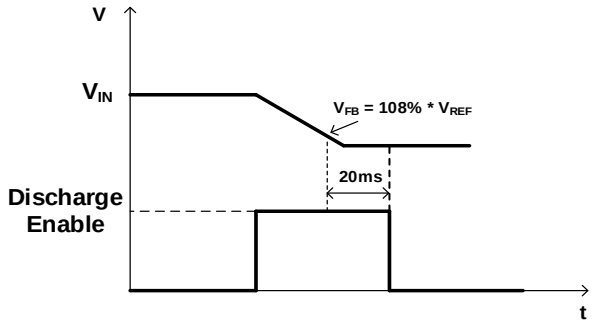


Figure 6: Input Discharge During High Voltage to Low Voltage Transition

QC mode is reset during the OVP rising edge.

Over-Current Protection

Once the device reaches its current limit threshold, the internal circuit regulates the gate voltage to hold the current in the power MOSFET constant (see Figure 7). If the over-current condition lasts longer than 2ms, the MPQ5029-C enters hiccup mode.

In hiccup mode, the MPQ5029-C turns off the power MOSFET. For QC mode, it resets to 5.1V, ADJ changes V_{IN} to 5.1V, V_{IN} OVP may occur, the QC logic resets, and the discharge resistor turns on. After the hiccup off timer (2s), the MPQ5029-C restarts to check if OC is still present. QC logic releases when the hiccup signal disappears.

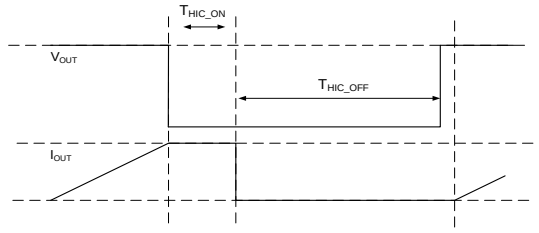


Figure 7: Over-Current Protection

Short-Circuit Protection (SCP)

If the load current increases rapidly due to a short circuit, the current may greatly exceed the current-limit threshold before the control loop can respond. If the current reaches an internal secondary current-limit level (about 9A), a fast turn-off circuit activates to turn off the power MOSFET. This limits the peak current through the switch to limit the input voltage drop. Afterward, the power MOSFET turns on again if the part is still in a short-circuit condition. The MPQ5029-C treats this as an over-current condition, and enters hiccup mode or thermal shutdown. After the short-circuit condition is removed, the MPQ5029-C recovers automatically.

If V_{IN} > 9V and the operation mode is CDP or DCP mode (non-QC3.0), the MPQ5029-C does not support output short-circuit protection (SCP). It does support output SCP when the operation mode is QC3.0 with V_{IN} > 9V. In this case, V_{IN} automatically changes to 5.1V (typical) once SCP is triggered.

Short-to-Battery Protection

The MPQ5029-C provides CC1, CC2, DP, DM, and OUT short-to-battery protections when the IC is enabled.

The MPQ5029-C has a high internal voltage rating. During a CC1/CC2 or DP/DM short-to-battery condition, the MPQ5029-C can withstand high voltage on the internal components. Additionally, the ESD breakdown voltage is much larger than the battery voltage.

During a 5V USB output short-to-battery condition, the USB input rises up to trigger OVP, and the USB input discharge path turns on.

When the MPQ4483 is used as a buck regulator, the buck output capacitor should be placed between the buck output and PGND, instead of RGND (see Figure 8).

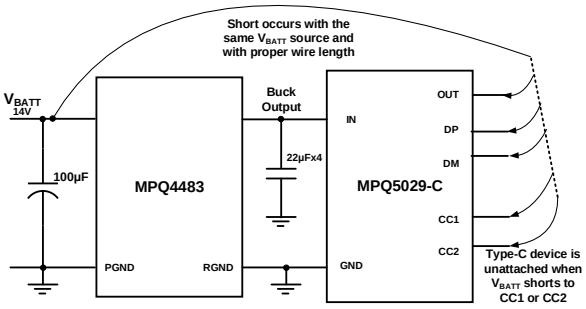


Figure 8: Short-to-Battery Set-Up

Fault Indication

FLT is the fault indication pin. FLT is in open-drain state during shutdown, start-up, and normal operation It asserts (logic low) during over-current, input over-voltage, DP/DM pin over-voltage, CC1/CC2 pin over-voltage, or

over-temperature condition. FLT asserts low until the fault condition is removed, and the

USB output voltage goes back to high. There is a 2ms deglitch timer during an over-current condition to prevent an FLT false trigger. If the over-current condition lasts for 2ms, FLT goes low. The FLT signal is not deglitched during over-voltage and over-temperature conditions.

Mode Selection

The MPQ5029-C supports DCP and CDP mode through MODE pin control (see Table 2). The MODE pin logic level can be changed dynamically when the MPQ5029-C is working. There are three logic levels: pull to ground, float pin, and tie to VCC. If MODE is connected to GND, CDP mode is selected. In CDP mode, the USB output voltage is always about 5V with current limit and line drop compensation. If MODE is connected to VCC, DCP mode is selected, QC3.0 is enabled, and line drop compensation is active for 5V. If MODE is left floating, DCP mode is selected, QC3.0 is disabled, and line drop compensation is active for 5V.

In DCP mode, the MPQ5029-C provides power for USB devices with protocol auto-detection, and supports the following charging schemes:

- USB Battery Charging Specification BC1.2 / Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- Type-C 5V @ 3A DFP mode

In QC3.0 mode, the MPQ5029-C provides power for portable devices, and supports the following charging schemes:

- USB Battery Charging Specification BC1.2 / Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider mode
- 1.2V/1.2V mode
- Type-C 5V @ 3A DFP mode
- Quick charge 3.0/2.0

Table 2: MODE Pin Selection

MODE Pin Status	Supported Charge Mode
Logic High	DCP mode with QC function, divider mode, 1.2V/1.2V mode, $5V_{OUT}$ with line drop compensation
Float	DCP mode without QC function, divider mode, 1.2V/1.2V mode, $5V_{OUT}$ with line drop compensation
GND	CDP mode, $5V_{OUT}$ with line drop compensation

CDP Mode

The MPQ5029-C supports charging downstream port (CDP) mode in compliance with the USB2.0 definition of a host or a hub.

DM outputs a 0.64V voltage when DP is forced with 0.6V, and DP does not output any voltage when DM is forced with 0.6V.

Client Mode

The MPQ5029-C supports client mode operation. This mode is useful when upgrading software through a USB port (see Figure 9)

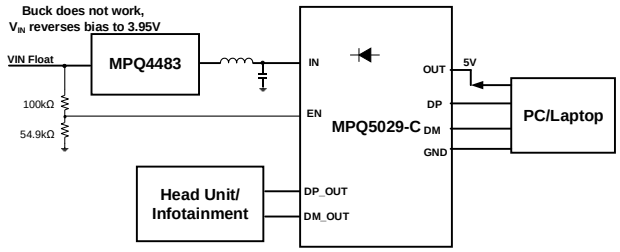


Figure 9: Client Mode

In this case, OUT is powered by an external 5V USB bus voltage, but the system input has no supply (see Figure 9). The MPQ5029-C USB switch shuts down due to low EN voltage (set by the EN divider resistors), and the DP/DM data switches turn on when their EN is higher than the MOSFET V_{GS} threshold. An external host (e.g. laptop) can read and update head unit software. Under this condition, V_{IN} is biased to about 3.95V through the USB switch and buck high-side body diode. Ensure other units on the same V_{IN} line do not start up.

USB Type-C Mode and VCONN

For USB Type-C solutions, two pins on the connector (CC1 and CC2) are used to establish and manage the source-to-sink connection. The

general concept for setting up a valid connection between a source and sink is based on being able to detect terminations residing in the product being attached. To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd = 5.1kΩ) termination model is used based on a pull-up resistor and pull-down resistor (see Figure 10).

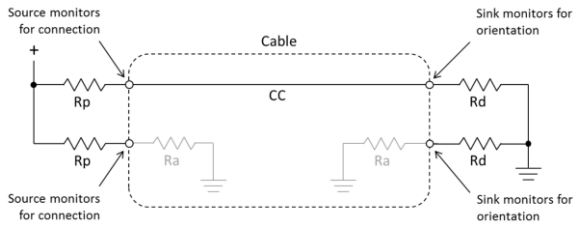


Figure 10: Pull-Up/Pull-Down CC Model

Initially, a source exposes independent Rp terminations on its CC1 and CC2 pins, and a sink exposes independent Rd terminations on its CC1 and CC2 pins. The source-to-sink combination of this circuit configuration represents a valid connection. To detect this, the source monitors CC1 and CC2 for a voltage lower than its unterminated voltage. The choice of Rp is a function of the pull-up termination voltage and the source's detection circuit. This indicates that a sink, a powered cable, or a sink connected via a powered cable has been attached.

Two termination combinations on the CC pins are defined for directly attached accessory modes: Ra/Ra for audio adapter accessory mode, and Rd/Rd for debug accessory mode. In both cases, the MPQ5029-C's V_{OUT} is disabled. See Figure 11.

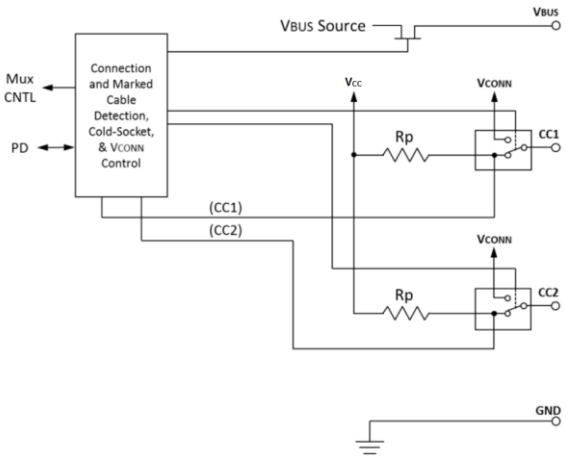


Figure 11: CC Pin Functional Block

A port that behaves as a source has the following functional characteristics:

1. The source uses a MOSFET to enable or disable the power delivery across V_{BUS}. Initially, the source is disabled.
2. The source supplies pull-up resistors (Rp) on CC1 and CC2 and monitors both to detect a sink. The presence of an Rd pull-down resistor on either CC1 or CC2 indicates that a sink is being attached. The value of Rp indicates the initial USB Type-C current level supported by the host. The MPQ5029-C default Rp is 4.7kΩ, which represents a 3A current level.
3. The source uses the CC pin pull-down characteristic to detect and determine which CC pin is intended to supply VCONN (when Ra is discovered).
4. Once a sink is detected, the source enables V_{BUS} and VCONN.
5. The source can adjust the value of Rp dynamically to indicate a change in the available USB Type-C current to a sink. For example, at high temperatures, the MPQ5029-C changes Rp to 12kΩ to indicate a 1.5A current ability.
6. The source monitors the continued presence of Rd to detect a sink detach. When a detach event is detected, the source is removed, and V_{BUS} and VCONN return to step 2.

Disable Type-C Mode (Type-A Mode)

During the MPQ5029-C's initial start-up, the IC sources 10μA for 20μs on CC1. If the CC1 voltage falls into the preset voltage range, the USB latches in Type-A mode unless the MPQ5029-C is re-enabled. Type-C mode is disabled, which means the CC attach and detach logic is disabled, and V_{BUS} is always enabled. The current limit changes to its Type-A specification.

To trigger this mode, the external pull-down resistor should be 90kΩ to 100kΩ. Do not add an extra capacitor on CC1. In normal Type-C mode applications, a 1nF capacitor should be added on CC1 to avoid falsely triggering Type-A mode.

Load Shedding vs. Temperature

When the sensed temperature is higher than 125°C, the USB port's CC pin pull-up resistance (Rp) will change to 12kΩ to advertise its source capability change (to 1.5A). The internal Rd detection threshold also changes from 0.4V to 1.6V. The Ra detection threshold changes to <0.4V. The current limit remains unchanged.

For QC mode, once the part enters load shedding, V_{BUS} restarts, then keeps working at 5V. Meanwhile, QC3.0 mode is disabled via DP/DM. For DCP mode without QC or CDP mode, once the part enters load shedding, V_{BUS} does not restart, but line drop compensation and ADJ function stop.

If the sensed temperature is lower than 85°C and lasts for 16s, USB Type-C current capability changes back to 3A (Rp = 4.7kΩ). V_{BUS} restarts with QC mode again if QC mode is selected.

In the typical Type-A application schematic, when load shedding occurs, ADJ stops working and the USB output reduces to 4.9V (set by the R1/R2 divider). This helps the Type-A downstream device reduce charge current.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 150°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 125°C), the chip is enabled again.

APPLICATION INFORMATION

COMPONENT SELECTION

Selecting the Input Capacitor

Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. 2.2μF to 22μF ceramic capacitors are recommended for most applications.

When selecting an input capacitor, be sure to consider the pre-stage converter stability. The input capacitor of the MPQ5029-C acts as the output capacitor of the converter. Ensure that the converter is stable with an additional output capacitor.

Selecting the Output Capacitor

Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended for their low ESR and small temperature coefficients. A 1μF ceramic capacitor is recommended for most applications.

Other Considerations

The upstream DC/DC converter should have a higher current limit threshold than the MPQ5029-C's current limit.

In normal Type-C mode application, a 1nF capacitor should be added on CC1 to avoid falsely triggering Type-A mode. For more details, see the Typical Application Circuit schematics on page 25.

ESD Protection for I/O Pins

A higher ESD level should be considered for all USB I/O pins. In order to further extend the DP, DM, CC1, and CC2 pins' ESD level for covering complicated application environments, an additional ESD diode should be added on all pins (see Figure 12).

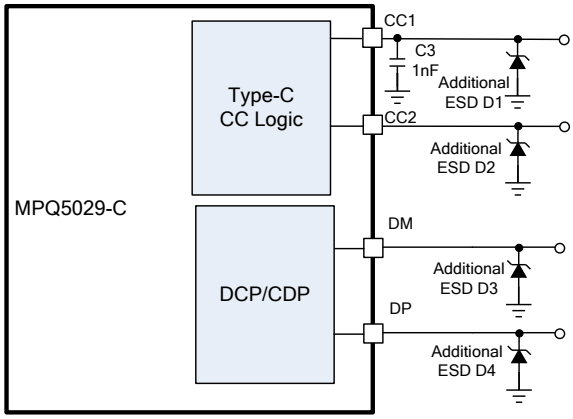


Figure 12: Recommended I/O pins ESD Enhancing

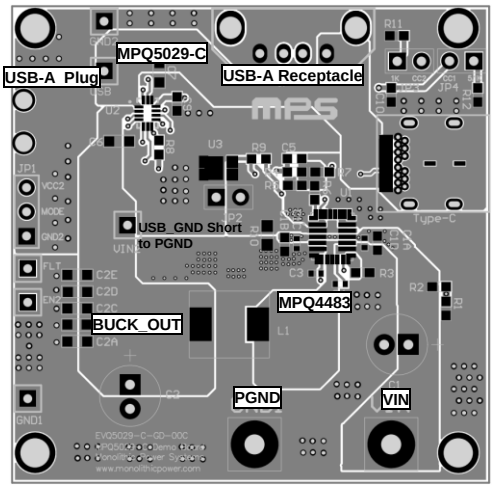
PCB Layout Guidelines [8]

Efficient PCB layout is critical for normal operation and thermal dissipation. For best results, refer to Figure 13 and follow the guidelines below:

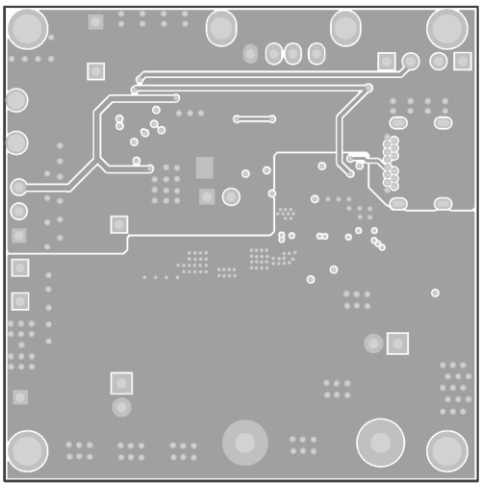
1. Use short, direct, and wide traces to connect the IC's IN/OUT pins.
2. Make the trace length between VCC and the capacitor to GND as short as possible.
3. Keep the V_{ADJ} trace to the upstream converter's FB pin as short as possible to prevent noise injection.
4. Route DP, DM, DP_OUT, and DM_OUT with differential pairs and continuous GND. Keep away from high speed signals.
5. Keep the routing as short as possible for DP, DM, DP_OUT, and DM_OUT.
6. Avoid vias and corners. Use two 45°C turns to make a single 90°C turn.

Note:

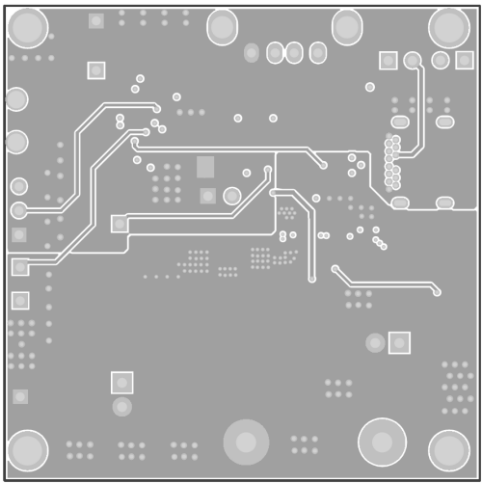
8) The recommended layout is based on the Typical Application Circuit (see Figure 17).



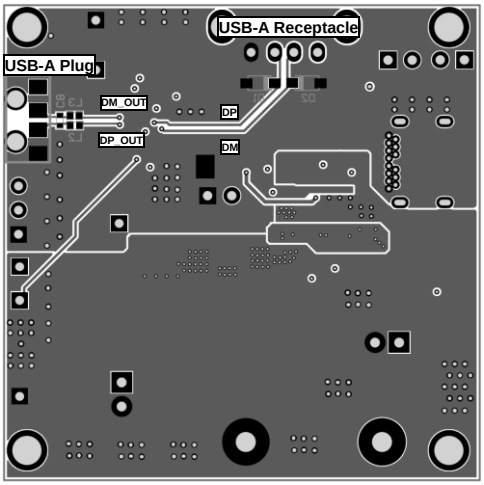
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 13: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

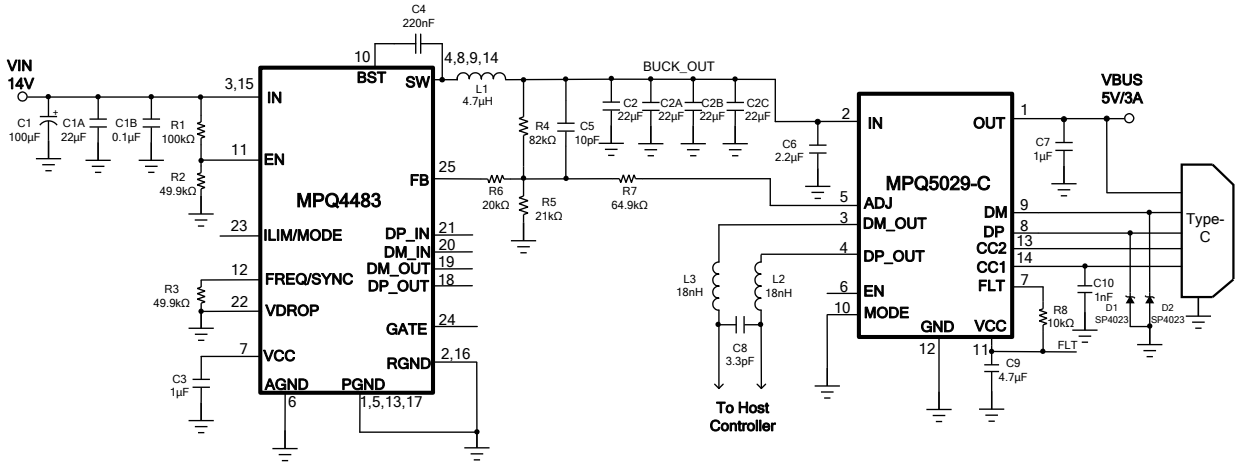


Figure 14: MPQ4483 + MPQ5029-C for Type-C Port with CDP Mode

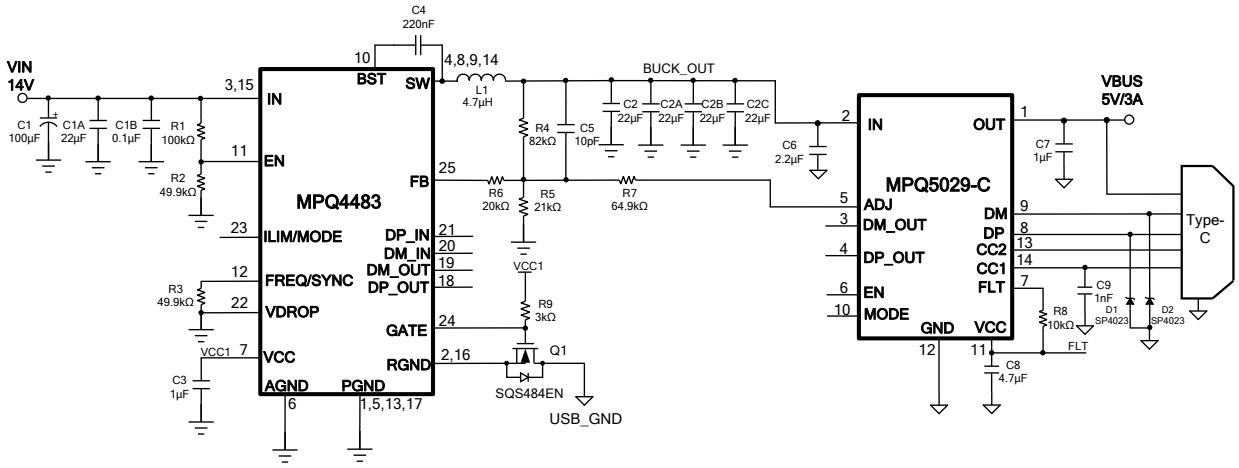


Figure 15: MPQ4483 + MPQ5029-C for Type-C Port with 5V DCP Mode (with MPQ4483 GND Short-to-Battery Protection)

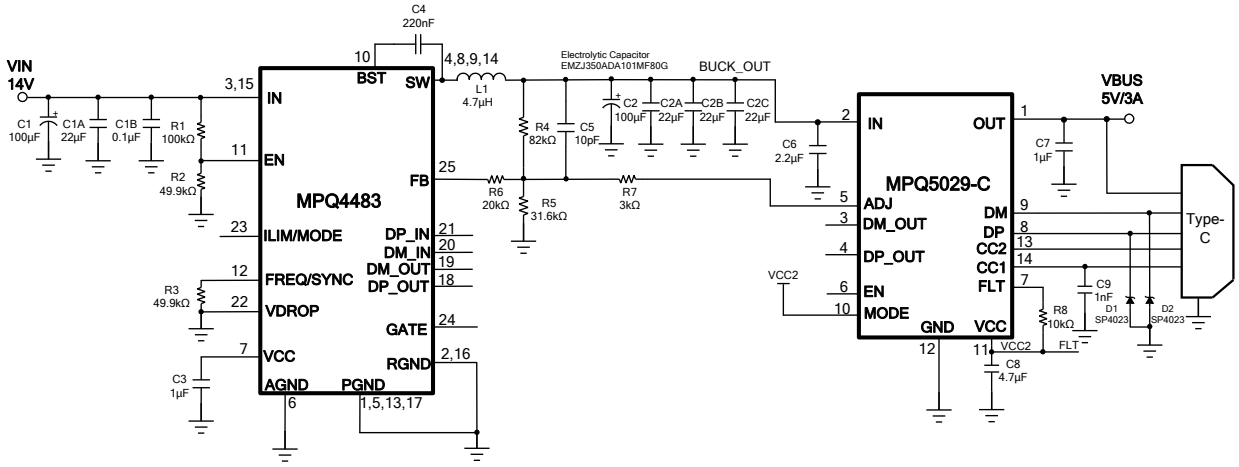


Figure 16: MPQ4483 + MPQ5029-C for Type-C Port with QC3.0

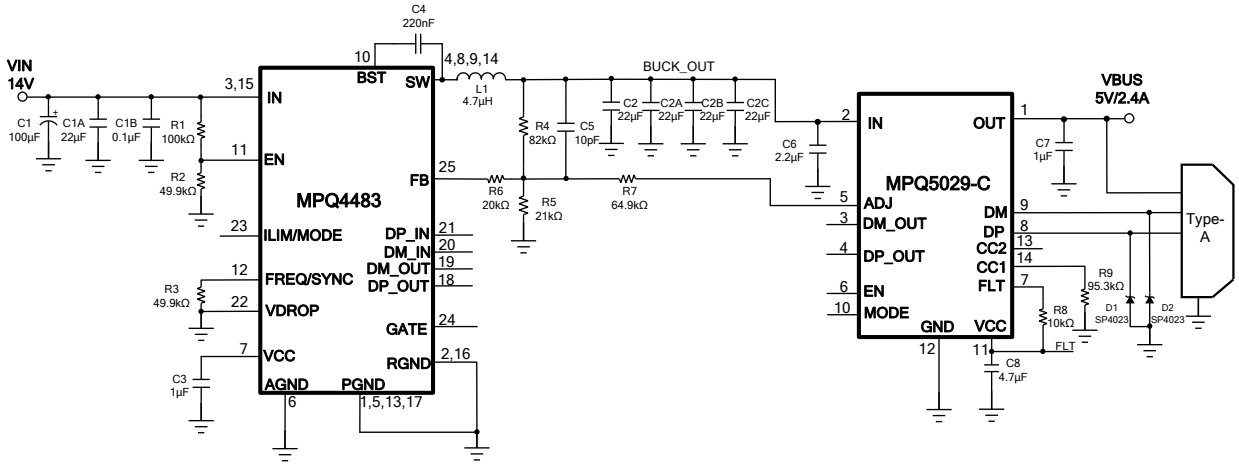
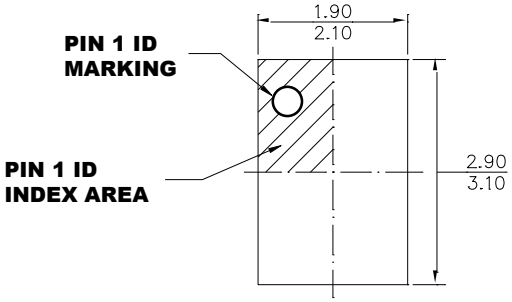


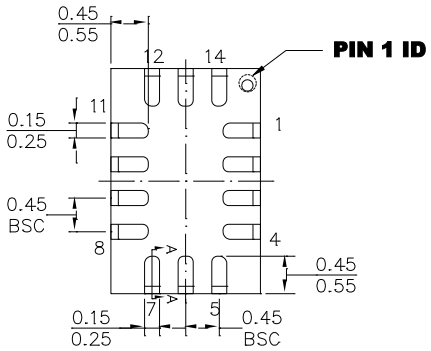
Figure 17: MPQ4483 + MPQ5029-C for Type-A Port with 5V DCP Mode

PACKAGE INFORMATION

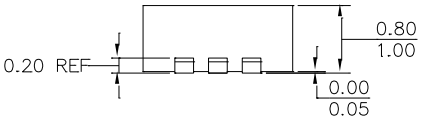
QFN-14 (2mmx3mm)



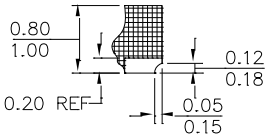
TOP VIEW



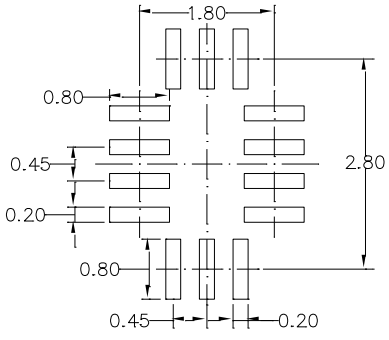
BOTTOM VIEW



SIDE VIEW



SECTION A-A



RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.