MPQ6517B

16V, Single-Phase, BLDC Motor Driver with Integrated Hall Sensor, AEC-Q100

DESCRIPTION

The MPQ6517B is a single-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-effect sensor. The device drives single-phase BLDC motors and fans with an output current (I_{OUT}) limit up to 2A. The 3.3V to 16V input voltage (V_{IN}) range and input line reverse-voltage protection (RVP) mean that an external diode is not required on the supply line.

The MPQ6517B controls the rotational speed through the pulse-width modulation (PWM) signal on the PWM pin. The MPQ6517B has a rotational speed detection feature and rotor lock fault indication on the FG/RD pin, with an open-drain output. The output speed vs. input duty cycle curve can be configured for flexibility. To reduce the fan driver's audible noise and power loss, the MPQ6517B features a soft on/off phase commutation and an automatic phase-lock function for the motor winding back electromotive force (BEMF) and current.

Full protection features include input over-voltage protection (OVP), under-voltage lockout (UVLO), rotor deadlock protection, thermal shutdown, and input RVP.

The MPQ6517B requires a minimal number of external components to reduce solution cost, and it is AEC-Q100 grade 1 qualified. The MPQ6517B is available in TSOT23-6-SL and TSOT23-6 packages.

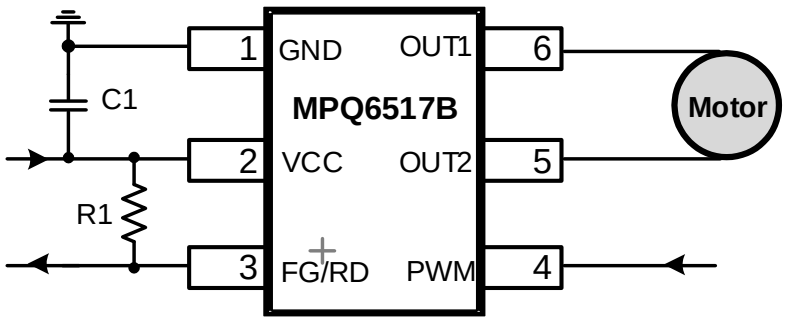
FEATURES

- Embedded Hall Sensor with High Sensitivity
- Wide 3.3V to 16V Operating Input Range
- Up to 2A Configurable Current Limit
- Integrated High-Side (HS) and Low-Side (LS) Power MOSFETs: Total 850mΩ
- Configurable Speed Curve
- Built-In, Adjustable Speed Curve Corner Duty
- Automatic Phase Lock Detection for Winding Back Electromotive Force (BEMF) and Current Zero-Crossing
- Soft On/Off Phase Commutation
- Rotational Speed Indicator (FG) Signal
- 12kHz to 48kHz PWM Input Frequency (f_{PWM}) Range
- Fixed 26kHz Output Switching Frequency (f_{SW})
- Input Line Reverse-Voltage Protection (RVP)
- Rotor Deadlock (RD) Protection with Automatic Recovery
- Thermal Protection and Automatic Recovery
- Built-In Input Over-Voltage Protection (OVP), and Under-Voltage Lockout (UVLO) with Automatic Recovery
- Available in TSOT23-6-SL and TSOT23-6 Packages
- Available in AEC-Q100 Grade 1

APPLICATIONS

- Brushless DC Motors
- Fans

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPQ6517BGJS-xxxx**-AEC1	TSOT23-6-SL	*See Below*	1
MPQ6517BGJ-xxxx**-AEC1	TSOT23-6	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MPQ6517BGJS-xxxx-AEC1-Z).

** “xxxx” is the configuration code identifier. The first four digits of the suffix (xxxx) can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number for the non-default function option. “0000” is the default value.

TOP MARKING (MPQ6517BGJS-XXXX-AEC1)

BDBY
LLL

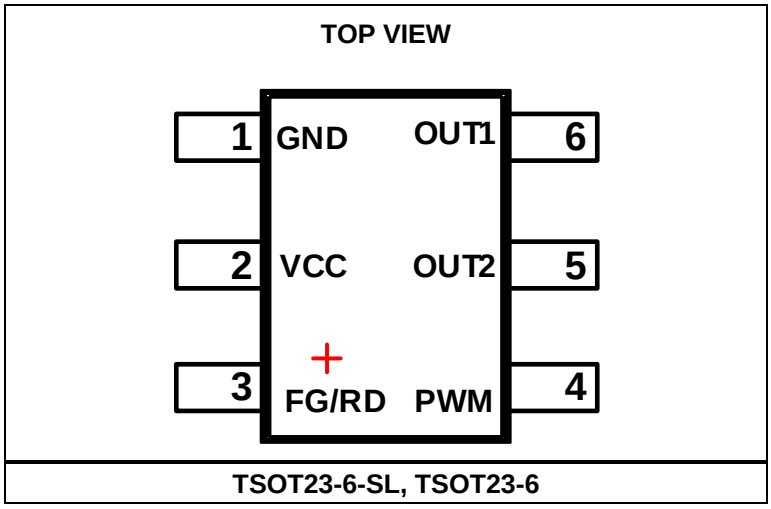
BDB: Product code
Y: Year code
LLL: Lot number

TOP MARKING (MPQ6517BGJ-XXXX-AEC1)

|BDBY

BDB: Product code
Y: Year code

PACKAGE REFERENCE



PIN FUNCTIONS

Pin #	Name	Description
1	GND	**Ground.**
2	VCC	**Input voltage supply.**
3	FG/RD	**Speed indication or rotor lock fault indication output.**
4	PWM	**Rotational speed control pulse-width modulation (PWM) input.** A PWM frequency between 12kHz and 48kHz is recommended during normal operation. PWM is internally pulled up to the internal LDO with 100kΩ of resistance.
5	OUT2	**Motor driver output 2.** The OUT2 pin is connected to the middle point of the internal N-channel MOSFET half-bridge.
6	OUT1	**Motor driver output 1.** The OUT1 pin is connected to the middle point of the internal N-channel MOSFET half-bridge.

ABSOLUTE MAXIMUM RATINGS (1)

V_{CC} ..... ±19V
FG/RD, $V_{OUT1/2}$ ..... -0.3V to V_{CC} + 0.3V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2) 1.25W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -60°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM) 750V

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 3.3V to 16V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSOT23-6 ..... 100 ..... 55... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = -40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input under-voltage lockout (UVLO) rising threshold	V_{UVLO}			3	3.25	V
Input UVLO hysteresis		Stop switching		0.15		V
		Shut down		1.1		V
Operating supply current	I_{CC}			6.5	7.8	mA
Reverse supply current	I_{CCREV}	V_{CC} = -18V			1	mA
PWM input high voltage	V_{PWMH}		1.5			V
PWM input low voltage	V_{PWML}				0.4	V
PWM input frequency	f_{PWM}		12		48	kHz
Min PWM input low-level time (5)			200			ns
PWM input internal pull-up resistance				100		kΩ
High-side (HS) MOSFET on resistance	R_{HSON}	I_{OUT} = 100mA, including reversed MOSFET		520		mΩ
Low-side (LS) MOSFET on resistance	R_{LSON}	I_{OUT} = 100mA		330		mΩ
Over-current (OC) limit protection threshold	I_{OCP}			3		A
Output current limit	I_{LMT}	SUCL = 100		1.36		A
PWM output frequency	f_{SW}	T_A = 25°C	23	26	29	kHz
FG output low-level voltage	V_{FG_L}	IFG/RD = 3mA, V_{PULL} = 5V			0.35	V
FG leakage current					1	μA
Soft turn-on angle	θ_{SON_100}	SON_100 = 10000		23.9		°
Soft turn-off angle	θ_{SOFF_100}	SOFF_100 = 11111		45		°
Adjustable delay angle	θ_E	THETA_E = 0000		0		°
Rotor-lock detection time	t_{RD}			0.6		s
Minimum recommended magnetic field (5)				±1		mT
Thermal shutdown threshold (5)				150		°C
Thermal shutdown hysteresis (5)				25		°C

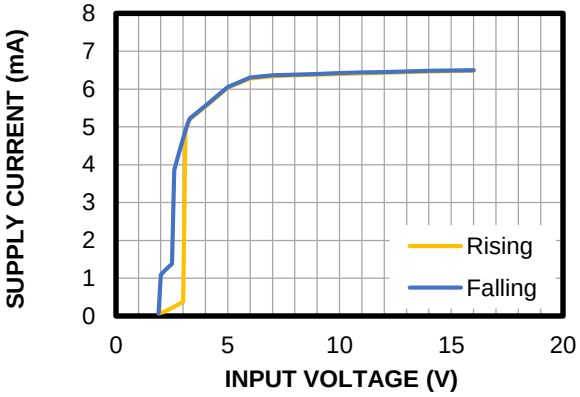
Note:

5) Guaranteed by design.

TYPICAL CHARACTERISTICS

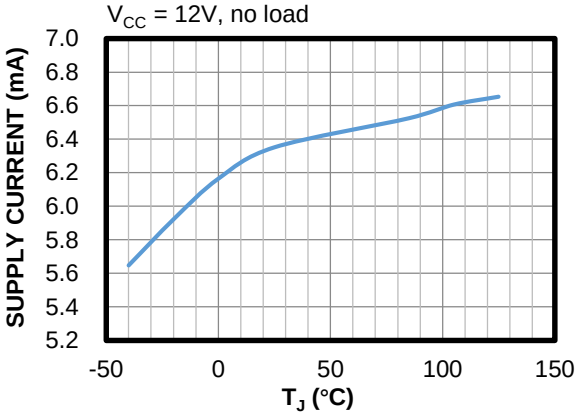
Supply Current vs. Input Voltage

V_{CC} = 2V to 16V, no load, T_J = 25°C

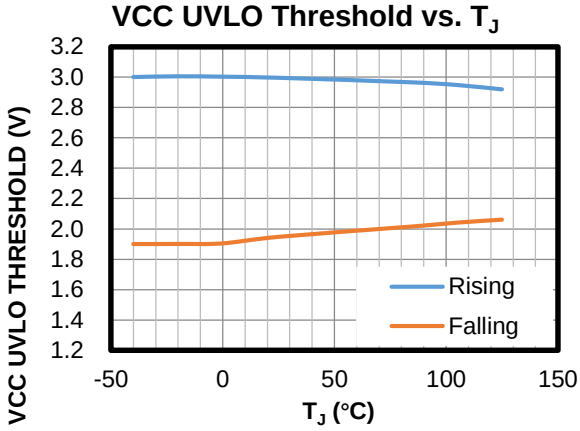


Supply Current vs. T_J

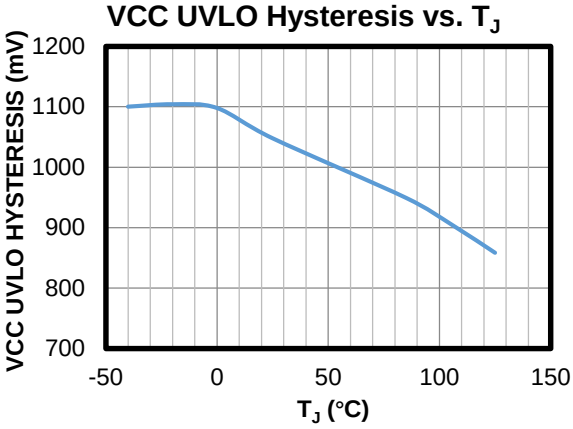
V_{CC} = 12V, no load



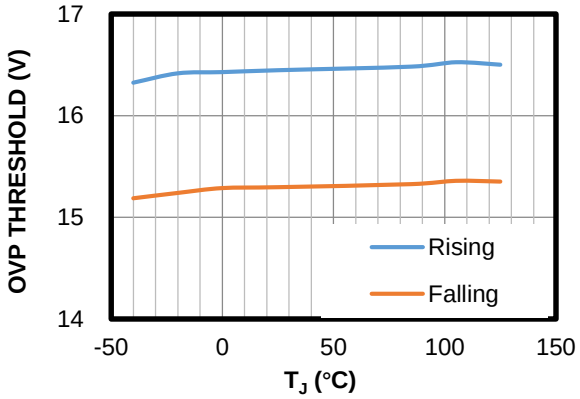
VCC UVLO Threshold vs. T_J



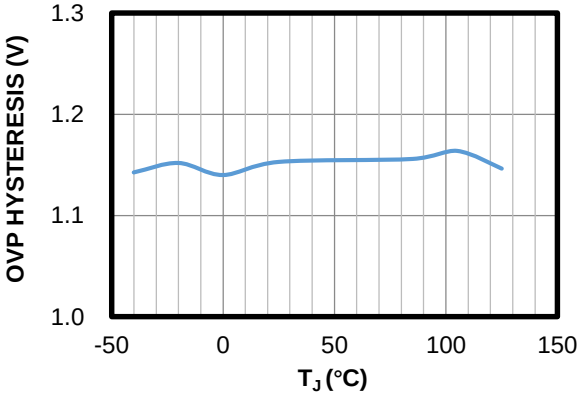
VCC UVLO Hysteresis vs. T_J



OVP Threshold vs. T_J



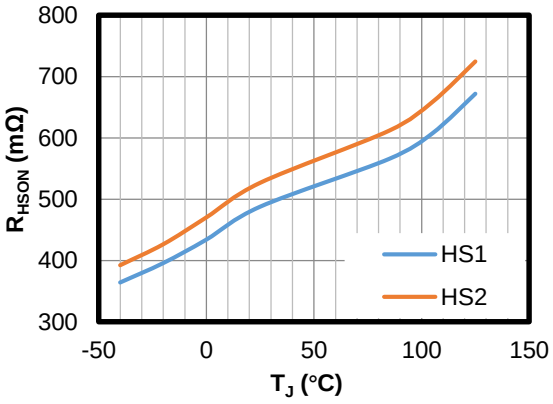
OVP Hysteresis vs. T_J



TYPICAL CHARACTERISTICS *(continued)*

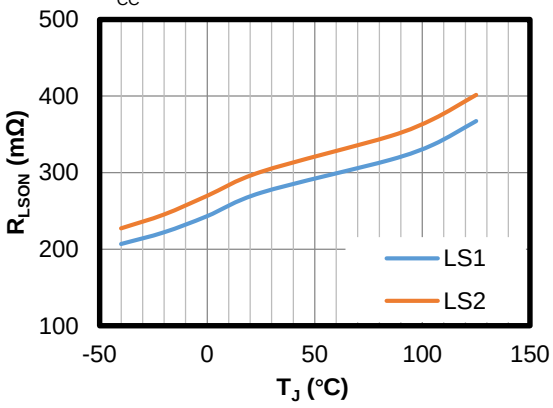
High-Side MOSFET On Resistance vs. T_J

V_{CC} = 12V

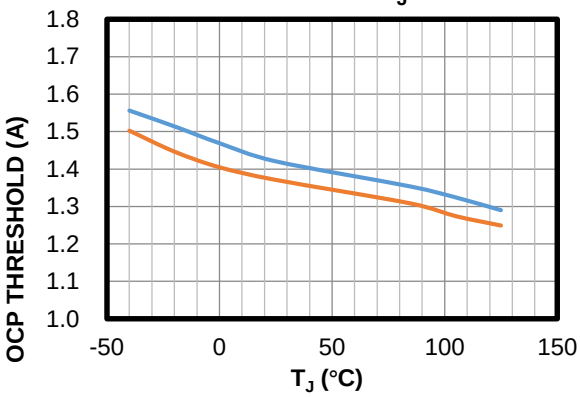


Low-Side MOSFET On Resistance vs. T_J

V_{CC} = 12V

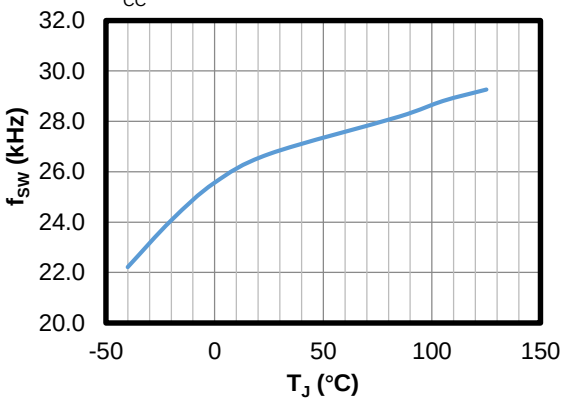


OCP Threshold vs. T_J



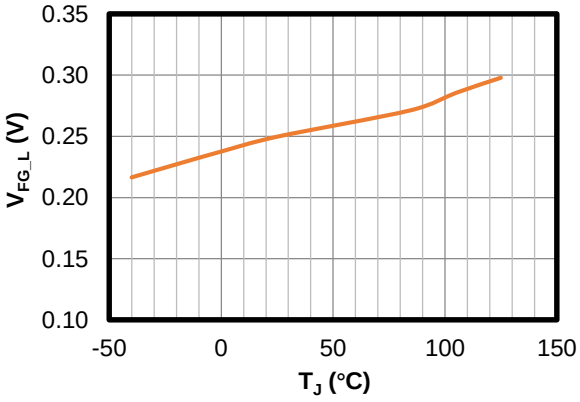
PWM Output Frequency vs. T_J

V_{CC} = 12V



V_{FG_L} vs. T_J

V_{CC} = 12V, $I_{FG/RD}$ = 3mA

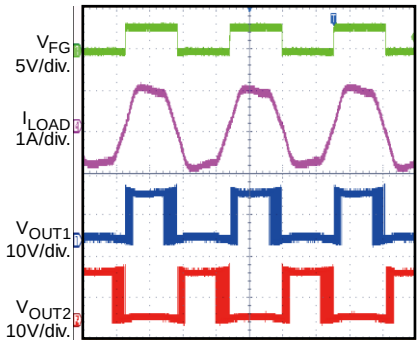


TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 12V, T_A = 25°C, tested with fan unit, unless otherwise noted.

Typical Waveform, 100% Duty Output

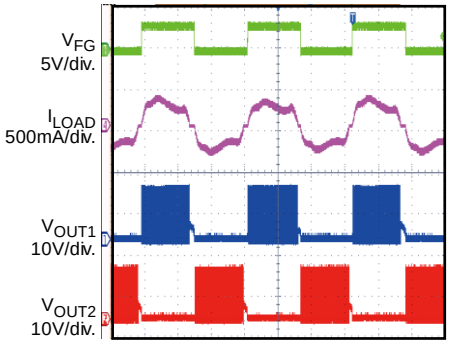
V_{CC} = 12V_{DC}, PWM = 25kHz, 100% Duty



2ms/div.

Typical Waveform, 50% Duty Output

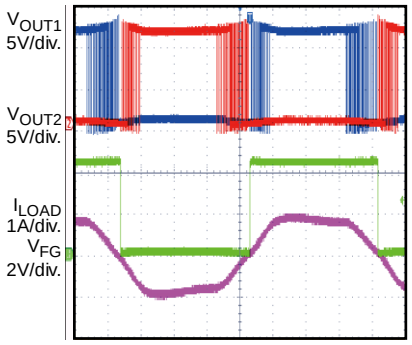
V_{CC} = 12V_{DC}, PWM = 25kHz, 50% Duty



4ms/div.

Typical Waveform, Switching Soft On and Soft Off

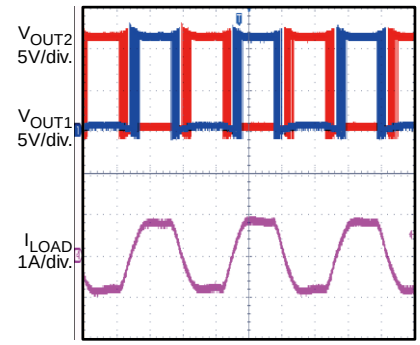
V_{CC} = 12V_{DC}, PWM = 5V_{DC}, with soft on/off phase transition



800µs/div.

Typical Waveform, Enable Soft On and Soft Off

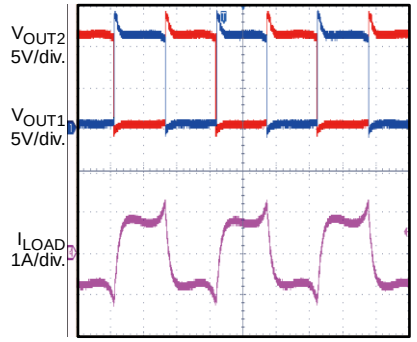
V_{CC} = 12V_{DC}, PWM = 5V_{DC}, with soft on/off phase transition



2ms/div.

Typical Waveform, Disable Soft On and Soft Off

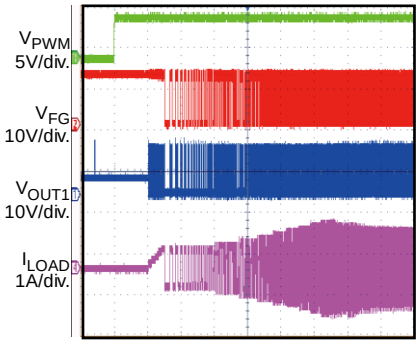
V_{CC} = 12V_{DC}, PWM = 5V_{DC}, without soft on/off phase transition



2ms/div.

Typical Waveform, Start-Up through PWM

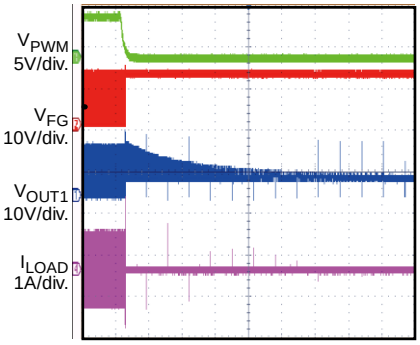
V_{CC} = 12V_{DC}, PWM = 0V_{DC} to 5V_{DC}



400ms/div.

Typical Waveform, Shutdown through PWM

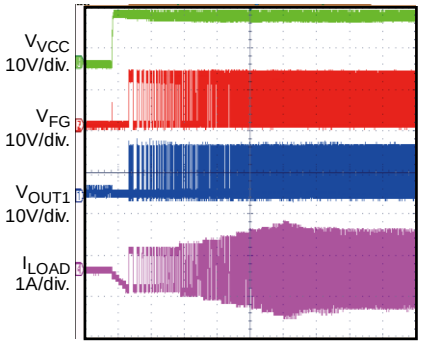
V_{CC} = 12V_{DC}, PWM = 5V_{DC} to 0V_{DC}



1s/div.

Typical Waveform, Start-Up through VCC

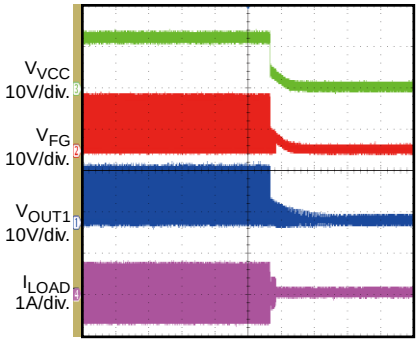
PWM = 5V_{DC}, V_{CC} = 0V_{DC} to 12V_{DC}



400ms/div.

Typical Waveform, Shutdown through VCC

PWM = 5V_{DC}, V_{CC} = 12V_{DC} to 0V_{DC}



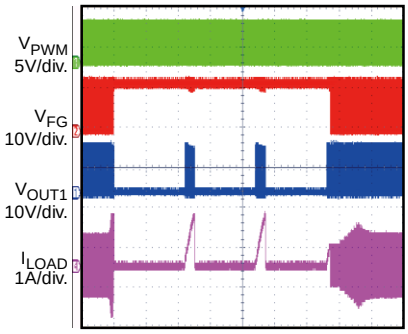
1s/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

VCC = 12V, T_A = 25°C, tested with fan unit, unless otherwise noted.

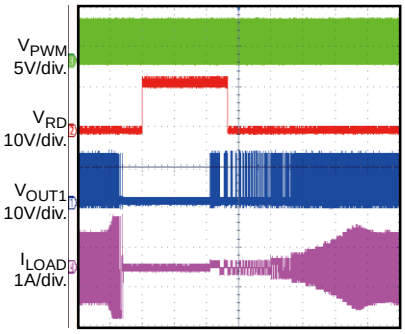
Typical Waveform, Rotor Lock and Release

V_{CC} = 12V_{DC}, PWM = 5V_{DC}, lock rotor and releaset



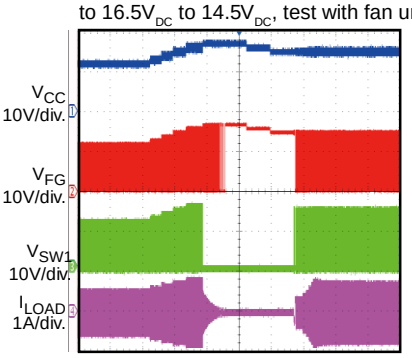
Typical Waveform, Rotor Lock and Release

V_{CC} = 12V_{DC}, PWM = 5V_{DC}, lock rotor and release



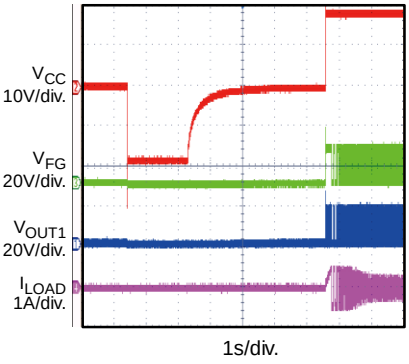
Typical Waveform, Over-Voltage Protection

PWM = 25kHz, 100% Duty, V_{CC} = 12V_{DC} to 16.5V_{DC} to 14.5V_{DC}, test with fan unit



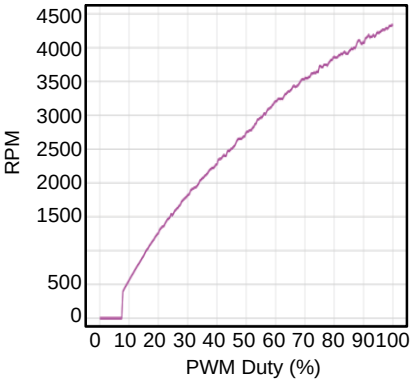
Typical Waveform, VCC Reverse Protection

VIN = 0V_{DC} to -18V_{DC} to 0V_{DC} to +18V_{DC}



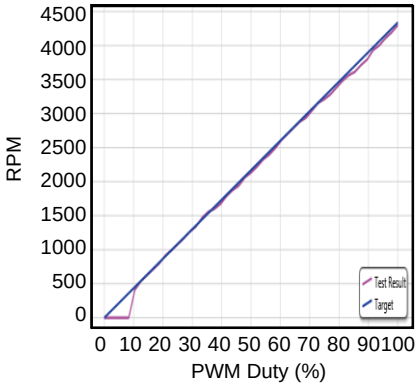
Typical Curve, RPM Output vs. PWM Input Duty

V_{CC} = 12V_{DC}, PWM = 25kHz, test with fan unit, default register setting



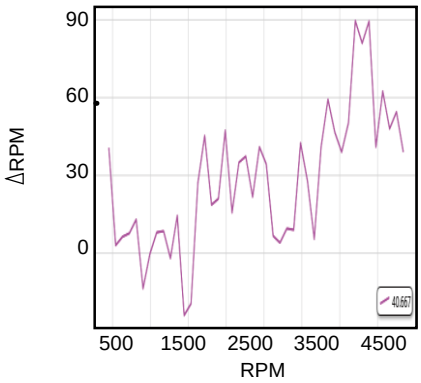
Typical Curve, RPM Output vs. PWM Input Duty

V_{CC} = 12V_{DC}, PWM = 25kHz, test with fan unit, optimized rpm curve and configured via MPS's GUI software



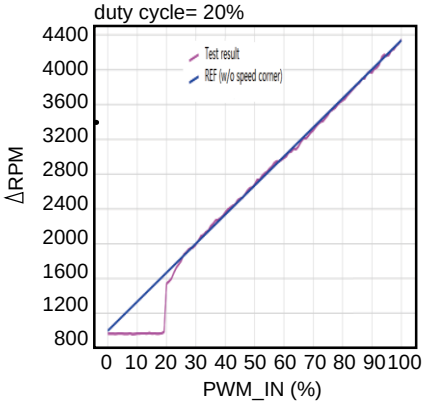
RPM Output Error vs. RPM Target

V_{CC} = 12V_{DC}, PWM = 25kHz, test with fan unit, optimized rpm curve and configured via MPS's GUI software



Typical Curve, RPM Output vs. PWM Input Duty

V_{CC} = 12V_{DC}, PWM = 25kHz, optimized rpm curve and configured via MPS's GUI software, speed corner duty cycle= 20%



FUNCTIONAL BLOCK DIAGRAM

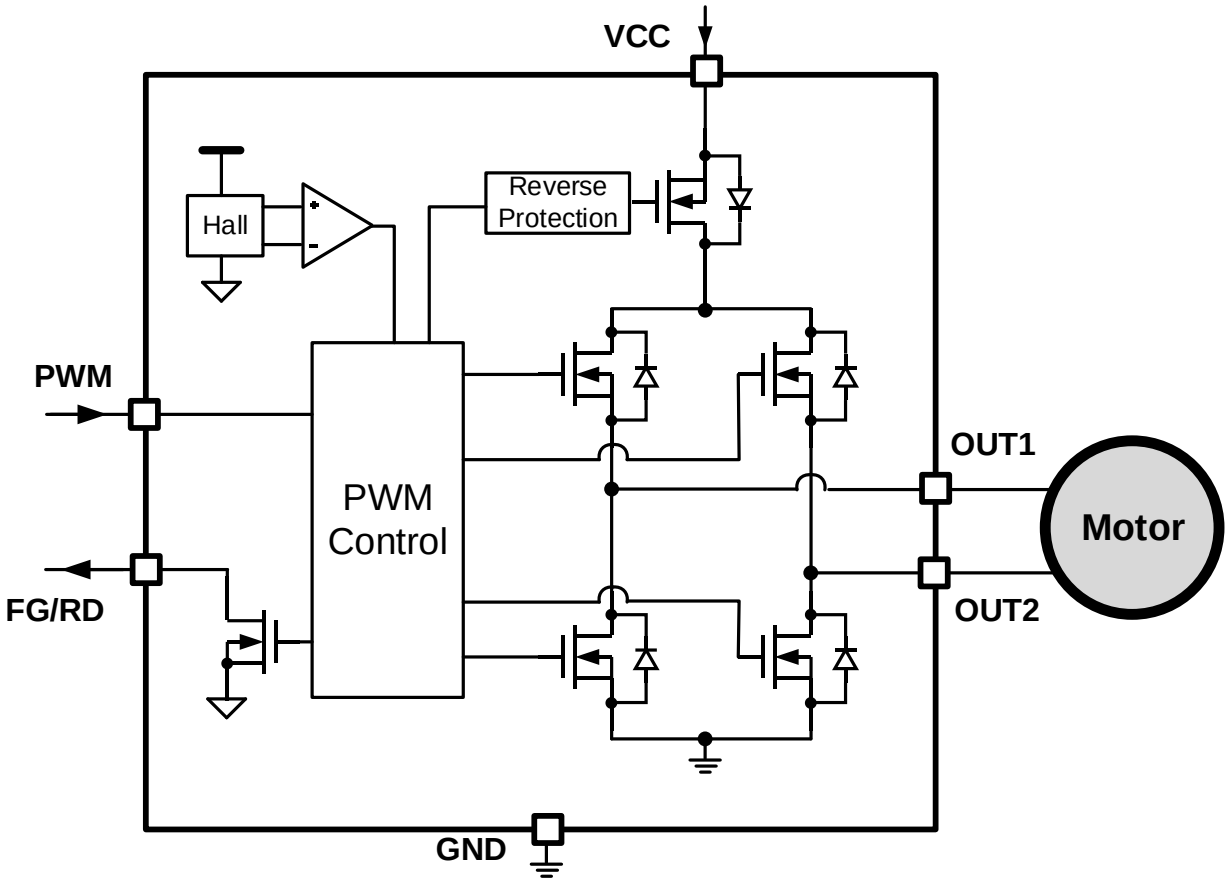


Figure 1: Functional Block Diagram

OPERATION

The MPQ6517B is a single-phase, brushless DC (BLDC) motor driver with integrated power MOSFETs and a Hall-effect sensor.

Speed Control

The MPQ6517B is controlled using a pulse-width modulation (PWM) input interface, which is compatible with industry-standard devices. The MPQ6517B detects the PWM input signal duty cycle and linearly controls the H-bridge output duty cycle, so the fan speed increases as the input duty cycle increases.

The PWM input accepts a wide input frequency (f_{PWM}) range (12kHz to 48kHz), while the output switching frequency (f_{SW}) stays constant at 26kHz above the audible frequency range.

Pulse-Width Modulation (PWM) Output Drive

The MPQ6517B controls the H-bridge MOSFET's switching to reduce speed variation and increase system efficiency (see Figure 2).

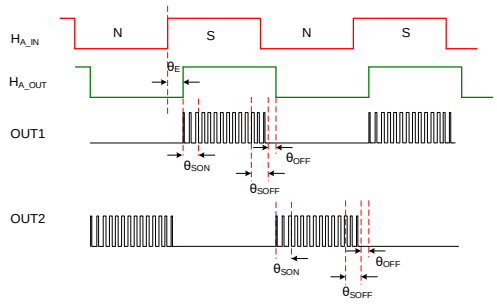


Figure 2: Timing Diagram

When the rotor magnet pole S approaches the top side of MPQ6517B, the internal Hall sensor outputs high. When the rotor magnet pole N approaches the top side of MPQ6517B, the internal Hall sensor outputs low. With this H_{A_IN} signal, the H_{A_OUT} signal is generated with a lag phase (θ_E, which can be configured between 0° and 15° via the THETA_E bits). During the H_{A_OUT} high interval, the OUT2 and OUT1 switching statuses can be divided to different timing sections, described below.

Soft Turn-On

During soft turn-on, OUT1 continues switching, and the duty cycle increases gradually from 0 to the set target duty cycle in a maximum of 16 steps. OUT2 remains low. See 'θ_{SON}' in figure 2. Determine the linear interpolation duration using the SON_100 and SON_12P5 bits. The duration ranges between 1.45° and 45° in 32 steps.

Normal PWM Switching

During normal PWM switching, OUT1 continues switching, and the duty cycle is fixed at the set target duty cycle. OUT2 remains low.

Soft Turn-Off

During soft turn-off, OUT1 continues switching, and the duty cycle decreases gradually from the set target duty cycle to 0 in a maximum of 16 steps. OUT2 remains low. See 'θ_{SOFF}' in figure 2. Determine the linear interpolation direction between the SOFF_100 and SOFF_12P5 bits, which can be between 1.45° and 45° in 32 steps.

Off

During the off time, OUT1 remains at high impedance, and OUT2 remains low. The time duration adaptively changes from 0° to 45°. In steady state, this functional block maintains the phase lock for the Hall output's falling edge and winding current zero-crossing edge.

During the interval at which the Hall output is low, the conducting phase changes, but the switching sequence remains the same.

Minimum Speed and Corner Speed Point

The minimum PWM output duty cycle is determined by the 00h register's value when the input PWM duty cycle is below the corner duty cycle set by register 14h. By setting register 00h to 0, the fan stops rotating when the PWM input duty cycle is below the corner duty cycle. By setting register 00h to a non-zero value, the fan maintains a minimum speed rotation when the PWM input duty cycle is below the corner duty cycle (see Figure 3).

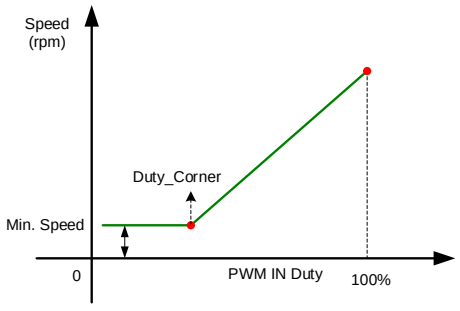


Figure 3: Configurable Speed Curve

Protection Circuits

The MPQ6517B is fully protected against over-voltage (OV), under-voltage (UV), over-current (OC), and over-temperature (OT) events, and also provides input reverse protection.

Over-Current Protection (OCP)

The MPQ6517B protects against internal overloads and short circuits by detecting the current flowing through each MOSFET. If the current flowing through any MOSFET exceeds the over-current protection (OCP) threshold after a 1.5µs of blanking time, that MOSFET turns off immediately. It needs a power recycle to reset the protection.

Overload Current Limit

If the current flowing through the high-side MOSFET (HS-FET) of the H-bridge exceeds the threshold set by the SUCL bits after a 1.5µs blanking time during normal switching, then the HS-FET turns off immediately. The HS-FET resumes switching in the next switching cycle. The overload current limit is fixed to about 1360mA by default.

To softly spin up the fan driver during start-up, the current limit increases from 0 to the configured current limit in 16 steps (see Figure 4). Each step limit value lasts for 16 internal Hall cycles. If there is a rotor lock fault, the current limit increases with 16 steps within a 600ms detection time.

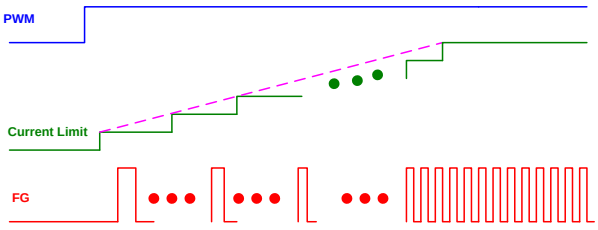


Figure 4: Start-Up Waveforms

Thermal Shutdown

Thermal monitoring is also integrated into the MPQ6517B. If the die temperature exceeds 150°C, the MOSFETs of the switching half-bridge turn off. Once the die temperature drops to a safe level, operation resumes automatically.

Under-Voltage Lockout (UVLO)

If V_{CC} falls below the under-voltage lockout (UVLO) threshold, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes once V_{CC} exceeds the UVLO threshold.

Rotor Deadlock (RD) Protection

If the FGRD bit is set to 11, the MPQ6517B detects the internal Hall signal and outputs a deadlock indication signal to FG/RD.

If the MPQ6517B cannot detect the Hall signal edge during the 0.6s detection time, both low-side MOSFETs (LS-FETs) of the H-bridge turn on. FG/RD is an open-drain output. After 1.8s, 2.4s, 3s, or 3.6s of lock-turn-off time (set by the RLOCK_SEL bits), the device attempts to start up again automatically. FG/RD output pulse again if three Hall signal edges are detected after the rotor lock condition is released (see Figure 5).

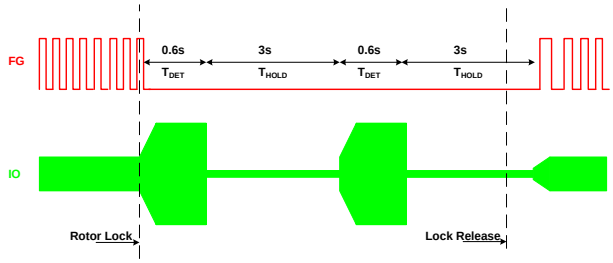


Figure 5: Rotor Deadlock Protection

Rotor Speed Indication (FG)

The MPQ6517B outputs a Hall detection signal to FG/RD for speed indication. The output signal frequency can be optional set to be 1x, 0.5x, or 2x the internal Hall sensor output frequency. FG/RD is an open-drain, so it requires a pull-up resistor in the application.

Over-Voltage Protection (OVP)

If V_{CC} exceeds the OV threshold (16.2V), the MPQ6517B turns off the two HS-FETs and turns on the two LS-FETs until V_{CC} drops below 15V. Then the device resumes normal operation.

Input Reverse-Voltage Protection (RVP)

If the input line is reverse-connected to VCC and GND, the MPQ6517B detects the fault condition automatically and shuts down to avoid damage.

Test Mode and Factory Mode

If VCC is powered, the MPQ6517B can enter test mode by sourcing 5mA to 10mA of current with an external resistor and a negative voltage for around 5ms. In test mode, all functional blocks are active, and the PWM and FG/RD pins can be used as the I²C interface to read or write the internal register bits (see Figure 6).

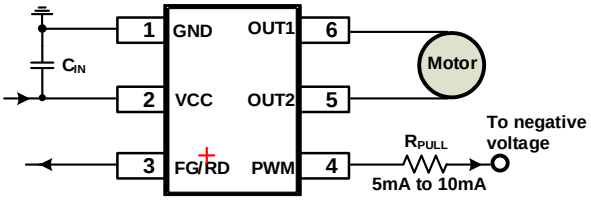


Figure 6: Test Mode Configuration

In test mode, first write the data 28h to the 11h register, and then write the data 04h to the 10h register. In factory mode, all writeable register values can be configured by the user. The MPQ6517B exits test mode or factory mode when power is cycled on VCC.

I²C Chip Address

After the start condition, the I²C-compatible master sends a 7-bit address followed by an eighth read (1) or write (0) bit. The following bit indicates the register address to which the data is written, or from which the data is read (see Figure 7).

1	0	1	0	1	0	1	R/W

Figure 7: I²C-Compatible Device Address

REGISTER MAP

Addr.	Type	D7	D6	D5	D4	D3	D2	D1	D0
00h	OTP/REG	PWMO[7:0]							
01h~08h	OTP/REG	PWMO[7:0]							
09h	OTP/REG	PROG[1:0]		PCODE[5:0]					
0Ah	OTP/REG	FGRD[1:0]		RPMS[2:0]			SUCL[2:0]		
0Bh	OTP/REG	FG	TM	HLL_CALI	SON_12P5[4:0]				
0Ch	OTP/REG	RESERVED	RESERVED	RESERVED	SON_100[4:0]				
0Dh	OTP/REG	RESERVED	SOFTEN	RESERVED	SOFF_12P5[4:0]				
0Eh	OTP/REG	RESERVED	RESERVED	RESERVED	SOFF_100[4:0]				
0Fh	OTP/REG	RESERVED	PLLEN	RLOCK_SEL[1:0]		THETA_E[3:0]			
10h	REG	RESERVED					FM	RESERVED	
11h~13h	REG	RESERVED							
14h	OTP/REG	DUTY_CORNER[7:0]							

All reserved bits must remain at their default values, unless otherwise noted.

SPEED_CURVE (0x00~0x08)

The SPEED_CURVE command sets the PWM output duty cycle for speed curve programming

Bits	Access	Bit Name	Addr	Default	Description
7:0	OTP/REG	PWMO	0x00	00000000	Output duty cycle lookup table for speed curve. The default is linear mode. Sets the minimum output duty cycle when the input duty cycle is below the corner duty cycle set by DUTY_CORNER (14h). When Reg 00h = 0, stop when the input PWM duty cycle is below the corner duty cycle. When Reg 00h is not equal to 0, keep the minimum output duty when the input PWM duty cycle is below corner duty cycle. Registers 01h~08h set the output duty cycle in every 12.5% input PWM duty cycle. It is the linear interpolation between adjacent point.
			0x01	00011111	
			0x02	00111111	
			0x03	01011111	
			0x04	01111111	
			0x05	10011111	
			0x06	10111111	
			0x07	11011111	
			0x08	11111111	

PROJECT (0x09)

The PROJECT command indicates the one-time programmable (OTP) memory flash and the project code

Bits	Access	Bit Name	Default	Description
7:6	REG	PROG	00	Indicates the OTP memory flash. 00: Not configured 01: Configured once 10: Configured twice
5:0	OTP/REG	PCODE	000000	The design's project code.

CFR_1 (0x0A)

The CFR_1 command configures the FG/RD pin, speed range, and start-up current limit.

Bits	Access	Bit Name	Default	Description
7:6	OTP/REG	FGRD	00	Selects the FG or RD output. 00: FG 01: 1/2 x FG 10: 2 x FG 11: RD
5:3	OTP/REG	RPMS	011	Selects the rotor's rpm operating range. 000: 50rpm to 800rpm 001: 100rpm to 1600rpm 010: 200rpm to 3200rpm 011: 400rpm to 6400rpm 100: 800rpm to 12800rpm 101: 1600rpm to 25600rpm 110: 3200rpm to 51200rpm
2:0	OTP/REG	SUCL	100	Sets the start-up current limit. The default value is 1360mA. 210mA/step. 000: 510mA 111: 2000mA

CFR_2 (0x0B)

The CFR_2 command indicates the FG signal and test mode, calibrates the Hall period, and sets the soft-on angle at a 12.5% PWM output duty cycle.

Bits	Access	Bit Name	Default	Description
7	REG	FG	0	Indicates the FG signal (read-only).
6	REG	TM	0	Indicates whether the device is in test mode (read-only). In test mode, turn on all functions except for the OTP flash block. If PWM is negative in power-on reset (POR), enter test mode. The TM bit is set to 1. Recycle the power to clear test mode and the TM bit. 0: Normal operation 1: Test mode
5	OTP/REG	HLL_CALI	0	Enables Hall period calibration. 1: Enabled 0: Disabled
4:0	OTP/REG	SON_12P5	11111	Sets the electrical angle to softly turn on the phase transition at a 12.5% PWM output duty cycle. The default value is 45°. 00000: 1.4° 11111: 45°

SOFT_ON/OFF_1 (0x0C)

The SOFT_ON/OFF_1 command sets the soft-on angle at a 100% PWM output duty cycle.

Bits	Access	Bit Name	Default	Description
7:5	N/A	RESERVED	N/A	Reserved.
4:0	OTP/REG	SON_100	10000	Sets the electrical angle to softly turn on the phase transition at a 100% PWM output duty cycle. The default value is 23.9°. 00000: 1.4° 11111: 45°

SOFT_ON/OFF_2 (0x0D)

The SOFT_ON/OFF_2 command enables the soft-on/off function and sets the soft-off angle at a 12.5% PWM output duty cycle.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	N/A	Reserved.
6	OTP/REG	SOFTEN	1	Enables the soft switching function. 1: Enabled 0: Disabled
5	N/A	RESERVED	N/A	Reserved.
4:0	OTP/REG	SOFF_12P5	10000	Sets the electrical angle to softly turn off the phase transition at a 12.5% PWM output duty cycle. The default value is 23.9°. 00000: 1.4° 11111: 45°

SOFT_ON/OFF_3 (0x0E)

The SOFT_OFF_3 command sets the soft-off angle at a 100% PWM output duty cycle.

Bits	Access	Bit Name	Default	Description
7:5	N/A	RESERVED	N/A	Reserved.
4:0	OTP/REG	SOFF_100	11111	Sets the electrical angle to softly turn off the phase transition at a 100% PWM output duty cycle. 00000: 1.4° 11111: 45°

CFR_3 (0x0F)

The CFR_3 command enables the load current zero-crossing phase lock, and also sets the lock turn-off time and Hall offset angle.

Bits	Access	Bit Name	Default	Description
7	N/A	RESERVED	N/A	Reserved.
6	OTP/REG	PLLEN	1	Enables the load current zero-crossing phase lock function. Note that in low-current applications, this bit may impact fan operation due to the accuracy. Verify the results in application when this function is enabled. 1: Enabled 0: Disabled
5:4	OTP/REG	RLOCK_SEL	11	Sets the rotor lock turn-off time to the detection time ratio. 00: 1:3 (0.6s/1.8s) 01: 1:4 (0.6s/2.4s) 10: 1:5 (0.6s/3.0s) 11: 1:6 (0.6s/3.6s)
3:0	OTP/REG	THETA_E	0000	Sets the electrical angle delay between the original Hall signal positive edge and the output current zero-crossing positive edge. 1° per step. 0000: 0° 1111: 15°

FM_MODE (0x10)

The FM_MODE command enables factory mode.

Bits	Access	Bit Name	Default	Description
7:3	N/A	RESERVED	N/A	Write this bit to 00000 when doing OTP configurations.
2	REG	FM	0	Factory mode enable.
1:0	REG	RESERVED	00	Write this bit to 00 when not in use.

OTP_CONFIGURATION (0x11)

The OTP_CONFIGURATION command is used for OTP configurations.

Bits	Access	Bit Name	Default	Description
7:0	N/A	RESERVED	N/A	Write 28h to this register first before doing OTP configurations.

RESERVED (0x12~0x13)

The RESERVED command is reserved

Bits	Access	Bit Name	Default	Description
7:0	N/A	RESERVED	N/A	Reserved.

CORNER_DUTY (0x14)

The CORNER_DUTY command sets the input PWM corner duty cycle.

Bits	Access	Bit Name	Default	Description
7:0	OTP/REG	DUTY_CORNER	00000000	Sets the speed corner duty cycle point. The output duty cycle stays at the value set by register 00h when the input duty cycle is below the duty cycle set by DUTY_CORNER. FFh: 100% ... 00h: 0%

APPLICATION INFORMATION

Selecting the Input Capacitor

Place an input capacitor (C1) near VCC to keep V_{IN} stable and reduce input switching voltage noise and ripple.

C1's impedance must be low at f_{SW}. Ceramic capacitors with X7R dielectrics are recommended for their low-ESR characteristics.

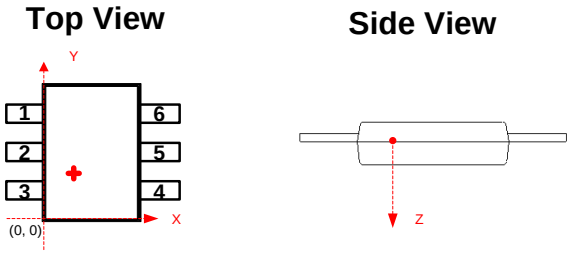
Ensure that the ceramic capacitance depends on the voltage rating. The DC biased voltage and value can drop by much as 50% at the rated voltage rating. Leave a sufficient voltage rating margin when selecting C1. For most applications (<500mA), a 2.2µF to 10µF ceramic capacitor is sufficient. In some applications, it may be required to add an additional, high capacitance, electrolytic capacitor that can absorb inductor energy.

Selecting the PWM Input Resistor

When the input PWM signal rating is >6.5V (which exceeds the PWM voltage rating), a resistor (R2) is required. The recommended value for R2 is 5.1kΩ.

Hall Sensor Position

The Hall sensor cell is located in the lower left corner of the package (see Figure 8).



(X, Y, Z) = (540µm, 508µm, 80µm)

Figure 8: Hall Sensor Position

Selecting the Input-Clamping TVS Diode

To avoid high-voltage spikes caused by the energy stored in the motor inductor when the inductor charges back to the input capacitor side, add a voltage-clamping transient voltage suppressor (TVS) diode. For a 12V application, a 18V TVS diode in a SOD-323 package is sufficient. If input reverse connection protection is required, it is recommended to use a unidirectional zero voltage switching (ZVS) diode (see Figure 11 on page 18). For small power fans that are shorter than 80cm (<500mA), the additional ZVS diode is not required.

Selecting the Input Snubber

Due to the input capacitor's charge/discharge energy during soft-switching phase transitions, the input current has switching cycle ringing. If required, add a 2Ω resistor in series with a 1µF capacitor (which act together as an RC snubber) in parallel to the input capacitor. This effectively prevents switching cycle ringing (see Figure 10 on page 18).

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 9 and follow the guidelines below:

1. Place the input capacitor (C1) close to the VCC and GND pins.
2. Add an additional, small-package ceramic capacitor (C2) as close to the VCC and GND pins as possible to absorb high-frequency noise. The recommended package size is 0402.

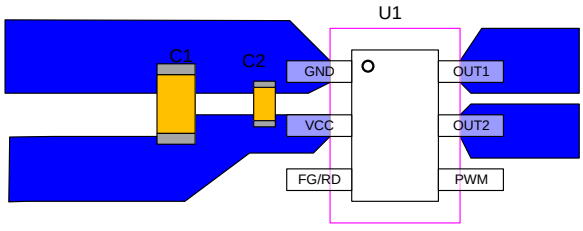


Figure 9: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

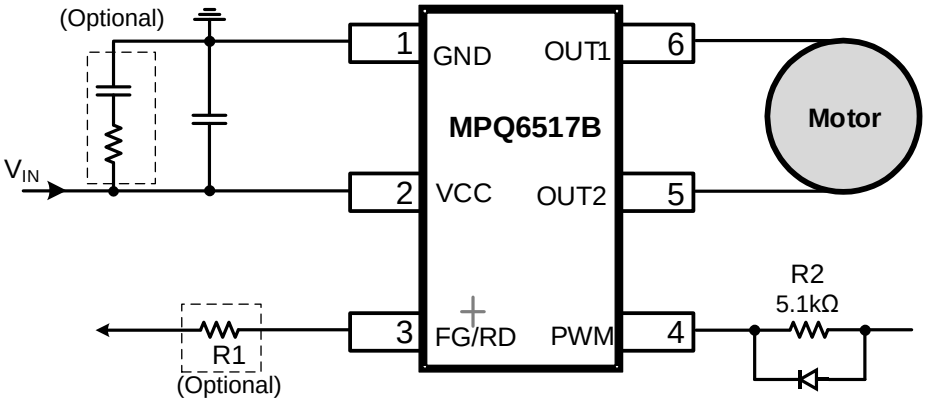


Figure 10: Typical Application Circuit with RC Snubber

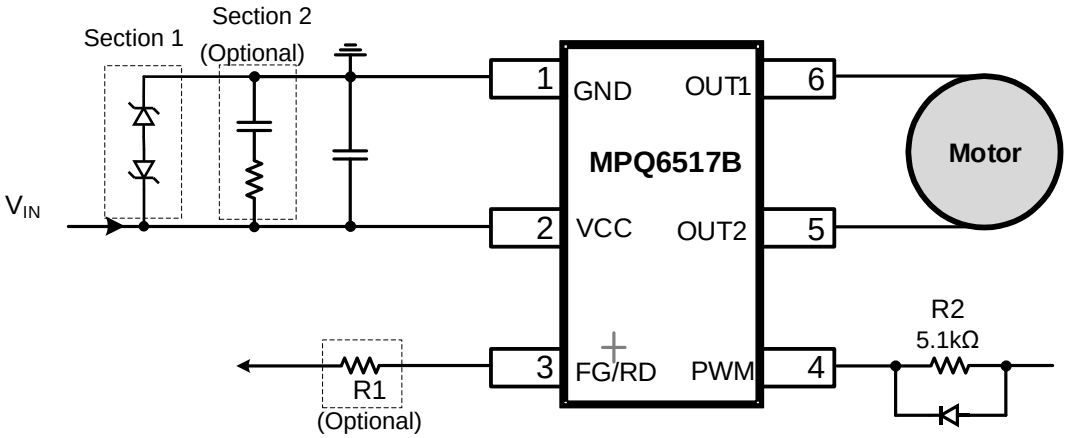
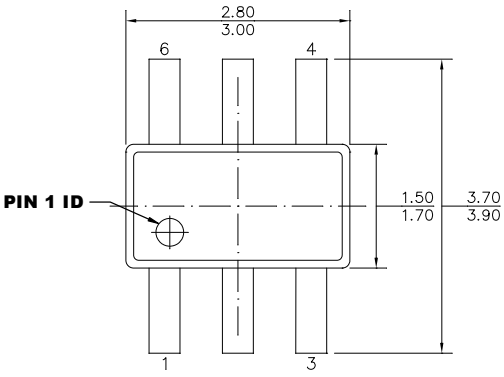


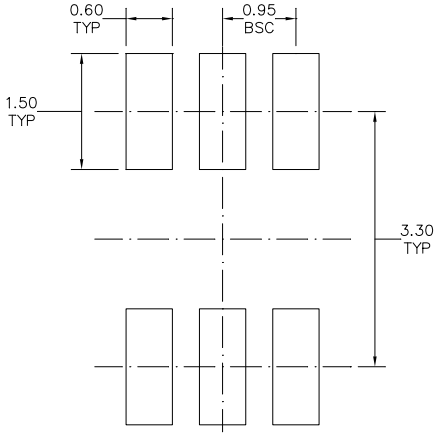
Figure 11: Typical Application Circuit with ZVS Diode

PACKAGE INFORMATION

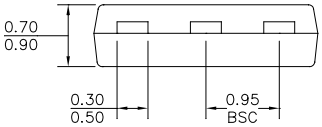
TSOT23-6-SL



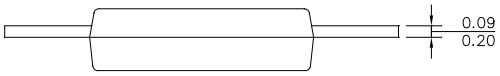
TOP VIEW



RECOMMENDED LAND PATTERN



FRONT VIEW



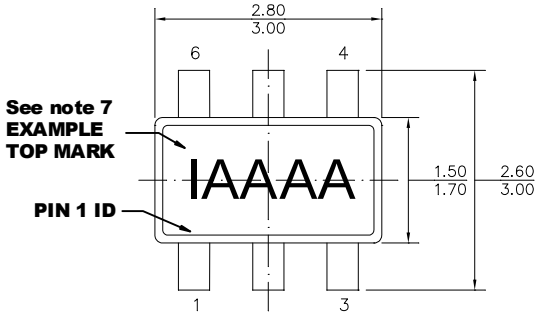
SIDE VIEW

NOTE:

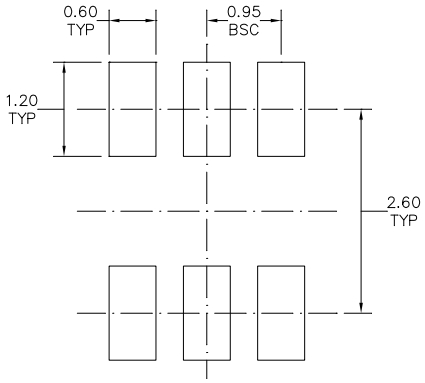
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION, OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING REFERENCE IS JEDEC MO-193,
6) DRAWING IS NOT TO SCALE.

PACKAGE INFORMATION *(continued)*

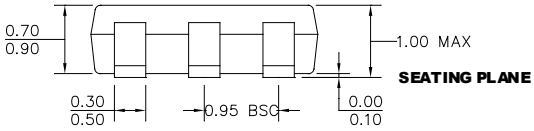
TSOT23-6



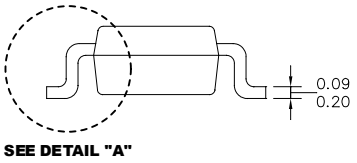
TOP VIEW



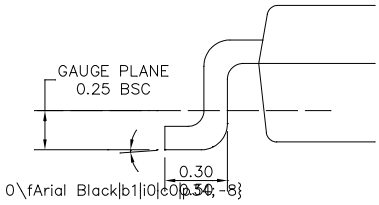
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

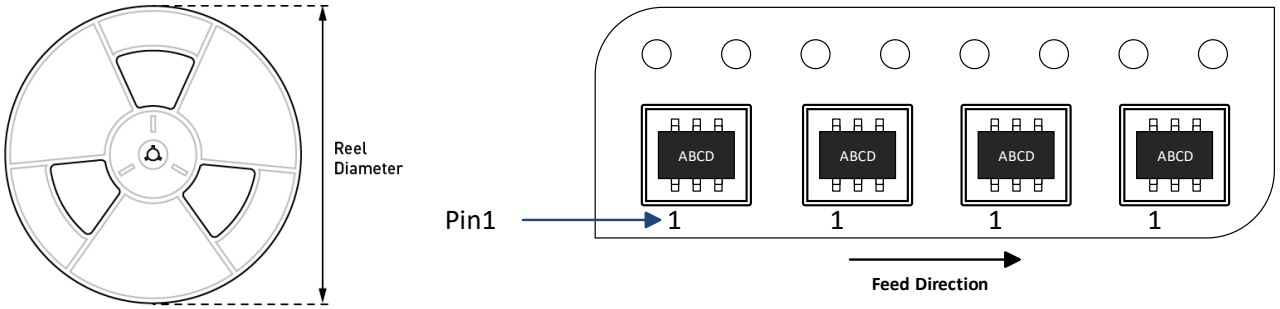


DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-193, VARIATION AB.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ6517BGJS-xxxx-AEC1	TSOT23-6-SL	5000	N/A	N/A	13in	12mm	8mm
MPQ6517BGJ-xxxx-AEC1	TSOT23-6	3000	N/A	N/A	7in	8mm	4mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	2/14/2023	Initial Release	-
1.1	9/18/2023	Added the TSOT23-6 package option (MPQ6517BGJ) to the Description and Features sections	1
		Added the TSOT23-6 package option (MPQ6517BGJ) to the Ordering Information and Top Marking sections	2
		Added the TSOT23-6 package to the Package Information section	20
		Added the TSOT23-6 package option (MPQ6517BGJ) to the Carrier Information section	21